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Low cost digital signal generation for driving space vector PWM inverter

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KEYWORDS

Pulse-width modulation (PWM);
Space vector PWM (SVPWM);
Voltage source inverter (VSI)

Abstract There is an increasing trend of using space vector pulse-width modulation (SVPWM) schemes for driving voltage source inverters because of their easier digital realization and better DC bus utilization. This paper introduces an SVPWM technique based on a reduced computation method, which is much simpler and more executable than conventional means without lookup tables or complex logical judgments. The SVPWM scheme is modeled and simulated using MATLAB SIMULINK and experimentally implemented and verified on microchip PIC microcontroller 18F4431 platform. The experimental results are presented for three-phase two-level inverter followed by three-phase LC filter.

1. Introduction

Voltage source inverters (VSIs) are increasingly applied in many industrial applications such as motor drives, uninterruptible power supplies (UPSs), frequency converters, and active filters [1,2]. The main job of voltage source inverters is to synthesize AC output voltage and frequency from a constant DC voltage via pulse-width modulation technique. Pulse-width modulation (PWM) techniques have been studied extensively during the last few decades. A large variety of methods, differing in concept and performance, have been developed to achieve the following aims: wide linear modulation range, fewer switching losses, less total harmonic distortion (THD), easy implementation, and less computation time [3,4].

Driving voltage source inverter is made by one of two popular PWM approaches, namely the sinusoidal PWM approach (SPWM) or space vector PWM approach (SVPWM). In SPWM technique, the reference modulation wave is compared with a triangular carrier wave, and the intersections define the switching instants. Within every carrier cycle, the average value of the output voltage becomes equal to the reference value. In SVPWM scheme, the reference voltage space vector is realized by switching between the nearest three inverter voltage space vectors which form the sector in which the reference vector resides. Each of the combined inverter voltage space vector is realized by switching a combination of the individual inverter voltage space vectors [5].

Many methods have been developed to implement the SVPWM for driving VSI's. Generally, the SVPWM implemen-

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tation involves sector identification, switching time calculation, switching vector determination, and optimum-switching-sequence selection for the inverter voltage vectors [6,7]. Sector identification can be done by coordinate transformation [8,9,10] or by repeated comparison of the three-phase reference voltages as introduced in [6,11]. The lookup tables can be used for determining the switching vectors in best switching sequence [12]. Calculating the duration of the switching vectors can be simplified by mapping the sector of the multilevel inverter to a corresponding sector of the two-level inverter [13,14].

The objective of this paper is to introduce a simplified SVPWM technique in which the inverter leg switching times are directly obtained from the instantaneous sampled reference phase voltages, and the inverter switching vectors are generated automatically. This method is much simpler and more executable than conventional means without lookup tables or complex logical judgments. In addition, an objective of this paper is to introduce a practical SVPWM inverter design based on a low cost microcontroller. The practical design is modeled using the MATLAB SIMULINK software package and experimentally implemented on the low cost microchip PIC microcontroller 18F4431 platform.

2. Two-level voltage source inverter

Voltage source inverter (VSI) is the most widely utilized device with power ratings ranging from fractions of a kilowatt to megawatt level. The major purpose of the PWM inverter is to generate a variable-voltage variable-frequency (VVVF) three-phase voltage from a DC voltage.

The circuit model of a typical two-level inverter is as shown in Fig. 1. S1–S6 are the six power switches that shape the output, and these are controlled by the signal to terminals a, à, b, b̀, c, and c̀. It is assumed that S1, S2, S3, and S4 as well as S5 and S6 are switched in a complementary way. There are only eight possible switching vectors. Six out of these eight vectors produce a non-zero voltage and are known as non-zero switching states. The remaining two vectors produce zero output voltage and known as zero switching states. The inverter output voltage is composed of these eight switching states. The six active vectors divide the space vector plane into six equal sized sectors of 60° with equal magnitude which forms an origin centered hexagon, and two zero space vectors found at the origin as shown in Fig. 2. The hexagon is the maximum boundary of the space vector, and the circle is the trajectory of the regular sinusoidal outputs in linear modulation. Table 1 lists all of the possible switching vectors and the respective line to line/line to neutral voltages.

To obtain a sinusoidal waveform from the VSI, a voltage reference V_{ref} is provided in terms of a revolving space vector. The magnitude and the frequency of the fundamental component are specified by the magnitude and frequency, respectively, of the reference vector. The reference vector is sampled once in every sub-cycle. The inverter is maintained in different states for appropriate durations such that an average voltage vector equal to the sampled reference vector is generated over a given sub-cycle.

3. Basic principle of space vector PWM

In space vector approach, the inverter states used are the two zero states and the two active states, whose voltage vectors are the closest to the commanded voltage vector. SVM algorithm has four switching rules: (a) the trajectory of $\overline{V}_{ref}$ should be a circle, (b) only one switching per state transition, (c) not more than three switching in one sampling period, and (d) The final state of one sample must be the initial state of the next sample.

These rules help in limiting the number of switching actions, and therefore, there is a decrease in the switching losses. In addition, they maintain symmetry in switching waveforms at the VSI output to achieve the lower THD [15]. For example, for a commanded vector in sector 1 as shown in Fig. 3, we

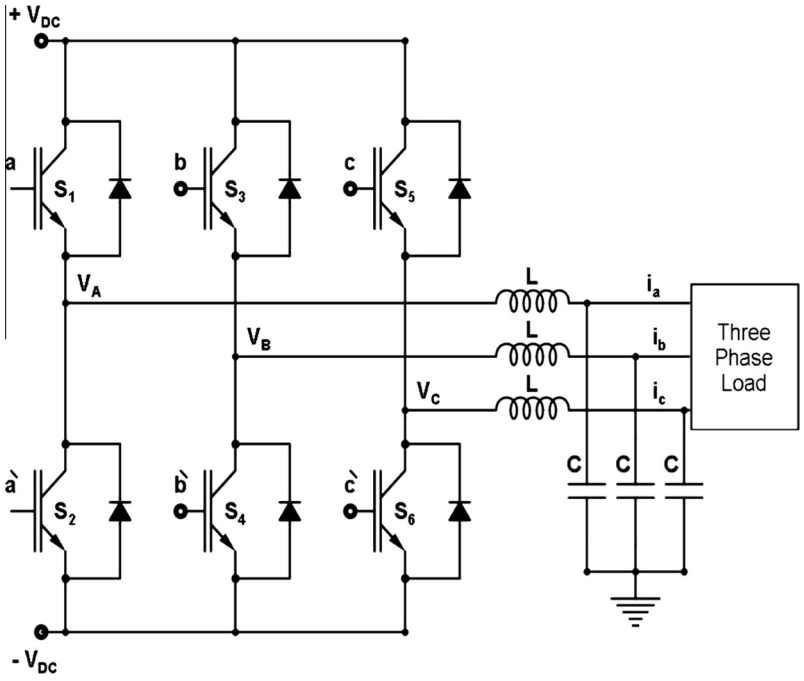


Figure 1 Two-level voltage source inverter.

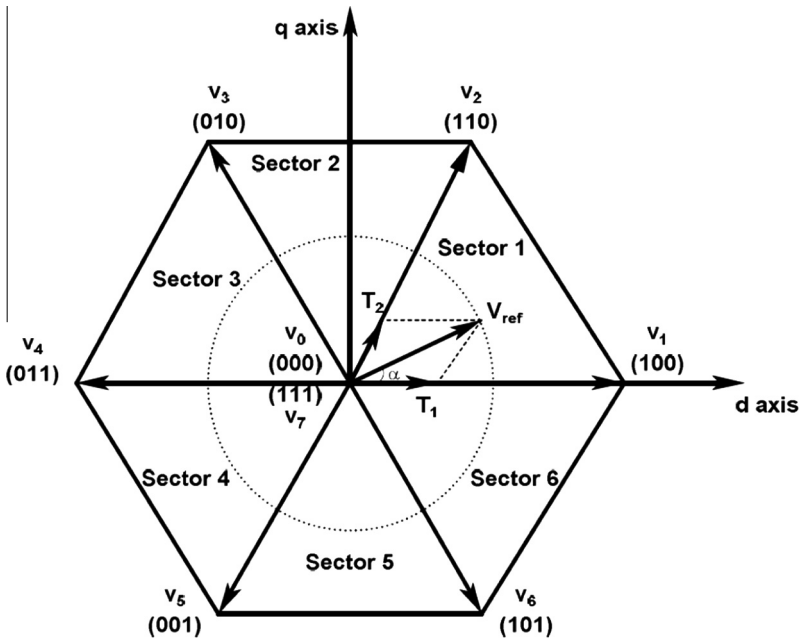


Figure 2 Output voltage space of the two-level inverter in dq coordinates.

Table 1 possible switching vectors, phase voltage, and output line to line voltage.

Voltage vectors	Switching vectors			Pole voltage			Line voltage		
	a	*b*	*c*	V_{ao}	V_{bo}	V_{co}	V_{ab}	V_{bc}	V_{ca}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	−1/3	−1/3	1	0	−1
V_2	1	1	0	1/3	1/3	−2/3	1	0	−1
V_3	0	1	0	−1/3	2/3	−1/3	−1	1	0
V_4	0	1	1	−2/3	1/3	1/3	−1	0	1
V_5	0	0	1	−1/3	−1/3	2/3	0	−1	1
V_6	1	0	1	1/3	−2/3	1/3	1	−1	0
V_7	1	1	1	0	0	0	0	0	0

All the respective voltage should be multiplied by V_{DC}.

assume that during the sampling interval T_s, the reference voltage $\overline{V}_{ref}$ remains steady, and then the switching states 0, 1, 2, and 7 can be used. Implementing the conventional SVPWM using the SVM rules $\overline{V}_{ref}$ can be expressed as follows:

$$\overline{V}_{ref} = \left(\frac{T_1}{T_s} \times \overline{V}_1\right)\left(\frac{T_2}{T_s} \times \overline{V}_2\right)\left(\frac{T_{0/7}}{T_s} \times \overline{V}_{0/7}\right) \quad (1)$$

Eq. (1) means the inverter is in active state 1 for a period T_1, and it is in active state 2 for a period T_2. For the remaining time of the sampling interval period T_s, there is no voltage applied. This can be achieved by applying inactive state 0 or 7 for the remaining time T_0 or T_7.

To generate this vector in an average sense, the durations for which the active state 1, the active state 2, and the two zero states together must be applied which are given by T_1, T_2, and T_Z, respectively, obtained as:

$$T_1 = \overline{V}_{ref} \sin(60° - \propto) \quad (2)$$

$$T_1 = \overline{V}_{ref} \sin(\propto) / \sin(60°) \quad (3)$$

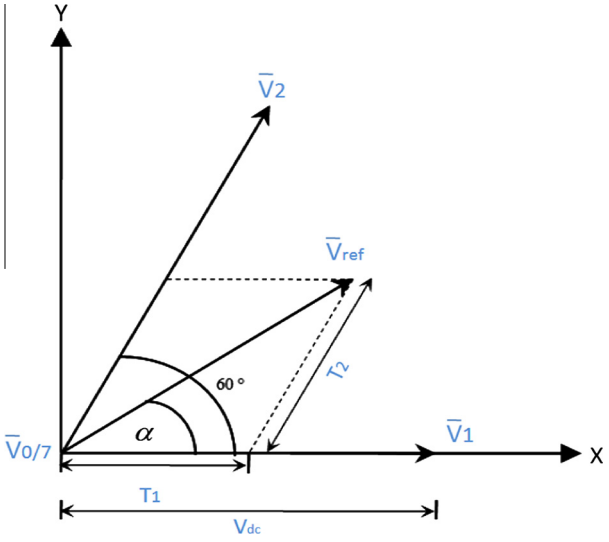


Figure 3 Reference vector in sector 1.

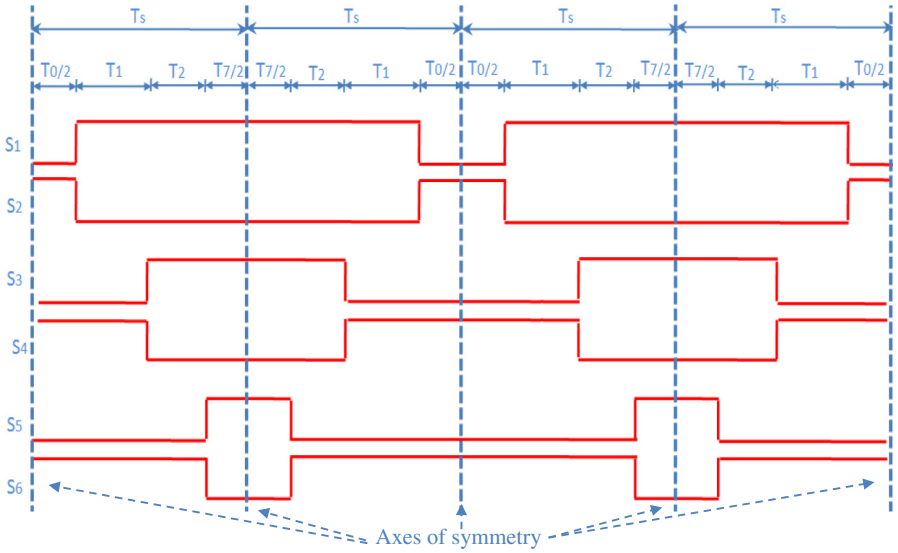


Figure 4 Typical VSI switching waveforms in sector 1.

$$T_z = T_s - T_1 - T_2 \tag{4}$$

where α is the angle of rotating vector $\overline{V}_{ref}$.

The division of the duration T_Z between the two zero vectors T_0 or T_7 is a degree of freedom in the space vector approach. This division of T_Z in a sub-cycle is equivalent to adding a common mode component to the three-phase average pole voltages. The typical VSI switching waveforms in sector 1, as defined in Eq. (1), are as given in Fig. 4. Realization of conventional SVPWM involves the following steps: (1) Coordinate transformation for the reference vector $\overline{V}_{ref}$ from rotating reference frame to stationary reference frame. (2) Determine time durations T_1, T_2, and T_0 (3) Determine the switching time of each transistor (S1–S6).

4. SVPWM using a reduced computation method

This method is based on the principle of equivalence of SVPWM with sinusoidal PWM (SPWM) and can generate the SVPWM signals directly from the instantaneous reference phase voltages. In the sinusoidal PWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier, and the individual pole voltages are generated independently of each other [3]. To obtain the maximum possible peak amplitude of the fundamental phase voltage in linear modulation, a common mode voltage V_{offset} is added to the reference phase voltages [17,19], where the magnitude of V_{offset} is given by

$$V_{offset} = -(V_{\max} + V_{\min})/2 \tag{5}$$

In Eq. (5), $V_{\max}$ is the maximum magnitude of the three sampled reference phase voltages, while $V_{\min}$ is the minimum magnitude of the three sampled reference phase voltages. In a sampling interval, the addition of the common mode voltage V_{offset} results in the active inverter switching vectors being centered in a sampling interval, making the SPWM technique equivalent to the SVPWM technique [3].

Eq. (5) is based on the fact that in a sampling interval, the reference phase which has lowest magnitude (termed the min-phase) crosses the triangular carrier first and causes the first transition in the inverter switching state, while the reference phase which has the maximum magnitude (termed the max-phase) crosses the carrier last and causes the last switching transition in the inverter switching states in a two-level SVPWM scheme [16,17]. Thus, the switching periods of the active vectors can be determined from the (max-phase and min-phase) sampled reference phase voltage amplitudes in a two-level inverter scheme [18]. The idea behind this SVPWM technique is to determine the sampled reference phase, from the three sampled reference phases, which crosses the triangular first (first-cross) and the reference phase which crosses the triangular carrier last (third-cross). This SVPWM technique presents a simple way to determine the time instants at which the three reference phases cross the triangular carriers using only the instantaneous reference phase amplitudes. These time instants are sorted to find the offset voltage [19,20]. This voltage is then added to the reference phase voltages, so the middle inverter switching vectors are centered (during a sampling interval), as in the conventional two-level SPWM scheme [21].

Implementing this SVPWM method for driving a two-level VSI involves three steps:

A. Read the sampled reference phase amplitudes of V_{AN}, V_{BN}, and V_{CN} for the present sampling interval and then calculate the time equivalents of phase voltages, that is, T_{as}, T_{bs}, and T_{cs} as:

$$T_{as} = V_{AN} \times \frac{T_s}{V_{DC}} \tag{6}$$

$$T_{bs} = V_{BN} \times \frac{T_s}{V_{DC}} \tag{7}$$

$$T_{cs} = V_{CN} \times \frac{T_s}{V_{DC}} \tag{8}$$

where T_s is the sampling time period, and V_{DC} is the DC link voltage across inverter terminals.

B. Find T_{offset} as:

$$T_{offset} = 0.5T_s - 0.5(T_{\max} + T_{\min}) \tag{9}$$

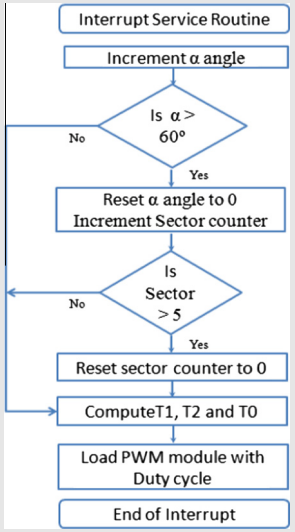
Conventional SVPWM	SVPWM based on equivalence with SPWM
Generates the gating drive signals using switching rules as listed below:	The gating drive signals are generated directly from the instantaneous samples of the reference phase amplitudes

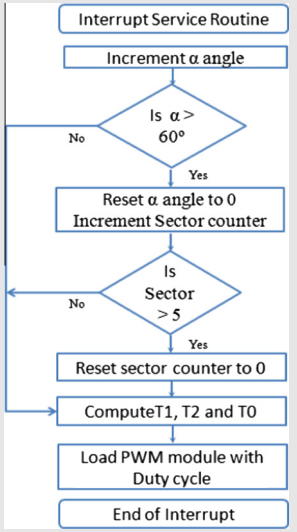
Sector	T_{ga}	T_{gb}	T_{gc}
1	$T_0/2$	$T_0/2 + T_1$	$T_S - T_0/2$
2	$T_0/2 + T_2$	$T_0/2$	$T_S - T_0/2$
3	$T_S - T_0/2$	$T_0/2$	$T_0/2 + T_1$
4	$T_S - T_0/2$	$T_0/2 + T_2$	$T_0/2$
5	$T_0/2 + T_1$	$T_S - T_0/2$	$T_0/2$
6	$T_0/2$	$T_S - T_0/2$	$T_0/2 + T_2$

Needs sector identification to define the switching rules in each sector
Needs V_{ref} and α angle information
Uses lookup tables for switching time calculations.

It needs no sector identifications
V_{ref} and α angle information is not needed
Do not use any lookup tables for switching time calculations

Digital implemntation





When the microcontroller is running at 20 MHz, this routine consumes processing time = 25.3 μs
This means:
- High CPU usage
- High execution time
- Big code size

When the microcontroller is running at 20 MHz, this routine consumes processing time = 15.2 μs
This means:
- Low CPU usage
- Low execution time
- Small code size

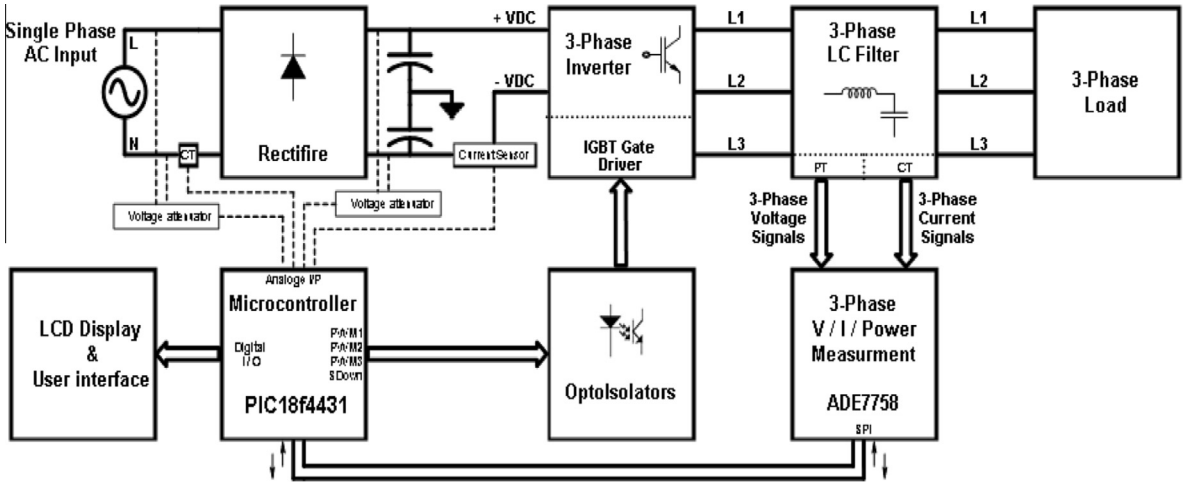


Figure 5 Overall block diagram of the experiment.

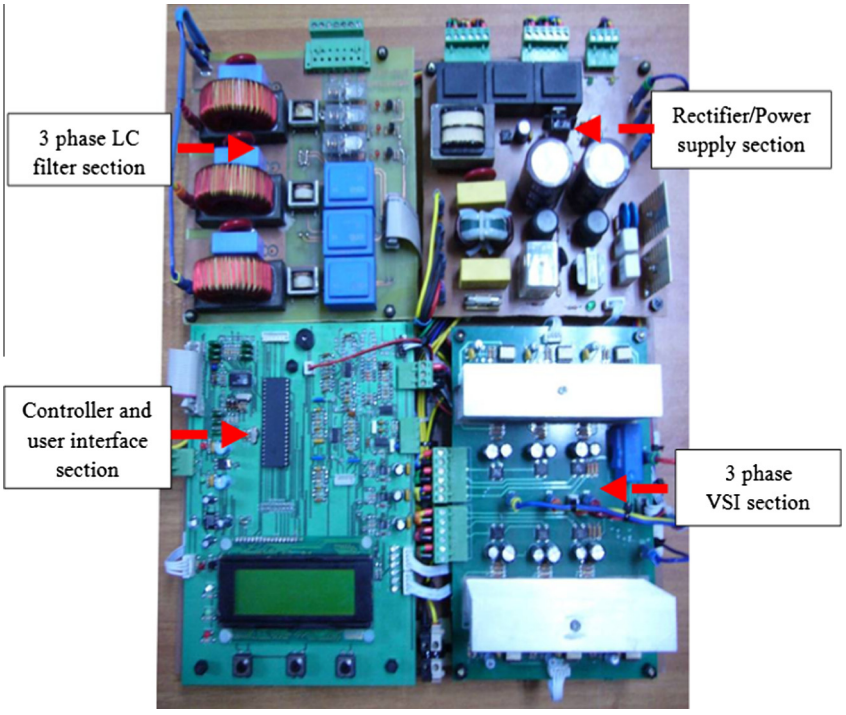


Figure 6 Real image for the experiment.

where $T_{\max}$, $T_{\min}$ are the maximum and minimum of T_{as}, T_{bs}, and T_{cs}.

C. Find T_{ga}, T_{gb} and T_{gc} as:

$$T_{ga} = T_{as} + T_{offset} \tag{10}$$

$$T_{gb} = T_{bs} + T_{offset} \tag{11}$$

$$T_{gc} = T_{cs} + T_{offset} \tag{12}$$

where T_{ga}, T_{gb}, and T_{gc} are the gating signals during which the top switches in a leg are turned on.

Eqs. (6)–(12) show that the centering of the middle inverter switching vectors of the SVPWM was achieved by the addition of an offset time signal to the inverter gating signals derived from the sampled amplitudes of the reference phase voltages which reduce the computation time required to determine the switching times for inverter legs, making the algorithm suitable for real-time implementation. Furthermore, the complicated calculations for inverter switching vector times and lookup tables for selecting the inverter switching vector which was found in conventional means are avoided in this scheme. A comparison between the conventional SVPWM algorithm and the SVPWM based on equivalence with SPWM is introduced below:

5. Experimental setup

5.1. Hardware

The practical work is as shown in Fig. 5. The input stage consists of a dual half bridge diode rectifier, which provides the

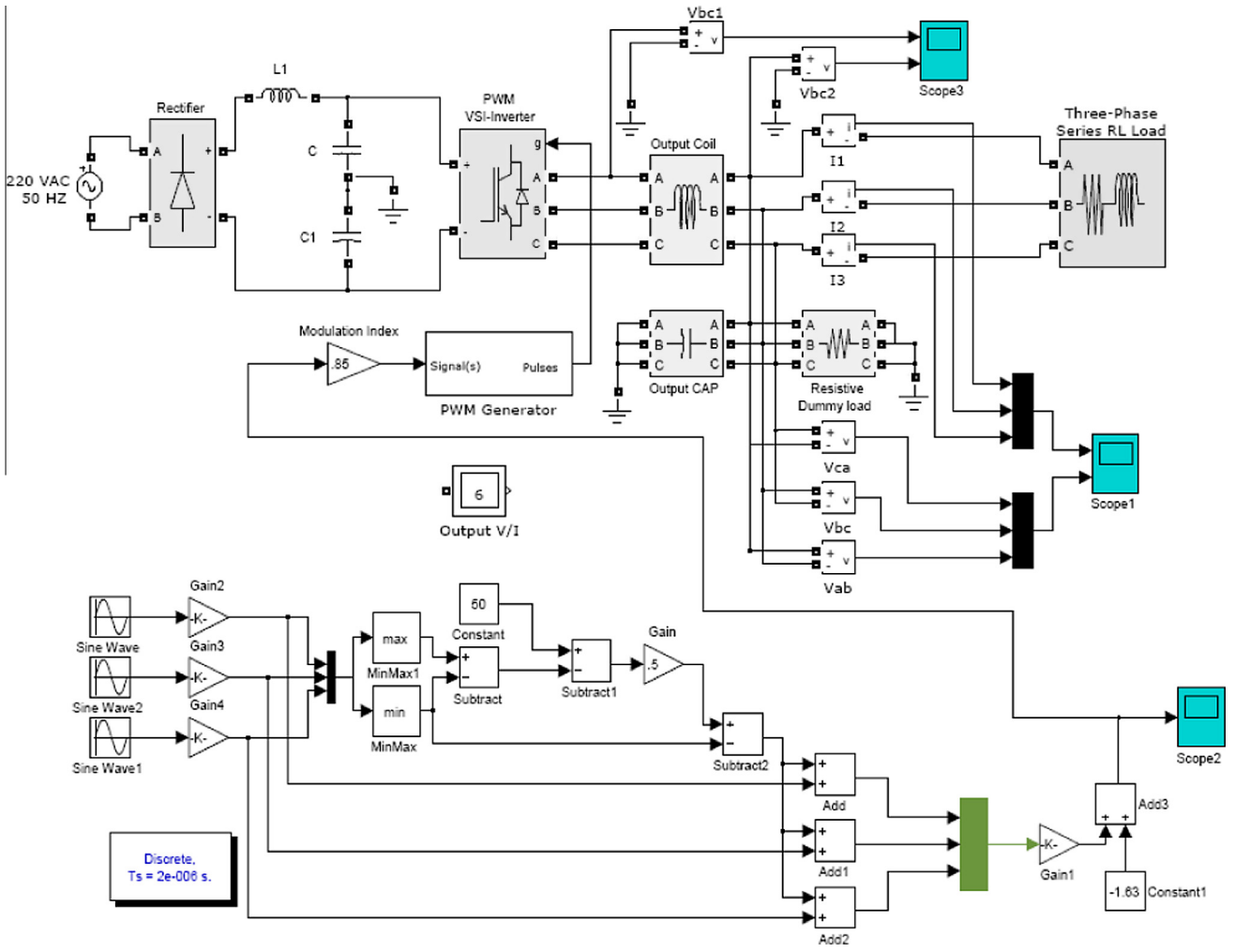


Figure 7 MATLAB SIMULINK model for the system.

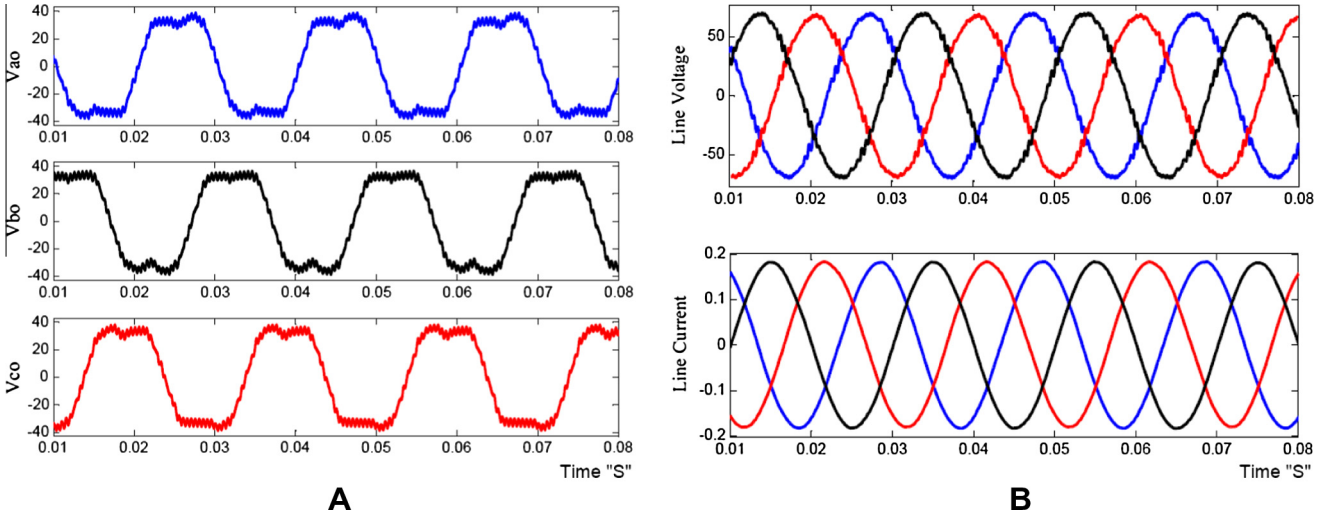


Figure 8 The simulation results at modulation index = 0.1. (A) Output pole voltage waveforms, (B) line voltage/current waveforms across load terminals.

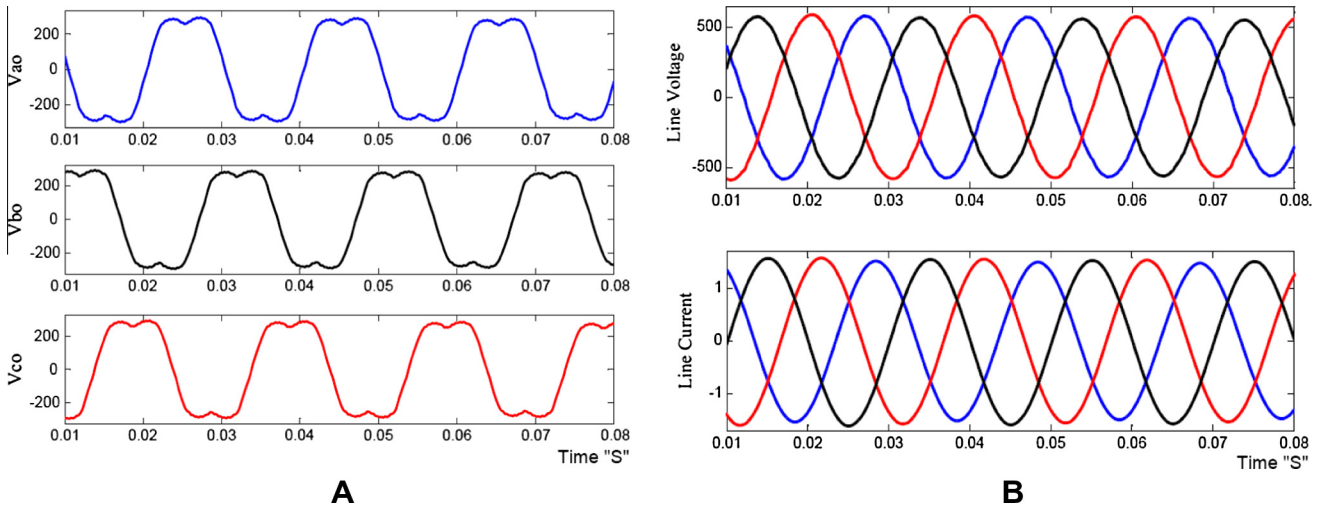


Figure 9 The simulation results at modulation index = 0.85. (A) Output pole voltage waveforms, (B) line voltage/current waveforms across load terminals.

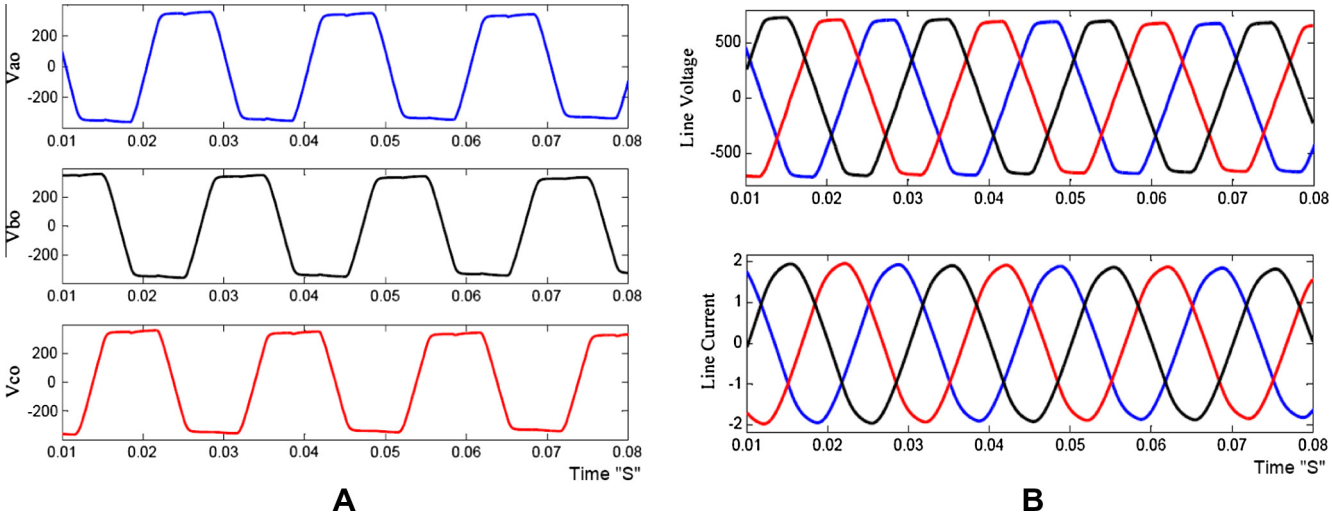


Figure 10 shows the simulation results at modulation index = 1.15. (A) Output pole voltage waveforms, (B) line voltage/current waveforms across load terminals.

DC bus voltage ±310 V from the 220VAC input and controlled by enabling signal from a microcontroller (MCU). The output is provided by a three-phase two-level VSI followed by a three-phase LC filter and an output enable relay. The inverter converts the DC bus voltage back to a sinusoidal voltage using the SVPWM technique. The output inverter is fully controlled by the MCU and generates a pure sinusoidal waveform, free of any disturbance. The system consists of four printed circuit boards (PCB), as shown in Fig. 6. (1) A rectifier/power supply PCB which provides the DC link voltage via the rectifier circuit and provides all DC power supply voltages for the various control circuits such as the main control circuits and the inverter driving circuits. (2) A three-phase two-level inverter PCB, which converts the DC voltage of the DC bus to a three-phase sinusoidal voltage with the required amplitude and frequency via six power IGBTs derived from the control circuit. (3) A three-phase LC filter PCB which removes the undesired component within the output waveforms coming from inverter and maintains the fundamental waveform with pure sinusoidal voltage. (4) A controller/user interface PCB, which manages all control algorithms and measurements of the system, also it contains a user interface that includes a 4×20 characters LCD with three input switches and three indication LEDs.

5.2. Software

The firmware is developed for a microchip PIC18F4431 microcontroller using ASSEMBLY language, Microchip MPLAB IDE ver. 8.3 compiler, and a PICKIT 3 programmer/debugger kit. The reference sine waveform is generated using the built-in PWM module within the microcontroller. The sine reference is stored in a lookup table. The table values are periodically taken from the table and then multiplied by the required amplitude. The resulting value gives the duty cycle of the PWM output. The pointer to the table is incremented by a value which corresponds to the desired output frequency. All the val-

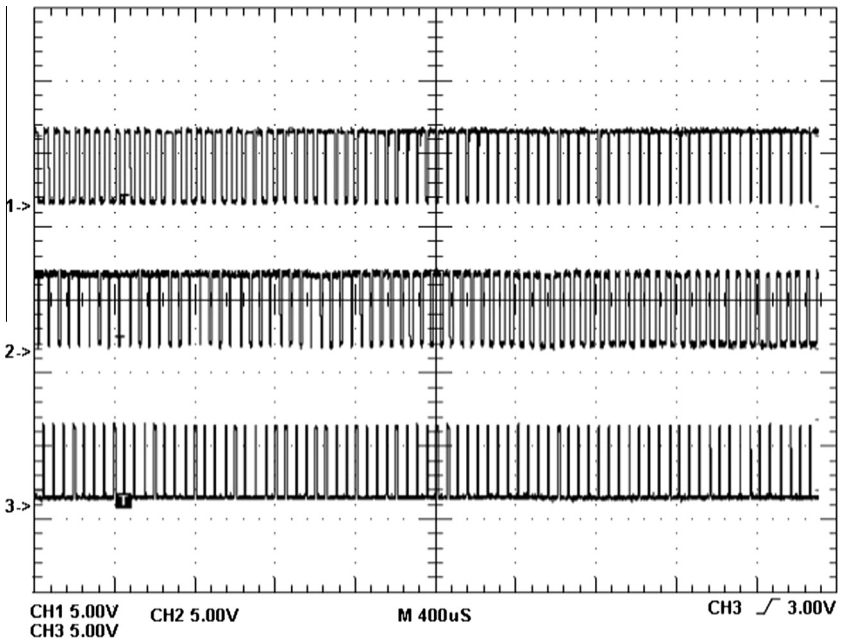


Figure 11 Experimental SV-PWM gating signals. CH1 = T_{ga}, CH2 = T_{gb}, and the CH3 = T_{gc}, X axis 400 μs/div, Y axis 5 V/div.

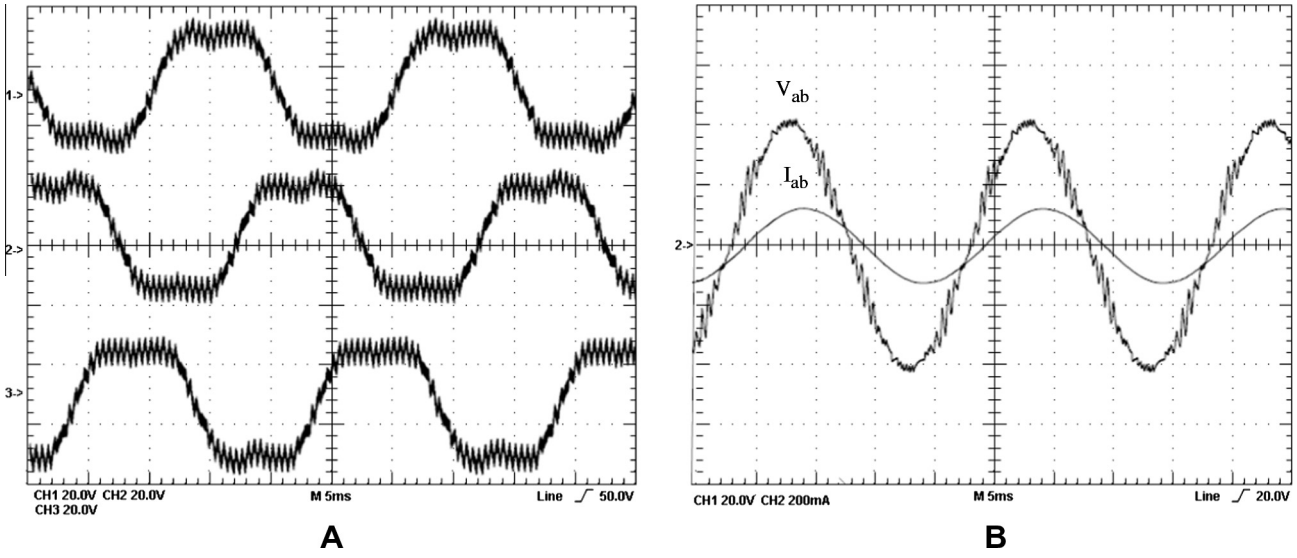


Figure 12 Experimental results for modulation index = 0.1. (A) Pole voltage CH1 = V_{a0}/CH2 = V_{b0}/CH3 = V_{c0} waveforms, (B) line voltage CH1 = V_{ab} line current CH1 = I_{ab} waveforms.

ues over one period give a sinusoidal modulated square wave output. If such a signal passes through an LC filter, a pure sine-wave voltage is generated on the inverter output. At every instant of reading sample from the sine table, the program will compute the minimum and maximum phase amplitudes then compute the offset time and then get/apply the new duty which will drive the VSI switches.

6. Simulation results

The practical system introduced in Section 5 is modeled and simulated using MATLAB SIMULINK software package. The MATLAB SIMULINK model is as shown in Fig. 7.

The simulation is performed under the following conditions: input voltage = 220 VAC, V_{DC} = 620 V, Output voltage fundamental harmonic f = 50 Hz, Switching frequency f_{sw} = 20 KHz, and the output of the system is connected to 1.5 KVA 0.7 P.F Inductive load.

The ratio between the fundamental waveform and the carrier signal is known as modulation index. The simulation is done for three different modulation indexes. Fig. 8 shows the simulation results for 1.5 KVA inductive load with 0.7 power factor at modulation index = 0.1, Fig. 9 shows the simulation results at modulation index = 0.85, and Fig. 10 shows the simulation results at modulation index = 1.15. From these simulation results, we can say that the SVPWM signal generation using the algorithm in Section 4 can work in the under-modulation region with some small harmonics in pole and line

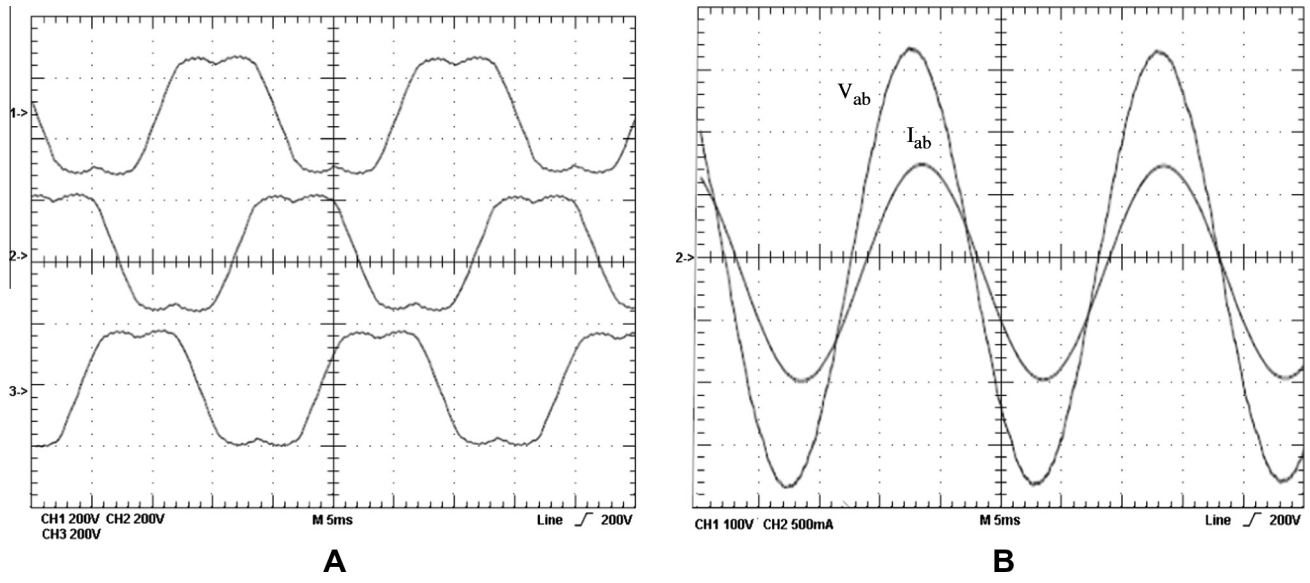


Figure 13 Experimental results for modulation index = 0.85. (A) Pole voltage CH1 = V_{a0}/CH2 = V_{b0}/CH3 = V_{c0} waveforms, (B) line voltage CH1 = V_{ab}, line current CH2 = I_{ab} waveforms.

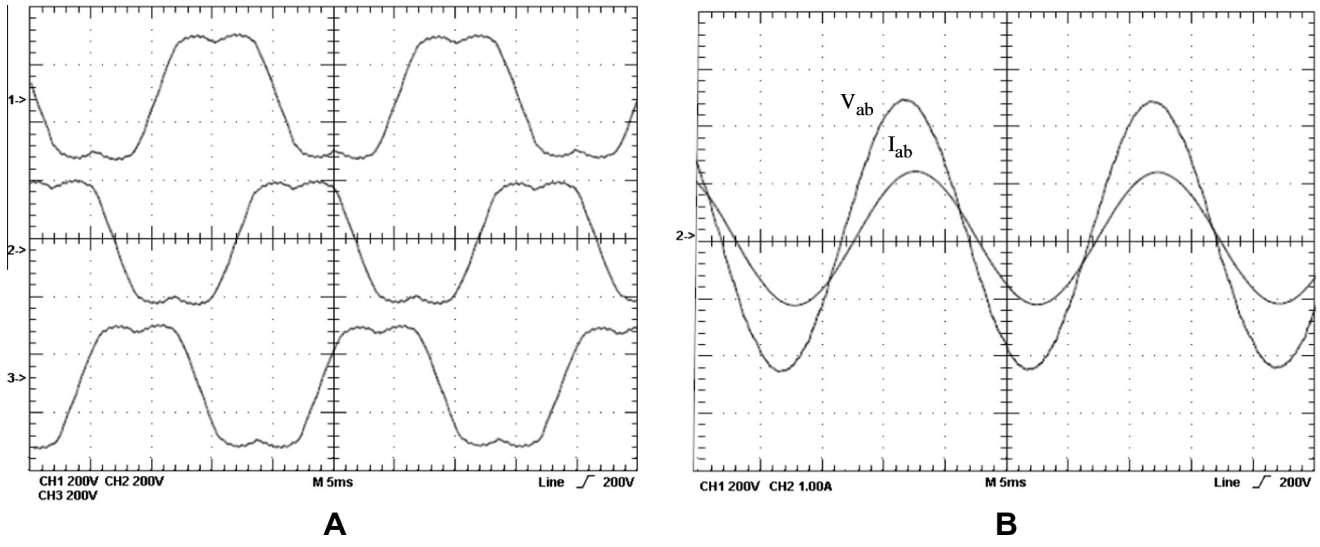


Figure 14 Experimental results for modulation index = 1.00. (A) Pole voltage CH1 = V_{a0}/CH2 = V_{b0}/CH3 = V_{c0} waveforms, (B) Line voltage CH1 = I_{ab}, line Current CH_2 = I_{ab} waveforms.

voltages as shown in Fig. 8, also it can work in the over-modulation region with some small distortions in the output line voltage at the largest modulation index of SVPWM as shown in Fig. 10, and finally, it works well in the linear modulation region as shown in Fig. 9.

7. Experimental results

The algorithm in Section 4 is implemented on a microchip PIC18F4431 microcontroller platform, and the experimental results are presented for a two-level VSI with output LC filter as shown in Fig. 1. The modulation index is varied from the under-modulation region to the over-modulation region. The experiment is done under the following conditions: DC link = 400 V is used for the inverter, output voltage fundamental harmonic $f = 50$ Hz, switching frequency f_{sw} = 20 kHz, and a three-phase 1.5 KVA/0.7 power factor load.

The experimental results are presented in (Figs. 11–15). Fig. 11 shows the generated SVPWM signal used to drive the inverter switches SW1, SW3, and SW5, respectively. (Figs. 12–15) show the pole voltage/line current waveforms at modulation index 0.1, 0.85, 1.00, and 1.15, respectively. The experimental results for the under-modulation region with a modulation index 0.1 are as shown in Fig. 12. Fig. 12a shows the pole voltage of three phases, Fig. 12b shows the line voltage and line current for phase A; it may be noted that the appearance of harmonics in voltage waveforms is due to low modulation index The experimental results for the modulation

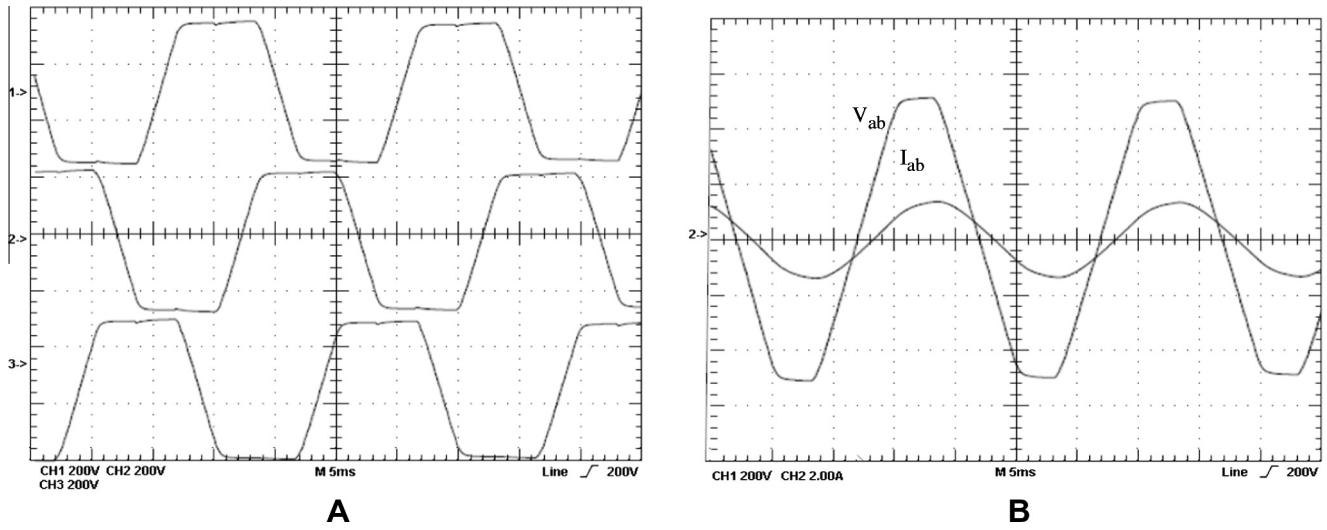


Figure 15 Experimental results for modulation index = 1.15. (A) Pole voltage CH1 = V_{a0}/CH2 = V_{b0}/CH3 = V_{c0} waveforms, (B) line voltage CH1 = I_{ab}, line current CH_2 = I_{ab} waveforms.

region with the modulation indexes 0.85 and 1.00 are as shown in Figs. 13 and 14. The line voltage and line current signals seem to be good with low harmonic and no distortion. Finally, the experimental result for the over-modulation region with a modulation index 1.15 is as shown in Fig. 15. Fig. 15a shows the pole voltage of three phases; it may be noted that these waveforms tend to be square waves due to over-modulation. Fig. 15b shows the line voltage and line current for phase A, and the small distortion within line voltage is due to large modulation index.

The simulation and experimental waveforms are identical. It demonstrates that the simplified implementation of SVPWM is feasible and effectual in driving three-phase two-level inverter, and it is much faster "about 1.66" and more executable than conventional means without lookup tables or complex logical judgments.

8. Conclusions

A space vector pulse-width modulation technique based on a reduced computation method was presented. The SVPWM scheme can drive the inverter gating signals from the sampled amplitudes of the reference phase voltages. The switching vectors for the inverter are derived using a simple digital logic which does not involve any complex computations and hence reduces the implementation time. A practical system design and real implementation for space vector PWM inverter, including MATLAB SIMULINK model, and simulation results for different modulation indexes were also presented. The space vector PWM scheme was implemented on microchip PIC microcontroller 18F4431 platform, and the experimental results were presented for two-level VSI with three-phase LC filter. The practical results show a good performance with less computation time "about 1.66 faster" and easy software implementation of the presented SVPWM scheme rather than conventional SVPWM.

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