1. Description

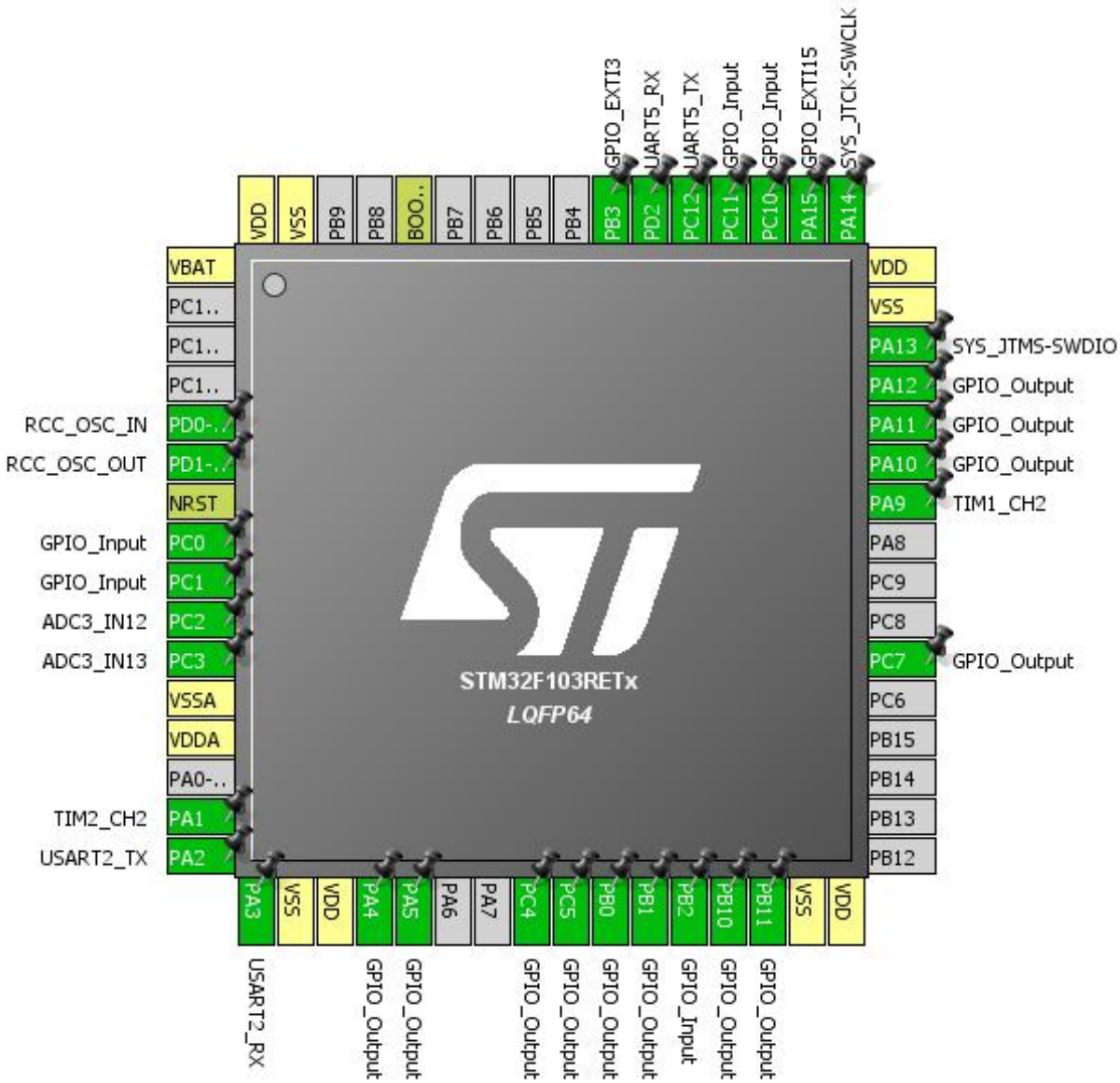
1.1. Project

Project Name	fstm_nsdtues
Board Name	fstm_nsdtues
Generated with:	STM32CubeMX 4.14.0
Date	08/31/2018

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



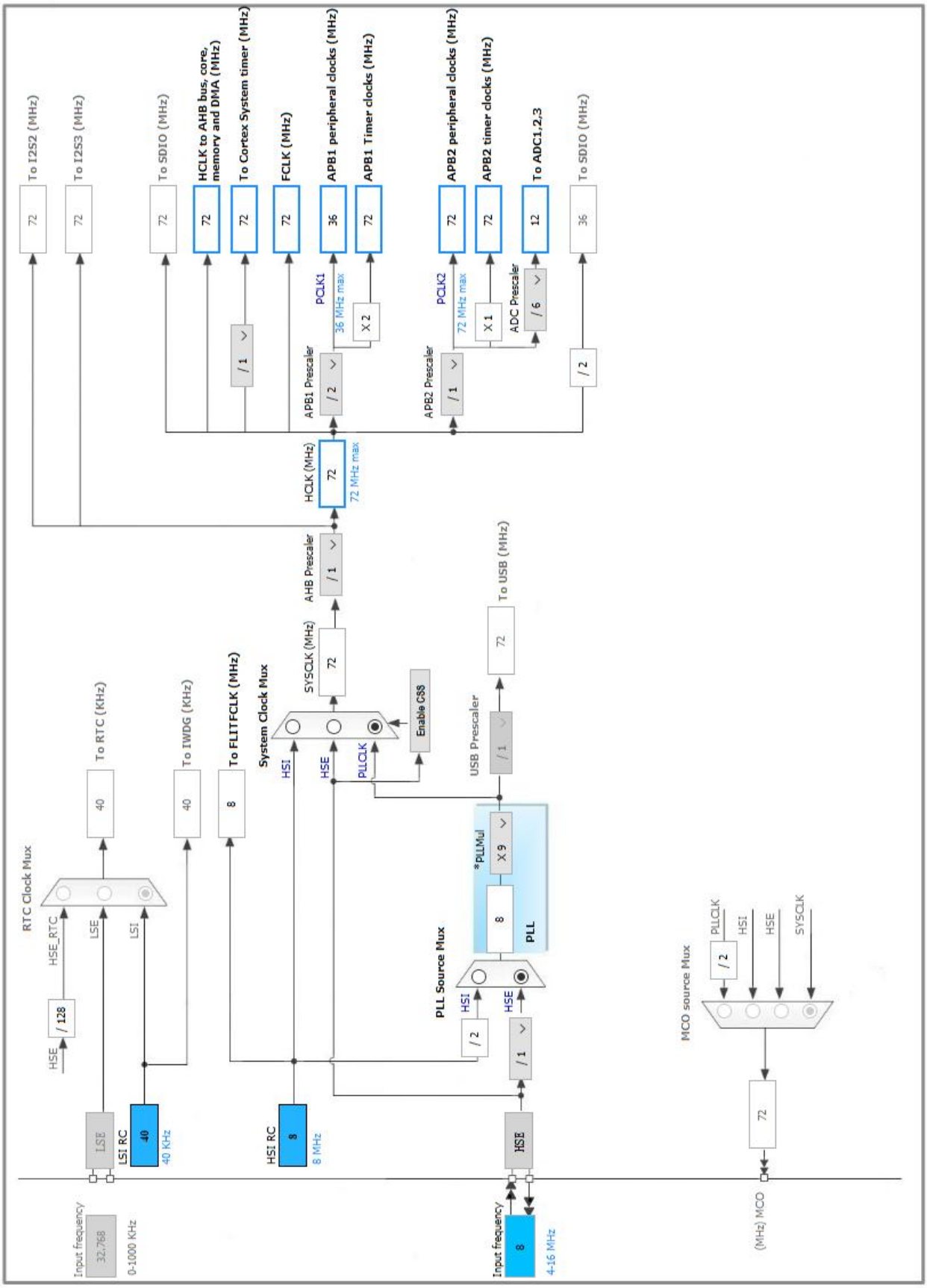
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Input	
9	PC1 *	I/O	GPIO_Input	
10	PC2	I/O	ADC3_IN12	
11	PC3	I/O	ADC3_IN13	
12	VSSA	Power		
13	VDDA	Power		
15	PA1	I/O	TIM2_CH2	
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Output	
21	PA5 *	I/O	GPIO_Output	
24	PC4 *	I/O	GPIO_Output	
25	PC5 *	I/O	GPIO_Output	
26	PB0 *	I/O	GPIO_Output	
27	PB1 *	I/O	GPIO_Output	
28	PB2 *	I/O	GPIO_Input	
29	PB10 *	I/O	GPIO_Output	
30	PB11 *	I/O	GPIO_Output	
31	VSS	Power		
32	VDD	Power		
38	PC7 *	I/O	GPIO_Output	
42	PA9	I/O	TIM1_CH2	
43	PA10 *	I/O	GPIO_Output	
44	PA11 *	I/O	GPIO_Output	
45	PA12 *	I/O	GPIO_Output	
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
50	PA15	I/O	GPIO_EXTI15	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
51	PC10 *	I/O	GPIO_Input	
52	PC11 *	I/O	GPIO_Input	
53	PC12	I/O	UART5_TX	
54	PD2	I/O	UART5_RX	
55	PB3	I/O	GPIO_EXTI3	
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC3

mode: IN12

mode: IN13

5.1.1. Parameter Settings:

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**2 ***
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 12
Sampling Time	**71.5 Cycles ***
Rank	**2 ***
Channel	**Channel 13 ***
Sampling Time	**71.5 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3

Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16

5.3. SYS

Debug: Serial-Wire

Timebase Source: SysTick

5.4. TIM1

Channel2: PWM Generation CH2

5.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**16 ***
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.5. TIM2

Clock Source : Internal Clock

Channel2: PWM Generation CH2

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**16 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4096 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.6. UART5

Mode: Asynchronous

5.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.7. USART2

Mode: Asynchronous

5.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC3	PC2	ADC3_IN12	Analog mode	n/a	n/a	
	PC3	ADC3_IN13	Analog mode	n/a	n/a	
RCC	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA9	TIM1_CH2	Alternate Function Push Pull	n/a	Low	
TIM2	PA1	TIM2_CH2	Alternate Function Push Pull	n/a	Low	
UART5	PC12	UART5_TX	Alternate Function Push Pull	n/a	**High ***	
	PD2	UART5_RX	Input mode	No pull-up and no pull-down	**n/a**	
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	**High ***	
	PA3	USART2_RX	Input mode	No pull-up and no pull-down	**n/a**	
GPIO	PC0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA4	GPIO_Output	Output Push Pull	n/a	Low	
	PA5	GPIO_Output	Output Push Pull	n/a	Low	
	PC4	GPIO_Output	Output Push Pull	n/a	Low	
	PC5	GPIO_Output	Output Push Pull	n/a	Low	
	PB0	GPIO_Output	Output Push Pull	n/a	Low	
	PB1	GPIO_Output	Output Push Pull	n/a	Low	
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB10	GPIO_Output	Output Push Pull	n/a	Low	
	PB11	GPIO_Output	Output Push Pull	n/a	Low	
	PC7	GPIO_Output	Output Push Pull	n/a	Low	
	PA10	GPIO_Output	Output Push Pull	n/a	Low	
	PA11	GPIO_Output	Output Push Pull	n/a	Low	
	PA12	GPIO_Output	Output Push Pull	n/a	Low	
	PA15	GPIO_EXTI15	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PC10	GPIO_Input	Input mode	**Pull-up ***	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC11	GPIO_Input	Input mode	**Pull-up ***	n/a	
	PB3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC3	DMA2_Channel5	Peripheral To Memory	Low

ADC3: DMA2_Channel5 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
Debug monitor	true	0	0
System tick timer	true	0	0
TIM2 global interrupt	true	0	0
USART2 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
UART5 global interrupt	true	0	0
DMA2 channel4 and channel5 global interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line3 interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
ADC3 global interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103RETx
Datasheet	14611_Rev11

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	fstm_nsdtues
Project Folder	D:\work\sy_hr02_lcd_v3.1__\syzn
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F1 V1.3.1

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No