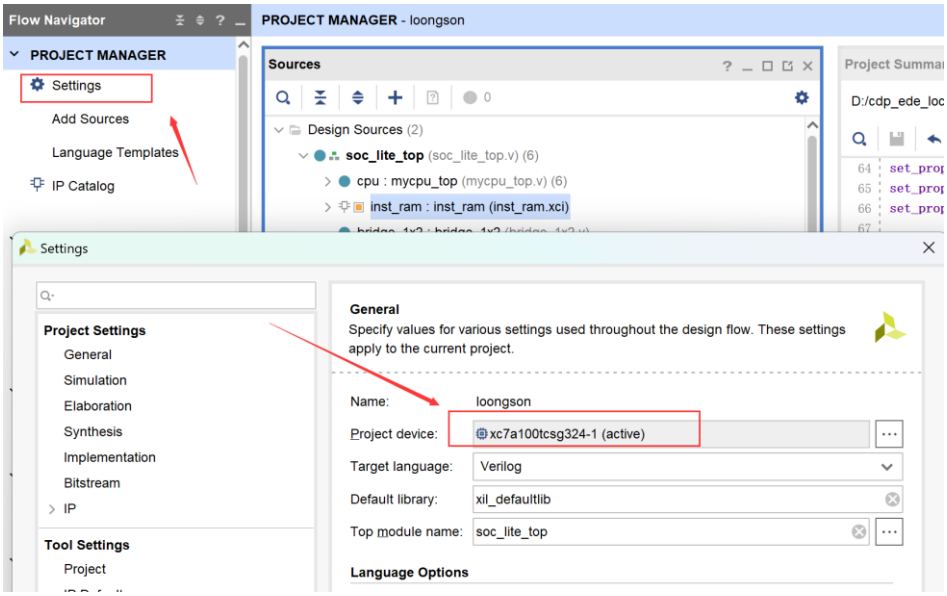
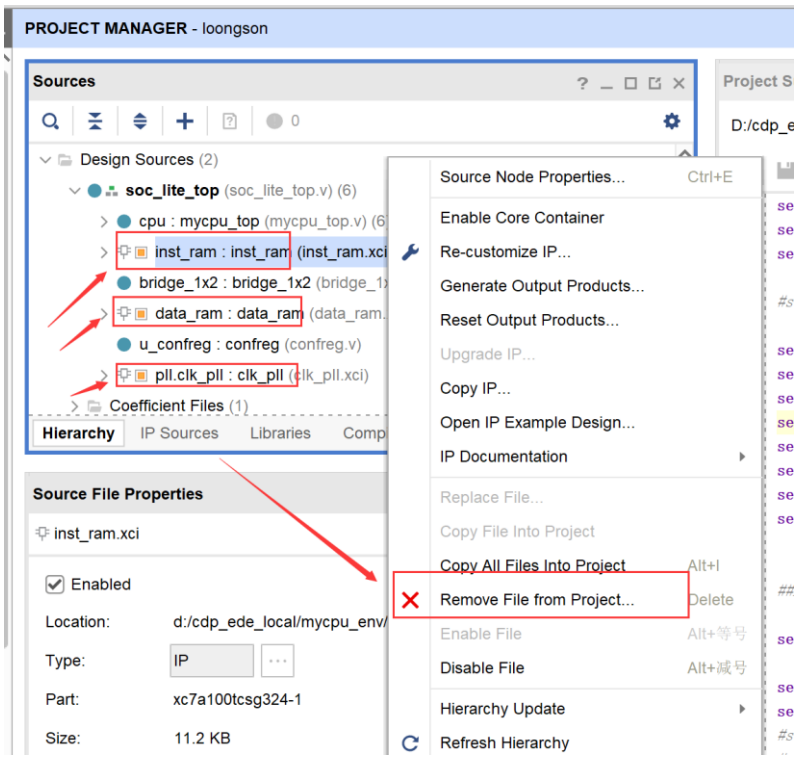
大家完成 39 条的仿真后，需要进行龙芯测试程序和冒泡排序的下载。龙芯测试程序下载步骤如下。
首先需要说明的是，39 条指令在下载测试时可能会出现资源数量不足的问题，所以我们下载测试 20 条指令即可。

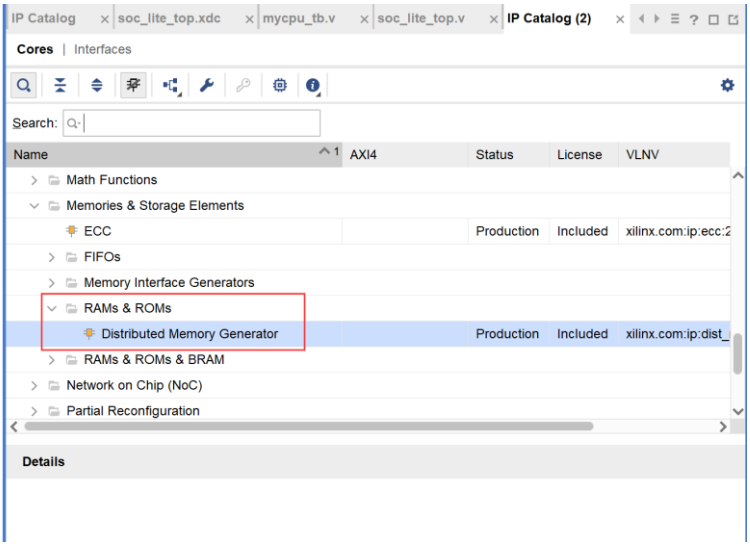
1.在 settings 里修改项目设备



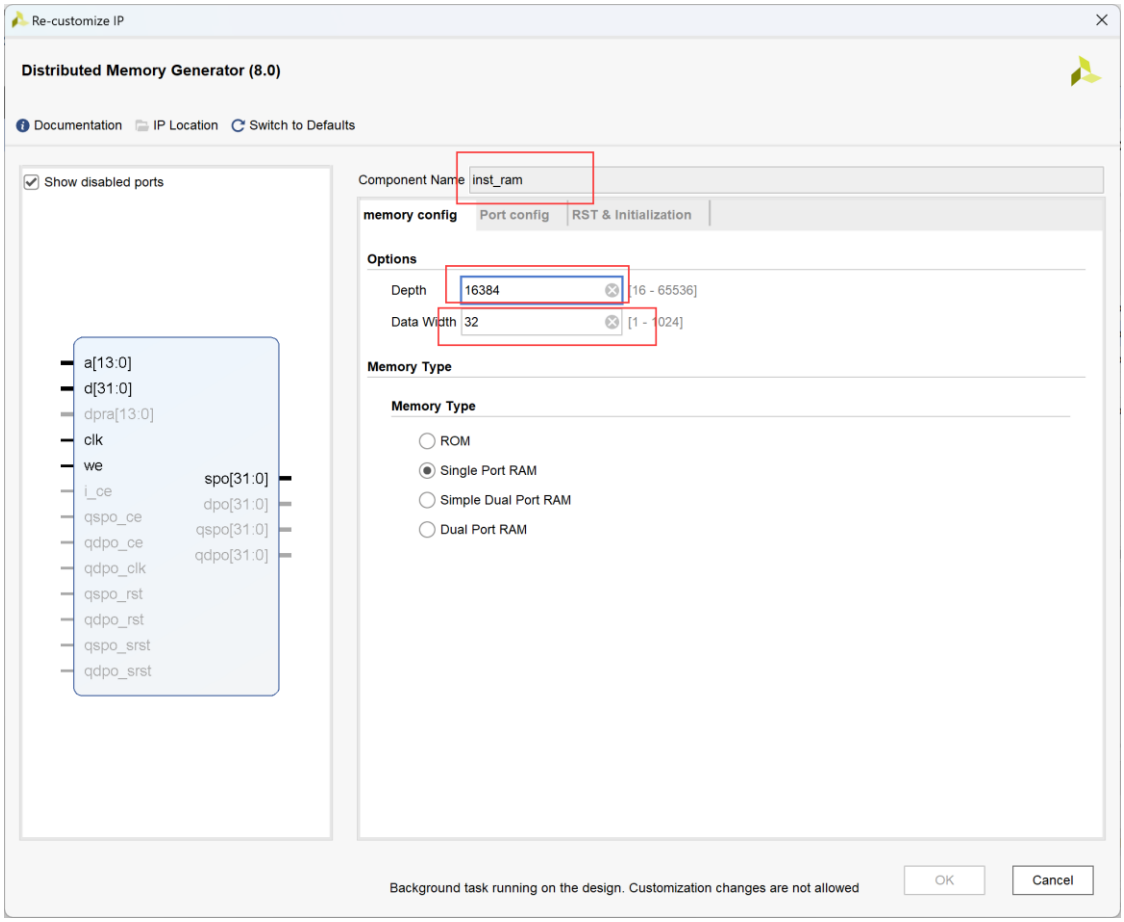
2.对于 3 个 ip 核 inst_ram、data_ram、pll.clk_pll，其设备型号与我们使用的开发板不同，因此需要重新生成。
首先删掉这三个 ip 核

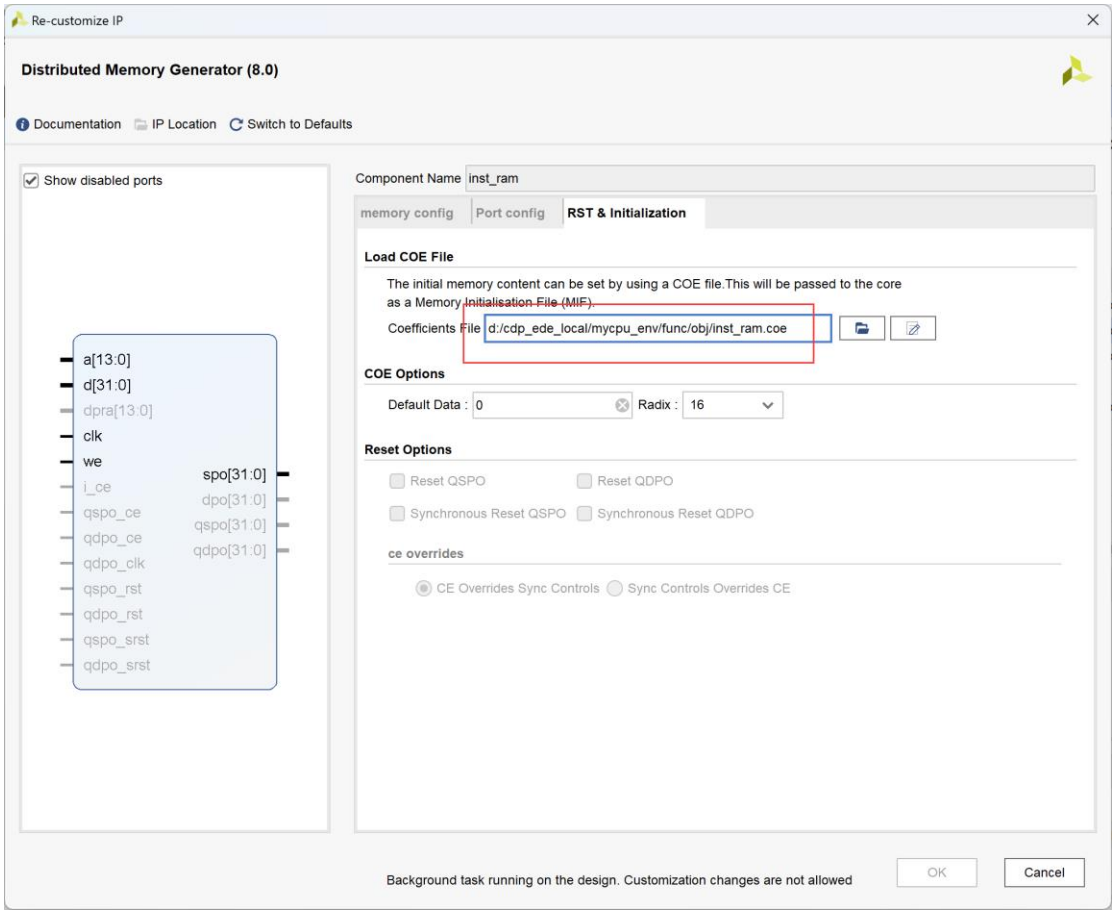


inst_ram、data_ram 都使用 ip catalog 中的 distributed memory generator。

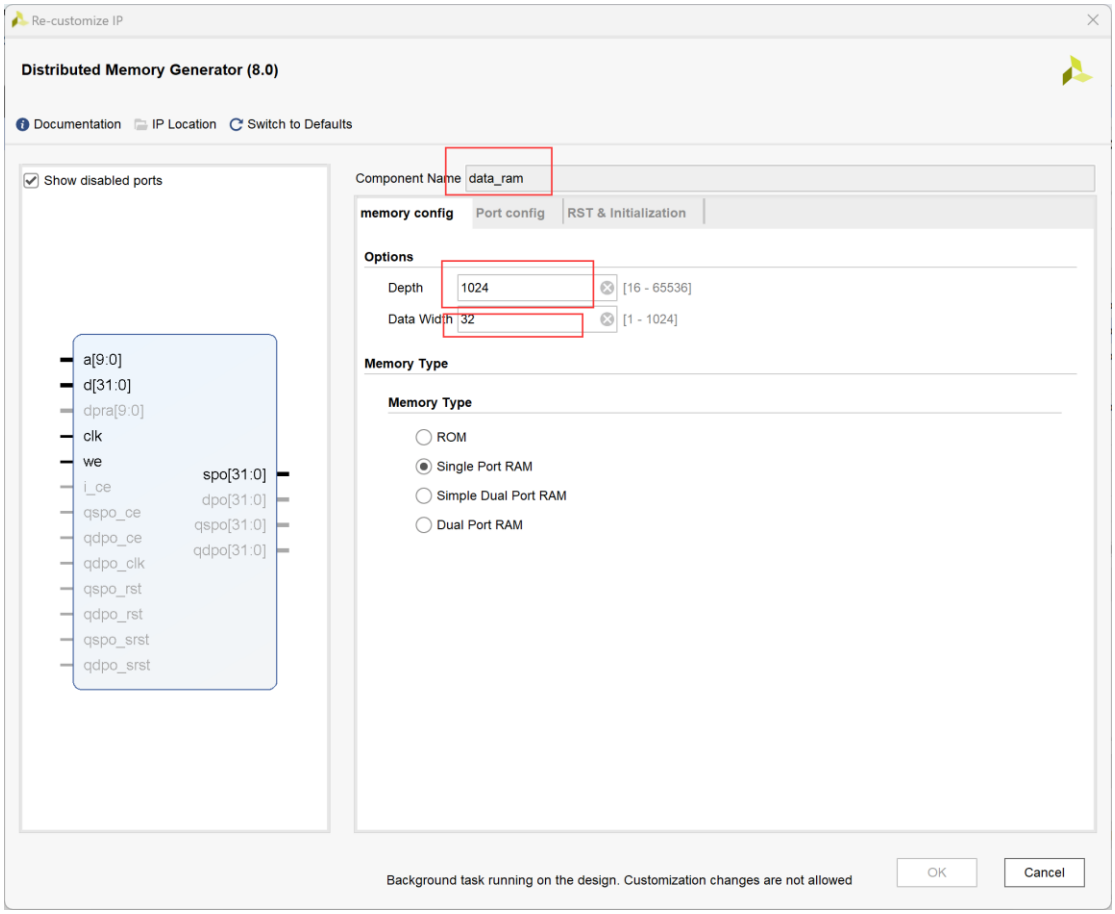


inst_ram 配置如下

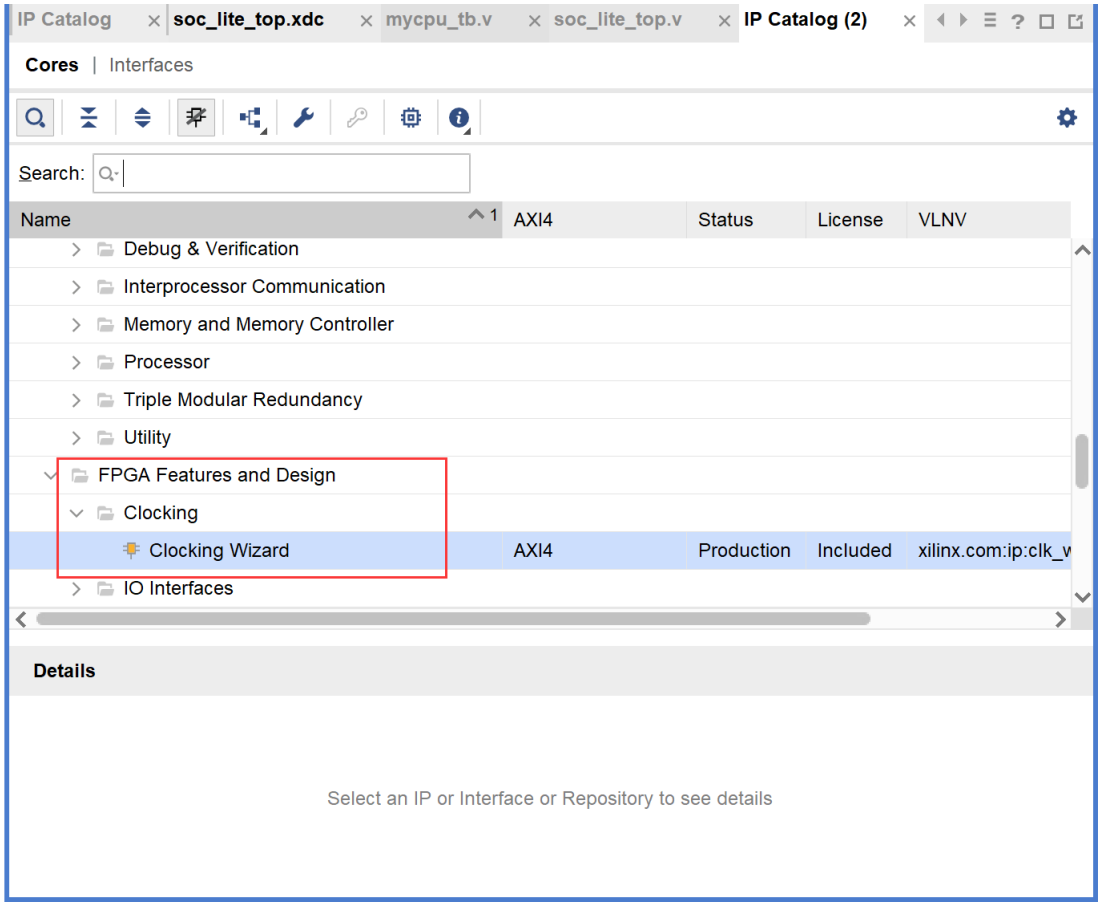




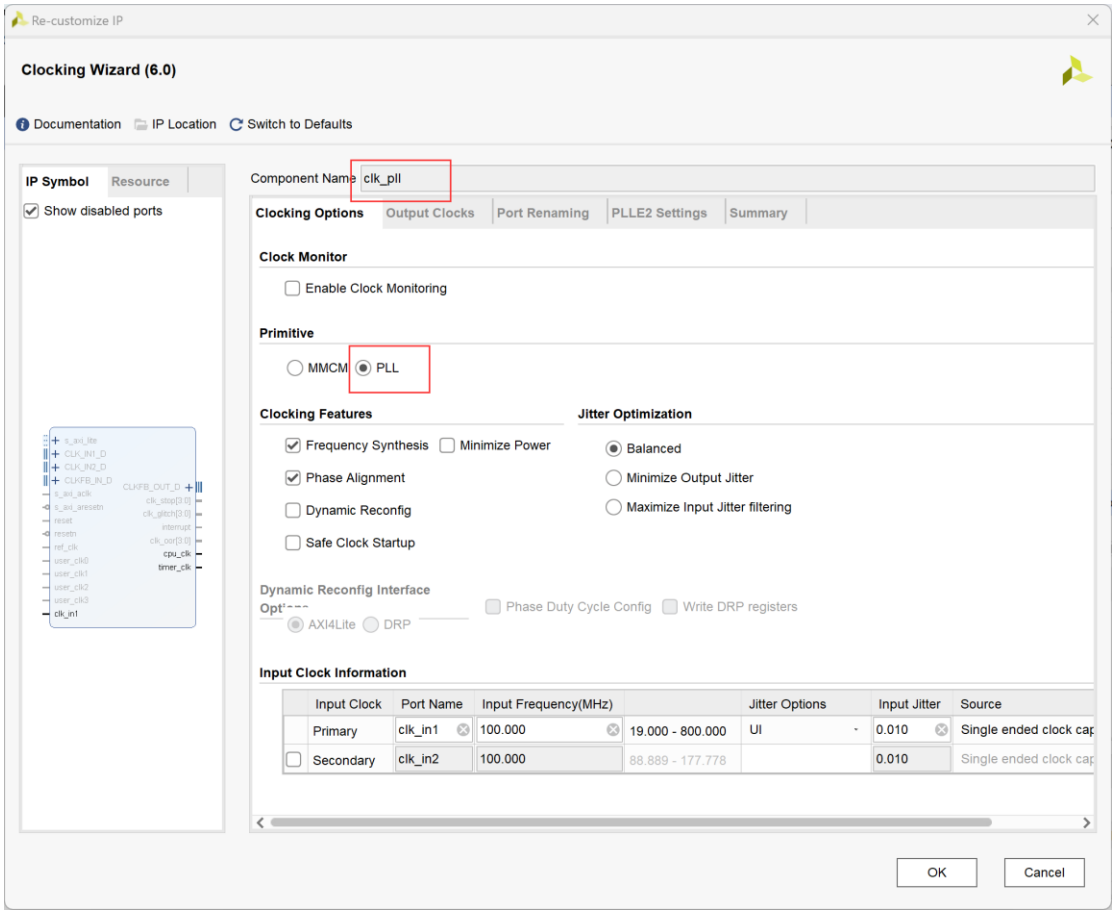
data_ram 配置如下，其他默认

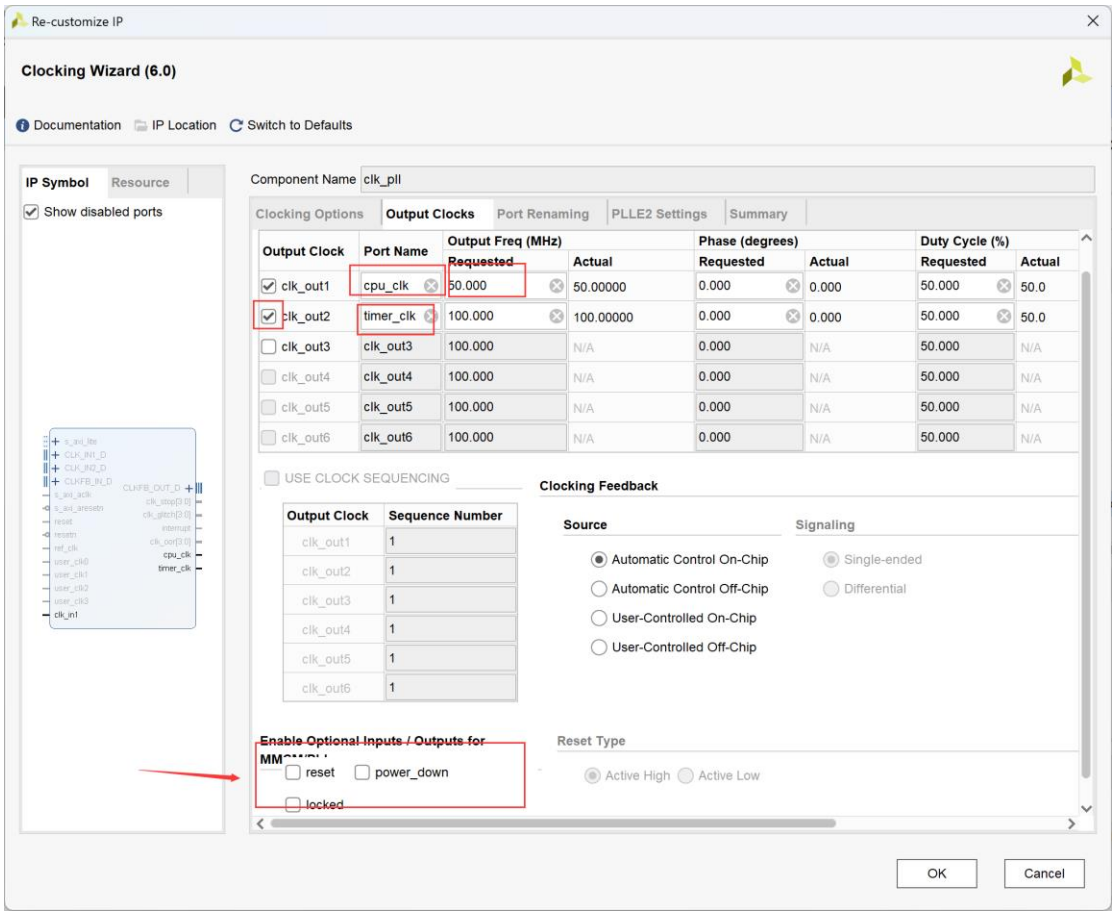


pll.clk_pll 使用 ip catalog 中的 clocking wizard


IP Catalog
soc_lite_top.xdc
mycpu_tb.v
soc_lite_top.v
IP Catalog (2)
Cores | Interfaces
Search:
Name
AXI4
Status
License
VLNV
Debug & Verification
Interprocessor Communication
Memory and Memory Controller
Processor
Triple Modular Redundancy
Utility
FPGA Features and Design
Clocking
Clocking Wizard
AXI4
Production
Included
xilinx.com:ip:clk_w
IO Interfaces
Details
Select an IP or Interface or Repository to see details

配置如下


Re-customize IP
Clocking Wizard (6.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Resource
Show disabled ports
Component Name clk_pll
Clocking Options
Output Clocks
Port Renaming
PLLE2 Settings
Summary
Clock Monitor
Enable Clock Monitoring
Primitive
MMCM
PLL
Clocking Features
Frequency Synthesis
Minimize Power
Phase Alignment
Dynamic Reconfig
Safe Clock Startup
Jitter Optimization
Balanced
Minimize Output Jitter
Maximize Input Jitter filtering
Dynamic Reconfig Interface
Phase Duty Cycle Config
Write DRP registers
AXI4Lite
DRP
Input Clock Information
Input Clock
Port Name
Input Frequency(MHz)
Jitter Options
Input Jitter
Source
Primary
clk_in1
100.000
19.000 - 800.000
UI
0.010
Single ended clock cap
Secondary
clk_in2
100.000
88.889 - 177.778
0.010
Single ended clock cap
OK
Cancel


Re-customize IP
Clocking Wizard (6.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Resource
Show disabled ports
Component Name clk_pll
Clocking Options
Output Clocks
Port Renaming
PLLE2 Settings
Summary
Output Clock
Port Name
Output Freq (MHz)
Requested
Actual
Phase (degrees)
Requested
Actual
Duty Cycle (%)
Requested
Actual
clk_out1
cpu_clk
50.000
50.00000
0.000
0.000
50.000
50.0
clk_out2
timer_clk
100.000
100.00000
0.000
0.000
50.000
50.0
clk_out3
clk_out3
100.000
N/A
0.000
N/A
50.000
N/A
clk_out4
clk_out4
100.000
N/A
0.000
N/A
50.000
N/A
clk_out5
clk_out5
100.000
N/A
0.000
N/A
50.000
N/A
clk_out6
clk_out6
100.000
N/A
0.000
N/A
50.000
N/A
USE CLOCK SEQUENCING
Output Clock
Sequence Number
clk_out1
1
clk_out2
1
clk_out3
1
clk_out4
1
clk_out5
1
clk_out6
1
Clocking Feedback
Source
Automatic Control On-Chip
Automatic Control Off-Chip
User-Controlled On-Chip
User-Controlled Off-Chip
Signaling
Single-ended
Differential
Enable Optional Inputs / Outputs for MMCM/PLL
reset
power_down
locked
Reset Type
Active High
Active Low
OK
Cancel

配置完成后，修改群里的 confreg.v、mycpu_tb.v、soc_lite_top.v，以及 xdc 文件，就可以在开发板上成功运行了。