Giorgos Dimitrakopoulos - Professor

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Positions held

- April 2024 - now: Professor, Electrical and Computer Engineering Dept., Democritus University of Thrace, Xanthi, Greece.
- Feb 2020 - April 2024: Associate Professor, Electrical and Computer Engineering Dept., Democritus University of Thrace, Xanthi, Greece.
- August 2015-Jan 2020: Assistant Professor, Electrical and Computer Engineering Dept., Democritus University of Thrace, Xanthi, Greece.
- January 2012- July 2015: Lecturer, Electrical and Computer Engineering Dept., Democritus University of Thrace, Xanthi, Greece.
- June 2010 – December 2011: Lecturer, Informatics and Communications Engineering Department of the University of West Macedonia, Kozani, Greece.
- January 2008 – February 2010: Postdoctoral researcher in Computer architecture and VLSI Systems Lab of the Institute of Computer Science (ICS) of the Foundation for Research and Technology – Hellas (FORTH), Heraklion, Greece.
- September 2009 – June 2010: Contract Lecturer, Informatics and Communications Engineering Department of the University of West Macedonia, Kozani, Greece
- January 2008 - August 2009: Contract Assistant Professor, Computer Science Department of the University of Crete, Heraklion, Greece

Education

- Dipl-Ing in Computer Engineering, 1996 - 2001, Computer Engineering and Informatics Dept., University of Patras, Greece.
- MSc in "Hardware Software Integrated Systems", 2001 - 2003, Computer Engineering and Informatics Dept., University of Patras, Greece.
- PhD in Computer Engineering, 2003 - Apr. 2007, Computer Engineering and Informatics Dept., University of Patras, Greece. Thesis: "Datapath design for high-performance microprocessors"

Honors and Awards

- Best Student Paper Award for my PhD students Christodoulos Peltekis and Kosmas Alexandridis at IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS) 2024 for the paper "Reusing Softmax Hardware Unit for GELU Computation in Transformers"
- Best Student Paper Award for my PhD student D. Mangiras - Electronics, Circuits and Systems Track of Modern Circuits and Systems Technologies (MOCAST) conference for the paper "Incremental Lagrangian Relaxation based Discrete Gate Sizing and Threshold Voltage Assignment", July 2021.
- Best Paper Award - T track in Design Automation and Test in Europe conferene for the paper "Error-Shielded Register Renaming Subsystem for a Dynamically Scheduled Out-of-Order Core" March 2019.
- EDAA Outstanding Dissertation Award for 2018 to my PhD student Anastasios Psarras in "Topic 2 – New directions in system-on-chip platforms co-design, novel emerging architectures and system-level management." for his PhD thesis "High-performance Networks-on-Chip".
- Second position to the timing optimization constest organized by the TAU workshop - ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), March 2019.
- Hipeac technology transfer award "Network-on-Chip for Think Silicon's ultra-low-power GPU", 2015.
- Best Paper Award - D track in Design Automation and Test in Europe conferene for the paper "PhaseNoC: TDM Scheduling at the Virtual-Channel Level for Efficient Network Traffic Isolation", March 2015.

Current Research interests

- RISC-V vector and systolic data-parallel accelerators
- High level synthesis design flows for agile ASIC design
- ML-driven digital integrated circuits design & verification

Publications

Journal Papers

1. V. Titopoulos, K. Alexandridis, C. Peltekis, C. Nicopoulos, G. Dimitrakopoulos, **"Optimizing Structured-Sparse Matrix Multiplication in RISC-V Vector Processors",** in IEEE Transactions on Computers, Jan. 2025.
2. C. Peltekis, G. Dimitrakopoulos, **"GCN-ABFT: Low-Cost Online Error Checking for Graph Convolutional Networks"** in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, accepted Dec. 2024.
3. A. Stefanidis, G. Dimitrakopoulos, **"Reinforcement-Learning based Synthesis of Custom Approximate Parallel Prefix Adders"**, in Journal of Low Power Electronics and Applications, 2024.
4. K. Alexandridis, G. Dimitrakopoulos, **"Online Alignment and Addition in Multi-Term Floating-Point Adders"** in IEEE Transactions on VLSI Systems, accepted Oct. 2024

5. D. Filippas, C. Peltekis, V. Titopoulos, I. Kansizoglou, G. Sirakoulis, A. Gasteratos, G. Dimitrakopoulos, **"A High-Level Synthesis Library for Synthesizing Efficient and Functional-Safe CNN Dataflow Accelerators"**, in IEEE Access, 2024
6. C. Peltekis, V. Titopoulos, C. Nicopoulos, G. Dimitrakopoulos, **"DeMM: A Decoupled Matrix Multiplication Engine Supporting Relaxed Structured Sparsity"**, in IEEE Computer Architecture Letters, 2024.
7. A. Stefanidis, I. Zoumpoulidou, D. Filippas, G. Dimitrakopoulos, G. Ch. Sirakoulis, **"Synthesis of Approximate Parallel Prefix Adders"** , in IEEE Transactions on VLSI Systems, vol. 31, no. 11, pp. 1686-1699, Nov. 2023,
8. C. Peltekis, D. Filippas, G. Dimitrakopoulos, C. Nicopoulos, **"Exploiting Data Encoding and Reordering for Low-Power Streaming in Systolic Arrays"**, in Microprocessors and Microsystems, Elsevier, vol. 102, Oct. 2023.
9. K. Rallis, I.-A. Fyrigos, P. Dimitrakis, G. Dimitrakopoulos, I. Karafyllidis, A. Rubio, G. Ch. Sirakoulis, **"A Reprogrammable Graphene Nanoribbon-based Logic Gate"**, in IEEE Transactions on Nanotechnology, Oct. 2023.
10. D. Mangiras, D. Chinnery, G. Dimitrakopoulos, **"Task-based Parallel Programming for Gate Sizing"** in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 42, no. 4, pp. 1309-1322, April 2023.
11. D. Filippas, C. Nicopoulos, and G. Dimitrakopoulos, **"Streaming Dilated Convolution Engine"**, in IEEE Transactions on VLSI Systems, vol. 31, no. 3, pp. 401 - 405, March 2023.
12. D. Filippas, C. Nicopoulos, and G. Dimitrakopoulos, **"Templatized Fused Vector Floating-Point Dot Product for High Level Synthesis"**, in Journal of Low Power Electronics and Applications, 12(4), 2022.
13. D. Filippas, N. Margomenos, N. Mitianoudis, C. Nicopoulos, and G. Dimitrakopoulos, **"Low-Cost On-Line Convolution Checksum Checker"**, in IEEE Transactions on VLSI Systems, vol: 30, no. 2, Feb. 2022.
14. D. Mangiras, G. Dimitrakopoulos, **"Incremental Lagrangian Relaxation based Discrete Gate Sizing and Threshold Voltage Assignment"**, in Technologies, 2021, 9(4):92, 2021.
15. G. Dimitrakopoulos, K. Papachatzopoulos, and V. Paliouras, **"Sum Propagate Adders"**, in IEEE Transactions on Emerging Topics in Computing (Special Section on Emerging and Impacting Trends on Computer Arithmetic), vol. 9, no. 3, pp. 1479-1488, July-Sept. 2021.
16. A. Stefanidis, D. Mangiras, C. Nicopoulos, D. Chinnery, G. Dimitrakopoulos **"Autonomous Application of Netlist Transformations inside Lagrangian Relaxation-based Optimization"**, in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 40, no. 8, pp. 1672-1686, Aug. 2021.
17. D. Konstantinou, C. Nicopoulos, J. Lee, and G. Dimitrakopoulos, **"Multicast-enabled Network-on-Chip Routers leveraging Partitioned Allocation and Switching"** , in Integration: the VLSI journal, Elsevier, vol. 77, pp. 104-112, 2021.

18. D. Mangiras, A. Stefanidis, I. Seitanidis, C. Nicopoulos, G. Dimitrakopoulos **"Timing-Driven Placement Optimization Facilitated by Timing-Compatibility Flip-Flop Clustering"** , in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 10 , Oct. 2020, pp. 2835 - 2848.
19. D. Konstantinou, A. Psarras, C. Nicopoulos, G. Dimitrakopoulos **"The Mesochronous Dual-Clock FIFO Buffer"** , in IEEE Transactions on VLSI Systems, vol. 28, no. 1, pp. 302-306, Jan. 2020.
20. I. Seitanidis, G. Dimitrakopoulos, P. Mattheakis, L. Masse-Navette, D. Chinnery, **"Timing-Driven and Placement-Aware Multi-Bit Register Composition"** , in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 38, no. 8., pp. 1501-1514, Aug., 2019.
21. I. Seitanidis, C. Nicopoulos, G. Dimitrakopoulos, **"Automatic Generation of Peak-Power Traffic for Networks-on-Chip"** , in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 38, no.1, pp. 96-108, Jan., 2019.
22. K. Patsidis, D. Konstantinou, C. Nicopoulos, G. Dimitrakopoulos, **"A Low-Cost Synthesizable RISC-V Dual-Issue Processor Core Leveraging the Compressed Instruction Set Extension"** , in Microprocessors and Microsystems, Elsevier, Sept. 2018.
23. A. Psarras, S. Moisidis, C. Nicopoulos, G. Dimitrakopoulos, **"Networks-on-Chip with Double-Data-Rate Links"** , in IEEE Transactions on Circuits and Systems I, vol. 64, no. 12, pp. 3103-3114, Dec. 2017.
24. A. Psarras, M. Paschou, C. Nicopoulos, G. Dimitrakopoulos, **"A Dual-Clock Multiple-Queue Shared Buffer"**, in IEEE Transactions on Computers, vol. 66, no. 10, pp. 1809 - 1815, Oct. 2017.
25. E. Karampasis, N. Papanikolaou, D. Voglitsis, M. Loupis, A. Psarras, A. Boubaris, D. Baros, G. Dimitrakopoulos, **"Active Thermoelectric Cooling Solutions for Airspace Applications: the THERMICOOL Project"**, in IEEE Access, 2017.
26. A. Psarras, I. Seitanidis, C. Nicopoulos, G. Dimitrakopoulos **"ShortPath: A Network-on-Chip Router with Fine-Grained Pipeline Bypassing"**, in IEEE Transactions on Computers, vol. 65, no. 10, pp. 3136-3147, Oct. 2016.
27. K. Chrysanthou, P. Englezakis, A. Prodromou, A. Panteli, C. Nicopoulos ,Y. Sazeides, G. Dimitrakopoulos, **"An On-Line and Real-Time Fault Detection and Localization Mechanism for Network-on-Chip Architectures"** , in ACM Transactions on Architecture and Code optimisation (TACO), Vol. 13, No. 2, June 2016.
28. A. Psarras, J. Lee, I. Seitanidis, C. Nicopoulos, G. Dimitrakopoulos **"PhaseNoC: Versatile Network Traffic Isolation through TDM-Scheduled Virtual Channels"**, in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.35, no.5, pp.844-857, May 2016.
29. I. Seitanidis, A. Psarras, K. Chrysanthou, C. Nicopoulos, G. Dimitrakopoulos **"ElastiStore: Flexible Elastic Buffering for Virtual-Channel-based Networks-on-Chip"**, in IEEE Transactions on VLSI Systems, vol.23, no.12, pp.3015-3028, Dec. 2015.
30. D. Bertozzi, G. Dimitrakopoulos, J. Flich, S. Sonntag, "**The fast evolving landscape of on-chip communication**", in Design Automation of Embedded Systems, Springer, vol. 19, no. 1-2, March 2015, pp. 59-76.
31. G. Dimitrakopoulos, E. Kalligeros, K. Galanopoulos "**Merged Switch Allocation and Traversal in Network-On-Chip Switches**", in IEEE Transactions on Computers, Oct. 2013, pp. 2001-2012.

32. D. S. Gracia, G. Dimitrakopoulos, T. Monreal Arnal, M. G.H. Katevenis, and V. Vinals Yufera "**LP-NUCA: Networks-in-Cache for high-performance low-power embedded processors**", in IEEE Transactions on VLSI Systems. vol.20, no.8, pp. 1510-1523, Aug. 2012.
33. H. T. Vergos, G. Dimitrakopoulos "**On modulo 2^N +1 adder design**", in IEEE Transactions on Computers, vol.61, no.2, pp. 173-186, Feb. 2012.
34. N. Chrysos, G. Dimitrakopoulos "**Practical High-Throughput Crossbar Scheduling**", in IEEE Micro, Micro's Top Picks from Hot Interconnects 16, Summer 2009.
35. G. Dimitrakopoulos, K. Galanopoulos, C. Mavrokefalidis, D. Nikolos, "**Low-Power Leading Zero Counting and Anticipation Logic for High-Speed Floating Point Units**", in IEEE Transactions on VLSI Systems, July 2008.
36. G. Dimitrakopoulos, C. Mavrokefalidis, K. Galanopoulos, and D. Nikolos, "**Sorter Based Permutation Units for Media-Enhanced Microprocessors**", in IEEE Transactions on VLSI Systems, vol. 15, no. 6, June 2007.
37. C. Efstathiou, H. T. Vergos, G. Dimitrakopoulos, and D. Nikolos, "**Efficient Diminished-1 Modulo 2^n +1 Multipliers**", in IEEE Transactions on Computers, vol. 54, no. 4, April 2005.
38. G. Dimitrakopoulos and D. Nikolos, "**High-Speed Parallel-Prefix VLSI Ling Adders**", in IEEE Transactions on Computers, vol. 54, no. 2, pp. 225-231, February 2005.
39. G. Dimitrakopoulos and V. Paliouras, "**A Novel Architecture and a Systematic Graph-Based Optimization Methodology for Modulo Multiplication**", in IEEE Transactions on Circuits and Systems I, vol. 51, no. 2, pp. 354 - 370, February 2004.

Conference Papers

1. V. Titopoulos, K. Alexandridis, G. Dimitrakopoulos, **"Custom Algorithm-Based Fault Tolerance for Attention Layers in Transformers"** IEEE International System-on-Chip Conference (SoCC), Oct. 2025.
2. G. Alexakis, D. Schoinianakis, G. Dimitrakopoulos, **"High-Performance Pipelined NTT Accelerators with Homogeneous Digit-Serial Modulo Arithmetic"**, Euromicro Digital Systems Design (DSD), Sept., 2025.
3. K. Alexandridis, V. Titopoulos, G. Dimitrakopoulos, **"FLASH-D: FlashAttention with Hidden Softmax Division",** IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), Aug., 2025.
4. V. Titopoulos, G. Alexakis, C. Nicopoulos, G. Dimitrakopoulos,**"Efficient Implementation of RISC-V Vector Permutation Instructions"**, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July, 2025.
5. K. Alexandridis, V. Titopoulos, G. Dimitrakopoulos, **"Low-Cost FlashAttention with Fused Exponential and Multiplication Hardware Operators",**IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July, 2025.
6. C. Peltekis, C. Nicopoulos, G. Dimitrakopoulos, **"Periodic Online Testing for Sparse Systolic Tensor Arrays"**, International Conference on Modern Circuits and Systems Technologies (MOCAST), June 2025.

7. V. Titopoulos, G. Alexakis, K. Alexandridis, C. Nicopoulos, G. Dimitrakopoulos, **"Register Dispersion: Reducing the Footprint of the Vector Register File in Vector Engines of Low-Cost RISC-V CPUs"**, in ACM International Conference on Computing Frontiers (CF' 25), May 2025, Italy.
8. K. Alexandridis, C. Peltekis, D. Filippas, G. Dimitrakopoulos, **"Floating-Point Multiply-Add with Approximate Normalization for Low-cost Matrix Engines"**, in IEEE International Conference on Electronics, Circuits, and Systems (ICECS), France, Nov. 2024.
9. C. Peltekis, D. Filippas, G. Dimitrakopoulos, **"Error Checking for Sparse Systolic Tensor Arrays"**, in IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), April 2024.
10. C. Peltekis, K. Alexandridis, G. Dimitrakopoulos, **"Reusing Softmax Hardware Unit for GELU Computation in Transformers"**, in IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), April 2024.
11. V. Titopoulos, K. Alexandridis, C. Peltekis, C. Nicopoulos, G. Dimitrakopoulos, **"IndexMAC: A Custom RISC-V Vector Instruction to Accelerate Structured-Sparse Matrix Multiplications"**, in Design Automation and Test in Europe (DATE), March 2024.
12. C. Peltekis, D. Filippas, G. Dimitrakopoulos, C. Nicopoulos,**"The Case for Asymmetric Systolic Array Floorplanning"**, in IEEE International Workshop on Cellular Nanoscale Networks and their Applications (CNNA), Sept. 2023.
13. K. Rallis, G. Dimitrakopoulos, P. Dimitrakis, A. Rubio, S. Cotofana, I. Karafyllidis, G. Ch. Sirakoulis, **"Novel Circuit Design Methodology with Graphene Nanoribbon Based Devices"** , in IEEE International Conference on Nanotechnology (NANO), 2023.
14. C. Peltekis, D. Filippas, G. Dimitrakopoulos, C. Nicopoulos, **"Low-Power Data Streaming in Systolic Arrays with Bus-Invert Coding and Zero-Value Clock Gating"**, in International Conference on Modern Circuits and Systems Technologies (MOCAST), June 2023.
15. G. Dimitrakopoulos, E. Kallitsounakis, Z. Takakis, A. Stefanidis, C. Nicopoulos, **"Multi-Armed Bandits for Autonomous Test Application in RISC-V Processor Verification"**, in International Conference on Modern Circuits and Systems Technologies (MOCAST), June 2023.
16. D. Filippas, C. Peltekis, G. Dimitrakopoulos, C. Nicopoulos, **"Reduced-Precision Floating-Point Arithmetic in Systolic Arrays with Skewed Pipelines"** in IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), June 2023.
17. C. Peltekis, D. Filippas, G. Dimitrakopoulos, C. Nicopoulos, D. Pnevmatikatos, **"ArrayFlex: A Systolic Array Architecture with Configurable Transparent Pipelining"**, in Design Automation and Test in Europe (DATE), Apr. 2023.
18. Y. Sazeides, A. Gerber, R. Gabor, A. Bramnik, G. Papadimitirou, D. Gizopoulos, C. Nicopoulos, G. Dimitrakopoulos, K. Patsidis, **"IDLD: Instantaneous Detection of Leakage and Duplication of Identifiers used for Register Renaming"**, in ACM/IEEE International Symposium on Microarchitecture (MICRO), Oct. 2022.
19. D. Filippas, C. Nicopoulos, G. Dimitrakopoulos, **"LeapConv: An Energy-efficient Streaming Convolution Engine with Reconfigurable Stride"** , in IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2022), July 2022.

20. C. Peltekis, D. Filippas, C. Nicopoulos, G. Dimitrakopoulos, **"FusedGCN: A Systolic Three-Matrix Multiplication Architecture for Graph Convolutional Networks"** , in IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2022), July 2022.
21. G. Dimitrakopoulos, A. Psarras, C. Nicopoulos, **"Virtual Channel Flow Control Across Mesochronous Clock Domains"** , in International Conference on Modern Circuits and Systems Technologies (MOCAST), June 2022.
22. D. Mangiras, G. Dimitrakopoulos, **"Incremental Lagrangian Relaxation based Discrete Gate Sizing and Threshold Voltage Assignment"**, in International Conference on Modern Circuits and Systems Technologies (MOCAST), July 2021.[**Best Student Paper Award**]
23. Y. Sazeides, A. Bramnik, R. Gabor, C. Nicopoulos, R. Canal, D. Konstantinou, G. Dimitrakopoulos, **"2D Error Correction for F/F based Arrays using In-Situ Real-Time Error Detection (RTD)",** in IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS), Oct. 2020.
24. R. Karamani, I. Fyrigos, V. Ntinas, O. Liolis, G. Dimitrakopoulos, M. Altun, A. Adamatzky, M. R. Stan, G. Ch. Sirakoulis, **"Memristive Learning Cellular Automata: Theory and Applications"**, in Proc. International Conference on Modern Circuits and Systems Technologies (MOCAST), Germany, Sept 2020.
25. K. Patsidis, C. Nicopoulos, G. Sirakoulis, G. Dimitrakopoulos, **"RISC-V^2: a Scalable RISC-V Vector Processor",** in IEEE International Symposium on Circuits and Systems (ISCAS), May 2020.
26. T. Xatzinikolaou, I.-A. Fyrigos, R.-E. Karamani, V. Ntinas, G. Dimitrakopoulos, S. Cotofana, G. Sirakoulis, **"Memristive Oscillatory Circuits for Resolution of NP-Complete Logic Puzzles: Sudoku Case"**, in IEEE International Symposium on Circuits and Systems (ISCAS), May 2020.
27. D. Konstantinou, C. Nicopoulos, J. Lee, G. Sirakoulis, G. Dimitrakopoulos, **"SmartFork: Partitioned Multicast Allocation and Switching in Network-on-Chip Routers"**, in IEEE International Symposium on Circuits and Systems (ISCAS), May 2020.
28. A. Stefanidis, D. Mangiras, C. Nicopoulos, D. Chinnery and G. Dimitrakopoulos, **"Design optimization by fine-grained interleaving of local netlist transformations in Lagrangian relaxation",** in ACM International Symposium on Physical Design (ISPD), March, 2020, pp. 87-94
29. D. Mangiras, P. Mattheakis, P.-O. Ribet and G. Dimitrakopoulos, **"Soft-Clustering Driven Flip-flop Placement Targeting Clock-induced OCV",** in ACM International Symposium on Physical Design (ISPD), March, 2020, pp. 25-32.
30. A. Stefanidis, D. Mangiras, C. Nicopoulos and G. Dimitrakopoulos, **"Multi-Armed Bandits for Autonomous Timing-driven Design Optimization",** in 29th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), July, 2019, pp. 17-22.
31. Z. Takakis, D. Mangiras, C. Nicopoulos and G. Dimitrakopoulos, **"Dynamic Adjustment of Test-Sequence Duration for Increasing the Functional Coverage"** in 4th International Verification and Security Workshop (IVSW), July 2019, pp. 61-66.
32. R. Gabor, Y. Sazeides, A. Bramnik, A. Andreou, C. Nicopoulos, K. Patsidis, D. Konstantinou and G. Dimitrakopoulos, **"Error-Shielded Register Renaming Subsystem for a Dynamically Scheduled Out-of-Order Core",** in Design Automation and Test in Europe (DATE), Mar. 2019. [**Best Paper Award**]

33. D. Konstantinou, A. Psarras, G. Dimitrakopoulos, C. Nicopoulos, **"Low-Power Dual-Edge-Triggered Synchronous Latency-Insensitive Systems",** in Proc. IEEE Int. Conf. on Modern Circuits and Systems Technologies (MOCAST), Greece, May 2018.
34. I. Seitanidis, G. Dimitrakopoulos, P. Mattheakis, L. Masse-Navette, D. Chinnery, **"Timing Driven Incremental Multi-Bit Register Composition Using a Placement Aware ILP formulation",** in Proc. ACM/IEEE Design Automation Conference (DAC), USA, June 2017.
35. M. Debnath, D. Konstatinou, C. Nicopoulos, G. Dimitrakopoulos, W-M Lin, and J. Lee **"Low-Cost Congestion Management in Networks-on-Chip Using Edge and In-Network Traffic Throttling"** in 2nd Int'l Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (HIPEAC-AISTECS), Sweden, 2017.
36. A. Psarras, S. Moisidis, C. Nicopoulos and G. Dimitrakopoulos **"RapidLink: a Network-on-Chip Architecture with Double-Data-Rate Links"** , in IEEE Int'l Conference on Electronics, Circuits, and Systems (ICECS), France, Dec. 2016.
37. I. Seitanidis, C. Nicopoulos and G. Dimitrakopoulos **"PowerMax: An Automated Methodology for Generating Peak-Power Traffic in Networks-on-Chip"** in 10th IEEE/ACM International Symposium on Networks-on-Chip (NoCS), Sept. 2016, Japan. [**Best Paper Award Finalist**]
38. A. Psarras, J. Lee, P. Mattheakis, C. Nicopoulos and G. Dimitrakopoulos **"A Low-Power Network-on-Chip Architecture for Tile-based Chip Multi-Processors"** in ACM Great Lakes Symposium on VLSI (GLSVLSI) 2016, Boston, USA, May 2016.
39. M. Paschou, A. Psarras, C. Nicopoulos and G. Dimitrakopoulos **"CrossOver: Clock Domain Crossing under Virtual-Channel Flow Control"** in Design Automation and Test in Europe (DATE), Dresden, Germany, Mar. 2016.
40. A. Panteloukas, A. Psarras, C. Nicopoulos and G. Dimitrakopoulos **"Timing Resilient Network-on-Chip Architectures"** in IEEE International On-Line Testing Symposium (IOLTS), July 2015.
41. A. Psarras, I. Seitanidis, C. Nicopoulos and G. Dimitrakopoulos **"PhaseNoC: TDM Scheduling at the Virtual-Channel Level for Efficient Network Traffic Isolation"** in Design Automation and Test in Europe (DATE), Grenoble, France, Mar. 2015. [**Best Paper Award**]
42. I. Seitanidis, A. Psarras, E. Kalligeros, C. Nicopoulos, G. Dimitrakopoulos **"ElastiNoC: A Self-Testable Distributed VC-based Network-on-Chip Architecture"** in 8th IEEE/ACM International Symposium on Networks-on-Chip (NoCS), Sept. 2014, Italy.
43. I. Seitanidis, A. Psarras, G. Dimitrakopoulos, C. Nicopoulos **"ElastiStore: An Elastic Buffer Architecture for Network-on-Chip Routers"**, in Design Automation and Test in Europe (DATE), Mar. 2014.
44. G. Dimitrakopoulos, I. Seitanidis, A. Psarras, K. Tsiouris, P. Matthaiakis, J. Cortadella **"Hardware Primitives for the Synthesis of Multithreaded Elastic Systems"**, in Design Automation and Test in Europe (DATE), Mar. 2014.
45. G. Dimitrakopoulos, N. Georgiadis, C. Nicopoulos, E. Kalligeros, **"Switch Folding: Network-on-Chip Routers with Time-Multiplexed Output Ports"**, in Design Automation and Test in Europe (DATE), Mar. 2013.

46. A. Roca, J. Flich, G. Dimitrakopoulos "**DESA: Distibuted Elastic Switch Architecture for efficient Networks-on-FPGAs**", in the International Conference on Field-Programmable Logic and Applications (FPL 2012) Oslo, Norway, August 2012.
47. G. Dimitrakopoulos, E. Kalligeros, "**Dynamic-Priority Arbiter and Multiplexer Soft Macros for On-Chip Networks Switches**", in ACM Design Automation and Test in Europe (DATE), Mar. 2012.
48. G. Dimitrakopoulos, E. Kalligeros, "**Low-cost fault-tolerant switch allocator for network-on-chip routers**", Proc. of the 6th Interconnection Network Architecture, On-Chip Multi-Chip Workshop (INA-OCMC), Jan. 2012.
49. G. Dimitrakopoulos, C. Kachris, E. Kalligeros, "**Scalable arbiters and multiplexers for on-FPGA interconnection networks**", in Proceedings of the 21st International Conference on Field-Programmable Logic and Applications (FPL 2011) Chania, Greece, September 2011.
50. G. Dimitrakopoulos and K. Galanopoulos, "**Switch allocator for bufferless network-on-chip routers**", in Proceedings of the Fifth ACM Interconnection Network Architecture, On-Chip Multi-Chip Workshop (INA-OCMC) Heraklion, Greece, January 2011.
51. G. Dimitrakopoulos, N. Chrysos, K. Galanopoulos "**Fast Arbiters for On-Chip Network Switches**", in IEEE International Conference on Computer Design (ICCD), Oct. 2008.
52. N. Chrysos and G. Dimitrakopoulos "**Backlog-Aware Crossbar Schedulers: A New Algorithm and its Efficient Hardware Implementation**", in IEEE Symposium on High-Performance Interconnects (HOT-Interconnects), pp. 67-74, Aug. 2008.
53. G. Dimitrakopoulos, C. Mavrokefalidis, K. Galanopoulos, and D. Nikolos, "**An Energy-Delay Efficient Subword Permutation Unit**", in IEEE Conference on Application Specific Systems, Architectures, and Processors (ASAP), Sept. 2006.
54. G. Dimitrakopoulos, C. Mavrokefalidis, K. Galanopoulos, and D. Nikolos, "**Fast Bit Permutation Unit for Media-Enhanced Microprocessor**", in IEEE International Symposium on Circuits and Systems (ISCAS), May 2006.
55. G. Dimitrakopoulos, D. G. Nikolos, H. T. Vergos, D. Nikolos, and C. Efstathiou, "**New architectures for modulo 2^n-1 adders**", in IEEE International Conference on Electronics, Circuits and Systems (ICECS), December 2005.
56. G. Dimitrakopoulos and D. Nikolos, "**Closed-Form Bounds for Interconnect-Aware Minimum Delay Gate Sizing**", in International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS 2005), Lectures Notes in Computer Science, vol. 3728, pp. 308 - 317, Sep. 2005.
57. G. Dimitrakopoulos, P. Kolovos, P. Kalogerakis, and D. Nikolos, "**Design of High-Speed Low-Power VLSI Parallel-Prefix Adders**", in Proc. of the 14th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS 2004), Lectures Notes in Computer Science, vol. 3254, pp. 248 - 257, August 2004.
58. C. Efstathiou, H. Vergos, G. Dimitrakopoulos, and D. Nikolos, "**Efficient Modulo 2^n + 1 Tree Multipliers for Diminished-1 Operands**", in Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems (ICECS' 03), December 2003, pp. 200-203.
59. G. Dimitrakopoulos, H. T. Vergos, D. Nikolos, and C. Efstathiou, **"A Family of Parallel Prefix Modulo 2^n-1 Adders**', in Proc. of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors (ASAP'03), June 2003, pp. 326 - 336.

60. G. Dimitrakopoulos, X. Kavousianos, and D. Nikolos, "**Virtual-Scan: A Novel Approach for Software-Based Self-Testing of Microprocessors**", in Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS'03), May 2003, pp. 237-240.
61. G. Dimitrakopoulos, H. T. Vergos, D. Nikolos, and C. Efstathiou, "**A Systematic Methodology for Designing Area-Time Efficient Parallel-Prefix Modulo 2^n - 1 Adders**", in Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS' 03), May 2003, pp. 225-228.
62. G. Dimitrakopoulos, X. Kavousianos, and D. Nikolos, "**Software-Based Self-testing of Microprocessors by Exploiting a Virtual Scan Path**', in the Supplement of the 4th European Dependable Computing Conference (EDCC-4), October 2002, pp. 23-24.
63. G. Dimitrakopoulos and V. Paliouras, "**Graph-Based Optimization for a CSD-Enhanced RNS Multiplier**", in Proceedings of the 45th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS'02), August 2002, Volume III, pp. 648-651.
64. G. Dimitrakopoulos, D. Nikolos, and D. Bakalis, "**Bit-Serial Test Pattern Generation by an Accumulator Behaving as a Non-Linear Feedback Shift Register**", in Proc. of the 8th IEEE International On-Line Testing Workshop (IOLTW'02), July 2002, pp. 152-157.

Book and Book Chapters

1. G. Dimitrakopoulos, A. Psarras, I. Seitanidis "**Microarchitecture of Network-on-Chip Routers**", Springer, ISBN 978-1-4614-4300-1, Oct. 2014.
2. G. Dimitrakopoulos and D. Bertozzi, "**Switch architecture**", Chapter 2 in "Designing Network-on-Chip Architectures in the Nanoscale Era", J. Flich and D. Bertozzi (editors), Dec. 2010, CRC press, ISBN: 978-1-4398-3710-8
3. G. Dimitrakopoulos, "**Logic Design of Basic Switch Components**", Chapter 3 in "Designing Network-on-Chip Architectures in the Nanoscale Era", J. Flich and D. Bertozzi (editors), Dec. 2010, CRC press, ISBN: 978-1-4398-3710-8
4. G. Dimitrakopoulos, C. Kachris, E. Kalligeros, "**Switch design for soft interconnection networks**", in "Embedded Systems Design with FPGAs", P. Athanas, D. Pnevmatikatos, N. Sklavos (editors), Springer.
5. D. Zoni, P. Englezakis, K. Chrysanthou, A. Canidio, A. Prodromou, A. Panteli, C. Nicopoulos. G. Dimitrakopoulos, Y. Sazeides, W. Fornaciari, **"Monitor and Knob Techniques in Network-on-Chip Architectures"**, in Harnessing Performance Variability in Embedded and High-performance Many/Multi-core Platforms A Cross-layer Approach W. Fornaciari and D. Soudris (editors), Springer 2018.

Editing

1. Scientific editor for the translation in Greek of the book: William J. Dally - R. Curtis Harting, "Digital Design: A Systems' Approach", Cambridge University Press, 2014, published in Greece by Crete University Press (CUP).

Research Projects

- Research graph for "Hardware accelerators for privacy preserving technologies", by Nokia (Jul 2024 - July 2027) - Principal investigator
- Research grant for "AI for SoC Verification", by Smart Silicon (Oct 2023 - Sept. 2026) - Principal Investigator.
- Research grant for “RISC-V compatible processor supporting vector extensions”, by Codasip, (Nov 2022 - Nov 2025). - Principal investigator
- Research grant for “High Level Synthesis for System on Chip”, by Mentor Graphics, a Siemens Business, Oregon, USA (Jan 2019 - Dec 2024). - Principal investigator
- Subcontractor in PAVET 2013: Multicore and Multithreaded Graphics Processingn Units for 3D graphics in embedded systems”, ThinkSilicon, Patras (1/4/2014-30/4/2015) - Principal Investigator
- 01/12/2020 – 31/12/2023: “ASPIDA: Design and implementation of system for improving the quality of life of elderly people”, Researcher
- “Thermicool: Thermoelectric cooling using innovative multistage active control modules”, CLEAN SKY RESEARCH and TECHNOLOGY DEVELOPMENT PROJECTS,. DUTH (1/7/2014-30/11/2014) - Researcher
- January 2008 – February 2010: HIPEAC 2 (European Network of Excellence on High Performance and Embedded Architecture and Compilation - www.hipeac.net) as a research coordinator of the interconnection networks research cluster. ICS – FORTH, Heraklion, Crete
- September 2005-December 2006: ARCHIMEDES, “VLSI design and testing of residue number system units for DSP processors and cryptographic units”, September 2004-February 2007 - Researcher
- PYTHAGORAS, “Datapath design space exploration for efficient VLSI implementations”, Greek Ministry of Education under EPEAEK II. University of Patras - Researcher
- October 2003 - July 2005: INTRALED (Industry-driven Training for Low Power European Designers), IST 2001 – 34631, University of Patras. - Researcher
- October 2001 - June 2003: “Design for Testability Techniques for Digital of Integrated Circuits”, funded by GiGA Hellas S.A., University of Patras. - Researcher

Invited Lectures - Tutorials

- "Agile Machine Learning Accelerator design with Optimized Arithmetic", Huawei Research summit, London, 2024
- "Multi-armed bandits as an orchestrator for applying design optimization transformations", Mentor graphics, Grenoble, France (Erasmus+ visit)
- “Optimized network on chip microarchitectures and design methodologies”, Chalmers University of Technology, Sweden, Sept. 2018.
- “Network-on-Chip traffic isolation”, University of Ferrara, Ferrara, Italy, July 2016. (Erasmus+ visit)
- “Network on Chip Research at DUTH”, Intel Mobile Communications, Munich, Germany, Oct. 2015
- “Network-on-Chip Switch architecture”, 3 day course at Universitat Politècnica de València (UPV), Valencia, Spain, Feb 2012.

- “Switch design: Unified view of Microarchitecture and Circuits”, Tutorial IEEE/ACM International Symposium on Network-on-Chip, May 2012, Denmark.
- “The Microarchitecture of Network-on-Chip”, Semina,r July 2012, University of Patras, Greece
- “Introduction to Network on Chip”, Fall 2012, University of Cyprus, Nicosia, Cyprus

Academic Advising

Current students

1. Apostolos Stefanidis, PhD student, working on "Integrated Circuits Design Automation with Reinforcement Learning"
2. Christodoulos Peltekis, PhD student, working on "Data parallel accelerators for Machine Learning Kernels"
3. Vasileios Titopoulos, PhD student, working on "Energy efficient vector processor architectures"
4. Kosmas Alexandridis, PhD student, working on "Automated Design and Verification of SoCs using Machine Learning techniques"
5. Aggelos Kavaleros, PhD student, working on "Machine Learning accelerators for 2.5D/3D chipset-based integrated circuits"
6. Georgios Alexakis, PhD student, working on "Hardware accelerators for privacy preserving technologies"

Graduated

PhD

1. Anastasios Psarras, PhD, "High performance Networks on Chip", 2017
2. Ioannis Seitanidis, PhD, "Low power Networks on chip", 2019
3. Dimitrios Mangiras, PhD "Timing optimization techniques for scalable physical synthesis of digital integrated circuits", 2022
4. Dionysios Filippas, PhD student, working on "Design of Machine Learning Hardware Accelerators", 2025

MSc

1. Charampos Ananiadis, MSc, "Design and evaluation of countermeasures for the protection of secure integrated circuits from malicious attacks", 2015
2. Zacharias Takakis, MSc, "UVM-based verification of RISC-V superscalar processors: A reinforcement learning approach"', 2019
3. Kariofyllis Patsidis, MSc, "Vector Processors for accelerating Convolutional Neural Networks", 2019
4. Anastasios Martidis, MSc, "Hardware-software co-desing of image fusion accelerators using high level synthesis", 2020.
5. Dionysios Filippas, MSc, "Hardware Accelerators for Data Clustering using High Level Synthesis", 2021

Dipl-Ing final year thesis

1. Konstantinos Tsouris, “Design of a pipelined FPGA soft processor”, 2013
2. Ioannis Seitanidis, “Network on chip routers with time shared resources“, 2013
3. Christos Samaras, “Elastic-Pipelined Network on Chip Routers ”, 2014
4. Charalampos Ananiadis ”Single-cycle speculative virtual-channel based routers for NoCs”, 2014
5. Konstantinos Karavelas, “Design space exploration of cache memory architectures”, 2014
6. Alexandros Panteloukas, “Error tolerant Network on Chip architectures”, 2014
7. Dimitrios Katsamanis, “Network interfaces for networks on chip”, 2015
8. Konstantinos Tovletoglou, “Image sensor hardware processing pipeline“, 2015
9. Vassilis Gavrielatos “Shared Buffer Network on Chip Routers", 2015
10. Dimitrios Konstantinou, “In network-on-chip multicasting”, 2016
11. Michalis Paschou, “Clock domain crossing in networks on chip“ 2016
12. Savvas Moisidis, “Cache coherent network interfaces**”**, 2016
13. Zacharias Takakis, “Bridge between AHB5 and AXI5 interfaces”, 2017
14. Apostolis Averkiadis, “UVM-based digital design verification”, 2017
15. Kariofyllis Patsidis, “RISC-V based processor design”, 2017
16. Dimitrios Mangiras, “Timing driven incremental placement”, 2017
17. Apostolos Stefanidis, “Gate sizing and device technology selection for leakage power reduction”, 2017
18. Vikentios Tsartsis, “Bufferless networks on chip”, 2017
19. Christos Gkantidis, “Optimizing cell legalization of digital integrated circuits”, 2018
20. Anastasios Martidis, “Simultaneous Multithreaded RISC-V processor core”, 2018
21. Dionysios Filippas, “Physical design of networks on chip”, 2019
22. Emmanouil Kallitsounakis, “UVM-based verification of network on chip IP”, 2019
23. Charalampos Eleftheriadis, “Polar code decoders hardware architectures”, 2020
24. Alexandros Mallios, "Clustering-based Clock tree synthesis", 2020
25. Antolis Sikalidis, "Logic locking of reusable IP for secure SoCs", 2020
26. Fotis Filippidis, "UVM-based verification of the RISC-V^2 vector processor", 2020
27. Christodoulos Peltekis, "Graph Convolutional Networks Systolic Accelerators", 2021
28. Nikolaos Altanis, "Templatized Floating Point Unit design using HLS", 2021
29. Antonis Aslanidis, "In memory computing: Low-cost RISC V processor with memristors crossbars", 2021
30. Nikolaos Margomenos, "Kd-tree partitioning algorithms parallel accelerators with HLS", 2021.
31. Ioanna Zoumpoulidou, "Synthesis of approximate arithmetic units", 2022

32. Despoina Michailidou, "Exploration of Systolic Architectures", 2022
33. Markos Stefanidis, "FPGA prototype of an HDR image synthesis accelerator", 2022
34. Vasileios Titopoulos, "Design of a scalable vector processor for RISCV ISA", 2022
35. Stratos Karakontis, "CNN accelerators in FPGAs", 2022
36. Dimitrios Mylonidis, "Random Instruction generator for RISC-V Vector Extensions", 2022
37. Kosmas Alexandridis, "RISC-V Vector processors with support for sparse data", 2023
38. Spyros Kolaggis, "Sparse Matrix Multiplication for accelerating Deep Learning Applications", 2023
39. Diamantis Patsidis, "Customizable Superscalar Processor in HLS", 2023
40. Alexandros Askepidis, "UVM-based verification of a UART module", 2023
41. Efstathios Katsimpinis, "Template digit-serial arithmetic operators for HLS", 2023
42. Stergios Kiourtsis "Cycle-accurate modelling of AMBA AHB5 interfaces for High-Level Synthesis", 2024
43. Sokratis Mpitzis, "Vector parallel in-memory processing with standard-cell-based memories", 2024
44. Aggelos Kavaleros, "Formal verification for CAN-bus transceivers", 2024
45. Georgios Alexakis, "RISCV OoO superscalar processors with integrated RISC-V vector engines", 2024
46. Georgios Pelekidis, "ML accelerator for embedded devices", 2025
47. Foivos Chaloftis, "Hardware Accelerators for Transformers in Machine Learning Applications", 2025
48. Ioannis Dingolis, "SoC Interconnects enhanced with hardware security mechanisms", 2025
49. Nikolaos Papaioanou, "RISCV processors with in-register-file processing", 2025
50. Ioannis Marinos Koutoulas, "Matrix engine integrated in a RISCV processor"

PhD thesis examination committee

1. Dario Suarez Gracia, University of Zaragoza, Spain, Nov. 2011 Advisor: Victor Vinals
2. Ana Bosque, University of Zaragoza, Spain, Nov. 2011 Advisors: José M. Llabería, Pablo Ibáñez, Victor Vinals
3. Antoni Roca, Universitat Politècnica de València (UPV), Spain, 2012 Advisor: Jose Flich
4. Ioannis Kouretas, University of Patras, July 2012, Advisor: Vassilis Paliouras
5. Nikita Nikitin, Universitat Politècnica de Catalunya (UPC), Spain, April 2013, Advisor: Jordi Cortadella
6. Pavlos Mattheakis, University of Crete, May 2013, Advisor: Christos Sotiriou
7. Panagiotis Georgiou, University of Ioannina, Oct. 2019, Advisor: Chrysovalantis Kavousianos
8. Ahsen Ejaz, Chalmers University of Technology, Gotenbord, Sweden, 2020, Advisor: Ioannis Sourdis
9. Savvas Moisidis, Democritus Universisty of Thrace, 2021, Advisor: I. Karafyllidis
10. Tomás Picornell Sanjuan, Universitat Politècnica de València (UPV), Spain, 2021 Advisor: Jose Flich, Carles Fernandez Luz
11. Vassilis Ntinas, Democritus University of Thrace, 2023 Advisor: Georgios Syrakoulis

12. Iosif - Angelos Firigos, Democritus University of Thrace, 2023 Advisor: Georgios Syrakoulis
13. K. Rallis, Democritus University of Thrace, 2024 Advisor: Georgios Syrakoulis
14. Kleanthis Papachatzopoulos, University of Patras, Advisor: V. Paliouras

Professional Activities and Service

- *Guest Editor*
    - IET Computer and Digital Techniques, special issue Interconnection Network Architectures: On chip and off chip networks, with Cyriel Minkenberg, IBM Zurich
    - Springer Design automation embedded systems, special issue on Network-on-Chip Architectures, with Soeren Sonntag, Intel, Germany and Davide Bertozzi, Univ. of Ferrara, Italy
- *General Chair*
    - International Workshop on Interconnection Network Architectures, On-Chip Multi-Chip (INA-OCMC-2014), Vienna, Austria.
- *Technical program chair*
    - 1st International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (AISTECS 2016), Prague.
    - International Workshop on Network-on architectures NoCArc - 2014 (in conjunction with the IEEE/ACM International Symposium on Microarchitecture - MICRO), Cambridge, UK
    - International Workshop on Interconnection Network Architectures, On-Chip Multi-Chip (INA-OCMC-2013), Berlin, Germany
    - International Workshop on Interconnection Network Architectures, On-Chip Multi-Chip (INA-OCMC-2012), Paris, France.
- *Technical program committee member*
    - ISVLSI 2022, 2025 (track chair Digital circuits and FPGA based designs)
    - DATE 2011, 2013, 2014, 2015, 2016, 2025, 2026
    - AICAS 2024 (track chair Architecture for AI computing)
    - DAC 2022, 2023
    - FPL 2011, 2012, 2013, 2014, 2015, 2020, 2021, 2022, 2023, 2024, 2025
    - ISPD 2022, 2023, 2024
    - VLSI-SoC 2022 - Track Chair (Digital circuits, low-power design, SoC, NoC, and reconfigurable architectures)
    - SAMOS 2014, 2015, 2016, 2017, 2017, 2019, 2020, 2021, 2022, 2023, 2024, 2025
    - MOCAST 2021, 2022, 2023, 2024, 2025
    - ASAP 2022
    - ARC 2018, 2019, 2020, 2021, 2022, 2023
    - NOCS 2015, 2016, 2017, 2018, 2019

    - NoCArc 2008-2018
    - AISTECS 2016, 2017, 2018, 2019
    - OMHI 2015, 2014, 2013, 2012
    - UCHPC 2015, 2014, 2013, 2012
    - INA-OCMC 2015, 2011, 2010
    - IEEE conference on VLSI design 2015, 2014
    - ICECS 2010
- *Reviewer*
  Regural reviewer for all IEEE Transactions covering my area of research (IEEE Transactions on Computers, IEEE Transactions on Circuits and Systems I, IEEE Transactions on VLSI Systems, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems,IEEE Transactions on Parallel and Distributed System) and other closely related journals Integration, the VLSI Journal, IET Computer and Digital techniques, IET Circuits, Devices and Systems, IET Electronics Letters.

Teaching Experience

Since 2008 taught various courses related to the design of Digital Integrated Circuits:

- Democritus University of Thrace, Electrical and Computer Engineering Dept.
    - Integrated circuits
    - VLSI Systems
    - High-level synthesis of digital integrated circuits
    - Computer organization
    - Computer architecture
    - System-on-Chip architectures [graduate]
- University of Patras, Computer Engineering and Informatics Dept. (MSc course)
    - Network-on-Chip architecture [graduate]
- University of West Macedonia, Informatics and Communications Eng. Dept (Lecturer)
    - Digital Design
    - Advanced digital design
    - VLSI circuit design
- University of Crete, Computer Science Dept. (contract assistant professor)
    - VLSI systems
    - Digital design laboratory