Introduction to Computer Architecture – Sample Questions

1. Convert the following number to the IEEE-754 single-precision floating-point format. Write the answer in hexadecimal.
   -17.75

2. Convert the following number in the IEEE-754 single-precision floating-point format to the decimal number
   0x4404c000

3. Calculate the average CPI of the following processor

   - The base CPI = 1
   - Instruction mix:
     - 30%: load or store instructions.
     - 20%: branch instructions.
     - The rest of the instructions: arithmetic / logic instructions.
   - Cache:
     - L1 D-cache miss rate = 10%
     - L1 I-cache miss rate = 10%
     - L1 cache miss penalty = 5 cycles (same for load & store misses)
     - L2 cache miss rate (local) = 20%
     - L2 cache miss penalty = 20 cycles
   - TLB:
     - TLB miss rate = 5% (instruction fetch, data load and store)
     - TLB miss penalty = 5 cycles (same for all miss types)
   - Branch prediction:
     - Misprediction rate = 5%
     - Misprediction penalty = 3 cycles
   - No load-use data hazard stalls

   A. What is the added cycles (in average) by the cache miss penalty? *(3 pts.)*

   B. What is the added cycles (in average) by the TLB miss penalty? *(3 pts.)*

   C. What is the added cycles (in average) by the branch misprediction penalty? *(3 pts.)*

   D. What is the final CPI with all the penalties? *(1 pts.)*

4. A data cache has the following spec:

- 128KB data capacity
- 2-way set associative, LRU replacement policy
- 64 words per block (1 word = 4 bytes = 32-bit)

If the CPU loads data in the following order, what would be the cache hit/miss results? Assume all accesses are loads (no stores). Indicate hit/miss for each access. Assume the cache is empty (i.e., all valid bits are zero) at the beginning.

		Cache?
L	**0x10000000**	
L	**0x10000004**	
L	**0x10000080**	
L	**0x10000100**	
L	**0x110000F4**	
L	**0x12000000**	
L	**0x11000080**	
L	**0x12001000**	
L	**0x10001008**	
L	**0x10000008**	
L	**0x12000008**	
L	**0x10010000**	
L	**0x10010004**	
L	**0x10090000**	

5. We're executing the RISC-V assembly code on the following processor.

- 5-stage pipeline (IF-ID-EX-MEM-WB)
- Load-use data hazard adds 1 cycle stall at the ID stage.
- "Always not taken" branch prediction for beq.
- However, when executing the following code, **assume the real outcome of EVERY beq instruction is always taken.**
- The real outcome of the beq instruction is determined at the EX stage.
- Jump is resolved at the IF stage

```
i1:    addi x1, x0, 0x100
i2:    lw   x2, 0(x1)
i3:    beq  x2, x3, i6
i4:    add  x3, x4, x5
i5:    j    i10
i6:    lw   x4, 4(x1)
i7:    add  x3, x3, x0
i8:    beq  x3, x4, i10
i9:    j    i6
i10:   sub  x10, x11, x12
```

a. How many cycles are required to complete the above code? That is, if i1 starts the IF stage at cycle 1, at which cycle the instruction i10 reaches the WB stage?

b. How many of the following happens?

- EX hazard forwarding (MEM→EX) :
- MEM hazard forwarding (WB→EX) :

6. Branch prediction:

- You have a branch predictor with a branch prediction buffer (BPB) that contains only 2 entries.
- Each entry in the BPB is a one-bit predictor, and all entries are initially set to “0” (not taken).
- In your program, there are four branch instructions: A, B, C, and D. Branch instructions A and C utilize entry 0 in the branch prediction buffer (BPB), while branch instructions B and D use entry 1 in the BPB.
- The execution order and actual outcomes of the branches are provided in the following table (T: taken, N: not taken).

Execution Order	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Instruction	A	B	C	D	A	A	C	D	B	C	A	D	C	B	A	A	B	B	A	C
Branch Outcome	T	T	T	N	N	N	T	T	N	T	N	T	T	N	N	N	N	N	T	T

How many branches were accurately predicted by the branch predictor?

Answer:

Execution Order		1		2		3		4		5		6		7		8		9		10		11		12		13		14		15		16		17		18		19		20	
Instruction		A		B		C		D		A		A		C		D		B		C		A		D		C		B		A		A		B		B		A		C	
Branch Outcome		T		T		T		N		N		N		T		T		N		T		N		T		T		N		N		N		N		N		T		T	
BPB status																																									
Prediction Correct?																																								