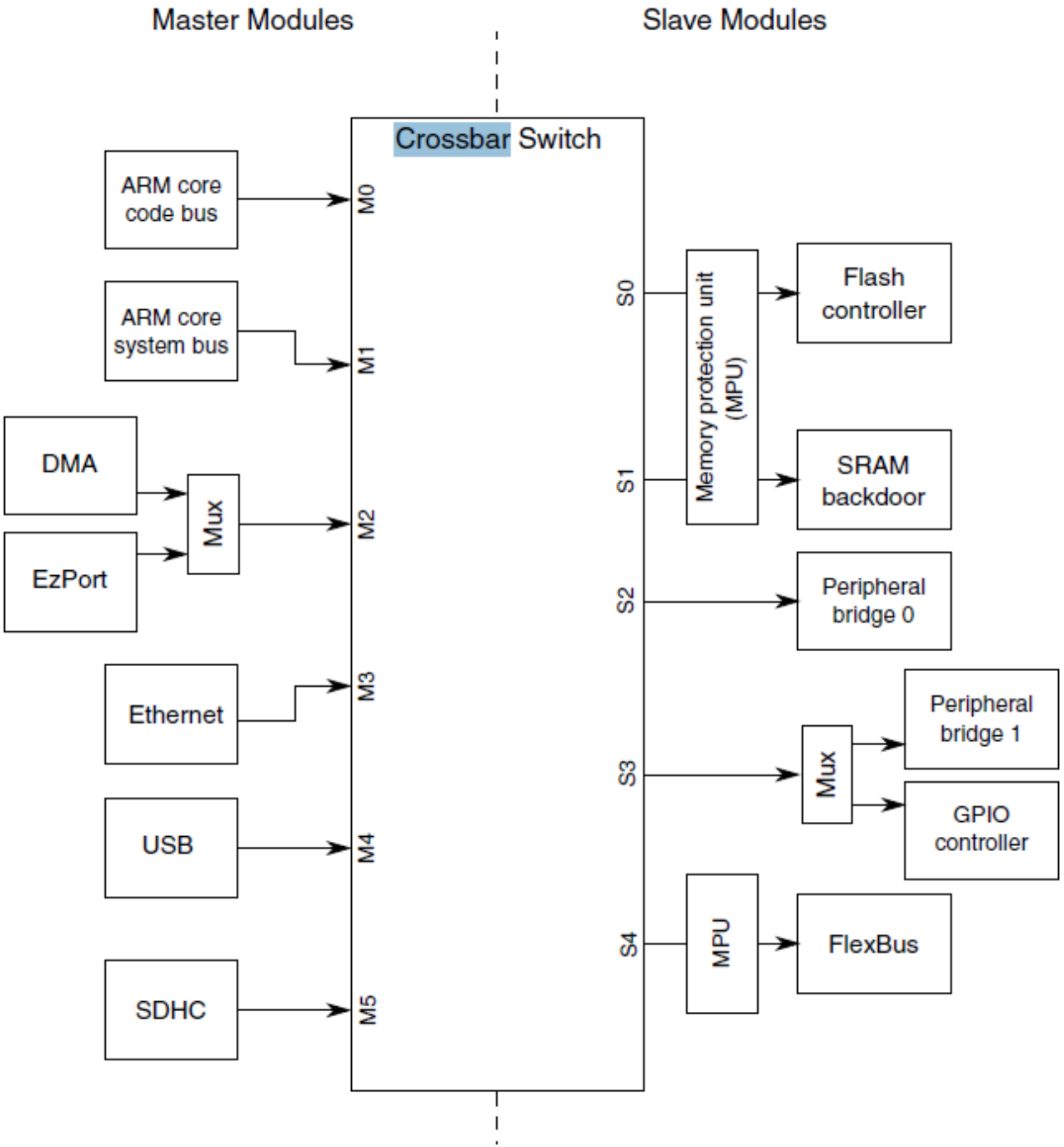
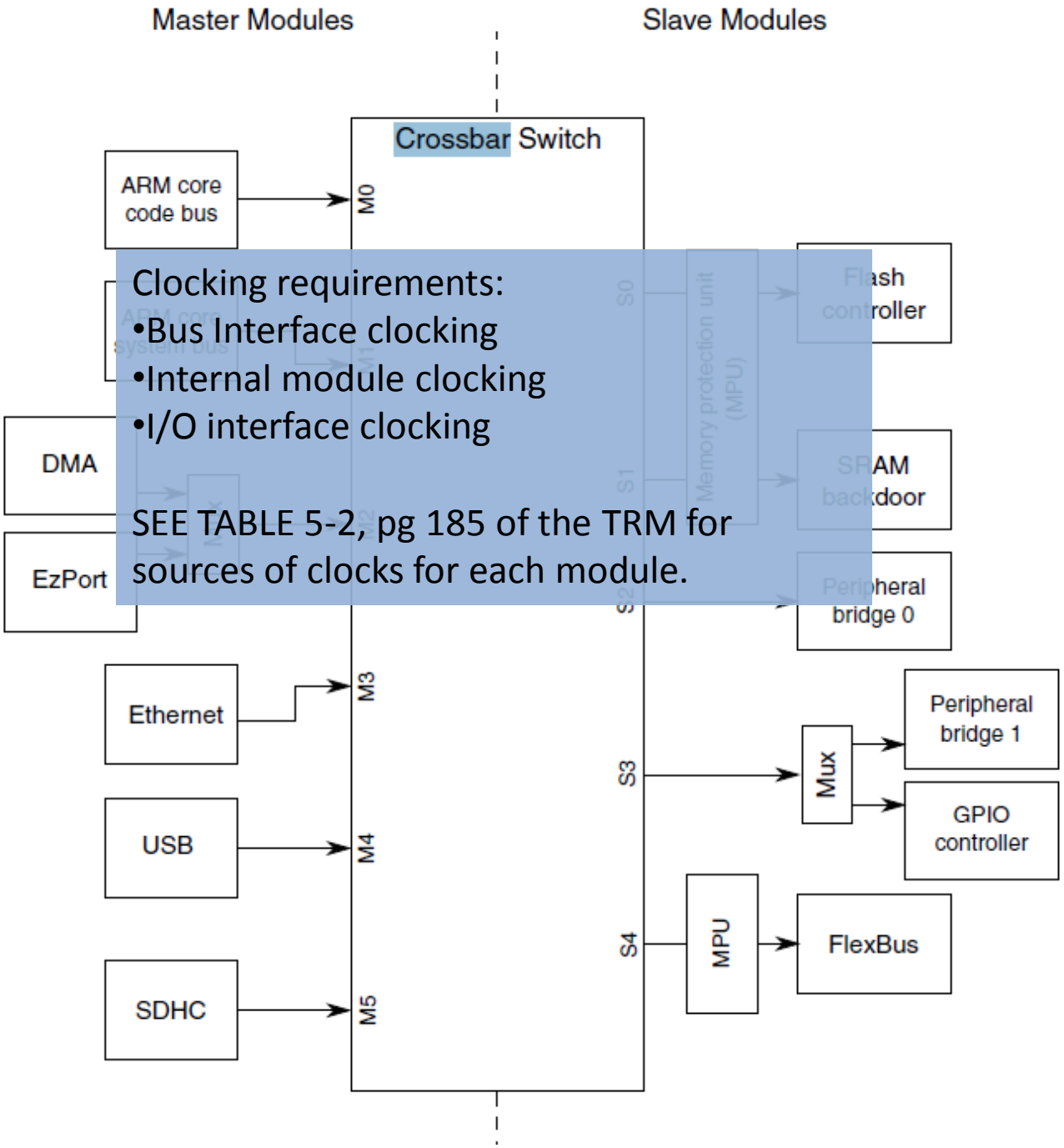
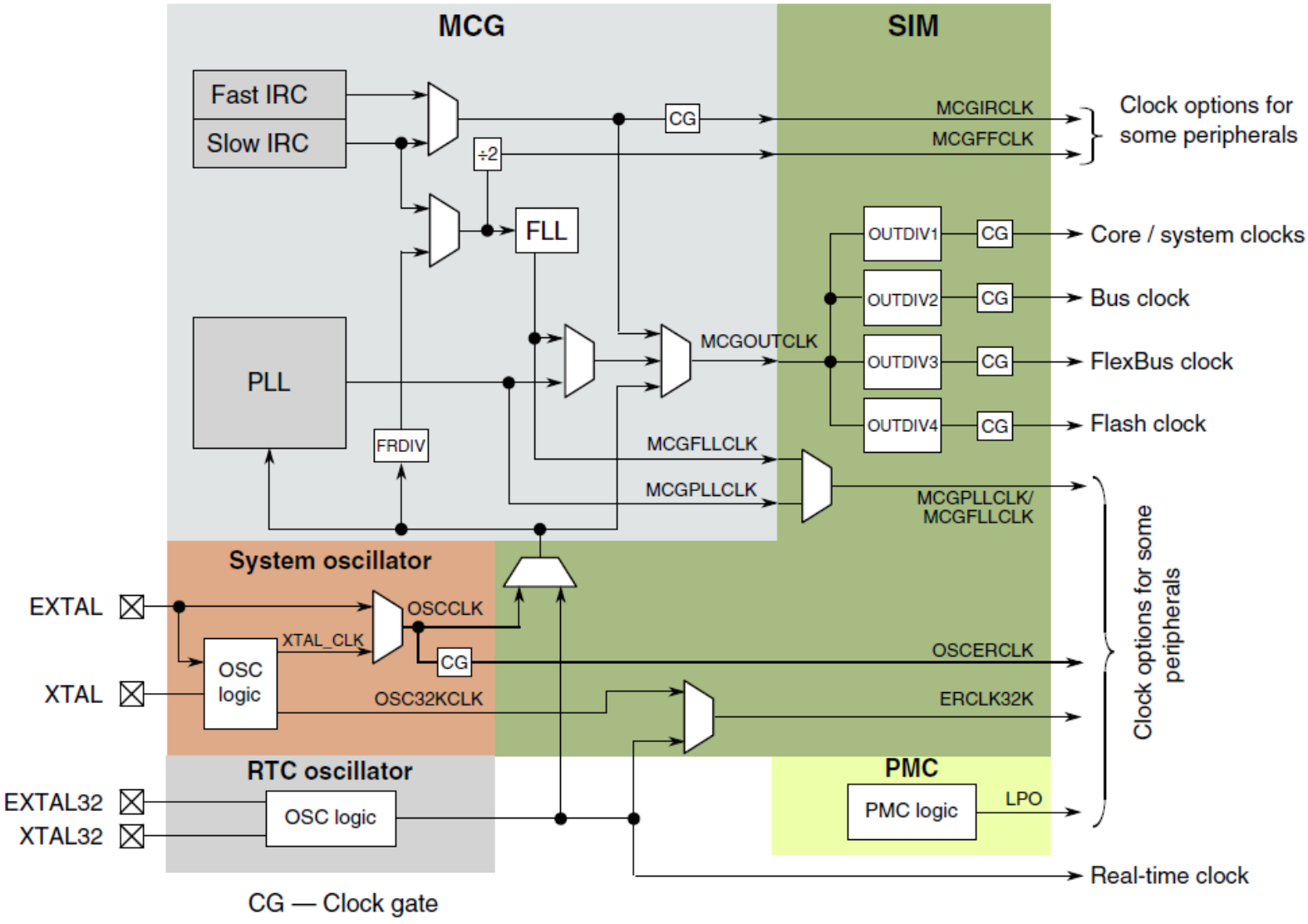
C[L]OCKS!


Master Modules
Slave Modules
Crossbar Switch
ARM core code bus
ARM core system bus
DMA
EzPort
Mux
Ethernet
USB
SDHC
M0
M1
M2
M3
M4
M5
S0
S1
S2
S3
S4
Memory protection unit (MPU)
Flash controller
SRAM backdoor
Peripheral bridge 0
Peripheral bridge 1
Mux
GPIO controller
MPU
FlexBus


Master Modules
Slave Modules
Crossbar Switch
ARM core code bus
M0
DMA
EzPort
Ethernet
M3
USB
M4
SDHC
M5
S0
S1
S3
S4
Memory protection unit (MPU)
Flash controller
SRAM backdoor
Peripheral bridge 0
Peripheral bridge 1
Mux
GPIO controller
MPU
FlexBus
Clocking requirements:
•Bus Interface clocking
•Internal module clocking
•I/O interface clocking
SEE TABLE 5-2, pg 185 of the TRM for sources of clocks for each module.

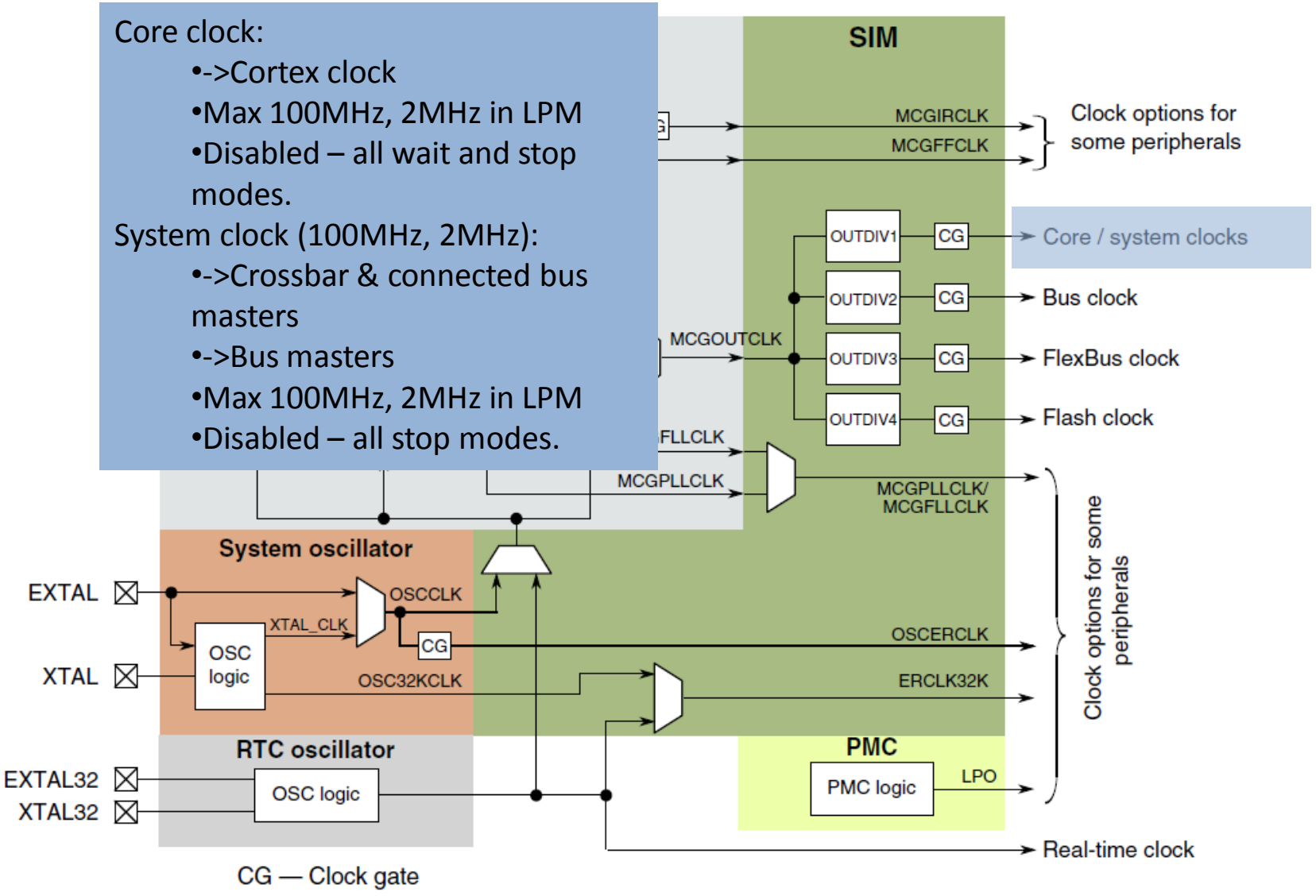

MCG
SIM
Fast IRC
Slow IRC
CG
MCGIRCLK
MCGFFCLK
Clock options for some peripherals
÷2
FLL
OUTDIV1
OUTDIV2
OUTDIV3
OUTDIV4
CG
Core / system clocks
Bus clock
FlexBus clock
Flash clock
PLL
MCGOUTCLK
FRDIV
MCGFLLCLK
MCGPLLCLK
MCGPLLCLK/
MCGFLLCLK
System oscillator
EXTAL
XTAL
OSC
logic
XTAL_CLK
OSCCLK
CG
OSCERCLK
OSC32KCLK
ERCLK32K
Clock options for some peripherals
RTC oscillator
EXTAL32
XTAL32
OSC logic
PMC
PMC logic
LPO
Real-time clock
CG — Clock gate

Core clock:

- ->Cortex clock
- Max 100MHz, 2MHz in LPM
- Disabled – all wait and stop modes.

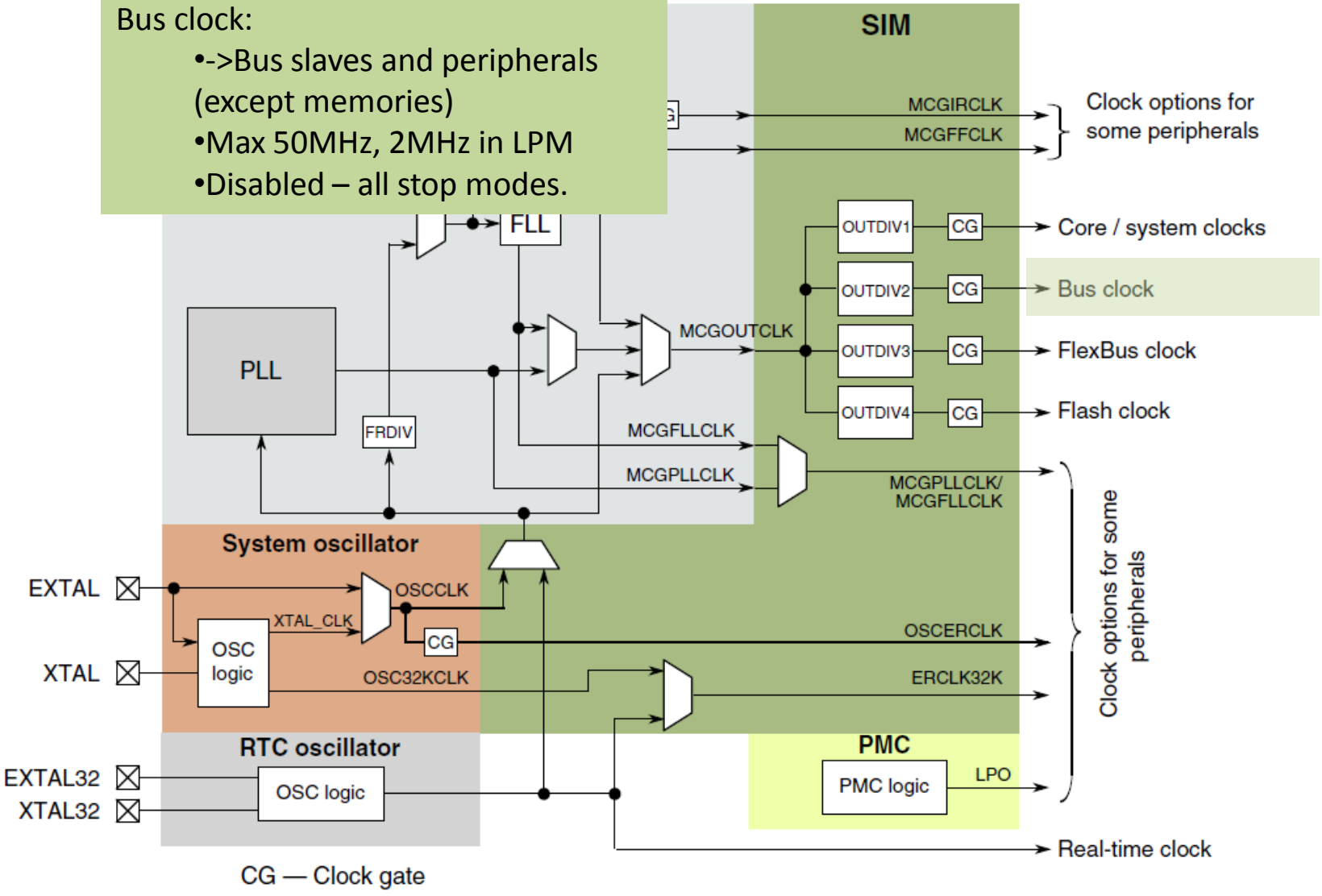
System clock (100MHz, 2MHz):

- ->Crossbar & connected bus masters
- ->Bus masters
- Max 100MHz, 2MHz in LPM
- Disabled – all stop modes.



Bus clock:

- ->Bus slaves and peripherals (except memories)
- Max 50MHz, 2MHz in LPM
- Disabled – all stop modes.

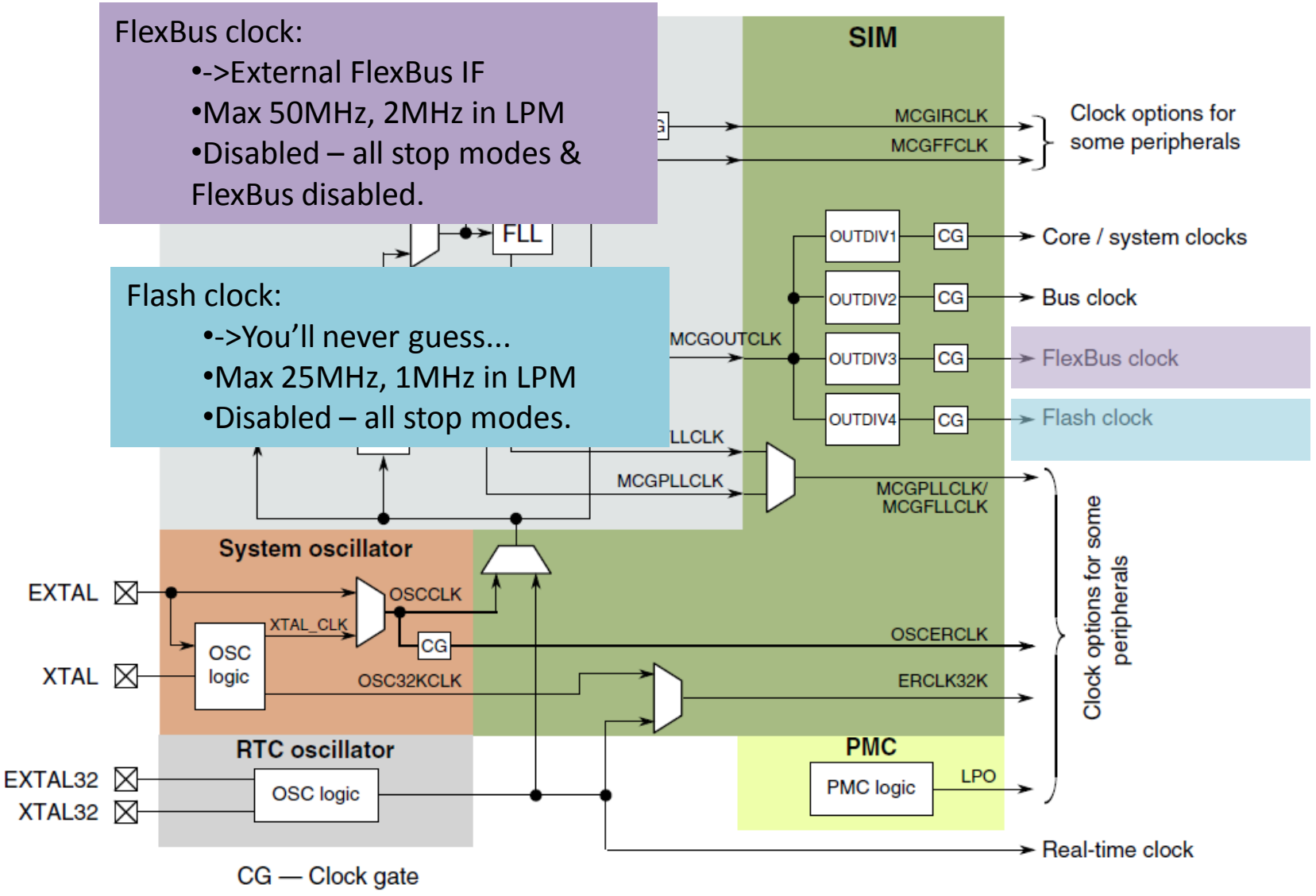


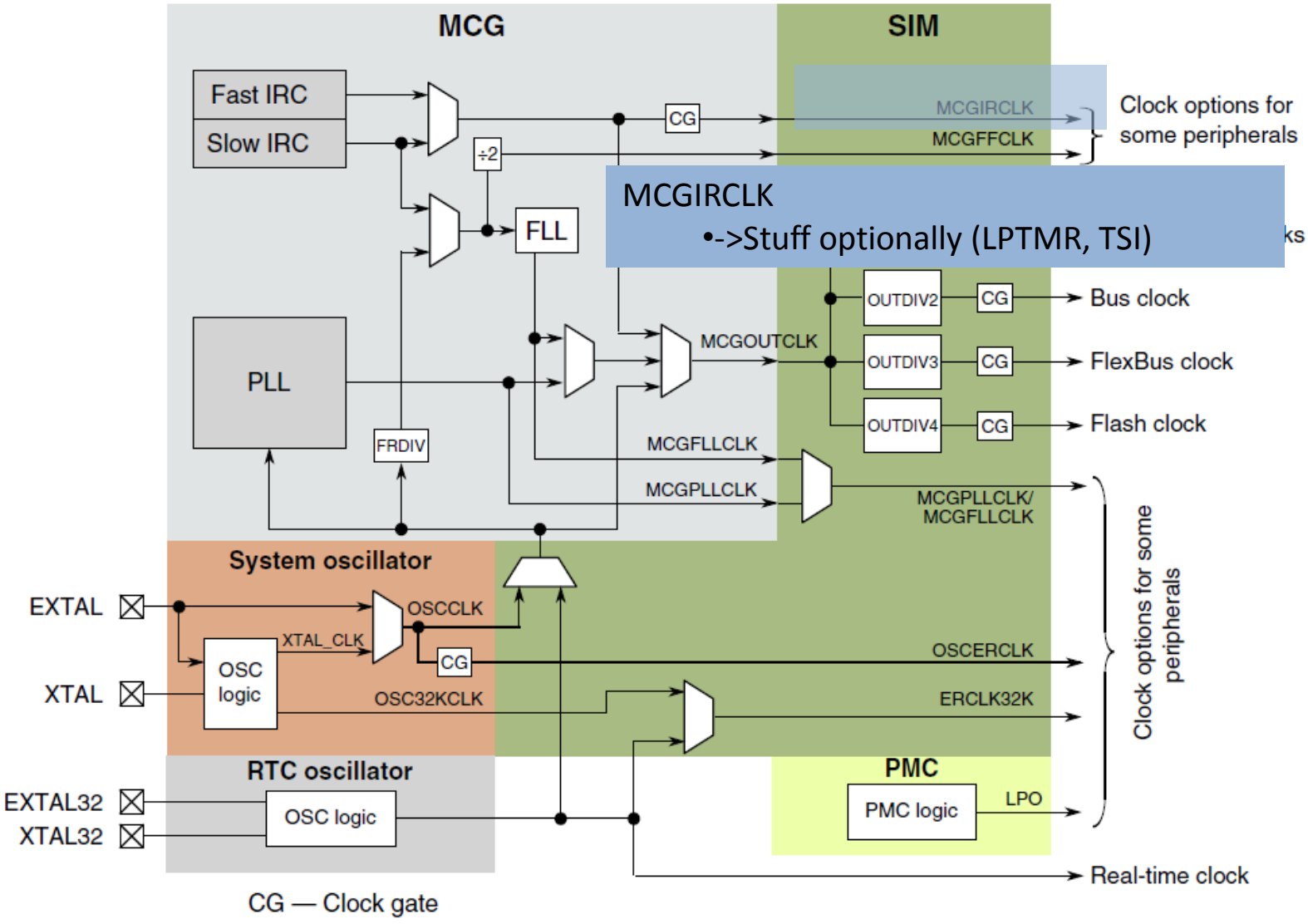
FlexBus clock:

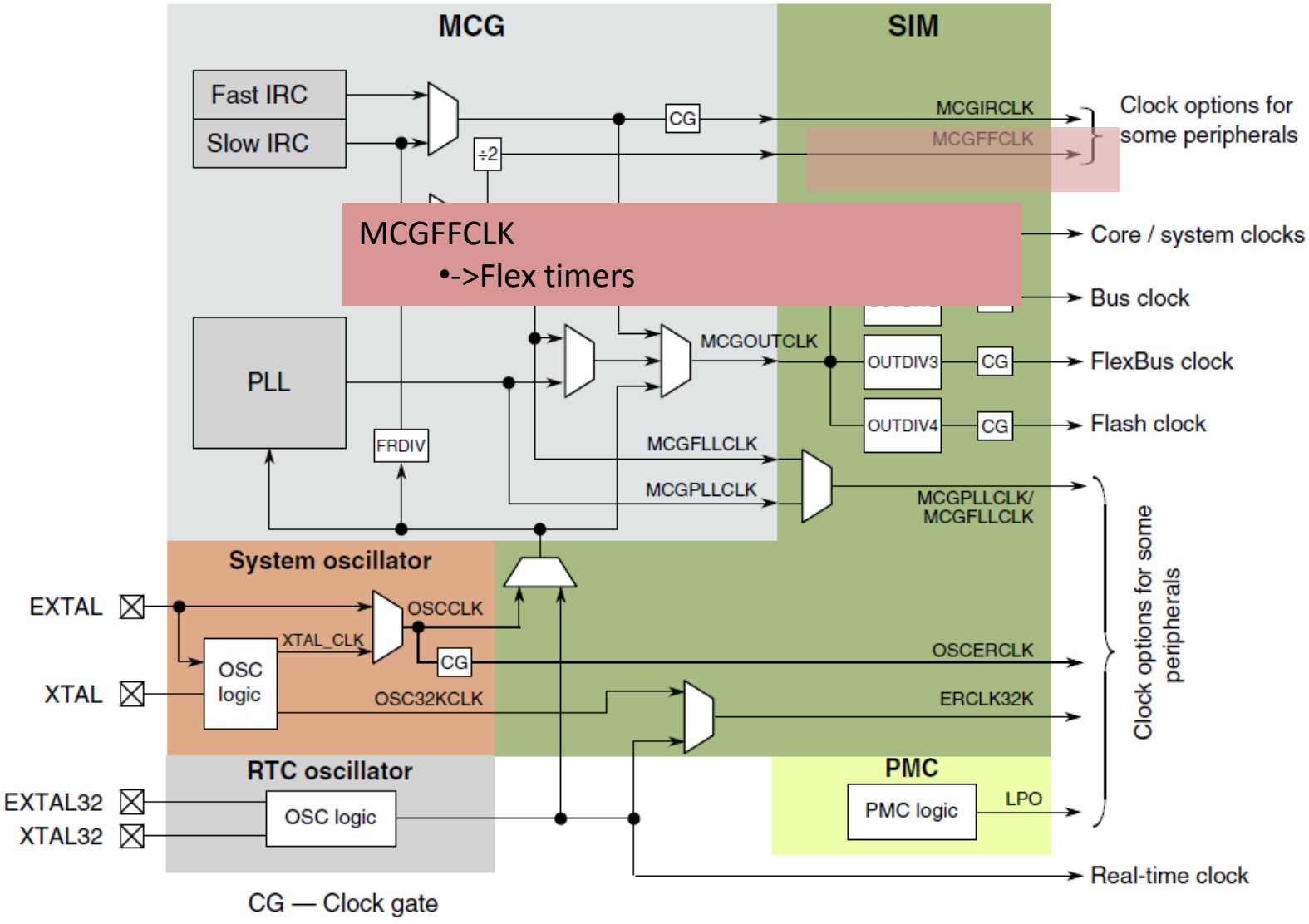
- ->External FlexBus IF
- Max 50MHz, 2MHz in LPM
- Disabled – all stop modes & FlexBus disabled.

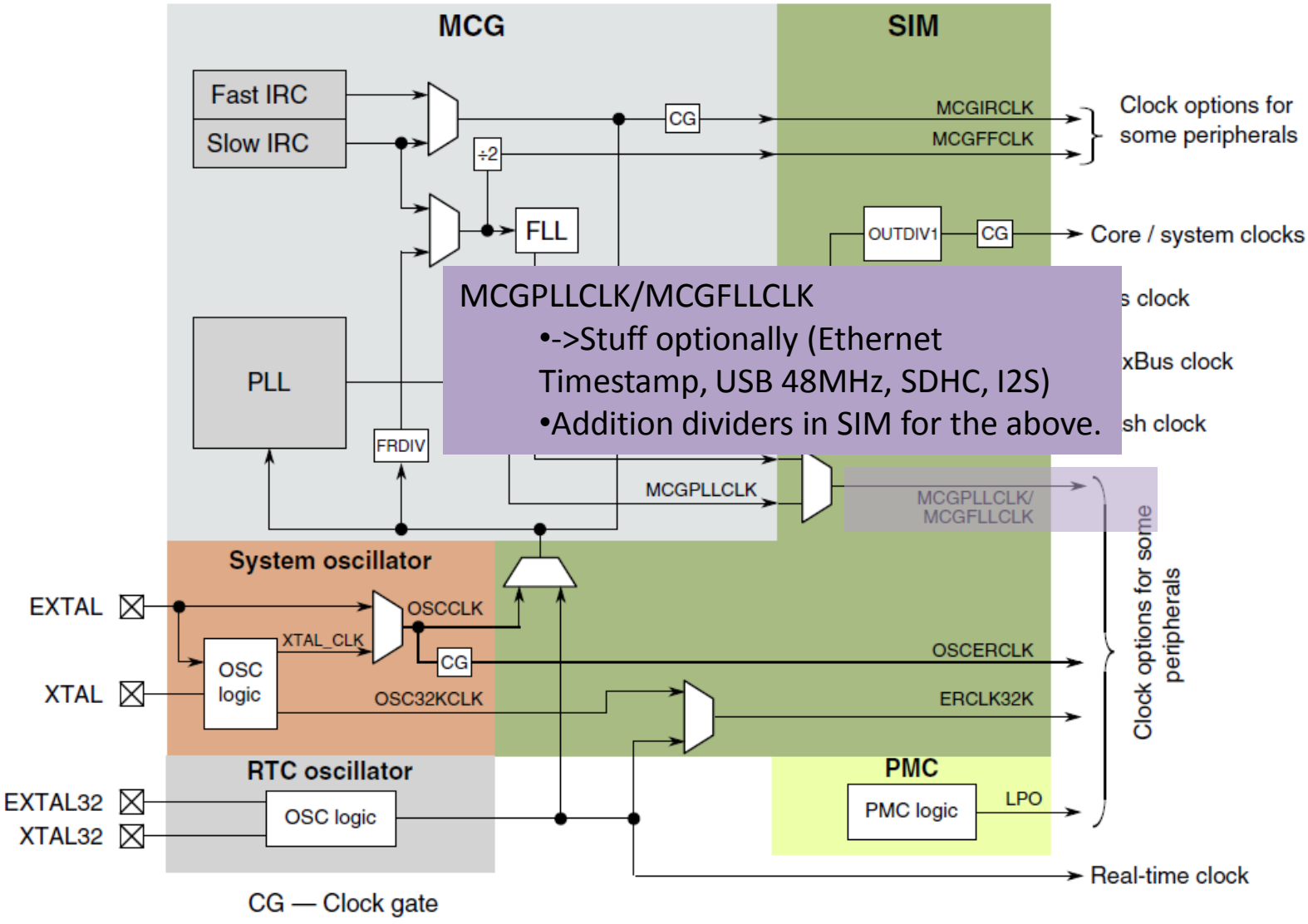
Flash clock:

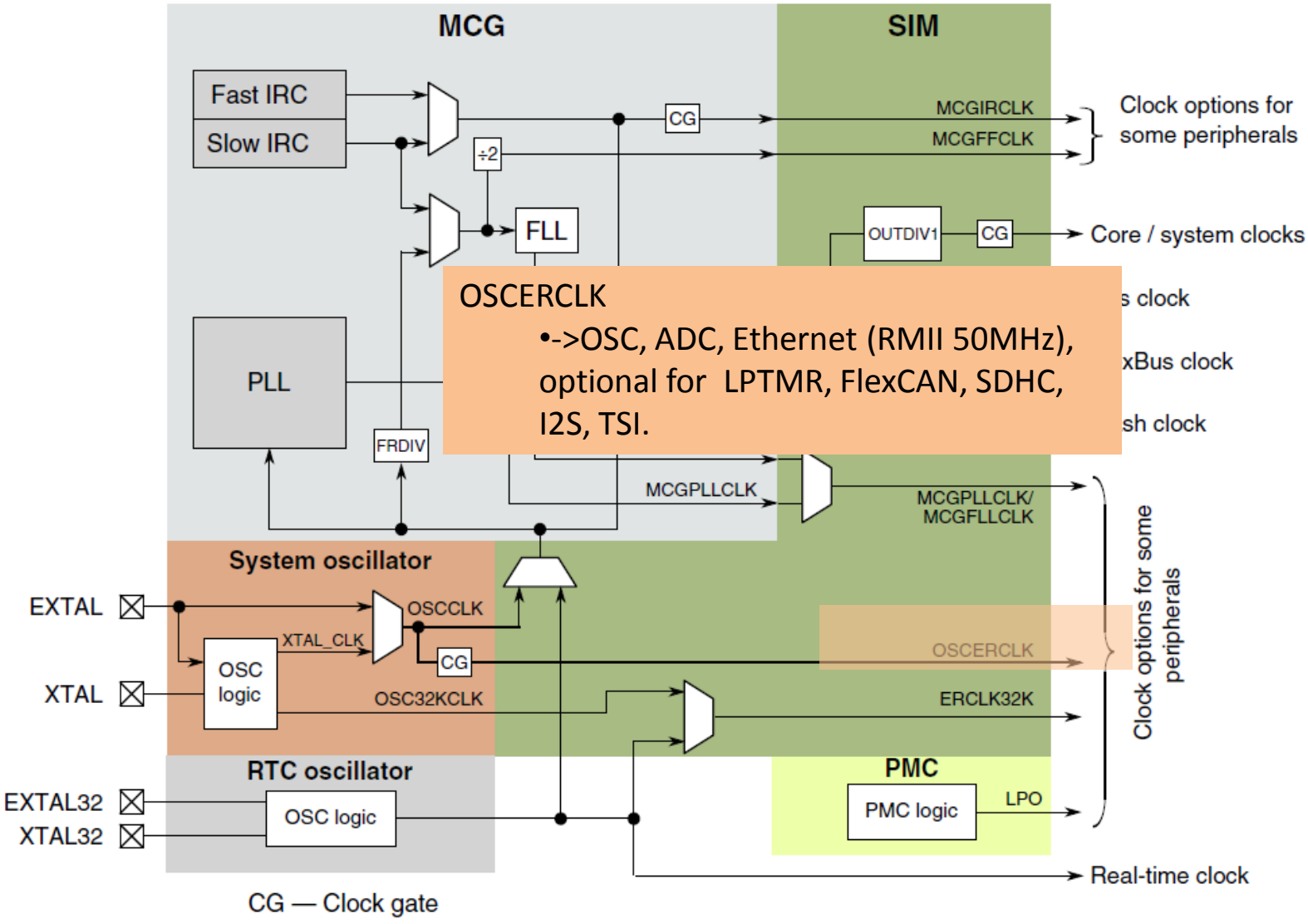
- ->You'll never guess...
- Max 25MHz, 1MHz in LPM
- Disabled – all stop modes.




MCG
SIM
Fast IRC
Slow IRC
CG
÷2
MCGIRCLK
MCGFFCLK
Clock options for some peripherals
MCGIRCLK
•->Stuff optionally (LPTMR, TSI)
FLL
PLL
FRDIV
MCGOUTCLK
OUTDIV2
OUTDIV3
OUTDIV4
CG
Bus clock
FlexBus clock
Flash clock
MCGFLLCLK
MCGPLLCLK
MCGPLLCLK/
MCGFLLCLK
System oscillator
EXTAL
XTAL
OSC logic
XTAL_CLK
OSCCLK
CG
OSCERCLK
OSC32KCLK
ERCLK32K
Clock options for some peripherals
RTC oscillator
EXTAL32
XTAL32
OSC logic
PMC
PMC logic
LPO
Real-time clock
CG — Clock gate

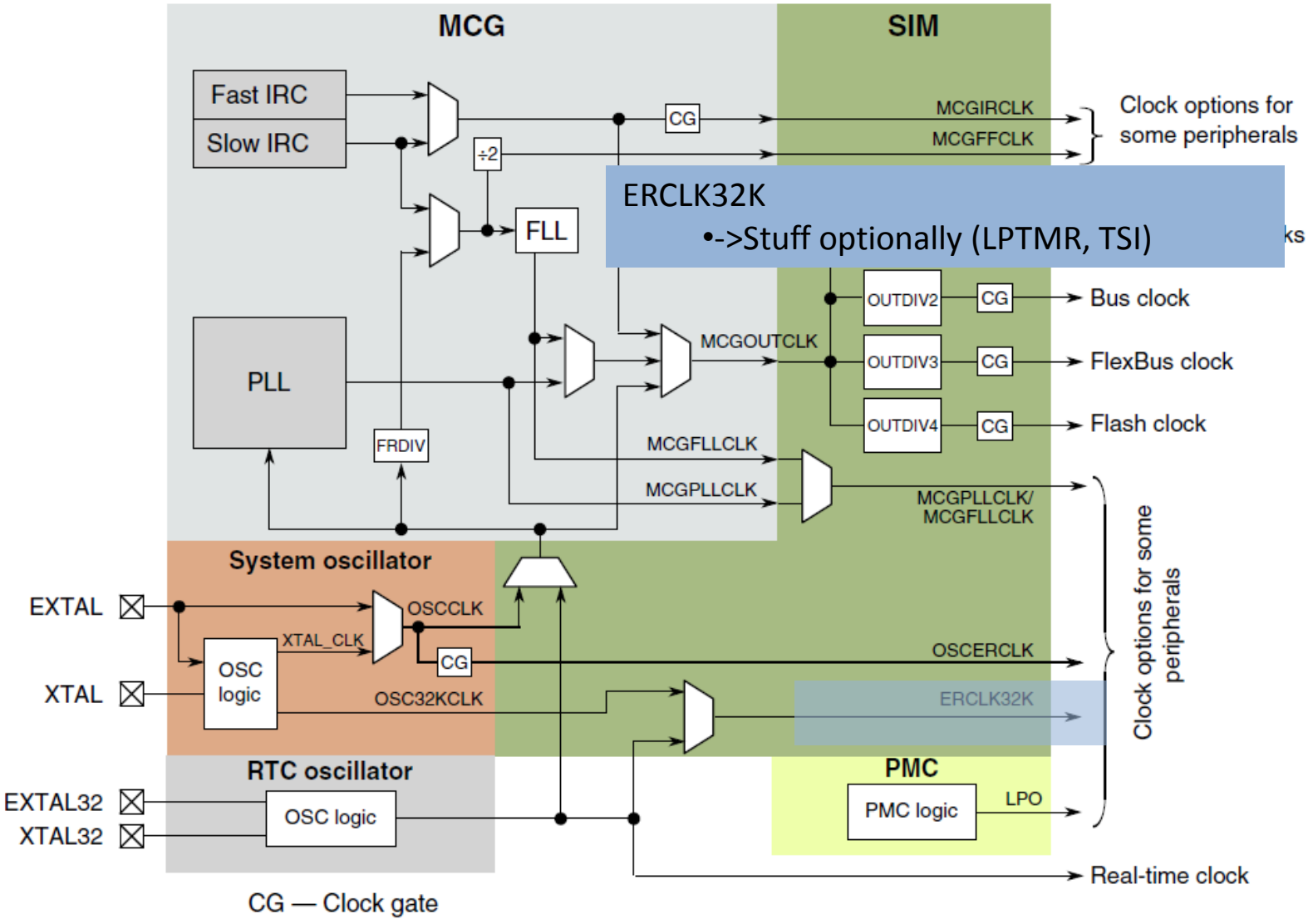

MCG
SIM
Fast IRC
Slow IRC
÷2
CG
MCGIRCLK
MCGFFCLK
Clock options for some peripherals
MCGFFCLK
•->Flex timers
Core / system clocks
Bus clock
PLL
MCGOUTCLK
OUTDIV3
CG
FlexBus clock
OUTDIV4
CG
Flash clock
FRDIV
MCGFLLCLK
MCGPLLCLK
MCGPLLCLK/
MCGFLLCLK
System oscillator
EXTAL
XTAL
OSC logic
XTAL_CLK
OSCCLK
CG
OSCERCLK
OSC32KCLK
ERCLK32K
Clock options for some peripherals
RTC oscillator
EXTAL32
XTAL32
OSC logic
PMC
PMC logic
LPO
Real-time clock
CG — Clock gate

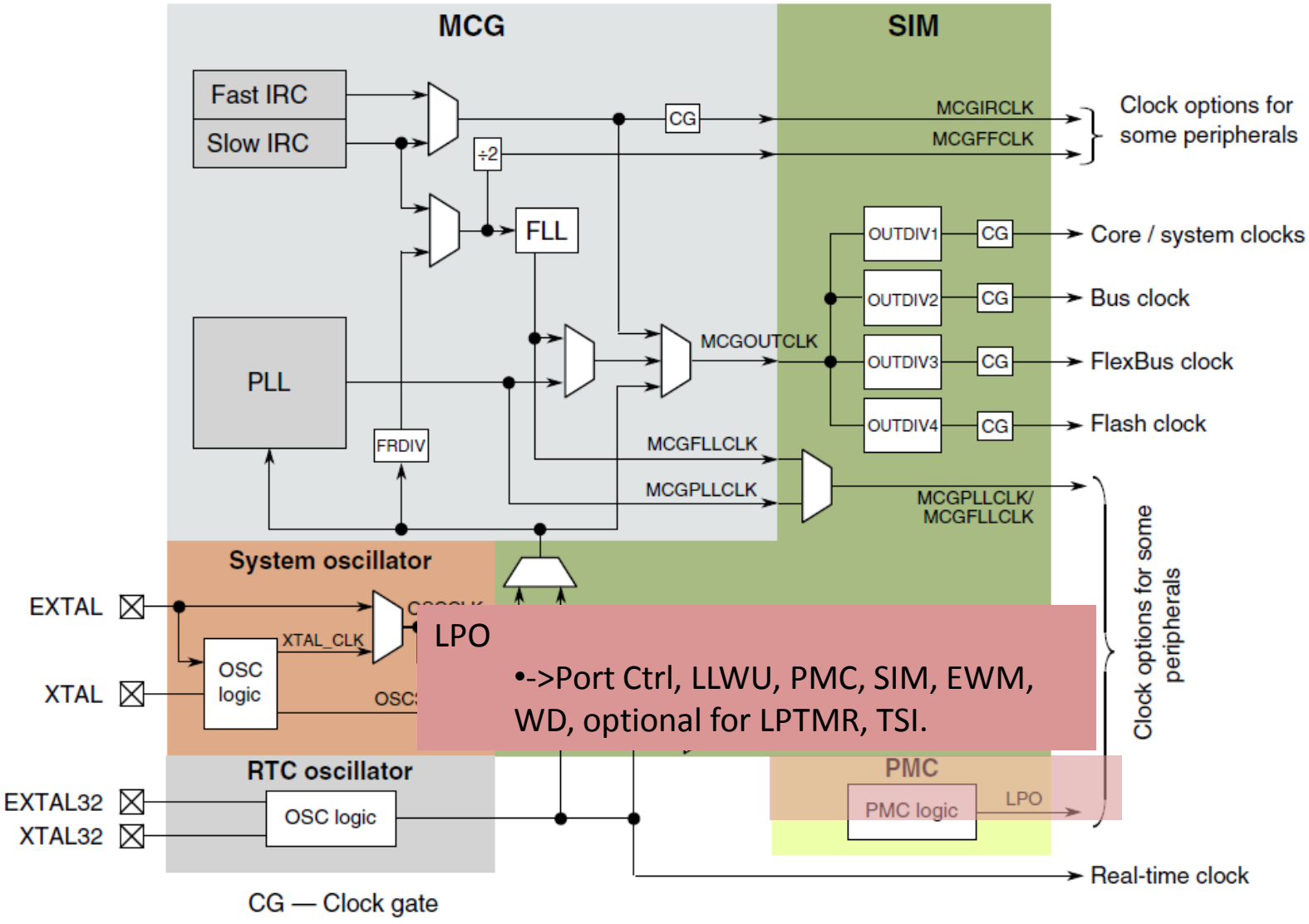

MCG
SIM
Fast IRC
Slow IRC
÷2
FLL
PLL
FRDIV
CG
MCGIRCLK
MCGFFCLK
Clock options for some peripherals
OUTDIV1
CG
Core / system clocks
MCGPLLCLK/MCGFLLCLK
•->Stuff optionally (Ethernet Timestamp, USB 48MHz, SDHC, I2S)
•Addition dividers in SIM for the above.
MCGPLLCLK
MCGPLLCLK/ MCGFLLCLK
System oscillator
EXTAL
XTAL
OSC logic
XTAL_CLK
OSCCLK
CG
OSC32KCLK
OSCERCLK
ERCLK32K
Clock options for some peripherals
RTC oscillator
EXTAL32
XTAL32
OSC logic
PMC
PMC logic
LPO
Real-time clock
CG — Clock gate



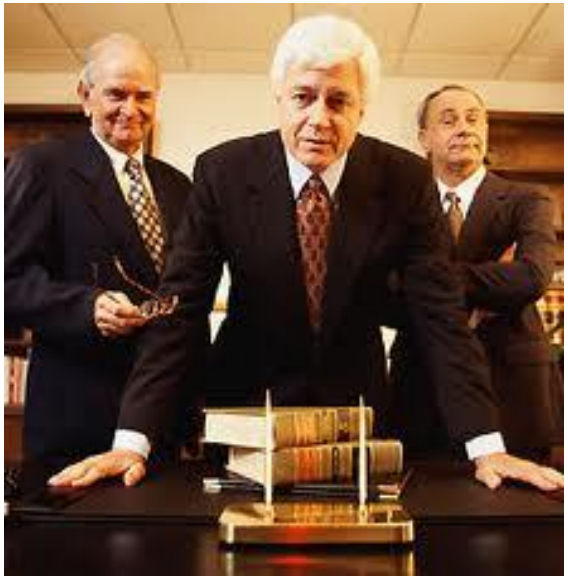
OSCERCLK

- ->OSC, ADC, Ethernet (RMII 50MHz), optional for LPTMR, FlexCAN, SDHC, I2S, TSI.


MCG
SIM
Fast IRC
Slow IRC
CG
MCGIRCLK
MCGFFCLK
Clock options for some peripherals
÷2
FLL
ERCLK32K
•->Stuff optionally (LPTMR, TSI)
PLL
MCGOUTCLK
OUTDIV2
OUTDIV3
OUTDIV4
CG
Bus clock
FlexBus clock
Flash clock
FRDIV
MCGFLLCLK
MCGPLLCLK
MCGPLLCLK/
MCGFLLCLK
System oscillator
EXTAL
XTAL
OSC logic
XTAL_CLK
OSCCLK
OSC32KCLK
OSCERCLK
ERCLK32K
Clock options for some peripherals
RTC oscillator
EXTAL32
XTAL32
OSC logic
PMC
PMC logic
LPO
Real-time clock
CG — Clock gate


MCG
SIM
Fast IRC
Slow IRC
CG
MCGIRCLK
MCGFFCLK
Clock options for some peripherals
÷2
FLL
OUTDIV1
OUTDIV2
OUTDIV3
OUTDIV4
CG
Core / system clocks
Bus clock
FlexBus clock
Flash clock
MCGOUTCLK
PLL
FRDIV
MCGFLLCLK
MCGPLLCLK
MCGPLLCLK/
MCGFLLCLK
System oscillator
EXTAL
XTAL
XTAL_CLK
OSC
logic
LPO
•->Port Ctrl, LLWU, PMC, SIM, EWM, WD, optional for LPTMR, TSI.
Clock options for some peripherals
RTC oscillator
EXTAL32
XTAL32
OSC logic
PMC
PMC logic
LPO
Real-time clock
CG — Clock gate

The Fine Print



- The core and system clock frequencies must be 100 MHz or slower.
- The bus clock frequency must be programmed to 50 MHz or less and an integer divide of the core clock.
- The flash clock frequency must be programmed to 25 MHz or less and an integer divide of the bus clock.
- The FlexBus clock frequency must be programmed to be less than or equal to the bus clock frequency.
- FLL input: 31kHz – 39kHz.
- PLL input: 2MHz – 4MHz.

Errata:
3801 MCG: In FEE and FEI Modes, the FLL output may stop when the DCO range is changed.
2553 MCG: MCGPLLCLK stalls for 2 PLL cycles if MCG_C5 is written to after the PLL is enabled.
2556 MCG: PLLCLKEN may not always enable the PLL.
2796 MCG: Slow Internal Reference Clock Operating Range does not meet specification.
2555 MCG: The DCO within the FLL cannot reach the minimum specified frequency.
2660 MCG: The PLL can be enabled in bypassed low power mode (BLPE) when the system is in normal stop mode.
3580 MCG: Total deviation of trimmed average DCO output frequency over voltage and temperature does not meet specification.
2554 MCG: When trimming the slow Internal Reference Clock (IRC) using the auto trim machine (ATM), the IRC is not automatically enabled.
666 WTF: Board occasionally bursts into flames for unknown reasons.

Common Cfgs

Option 1:
Core clock 50 MHz
System clock 50 MHz
Bus clock 50 MHz
FlexBus clock 50 MHz
Flash clock 25 MHz

Option 2:
Core clock 100 MHz
System clock 100 MHz
Bus clock 50 MHz
FlexBus clock 25 MHz
Flash clock 25 MHz

Option 3:
Core clock 96 MHz
System clock 96 MHz
Bus clock 48 MHz
FlexBus clock 48 MHz
Flash clock 24 MHz

Typical Startup (doc_quick-ref-KQRUG.pdf)

- Disable watchdog
- Initialize RAM
- **Enable port clocks**
- **Ramp system clock to selected frequency**
- Enable pin interrupt
- Enable UART for terminal communication
- Jump to start of main function for application

MCG Modes

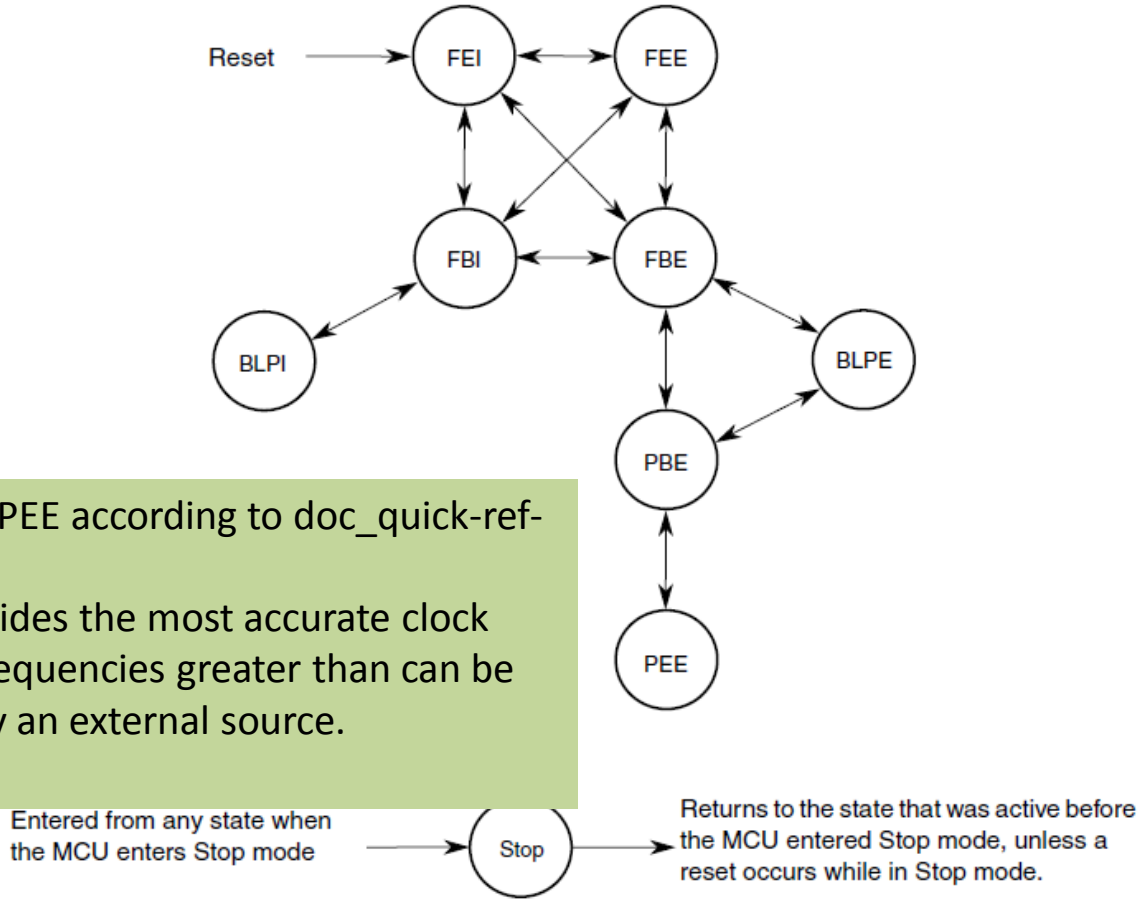
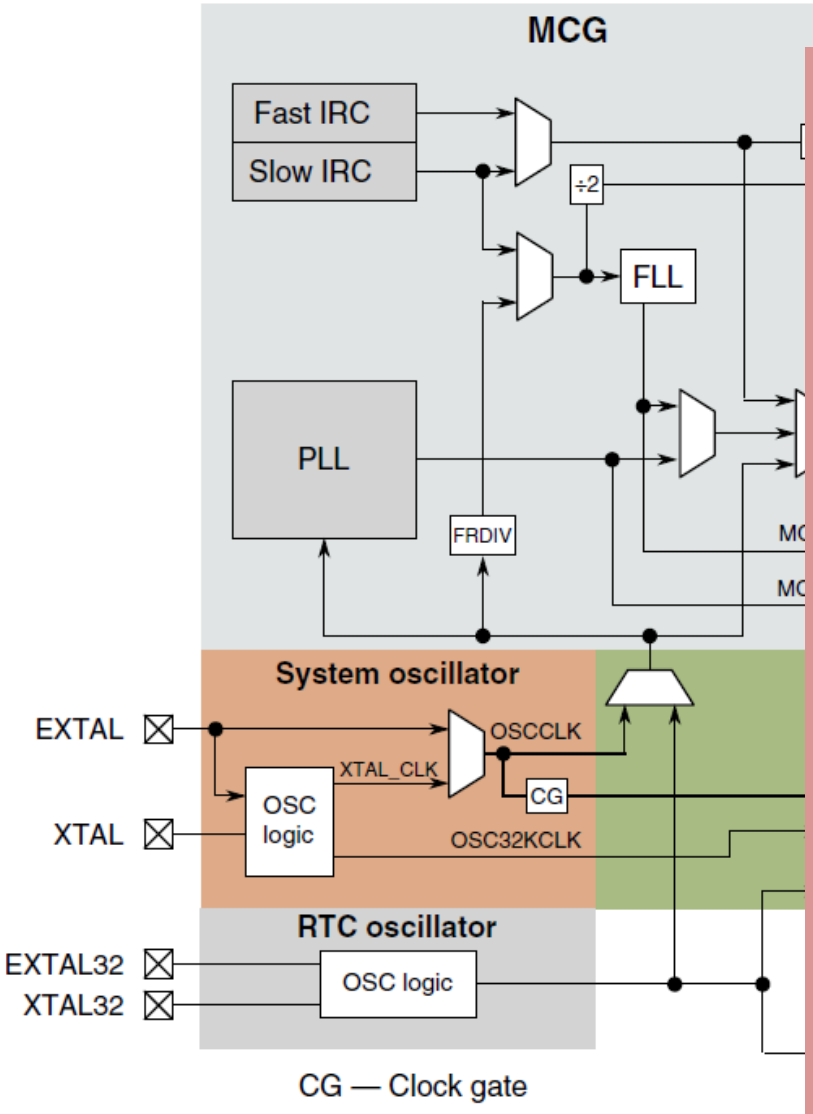


Figure 24-12. MCG Mode State Diagram

The need to PEE according to doc_quick-ref-KQRUG.pdf:
The PLL provides the most accurate clock source for frequencies greater than can be generated by an external source.



PLL

From doc_manual-TWR-K60N512-UM.pdf:

1. The external oscillator for the Multipurpose Clock Generator (MCG) module can range from 32.768 KHz **up to a 32 MHz** crystal or ceramic resonator.
2. The EXTAL pin of the main external oscillator can also be driven directly from an external clock source. The TWR-K60N512 features a **50 MHz** on-board clock oscillator as seen in sheet 4 of the schematics.

From doc_refman-K60P100M100SF2RM.pdf:

1. Do not use PLL if using an external clock source less than 2 MHz (e.g. EXTAL32).

Conclusion:

- Can't use PLL with default EXTAL source! (wtf?…)
- Found that 50MHz works in practice. Maybe the 32MHz is only if using the OSC with a crystal (?)

The example

- Set jumper J3 to 1-2 TWR-SER CCA (Route 25MHz clock to CLOCKIN0).
- Set jumper J6 2-3 on TWR-K60N512 CCA (Route CLKIN0 to EXTAL).
- **Go from FEI to PEE: 25MHz EXTAL, MCGOUTCLK Freq = 100MHz with fail safe to fast IRC (4MHz) FEI 20MHz.**