Understanding and Optimizing Deep Learning Cold-Start Latency on Edge Devices

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ABSTRACT

DNNs are ubiquitous on edge devices nowadays. With its increasing importance and use cases, it's not likely to pack all DNNs into device memory and expect that each inference has been warmed up. Therefore, cold inference, the process to read, initialize, and execute a DNN model, is becoming commonplace and its performance is urgently demanded to be optimized. To this end, we present NNV12, the first ondevice inference engine that optimizes for cold inference. NNV12 is built atop 3 novel optimization knobs: selecting a proper kernel (implementation) for each DNN operator, bypassing the weights transformation process by caching the post-transformed weights on disk, and pipelined execution of many kernels on asymmetric processors. To tackle with the huge search space, NNV12 employs a heuristic-based scheme to obtain a near-optimal kernel scheduling plan. We fully implement a prototype of NNV12 and evaluate its performance across extensive experiments. It shows that NNV12 achieves up to 15.2× and 401.5× compared to the state-of-the-art DNN engines on edge CPUs and GPUs, respectively.

1 INTRODUCTION

Deep Neural Networks (DNNs) have been landed to myriads of areas from computer vision [54] to natural language understanding [63]. Pursuing low inference delay and data privacy, DNN deployment is shifting from large data centers to humble edge devices, e.g., smartphones, IoT, wearables, and autonomous vehicles [24]. To unleash the power of those edge devices for DNNs, a mass of research efforts have been invested by our community [27, 37, 40, 55, 56, 61, 64].

There are two notable trends of on-device DNN deployments: (1) The number of DNNs per device is explosively increasing. We follow a prior work [58] to dig into the DNN usage of Google Play apps, and find that the number of DNN-embedded apps has increased by 260% within less than 3 years from Jun. 2018 to Mar. 2021. Those apps have been downloaded by billions of times. Indeed, on-device DNNs multitasking has been de facto not only in smartphones but also Home Hubs [2], cameras [60] and robots [20], etc. (2) The complexity of DNNs are increasing as well. Bert [26], the state-of-the-art network for NLP tasks, has been deployed

on mobile devices for many killer apps like QA [1]. Though after compression, it still takes more than 100MB memory.

Those trends highlight the crowdedness of DNNs on resource constrained devices. Consequently, it's not likely to pack all DNNs into device memory and expect that each-time DNN inference has been warmed up. In other words, *cold inference*, i.e., the process to load, initialize and execute a DNN model, is becoming commonplace. Alike warm inference, the speed of cold inference matters critically to the user experience and application QoE. Here we list a few examples.

- A mobile browser needs to cold-start a language translation model immediately when a user opens a specific web page to guarantee a short page load time (PLT) [45].
- An auto-driving car or robot need to cold-start an obstacle detection model quickly to avoid running into an accident, either after the model is cleared from memory intentionally or the DL execution engine crashes unintentionally [57].
- A Home Hub needs to quickly cold-start a speech recognition model to guarantee its smooth interaction with users [34].

Unfortunately, the state-of-the-art DNN engines including TFLite [12] and ncnn [10] are not ready to boost cold inference as fast as warm inference. As we will quantitatively show in §2, the cold inference latency of those engines is 3.1×-12.7× and 85.5×-443.5× slower than warm inference on CPU and GPU, respectively. Taking a step closer, we find the major bottlenecks of cold inference include reading the weights from disk into memory (weights reading), converting raw weights into an execution-ready format (weights transformation), and the actual model execution. Those complicated operations distinguish cold inference from traditional warm inference and invalidate most of the techniques brought by prior work in optimizing the inference speed.

There are two main related research fields that can possibly mitigate such high cold inference latency. One is through *DNN weights sharing* that aims to pack more DNNs into device memory so each DNN inference is pre-warmed [21, 23, 40, 42]. Those methods, however, are not scalable as with more DNNs the model accuracy drops significantly. Or, one may pre-warm a DNN model by predicting when it will be needed [17, 48, 62]. However, we suspect that it is difficult to precisely predict when a model will be needed.

Both above approaches address the cold inference problem in an *indirect* manner, relying on altering the models

structures or external knowledge. Instead, for the first time, we propose a system named NNV12 that *directly* optimizes the DNN cold inference latency on edge devices. NNV12 does not rely on any assumptions of model structures or runtime environment, and incurs zero accuracy loss.

Optimization knobs (§3.2) We first thoroughly explore the design spaces of cold inference and identify three effective optimization knobs that are rarely touched on in previous literature. (1) The selection of kernel. DNN engines typically incorporate many different implementations for one single operator (namely kernel), e.g., 28 for convolution in ncnn. Those built-in kernels are to improve the inference speed under specific operator configurations, and the current strategy of kernel selection is purely based on its warm inference speed. However, a key observation we make is that the fastest kernel in warm inference does not necessarily exhibit the best performance in cold inference, e.g., a winogradbased kernel [39] executes fast but spends much time in weights transformation resulting in long cold inference delay. (2) Post-transformed weights caching. Weights transformation can be bypassed by storing the post-transformed weights on disk so they can be directly read and executed. However, the transformed weights might occupy more storage and incur higher I/O time. Reading raw or post-transformed weights opens tradeoff among disk I/O and computations. (3) The order of operator execution and core binding The weights reading, transformation, and execution can be pipelined to reduce the blocking time of disk/memory I/O. The pipeline technique can also orchestrate with the asymmetric processor on edge devices, .e.g., CPU/GPU and BIG.little core, which can hardly be fully utilized in executing DNNs sequentially.

Formulation and challenges (§3.3) The above optimizations need to be jointly considered because their impacts on cold inference are tightly coupled, e.g., choosing a different kernel could overturn an optimal pipeline strategy. To design a holistic and judicious cold inference scheme, we face two primary challenges. First, the search space is too large. We formulize the problem in combined kernel selection, transformation bypassing, and execution pipeline to obtain an optimal kernel scheduling plan. The problem turns out to be NP-hard. Second, the placement of different operations (reading, transformation, and execution) could interfere with each other due to the limited disk/memory I/O bandwidth, which further complicates the problem.

A heuristic-based kernel scheduling algorithm (§3.4) It is inspired by a few key observations such that (1) There exists operation-processor affinity, e.g., the BIG vs. little core acceleration ratio is more significant for kernel execution than weights reading and transformation. Therefore, the kernel execution is always prioritized on the stronger processor. (2) Multithreading on multiple cores is more efficient on execution operation than others. Hence we only use BIG

cores to multithread the execution operation while placing the reading/transformation operations on little cores separately. It also exploits the opportunity that weights reading/transformation operations have fewer dependencies than execution operations, therefore can be easily scheduled individually.

Atop those heuristics, we design an intuitive yet effective kernel scheduling algorithm. Its key idea is to balance the workloads on different processors or cores to minimize the total running time. Meanwhile, during the decision making, NNV12 keeps calibrating the per-operation performance through re-profiling for better scheduling planning. We then extend the above design to the GPU platform (§3.5) by introducing new GPU-specific operations into the scheduling pipeline and a shader caching technique. Furthermore, to ensure that the kernel selection for cold inference will not compromise the warm inference latency in continuous inference tasks (§3.6), NNV12 leverages the spare CPU time slots during cold inference to prepare for warm inference.

We've implemented a prototype of NNV12 atop ncnn that fully realizes the above techniques. We then perform extensive experiments to evaluate NNV12's performance through 12 typical DNN models and 4 devices including 2 smartphones (CPU) and 2 Jetson embedded devices (GPU). The results show that, on Meizu 16T CPU, NNV12 can reduce the cold inference latency by $5.1\times/9.5\times/3.7\times$ at average compared to ncnn, tflite, and AsyMo [55], respectively. On Jetson TX2 GPU, the improvement is even up to $58.2\times/401.5\times$ compared to ncnn and TensorFlow, respectively. NNV12 also greatly reduces the energy consumption of cold inference. The ablation study further shows that each individual technique of NNV12 contributes to significant improvements.

The major contributions of this work are:

- We highlight the importance of NN cold inference and reveal the unsatisfactory support for cold inference quantitatively on the state-of-the-art DNN engines.
- We identify three optimization knobs that can effectively reduce the cold inference latency yet are underexplored in prior literature: kernel selection, weights transformation bypassing, and pipelined inference.
- We propose a holistic framework NNV12 that judiciously considers the three above optimization knobs through a heuristic-based kernel scheduling.
- We implement a prototype of NNV12 and demonstrate its effectiveness through extensive experiments.

2 UNDERSTANDING NN COLD START

We first perform a set of measurement studies to understand cold inference on edge devices. We use two typical devices: Google Pixel 5 smartphone with Kryo 475 CPU [8] and Jetson TX2 with NVIDIA Pascal GPU [4]. We experiment with 3

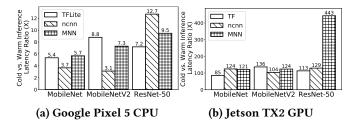


Figure 1: Cold inference is significantly slower $(3.1 \times -443.5 \times)$ than warm inference on vanilla DL libraries.

Device Platform	Google Pixel 5	Jetson TX2
Processor	CPU	GPU
Weights reading	36.52 ms	43.03 ms
Memory allocation	1.34 ms	0.69 ms
GPU preparation	-	3004.01 ms
Weights transformation	1135.28 ms	1616.84 ms
Model execution	190.12 ms	802.77 ms
Total cold inference	1363.23 ms	5467.48 ms
Warm inference	185.82 ms	137.02 ms

Table 1: A breakdown of ResNet-50 cold inference latency on edge CPU and GPU.

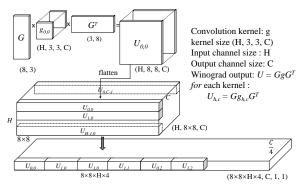


Figure 2: The weights transformation example for a winograd-based convolution kernel [39].

DNN models (MobileNetv1/v2, ResNet-50) on 3 popular DL libraries: TFLite/TF, ncnn [10], and MNN [33].

Figure 1 illustrates the performance gap between cold and warm inference on the above hardware and libraries. As observed, the gap is 3.1×-12.7× on CPU and 85.5×-433.5× on GPU. Concretely, the cold inference latency of ResNet-50 on Kryo 475 CPU takes at least 511.67 ms, while the warm inference only takes 141.56 ms. Such huge gap can inevitably hurt the user experience under scenarios as described in §1. **Cold inference breakdown** We then investigate the cold inference process internally. While different DL libraries differ in implementation, conceptually their cold inference mainly includes the following stages:

- **Memory allocation**: requesting memory from OS to hold the weights and intermediate results during inference.
- **Weights reading**: reading the model weights from device storage into memory.

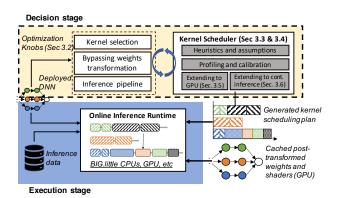


Figure 3: The simplified workflow of NNV12.

- Weights transformation: converting raw weights into the proper format to facilitate the inference. This process depends on the kernel implementation for each operator. For example, as shown in Figure 2, in a winograd-based convolution kernel [39], the weights will be transformed from size (H, 3, 3, C) to $(8 \times 8 \times H \times 4, \frac{C}{4}, 1, 1)$.
- **Model execution**: the actual inference (forward) process by invoking each operator of the model.
- **GPU preparation** (only for GPU): setting up the GPU driver, creating data pipeline, compiling shader codes, etc.

Table 1 shows the breakdown of cold inference with ResNet-50. On both CPU and GPU, each stage except memory allocation contributes to a considerable portion of the slow cold inference. To obtain an acceptable cold inference latency, we need to optimize each of the above stages.

3 NNV12 DESIGN

3.1 Overview

NNV12 is designed to enable fast NN cold inference on edge devices with the following principles:

- It shall sacrifice zero prediction accuracy.
- It shall require minimal additional efforts from developers.
- It builds atop DL kernels that are already existing in DL libraries. Generating better-optimized kernels is not our contribution and is orthogonal to this work.

The workflow of NNV12 consists of two main stages as shown in Figure 3: offline decision generation and online cold inference runtime. The decision stage is to generate an optimal kernel scheduling plan for a huge design space as explored in §3.2. This stage runs fully automatically on device for one shot, e.g., when a model is fetched to the device, so the decision is optimized for different devices' hardware capacity and requires no efforts from developers. NNV12 follows the generated plan to optimize the cold inference at runtime.

From developers' perspective, NNV12 is like traditional DL inference libraries in deployment. Internally there are three key differences. First, NNV12 registers many kernels to one

S1:sgemm	S2:sgemm_pack4	S3:1x1s1_sgem	m S4:1x1s1_sgemm_pack4
S5:1x1s1_sge	emm_pack4to1		S6:1x1s2_sgemm_pack4
S7:3x3s2_sge	emm_pack4 W1:3	3x3s1_winograd	W2:3x3s1_winograd_pack4
W3:3x3s1_w	inograd_pack4to1	P1:pack4	P2:pack4to1 P3:pack1to4
P4:3x3s1_pa	ck1to4 P5:3x3s2_p	oack4 P6:3x3s2	_pack1to4 P7:5x5s1_pack4
P8:5x5s2_pa	ck4 P9:7x7s2_pac	k1to4 G1:vani	lla G2:1x1s1 G3:1x1s2
G4:3x3s1	G5:3x3s2 G6:4x4s4	G7:5x5s1 G8:5	x5s2 G9:7x7s2

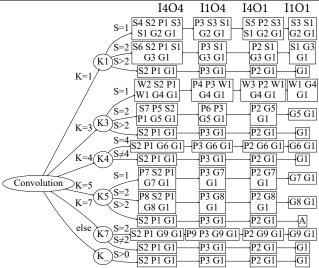


Figure 4: The 28 kernels implemented by ncnn for convolution. On the top box, "A:B" indicates "B" is a kernel implemention and abbreviated as "A". Within the tree structure, each node (as rectangle) contains the usable kernels for each situation. K/S indicate the convolutional kernel size and stride size. "I4O4" means the input and output channels are divisible by 4.

operator and can possibly select any of them based on the offline decision-making. Instead, traditional DL libraries use a static policy to select kernels based on heuristics without considering the hardware heterogeneity and the preparation stages of cold inference. Second, NNV12 might bypass the weights transformation stage by directly loading the post-transformed weights into memory. Third, NNV12 judiciously pipelines the weights reading from disk, weights transformation, and kernel execution on heterogeneous processors of edge devices. All those design points are jointly considered and addressed by NNV12's kernel scheduler (§3.4).

3.2 Optimization Knobs

We first discuss the optimization knobs that can be explored: kernel selection, weights transformation bypassing, and inference pipeline. While being intuitive, those optimizations have been rarely touched in prior work.

3.2.1 Kernel selection. A DNN model can be represented as a directed data graph consisting of many operators. An operator describes how the input data is mapped to output

Kernels	Cold Inference Time (ms)					
Kerners	Read	Weights	Read	Execution		
	Raw	Trans.	Cache	Execution		
3x3s1-winograd-pack4	0.70	38.23	5.23	2.98		
sgemm-pack4	0.70	2.21	0.70	8.14		
pack4	0.70	2.22	0.70	18.63		
3x3s1-winograd	0.70	65.67	4.12	3.37		
3x3s1	0.70	0.00	0.70	8.01		
general	0.70	0.00	0.70	87.12		

Table 2: The weights transformation (on CPU little cores) and execution time (on CPU BIG cores) of different kernel alternatives for conv op (kernel size = 3, stride = 1, input/output size = 64/192). "Read Raw/Cache" is the I/O time of reading the weights w/o and with cache policy (i.e., pre-transformed).

data at a high level, while the "kernels" are referred to how such mapping is implemented concretely.

One operator, many kernels A key observation we make from existing DL libraries is that there are often multiple kernels implemented for one operator, especially those computation-intensive ones. For instance, as shown in Figure 4, ncnn implements 28 different kernels for convolutional operator.

There are three main reasons for such phenomenon. (1) Kernels can be better optimized with assumptions on the input/weights configurations, e.g., the convolution kernel size and input/output channel numbers. (2) The relative kernel performance relies on the specific hardware platforms. Therefore, developers write multiple kernels to obtain good performance on different platforms by choosing the best fitting. (3) New kernels are emerging but the old ones are kept in the codebase for legacy reasons.

No silver-bullet kernel The current kernel selection policy of popular DNN engines is hard-coded and only considers the warm inference speed. However, such selection may not be optimal for cold inference. Taking ncnn as an example, as we quantitatively show in Table 2, the default kernel used by ncnn for convolution operators with 4x input/output channel numbers and 3x3 convolution kernel size is a winograd-based implementation (3x3s1-winograd-pack4) because it achieves the fastest warm inference. Such a kernel, however, incurs a high time cost in weights transformation. Instead, a more generic sgemm-based implementation (sgemm-pack4) has less total time cost with simpler weights transformation.

3.2.2 Bypassed weights transformation. As shown above, the weights transformation for certain kernels can be extremely costly, despite that the kernel executes quite fast. One possible method to avoid the heavy transformation while leveraging the kernel's fast execution is to cache the transformed weights on disk, which can be directly loaded and executed.

Notation	Description
M_l, M_b	Number of little and BIG CPU cores
N	Number of model layers
r_i, w_i, e_i	The <i>i</i> -th read/transform/execution operation $(1 \le i \le N)$
f(i, j, t)	Whether operation i executes on core j at time t
$S_{i,j}$	The timestamp when operation i starts running on core j
E_i	The timestamp when operation i finish running
T(f(i, j, t))	Latency of operation <i>i</i> runs
Θ_i	The set of precursor operations of operation i
η , F	The set of all operations and all inference operations

Table 3: Notations used in §3.3 and §3.4.

This method, however, could introduce additional disk storage and I/O. As shown in the column "Read Cache" column of Table 2, the post-transformation weights often occupy more storage because the weights will be duplicated. In other words, caching post-transformation weights trades off disk read with memory-access-intensive weights transformation for a given kernel. From the perspective of a whole model's cold inference that consists of many kernels, it opens rich trade-offs between the I/O and memory access.

3.2.3 Pipelined inference. Nowadays edge devices are typically equipped with multi-process/core architecture such as BIG.little CPU cores. To fully exploit those processors to boost cold inference, one might simply multithread the kernel preparation and execution, e.g., using many threads to read and transform the weights simultaneously. However, we observe the benefits from such multithreading are limited due to two reasons. First, weights reading and transformation stages are not bounded by the computation but disk I/O and memory I/O, respectively. Second, the asymmetric multiprocessor on edge devices makes it difficult to partition the DL workloads to fully utilize each processor's capacity [55], therefore a straggler processor could significantly slow down the whole inference regarding the data flow dependency.

Instead of simply multithreading the kernels separately, we propose to pipeline them: overlap different kernels' weights reading, transformation, and execution. This is based on a key opportunity that DNNs typically have a layer-by-layer computation pattern. As such, the system does not need to wait for the whole model to be loaded or all weights to be transformed to begin the kernel execution. Instead, the loading, transformation, and execution of different layers can be possibly pipelined. The concept of the layer in DNNs also provides an easy-to-use basis to schedule the I/O, memory-intensive, and computation-intensive stages in devices.

3.3 Problem Formulation

The need for a kernel scheduler To fully harness the optimization knobs introduced in §3.2, we need a global kernel scheduler to determine (i) which kernel to use for each operator; (ii) whether to load the raw weights or the cached

post-transformed weights for each kernel; (iii) when and where to execute each operation. In this work, we use the term operation to indicate each stage of a kernel, e.g., its weights reading, transformation, and execution are three different operations. Apparently, those knobs need to be jointly considered as they inherently are coupled with each other. For instance, choosing a different kernel could overturn an optimal pipeline strategy.

Formulation of the kernel scheduling problem For simplicity, we first use BIG.little CPU architecture as the target scheduling platform to introduce our formulation and scheduling scheme. They can be easily extended to other heterogeneous processors, e.g., CPU + GPU as will be discussed later. The annotations used are summarized in Tabel 3. We use f(i, j, t) = 1 to indicate operation i executes on core j at time t (otherwise 0). Based on that, $S_{i,j}$ and E_i can be expressed by f(i, j, t) in Equation (1). Here, η_i means the set of cores where operation i runs on.

$$\eta_{i} = \{j | \sum_{t} f(i, j, t) \ge 1\}
S_{i,j} = \arg\min_{t} \{f(i, j, t) = 1\}, \quad j \in \eta_{i}
E_{i} = \max\{S_{i,j} + T(f(i, j, t))\}, \quad j \in \eta_{i}$$
(1)

Minimizing the cold-inference latency equals to minimizing the finishing time of the last execution operation f_N :

$$\min E_{e_{N}}$$

$$s.t. \begin{cases} S_{i,j} \geq E_{\alpha}, & \alpha \in \Theta_{i}, \forall i, \forall j \\ \sum\limits_{i \in \eta} f(i, j, t) \leq 1, & \forall t, \forall j \\ \sum\limits_{i \in \eta} \sum\limits_{j=0}^{M_{l} + M_{b}} f(i, j, t) \leq M_{l} + M_{b}, & \forall t \end{cases}$$

$$(2)$$

The solver is restricted by three conditions: (1) For each operation, its starting time is no earlier than the end time of its all precursor operations. We can build a dependency graph among the total $3 \times N$ operations in a DNN by integrating the original dependency of the model (among execution operations) and the read-transform-execution flow of every single kernel. (2) For each core, only one operation can run at a given timestamp; (3) At any time, the total number of cores being used should be no larger than $M_l + M_h$. Challenges Solving the above challenges faces the following primary challenges. First, according to Equation (1), $S_{i,i}$ and E_i are nonlinear functions of the optimization variables f(i, j, t). There it is Nonlinear Integer Programming, a classical NP-hard problem. Second, we observe that the execution time T(f(i, j, t)) can be interfered with by each other even though they run on different cores. This is mainly because the co-running operations reach the limit of disk and/or memory I/O speed. In summary, it's not likely to obtain an optimal kernel scheduling plan directly.

3.4 A Heuristic-Based Kernel Scheduler

```
Algorithm 1: Our kernel scheduler
   input
               : Number of little cores, M_I;
                 Number of layers, N;
                 Sets of candidate kernels' combination, K;
                operations r_i, w_i, e_i \ (i \in \{1, 2, ..., N\}).
   output : Combination of selected kernels, K_c;
                The list of operations running on little core j,
                 Q_j (j \in \{1, 2, ..., M_l\});
                 The list of operations running on BIG cores, Q_0.
Filter out the kernel candidates that exhibit no faster operation;
2 foreach combination k = \{ \langle r_i, w_i, e_i \rangle | i = 1, 2, ...N \} (k \in K)
      do
         Initialize Q_0: Insert the operations r_1, w_1 and all e_i of k into
3
           the BIG cores sequentially, s=2;
          Initialize the execution time of the operations on core j:
           T_{Q_i} = 0, j \in \{0, 1, ..., M_l\};
          Update the execution time of operation o on little cores t_o^1
5
           and BIG cores t_a^b:
         while \left| \max_{1 \le j \le M_l} T_{Q_j} - T_{Q_0} \right| > \varepsilon \text{ or } T_{Q_j} = 0, \ (j \in \{0, 1, ..., M_l\})
               if \max_{1 \le j \le M_l} T_{Q_j} > T_{Q_0} then
 8
                          if (t_{r_i}^b + t_{w_i}^b) + (t_{r_i}^l + t_{w_i}^l) < \max_{1 \le j \le M_l} T_{Q_j} - T_{Q_0}
 9
                                 Insert r_i, w_i into Q_0 header, s := i;
10
                                 break;
11
                Initialize Q_j\ (j=1,..,M_l): schedule r_i,\ w_i
12
                 (i = s + 1, ..., N) to different little cores sequentially;
               while \max_{1 \leq j \leq M_l} T_{Q_j} - \min_{1 \leq j \leq M_l} T_{Q_j} > \varepsilon do
13
                      j_{\max} := \arg\max_{1 \le j \le M_l} T_{Q_j}
                     j_{\min} := \arg \min_{1 \le j \le M_l} T_{Q_j}
15
                      Sort operations in Q_{imax} descendingly according
                       to the execution time as Q_{sort};
                      \textbf{for each} \ operation \ (r,w) \ in \ Q_{sort} \ \textbf{do}
17
                           if t_r^l + t_w^l < \frac{T_{Qj_{\text{max}}} - T_{Qj_{\text{min}}}}{2} then
18
                            Move (r, w) from Q_{i_{max}} to Q_{i_{min}};
19
                      Compute T_{Q_i} (j = 0, 1, ..., M_l);
20
          Compute the completion time of kernel combination k, T_{cold}^{k};
21
22 K_c = \arg\min_{l} (T_{cold}^k)
```

Heuristics We design our kernel scheduling algorithm based on the following heuristics. First, for almost every DNN we have tested, the kernel execution is still the most time-consuming type of operation. The lower bound we can possibly achieve for cold inference latency is equal to the warm inference, which usually places all the execution operations on BIG cores with multithreading acceleration. Second, there exists operation-to-hardware affinity. As shown in Figure 5, the BIG core on Meizu 16T can reduce the execution time by 6× compared to the little core, but can only reduce the

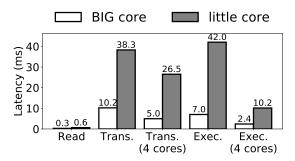


Figure 5: The consumed time of different stages of cold start on different ARM core types and numbers.

weights reading and transformation by 2× and 3.8×, respectively. This is because weights reading and transformation are more likely to be bottlenecked by disk I/O and memory I/O instead of computing. Third, multithreading is more efficient for execution operation than other operations. Conceptually, every single operation can be multithreaded on multiple cores for acceleration. However, according to our experiments (Figure 5), the speedup of multithreading on kernel execution can almost linearly scale with the number of cores (only BIG or little ones), yet multithreading exhibits poor performance on weights reading and transformation. This is because multithreading is more friendly to computation-intensive operations as it incurs inter-cores synchronization overhead.

Assumptions Based on the above heuristics, we build our algorithm atop the following key assumptions.

- Each kernel's execution operation always occupies all BIG cores and is executed sequentially. This is critical to push the performance of cold inference to the limit of warm inference.
- Weights reading and transformation operations of the same operator are always bundled together (as a new preparation operation) and mostly placed on little cores without multithreading. As such, we can use many little cores to run those operations separately at the same time. This is based on an important observation that those two operations have very few precursor operations (0 or 1) as compared to execution operation (at least 2), therefore can be easily pipelined.

Based on the above assumptions, we design an algorithm to determine: 1) which kernel to choose for each operator, and 2) how to schedule the operations of the kernels among the little cores and BIG cores. While it is still NP-hard (alike the Knapsack problem [25]), the observations guide us to a low-complexity algorithm as will be discussed below.

Algorithm of kernel scheduling. Our proposed algorithm (Algorithm 1) is composed of two layers. In the outer layer (line 2), we traverse to find the optimal kernel combination. A kernel combination refers to, for each operator, what kernel to use and whether to bypass the weights transformation.

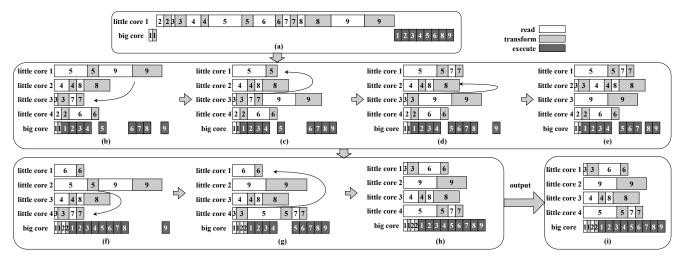


Figure 6: An illustrative example of how NNV12's kernel scheduling algorithm works (Algorithm 1).

There are $\prod_{i=1}^{N} (2 \cdot c_i)$ such combinations, where c_i is the number of kernel candidates of i^{th} operator. Apparently, we do not need to iterate over all of them; instead, for each operator, we filter out the kernel candidates that exhibit no faster operation in either preparation or execution than any other candidate. After that, there are only 1–2 candidate kernels left for each operator as observed.

In the inner layer, the kernel combination is given and we need to properly schedule the operations of the kernels among the BIG cores and little cores, with the objective of minimizing the completion time of the last kernel. As each kernel's execution operation always occupies all BIG cores and the execution operation should be executed after the weights reading and transformation operation from the same kernel, the scheduling can be divided into two categories: on BIG cores (can be considered as a whole) and on little cores. We just need to: (1) balance the loads among the little cores to minimize the largest completion time of the little cores; (2) balance the workloads between the little cores and large cores to minimize the completion time of BIG cores. To this end, our proposed algorithm undergoes two loops: the BIG-core loop and little-core loop.

In the BIG-core loop (line 6-11), we determine which operations should be executed on BIG cores. It is straightforward that all the operations of the first kernel (to fast boot) and all the execution operations of the rest kernels should run on BIG cores (line 3). If the completion time of BIG cores (T_{Q_0}) is still less than the largest completion time of the little cores after moving one reading and transformation operation from little cores to BIG cores (line 9), the weights reading and transformation operation should be inserted to the BIG cores (line 10); Otherwise, the weights reading and transformation operation remains running on little cores. In the little-core loop (line 13-20), the reading and transformation operations are scheduled among the little

cores to balance the workloads. We initialize the operation lists of little cores (line 12) by sequentially scheduling the reading and transformation operations one by one to different little cores (as shown in Figure 6(b)). If the little core with the earliest completion time has the potential to accommodate the reading and transformation operations from the little core with the largest completion time (line 18), migrate the reading and transformation operations to balance the workloads (line 19). Through the above loops, the workloads can be balanced to large extent among all the cores.

An illustrative example is shown in Figure 6. Figure 6(a) corresponds to Line 3 in Algorithm (1), where we set the reading and transformation operations of layer 1 and all execution operations on BIG cores, while the other operations are placed on little core. Figure 6(b)–(e) and Figure 6(f)–(h) are two iterations of the BIG-core loop in Algorithm (1). Figure 6(b)–(e) are four iterations of the little-core loop.

3.5 Extending to GPU

In the previous sections, we mainly introduce how NNV12 fits BIG.little CPU architecture. Conceptually, the above design can be easily extended into GPU platform by treating the GPU as the BIG core and CPU as little cores. Yet, the unique characteristics of GPUs require NNV12 to make further revisions and optimizations to achieve optimal performance.

Creating pipeline as another operation For each operator, in addition to the weights reading, transformation, and kernel execution on CPU, there is another operation in the cold inference namely *creating pipeline* [13]. Taking Vulkan as an instance, this step sets up a pipeline that describes the configurable state of the graphics card, like the viewport size and depth buffer operation. It is usually implemented with ahead-of-time compilation [14], therefore incurs no overhead for warm inference. In cold inference, however, this

operation can take a considerable amount of time to run as previously shown in Table 1.

Operations-to-processor placement The GPU is only in charge of kernel execution while all other operations are scheduled on CPUs as the latter can hardly be accelerated by GPU. It also helps reduce the CPU-GPU data copy. Further partitioning the execution across CPU and GPU [37] might enlarge the optimization spaces but is orthogonal to this work and left to be explored in the future.

Caching compute shaders One time-consuming and GPU-specific process we observed is shaders compiling [7]. In Neural Networks, a kernel is implemented as a shader [16]. For example, 3D graphics and compute API Vulkan drivers are supposed to ingest shaders already translated into an intermediate binary format called SPIR-V (Standard Portable Intermediate Representation). For a given DNN model, the shaders that need to be compiled and generated at each layer are determined. Therefore, we can cache those shaders on disk and load them directly to speed up the cold inference just as how we bypass the weights transformation stage.

3.6 Extending to Continuous Inference

The kernels selected by NNV12 are optimized for cold inference. As discussed in §3.2, the kernels with the fastest warm inference might be different from what NNV12 selects. We use K_{cold} and K_{warm} to represent two different sets of kernels. If NNV12 keeps using the kernels of K_{cold} in subsequent inferences, it leads to a suboptimal warm inference latency.

To handle such side effects, NNV12 provides an additional mode besides the one only optimized for cold inference as discussed above. This mode indicates that there will be continuous inferences tasks. In that case, NNV12 still follows the aforementioned techniques to optimize the cold inference, but makes the following key differences: (1) It also prepares the kernels in K_{cold} – K_{warm} and switches to kernels in K_{warm} for later inferences. (2) The preparation of those additional kernels is performed on little cores when idle during the cold inference. This design is motivated by our observation that, in most scenarios, the little cores have some idle time before the kernel execution finishes on BIG cores. If such idle time is not enough to prepare the kernels in $K_{cold} - K_{warm}$, the rest of the operations will be pipelined in the second inference as NNV12 does for the cold inference. In §4.6 we experimentally show that NNV12 achieves (near-)optimal performance in continuous inference as well.

4 EVALUATION

4.1 Methodology

NNV12 prototype We've implemented a prototype of NNV12 with 18K C++ LoC atop ncnn (version 20211208) for its lightweight codebase and superior performance as compared to

TFLite. We used Vulkan GPU backend for its more generic support for different platforms. Note that the techniques of NNV12 are compatible with other DL libraries as well.

Models We use 12 popular NN models as summarized in Table 4 to test the performance of NNV12. Those models span across different tasks (image classification and object detection) and computation complexity. We mainly use CNN models in our experiments because a recent empirical study shows that CNNs are dominant use cases in nowaday edge devices [15]. The models mainly come from the official model zoo of those libraries [11], while for the ones that do not exist in the zoo, we generate them by ourselves, e.g., implementing the model structure in TF APIs and then converting it to TFLite format. We manually check that the same model used by each library has a consistent structure.

Hardware and OS As shown in Table 5, we perform experiments on 4 different edge devices: Meizu 16T smartphone with Snapdragon 855 SoC, Google Pixel 5 with Snapdragon 765G SoC, Jetson TX2, and Jetson Nano. The OS of Meizu 16T and Google Pixel 5 is Android 11. The OS of Jetson TX2 and Jetson Nano is Ubuntu 18.04. During cold inference experiments, We use only CPUs for the two smartphones and use GPUs on the Jetson boards. The reason is that, on smartphone SoCs, the CPUs perform much better than GPUs for cold inference as GPU preparation takes much more time than CPU as discussed in Table 1. Therefore, it's straightforward to use CPU for cold inference tasks on smartphones, making it meaningless to report their GPU performance. Yet, on Jetson TX2/Nano with much more powerful GPUs, the DNNs are almost always placed on GPUs rather than CPUs. **Baselines** On Meizu 16T and Pixel 5, we compare the performance of NNV12 to 3 baselines: ncnn, TFLite, and AsyMo [55]. Since NNV12 is implemented atop ncnn, the comparison between them can directly reveal the effectiveness of NNV12's key techniques. Still, TFLite is added as it is the most popular DL library used in end devices (version 2.5.0). AsyMo is the state-of-the-art DL engine that can fully exploit the asymmetric CPU architecture on smartphones. Since AsyMo is not open-sourced yet, we re-implement it atop ncnn for a fair comparison. On Jetson TX2/Nano, we also use ncnn with its Vulkan backend. However, since TFLite does not support either Vulkan or CUDA backend, we replace it with TensorFlow (version 2.5.0) for comparison.

Setups and configurations On Meizu 16T and Pixel 5, we exhaustively try different core numbers for TFLite and ncnn and use the core number that achieves the optimal performance by default. In practice, it turns out to be 4 cores on Meizu 16T and 2 cores on Pixel 5. Note that AsyMo always uses all the CPU cores available. The model files are stored on SDCards for both smartphones and Jetson boards. To eliminate the impacts of file cache, we clear the system cache

Model Tas		Parameters	Model Size FLOPs	Storage	Scheduling Plan Generation Time (Offline)			e (Offline)	
Wiodei	lask	1 at afficiers	Widdel Size TLOI's	Overhead	Meizu 16T	Pixel 5	TX2	Nano	
AlexNet [36]	С	61.3M	237.5M	1.4G	172.3M	1,538.4ms	4,157.4ms	8,197.3ms	22,962.6ms
GooLeNet [52]	С	7.1M	26.9M	3.2G	22.6M	1,301.9ms	2,304.3ms	6,457.6ms	9,648.7ms
MobileNet [30]	С	4.4M	16.2M	1.1G	12.6M	796.5ms	1,796.5ms	5,443.0ms	8,357.5ms
MobileNetV2 [51]	С	3.7M	13.3M	0.6G	10.3M	759.3ms	1,796.5ms	4,770.0ms	8,441.1ms
ResNet18 [29]	С	12.7M	45.5M	3.9G	34.3M	892.6ms	1,896.2ms	1,461.1ms	2,599.1ms
ShuffleNet [65]	С	3.6M	12.9M	1.9G	10.0M	577.8ms	1,005.9ms	5,872.3ms	7,996.8ms
EfficientNetB0 [53]	С	5.4M	19.6M	0.8G	15.2M	1,129.9ms	2,446.0ms	6,481.2ms	6,031.4ms
ResNet50 [29]	С	25.7M	97.4M	7.8G	89.7M	1,652.2ms	2,974.3ms	3,757.6ms	3,854.0ms
SqueezeNet [32]	С	1.4M	4.7M	1.7G	3.8M	717.9ms	1,788.8ms	5,849.8ms	6,738.9ms
ShuffleNetV2 [44]	С	3.4M	12.0M	0.5G	10.9M	532.1ms	920.7ms	4,724.5ms	5,665.3ms
MobileNetv2-YOLOv3 [50]	OD	3.6M	13.1M	1.0G	12.5M	849.2ms	2,544.5ms	3,394.3ms	4,979.7ms
MobileNet-YOLO [49]	OD	11.9M	49.1M	2.9G	38.3M	984.2ms	2,485.5ms	5,047.5ms	7,710.2ms

Table 4: The NN models used in experiments. Input size: 224x224. "C": classification; "OD": Object Detection.

Devices	CPU	\mathbf{GPU}
Meizu 16T [5]	2.8GHz Cortex-A76	
Snapdragon	3×2.4GHz Cortex-A76	Adreno 640
855 [9]	4×1.8GHz Cortex-A55	
Pixel 5 [6]	2.4GHz Cortex-A76	
Snapdragon	2.2GHz Cortex-A76	Adreno 620
765G [8]	4×1.8GHz Cortex-A55	
Jetson TX2 [4]	2×4×2.0GHz Cortex-A57	256-core Pascal
Jetson Nano [3]	4×1.43GHz Cortex-A57	128-core Maxwell

Table 5: Experimental platform specifications.

HW Platform	Speedup over baselines (min - max, avg)		
11 W 1 latioili	ncnn	TFLite (TF)	
Meizu 16T (CPU)	3.2× - 10.3× (5.1×)	4.8× - 15.2× (9.5×)	
Pixel 5 (CPU)	$2.4 \times - 7.6 \times (3.8 \times)$	2.1× - 5.2× (2.1×)	
Jetson TX2 (GPU)	9.0× - 38.9× (29.6×)	14.6× - 355.3× (154.8×)	
Jetson Nano (GPU)	4.0× - 58.2× (28.5×)	10.4× - 401.5× (234.3×)	

Table 6: Summarized performance comparision of NNV12 over baselines on different platforms.

before each cold inference. For all experiments, the cold inference latency does not include the loading and initialization time of the libraries. Each experiment is repeated by 100 times and the average numbers are reported.

4.2 End-to-End Performance

Cold inference latency on CPU Figure 7 compares the cold inference latency of NNV12 with the baselines on edge CPUs and Table 6 summarizes NNV12's overall improvements. It shows that NNV12 significantly outperforms the baselines on all models and platforms, i.e., $2.1 \times -15.2 \times$ speedup over TFLite and $2.4 \times -10.3 \times$ speedup over ncnn.

NNV12 also achieves close performance to warm inference, i.e., only $1.72\times$ slower at average. On ShuffleNetV2, the gap is even negligible (≤ 1 ms). This is because NNV12 effectively overlaps the preparation stages (loading and transformation) with the execution, therefore their latency can be mostly hidden. Yet, the gap still exists for three reasons. First, the model

execution could be waiting for the preparation to be done on CPU little cores when the overlapping is not perfectly planned. Second, even without waiting, the execution could be slowed down due to the cross-operation interference as mentioned in §3.4. Third, NNV12 selects kernel for fast cold inference, whose real execution speed might be slower than the original selection that optimizes for the warm inference.

The more competitive baseline AsyMo achieves relatively limited improvements over the vanilla DNN engine ncnn, i.e., only 1.03×-1.28× speedup. This is because it only improves the execution speed by fully utilizing the asymmetric CPU cores through kernel scheduling, but the weights preparation still takes a considerable amount of time in cold inference.

Impacts of CPU core numbers In the above experiments, we always set the CPU core number to the one obtaining the best performance for TFLite and ncnn. In practice, it turns out to be 4 on Meizu 16T and 2 on Pixel 5. Figure 8 further shows a comprehensive comparison by using different core numbers on Meizu 16T. It confirms our observation that using 4 cores exhibits the best performance for TFLite and ncnn, which is also consistent with the prior study [55]. This is mainly because those DL engines cannot well exploit the asymmetric CPU cores for DL execution. Note that they also use multi-threads to accelerate the weights transformation yet the profit from more threads is also marginal. This is because the weights transformation is mainly memory-bounded. Instead, NNV12 pipelines different kinds of operations to fully exploit the disk, memory, and computing capacity.

Cold inference latency on GPU Figure 9 compares the cold inference latency of NNV12 with the baselines on edge GPUs and Table 6 summarizes NNV12's overall improvements. It shows that the performance improvement of NNV12 compared to the baselines is even more significant than CPU, i.e., $10.4\times-401.5\times$ speedup over TensorFlow and $4.0\times-58.2\times$ speedup over ncnn. There are two primary reasons for such

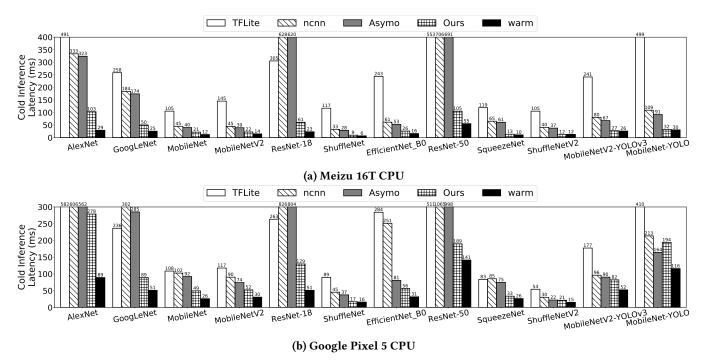


Figure 7: The cold inference latency of NNV12 and baselines on edge CPUs.

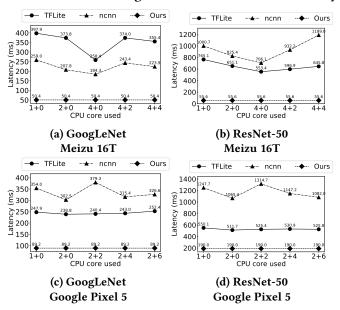


Figure 8: The cold inference latency of NNV12 and baselines running on different CPU core numbers. "X+Y" indicate X BIG cores and Y little cores.

a huge improvement. First, the cold inference on GPU requires more preparations such as creating pipeline. Therefore NNV12's key techniques, especially the kernel pipeline (§3.4), bring more benefits. Second, NNV12 incorporates additional optimizations for GPU like shader caching (§3.5).

Energy consumption We also evaluate the energy consumption of NNV12 and illustrate the results in Figure 10. We observe that NNV12 can significantly reduce the energy consumption, i.e., $0.2 \times -0.6 \times$ compared to ncnn. Such energy-saving mainly comes from the saved inference time through NNV12's key techniques, especially the kernel selection.

4.3 Ablation Study

We then evaluate the benefits brought by NNV12's each key technique separately. The results are illustrated in Figure 11. Our major observation is that each of NNV12's key techniques contributes noticeably to the cold inference speedup. For example, with ResNet-50 and Jetson TX2, the kernel selection first reduces the cold inference latency from 8,272ms to 2,300ms. Caching the post-transformed weights further reduces the latency to 555ms, and with pipelined execution the latency finally becomes 240ms.

4.4 Resource Overhead

There are two kinds of overhead NNV12 introduces: at offline, NNV12 needs to generate the optimal kernel scheduling plan according (§3.4); to boost the cold inference, NNV12 opportunistically stores the post-transformed weights on disk in addition to the raw weights (§3.2). (1) **Time to generate scheduling plan** As shown in Table 4, NNV12 takes only 532.1ms-4157.4ms on Meizu 16T and Pixel 5 CPU to generate the kernel scheduling plan. It takes more time on Jetson TX2 and Nano, i.e., 1461.1ms-22962.6ms, because of the more

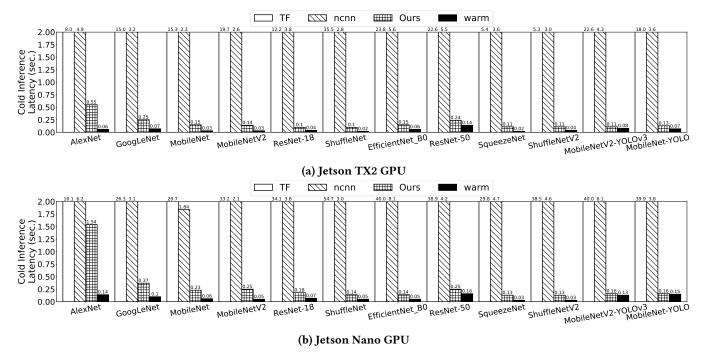


Figure 9: The cold inference latency of NNV12 and baselines on edge GPUs.

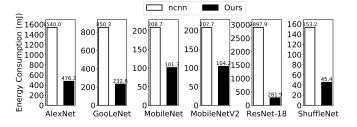


Figure 10: The energy consumption of cold inference.

complicated preparation stages of GPUs. Note that this overhead only occurs for one shot when a model is fetched to a device, and shall not compromise the user experience. (2) **Disk storage for post-transformed weights** As shown in Table 4, the storage overhead to cache the post-transformed weights is 7.1MB–164.8MB. Note that not every layer will apply the cache technique depending on the operator characteristics and kernel scheduling strategy. Since nowaday edge devices are typically equipped with a few to tens of GBs disk, such storage overhead is tolerable.

4.5 Case Study: Memory-Bounded Multitasking Inference

A killer use case of NNV12 is to quickly switch among multiple models when the memory is not enough to support multitasking inference. NNV12 addresses this issue by directly optimizing the cold inference as the memory only needs to be allocated for one shot. We compare NNV12 with two more

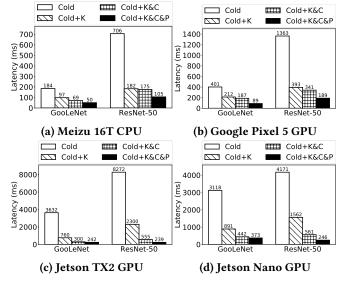


Figure 11: The ablation study results of NNV12. "K": kernel selection; "C": caching the post-transformed weights (and shaders); "P": kernel execution pipeline.

baselines: (1) Partial-warm: fixing as much portion of each DNNs as possible in memory and loading the rest in demand. It ensures the peak memory usage, i.e., the peak memory usage during one model inference plus the fixed portion of other models combined, is no more than the given memory bound. The more memory available, the less to be loaded on demand and therefore the faster cold inference can run.

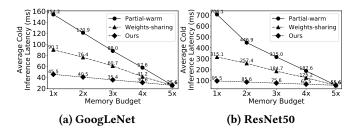


Figure 12: The average cold inference latency in memory-bounded DNN multitasking scenarios.

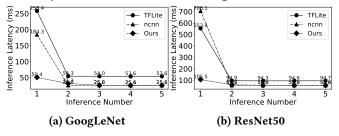


Figure 13: The cold inference and subsequent warm inference latency of NNV12 and baselines.

(2) Weights-sharing: inheriting the key idea from [41], this method assumes there is part of weights among the DNNs can be shared. Then it uses the method of Partial-warm approach to fix those weights in memory as much as possible. To enable weights sharing, this approach often requires to re-train the DNNs and incurs accuracy drop. To be fair in this experiment, NNV12 is also enhanced with the partial warmup idea so that the number of operations to be pipelined is reduced as some weights can be kept in memory persistently.

For this experiment, we assume there are 5 GoogLeNet or ResNet-50 models (with different weights) that will be randomly picked to execute. We set the proportion of shared weights for Weights-sharing method to be 50%, which is typically higher than in reality. We vary the memory bound from 1×-5× to the peak memory usage during the model inference. As shown in Figure 12, when the memory bound is just enough to support one inference (1×), the other two baselines are like the vanilla libraries, therefore, perform much worse than NNV12. With larger memory bound, each method improves as they can store some weights in memory persistently. Even though, NNV12 still consistently outperforms other baselines until the memory is large enough (5×) to keep all models in memory.

4.6 NNV12 in Continuous Inference

Recall that NNV12 incorporates a unique design (§3.6) to optimize for consecutive inferences as well. We experiment with GoogLeNet and ResNet-50 on Meizu 16T. The results are illustrated in Figure(13). It shows that NNV12 not only greatly optimizes the cold inference latency, but also achieves close

performance to ncnn in the second inference, i.e., only 8% slower, and the same speed since the 3rd inference. NNV12 runs slightly slower on the second inference than ncnn because the idle time of little cores during cold inference might not be enough to prepare all the kernels for the warm inference. In that case, NNV12 follows the pipeline design to speed up the second inference.

5 RELATED WORK

DNN weights sharing To reduce the memory footprint of multiple concurrent DNNs, prior works [27, 37, 40, 55, 56, 61, 64] have proposed to let the DNNs share certain layers of weights (especially the beginning ones). This approach has the scalability issue as with more DNNs the model accuracy can drop significantly. Or, they virtualize the DNN weights memory to better manage the data in/out switching among DRAM and disk [41]. This approach still incurs a high overhead in data swapping, thus does not address the slow cold start inference. Instead, this work directly optimizes the cold inference and does not compromise accuracy.

Apps pre-launch Mobile apps also face the cold launch problem. Prior works mainly use pre-launching [17, 48, 62] to mitigate the slow cold launch, i.e., by predicting when an app is going to be launched soon so the OS can prepare it. Intuitively, we can retrofit this idea to reduce the cold inference times of DNNs as well. Yet, it has the following drawbacks. First, there will be much more DNNs than apps on a device [15, 58], making an accurate prediction difficult. Second, unlike apps, DNNs are transparent to mobile OSes, thus there is no unified interface for OSes to bookkeep and operate on the DNNs hosted on a device.

DNN fast switch on clouds PipeSwitch [18] enables fast switch among training and inference tasks on the same cloud GPU. It inspired some of NNV12's design points, e.g., pipelined I/O and execution by exploiting the layer-by-layer structure of DNNs. However, PipeSwitch is not designed for cold inference optimization, as it does not consider the model loading and weights transformation stages. Therefore it's not directly comparable to NNV12.

DNN inference optimizations There are two main categories of on-device DNN inference optimizations. One is at system level, e.g., by exploiting heterogeneous processors [22, 28, 31, 37], cache [46, 61], or adaptive offloading [38, 59]. Such methods only work for warm inference. The other one is model level, e.g., quantization [35, 43] or sparsifiction [19, 47]. While those works mainly target warm inference, conceptually, they can also improve the cold inference as they reduce the execution time and/or the weights to be read from disk. NNV12 explores optimization knobs from different aspects and is orthogonal to them.

6 CONCLUSIONS

In this work, we propose NNV12, the first DL engine that optimizes the cold inference on edge devices. NNV12 fully exploits three optimizations knobs: kernel selection, weights transformation caching, and pipelined inference through a heuristic-based kernel scheduling scheme. Extensive experiments demonstrate the effectiveness of NNV12 to boost cold inference on edge CPU and GPU hardware.

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