A Hybrid Operating System Design Approach using Hardware Acceleration

Insop Song
Ericsson

Real Time Linux Workshop 2012
UNC Chapel Hill, NC

Hardware OS

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- more deterministic

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Why Hardware OS NOT seen much?

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Hybrid OS

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Process scheduling

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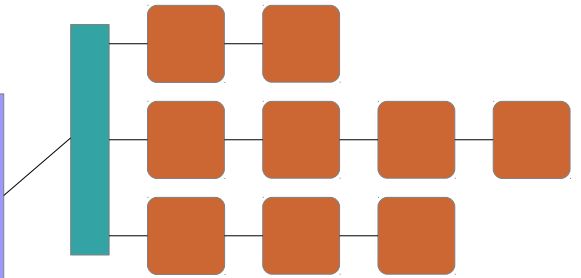

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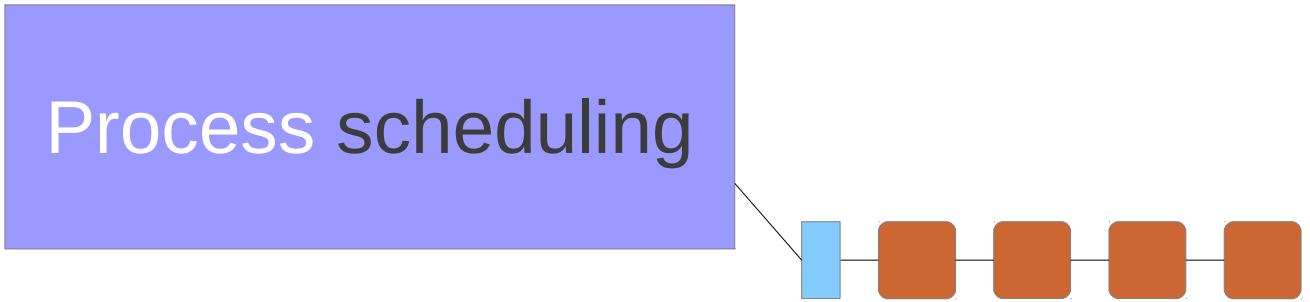

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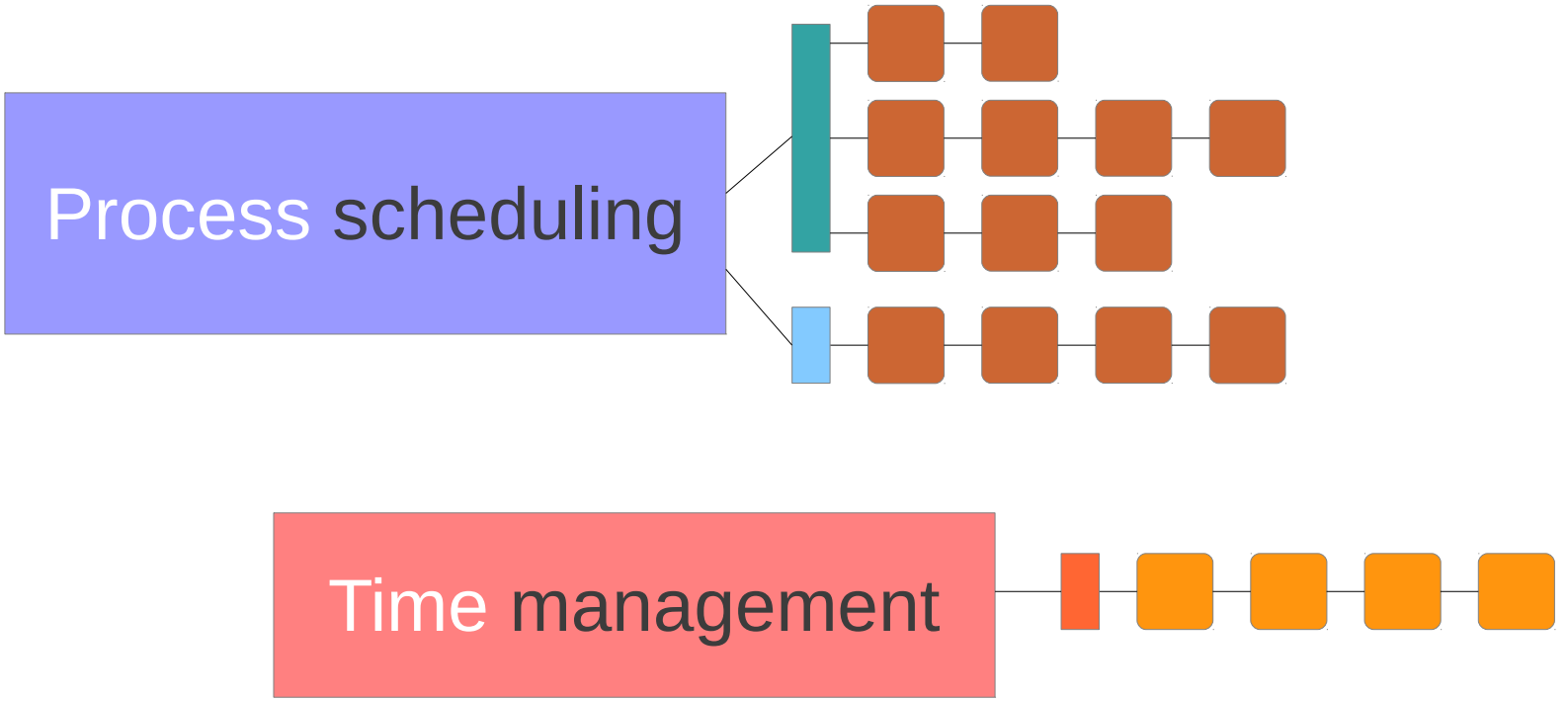

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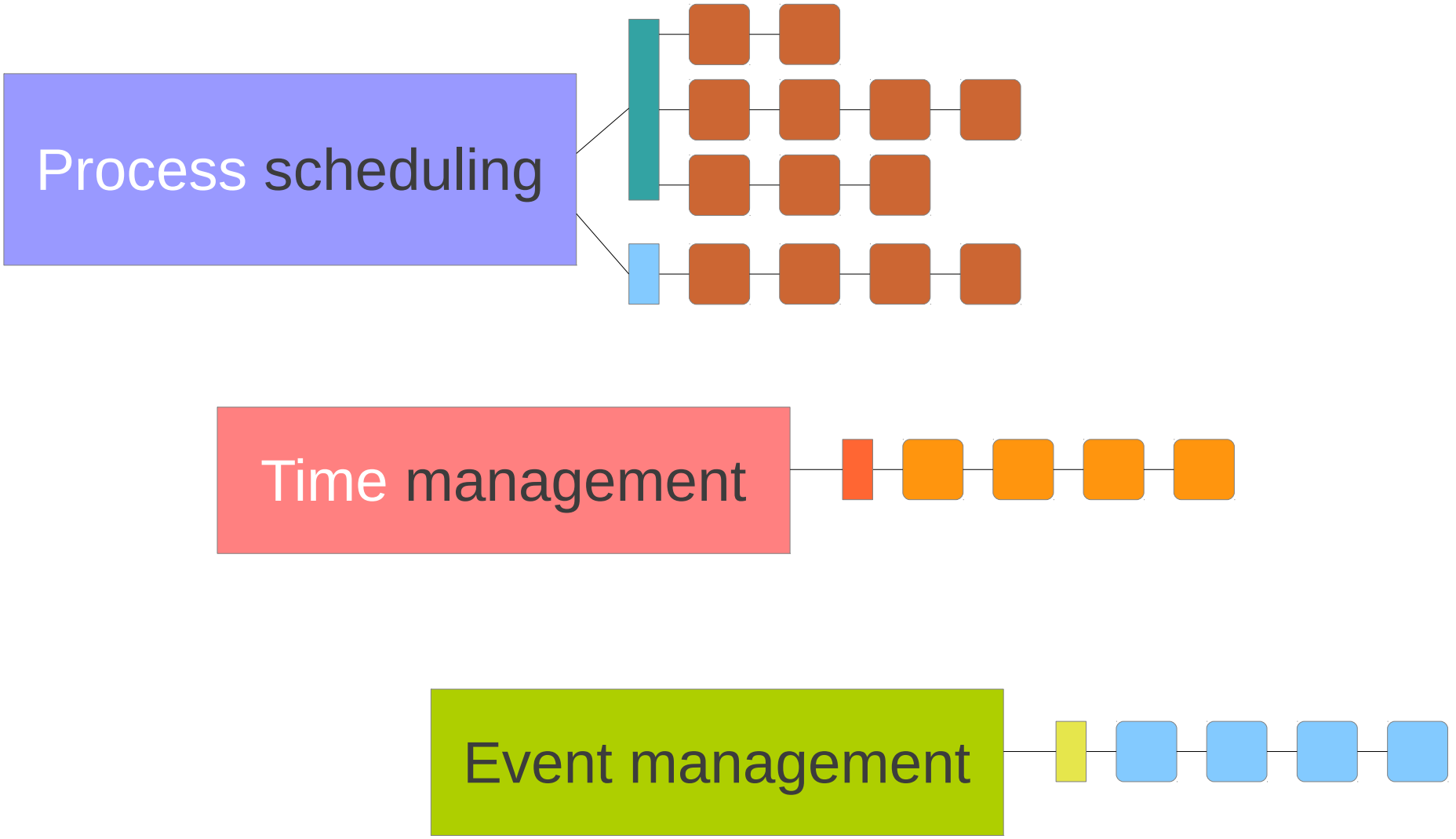

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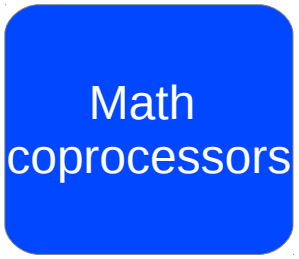

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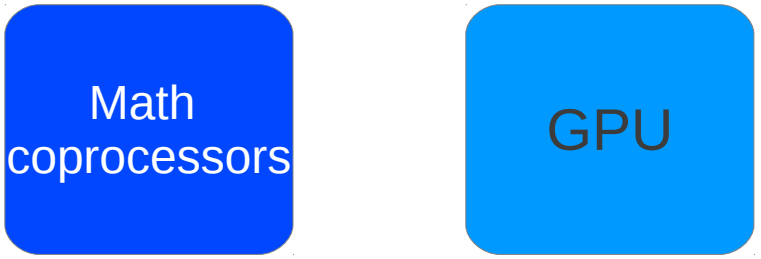

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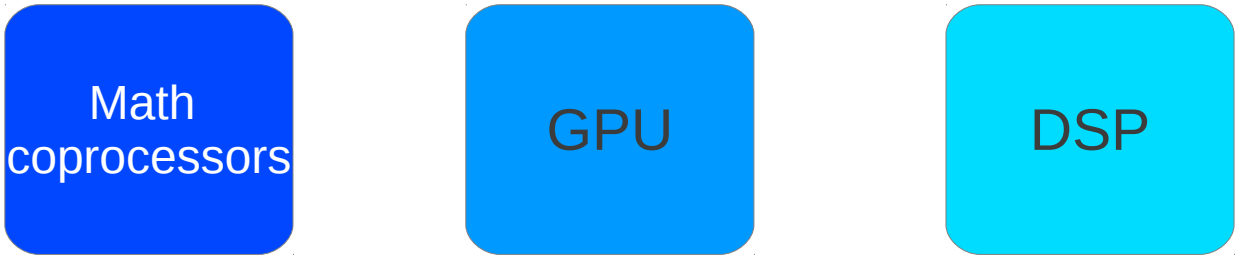

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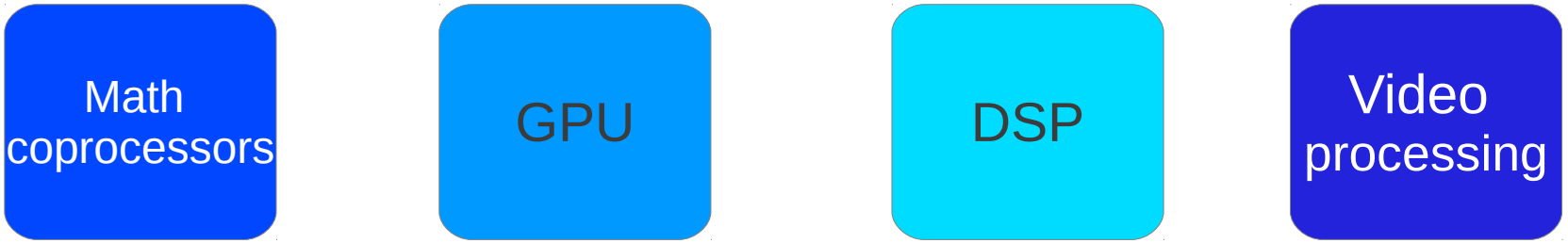

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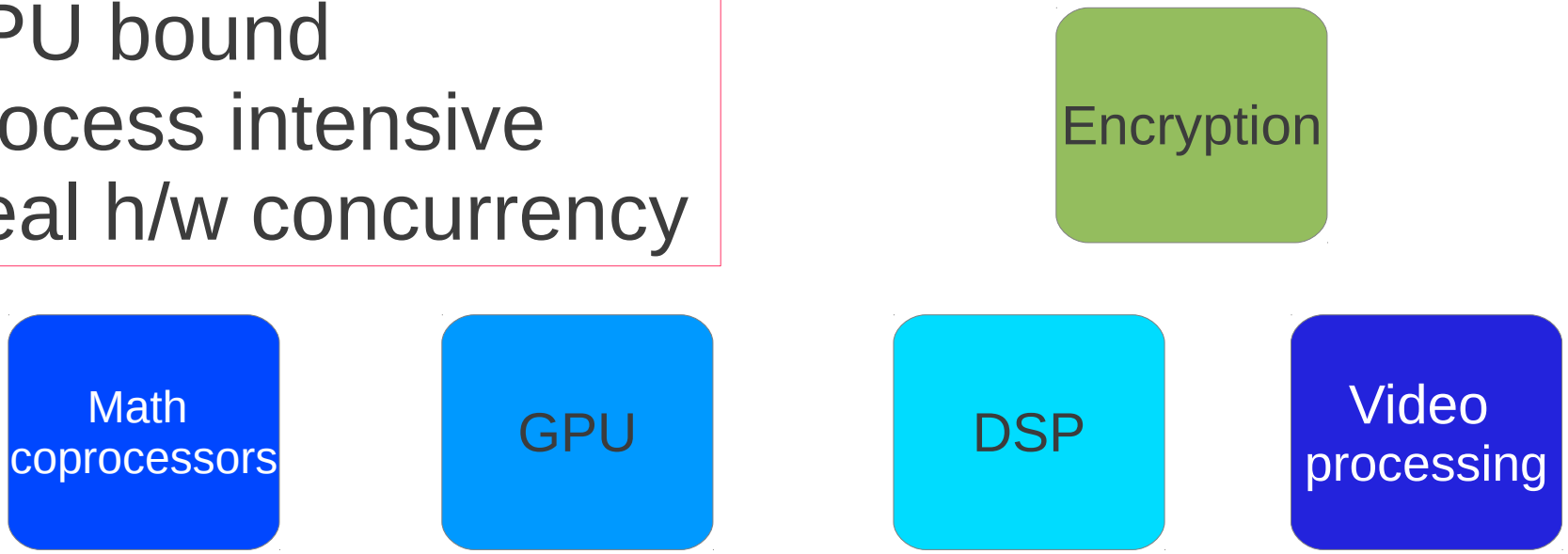

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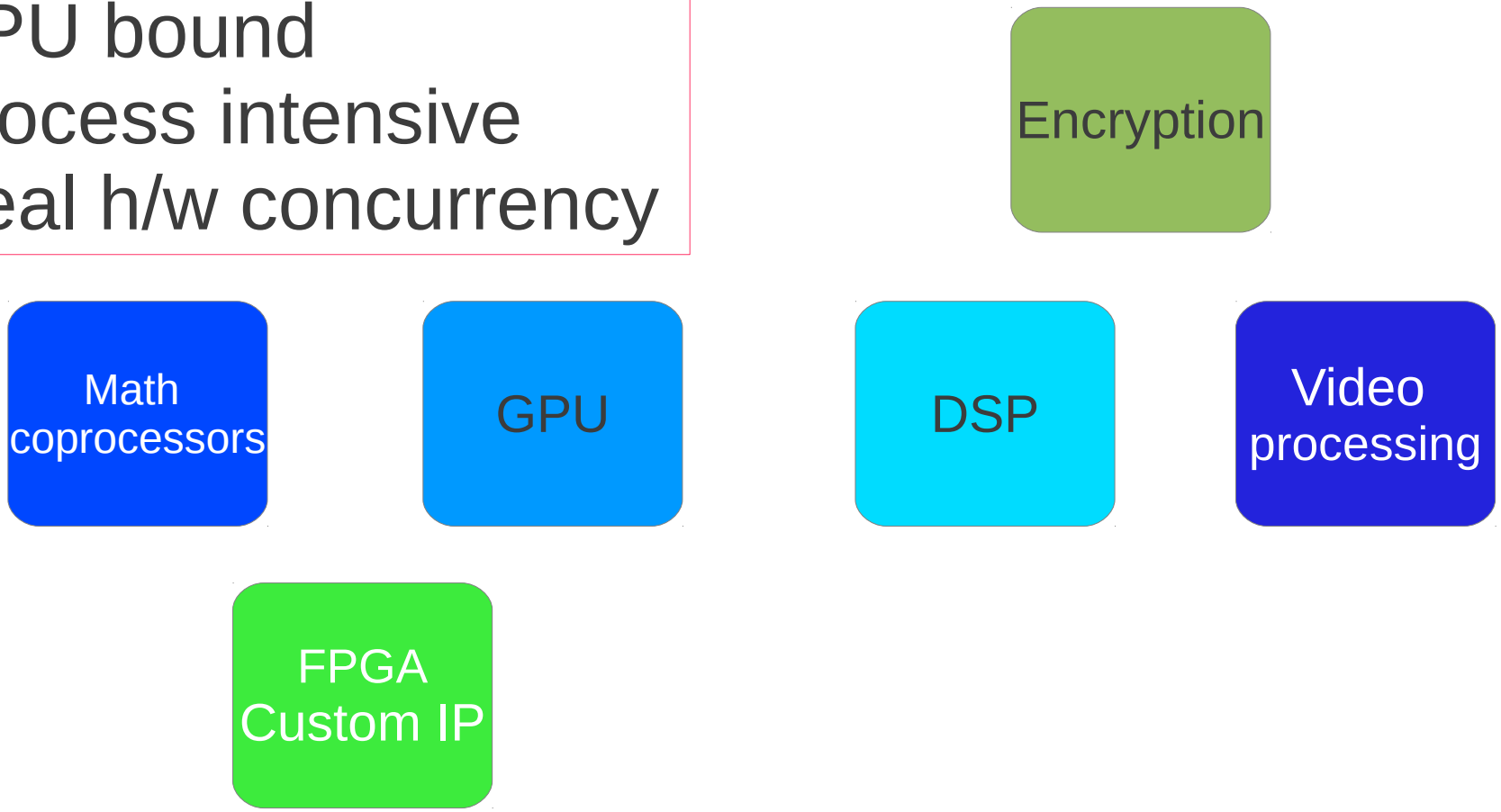

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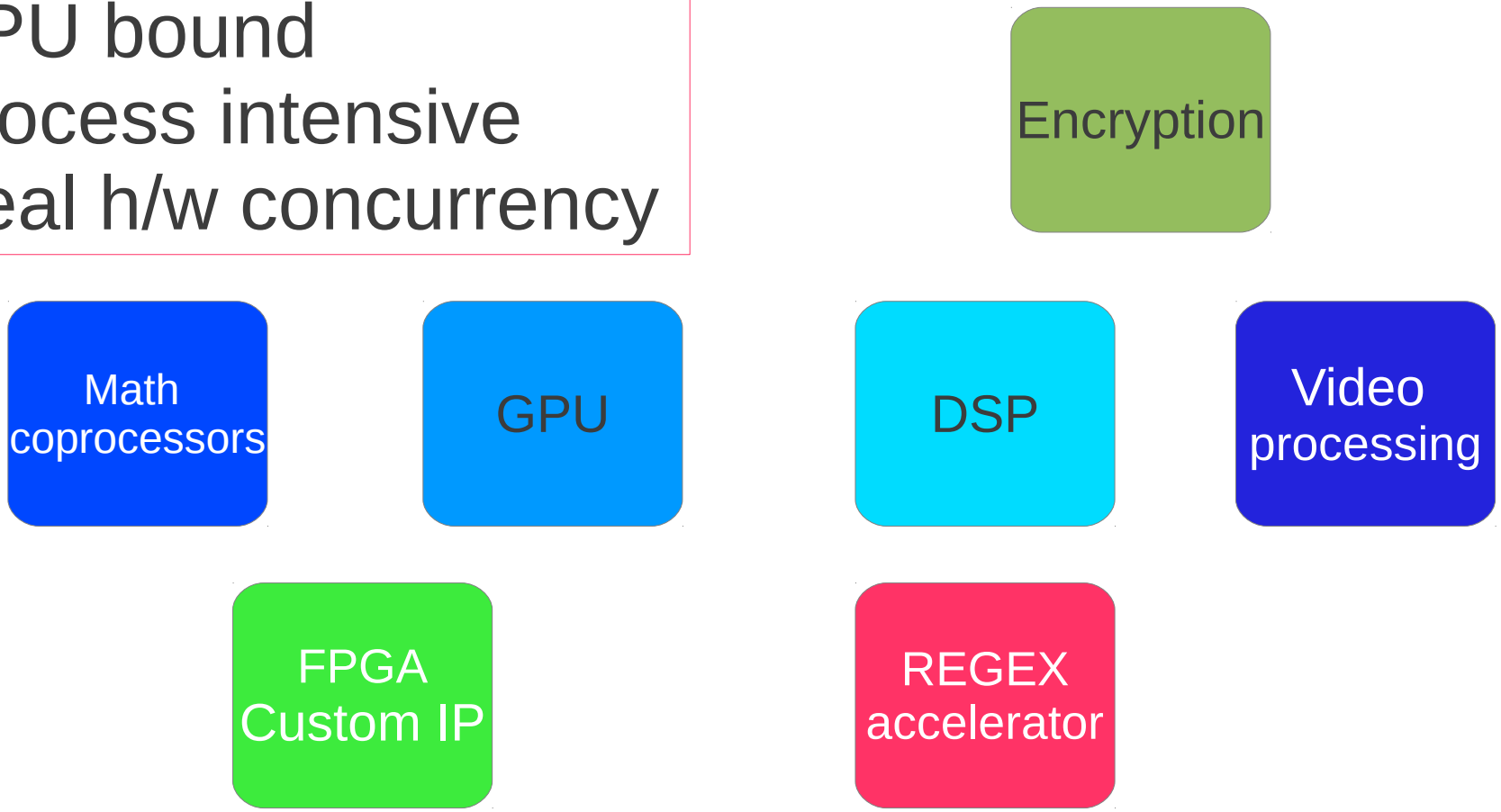

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  - papers can be found from 90s
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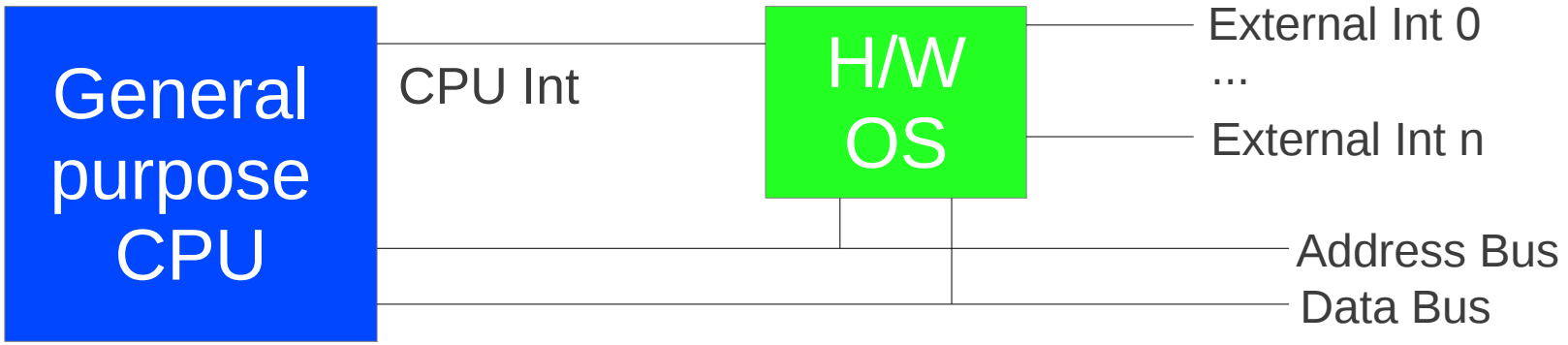

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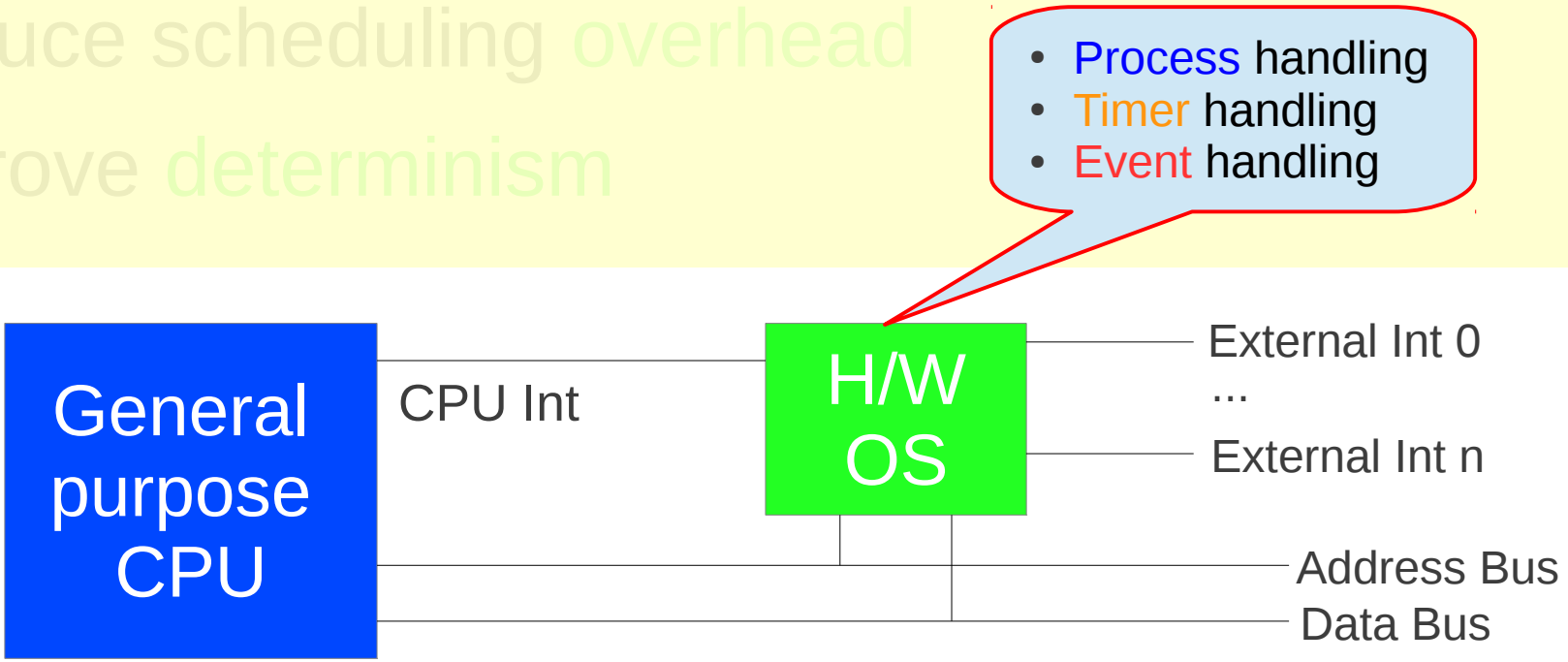
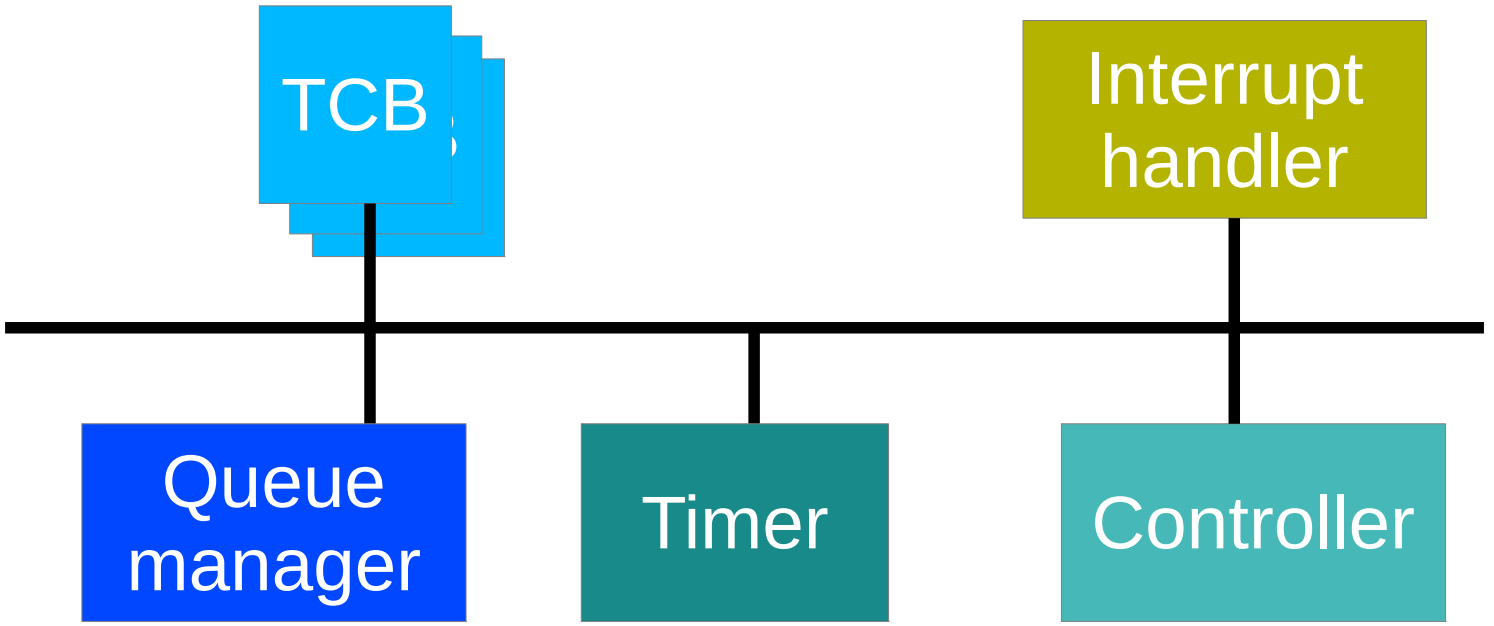


H/W blocks inside Hardware OS



Selected List of H/W OS

- Silicon TRON
- F-Timer
- Cooling's scheduler co-processor board
- FASTCHART/RTM (real time unit)
- A. Morton's scheduler coprocessor
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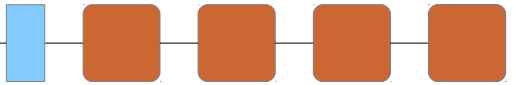
Great! H/W OS is available?

- Not quite
- Before we discuss why not
  - Let's talk briefly Linux and Open source software

- Why not h/w OS is available?
  - Need software OS change
  - OS scheduler is quite complex and changing

Linux scheduler and hrtimer

Process scheduling
CFS, SCHED_DEAD



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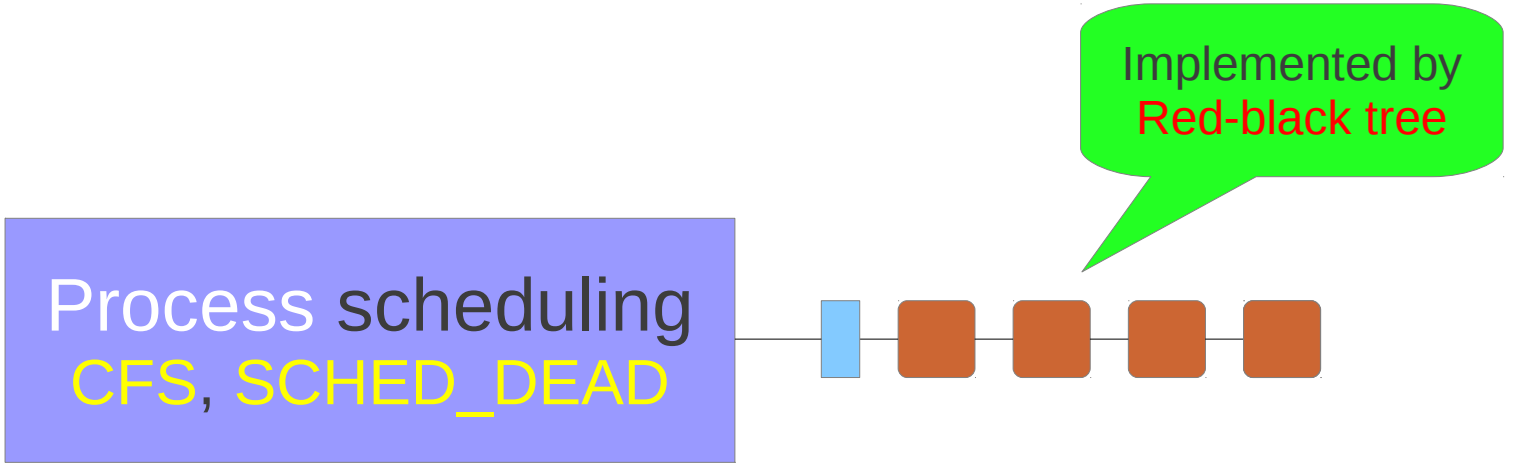

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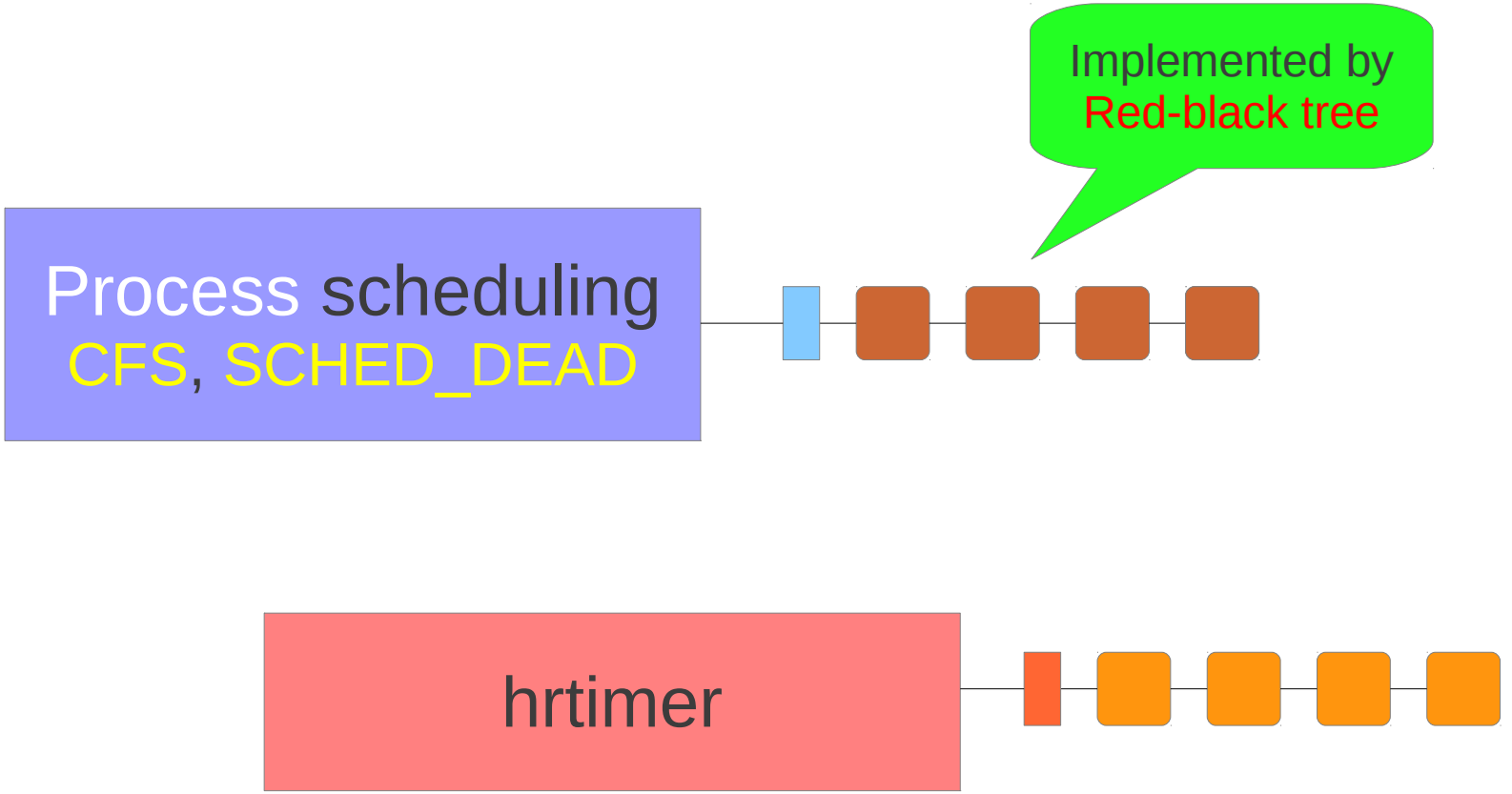

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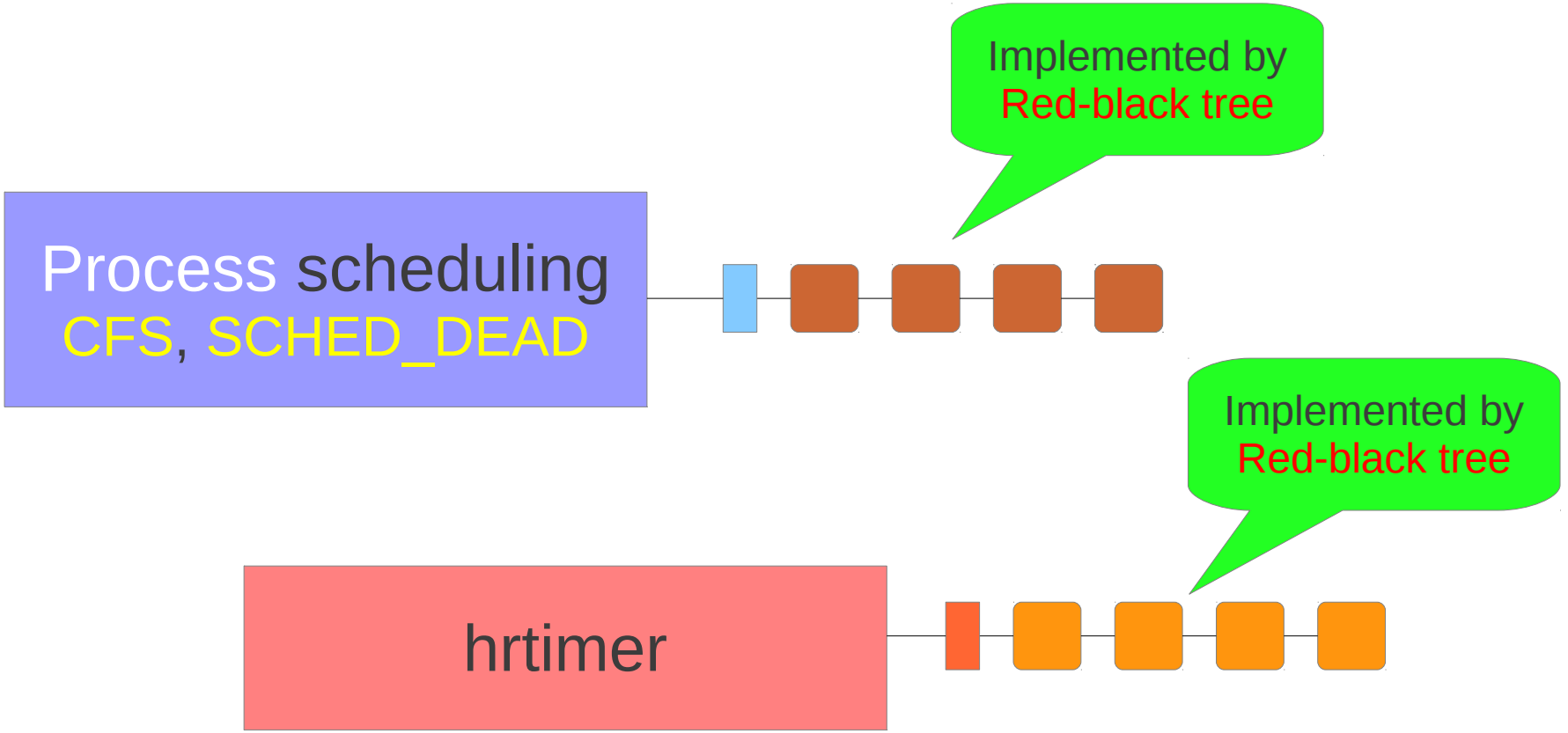

Hybrid approach

- Instead of trying to implement full/semi-full scheduler in h/w
  - Only implement a priority queue in h/w
  - Scheduler use h/w queue instead of RB-tree

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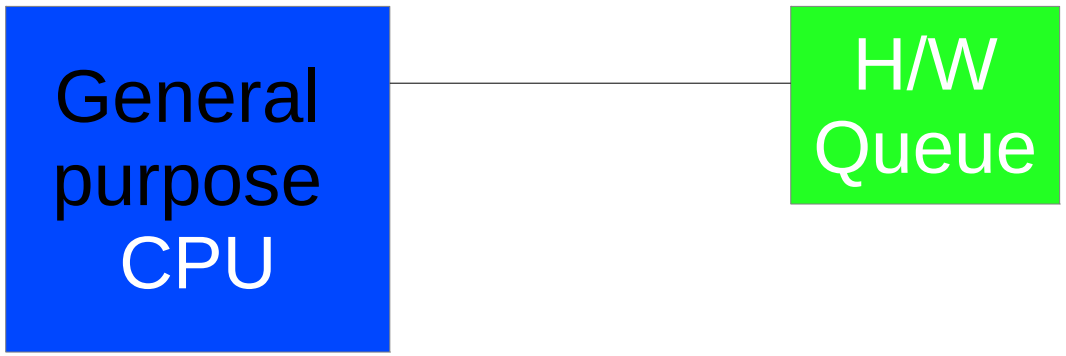

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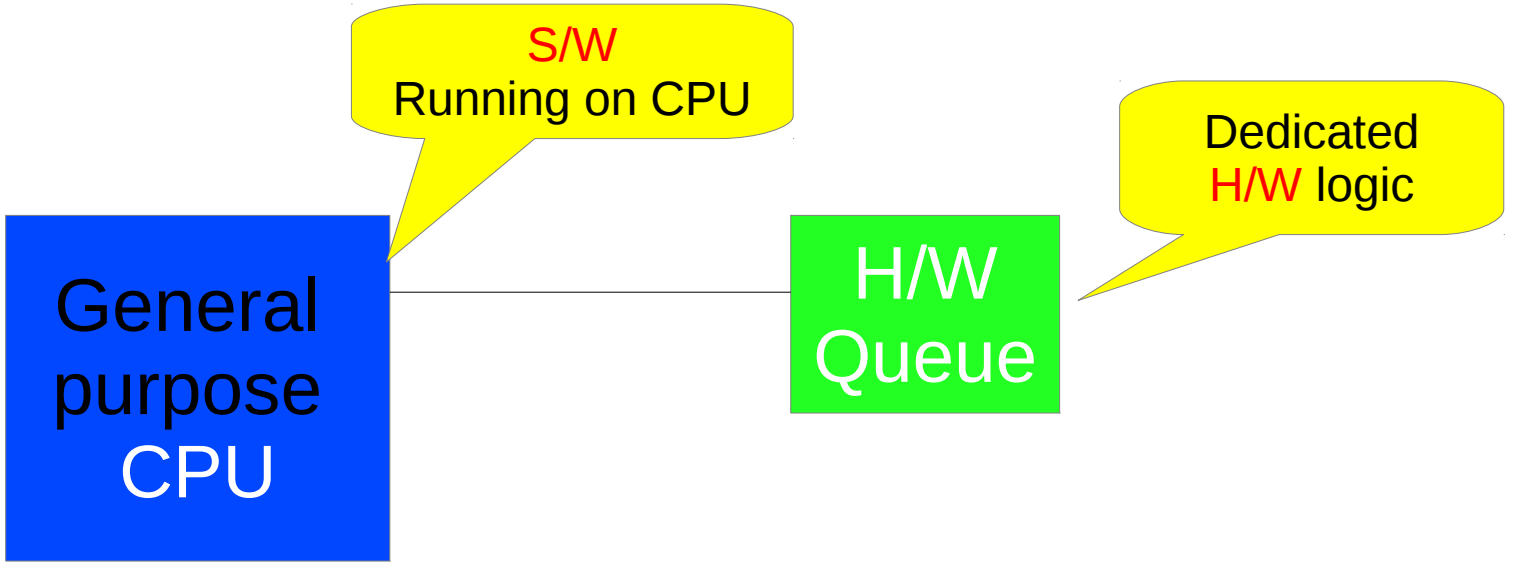

H/W Priority Queue

- Requirements:
  - Enqueue/dequeue in one cycle
  - Maintain FIFO order
- Example application of h/w priority queue
  - Network switch/router traffic management
    - for maintaining QoS during congestion

Types of h/w priority queues

- N: number entry
- P: number priorities

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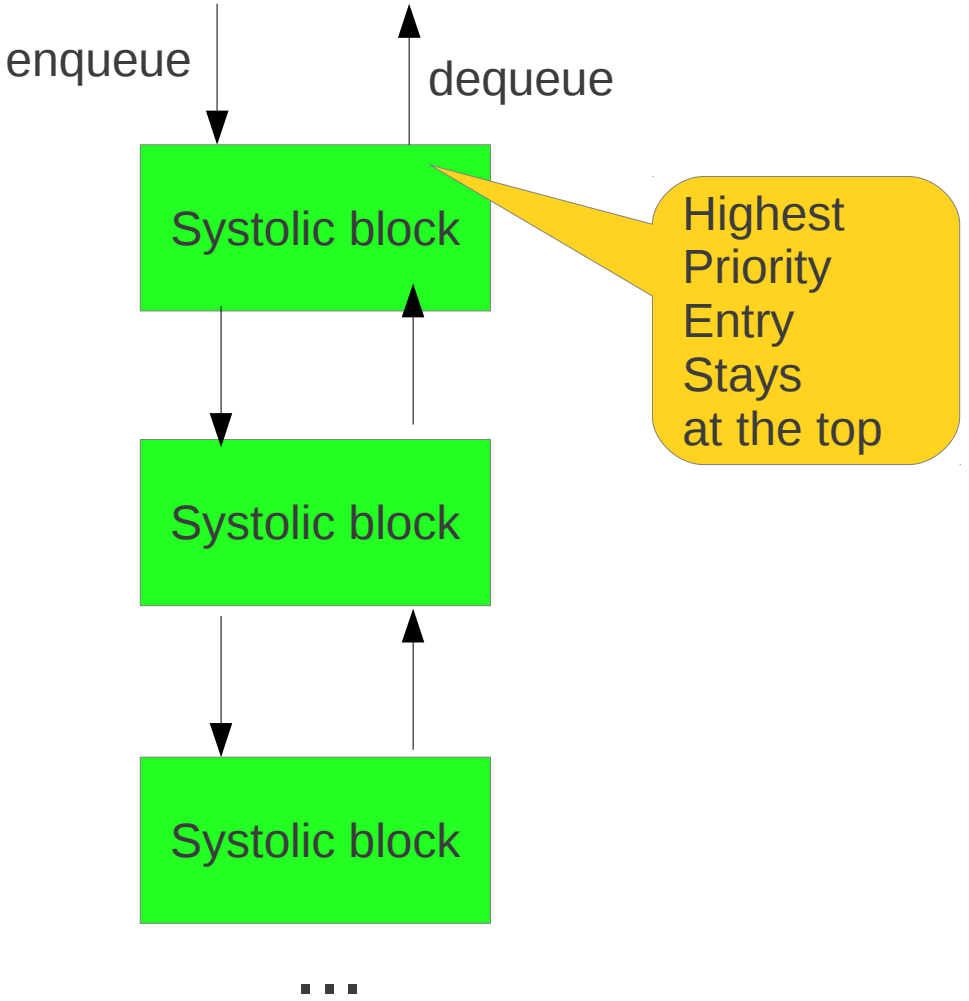
Tagged Up/Down H/W Sorter



Implementation

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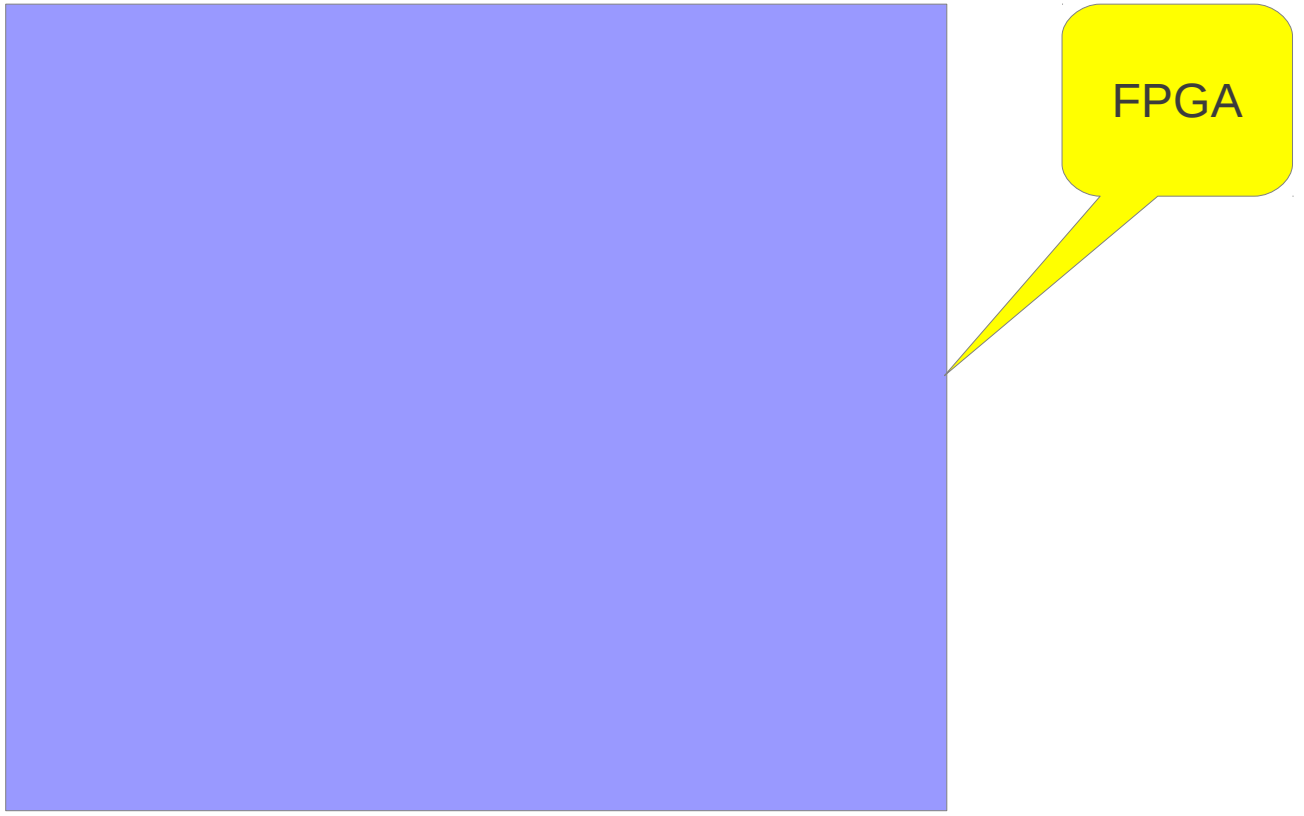

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- FPGA
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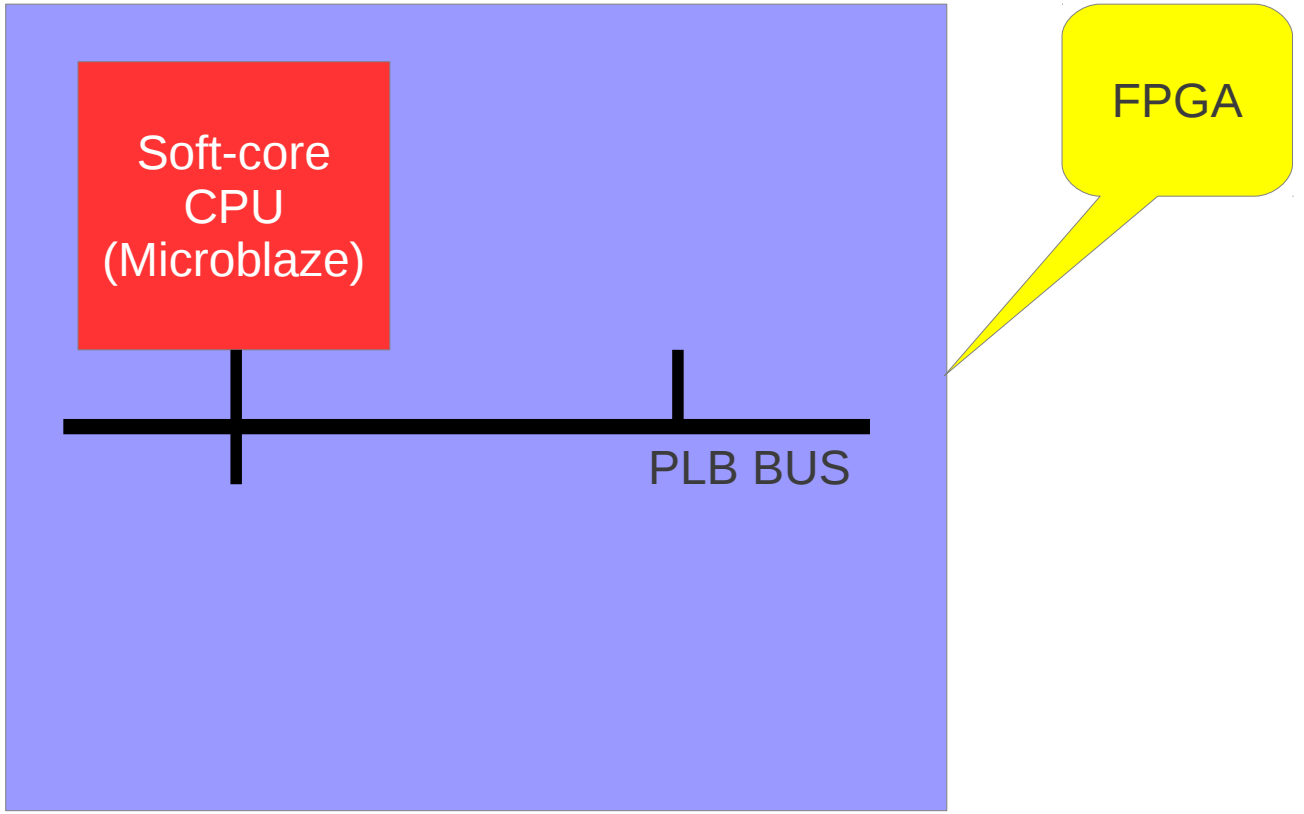

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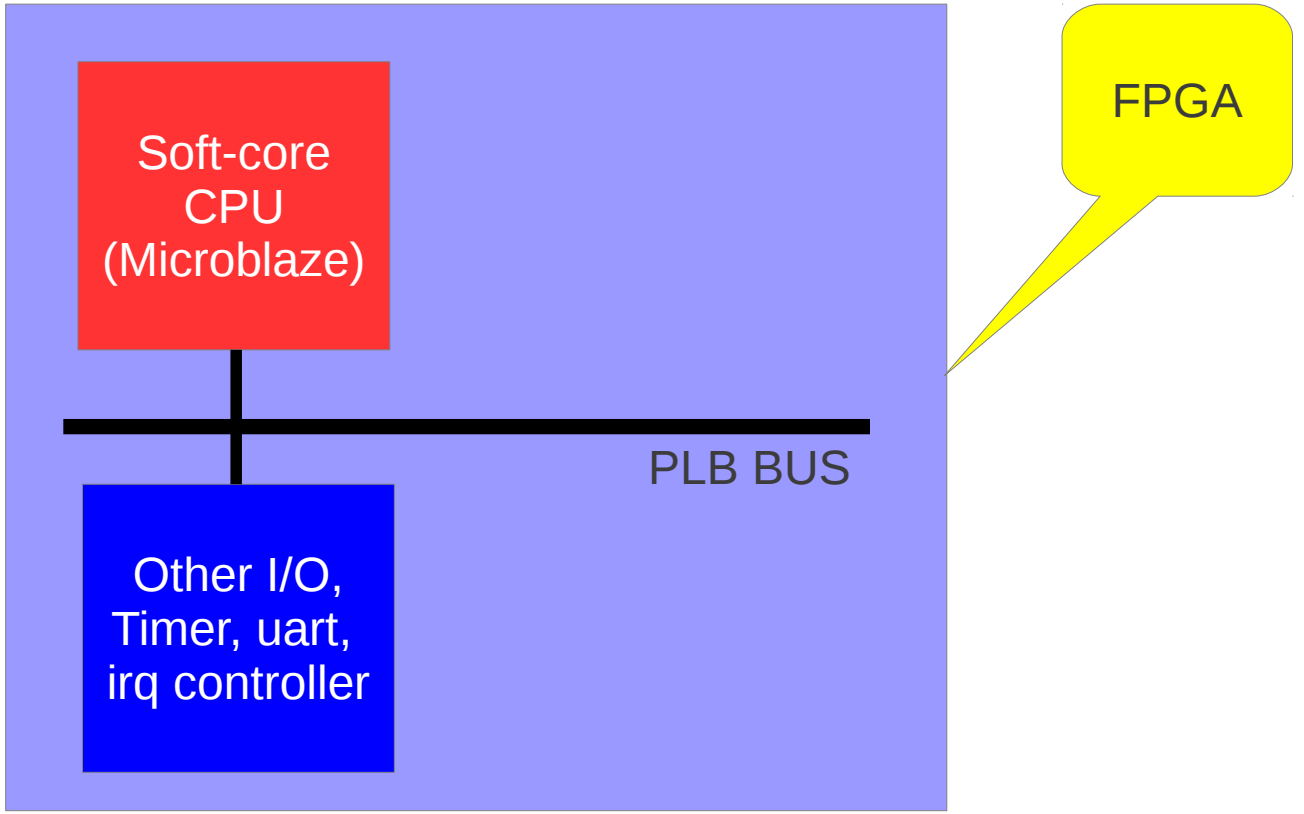

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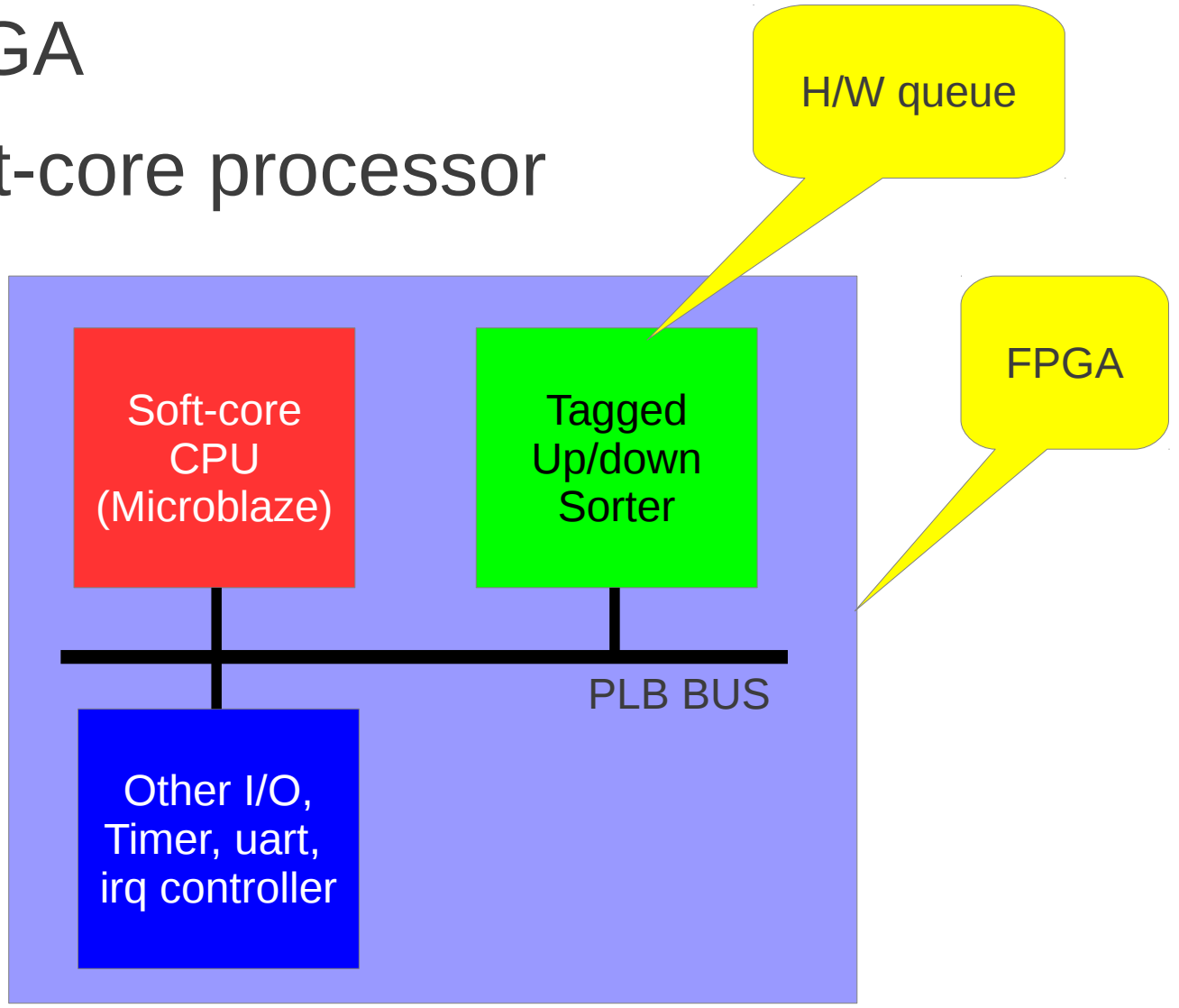

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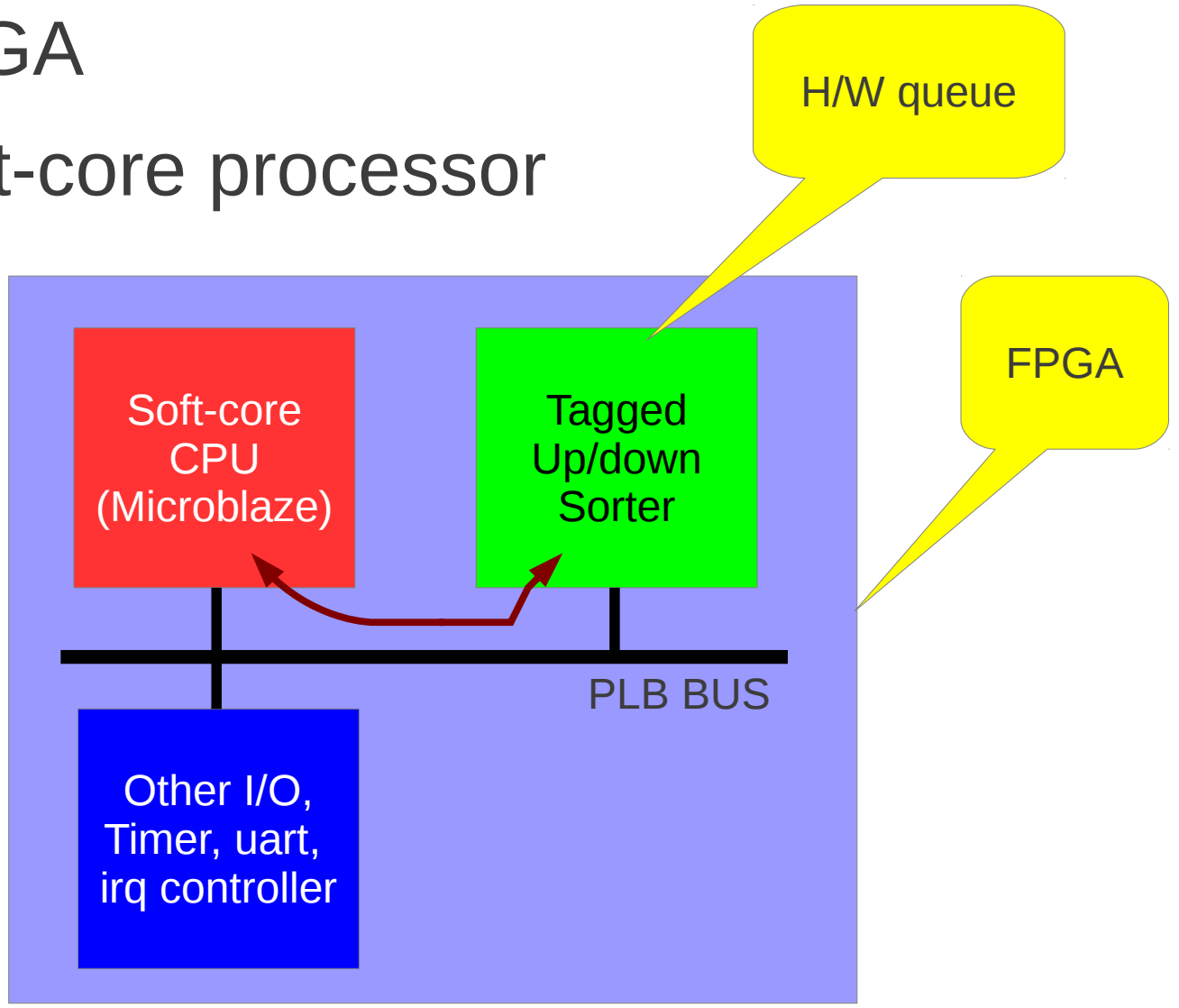
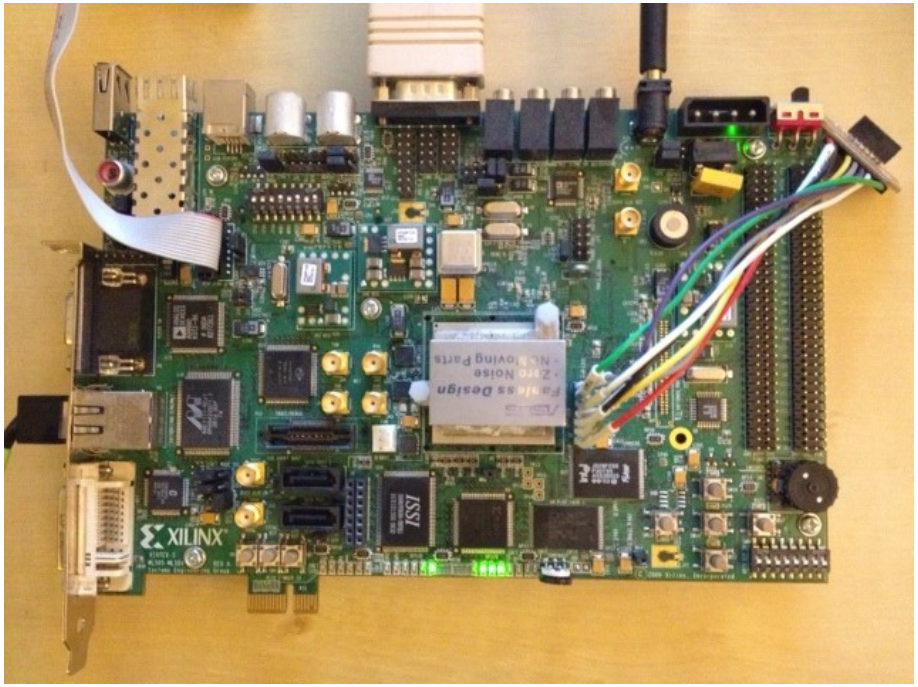


Experimental setup

- FPGA (Field Programmable Gate Array)
  - Xilinx Virtex5
- Soft-core CPU
  - Microblaze
- ML505 evaluation board



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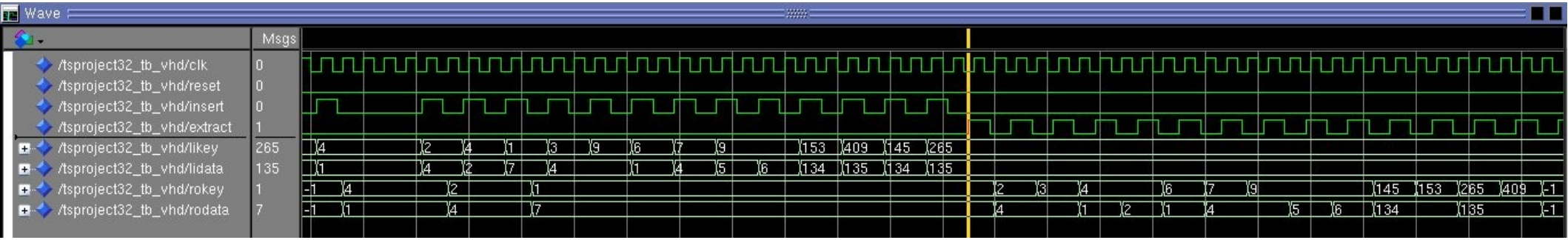

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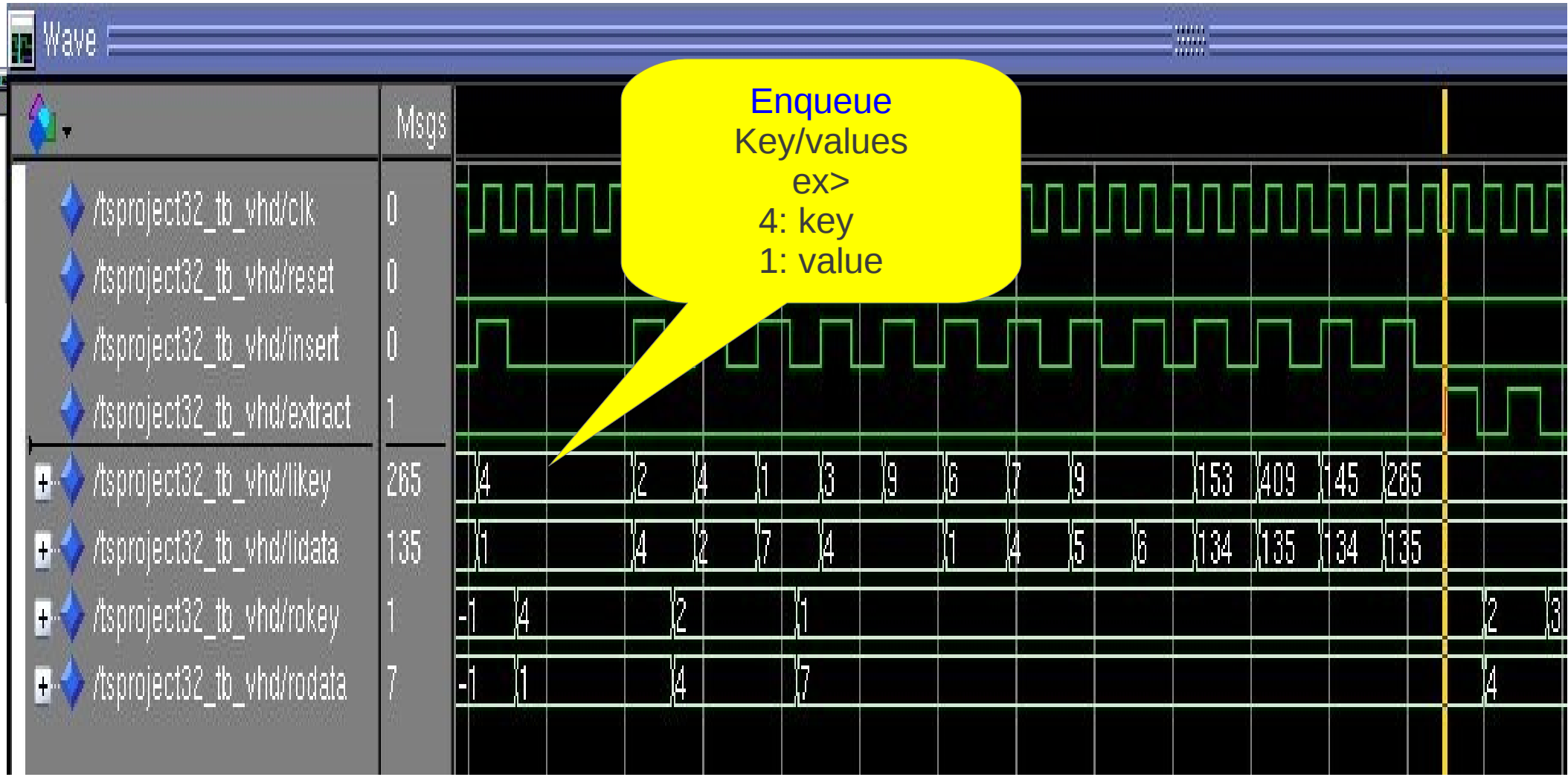

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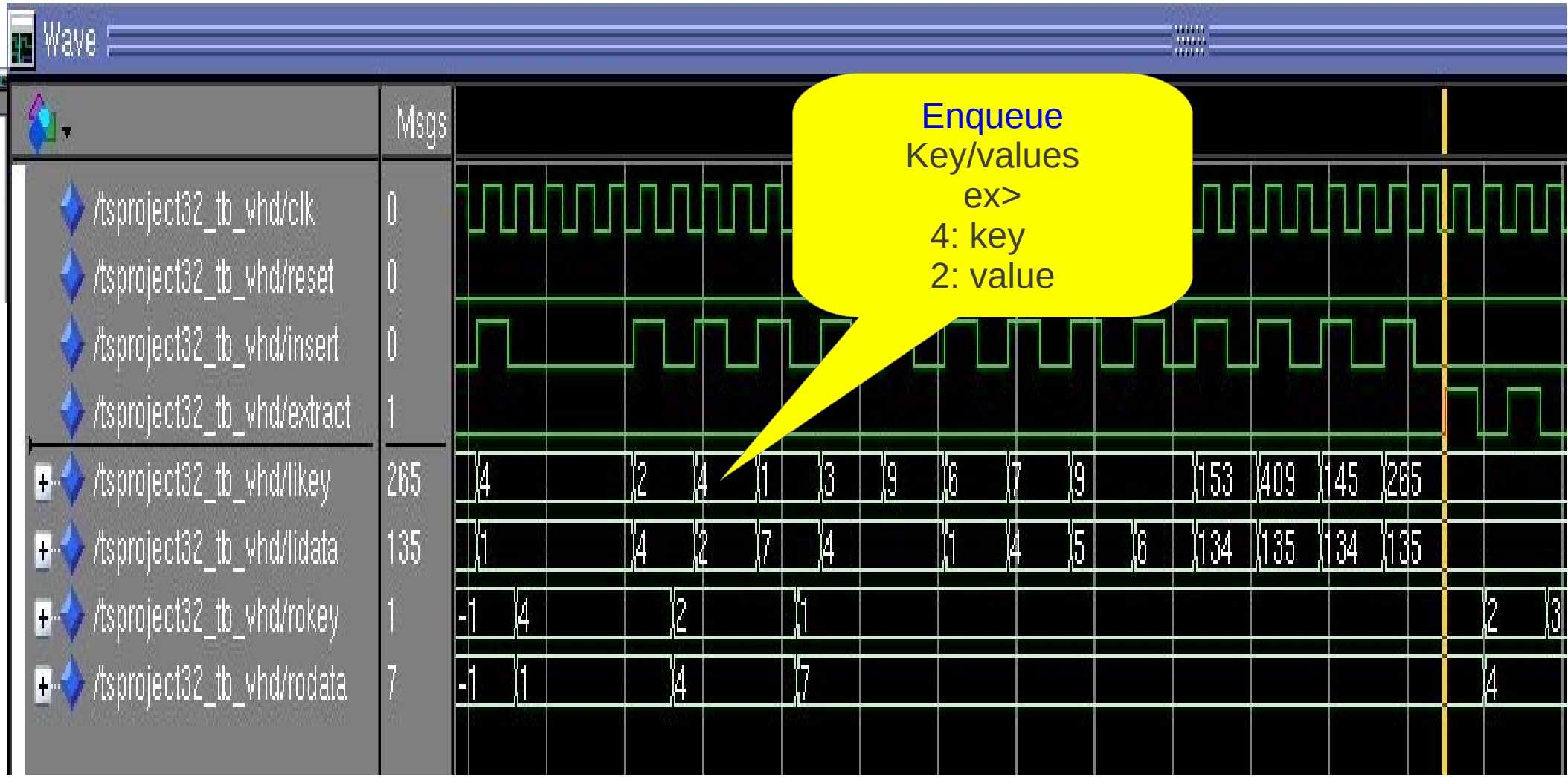

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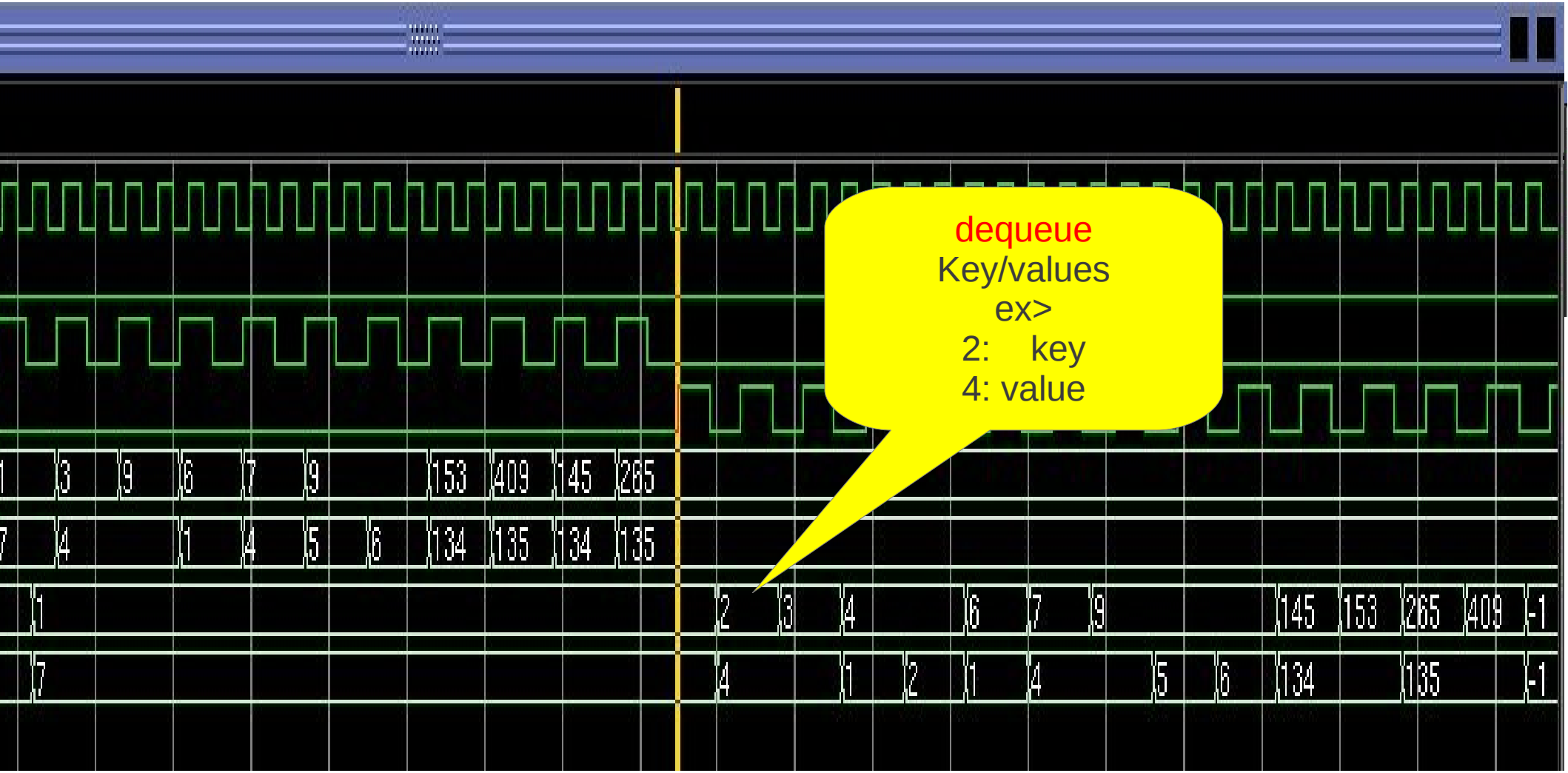

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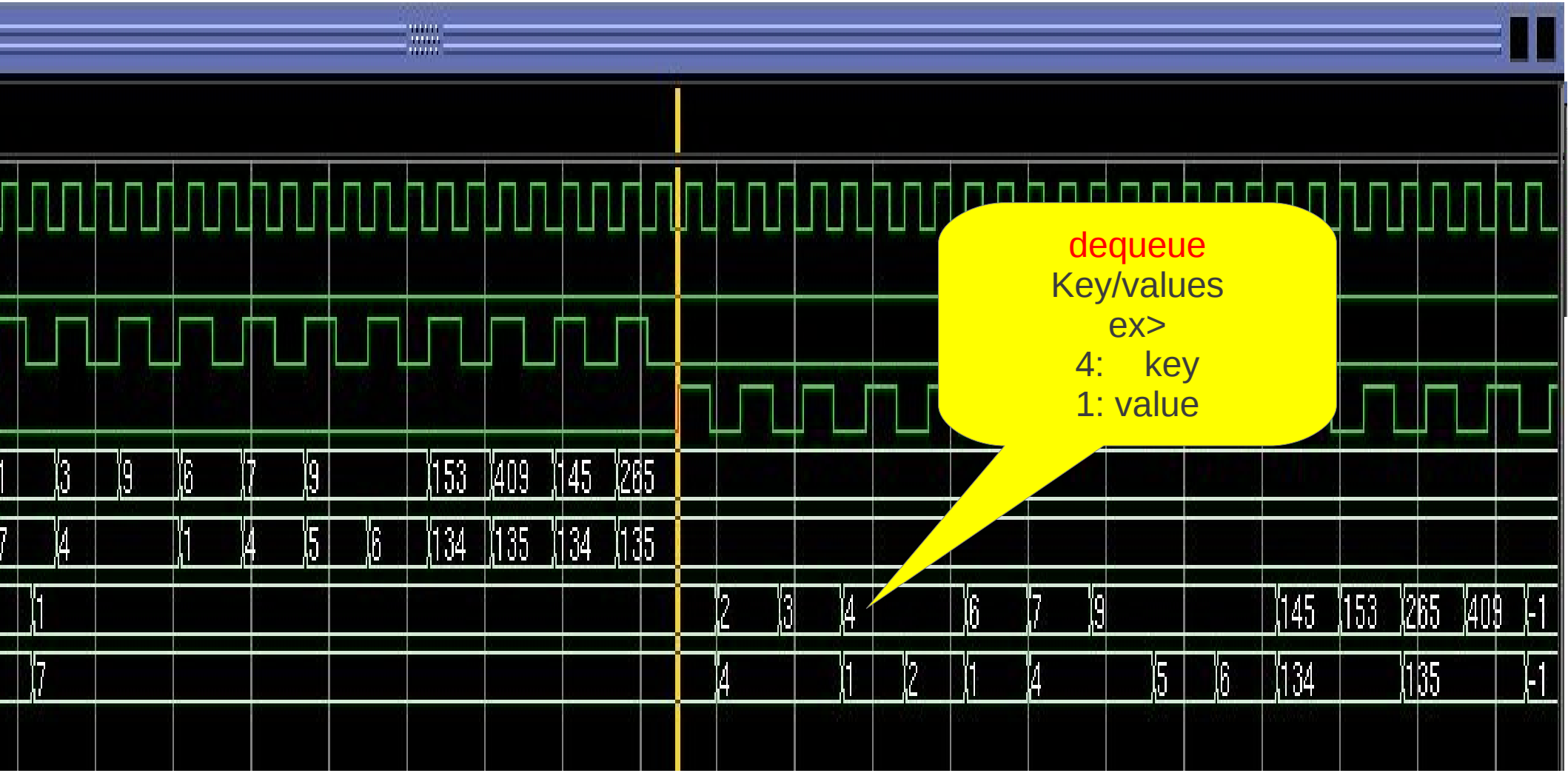

H/W Priority Queue Simulation

Scheduler change, sched_fair.c

```
/*
 * modified __enqueue_entity() to use Tagged Sorter
 * instead of rb-tree
 */
static void __enqueue_entity(struct cfs_rq *cfs_rq, struct sched_entity *se)
{
  struct rb_node **link = &cfs_rq->tasks_timeline.rb_node;
  struct rb_node *parent = NULL;
  struct sched_entity *entry;

  s64 key = entity_key(cfs_rq, se);
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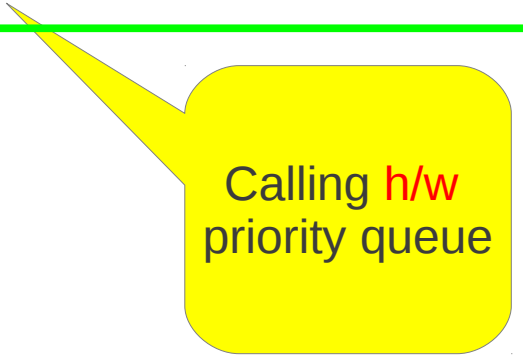


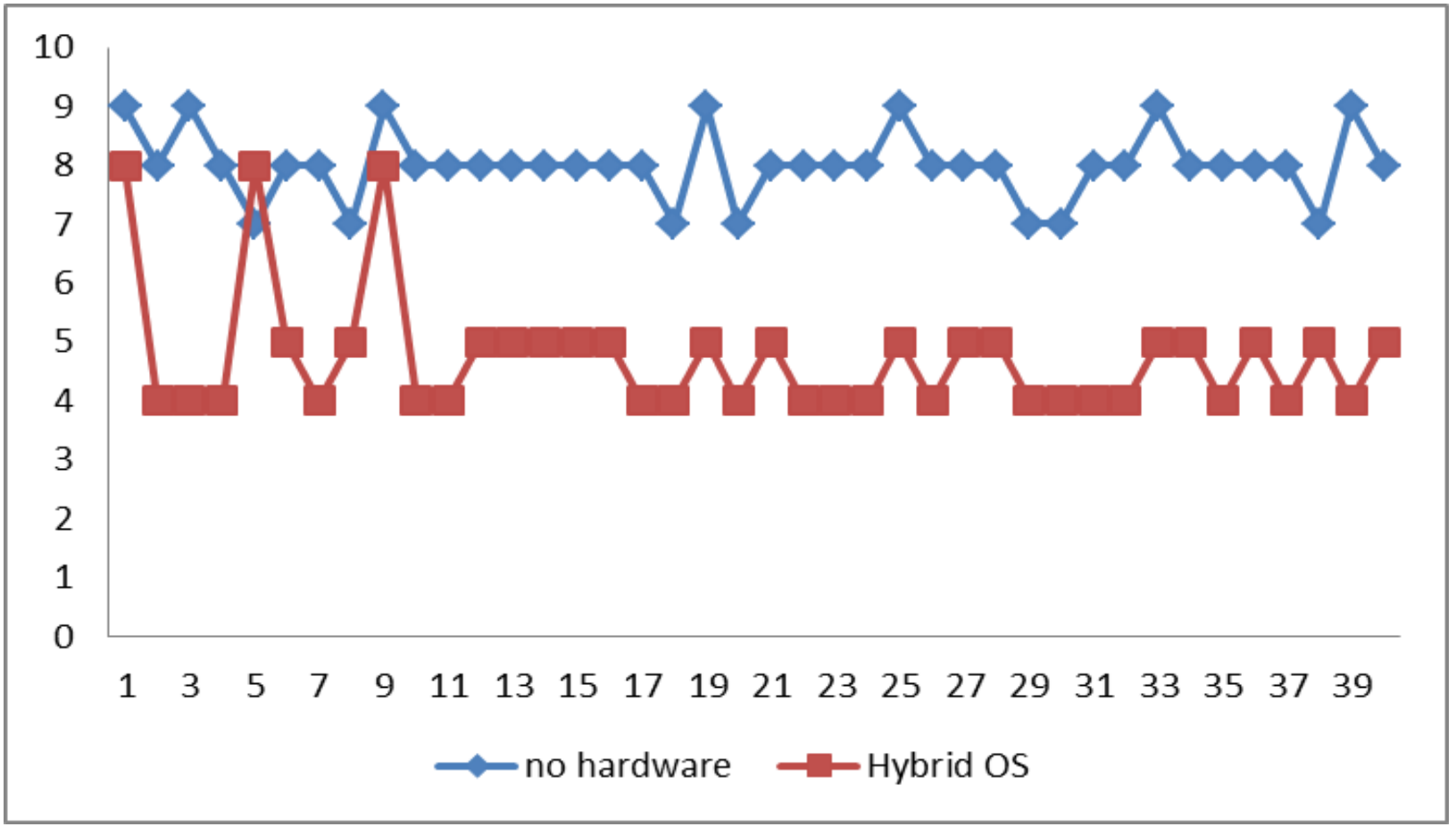
H/W interface

```
/*
 * enqueue entity to Tagged Sorter (HyOS)
 */
static void __enqueue_tagged_sorter(unsigned int key, unsigned int  data)
{
  if (init == 0) {
    hyos = (char*)ioremap(XPAR_HYOS_PLB_0_BASEADDR, 0x10000);
    init = 1;
  }

  if (hyos != NULL) {
    iowrite32(key,hyos+4*4);    // key
    iowrite32(data,hyos+5*4);   // val
    iowrite32(0xffffffff,hyos); // enqueue trigger
    iowrite32(0x0,hyos);
  }
}
```

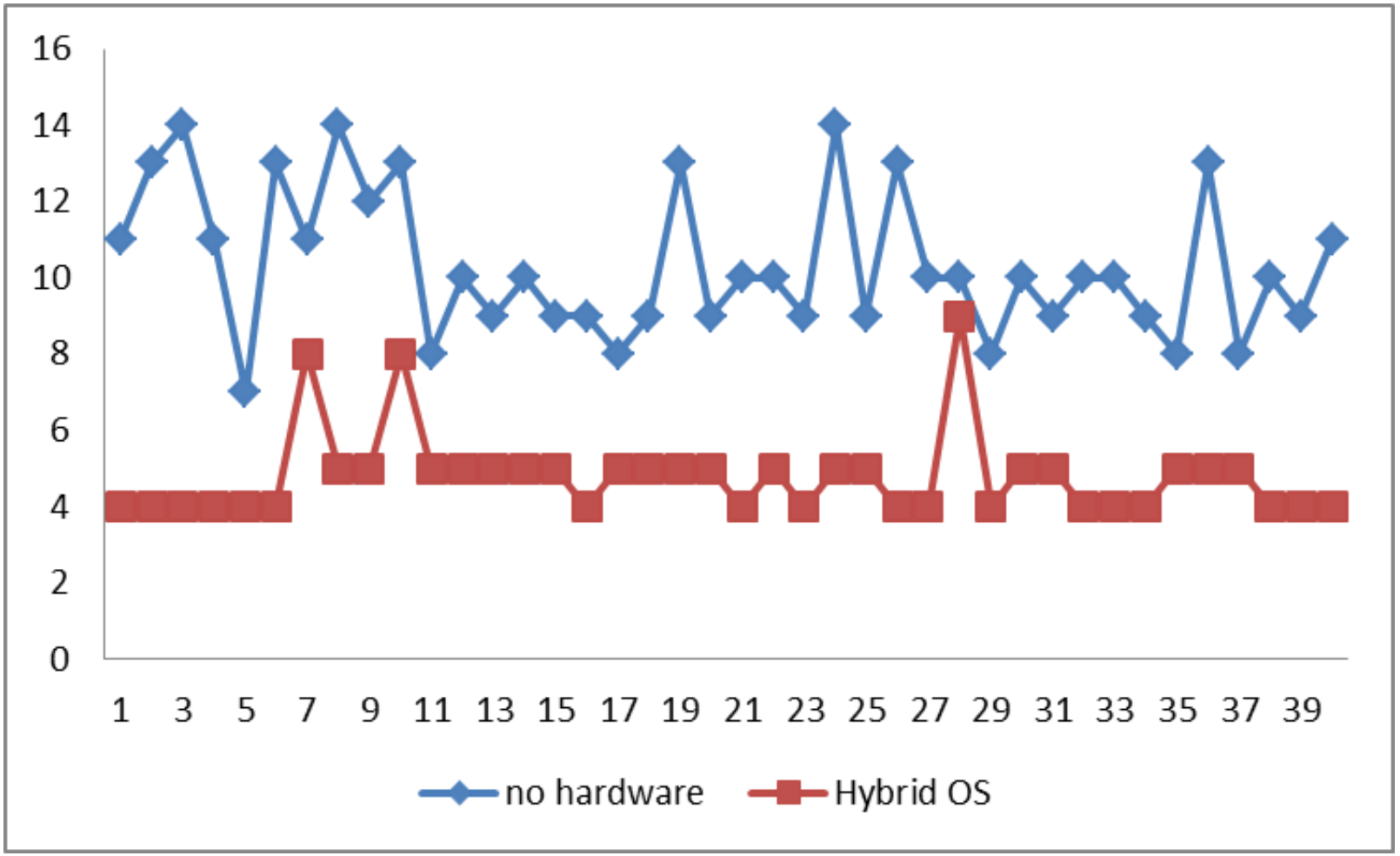
Experimental results 1

- Enqueue time for no load



Experimental results 2

- Enqueue time for 4 yes



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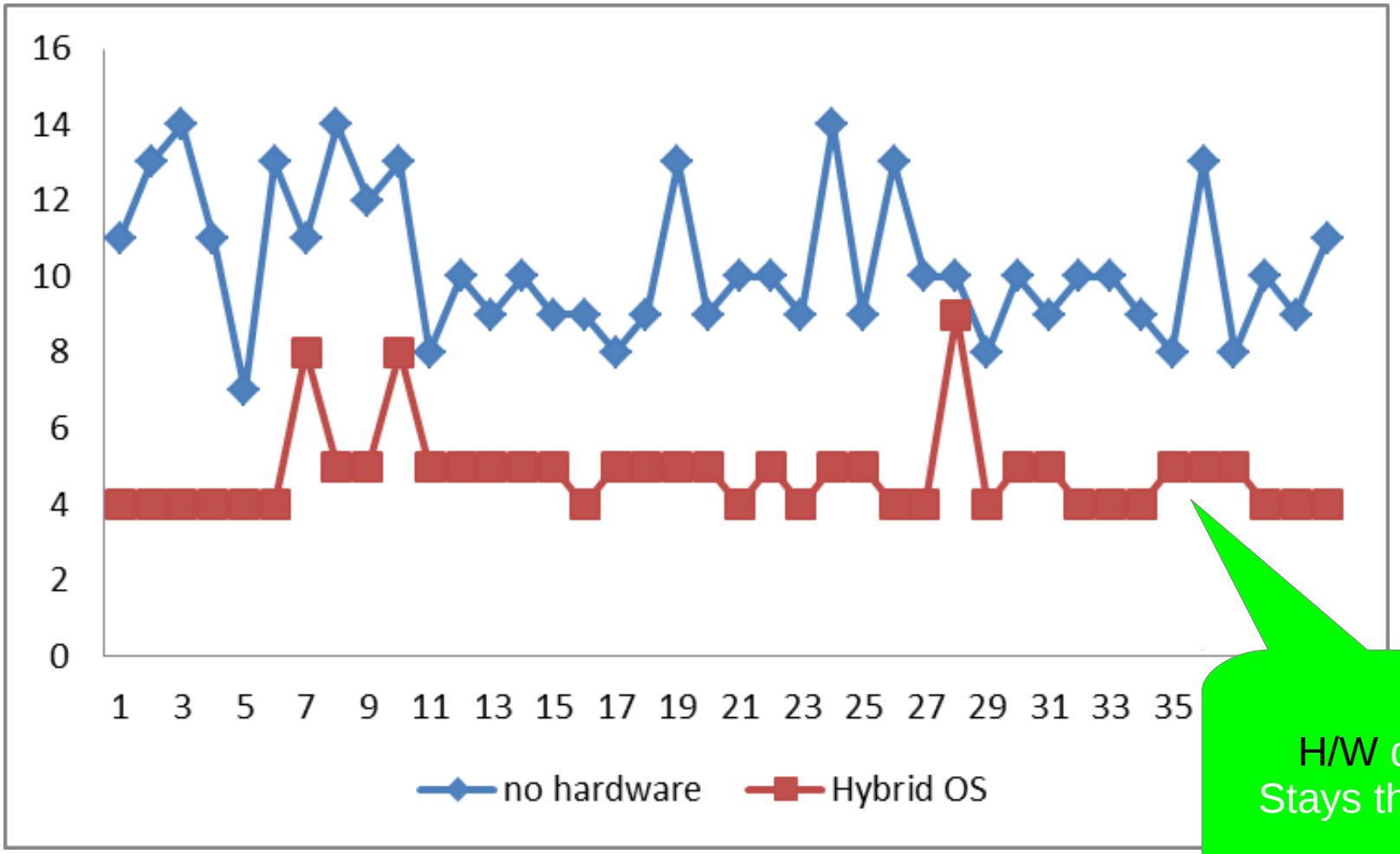
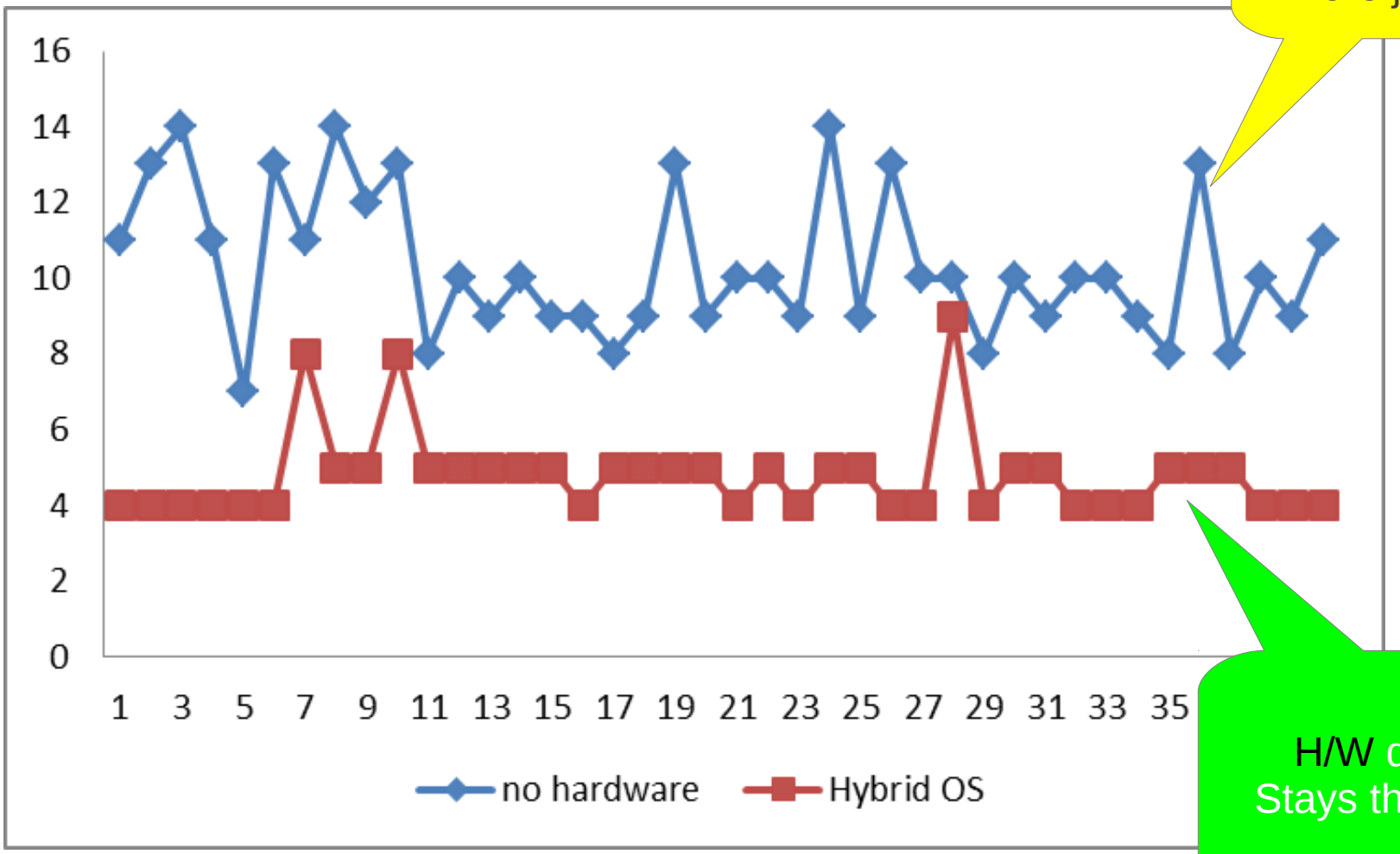


Experimental results 2

- Enqueue time for 4 yes



S/W queue increased & more jitters

H/W queue Stays the same

Conclusion

- H/W OS and H/W accelerator can
  - Improve performance
  - Reduce overhead
- Hybrid approach
  - Instead of implement full scheduler
  - Off-load a commonly used s/w component to h/w

- Could look for more s/w components could be off-loaded

Thank you!

Questions?