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# OrCAD® X Capture

**Course Version 24.1**

**Lab Manual**

**Revision 1.0**

**cadence®**

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## Table of Contents

### OrCAD X Capture

<b>Module 1:</b>	<b>About This Course .....</b>	<b>9</b>
	There are no labs for this module.....	11
<b>Module 2:</b>	<b>Introduction to OrCAD X Capture.....</b>	<b>13</b>
<b>Lab 2-1</b>	<b>Setting Environment Variables.....</b>	<b>15</b>
	Renaming Existing Environment Variables Renaming.....	16
	Setting the CDS_SITE Variable.....	17
	Setting the HOME Variable .....	18
<b>Lab 2-2</b>	<b>Opening the Sample Project.....</b>	<b>19</b>
	Starting OrCAD® X Capture .....	19
	Closing the Start Page .....	19
	Setting Application to Light Theme.....	20
	Opening a Project.....	20
	Opening a Schematic .....	21
	Zooming.....	21
	Panning.....	22
<b>Lab 2-3</b>	<b>Selecting Objects .....</b>	<b>24</b>
	Selecting Multiple Objects .....	24
	Using the Selection Filter.....	25
<b>Lab 2-4</b>	<b>Editing Objects.....</b>	<b>27</b>
	Moving Individual Parts and Wires.....	27
	Moving a Group.....	27
	Using Delete and Undo .....	27
	Copying Parts .....	28
<b>Lab 2-5</b>	<b>Using the Help System (Optional) .....</b>	<b>30</b>
	Accessing Online Help.....	30
<b>Module 3:</b>	<b>Setting Up Your Environment.....</b>	<b>31</b>
<b>Lab 3-1</b>	<b>Setting Up Preferences.....</b>	<b>33</b>
	Opening the Intro Project .....	33
	Assigning Colors.....	33
	Restoring Default Colors.....	34
	Controlling Area Selection.....	34
	Setting Miscellaneous Preferences .....	35
	Setting Auto Backup Preferences .....	37
	Closing the Project .....	37
<b>Lab 3-2</b>	<b>Setting Up the Design Template.....</b>	<b>38</b>
	Accessing Design Template Settings .....	38
	Filling in the Title Block Information .....	39
	Adding a Name and Address .....	39
	Adding a Document Number, Revision, and CAGE Code .....	39
	Adding the Title Block.....	39

<b>Module 4:</b>	<b>Working with Libraries .....</b>	<b>41</b>
<b>Lab 4-1</b>	<b>Opening and Viewing an Existing Library .....</b>	<b>43</b>
	Opening the CLASS_LIB Library .....	43
	Viewing a Part.....	44
	Closing the Library .....	45
<b>Lab 4-2</b>	<b>Creating a New PRACTICE_LIB Library .....</b>	<b>46</b>
	Renaming the Library .....	46
<b>Lab 4-3</b>	<b>Copying and Renaming Parts and Symbols .....</b>	<b>47</b>
	Opening a Cadence-Supplied Library .....	47
	Copying Between Libraries.....	48
	Renaming the GND_POWER Symbol .....	50
<b>Lab 4-4</b>	<b>Creating a Homogeneous Part .....</b>	<b>51</b>
	Adding a New Part to the Library .....	51
	Creating the Part Graphics .....	52
	Resizing the Bounding Box .....	53
	Adding Pins.....	54
	Modifying Pin Properties .....	55
	Adding Power Pins .....	57
	Assigning Pin Numbers to All Gates in the Package .....	58
	Setting Up Pin Swapping.....	59
	Adding a User Property .....	60
	Controlling Display of Properties.....	61
	Controlling Display of Pin Names .....	62
<b>Lab 4-5</b>	<b>Creating a Heterogeneous Part.....</b>	<b>63</b>
	Creating the Symbol for the First Gate .....	63
	Adding Pins.....	64
	Placing the Power Pins .....	66
	Hiding Pin Names .....	68
	Adding a Gate-Grouping Property .....	68
	Creating the Symbol for Gates 2, 3, and 4.....	69
<b>Lab 4-6</b>	<b>Creating a Power Symbol.....</b>	<b>71</b>
<b>Lab 4-7</b>	<b>Creating Parts Using a Spreadsheet Interface.....</b>	<b>74</b>
<b>Lab 4-8</b>	<b>Splitting an Existing Part .....</b>	<b>78</b>
	Copying Between Libraries.....	78
	Using the Split Part Command.....	78
	Viewing the Split Part .....	81
<b>Lab 4-9</b>	<b>Generating Parts from Imported Data.....</b>	<b>82</b>
	Importing a Xilinx Pad File.....	82
	Viewing the Generated Part .....	84
	Importing a BGA Text File .....	84
	Viewing the Generated Part .....	85
<b>Module 5:</b>	<b>Building a Simple Schematic .....</b>	<b>87</b>
<b>Lab 5-1</b>	<b>Creating a New Project.....</b>	<b>89</b>
	Setting Project Name and Location.....	89
	Viewing the Schematic Title Block .....	90
<b>Lab 5-2</b>	<b>Placing Parts.....</b>	<b>91</b>
	Adding a 74F162 .....	91

	Adding a 74LS00 .....	94
<b>Lab 5-3</b>	<b>Adding and Naming Wires.....</b>	<b>96</b>
	Adding Wires .....	96
	Naming Wires .....	97
	Auto Wire Between Two Points .....	99
<b>Lab 5-4</b>	<b>Assigning Reference Designators.....</b>	<b>100</b>
	Manual Assignment .....	100
	Automatic Assignment .....	100
<b>Lab 5-5</b>	<b>Running Design Rules Check.....</b>	<b>102</b>
	Fixing the Unconnected Pin Warning.....	105
<b>Module 6:</b>	<b>Building a Multi-Sheet Schematic .....</b>	<b>107</b>
<b>Lab 6-1</b>	<b>Creating a New Project.....</b>	<b>109</b>
	Editing the Design Template.....	109
	Setting Project Name and Location.....	109
	Viewing the Title Block .....	110
	Viewing the System Files .....	110
	Viewing the Design Resources.....	110
<b>Lab 6-2</b>	<b>Creating Page1 .....</b>	<b>112</b>
	Adding a 12-Pin Header Connector.....	112
	Mirroring the Connector .....	113
	Assigning a Part Reference .....	113
	Adding Decoupling Capacitors .....	114
	Copying the Capacitor.....	116
	Drawing the BUS Wire .....	117
	Adding BUS Connections .....	117
	Alternate Method to Drawing Bus Connections.....	118
	Adding Power and Ground Symbols .....	119
	Making Ground Symbol Names Visible.....	121
	Adding an Off-Page Connector .....	122
	Viewing Design Cache .....	124
<b>Lab 6-3</b>	<b>Copying from One Design to Another.....</b>	<b>125</b>
	Opening Two Projects at Once .....	125
	Copying Between Projects.....	125
<b>Lab 6-4</b>	<b>Completing the Schematic.....</b>	<b>127</b>
	Modifying the Copied Page .....	127
<b>Lab 6-5</b>	<b>Annotating a Multi-Sheet Design.....</b>	<b>130</b>
	Opening the Schematic .....	130
	Annotating Part References .....	130
	Viewing Results .....	130
	Using Reference Designator Controls.....	131
<b>Lab 6-6</b>	<b>Checking the Design for Errors .....</b>	<b>133</b>
<b>Lab 6-7</b>	<b>Cross Referencing Multi-Sheet Nets.....</b>	<b>135</b>
<b>Lab 6-8</b>	<b>Searching for Objects in the Schematic .....</b>	<b>137</b>
	Searching the Current Page .....	137
	Searching the Entire Design.....	138
	Searching for Specific Parts and Nets .....	139

<b>Lab 6-9</b>	<b>Modifying Wire Attributes.....</b>	<b>141</b>
	Assigning Attributes to the VCC Net.....	141
	Assigning Attributes to the CLOCK Net .....	142
<b>Module 7:</b>	<b>Editing Part Properties .....</b>	<b>145</b>
<b>Lab 7-1</b>	<b>Using the Property Editor .....</b>	<b>147</b>
	Pivoting the Spreadsheet .....	147
	Filtering by Object Type.....	148
	Selecting a Property Filter .....	149
<b>Lab 7-2</b>	<b>Using the Allegro X PCB Designer Property Filter .....</b>	<b>150</b>
	Applying the Property Filter.....	150
	Assigning a PCB Footprint Name .....	150
	Multiple Object Property Editing .....	152
	Multiple Object Property Display .....	153
	Adding a New Property to Multiple Objects .....	154
<b>Lab 7-3</b>	<b>Using an Update Properties File .....</b>	<b>156</b>
	Viewing the Parts Update File .....	156
	Updating Part Properties .....	156
	Viewing the Session Log and Report .....	158
	Viewing the Resulting Properties in the Schematic .....	158
<b>Lab 7-4</b>	<b>Using an Export/Import Properties File .....</b>	<b>160</b>
	Exporting Part Properties.....	160
	Viewing the Export File with Excel .....	161
	Editing the Export File .....	162
	Saving the Export File.....	162
	Importing the File.....	163
	Viewing Resulting Properties in the Schematic .....	164
<b>Lab 7-5</b>	<b>Multiple Object Editing with the Browse Spreadsheet.....</b>	<b>165</b>
	Searching for Off-Page Connectors .....	165
	Searching for Title Blocks .....	166
<b>Lab 7-6</b>	<b>Creating a Bill of Materials Report.....</b>	<b>168</b>
	Customizing the Format of the BOM Report.....	169
	Creating a Custom BOM Report .....	169
	Saving Line Item Definitions (Optional Information).....	170
<b>Lab 7-7</b>	<b>Creating a Netlist for Allegro X PCB Editor/OrCAD X Presto.....</b>	<b>171</b>
	Viewing Files in the Project Manager .....	172
<b>Module 8:</b>	<b>Building a Hierarchical Design .....</b>	<b>175</b>
<b>Lab 8-1</b>	<b>Opening and Viewing a Hierarchical Design.....</b>	<b>177</b>
	Opening the Training Project.....	177
	Viewing the Training Root Schematic .....	177
	Viewing the HSRAM Schematic .....	178
	Viewing the Data Schematic.....	178
<b>Lab 8-2</b>	<b>Editing the Training Root Schematic .....</b>	<b>180</b>
	Opening the Training Root Schematic .....	180
	Adding Ground to Connector J1 .....	180
	Adding the BA[0-7] Bus .....	182
	Adding Off-Page Connectors .....	186

	Viewing Online DRC Warnings .....	187
	A Note About Net Names .....	187
	Adding Bypass Capacitors .....	188
<b>Lab 8-3</b>	<b>Making Power Pins Visible .....</b>	<b>190</b>
<b>Lab 8-4</b>	<b>Reusing a DAAMP Block .....</b>	<b>192</b>
	Copying Between Projects.....	192
	Viewing the Copied DAAMP Design .....	193
	Opening the DATA Schematic .....	194
	Adding a DAAMP Block Symbol to the DATA Schematic .....	194
	Instantiating Another DAAMP Block .....	196
	Synchronizing the DATA Schematic and Block Symbol .....	197
	Finishing the DATA Schematic .....	199
<b>Lab 8-5</b>	<b>Annotating the Design .....</b>	<b>202</b>
	Viewing Reference Designator Assignments .....	203
<b>Lab 8-6</b>	<b>Running Design Rules Check .....</b>	<b>205</b>
	Setting Up the Design Rules Check .....	205
	Reviewing the DRC Report .....	207
<b>Lab 8-7</b>	<b>Waiving DRCs .....</b>	<b>209</b>
	Viewing the Error Markers .....	209
	Waiving DRCs in Schematic and Report .....	210
	Restoring Waived DRC Markers .....	210
	Alternate Method for Restoring Waived DRCs .....	211
<b>Lab 8-8</b>	<b>Hierarchical Cross Referencing and Plotting .....</b>	<b>213</b>
	Adding Intersheet References .....	213
	Viewing the Intersheet Reference Report .....	214
	Viewing the Intersheet References in the Hierarchical Design .....	214
	Fixing the Intersheet Reference Warnings .....	215
<b>Lab 8-9</b>	<b>Creating a Bill of Materials Report .....</b>	<b>218</b>
<b>Lab 8-10</b>	<b>Archiving a Project .....</b>	<b>219</b>
<b>Lab 8-11</b>	<b>Creating a New Project from an Existing One .....</b>	<b>221</b>
<b>Appendix A:</b>	<b>Optional Topics .....</b>	<b>225</b>
<b>Lab A-1</b>	<b>Customizing Toolbars .....</b>	<b>227</b>
	Opening and Closing the Toolbars .....	227
	Adding or Removing Icons from Toolbars .....	227
<b>Lab A-2</b>	<b>Testing the LM324 Part .....</b>	<b>229</b>
	Creating a Test Design .....	229
	Adding the <i>PRACTICE_LIB</i> to Your Project Setup .....	230
	Placing the LM324 .....	231
	Editing the PACKAGE Property .....	232
	Annotating the Test Design .....	234
<b>Lab A-3</b>	<b>Creating a Custom Title Block .....</b>	<b>235</b>
	Opening the Title Block Symbol .....	235
	Adding Reserved Title Block Properties .....	235
	Adding Page Name Property .....	238
	Adding a Company Logo .....	239
	Specifying Default Title Block Content .....	239

Testing the Title Block .....	240
<b>Lab A-4    Manually Creating a Hierarchical Block Symbol .....</b>	<b>241</b>
Top-Down Method.....	241
Drawing the Rectangle.....	241
Adding Block Pins D0-D7.....	242
Adding Block Pins VCLK, GAIN, VREF and OUT.....	243
Creating the LOGIC Circuit Schematic .....	244
Deleting the LOGIC Circuit.....	245
<b>Lab A-5    Using the Fisheye View .....</b>	<b>246</b>
Switching to Fisheye Mode.....	246
Setting the Fisheye Focus.....	247
Setting the Fisheye Dynamic Focus Mode .....	248
Fisheye Zoom Levels .....	249
<b>Appendix B:    Keyboard Shortcuts (Hot Keys).....</b>	<b>251</b>

## **Module 1: About This Course**

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**There are no labs for this module.**

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## **Module 2: Introduction to OrCAD X Capture**

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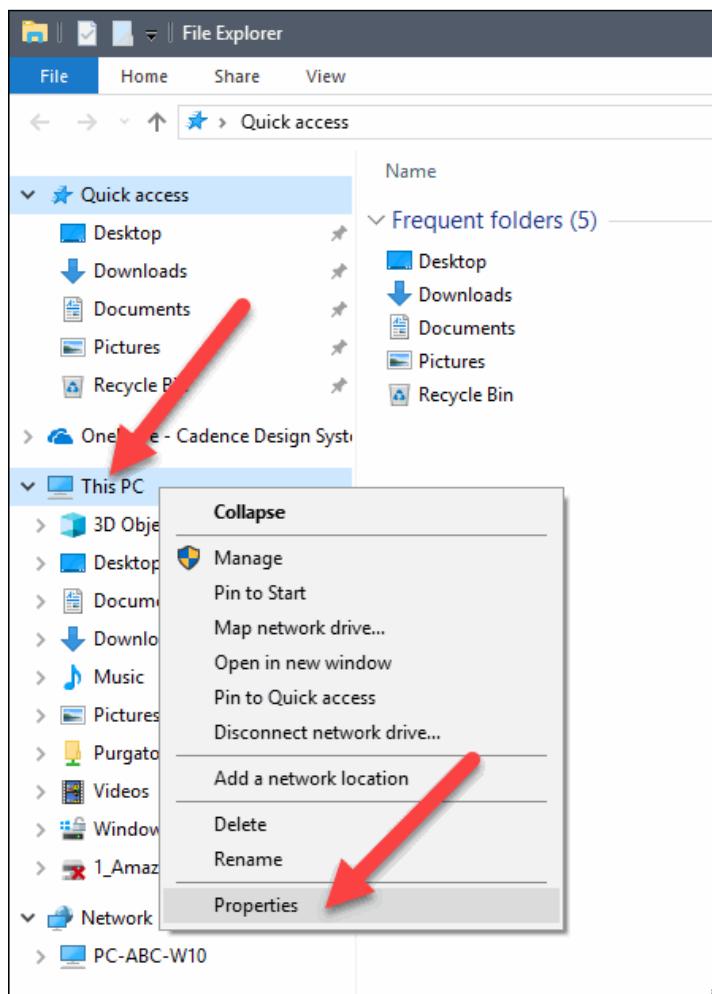
## Lab 2-1 Setting Environment Variables

**Objective:** To define variables needed for class setup.

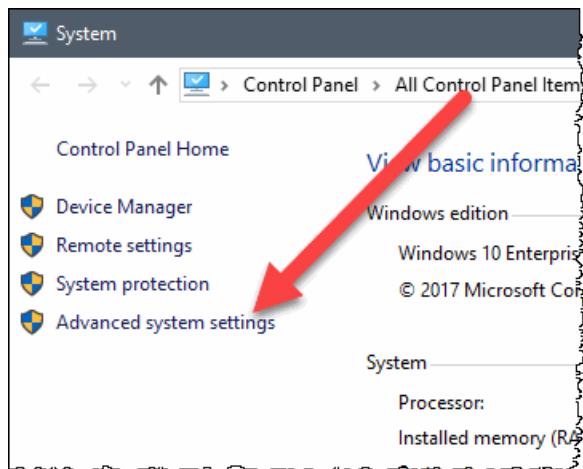
This course requires the CDS\_SITE system variable to be set to the <course\_dir>/Capture/site folder, where <course\_dir> is the path to the Capture folder on your system.

The path to the Capture folder should not contain spaces. For example, create the C:/user1 folder and place the Capture folder there. Then set the CDS\_SITE system variable to C:/User1/ Capture/site.

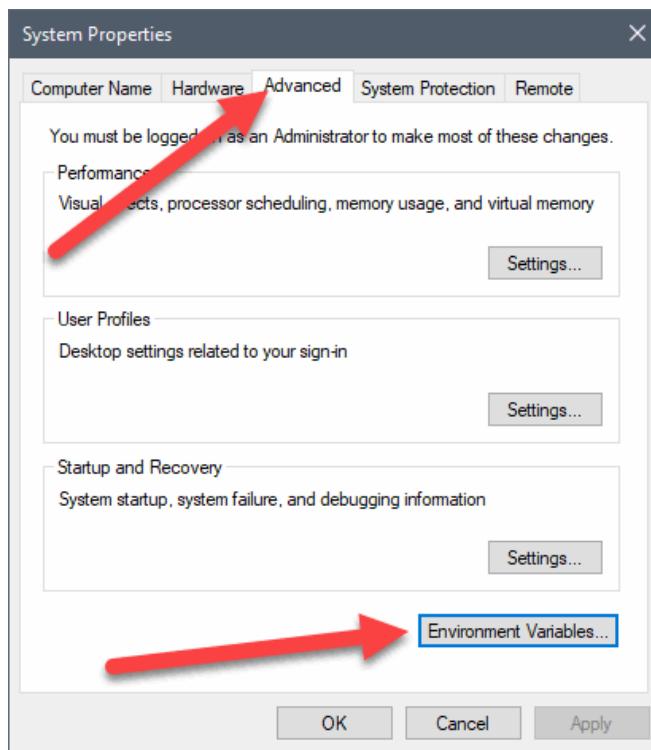
1. Open a **File Explorer** window.
2. Right-click on **This PC** and select **Properties** from the pop-up menu.



3. Click the **Advanced system settings** link in the left column.



4. In the System Properties window, click on the **Advanced** tab, then click the **Environment Variables** button near the bottom of that tab.

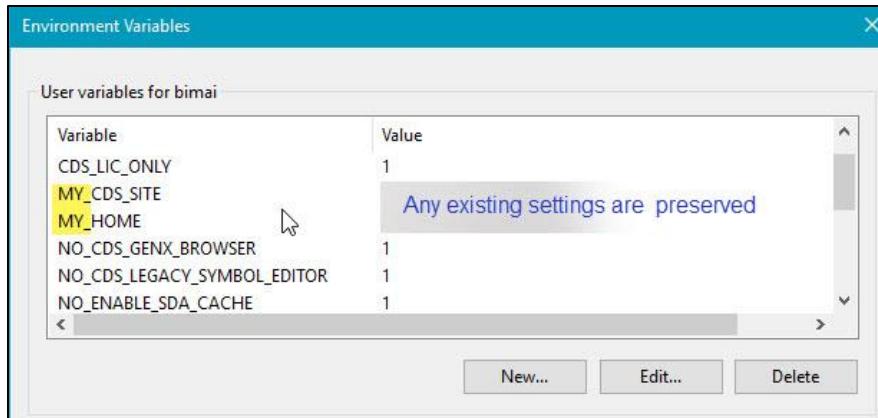


## **Renaming Existing Environment Variables Renaming**

Renaming existing system variables preserves your system setup so you can restore it after training.

1. Look for existing CDS\_SITE and HOME variables on your system.  
They would most likely be listed in the User variables window.

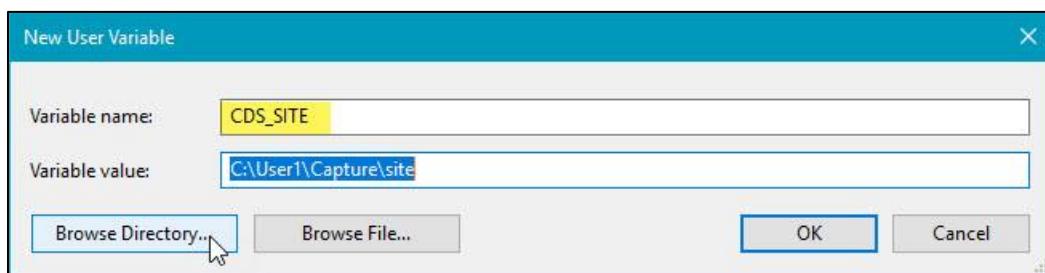
2. If you have an existing HOME variable defined on your system, select it, click **Edit**, and change the variable name to MY\_HOME.
3. Click **OK** in the Edit User Variable window.
4. If you have an existing CDS\_SITE variable, select it, click **Edit** and change the variable name to MY\_CDS\_SITE.



## Setting the CDS\_SITE Variable

1. In the User Variables section, click **New**.
2. In the New User Variable window, enter **CDS\_SITE**.
3. Click **Browse Directory** and select the *C:\User1\Capture\site* folder.

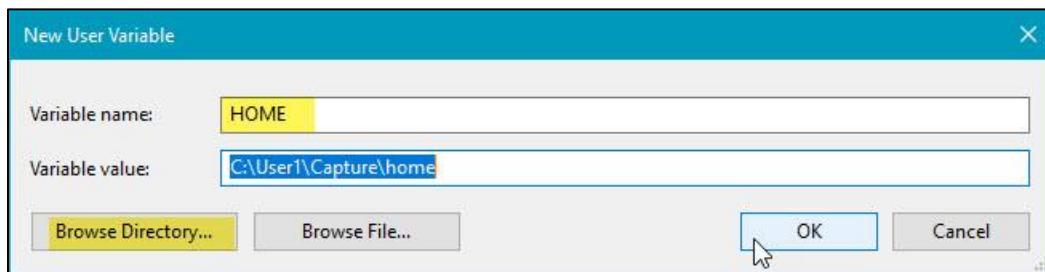
**Important:** In the following step, the *C:\User1* portion of the path will vary. Always replace the *C:\User1* portion of your lab instructions with the actual path to the Capture folder on your system.



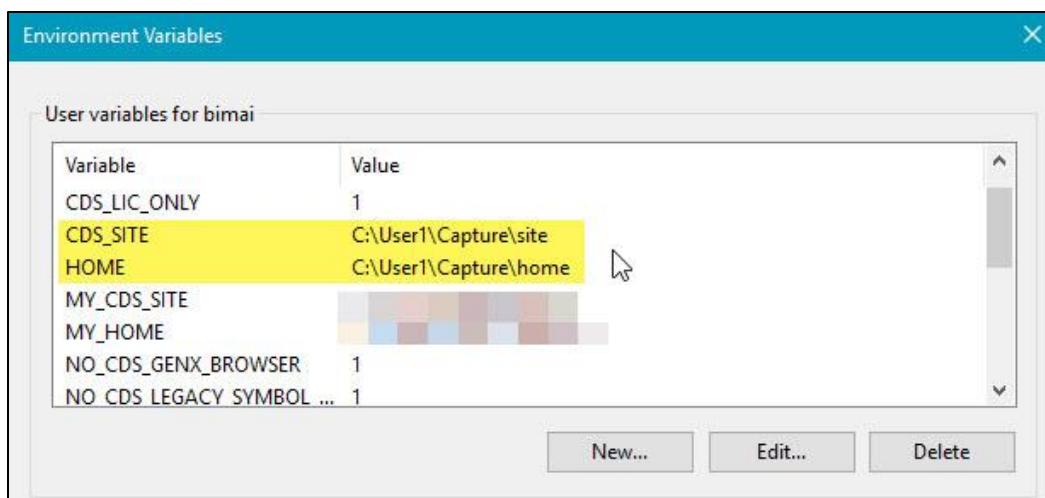
4. Click **OK**.

## Setting the HOME Variable

1. In the User Variables section, click **New**.
2. In the New User Variable window, enter **HOME**.



3. Click **Browse Directory** and select the *C:\User1\Capture\home* folder.
4. Click **OK**.



**Important:** Remember that you need to replace the path shown above with the actual path to these folders on your system.

5. Click **OK** to close the Environment Variables window.
6. Click **OK** in the System Properties window.
7. Close the System window.



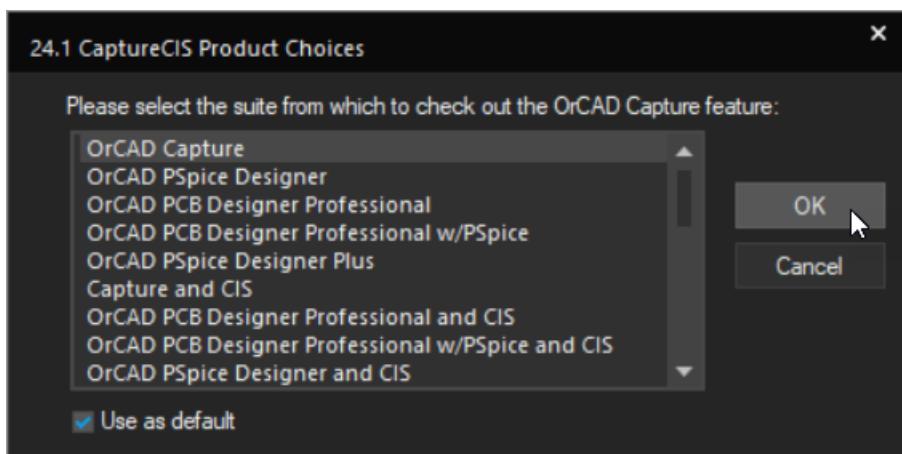
## Lab 2-2 Opening the Sample Project

**Objective:** To introduce some basic operations.

---

### Starting OrCAD® X Capture

1. Choose **Start – Cadence OrCAD X and Allegro X 24.1 – Capture CIS 24.1**.
2. In the Cadence® Product Choices window, select **OrCAD Capture**.



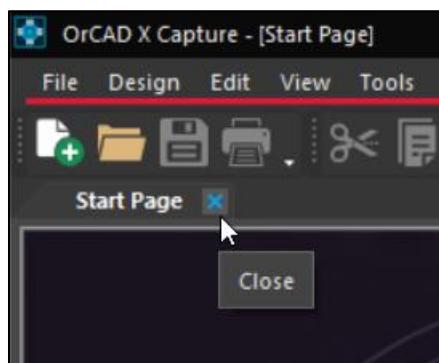
**Note:** If no license prompt appears, use the **File – Change Product** command in the Capture window to choose your license.

3. Click the **Use as default** option and click **OK**.

The Capture session window appears.

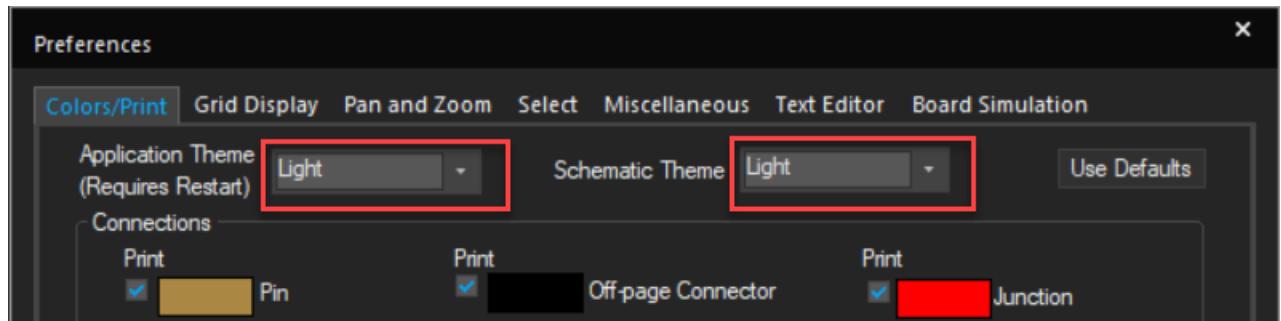
### Closing the Start Page

1. Click on the **Start Page** tab to close.



## Setting Application to Light Theme

1. Choose **Options – Preferences**.
2. In the **Colors/Print** tab, toggle the Application Theme to Light.



3. Click **OK**.

## Restart Session

1. Choose **File – Exit**.
2. Choose **Start – Cadence OrCAD X and Allegro X 24.1 – Capture CIS 24.1**.
3. Notice the Capture session window is now in a light theme.
4. Briefly glance at the Start Page contents.
5. Close the **Start Page** tab.

To open the Start Page again, choose **Help – Start Page**.

## Opening a Project

1. Choose **File – Open – Project**.

The Open Project window appears.

**Important:** In the following step, the *C:\User1* portion of the path will vary. Always replace the *C:\User1* portion of your lab instructions with the actual path to the *Capture* folder on your system.

2. Navigate to the *C:\User1\Capture\sample* directory.

The *Capture* folder is your lab database. All your lab files are stored in this folder.

3. Select **sample.opj** and click **Open**.

The Project Manager window opens.

4. Notice that the path to the project file is displayed at the top of the Capture session window.

## Opening a Schematic

1. In the Project Manager window, **double-click .\sample.dsn**.

2. **Double-click Schematic**.

3. **Double-click PAGE1**.

Page one opens.

4. Maximize the schematic window and click the **Zoom to All** icon.

The schematic page fits to the window.



## Zooming

1. Click the **Zoom In** icon.

The image has been magnified by a factor of 2 to 1.



2. Click the **Zoom Out** icon.

You learn how to set user preferences like the zoom scale factor later in the course.



3. Press the **I** key to zoom in and the **O** key to zoom out.

4. When zooming in, notice that the view centers on your cursor.

5. You can also press the **Ctrl** key and use the scroll wheel to zoom in or out.

6. Click the **Zoom to Region** icon and notice that the cursor shape turns into a magnifying glass.



- a. Click (or drag) to define the area you want to zoom into.

- b. **Right-click** and select **End Mode** or use the **Esc** key to exit the command.

## Panning

1. Click the **Zoom to All** icon, followed by the **Zoom In** icon.

2. Place your cursor on a part (do not click).

3. Press the **C** key.

The location of your cursor becomes the new center point of view. Try this on another part.

4. To pan, press the **C** key and move the mouse back and forth (do *not* click with the mouse).

**Important:** For more information about all keyboard shortcuts and function key settings, see Appendix B.

## Panning with the Middle Mouse Button

1. Click the **middle** mouse button once. A panning cursor appears.



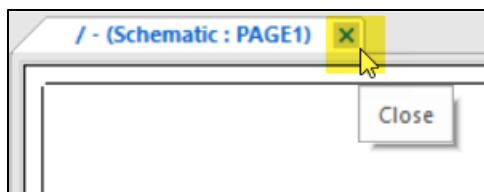
2. Move your cursor slowly around on the page to pan the view. When finished, click the **middle** mouse button again.

You can also press and hold the middle mouse button to pan the view.

## Closing the Schematic

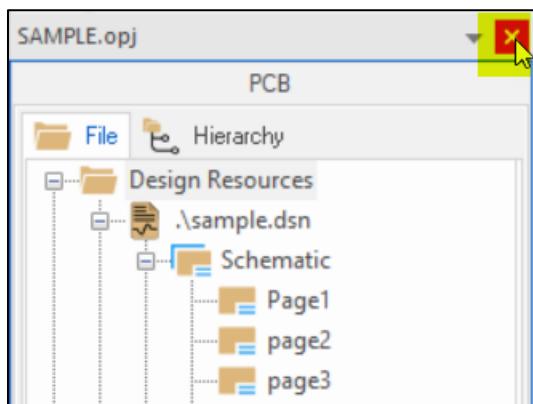
1. Click on the schematic page and choose **File – Close**.

You can also click the **X** on the **PAGE1** tab to close the page.



## Closing the Project

1. Click the X on the **sample** tab to close the project.



The main OrCAD X Capture session window is still running.



## Lab 2-3 Selecting Objects

**Objective:** To use the object selection features.

---

### Opening the Intro Project

1. Choose **File – Open – Project**.

The Open Project window appears.

2. Navigate to the *C:\User1\Capture\intro* directory, select **intro.opj**, and click **Open**.

### Opening the Schematic

1. In Project Manager, **double-click .\intro.dsn**.
2. **Double-click on Schematic**.
3. **Double-click PAGE1**.

### Selecting Objects

1. Click on a part and notice the dashed outline around the part.
2. Click to select a wire and notice that the wire segment highlights and selection boxes appear at the endpoints.
3. Zoom in and select any text string (for example, a net name or reference designator).
4. Notice that the text string highlights and selection boxes appear around it.
5. Click in an open area to clear all selected objects.

You can also press the Esc key.

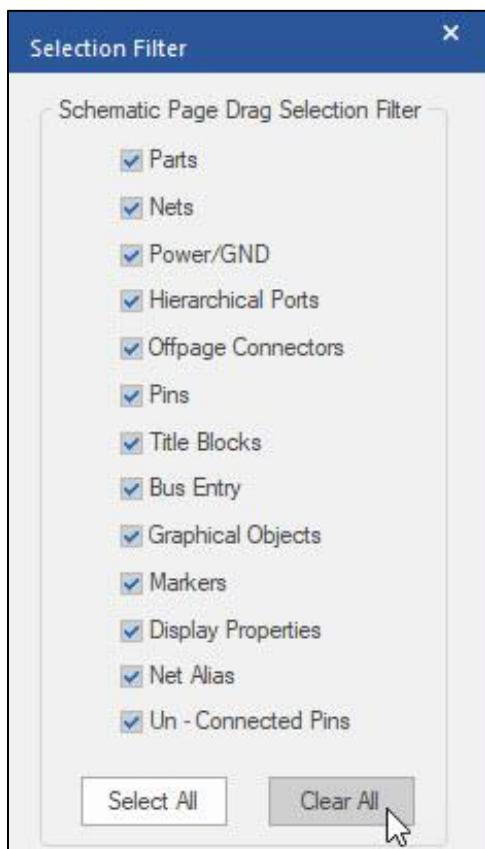
### Selecting Multiple Objects

1. Click on capacitor **C1**. Press the **Ctrl** key and click on capacitor **C2**.  
Both caps are now selected.

2. Press **Ctrl** and click on capacitor **C2** again.  
Capacitor **C2** is removed from the selected set.
3. Click in an open area to deselect all objects on the page.
4. Drag a rectangle around capacitors **C1** and **C2** (including the power and ground symbols and wires).  
All parts, wires, and text in the rectangle are selected.
5. Press **Esc** to unselect all objects.

## Using the Selection Filter

1. Place your cursor on the schematic page, **right-click** and choose **Selection Filter**.



2. In the Selection Filter, select **Clear All**.
3. Select the **Nets** checkbox and click **OK**.

4. Drag a box around everything on the page and notice that only the wires are selected.
5. Click in an open area to deselect all objects on the page.
6. Open the Selection Filter, click **Select All**, and **OK**.



## Lab 2-4 Editing Objects

**Objective:** To move, delete, and copy objects.

---

### Moving Individual Parts and Wires

1. Place your cursor on a part, press and hold the left mouse button, and drag the part to a new location.

Notice that the attached wires stretch with the part.

2. Place your cursor on a wire, press and hold the left mouse button, and drag the wire segment to a new location.

Notice that the wire segment remains connected.

3. Use the **Undo** toolbar icon to return the parts to their original locations.

4. Hold the **Alt** key and drag **C2** to the right.

The part is disconnected from the wires.

5. Undo the previous step.

### Moving a Group

1. Drag a rectangle around capacitors **C1** and **C2** (including the power/ground symbols and wires).

2. Place your cursor on a part or wire and notice that the cursor changes to a crosshair.

3. Press and hold the left mouse button when the cursor changes into a crosshair shape and drag the selected group to a new location.

4. Press **Esc** to clear the selected set.

### Using Delete and Undo

1. Click to select a part, then **right-click** and choose **Delete**.

2. Press **Ctrl+Z** to undo the deletion.

3. Click to reselect the part, and press **Delete** or **Backspace**.
4. Click the **Undo** icon in the main toolbar.
5. Click capacitor **C1**. Hold the **Ctrl** key down and click capacitor **C2**.  
Both caps are selected.
6. Press the **Backspace** or **Delete** key to delete both capacitors at once.
7. Undo the deletion.
8. Drag a rectangle across **C1**. Then **Ctrl+Left** drag across **C2** and the rest of the circuit (including the power/ground symbols and wires) to add to the selected set.
9. Delete the selected parts and wires, then undo the deletion.
10. Select and delete **C1**, then select and delete **C2**.
11. Try to undo both deletions.  
Capture has unlimited undo capability.

## Copying Parts

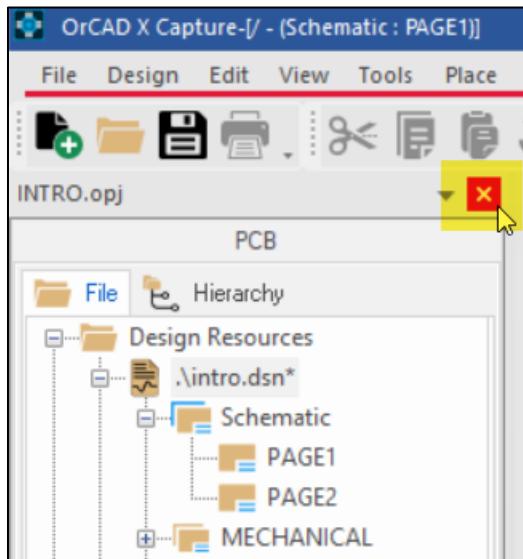
1. Press and hold the **Ctrl** key, and the left mouse will drag on a part to create a copy of the part.
2. Press **Ctrl+Z** to undo the copy.
3. Click on a part.
  - a. Press **Ctrl+C** to copy and **Ctrl+V** and click to paste a copy of the part.
  - b. Press **Ctrl+Z** to undo the copy.
4. Drag a rectangle around the capacitors (including the power/ground symbols and wires).
  - a. Press **Ctrl+C** to copy the group.
  - b. Press **Ctrl+V** and click to place a copy of the group.
  - c. Press **Ctrl+Z** to undo the group copy.

## Closing the Schematic

1. Close the schematic window and click **No** to Discard all changes to the page.

## Closing the Project

1. Close the project tab and click **No** to continue.



The Capture session window is still running.



## Lab 2-5 Using the Help System (Optional)

**Objective:** To access and use online Help, online tutorials, and online manuals and product notes.

---

### Accessing Online Help

1. In the Capture session window, choose **Help – What's New**.  
The Doc Assistant window opens.
2. Scroll through the list of new features and improvements.
3. Close the Cadence Help window.



# **Module 3: Setting Up Your Environment**

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## Lab 3-1 Setting Up Preferences

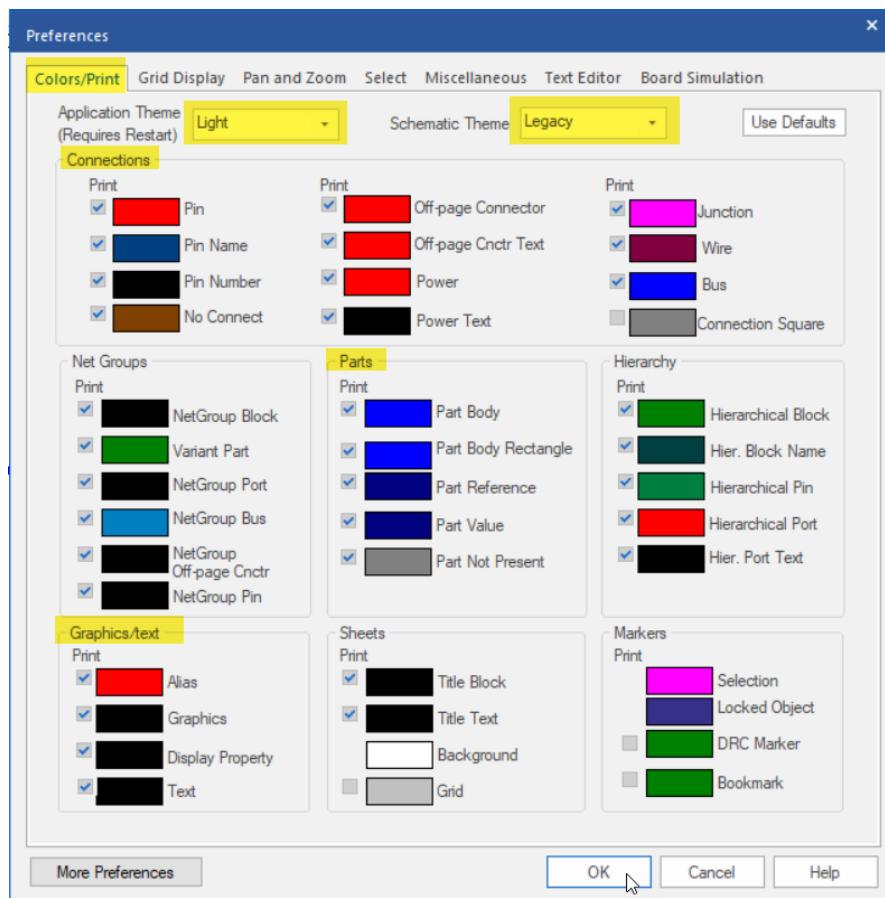
**Objective:** To set user-level preferences.

### Opening the Intro Project

1. In the Capture session window, choose **File – Open – Project** and select the *C:\User1\Capture\intro\intro.opj* file.

### Assigning Colors

1. In the Project Manager window, open **PAGE1**.
2. Enlarge the schematic window and zoom in on capacitors **C1** and **C2**.
3. Notice the current color settings.
4. Choose **Options – Preferences**.



## Setting Up Your Environment

5. In the Parts section, click the color box next to Part Body. Click a different color from the color palette and click **OK**.
6. Change the color assignments for Part Reference and Part Value.
7. In the Connections section, change the color for Wire.
8. Click **OK** in the Preferences window.

The color assignments take effect immediately. These preferences are stored locally on your system (any design opened on your system will use these color settings).

9. If your grid is not visible, use the **View – Grid** command to turn it on.
10. Try several more color assignments to help you learn what types of objects are in a schematic (optional).  
For example, in the Connections section, experiment with colors for Pin, Junction, Power, Power Text, and Off-page Connector.  
In the Graphics/text section, change the color for Alias. In the Sheets section, change the colors for the Title Block, Background, and Grid.

## Restoring Default Colors

1. Choose **Options – Preferences**.
2. Click the **Use Defaults** button in the upper-right corner of the **Colors/Print** tab.  
The form now displays the original color assignments.
3. Click **OK**.

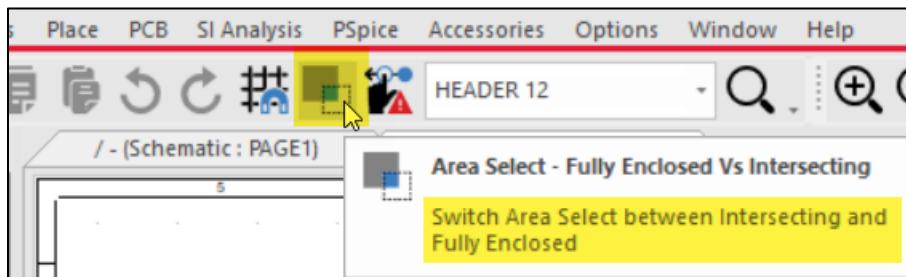
## Controlling Area Selection

1. Return to the Project Manager window and open PAGE2 of the design.
2. Zoom in to U2A (74LS00).
3. Choose **Options – Preferences** and choose the **Select** tab.
4. Change the Area Select setting to Fully Enclosed in the **Schematic Page Editor** section and click **OK**.

5. Drag a selection rectangle across (but do not fully enclose) U2A.  
Notice that the part is not selected.
6. Drag a larger selection rectangle and fully enclose U2A (including pin stubs).  
Notice that the part is now selected.
7. Click left in an open area to deselect all objects.
8. Choose **Options – Preferences** and click the **Select** tab.
9. Change the Area Select setting back to **Intersecting** and click **OK**.

10. Drag a rectangle across a portion of U2A to select it.

**Note:** You can use the Area Select icon to toggle between the two settings.

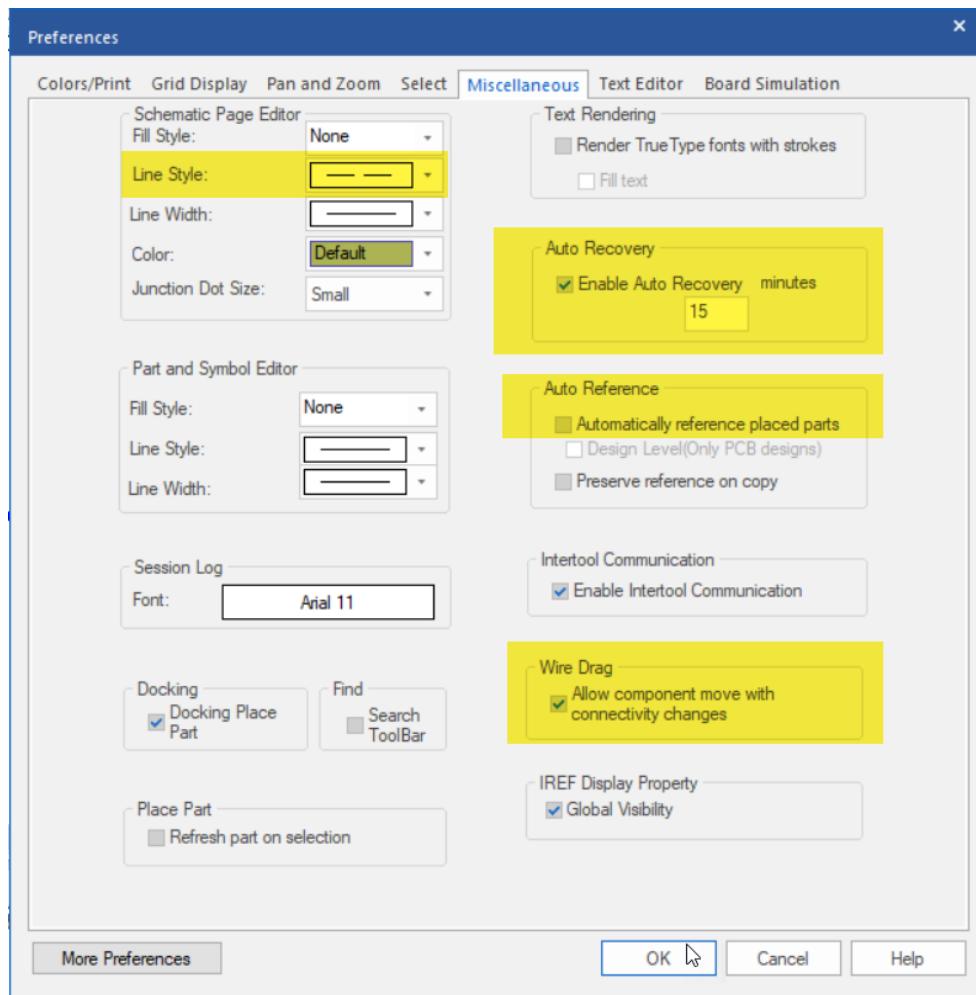


## Setting Miscellaneous Preferences

1. Choose **Options – Preferences**.
2. Click the **Miscellaneous** tab and set the following:
  - In the Schematic Page Editor section, set **Line Style** to dashed.
  - Set Auto Recovery to **On** every **15** minutes.
  - Deselect **Automatically reference placed parts**.
  - Make sure the **Wire Drag** option is selected.

## Setting Up Your Environment

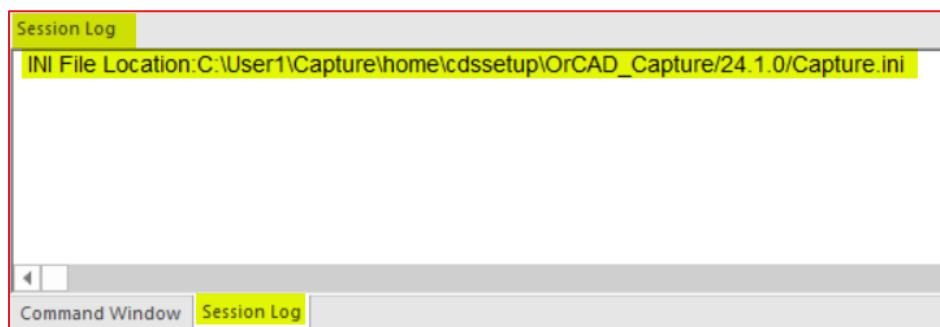
3. Your settings should match the following example.



4. Click **OK** to close the Preferences window.

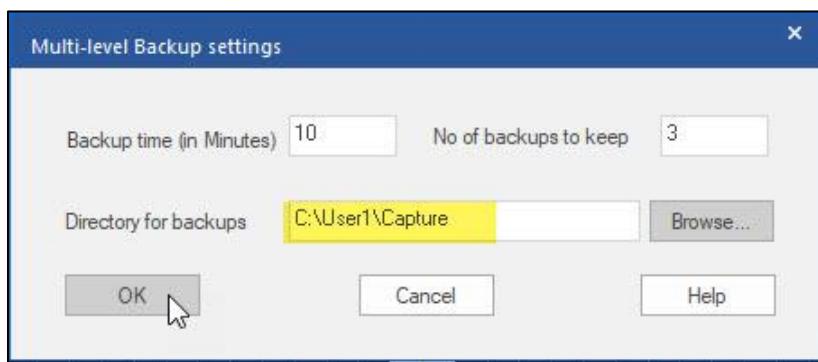
These user preferences are saved in the `$HOME/cdssetup/OrCAD_Capture/24.1.0/Capture.ini` file and are immediately applied to your current design and any other designs you open (even designs created by others).

**Note:** When you start OrCAD® X Capture, the path to the `Capture.ini` file is shown in the Session Log window.



## Setting Auto Backup Preferences

1. Choose **Options – Autobackup**.
2. To set the Directory for backups field, click **Browse**.
3. Navigate to the *C:\User1\Capture* directory and click **Select Folder**.
4. Enter the time interval you wish backup to occur and the number of backups you want to maintain.



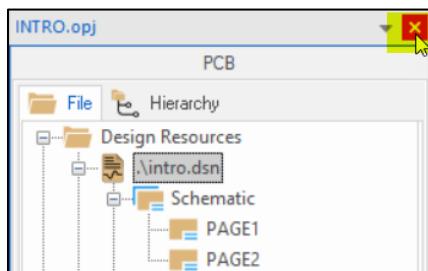
5. Click **OK**.

## Closing All Schematic Pages

1. Right-click on any of the schematic page tabs and choose **Close All Tabs**.  
Both pages are closed.

## Closing the Project

1. Click on the **intro** tab to close the project.



The Project Manager window closes, but the Capture session window is still running.

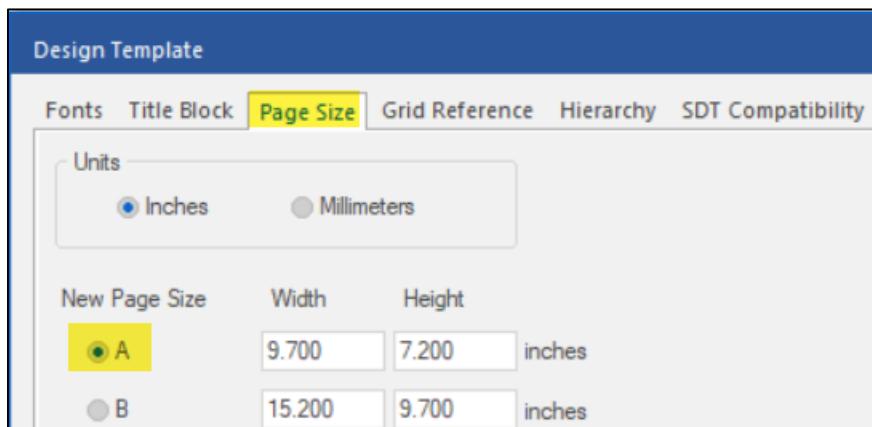


## Lab 3-2 Setting Up the Design Template

**Objective:** To set design-level parameters used for all new designs.

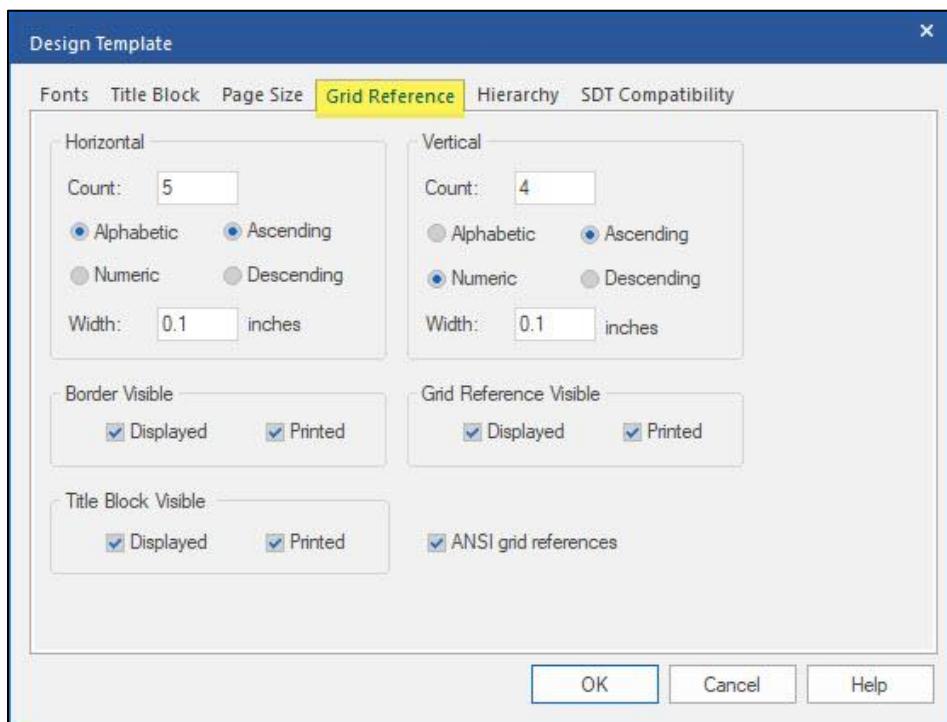
### Accessing Design Template Settings

1. Choose **Options – Design Template**.
2. Select the **Page Size** tab and make sure the **Page Size** is set to A.



3. Choose the **Grid Reference** tab.

Make sure that the settings match this graphic.



## Filling in the Title Block Information

1. Click the **Title Block** tab.

2. In the **Title** field, enter:

Project1

## Adding a Name and Address

1. In the Organization Name field, enter your company name.

2. In the Organization Address1 field, enter your company street address.

3. In the Organization Address2 field, enter the city, state, and zip code.

4. Use the Address 3 and 4 fields *only* if necessary.

## Adding a Document Number, Revision, and CAGE Code

1. In the Document Number field, enter:

CDS-12345

2. In the Revision field, enter:

A

3. Add a CAGE Code of **US98765**.

## Adding the Title Block

1. Click the browser button to the right of the Library Name field and navigate to the *C:\User1\Capture\training\_libs* folder.

**Important:** This path will vary depending on where the course database is installed.  
Remember to replace the *C:\User1* portion with the actual path to your *Capture* directory.

2. Click **CLASS\_LIB.OLB** and click **Open**.

3. In the Title Block Name field, enter:

TitleBlock0

4. Click **OK**.

These design template settings are saved in the `$HOME/cdssetup/OrCAD_Capture/24.1.0/Capture.ini` file but won't be applied until you create a new design.

The design template settings are retained in a design even when it is transferred. Changes to your design template settings will not affect existing designs.



## **Module 4: Working with Libraries**

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## Lab 4-1 Opening and Viewing an Existing Library

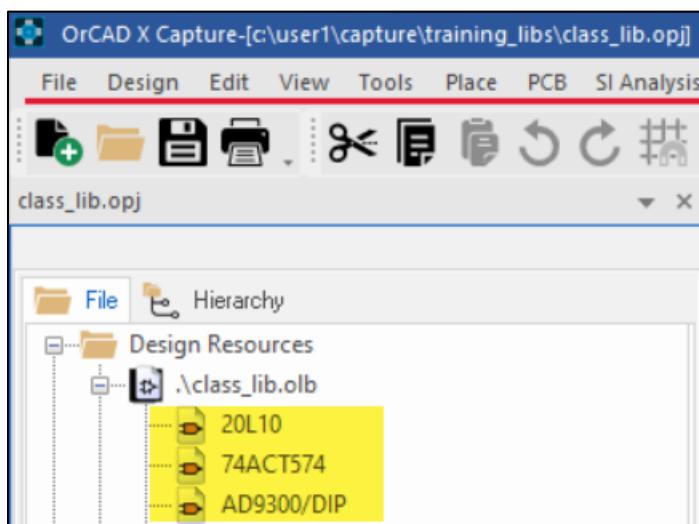
**Objective:** To open a library and view existing parts.

---

### Opening the CLASS\_LIB Library

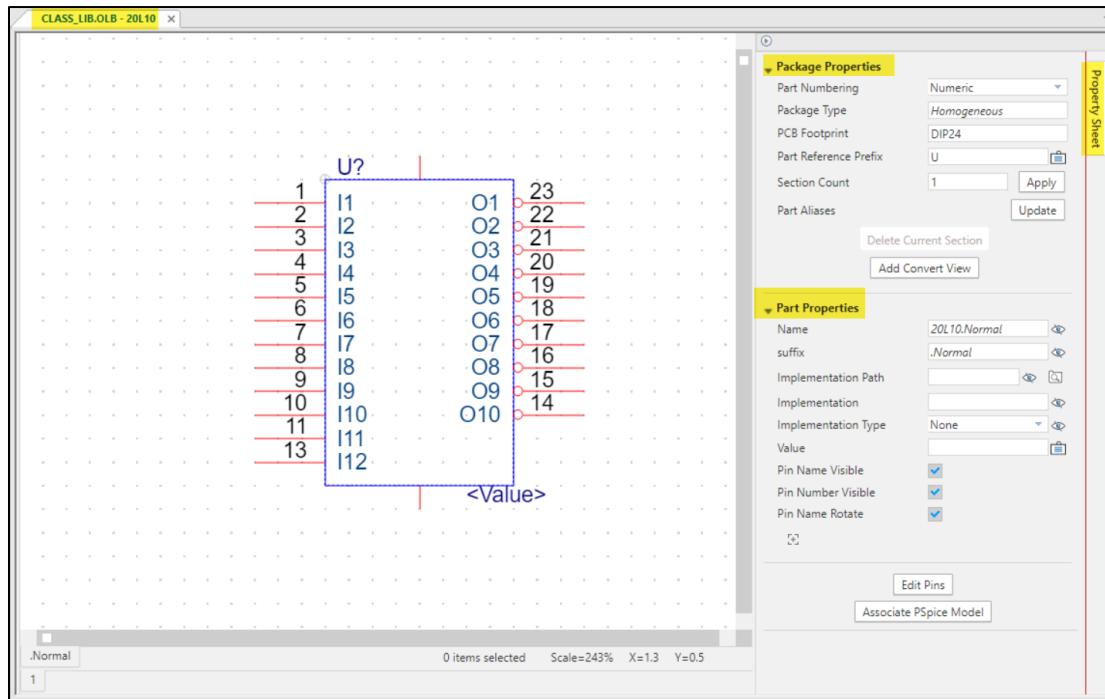
1. In the Capture session window, choose **File – Open – Library** and navigate to the *C:\User1\Capture\training\_libs* folder.  
**Important:** The *C:\User1* portion of the path is variable. Always replace the beginning part of this path with the actual path to the *Capture* folder on your system.
2. Select **CLASS\_LIB.OLB** and click **Open**.

The Project Manager lists the parts in the library.

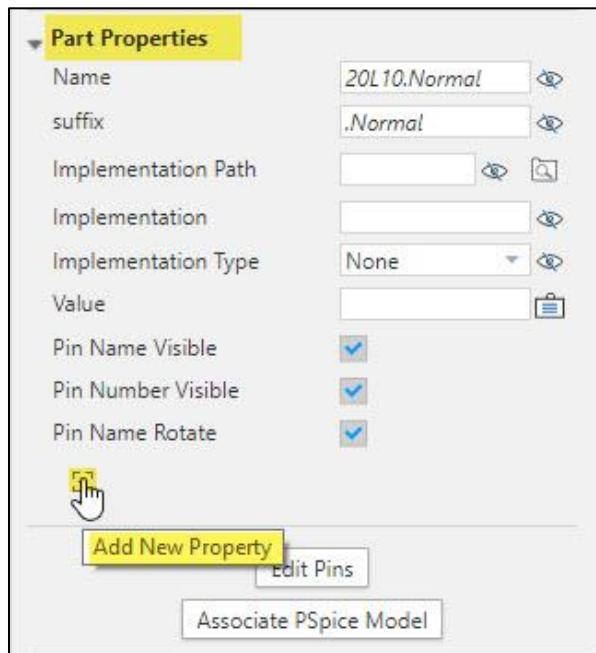


## Viewing a Part

- Under the Project Manager, double-click on **20L10** to open the part in the Part Editor.

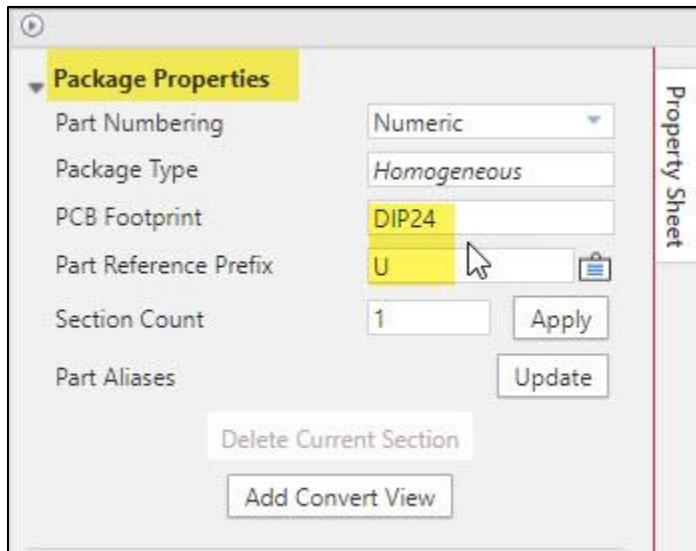


- In the Property Sheet in the right pane, locate the Part Properties section. Notice that you can control pin name visibility and add new properties to the part.



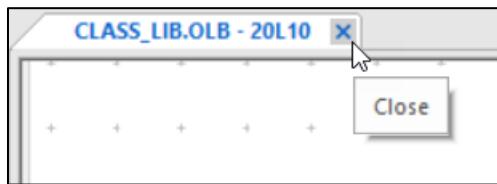
Do not make any changes. You will create library parts in the next lesson.

3. Locate the Package Properties section of the Property Sheet and notice you can assign a reference designator prefix and PCB Footprint to the part.



4. Choose **File – Close** to close the 20L10 part without saving.

**Note:** You can also use the window tab to close the part.



## Closing the Library

1. Click in the Project Manager window and choose **File – Close** to close the library.

The Capture session window is still running.

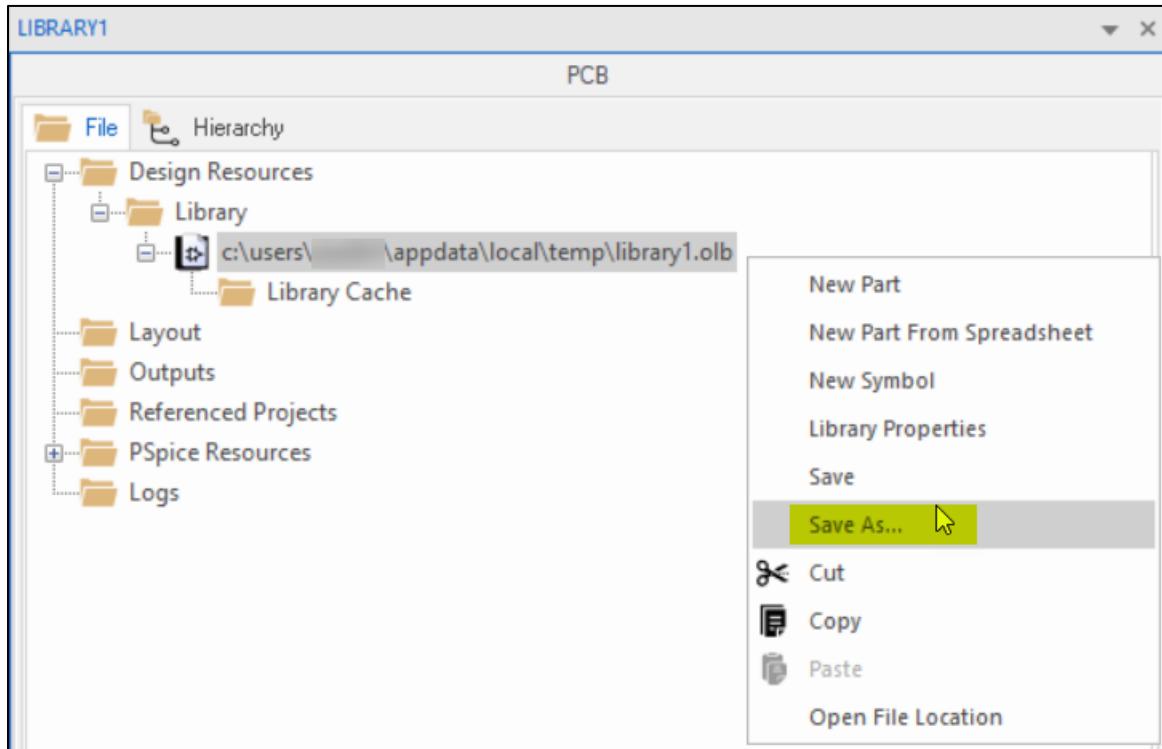


## Lab 4-2 Creating a New PRACTICE\_LIB Library

**Objective:** To create a library and rename the library.

1. In the Capture session window, choose **File – New – Library**.

The Project Manager window opens, and a new library file is listed under the Design Resources folder. By default, the new library name is *libraryn.olv*, where the letter *n* is the number 1 or greater.



The default location and name of your new library may differ.

### Renaming the Library

1. To change the name and location of the new library, right-click on the library *libraryn.olv* and choose **Save As**.
2. Navigate to the *C:\User1\Capture\training\_libs* folder and save the library as *practice.lib.olv*.

The new location and library name are shown in the Project Manager window.

3. Choose **File – Close** to close the new library.

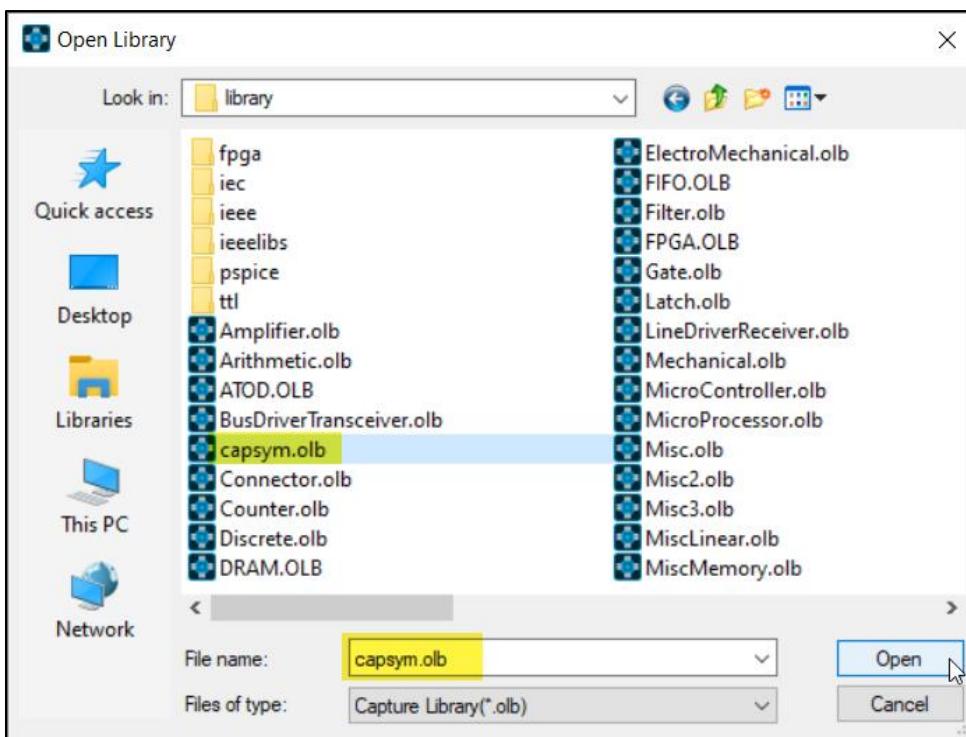


## Lab 4-3 Copying and Renaming Parts and Symbols

**Objective:** To copy parts from one library to another.

### Opening a Cadence-Supplied Library

1. Choose **File – Open – Library**.
2. Navigate to the `$CDSROOT\tools\capture\library` folder (where `$CDSROOT` represents the path to your Cadence software installation – for example, `C:\Cadence\SPB_24.1`). See the instructor for help.



3. Click on **capsym.olb** and click **Open**.

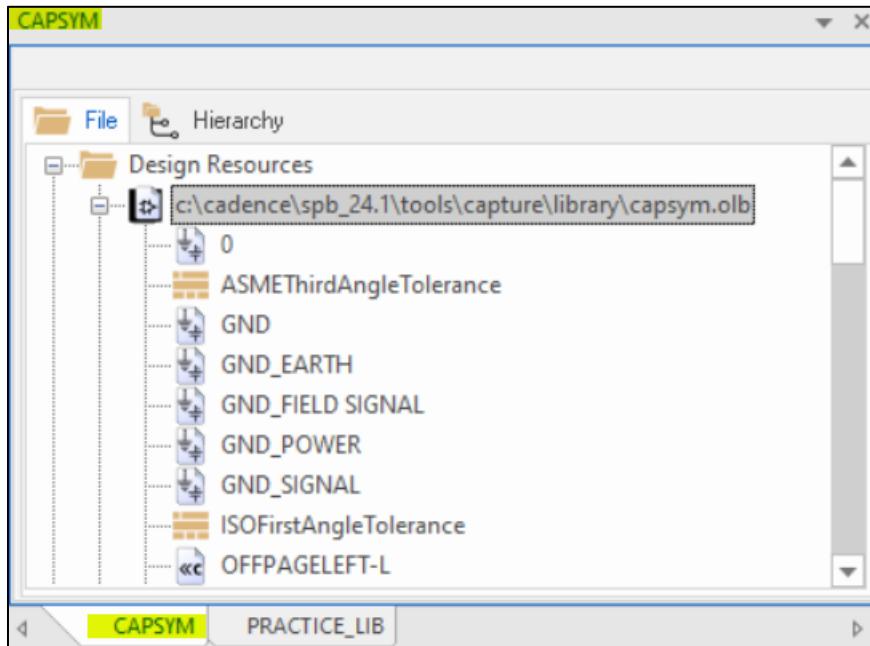
The *CAPSYM* library opens in the Project Manager. This is a standard library containing voltage symbols, title block symbols, off-page connector symbols, and more.

You will copy parts from this Cadence-supplied library and paste them into your *PRACTICE\_LIB* library.

**Note:** Under the Warning pop-up box, click **Yes** to open in **READONLY** mode

## Opening Your PRACTICE\_LIB Library

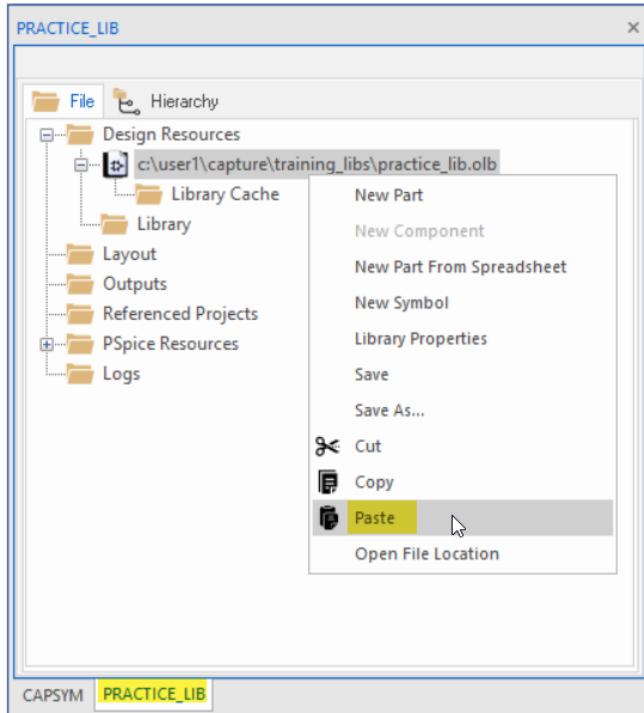
1. Choose **File – Open – Library**, navigate to the *C:\User1\Capture\training\_libs* folder and select the **PRACTICE\_LIB.OLB** file.  
You now have two libraries open.
2. Click the tabs along the bottom of the Project Manager window to switch between libraries.



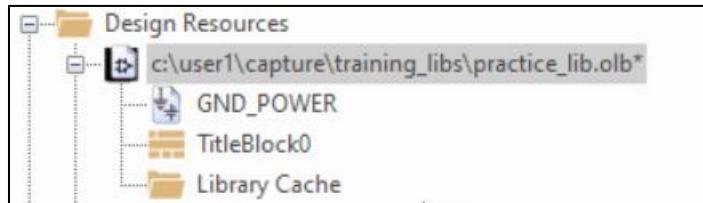
## Copying Between Libraries

1. In the *CAPSYM* library, select the **GND\_POWER**.
2. Choose **Edit – Copy** (or **Ctrl+C**).

3. Click the **PRACTICE\_LIB** tab, right-click on **practice\_lib.olb**, and choose **Paste** (or **Ctrl+V**).



4. Repeat the process to copy the **TITLEBLOCK0** symbol from the CAPSYM library to the PRACTICE\_LIB library.



5. Choose **File – Save** to save the PRACTICE\_LIB library.

### Closing the CAPSYM Library

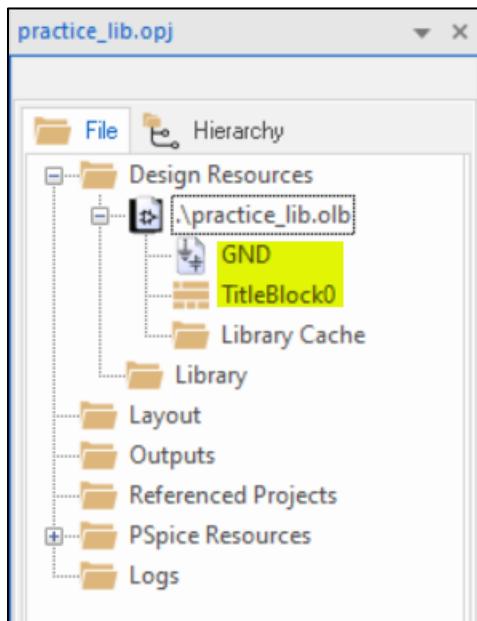
1. Click the **CAPSYM** library tab and choose **File – Close**.

### **Renaming the GND\_POWER Symbol**

1. In the **PRACTICE\_LIB** library, right-click on the **GND\_POWER** symbol and choose **Rename**.
2. Change the Name to **GND** and click **OK**.



3. In the Project Manager, select the **practice\_lib.olb** file and choose **File – Save** to save the library and **Yes** to continue.



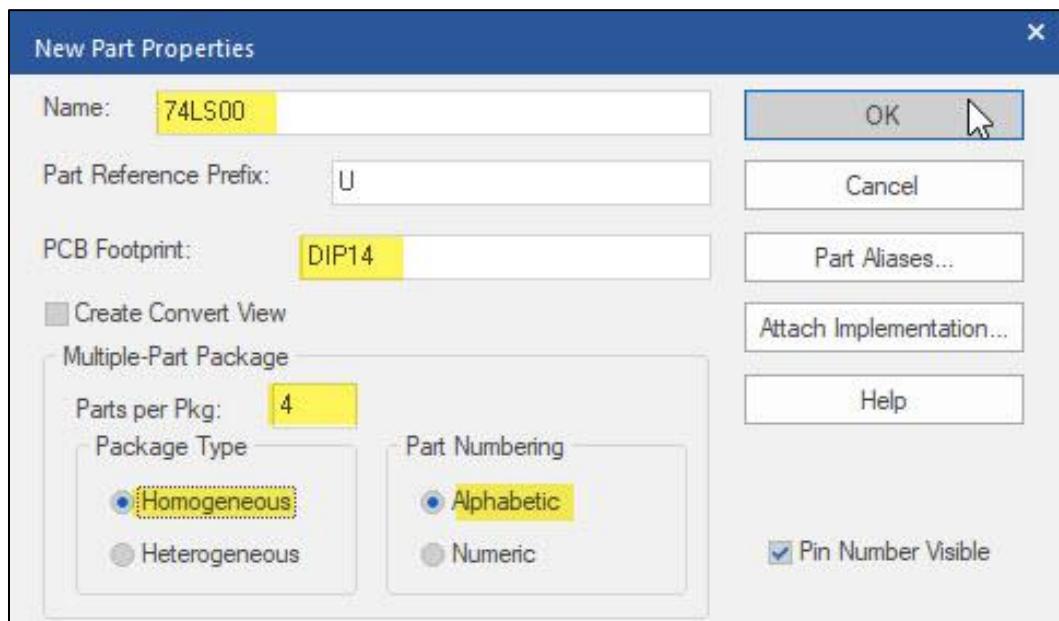
End of Lab

## Lab 4-4 Creating a Homogeneous Part

**Objective:** To create a gate-level symbol that fits multiple times into a physical part.

### Adding a New Part to the Library

1. In the Project Manager, select **practice\_lib.olb**.
2. Right-click and select **New Part**.  
The New Part Properties dialog box appears.
3. Complete the form as shown below.



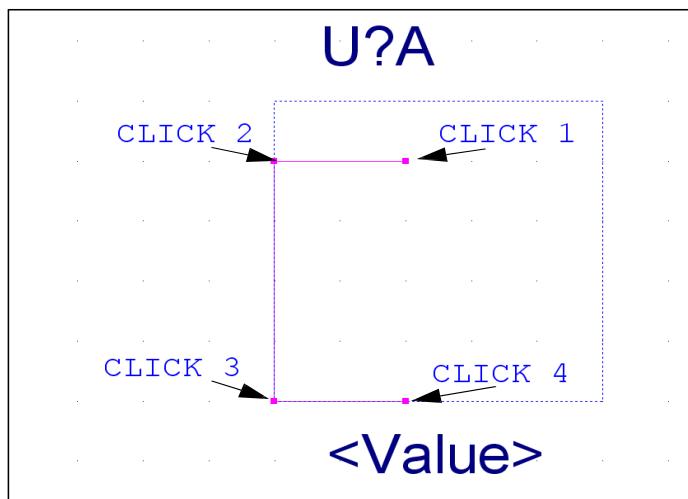
Be sure to set the Parts per Pkg field to **4**.

4. Click **OK**.

## Creating the Part Graphics

The Part Editor automatically displays a part boundary box with five grid spaces square. All part graphics must fit within the dotted boundary.

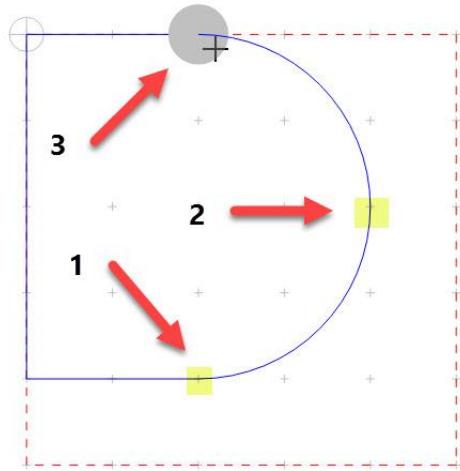
1. Maximize the Part Editor window.
2. Choose **View – Zoom – All** or click the **Zoom to all** icon.
3. Choose **Place – Polyline** (or click the **Place polyline** icon on the Draw Graphical toolbar) and add lines, as shown below.



4. Right-click and select **End Mode**.
5. Press **Esc** to deselect the polyline.  
You can also click in an open area to deselect all objects.
6. Choose **Place – Arc** or click the icon on the Draw toolbar.
7. Examine the “dots” on the screen. Your first click needs to be on the end of the lowest line segment and will be the “starting point” of an imaginary circle.
8. Click a second time to indicate the midpoint the arc must pass through.



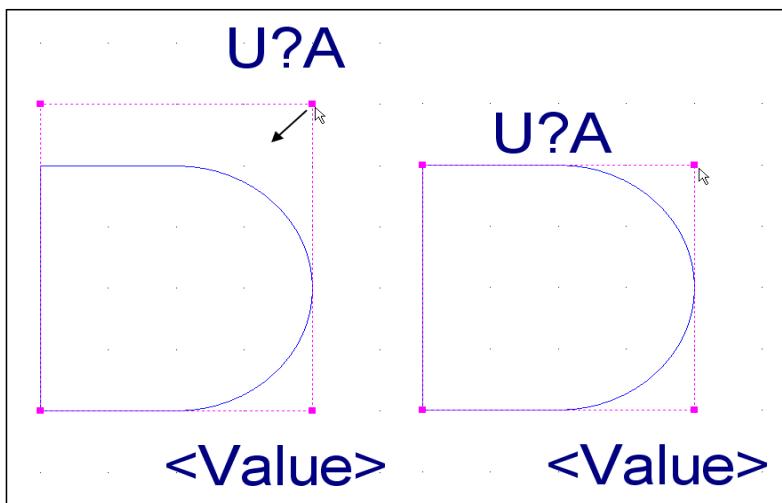
9. Click a third time to indicate the endpoint of the arc. Then **right-click** and choose **End Mode**.



### Resizing the Bounding Box

The part bounding box must touch the edges of the part graphics. This ensures that when you attach pins to the bounding box, they contact the polygon.

1. Select the bounding box and drag the handles (the small boxes in each corner of the bounding box) to reduce its size, as shown below.



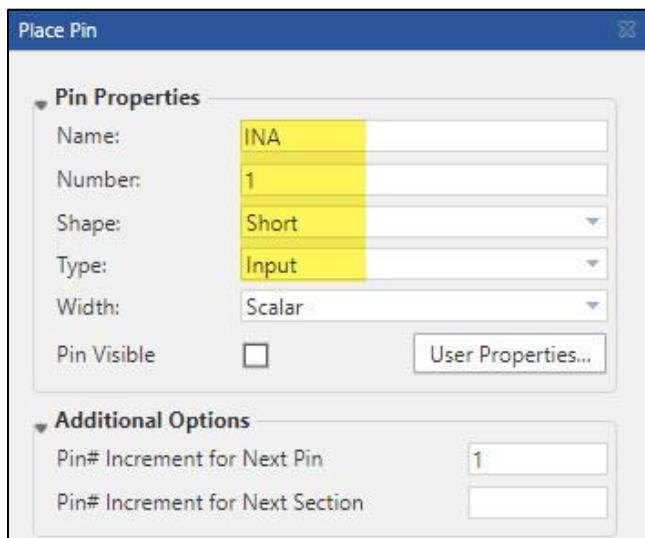
2. Press **Esc** to deselect the bounding box.
3. Choose **File – Save**.

## Adding Pins

1. Click the **Place Pin** icon or choose **Place – Pin**.



2. Enter the information as shown below.

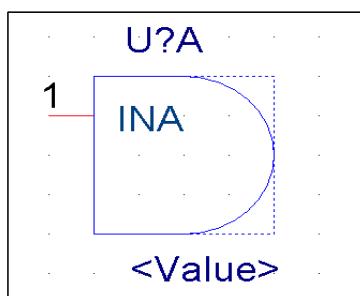


3. Click **OK**.

The pin image attaches to the boundary box. As you move your cursor, the pin snaps to 100 mil grid points along the boundary edges.

**Important:** Do not double-click when adding a pin because this places two pins at the same location.

4. Position it as shown below and click to place it.

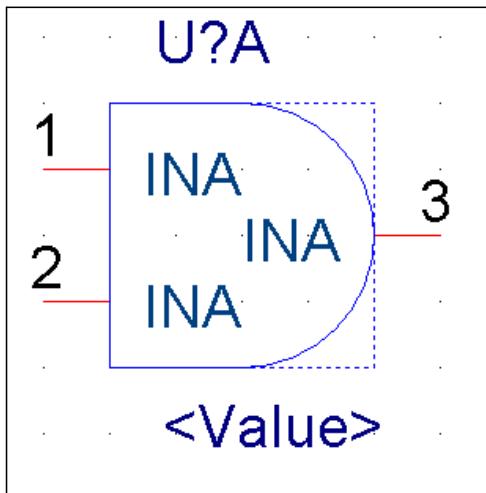


5. Move the cursor and notice that a second pin is now attached and ready for placement.

6. Click to add a second pin, two grids below the first pin.

Notice that the pin number is automatically incremented. You can change the pin name later.

7. Place the third pin on the right side, as shown below.



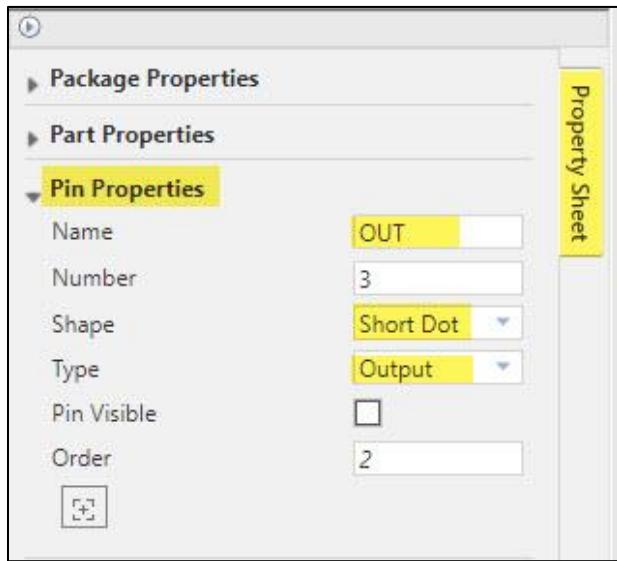
8. Press **Esc** to end the command.

## Modifying Pin Properties

1. Click **pin 2** and locate the Pin Properties section in the right pane.
2. Change the Name field to **INB** and press the **Tab** key.  
The pin name on the part becomes INB.
3. Click on **pin 3**.

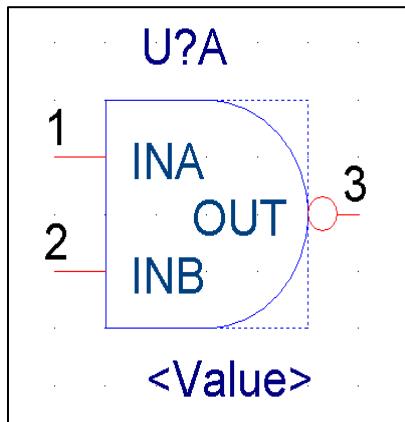
## Working with Libraries

4. Change the Name to **OUT**, toggle the Shape field to **Short Dot**, and toggle the Type field to **Output**.



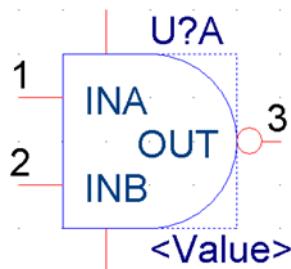
5. Press **Esc** to deselect all pins.

Your part now resembles this one.

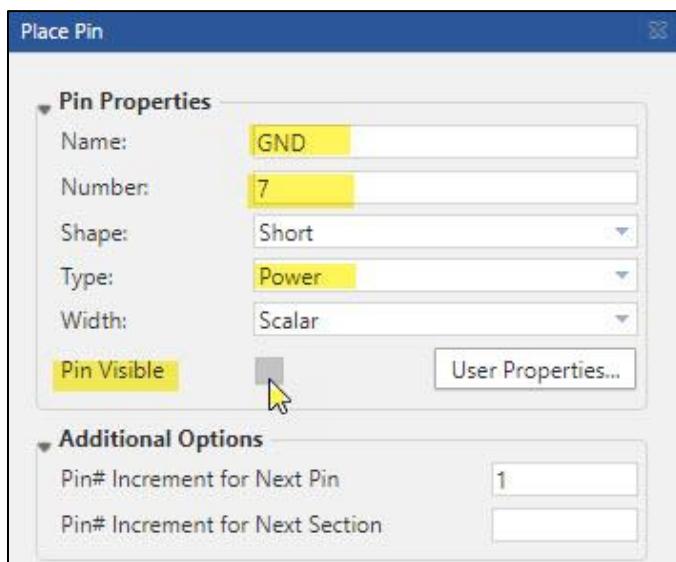


## Adding Power Pins

In this section, you add two power pins, as shown below.



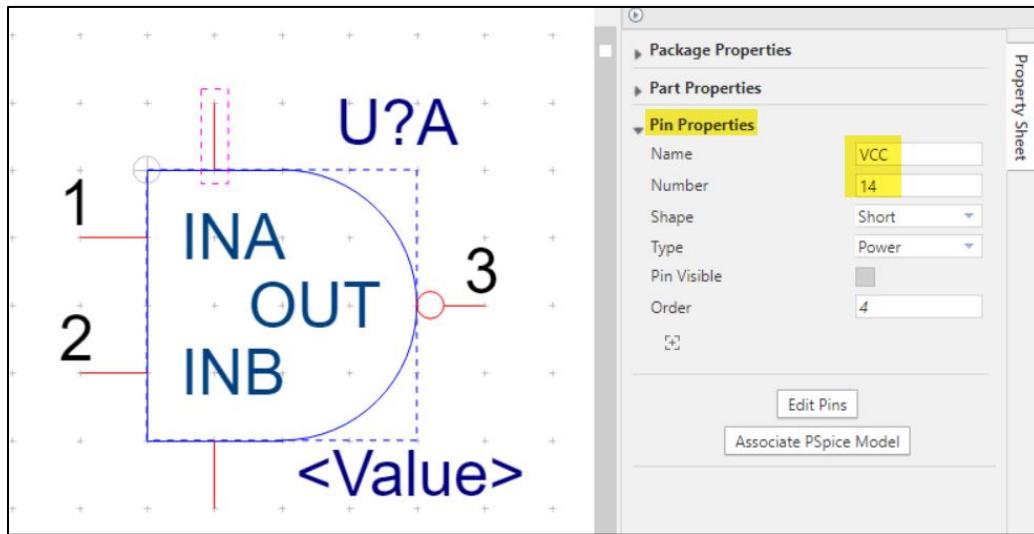
1. Select and drag the part reference *U?A* and *<Value>* to make room for the power pins, as shown above.
2. Click the **Place Pin** icon. Enter the values shown below.



3. Make sure the **Pin Visible** checkbox is *not* selected.  
For this part, you don't want the power pins visible when the part is placed in the design.
4. Click **OK**.
5. Place the **GND** pin at the bottom of the graphic.
6. Remain in pin placement mode and place another power pin at the top of the graphic.
7. Press **Esc**.

Working with Libraries

- Click the power pin you placed at the top of the graphic, change the name to **VCC** and change the pin number to **14**.

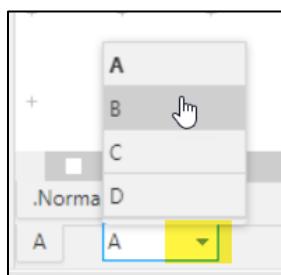


- Choose **File – Save**.

### Assigning Pin Numbers to All Gates in the Package

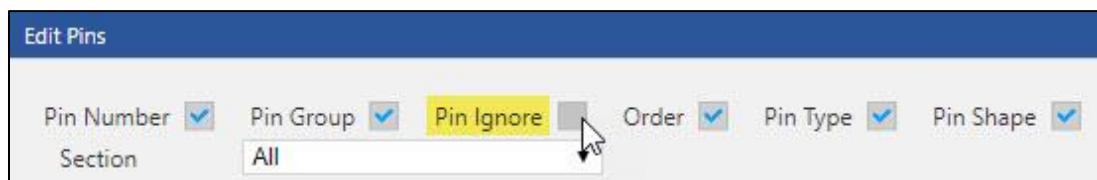
This is a homogeneous part with 4 parts per package. The symbol graphics represent one of four identical sections.

- In the lower-left corner of the work area, click to toggle the field to B, C, and D to view the other gates in the package. Notice that you still need to assign unique pin numbers for the other three gates.



- In the right corner of the work area, click on the **Property Sheet** tab and click **Edit Pins**.

- In the Edit Pins window, turn off the checkbox for Pin Ignore.



This hides the Pin Ignore columns.

- Enter the pin numbers for sections B, C, and D, as shown below.

Normal View: Pin Name	Section: A Pin Number	Section: B Pin Number	Section: C Pin Number	Section: D Pin Number	Order	Pin Group	Normal V Pin Shape
INA	1	4	9	12	0		Short
INB	2	5	10	13	1		Short
OUT	3	6	8	11	2		Short Dot
GND	7	7	7	7	3		Short
VCC	14	14	14	14	4		Short

- Click **Apply**.

## Setting Up Pin Swapping

You can add pin swap properties if you want to perform pin swapping in Allegro® X PCB Editor.

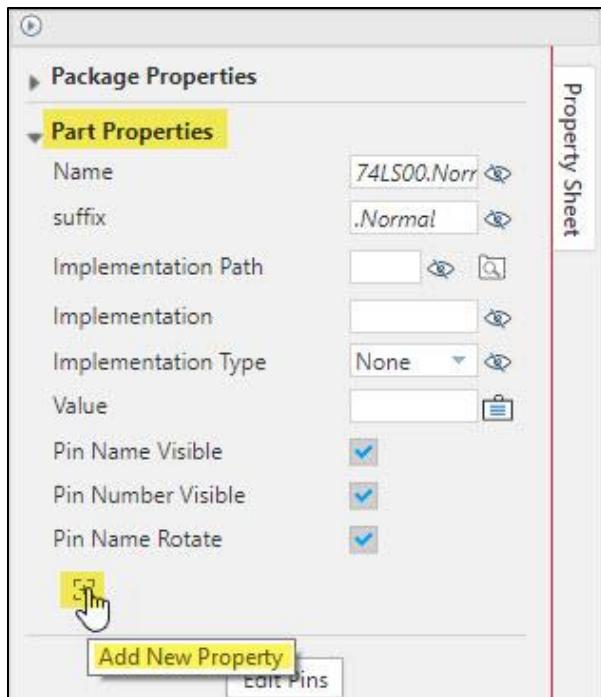
- In the Edit Pins window, locate the **Pin Group** column.
- For the input pins (INA and INB), assign the number **1**, as shown below.

Normal View: Pin Name	Section: A Pin Num...	Section: B Pin Num...	Section: C Pin Num...	Section: D Pin Num...	Order	Pin Group	Normal View Pin Shape
INA	1	4	9	12	0	1	Short
INB	2	5	10	13	1	1	Short
OUT	3	6	8	11	2		Short Dot
GND	7	7	7	7	3		Short
VCC	14	14	14	14	4		Short

3. Click **OK**.
4. Choose **File – Save**. Click Yes to All to save the changes.

## Adding a User Property

1. In the Part Properties section of the **Property Sheet** tab, click on the **Add New Property** widget.



2. Toggle the property name to **PART\_NUMBER** and enter the part number, as shown below.

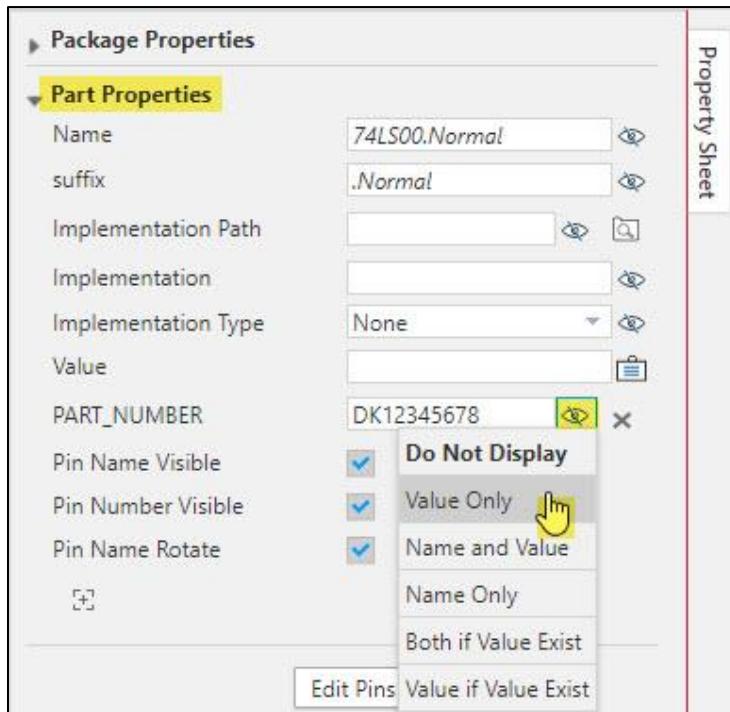


3. Click the **Add Property** icon to the right.

The PART\_NUMBER property is added to the Part Properties section of the Property Sheet.

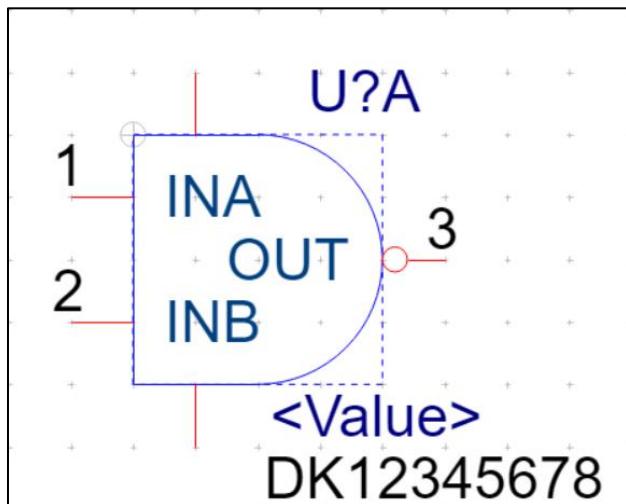
## Controlling Display of Properties

1. In the Part Properties section, right-click to toggle the visibility setting for the PART\_NUMBER property to **Value Only**.



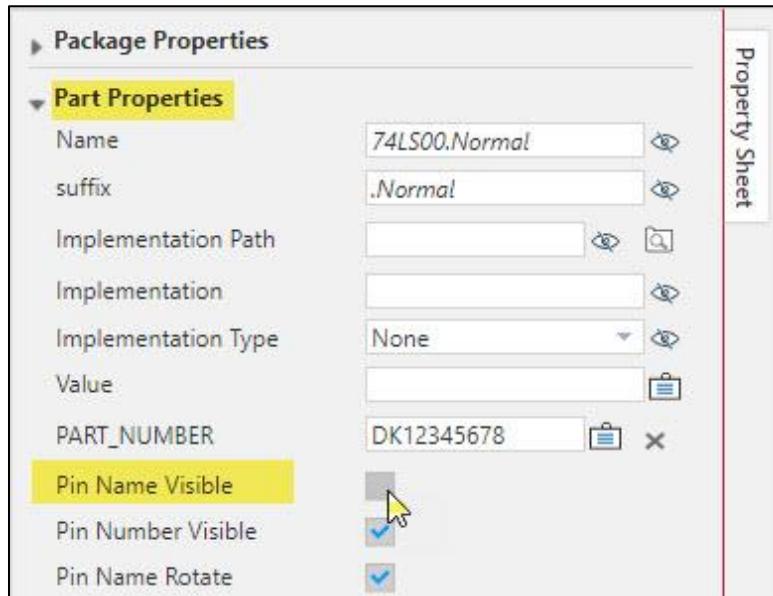
The part number is now visible on the part.

2. Drag to position the part number text and save the part.



## Controlling Display of Pin Names

1. In the Part Properties section, turn off the checkbox for **Pin Name Visible**.



2. Notice that the logical pin names **INA**, **INB**, and **OUT** are no longer visible on the part.
3. Choose **File – Save**. Click **Yes to All** to save the changes.

## Closing the Part

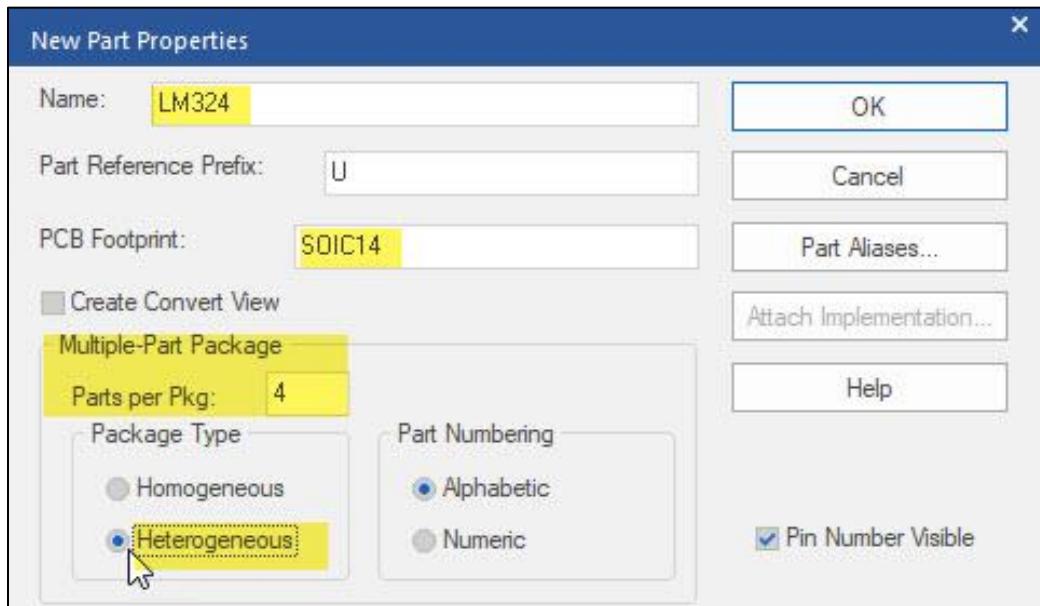
1. Choose **File – Close**.



## Lab 4-5 Creating a Heterogeneous Part

**Objective:** To create a part composed of dissimilar gates.

1. In the Project Manager, right-click on the **practice\_lib.olb** and select **New Part**.
2. Enter the information shown below.



**Important:** Be sure to select the **Heterogeneous** option.

3. Click **OK**.

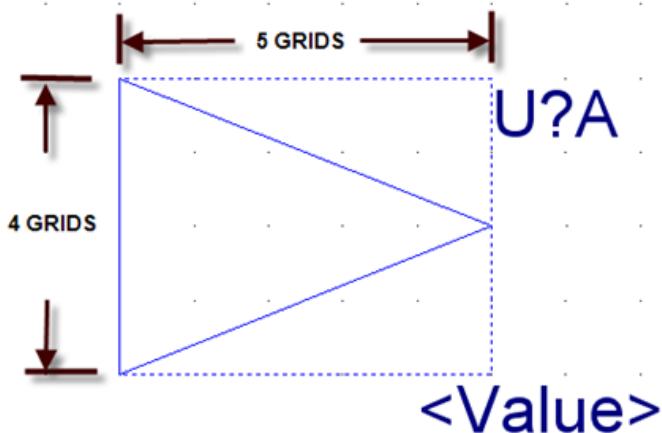
### Creating the Symbol for the First Gate

1. Maximize your window and click the **Zoom to all** toolbar icon.
2. Choose **Place – Polyline**. 

## Working with Libraries

3. Draw a triangle using the 4 x 5 grid shown in the example below.

**Hold the Shift key down** to add the diagonal segments.



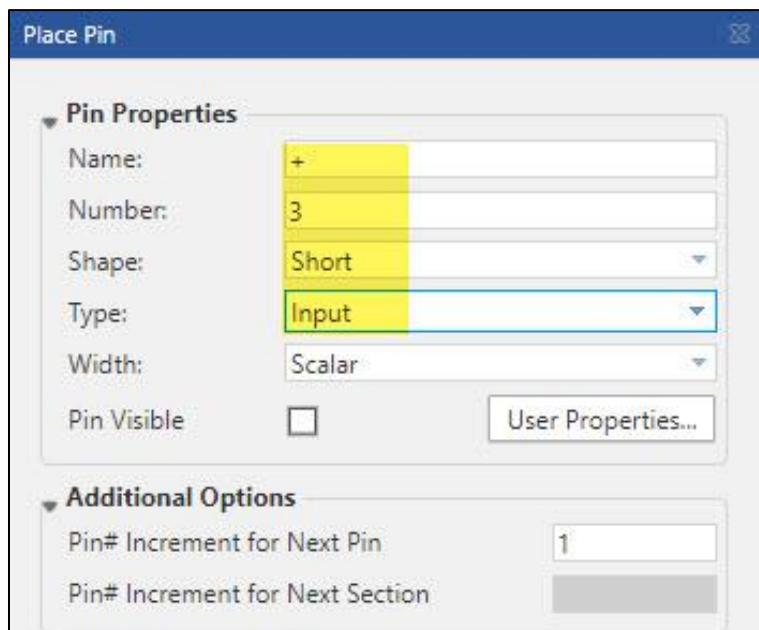
4. Resize the bounding box to fit the symbol polygon.

### Adding Pins

1. Click the **Place Pin** icon.

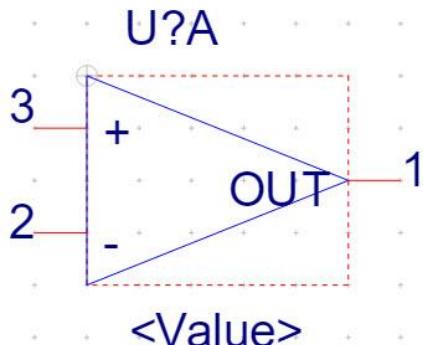


2. Enter the information as shown and click **OK**.



The pin attaches to the edge of the bounding box.

3. Click to add the first pin, as shown below.



4. Press the **ESC** key to end the command.
5. Add two more pins, as shown above, with the following settings.

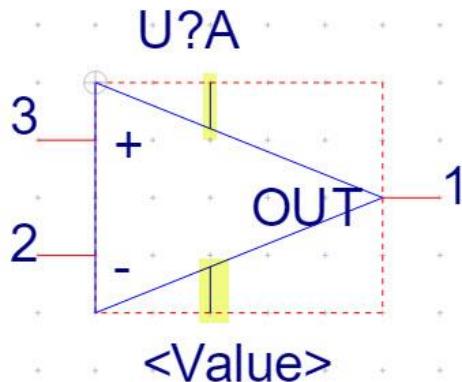
Next pin:  
Name ( - )  
Number ( 2 )  
Type( Input)

Next pin:  
Name ( OUT )  
Number ( 1 )  
Type ( Output )

6. Click on the **Snap To grid** icon to toggle the snap grid OFF.



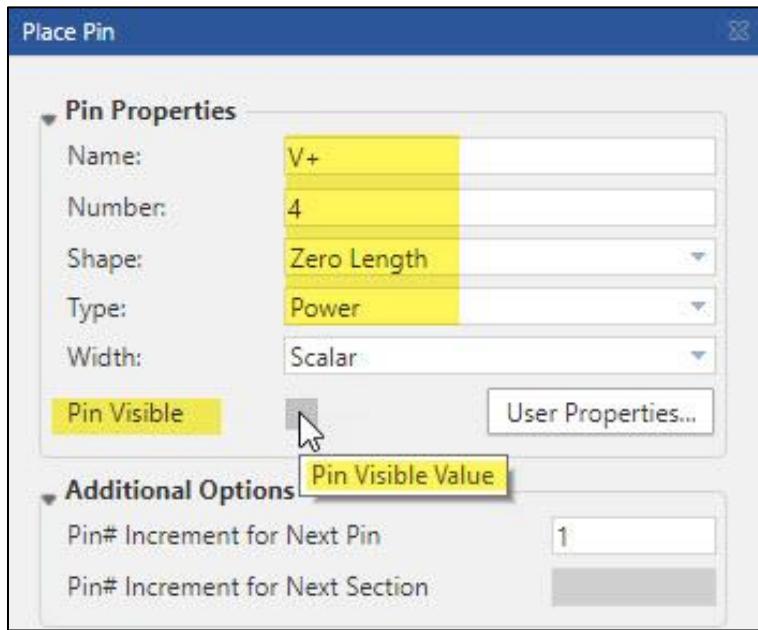
7. Choose **Place – Line**.
8. Draw two short stubs from the edge of the triangle to the edge of the bounding box.



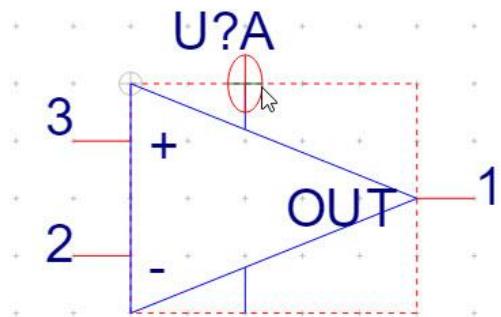
9. Toggle the **Snap To grid** back ON when you finish.

## Placing the Power Pins

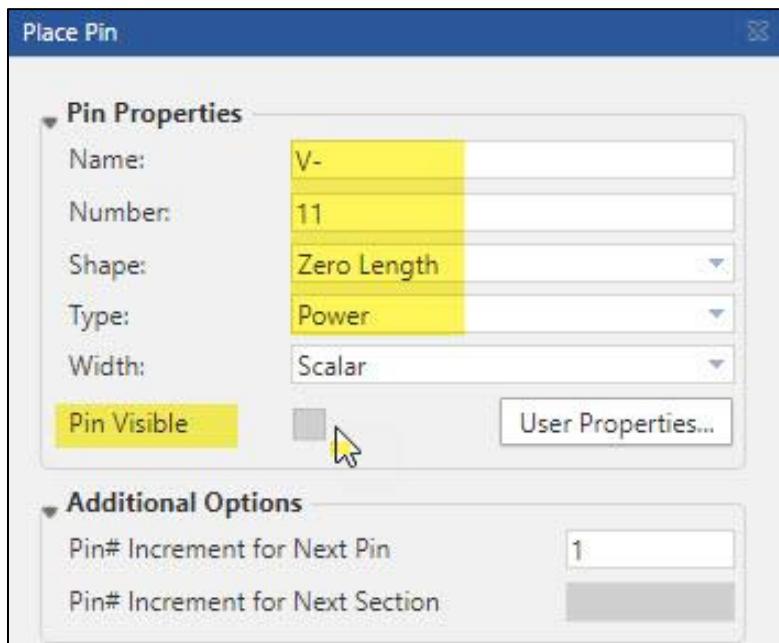
1. Choose **Place – Pin**.
2. Enter the information as shown below and click **OK**.



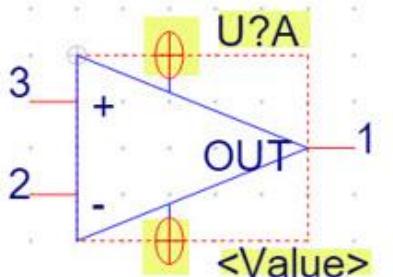
3. Click to add the power pin to the end of the line stub at the top of the part.



4. Add the second power pin to the bottom line stub using the information shown below.



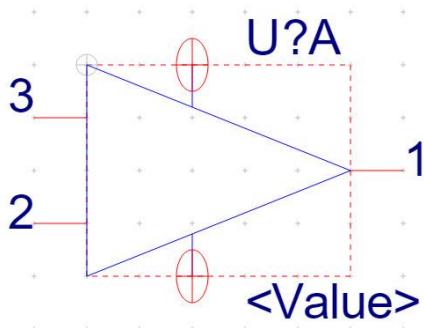
5. Drag the part reference U?A and <VALUE>, as shown below.



6. Choose **File – Save**. Click **Yes to All** to save the changes.

## Hiding Pin Names

1. In the Part Properties section of the Property Sheet, turn off the checkbox for **Pin Name Visible**.

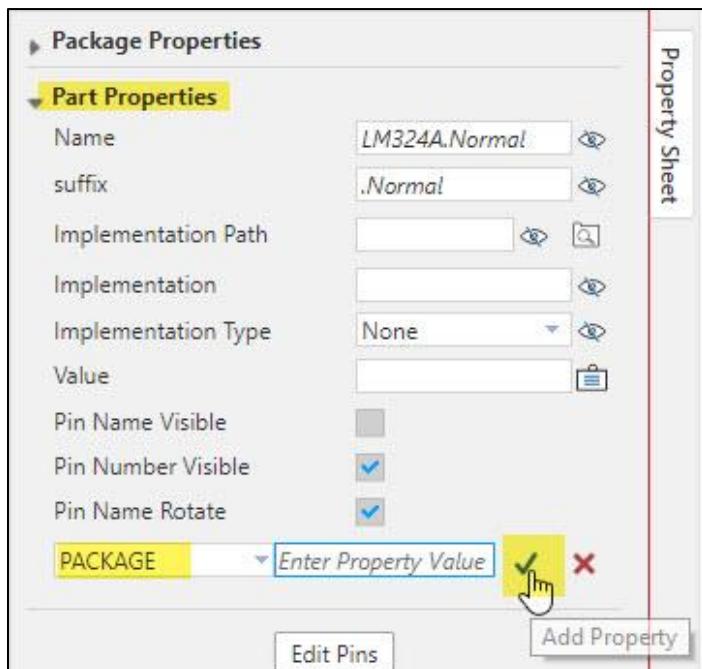


2. Save the part.

## Adding a Gate-Grouping Property

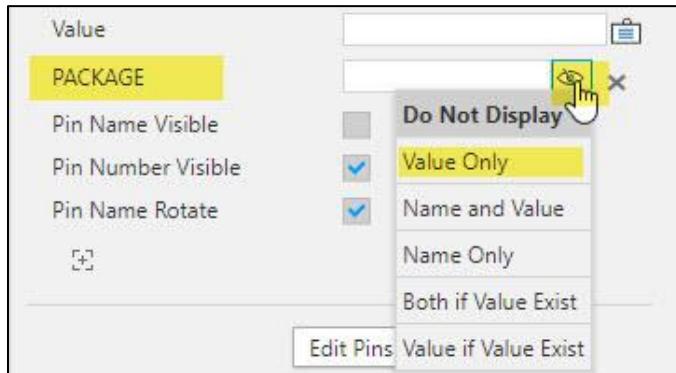
This is an important aspect of a heterogeneous part. See the lecture material for more details.

1. In the Part Properties section of the Property pane, type in a new property named **PACKAGE**.

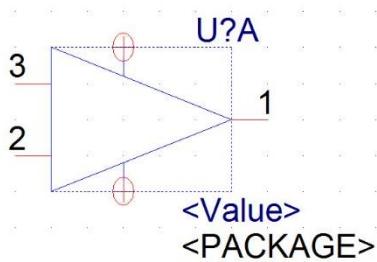


Leave the Property value field blank and click the **Add Property** icon.

- Once the property has been added, right-click to change the visibility to **Value Only**.



- Check that your part looks like this.



- Choose **File – Save**.

### Creating the Symbol for Gates 2, 3, and 4

- Choose **View – Next Part** and click the **Zoom to all** icon.
- Create the next sections in the package. What makes these sections different from the first section is that they don't have any power pins.

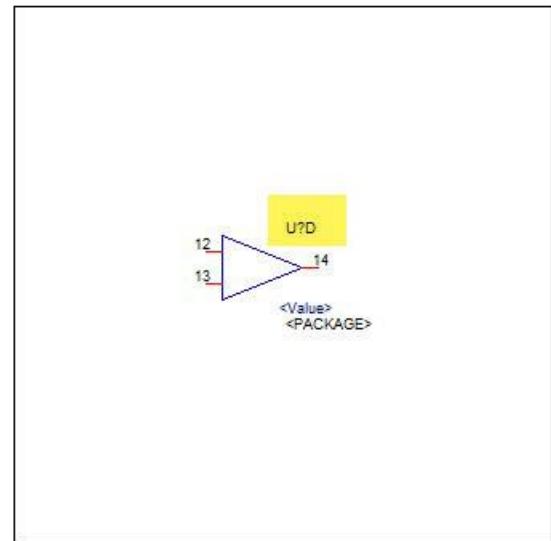
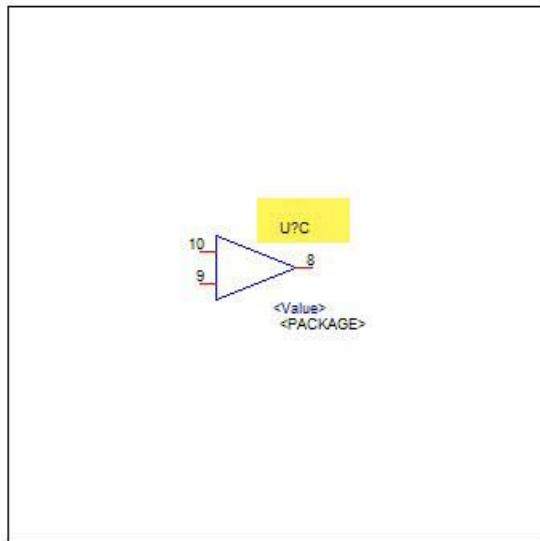
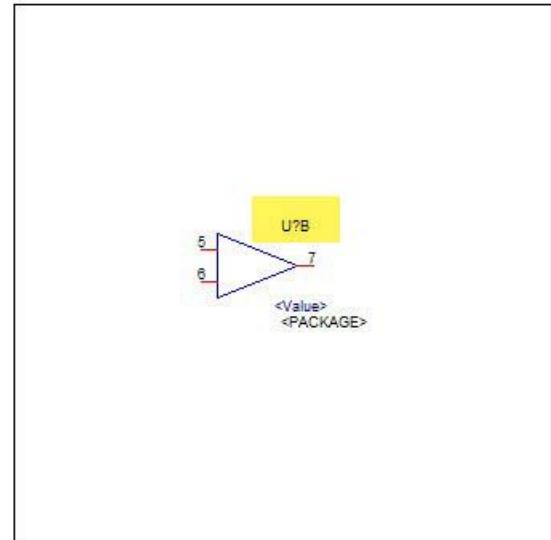
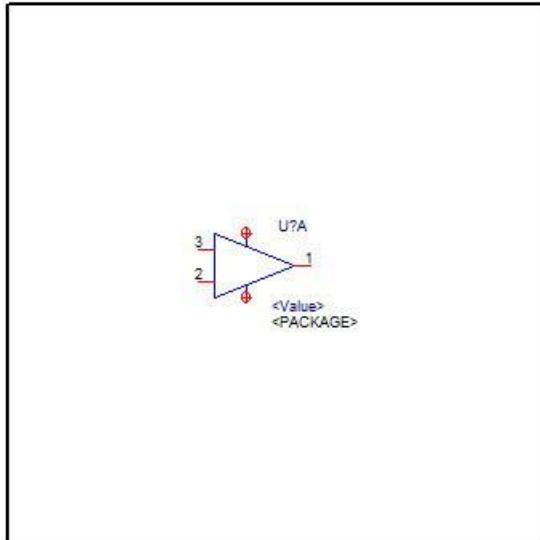
Here are the pin names and numbers for the other gates.

Gate B	Gate C	Gate D
+ = 5	+ = 10	+ = 12
- = 6	- = 9	- = 13
OUT = 7	OUT = 8	OUT = 14

**Tip:** You can copy the graphics, pins, and properties from one section to another (pin numbers will need to be re-assigned in each of the copied sections).

Working with Libraries

Don't forget to delete the power pins and switch the pin names to invisible, as shown below.



3. Save and close the part.

### Optional Lab

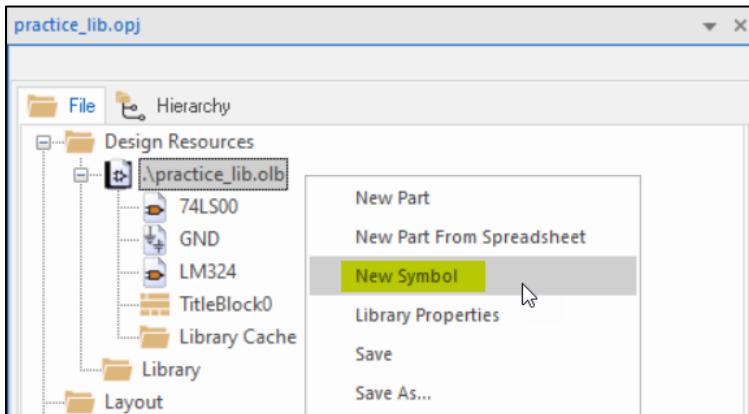
After class, see **Appendix A: Optional Topics, Lab A-2: Testing the LM324 Part.**



## Lab 4-6 Creating a Power Symbol

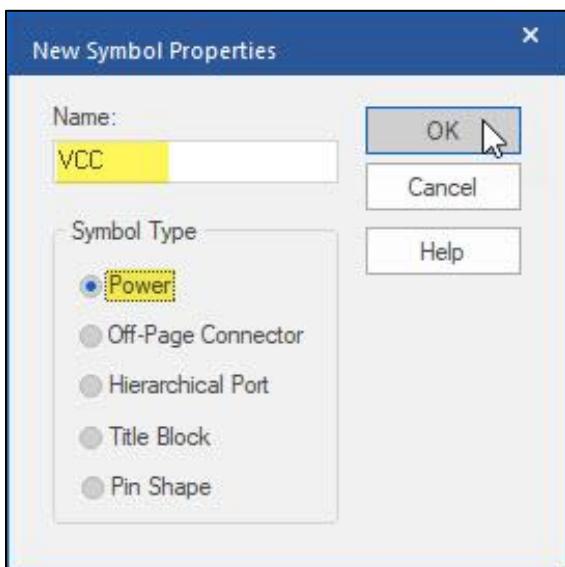
**Objective:** To create a power symbol.

1. Right-click on **practice\_lib.olb** and select **New Symbol**.

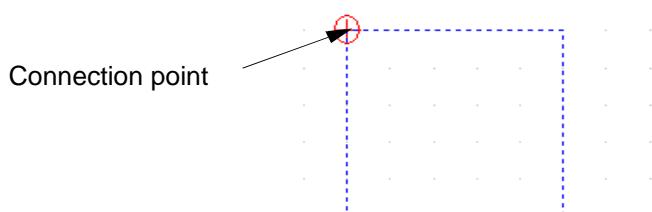


The New Symbol Properties window appears.

2. Name the symbol **VCC**. Set Symbol Type to **Power** and click **OK**.

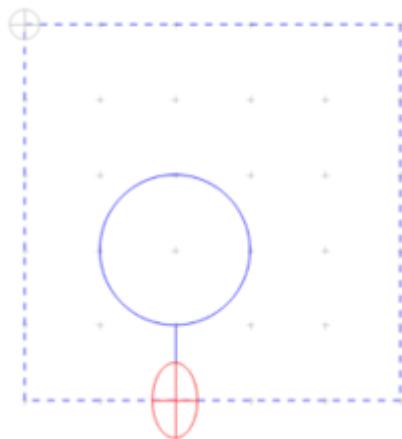


3. Click the **Zoom to all** icon.

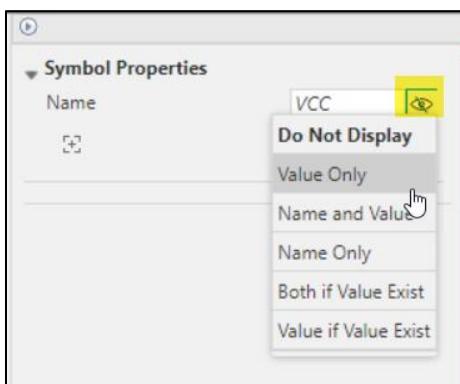


The symbol graphic consists of one zero-length pin located at the origin in the upper left corner of the bounding box. Power symbols have only one connection point.

4. Drag the connection point to the bottom edge of the bounding box.
5. Use **Place – Line** to draw a vertical line that is one grid long and up from the connection point.
6. Use **Place – Ellipse** to draw a circle 2 grids square and drag it to the top of the line. Alternately, choose **Place – Polyline** to draw an arrow shape on the top of a line, as shown below.

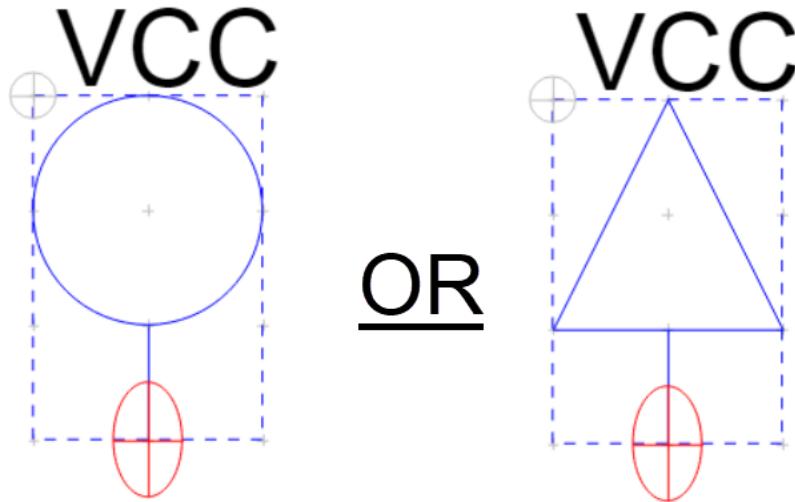


7. You can temporarily disable Snap to Grid. Click the **Snap to Grid** icon, then draw (or move) the graphics as needed.
- Caution:** *Be sure to toggle Snap to Grid back on when you're done!*
8. In the Symbol Properties section of the Property Sheet, set the visibility for the Name property to **Value Only**.



9. Reduce the size of the bounding box and reposition the name property to the top of the symbol.

The symbol should look like one of the following examples.



10. Save and close the symbol.

### Optional Lab

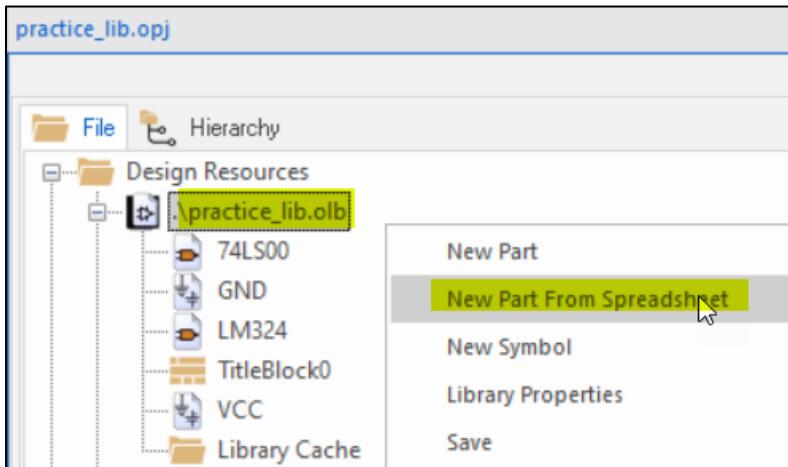
After class, see **Appendix A: Optional Topics, Lab A-3: Creating a Custom Title Block.**



## Lab 4-7 Creating Parts Using a Spreadsheet Interface

**Objective:** To create a high pin-count split part using a spreadsheet-like interface.

1. Right-click on **practice\_lib.olb** and select **New Part From Spreadsheet**.



The New Part Creation Spreadsheet opens.

2. In the Part Name field, enter **PCA9548**.
3. In **No. of Sections**, enter **3**.
4. This part has 24 pins. Use the following table to enter the pin data into the cells of the spreadsheet. See the **Tip** below the table to save time.

Pin Number	Pin Name	Pin Type	Pin Shape	Position	Section
1	A0	Input	Short	Left	A
2	A1	Input	Short	Left	A
3	RESET	Input	Short	Left	A
4	SD0	Output	Short	Right	A
5	SC0	Output	Short Clock	Right	A
6	SD1	Output	Short	Right	A
7	SC1	Output	Short Dot Clock	Right	A
8	SD2	Output	Short	Right	A
9	SC2	Output	Short Clock	Right	A
10	SD3	Output	Short	Right	A

11	SC3	Output	Short Dot Clock	Right	A
12	GND	Power	Short	Bottom	C
13	SD4	Output	Short	Right	B
14	SC4	Output	Short Clock	Right	B
15	SD5	Output	Short	Right	B
16	SC5	Output	Short Dot Clock	Right	B
17	SD6	Output	Short	Right	B
18	SC6	Output	Short Clock	Right	B
19	SD7	Output	Short	Right	B
20	SC7	Output	Short Dot Clock	Right	B
21	A2	Input	Short	Left	B
22	SCL	Input	Short Clock	Left	B
23	SDA	Bidirectional	Short	Left	B
24	VDD	Power	Short	Top	C

**Tip:** To copy column information from this lab PDF file, press the **Alt** key and drag a rectangle down the column.

Alternately, you can open the *C:\User1\Capture\data\_files\part\_spreadsheet.xls* file in Excel and use **Ctrl+C** and **Ctrl+V** to copy and paste it into the spreadsheet tool, as shown below.

Be careful to paste the correct information into the correct columns and not to paste any information into the Pin Visibility and PinGroup columns of the New Part Creation Spreadsheet.

## Working with Libraries

When you have finished entering the data, your spreadsheet should look like this:

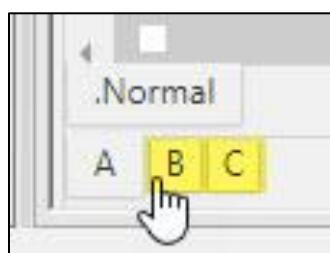
New Part Creation Spreadsheet								
	Number	Name	Type	Pin Visibility	Shape	PinGroup	Position	Section
1	1	A0	Input	<input checked="" type="checkbox"/>	Short		Left	A
2	2	A1	Input	<input checked="" type="checkbox"/>	Short		Left	A
3	3	RESET	Input	<input checked="" type="checkbox"/>	Short		Left	A
4	4	SD0	Output	<input checked="" type="checkbox"/>	Short		Right	A
5	5	SC0	Output	<input checked="" type="checkbox"/>	Short Clock		Right	A
6	6	SD1	Output	<input checked="" type="checkbox"/>	Short		Right	A
7	7	SC1	Output	<input checked="" type="checkbox"/>	Short Dot Clock		Right	A
8	8	SD2	Output	<input checked="" type="checkbox"/>	Short		Right	A
9	9	SC2	Output	<input checked="" type="checkbox"/>	Short Clock		Right	A
10	10	SD3	Output	<input checked="" type="checkbox"/>	Short		Right	A
11	11	SC3	Output	<input checked="" type="checkbox"/>	Short Dot Clock		Right	A
12	12	GND	Power	<input type="checkbox"/>	Short		Bottom	C
13	13	SD4	Output	<input checked="" type="checkbox"/>	Short		Right	B
14	14	SC4	Output	<input checked="" type="checkbox"/>	Short Clock		Right	B
15	15	SD5	Output	<input checked="" type="checkbox"/>	Short		Right	B
16	16	SC5	Output	<input checked="" type="checkbox"/>	Short Dot Clock		Right	B
17	17	SD6	Output	<input checked="" type="checkbox"/>	Short		Right	B
18	18	SC6	Output	<input checked="" type="checkbox"/>	Short Clock		Right	B
19	19	SD7	Output	<input checked="" type="checkbox"/>	Short		Right	B
20	20	SC7	Output	<input checked="" type="checkbox"/>	Short Dot Clock		Right	B
21	21	A2	Input	<input checked="" type="checkbox"/>	Short		Left	B
22	22	SCL	Input	<input checked="" type="checkbox"/>	Short Clock		Left	B
23	23	SDA	Bidirectional	<input checked="" type="checkbox"/>	Short		Left	B
24	24	VDD	Power	<input type="checkbox"/>	Short		Top	C

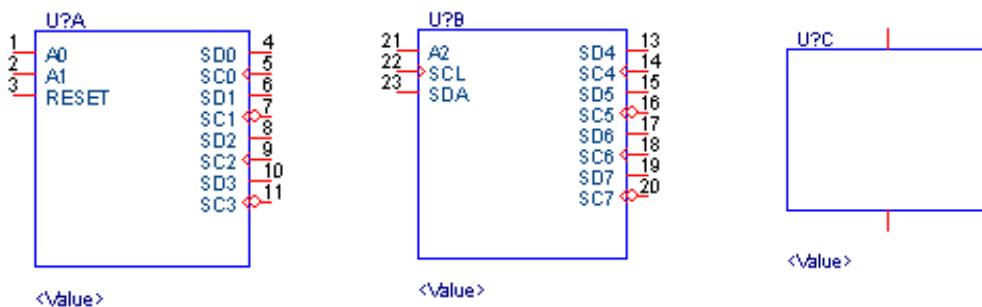
 Add Pins... Delete Pins Save  Cancel Help

5. Click **Save** to apply the data and create a new part.

The new part is listed in the Project Manager window.

6. Double-click on the **PCA9548** part to open it, then click on the ABC tiles in the lower-left corner to view all three symbols.





7. When you use the New Part Creation Spreadsheet to generate a part, you may need to adjust pin locations or add user properties. See if you can make the VDD and GND pins visible.

**Tip:** Click on a power pin and look for the Pin Properties section in the Property Sheet.

8. Save and close the part.



## Lab 4-8    Splitting an Existing Part

**Objective:** To use the Split Part command to break a part into two sections.

---

### Copying Between Libraries

1. Choose **File – Open – Library**.
2. Navigate to the *C:\User1\Capture\training\_libs* directory.
3. Click **CLASS\_LIB.OLB** and click **Open**.  
You will copy from the *CLASS\_LIB* and paste it into your *PRACTICE\_LIB*. Each library has a tab along the bottom of the Project Manager window.
4. In the *CLASS\_LIB* window, **right-click** on the **EPF8282A/LCC** part and choose **Copy**.
5. Click on the **PRACTICE\_LIB** tab, **right-click** on **practice\_lib.olb**, and choose **Paste**.  
The copied part is added to the library.
6. Close the *CLASS\_LIB* library.
7. **Right-click** on **practice\_lib.olb** and choose **Save**.  
**Important:** We do not recommend having parts with the same name in different libraries. When copying parts and symbols, remember to give the copied parts a unique name in the destination library.

### Using the Split Part Command

1. **Right-click** on the **EPF8282A/LCC** part and choose **Split Part**.  
The Split Part Section Input Spreadsheet opens.
2. At the top of the form, change the No. of Sections field to **3**.
3. In the upper-right corner of the form, change the Part Numbering field from **Numeric** to **Alphabetic**.

- Double-click on the **Name** column header to sort the pin names alphabetically in ascending order.

Split Part Section Input Spreadsheet

Part Name:		EPF8282A/LCC	No. of Sections:	3	Part Ref Prefix:	U	Part Numbering	<input type="radio"/> Numeric <input checked="" type="radio"/> Alphabetic
	Number	Name	Type	Pin Visibility	Shape	PinGroup	Position	Section
1	78	ADD0	Output	<input checked="" type="checkbox"/>	Line		Right	A
2	76	ADD1	Output	<input checked="" type="checkbox"/>	Line		Right	A
3	62	ADD10	Output	<input checked="" type="checkbox"/>	Line		Right	A
4	61	ADD11	Output	<input checked="" type="checkbox"/>	Line		Right	A

## Assigning Pins to Section B

- Change the Section column for input pins BD0-BD7 to **B**.

25	BD0	Input	<input checked="" type="checkbox"/>	Line		Left	A
24	BD1	Input	<input checked="" type="checkbox"/>	Line		Left	A
23	BD2	Input	<input checked="" type="checkbox"/>	Line		Left	B
22	BD3	Input	<input checked="" type="checkbox"/>	Line		Left	C
21	BD4	Input	<input checked="" type="checkbox"/>	Line		Left	A
20	BD5	Input	<input checked="" type="checkbox"/>	Line		Left	A
19	BD6	Input	<input checked="" type="checkbox"/>	Line		Left	A
18	BD7	Input	<input checked="" type="checkbox"/>	Line		Left	A

**Tip:** Drag across the Section fields, then **Ctrl+left**, and click on the down arrow to choose section B from the pull-down menu.

- Do the same for output pins RD0-RD7 and VD0-VD7.

81	RD0	Bidirectional	<input checked="" type="checkbox"/>	Line		Right	B
82	RD1	Bidirectional	<input checked="" type="checkbox"/>	Line		Right	B
83	RD2	Bidirectional	<input checked="" type="checkbox"/>	Line		Right	B
84	RD3	Bidirectional	<input checked="" type="checkbox"/>	Line		Right	B
1	RD4	Bidirectional	<input checked="" type="checkbox"/>	Line		Right	B
2	RD5	Bidirectional	<input checked="" type="checkbox"/>	Line		Right	B
3	RD6	Bidirectional	<input checked="" type="checkbox"/>	Line		Right	B
4	RD7	Bidirectional	<input checked="" type="checkbox"/>	Line		Right	B
40	VD1	Input	<input checked="" type="checkbox"/>	Line		Right	B
41	VD2	Input	<input checked="" type="checkbox"/>	Line		Right	B
42	VD3	Input	<input checked="" type="checkbox"/>	Line		Right	B
43	VD4	Input	<input checked="" type="checkbox"/>	Line		Right	B
44	VD5	Input	<input checked="" type="checkbox"/>	Line		Right	B
45	VD6	Input	<input checked="" type="checkbox"/>	Line		Right	B
46	VD7	Input	<input checked="" type="checkbox"/>	Line		Right	B

## Assigning Pins to Section C

1. Double-click on the **Type** column header to sort the pins by type. Then scroll to locate all the Power pins and change the Section column to **C**.

5	GND	Power	<input type="checkbox"/>	Zero L		Bottom	C 
26	GND	Power	<input type="checkbox"/>	Zero L		Bottom	C
47	GND	Power	<input type="checkbox"/>	Zero L		Bottom	C
68	GND	Power	<input type="checkbox"/>	Zero L		Bottom	C
17	VCC	Power	<input type="checkbox"/>	Zero L		Top	C
38	VCC	Power	<input type="checkbox"/>	Zero L		Top	C
59	VCC	Power	<input type="checkbox"/>	Zero L		Top	C
80	VCC	Power	<input type="checkbox"/>	Zero L		Top	C

2. For all VCC and GND pins, turn on the **Pin Visibility** checkbox and toggle the **Shape** field to **Short**.

Number	Name	Type	Pin Visibility	Shape	PinGroup	Position	Section
28	GAIN	Output	<input checked="" type="checkbox"/>	Line		Right	A
48	NRS	Output	<input checked="" type="checkbox"/>	Line		Right	A
49	RDCLK	Output	<input checked="" type="checkbox"/>	Clock		Right	A
77	RDYNBUSY	Output	<input checked="" type="checkbox"/>	Line		Right	A
27	TDO	Output	<input checked="" type="checkbox"/>	Line		Left	A
5	GND	Power	<input checked="" type="checkbox"/> 	Short 		Bottom	C
26	GND	Power	<input checked="" type="checkbox"/> 	Short		Bottom	C
47	GND	Power	<input checked="" type="checkbox"/>	Short		Bottom	C
68	GND	Power	<input checked="" type="checkbox"/>	Short		Bottom	C
17	VCC	Power	<input checked="" type="checkbox"/>	Short		Top	C
38	VCC	Power	<input checked="" type="checkbox"/>	Short		Top	C
59	VCC	Power	<input checked="" type="checkbox"/>	Short		Top	C
80	VCC	Power	<input checked="" type="checkbox"/>	Short		Top	C

3. Click **Save**.

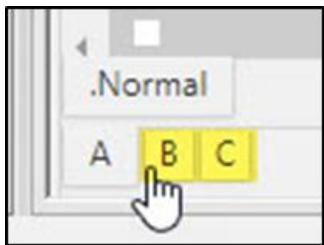
If a warning occurs, click **Continue**.

4. Click **Yes** to regenerate the part.

The part is now split into three sections.

### Viewing the Split Part

1. In the **PRACTICE\_LIB** library, double-click on part **EPF8282A/LCC**.  
Section A of the part is displayed.
2. Click on the ABC tiles in the lower-left corner to view all three symbols.



3. Close the part.  
The PRACTICE\_LIB library should still be open.



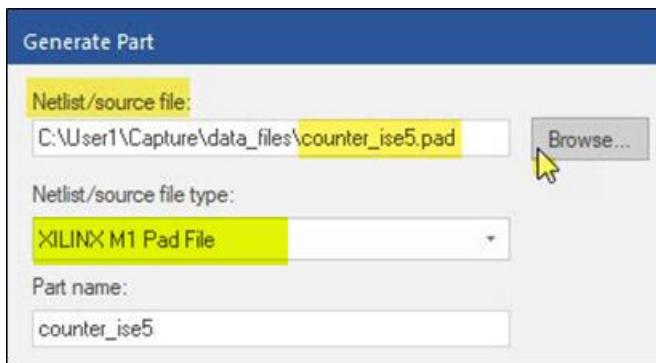
## Lab 4-9 Generating Parts from Imported Data

**Objective:** To auto-generate parts by importing various text files.

### Importing a Xilinx Pad File

1. Click to activate the Project Manager window, then choose **Tools – Generate Part**.
2. In the Generate Part window, click the **Browse** button to specify a source file.
3. In the Browse File window, navigate to the *C:\User1\Capture\data\_files* directory.  
**Note:** Always replace the *User1* portion of the path with the actual path to the *Capture* folder on your system.
4. Set the Files of the type field to **XILINX M1 Pad File**, and select the **counter\_ise5.pad** file, and click **Open**.

The source file type and part name fields are populated automatically.



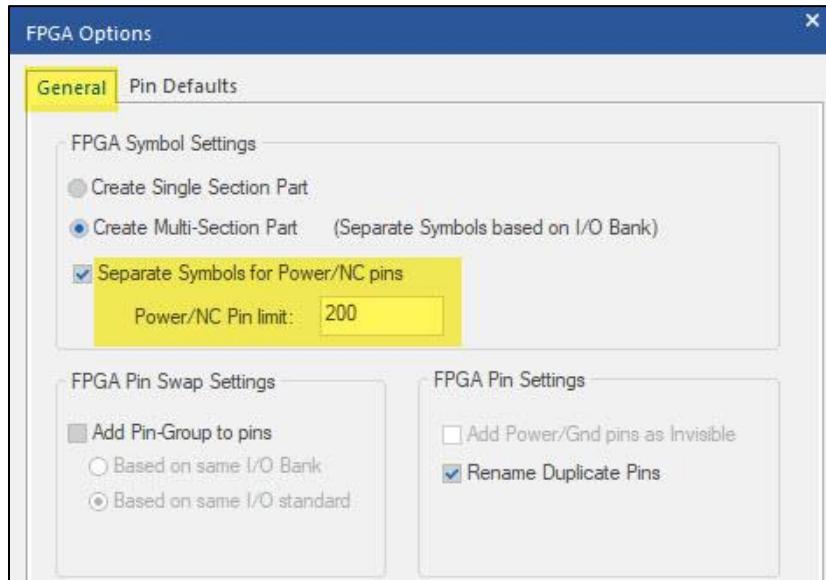
5. To specify the destination library, click **Browse** and navigate to the *C:\User1\Capture\training\_libs\PRACTICE\_LIB.OLB* file.



6. Click the **FPGA Setup** button (in the upper-right corner) to control how the part will be generated.

The FPGA Options window opens.

7. In the **General** tab, set the options shown below.



8. Click **OK**.

9. Click **OK** in the Generate Part window.

The Split Part Section Input Spreadsheet window opens.

**Note:** Click **No** to open in READ ONLY mode.

10. Expand/scroll the window and **double-click** on the Section column header to sort the pins by section. The Section column is the last column on the right.

11. Notice the part will have 10 sections based on your FPGA setup options.

12. For all Power pins in Section 10, drag across the **Shape** fields, then **Ctrl+left** on the down arrow to choose **Short** from the pull-down menu.

Number	Name	Type	Pin Visibility	Shape
B33	TMS	Passive	<input checked="" type="checkbox"/>	Line
A21	VCCINT	Power	<input checked="" type="checkbox"/>	Short
AB2	VCCINT_AB	Power	<input checked="" type="checkbox"/>	Line
AB32	VCCINT_AB	Power	<input checked="" type="checkbox"/>	Short Clock
AD2	VCCINT_AD	Power	<input checked="" type="checkbox"/>	Short Dot
AD32	VCCINT_AD	Power	<input checked="" type="checkbox"/>	Short Dot Cl
AG3	VCCINT_AG	Power	<input checked="" type="checkbox"/>	Short
AG31	VCCINT_AG	Power	<input checked="" type="checkbox"/>	Zero Length
AJ13	VCCINT_AJ1	Power	<input checked="" type="checkbox"/>	Short
AK8	VCCINT_AK	Power	<input checked="" type="checkbox"/>	Short

13. In the Split Part Section Input Spreadsheet window, click **Save** to create the part.

## Viewing the Generated Part

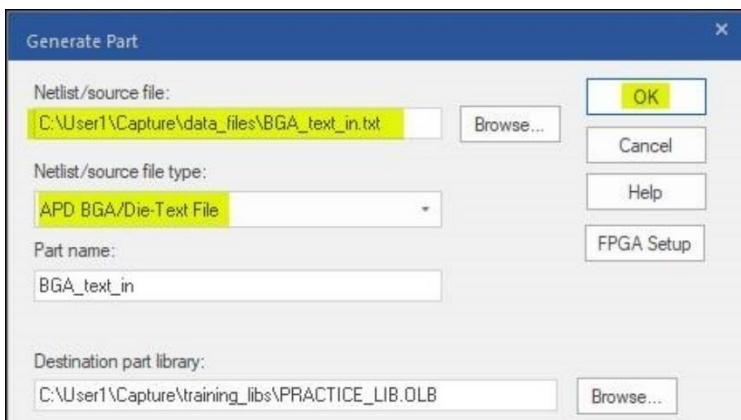
1. Double-click on the new **counter\_ise5** part in the *PRACTICE\_LIB* window and view the ten symbols for the FPGA.



2. Close the part.

## Importing a BGA Text File

1. Click on the Project Manager window and choose **Tools – Generate Part**.
2. In the Generate Part window, click the **Browse** button to specify a source file.
3. In the Browse File window, navigate to the *C:\User1\Capture\data\_files* directory.
4. Set the files in the type field to APD BGA/Die-Text Files, select the *BGA\_text\_in.txt* file, and click **Open**.



5. Click **OK** in the Generate Part window to start the process.

The Split Part Section Input Spreadsheet window opens.

6. Set the number of sections to **8** and the part numbering to **Alphabetic**.



7. Expand the width of the **Name** field so you can see all the pin names.
8. Assign all the BUS\_DATA pins to section **B**, the DQ pins to section **C**, the NC pins to section **D**, the RXD pins to section **E**, the TXD and TXE pins to section **F**, the VDD pins to section **G**, and the VSS pins to section **H**.
9. Toggle the **Shape** field for all Power pins to **Short**.
10. In the Split Part Section Input Spreadsheet window, click **Save** to create the part.

### Viewing the Generated Part

1. Double-click on the **BGA\_text\_in** part in the *PRACTICE\_LIB* and view the eight symbols for the BGA part.



You can widen some of the symbol outlines if you want to.

2. Save and close the part.

### Closing the Practice Library

1. Close the *PRACTICE\_LIB* library.

The Capture session window is still running.



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# **Module 5: Building a Simple Schematic**

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## Lab 5-1 Creating a New Project

**Objective:** To use the PCB Project wizard.

---

### Setting Project Name and Location

1. In the Capture session window, choose **File – New – Project**.

The New Project window appears.

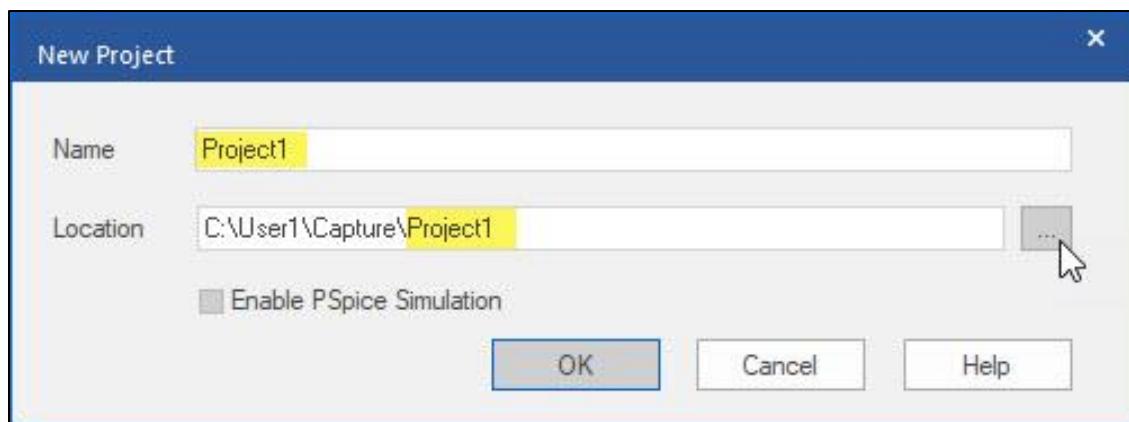
2. In the Name field, enter **Project1**.

3. Click the **Browser** button to the right of the Location field.

**Note:** In the next step, always replace *User1* with the actual path to the *Capture* folder on your system.

4. In the Select Folder window, navigate to the *C:\User1\Capture* directory and click the **Select Folder** button.

5. Add the **Project1** folder name to the end of the path, as shown below, and click **OK**.



The new project is displayed in the Project Manager window, and a blank schematic page is opened.

6. Notice the project name shown at the top of the Project Manager window.

### Viewing the Schematic Title Block

1. Click in the schematic window to make it active.
2. Click the **Zoom to all** icon and notice that the data in the title block matches the information you entered in the design template.
3. Click the **Zoom out** icon.

You are ready to begin your first design.



## Lab 5-2 Placing Parts

**Objective:** To add parts to the schematic.

---

### Adding a 74F162

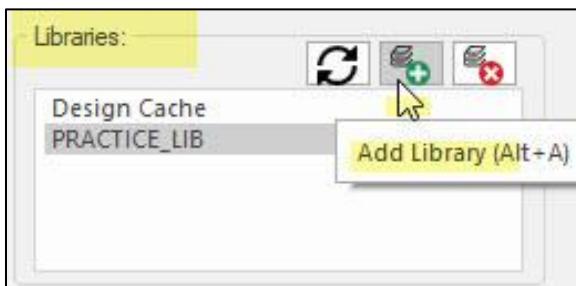
1. Make sure the schematic window is active.

2. Choose **Place – Part**.



The Place Part pane appears along the right side of the Capture session window.

3. In the Libraries section, click the **Add Library** icon.



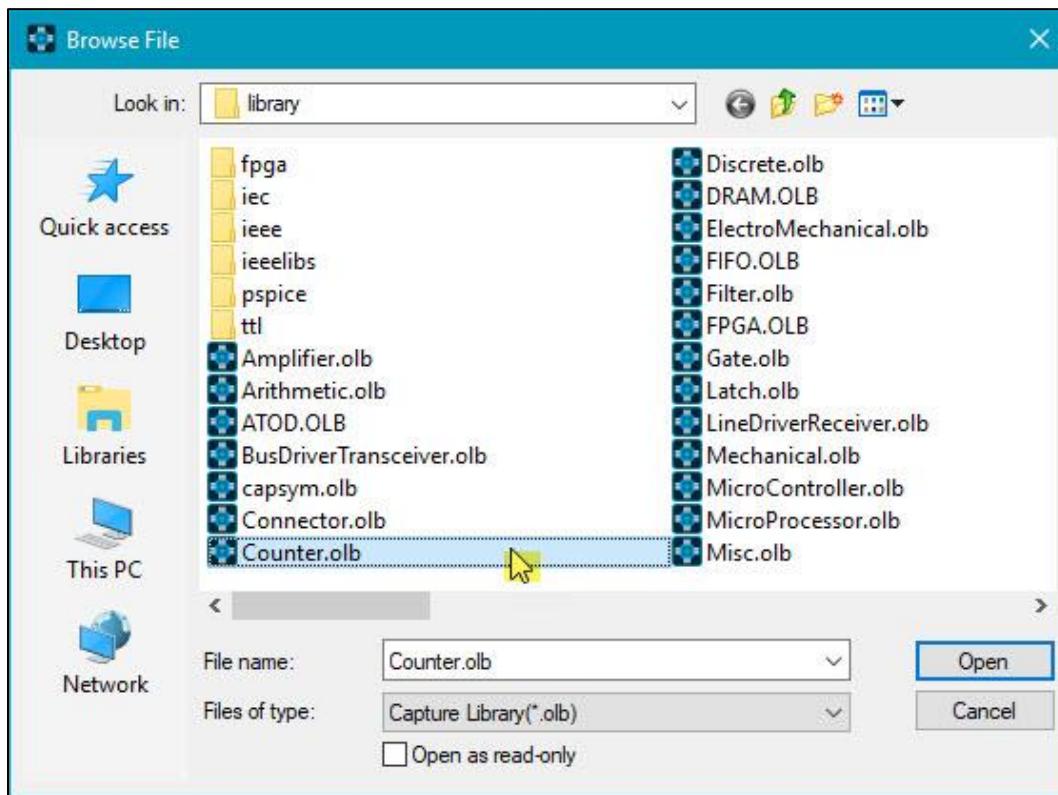
The Browse File window appears.

4. Set the Look in *the* field to `$CDSROOT\tools\capture\library`.

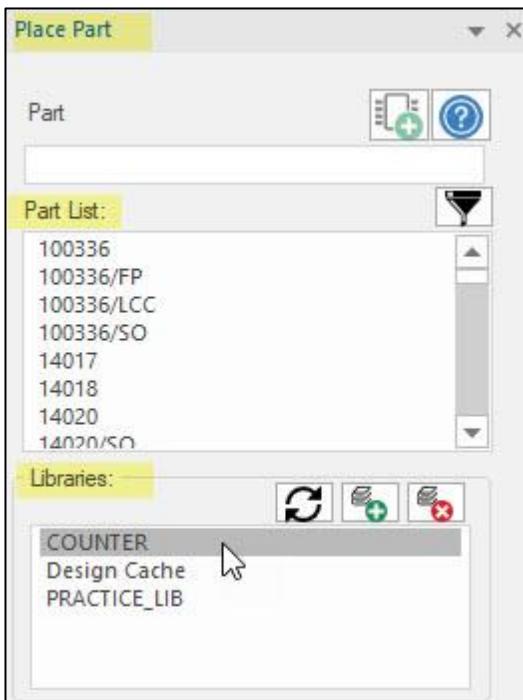
This is where the Capture libraries are installed. The `$CDSROOT` variable represents where the Cadence software is installed on your system.

Building a Simple Schematic

5. Select the **Counter.olb** library and click **Open**.

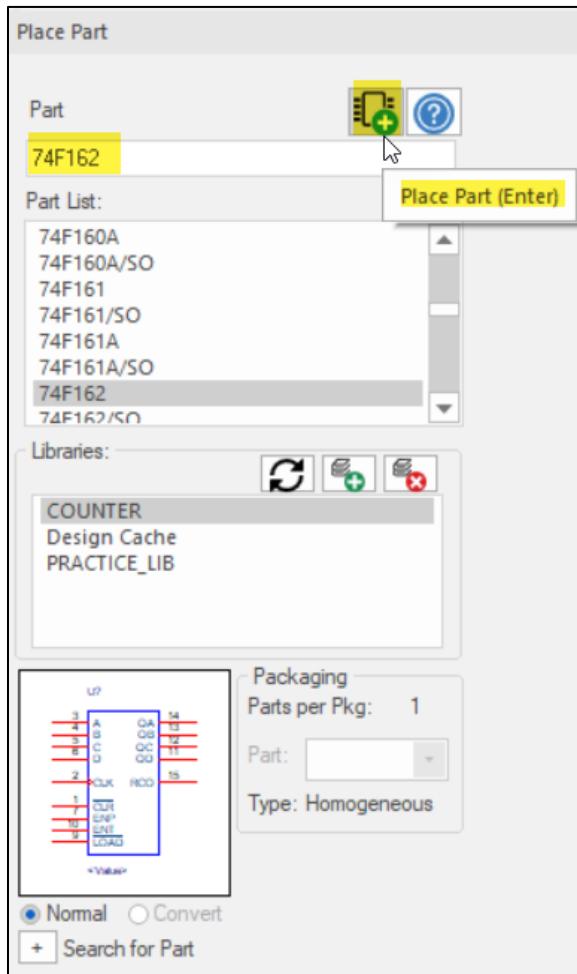


The *COUNTER* library is added to the Libraries list in the Place Part pane. All the parts in this library are listed in the Part List.



6. In the Part field, enter **74F162**.

Notice how each character you enter is used to search the Part List for all matching entries.



A graphic of the 74F162 part is shown in the Place Part pane.

7. In the top-right corner of the Place Part pane, click the **Place Part** icon.

The part attaches to the cursor.

8. Click to place the part on the page.

The part remains attached to the cursor, ready to place more instances of it.

9. **Right-click** and select **End Mode**.

10. Click anywhere on the page to deselect the newly added part.

### 11. Choose **File – Save**.

The 74F162 part was in the *COUNTER* library. This library was added to the Libraries list. This library list is stored in the *Capture.ini* file.

## Adding a 74LS00

1. In the Place Part pane, click the plus sign (+) to the left of Search for Part.

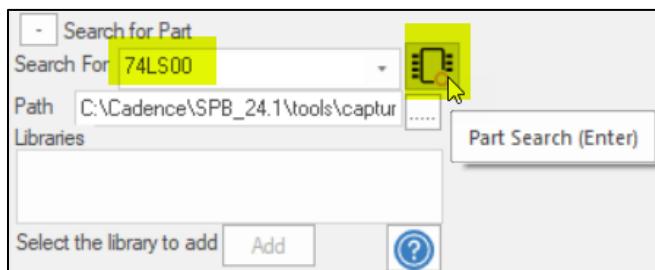


2. In the Search For field, enter **74LS00**.
3. Make sure the library Path field (located below the part search field) shows the following installation path and library directory:

`$CDSROOT\tools\capture\library`

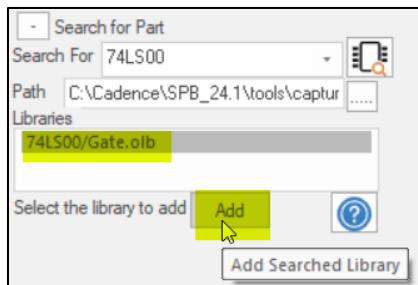
Replace the `$CDSROOT` variable with the path to where the Cadence software is installed (for example, `C:\Cadence\SPB_24.1`). If the path is not correct, click the **Browser** button to correct the path.

4. Click the **Part Search** icon.



The search results are shown in the Libraries list (for example, *74LS00/Gate.olb*). This means that the 74LS00 part was found in the *GATE* library.

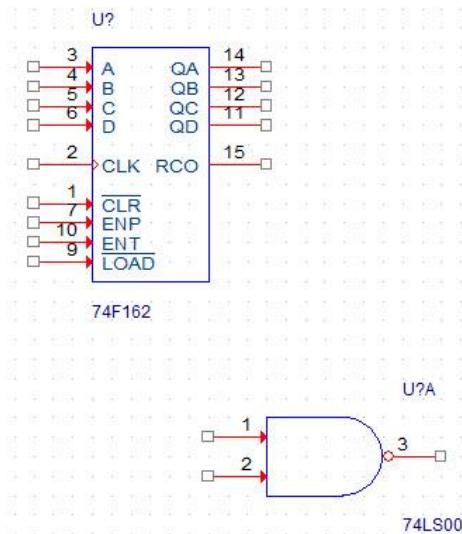
5. Click the **74LS00/Gate.olb** entry in the Libraries list and click **Add**.



The *GATE* library is added to the Libraries list in the Place Part pane, and the 74LS00 part is automatically selected in the Part List.

6. In the top-right corner of the Place Part pane, click the **Place Part** icon to add this part to the schematic.
7. To exit from place part mode, press **Esc**.
8. Press **Esc** again to deselect the newly added part.
9. Choose **File – Save**.

The schematic page should look something like the following:

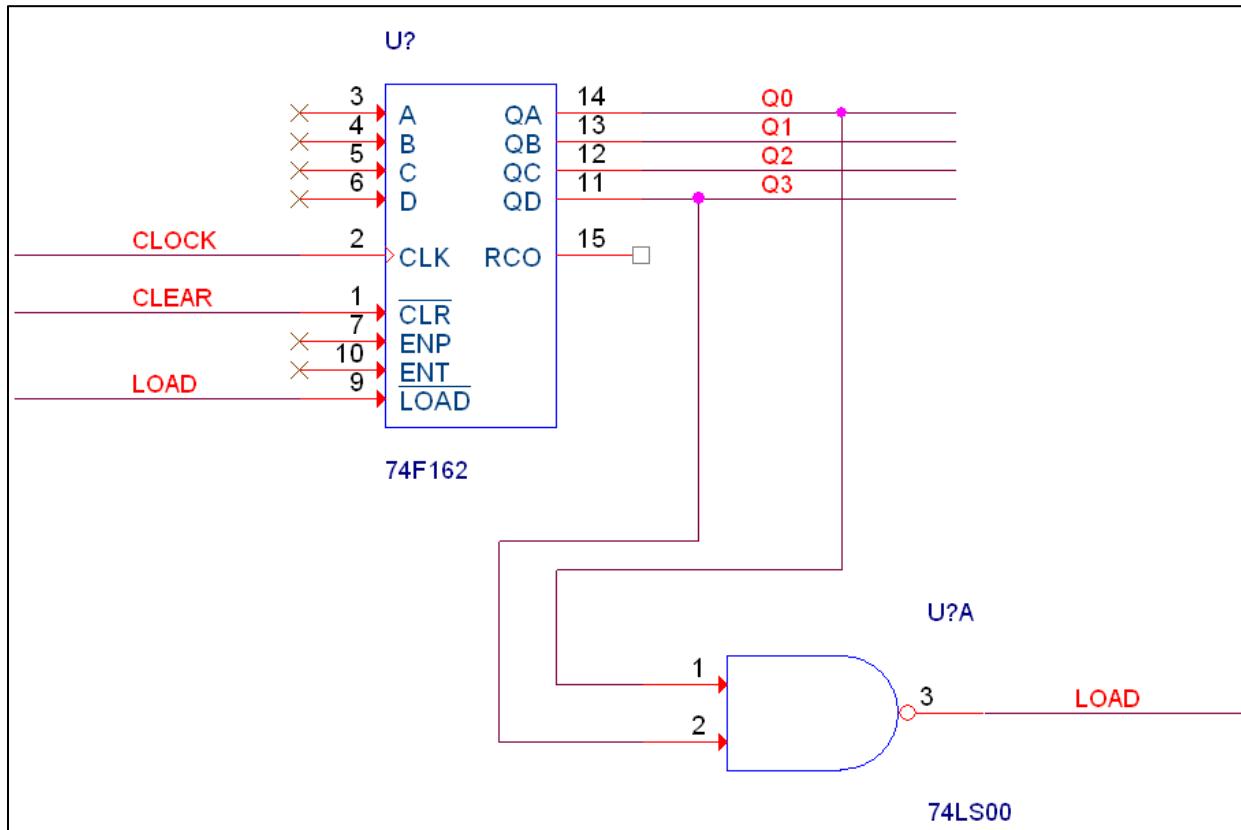


The 74F162 part was in the COUNTER library, and the 74LS00 part was in the GATE library. When you added these libraries to the Libraries list in the Place Part pane, Capture added these libraries to the *Capture.ini* file, where they become permanently available for this project and for all future projects you create.



**Lab 5-3 Adding and Naming Wires****Objective:** To add and name wires and complete the schematic.

Use this example as a guide for this lab.

**Adding Wires**

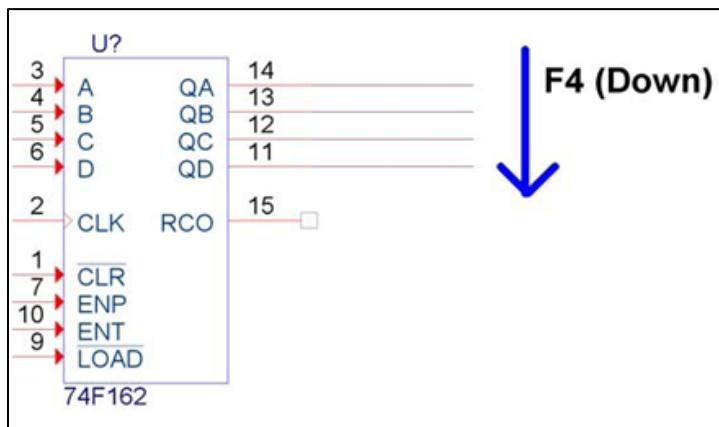
1. Choose **Place – Wire**.

You can also use the **Place – Wire** icon in the schematic toolbar (or press **w**). 

2. Click pin **14** of part **74F162**. Move the pointer to the right a short distance. **Double-click** to end the wire.
3. Press **F4** three times.

The wire segment is repeated each time, one grid down from the original.

4. Press **Esc** twice.



## Naming Wires

1. Choose **Place – Net Alias**.

You can also click the **Place – Net Alias** icon or press **n**.



2. In the Place Net Alias window, enter **Q0** and click **OK**.

A net name box is attached to the cursor.

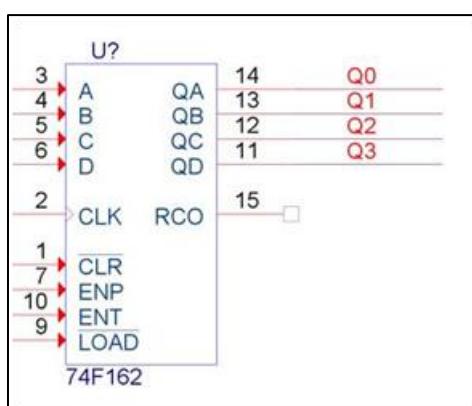
3. Click the wire attached to pin 14 of the 74F162 part.

Net name **Q0** is assigned to the selected wire. Place Net Alias is still active.

4. In this order, click the wires attached to pins 13, 12, and 11.

Capture automatically increments the net names to **Q1**, **Q2**, and **Q3**, respectively.

5. Press **Esc** twice.

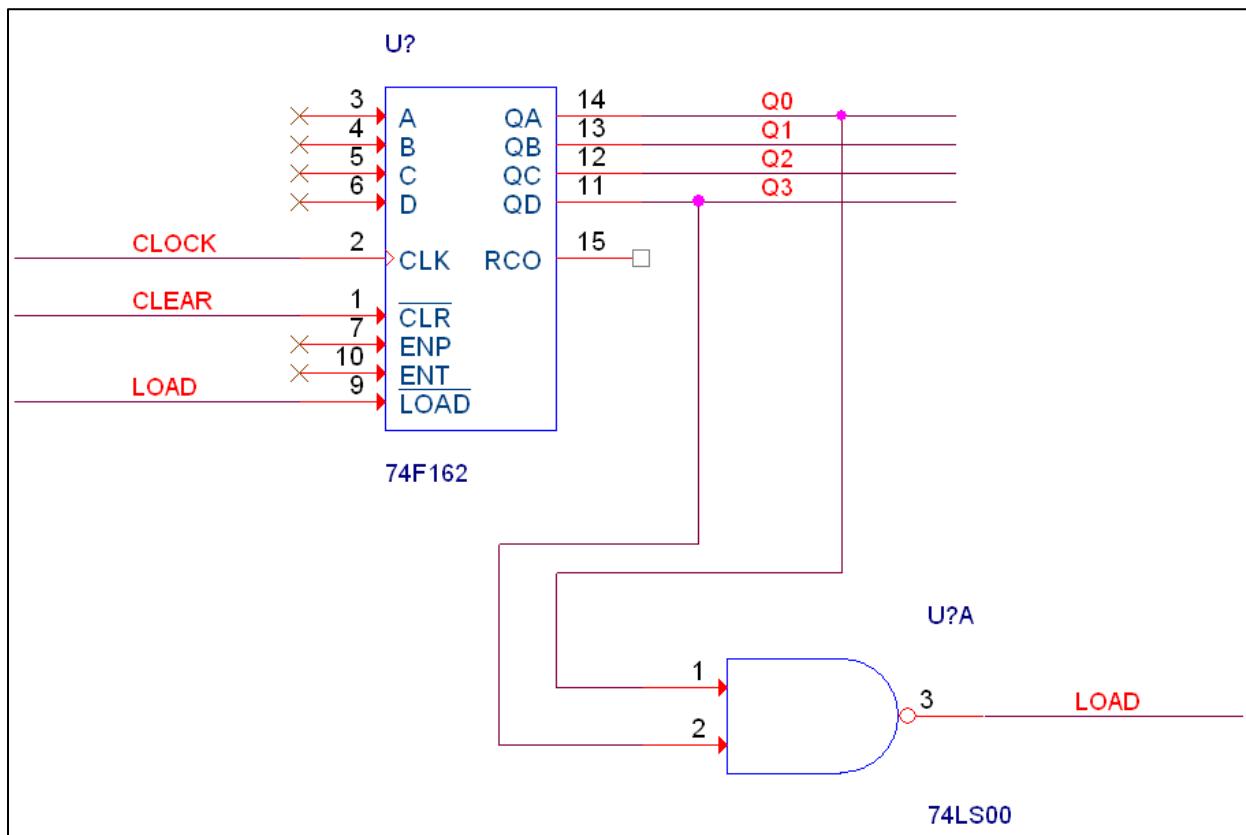


## Building a Simple Schematic

Pressing the **F4** key to repeat the prior action does not work in **Place – Net Alias**. Also, if the net alias ends in a non-numeric character, the name remains the same when you place successive aliases.

## Completing the Schematic

1. Use the **Place – Wire** and **Place – Net Alias** icons to complete the schematic. Connect the 74LS00 gate and add the CLOCK, CLEAR, and LOAD nets to the 74F162, as shown below.



2. Choose **Place – No Connect** to add No Connect symbols to all unconnected pins of the 74F162 part (except pin 15).



All pins with No Connect markers are ignored during design rule checking.

**Note:** To remove a No Connect symbol, choose **Place – No Connect** and click on an existing No Connect symbol already set on a pin in the schematic.

3. Save the design.

## Auto Wire Between Two Points

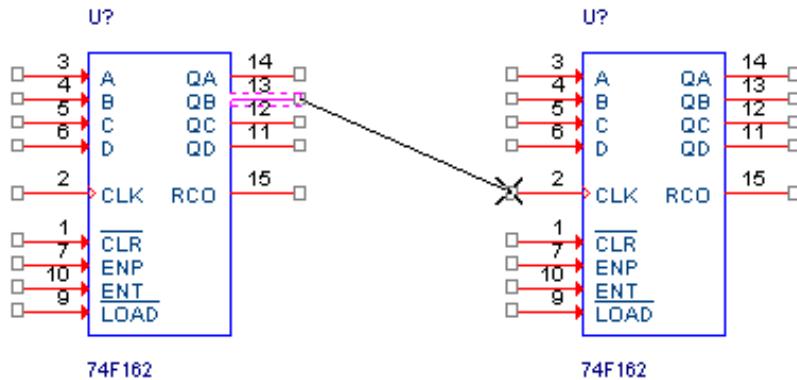
1. In another part of the page, add two more 74F162 parts.

You can copy and paste the part if you prefer.

2. Choose **Place – Auto-Wire – Two Points** or click the **Auto Connect Two Points** icon.



3. Select two pins you want to connect.



A connection is added between the selected pins.

4. Continue to experiment with the Auto Connect Two Points command. When you are finished experimenting, delete the two new 74F162 parts and wires.
5. Save the design.
6. Close the **Place Part** tab.



## Lab 5-4 Assigning Reference Designators

**Objective:** To manually and automatically assign reference designators.

---

### Manual Assignment

1. Click on the temporary reference designator **U?** of the 74F162 part.
2. **Right-click** and select **Edit Properties**.
3. In the Properties Editor window, enter **U1** in the *Value* field and click **OK**.
4. Click anywhere on the schematic page to deselect the reference designator text.
5. Notice the reference designator you assigned is underlined.  
This means that it is a manually assigned designator.
6. Save the design.

### Automatic Assignment

1. In the Project Manager window, select the design file **project1.dsn**.
2. Choose **Tools – Annotate** (or click the icon in the main toolbar). 
3. In the Action section, select **Incremental Reference Update**.
4. Click **OK** and **Yes** to continue.
5. Click **OK**.  
Your design is annotated and saved.
6. View the auto-assigned reference designator (U2A). Notice that the manually assigned reference designator was not changed because you ran the annotation program in incremental mode.

**Important:** The **Options – Preferences – Miscellaneous** tab contains an Auto Reference checkbox, which is currently disabled. When selected, this option automatically assigns a reference designator as you add each part to the schematic.



## Lab 5-5 Running Design Rules Check

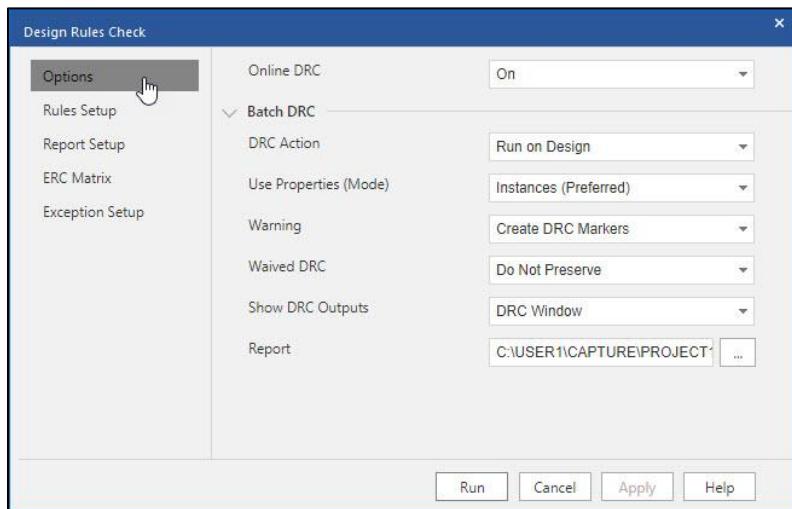
**Objective:** To verify design rules and correct violations.

1. In the Project Manager window, select the design file **project1.dsn**.
2. Choose **PCB – Design Rules Check** (or click the icon in the main toolbar).

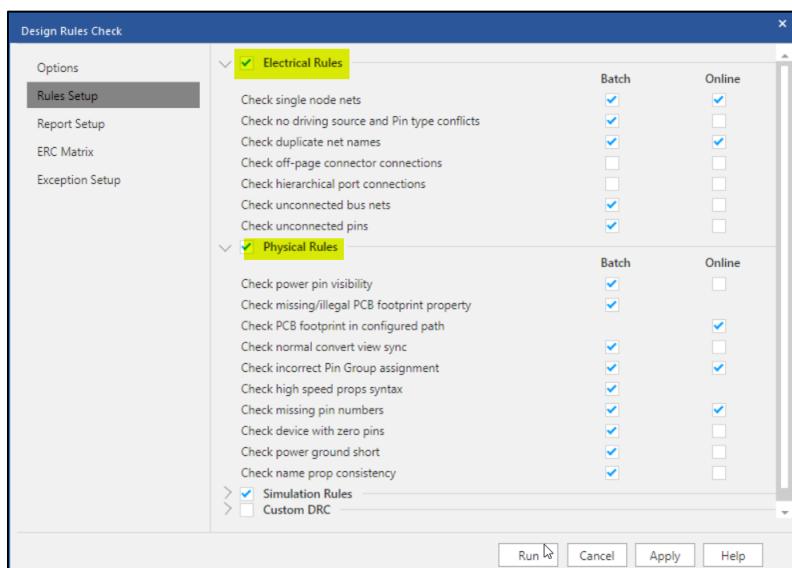
The Design Rules Check window opens.



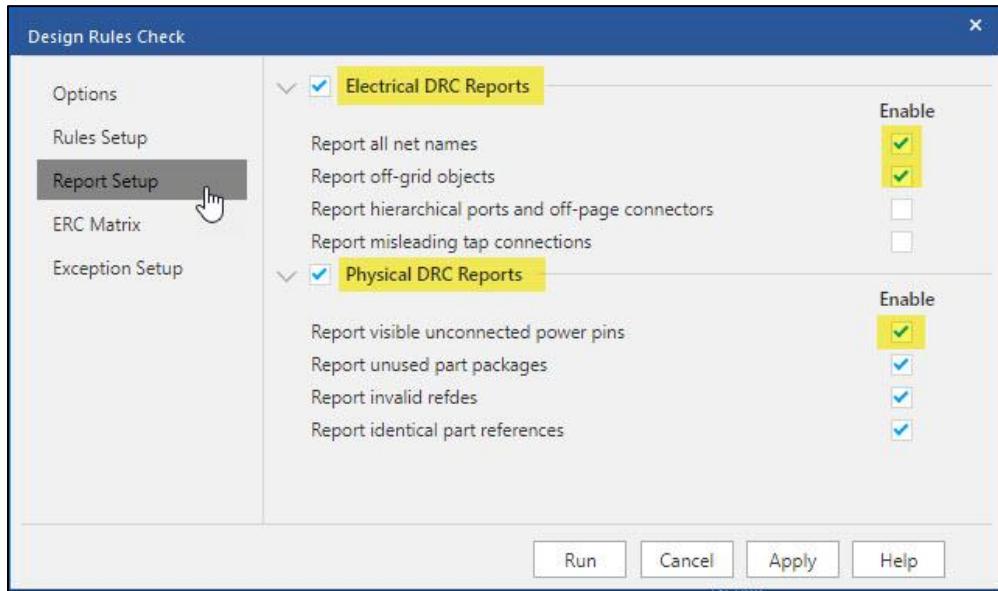
3. In the **Options** tab, make sure the following options are selected.



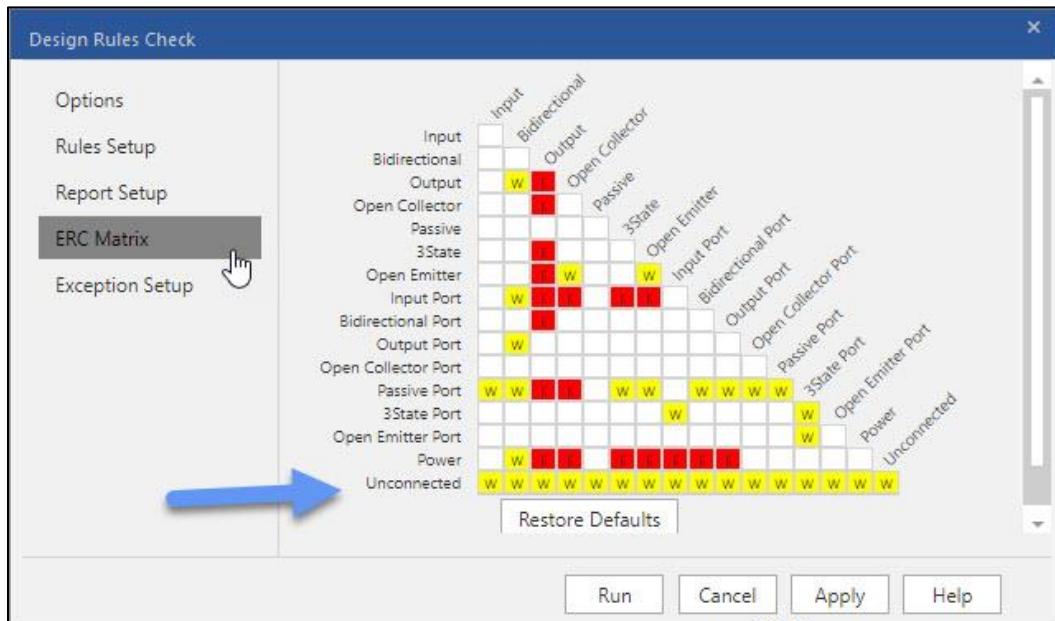
4. Click the **Rules Setup** tab and examine the list of electrical and physical rules. Notice that each rule has a checkbox for batch and online checking.



5. Click the **Report Setup** tab and set the options, as shown below.



6. Click the **ERC Matrix** tab and set the matrix buttons along the bottom row to **W**, as shown below.



This change will flag all unconnected pins as warnings (when they are not marked with a No Connect symbol).

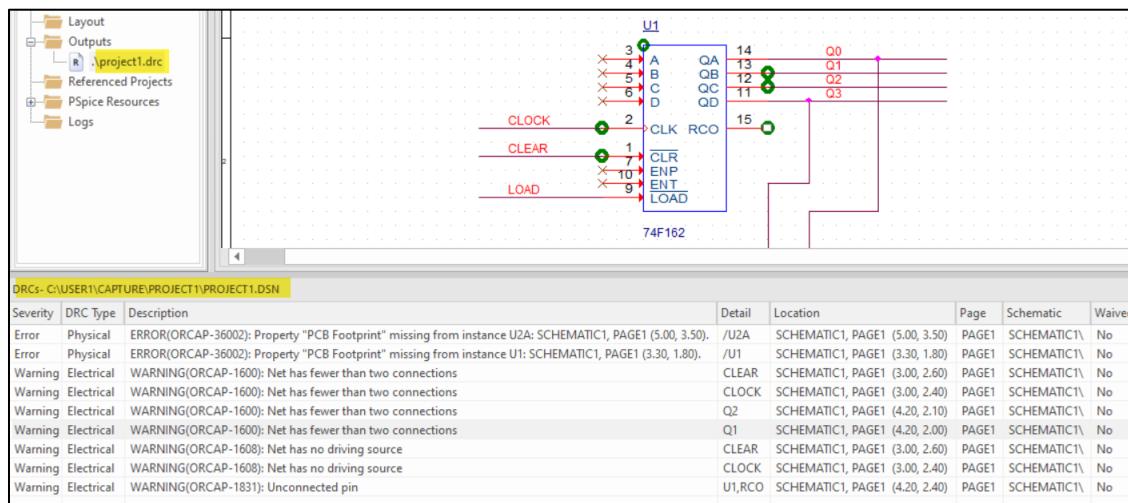
7. Click **Run** to check the schematic.
8. When prompted to view error messages in the session log, click **No**.

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## Building a Simple Schematic

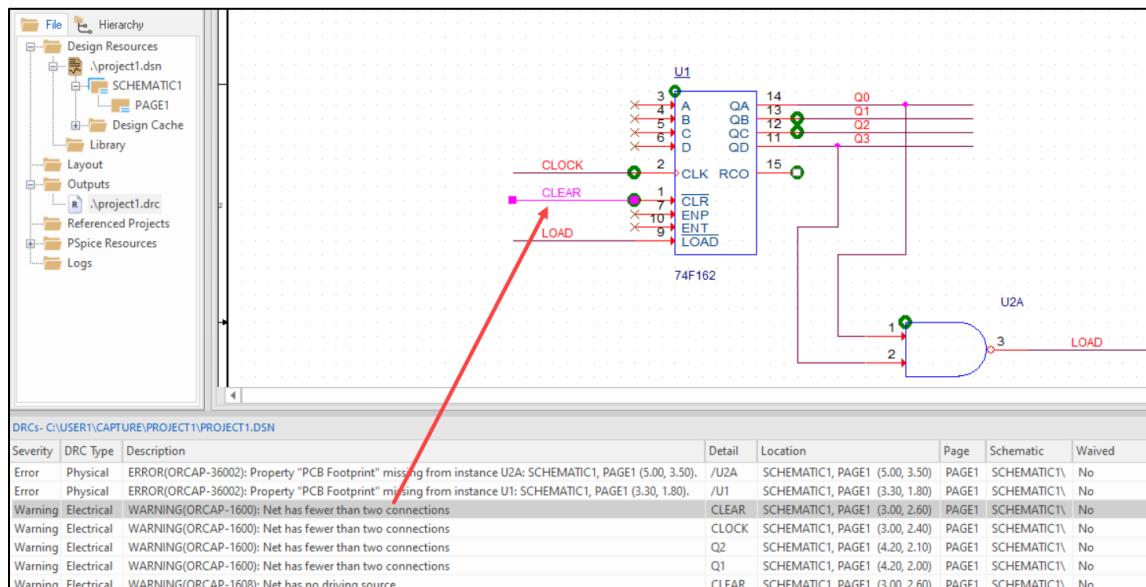
9. Notice a DRC window is displayed along the bottom of the Capture work area.

Several errors and warnings are shown below. The same information is also in *project1.drc* report file, listed under the Outputs branch in the Project Manager.

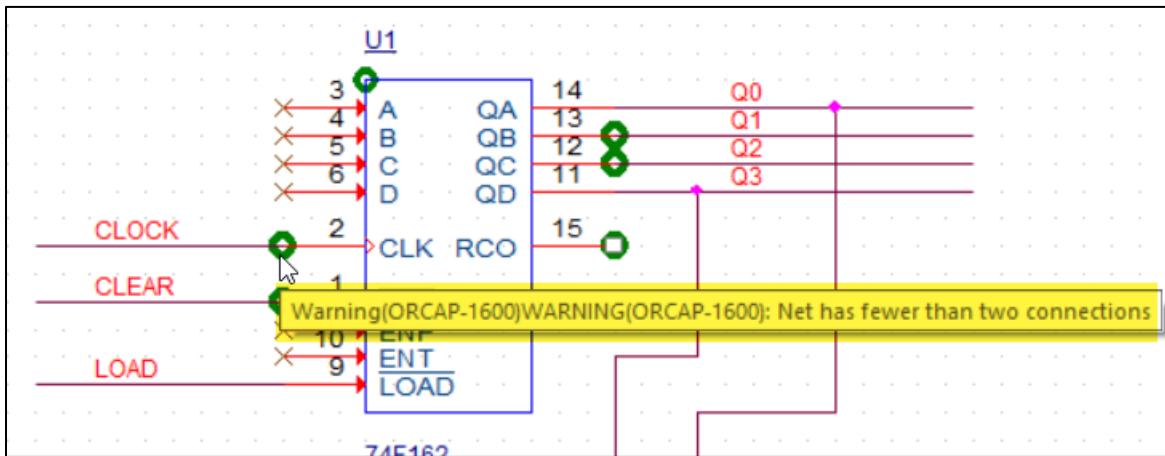


The DRC window contains warnings for an unconnected pin, nets with no driving source, and nets with fewer than two connections (one-pin signals).

10. Double-click on an error in the DRC window and see it highlighted in the schematic.



11. Notice the errors are also flagged with DRC markers on the schematic page. Just hover your cursor over a DRC marker to see a tooltip describing the error.



These DRC markers were added when you ran DRC. You can also **double-click** on a DRC marker to get more information.

### Fixing the Unconnected Pin Warning

1. Choose **Place – No Connect** and add a No Connect symbol on pin **15** of the 74F162.
  2. Press **Esc**.
  3. Save the design.
  4. Choose **PCB – Design Rules Check** and click **Run**.
  5. Click **No** to skip the session log messages.
  6. In the schematic, notice that the error marker on U1 pin 15 has been cleared.  
You used the No Connect symbol to notify the error checker that the pin was intentionally left unconnected.
  7. Close the schematic window.
- The remaining errors are addressed later in the course.

### Closing the Project

1. Choose **File – Close** to close the project.
- The Capture session window is still running.



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# **Module 6: Building a Multi-Sheet Schematic**

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## Lab 6-1 Creating a New Project

**Objective:** To create a new project for a multi-sheet design.

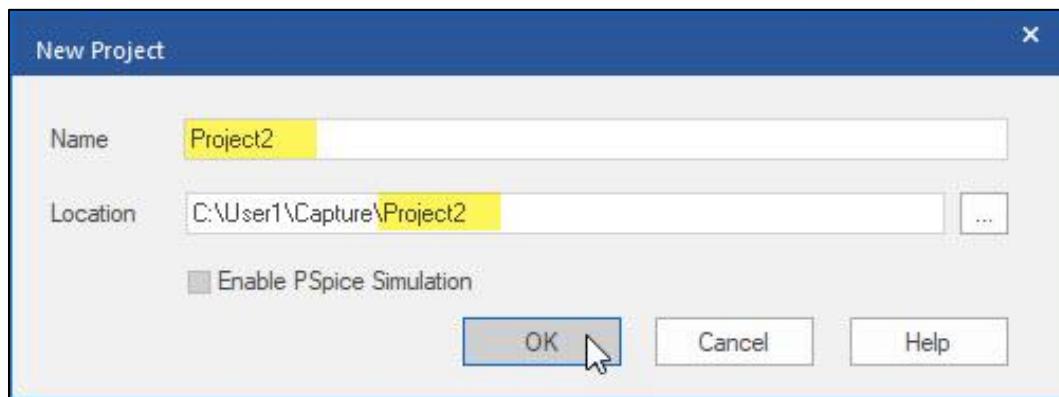
---

### Editing the Design Template

1. Choose **Options – Design Template**.
2. In the **Title Block** tab, enter **Project2** in the Title field and click **OK**.

### Setting Project Name and Location

1. Choose **File – New – Project**.
2. In the Name field, enter **Project2**.
3. To specify a location for the new project, click **Browse**.
4. In the Select Directory window, double-click to navigate to the *C:\User1\Capture* directory.
5. Click the **Select Folder** button.
6. Add the **Project2** folder to the end of the project location path, as shown below.



**Important:** Always replace the *User1* variable with the actual path to the *Capture* folder on your system.

7. Click **OK**.  
The New Project Wizard creates the project and opens a blank page.

## Viewing the Title Block

1. Close the DRC window.
2. Click in the schematic window to make it active and resize this window.
3. Click the **Zoom to all** icon.  
Notice that the data in the title block reflects the change you made to the design template.
4. Click the **Zoom Out** icon.

## Viewing the System Files

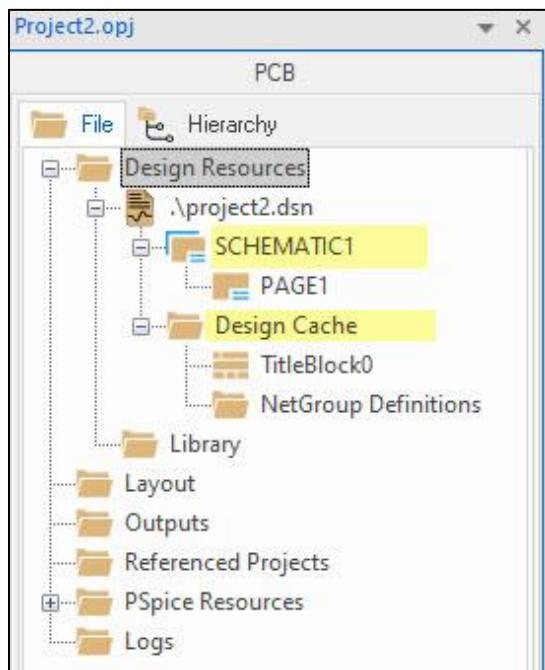
1. In Windows Explorer, navigate to the directory *C:\User1\Capture\Project2*.
2. Notice the following files in the project directory:
  - *PROJECT2.DSN* (binary design file)
  - *Project2.opj* (ASCII project file)
3. Close Windows Explorer.

## Viewing the Design Resources

1. Click in the Project Manager window to make it active.
2. Click the plus sign (+) to the left of *project2.dsn*.
3. Click the plus sign (+) to the left of *SCHMATIC1*.  
The schematic folder expands to show *PAGE1*.

4. Click the plus sign (+) to the left of the Design Cache.

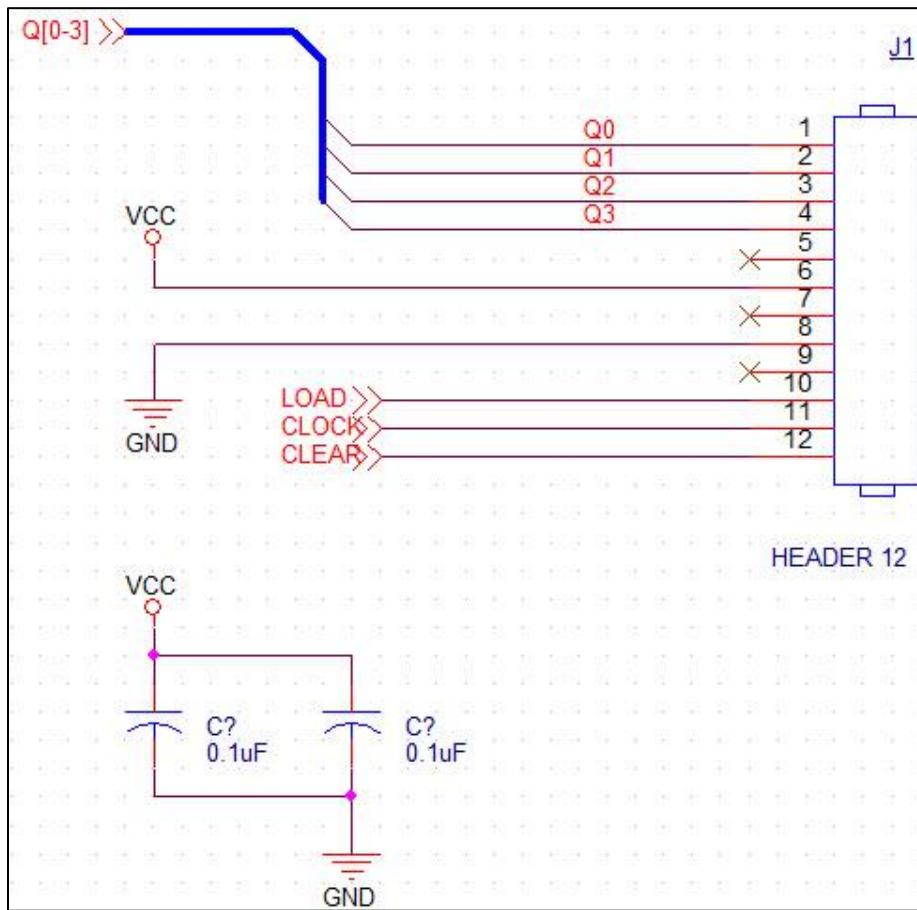
The Design Cache branch expands to show the parts that have been added to the design. The only symbol currently in the design is *TitleBlock0*.



End of Lab

**Lab 6-2 Creating Page1****Objective:** To create the first page of a multi-page schematic.

Use this illustration as a guide to complete the steps in this lab.

**Adding a 12-Pin Header Connector**

1. Make sure the schematic window is active. Click the **Place Part** icon on the schematic toolbar (or press **p**). 
2. In the Search for Part section, make sure the library Path field (located at the bottom of the dialog box) shows the following installation path and library directory:

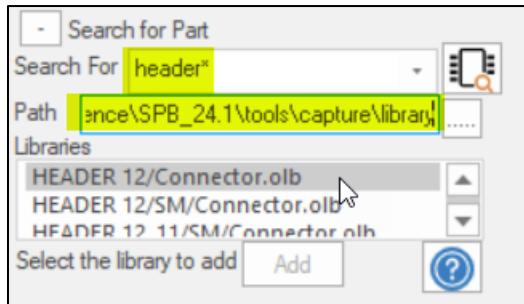
```
$CDSROOT\tools\capture\library
```

Replace the **\$CDSROOT** variable with the path to where the Cadence® software is installed (for example, *C:\Cadence\SPB\_24.1*). If the path is not correct, click the browser button to correct the path.

3. In the Search For field, enter **header\*** and click the **Part Search** icon.

Capture locates many different headers in a *CONNECTOR* library.

4. Scroll down the Libraries list and **double-click HEADER 12/Connector.olb**.



The *CONNECTOR* library has been added to the Libraries list, and the HEADER 12 part is attached to your cursor.

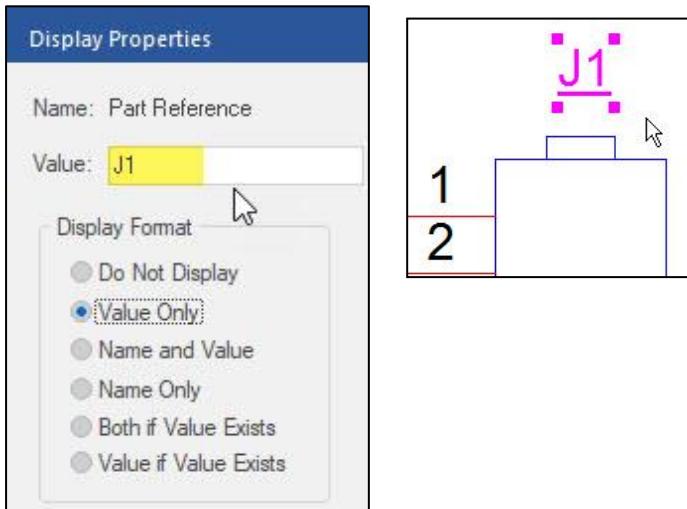
5. Click to place the connector on the page, press Esc to quit the command, and deselect the part.
6. Close the **Place Part** tab.

### Mirroring the Connector

1. Select the connector part, **right-click** and select **Mirror Horizontally**.  
The connector pins should now be facing to the left.
2. Click in an open area to deselect the part.

### Assigning a Part Reference

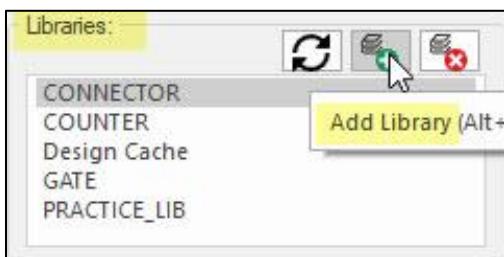
1. Select the Part Reference text for the connector (J?), **right-click** and choose **Edit Properties** (or **double-click**).
2. In the Property Editor window, change the Part Reference field to **J1** and click **OK**.



3. Press **Esc** to deselect the text.
4. Notice the underlined Part Reference indicating a user-assigned value.
5. Choose **File – Save**.

## Adding Decoupling Capacitors

1. Click the **Place Part** icon (or press **p**).
2. In the Libraries section of the Place Part pane, click the **Add Library** icon.



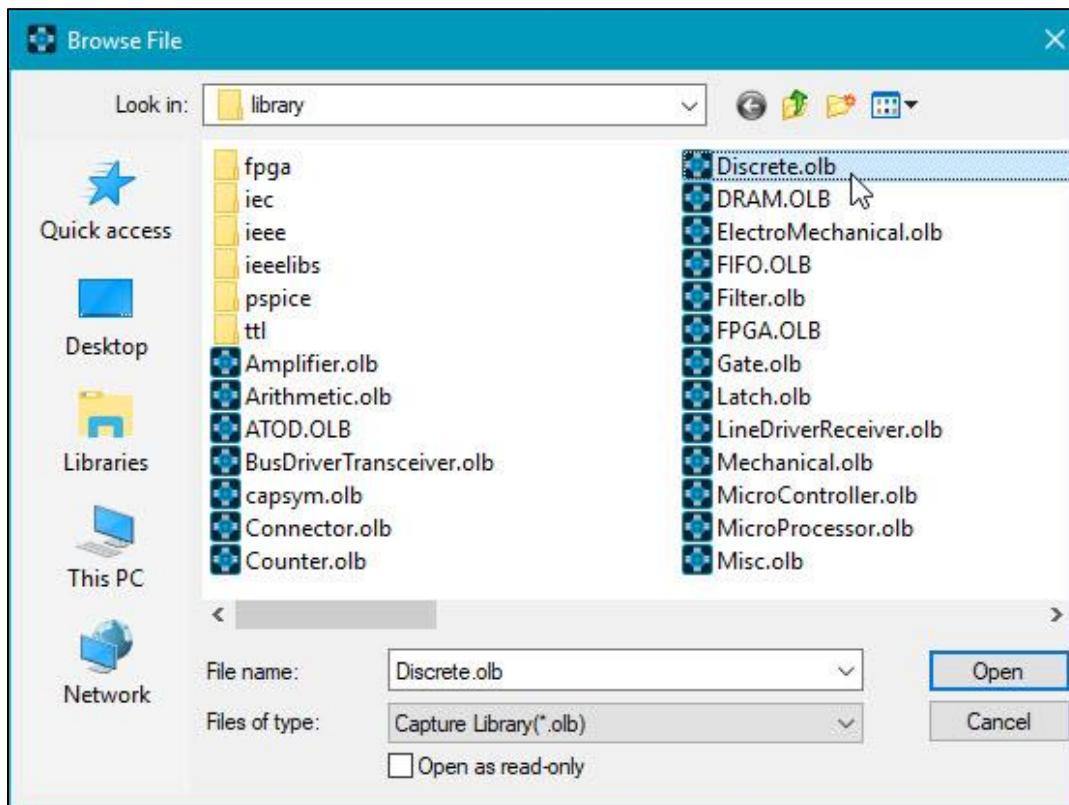
The Browse File window appears.

3. In the Look in field, navigate to the following library directory:

`$CDSROOT\tools\capture\library`

Replace the `$CDSROOT` variable with the path to where the Cadence software is installed.

4. Select the **Discrete.olb** library and click **Open**.



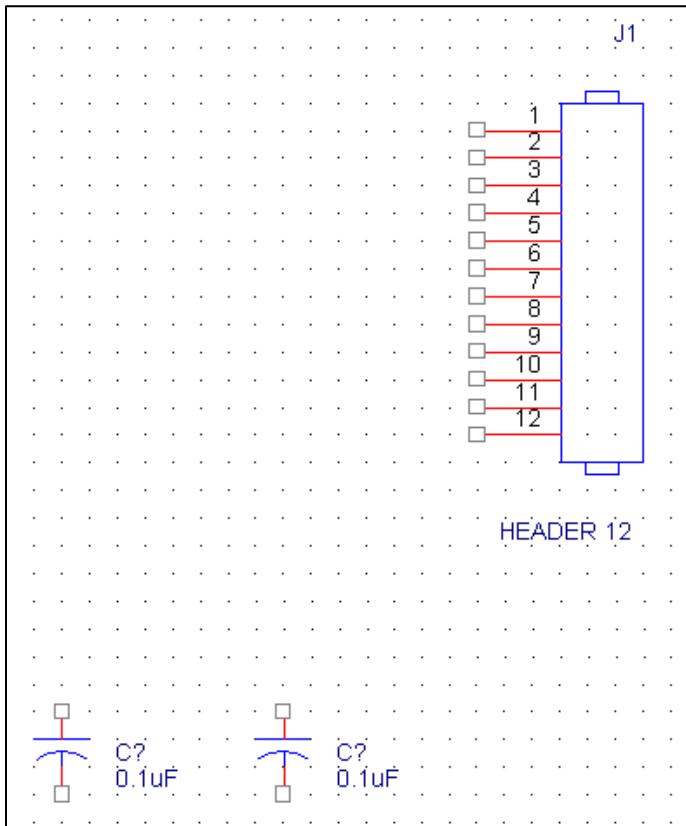
The *DISCRETE* library is added to the Libraries list, and all the parts in this library are listed in the Part List.

5. In the Part field, enter **cap**.
6. **Double**-click to select the **CAP** from the Part List – but do *not* place the part yet.
7. **Right**-click and select **Edit Properties**.
8. In the Part Value field, enter **0.1uF** and click **OK**.
9. Click to place the capacitor in the design.

You can place both capacitors now or follow the steps in the next procedure, *Copying the Capacitor*.

### Copying the Capacitor

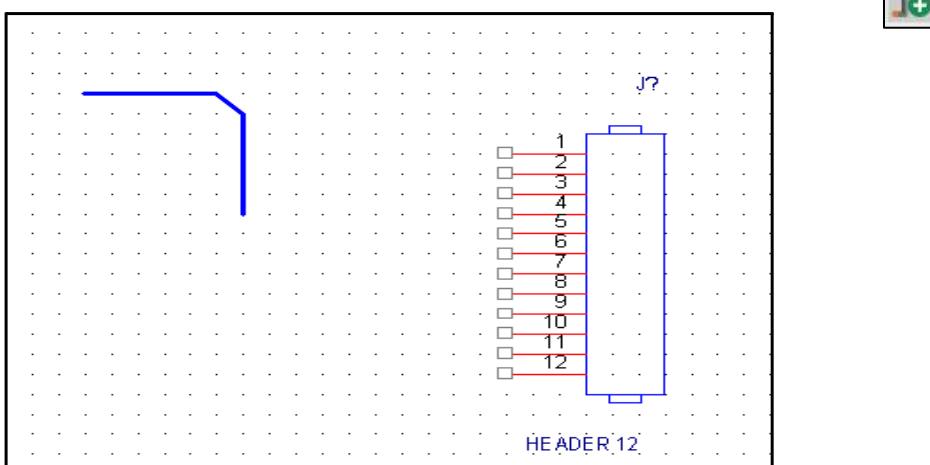
1. Select the capacitor, then **Ctrl+left** drag to copy the capacitor to a new location.



2. Choose **File – Save**.
3. Close the **Place Part** tab.

## Drawing the BUS Wire

1. Use the **Place – Bus** command or icon to draw a bus wire, as shown below. Leave 10-12 grid spaces to the connector.

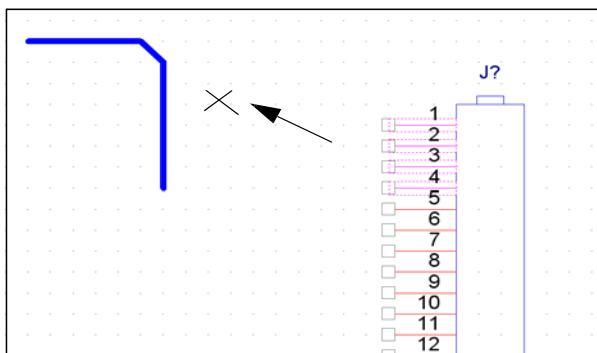


**Tip:** To angle the bus wire, press **Shift** when drawing.

## Adding BUS Connections

1. Choose **Place – Auto Wire – Connect to Bus** or click the **Auto Connect to Bus** icon.

The route pointer appears.



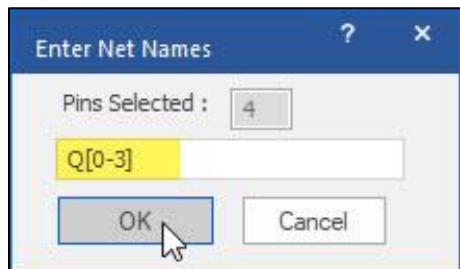
2. Click pins **1-4** of the connector. Click the bus you drew to the left of the connector. The wires and bus entries to the bus are drawn for you.



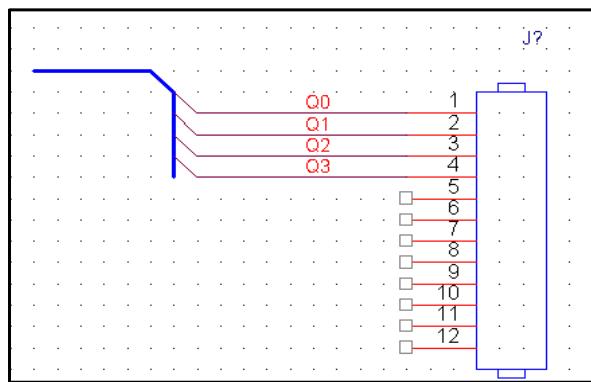
## Building a Multi-Sheet Schematic

The Enter Net Names window appears.

- Enter **Q[0-3]** and click **OK**.



The auto-connected nets are annotated.



### Alternate Method to Drawing Bus Connections

- Delete all the wiring you just added, including the thick bus wire.
- Use the skills you've learned to add four wires to the connector. Name them Q0 through Q3.

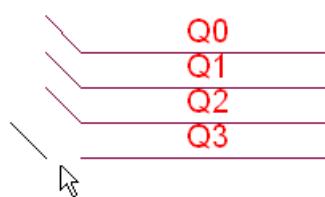
**Tip:** Remember the F4 key repeats the last drawn wire, and a net name will automatically increment if it ends with a number.

- Click the **Place Bus Entry** icon.

A bus entry symbol is attached to your cursor.



- Click to add bus entries to the ends of the Q0–Q3 signals.



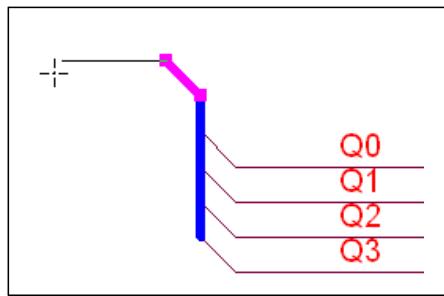
After placing the first bus entry symbol, you can press **F4** repeatedly to place more; place the first bus entry symbol, press **Esc**, and then **F4** to repeat.

5. Click the **Place Bus** icon.



6. Click to add a bus wire to the ends of the bus entries.

Press **Shift** while drawing any wire or polyline to add diagonal segments.



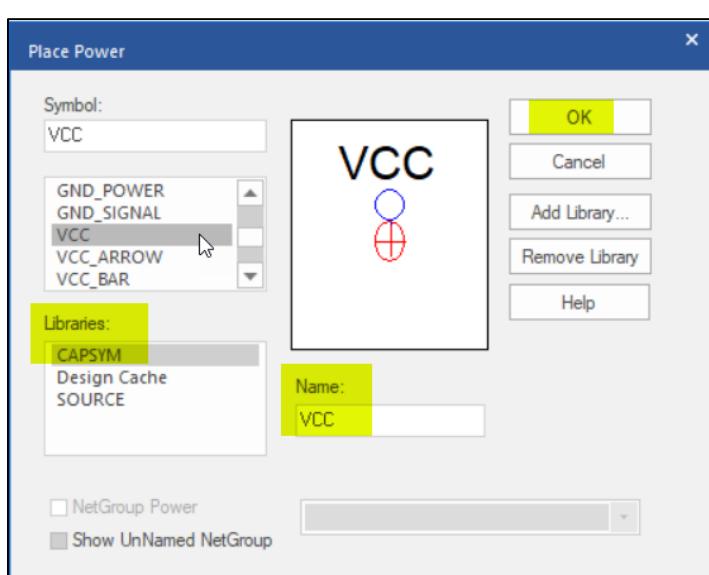
7. Save the design.

## Adding Power and Ground Symbols

1. Click the **Place Power** icon.



2. In the Libraries section of the Place Power window, click **CAPSYM**.
3. Select the **VCC** symbol from the CAPSYM library and click **OK**.



4. Add two VCC symbols to the schematic.

5. Click the **Place Ground** icon.

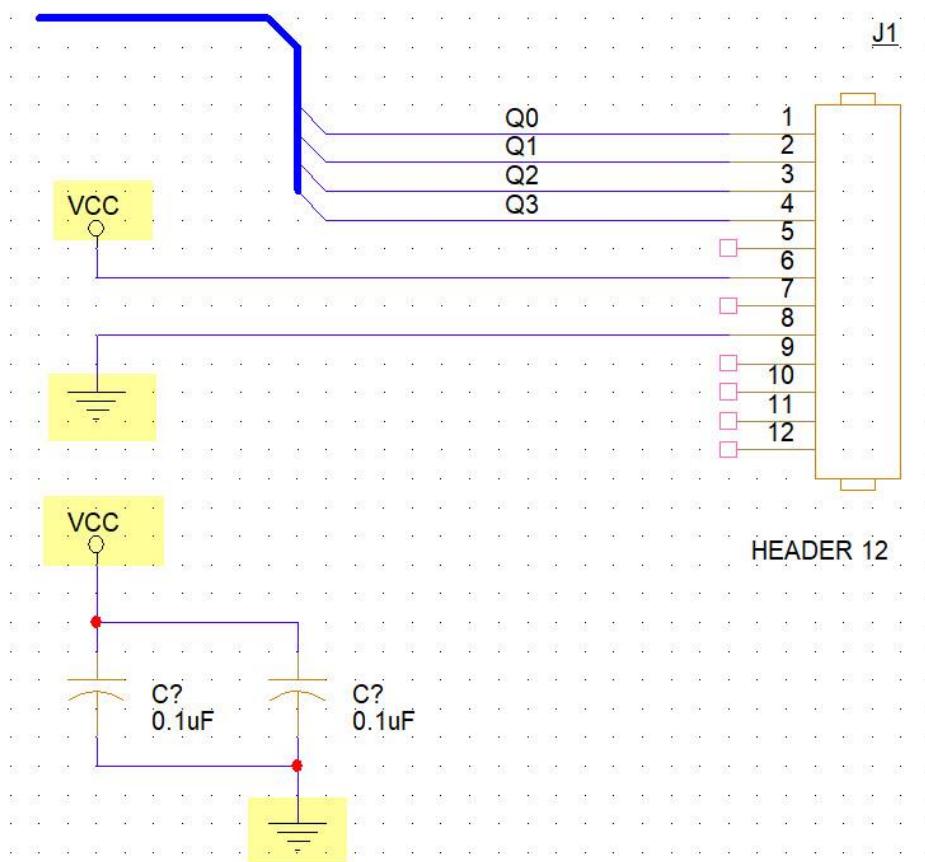


6. Select the **GND** symbol and click **OK**. Place two GND symbols in the schematic.

7. Press **Esc** to exit the command. Press **Esc** again to deselect all parts.

8. To move a power or ground symbol, hold the left mouse button and drag the symbol to a new location. To copy it, use **Ctrl+left** drag.

9. Connect the power and ground symbols to the connector and the capacitors, as shown in the example below.



10. Save the design.

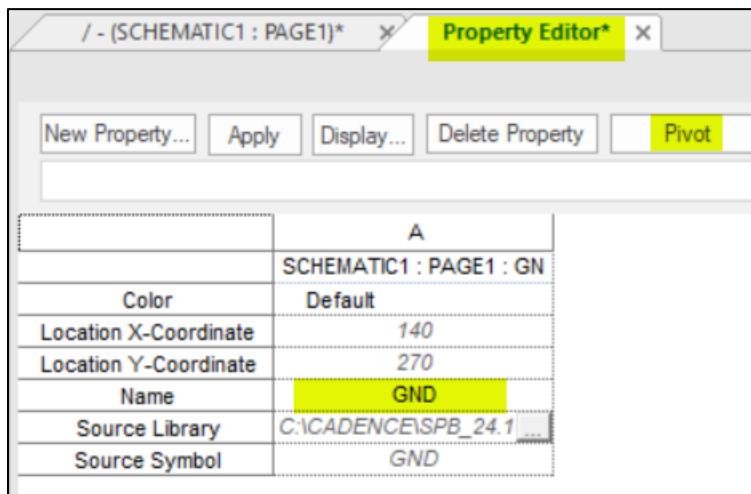
## Making Ground Symbol Names Visible

1. Select a **GND** symbol. Right-click and select **Edit Properties**.

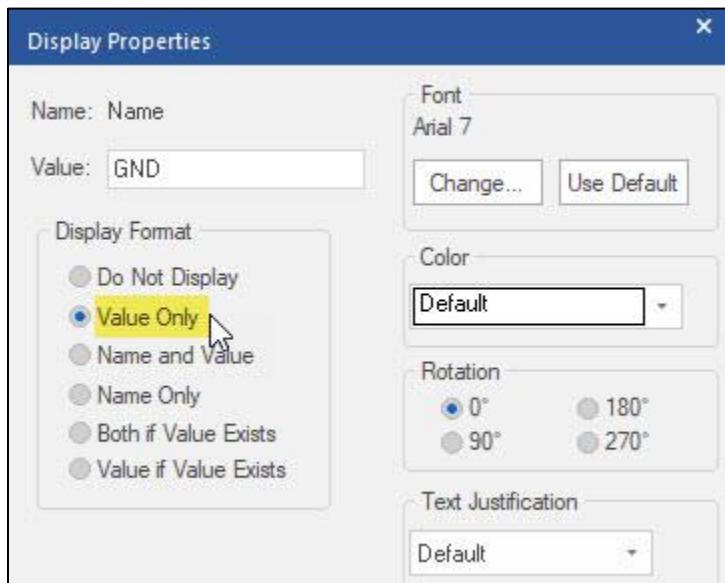
You can also **double**-click on a part or symbol to access the Property Editor.

2. In the Property Editor, pivot the table so that each property is displayed in a separate row.

3. Select the **GND** name as shown and click the **Display** button.



4. In the Display Properties window, select **Value Only** and click **OK**.



Building a Multi-Sheet Schematic

5. Close the **Property Editor** window and deselect the symbol.

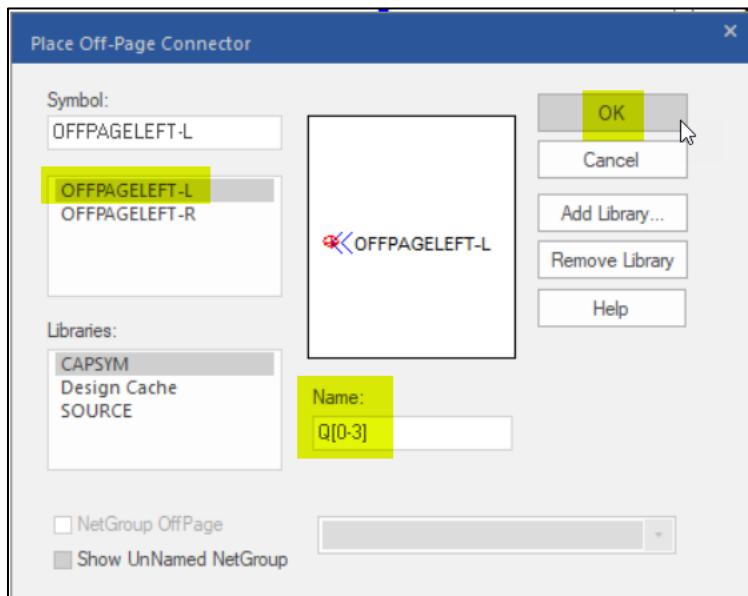


### Adding an Off-Page Connector

1. Click the **Place Off-Page Connector** icon.

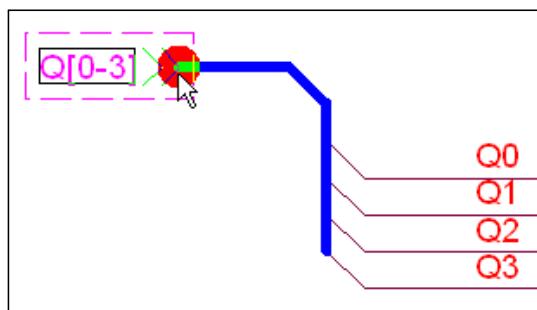


2. In the Off-Page Connector window, select the *CAPSYM* library and click **OFFPAGELEFT – L** from the list.
3. In the Name field (at the bottom), enter **Q[0-3]** and click **OK**.



The off-page connector is attached to your pointer.

4. To rotate the symbol, press **r**. Press twice to rotate it 180 degrees and click to attach it to the end of the bus wire.



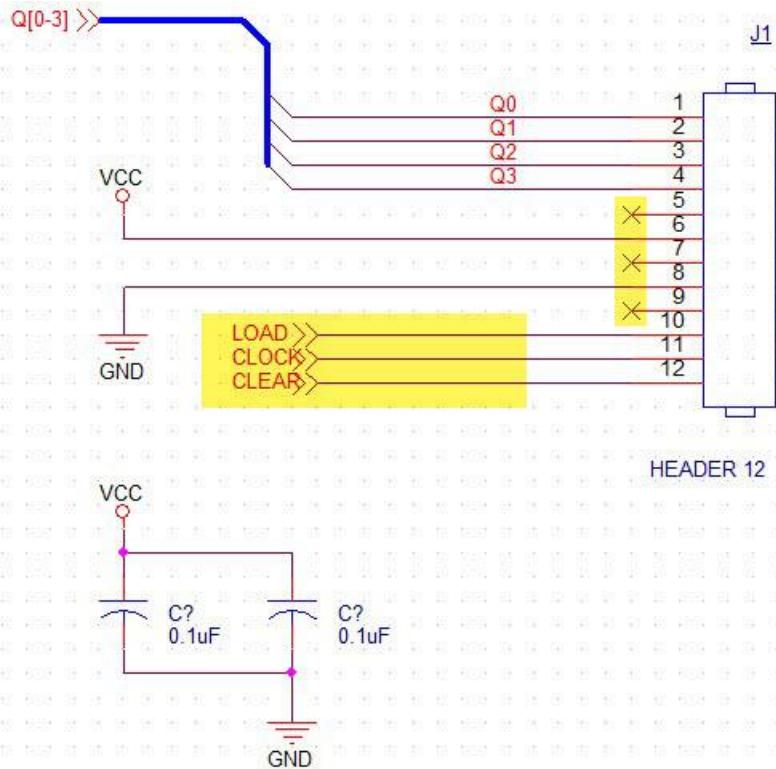
5. Press **Esc** to exit the command. Press **Esc** again to deselect the off-page connector.

## Completing the Schematic

1. Add wires for the LOAD, CLEAR, and CLOCK nets to the connector, as shown below, and add off-page connectors to these nets.  
**Tip:** There is an easy way to change the name of an off-page connector while it is attached to your cursor. **Right-click** and select **Edit Properties**.

2. Place no-connect symbols on all unconnected pins of the HEADER 12 part.

Compare your results to the example below.

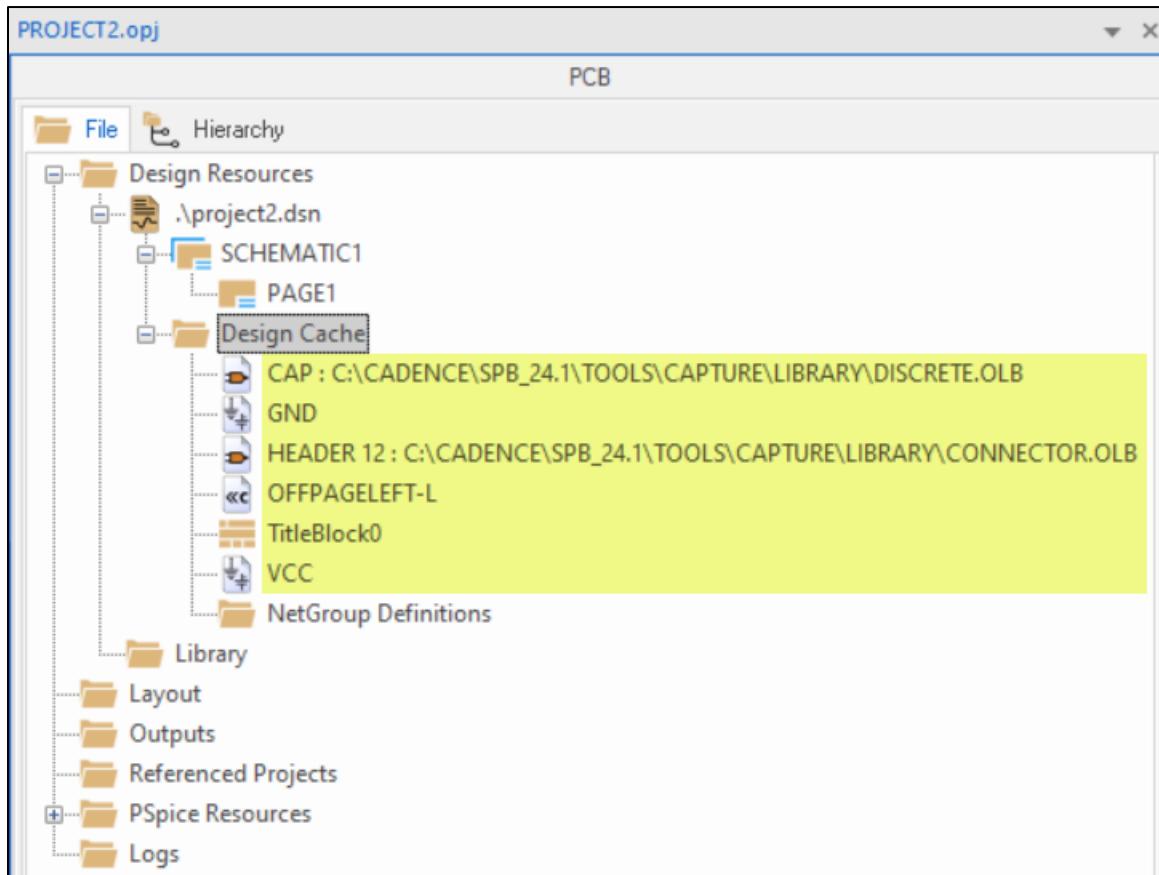


## Saving and Closing the Schematic

1. Choose **File – Save**.
2. Choose **File – Close**.  
Do not close the Project Manager window.

## Viewing Design Cache

1. In the Project Manager window, notice the list of parts under the Design Cache folder. This list represents all the parts that have been added to this design so far.



2. Click the minus sign (-) to the left of the Design Cache folder to collapse the display.

Do not close the project.



## Lab 6-3 Copying from One Design to Another

**Objective:** To copy a schematic page from another design.

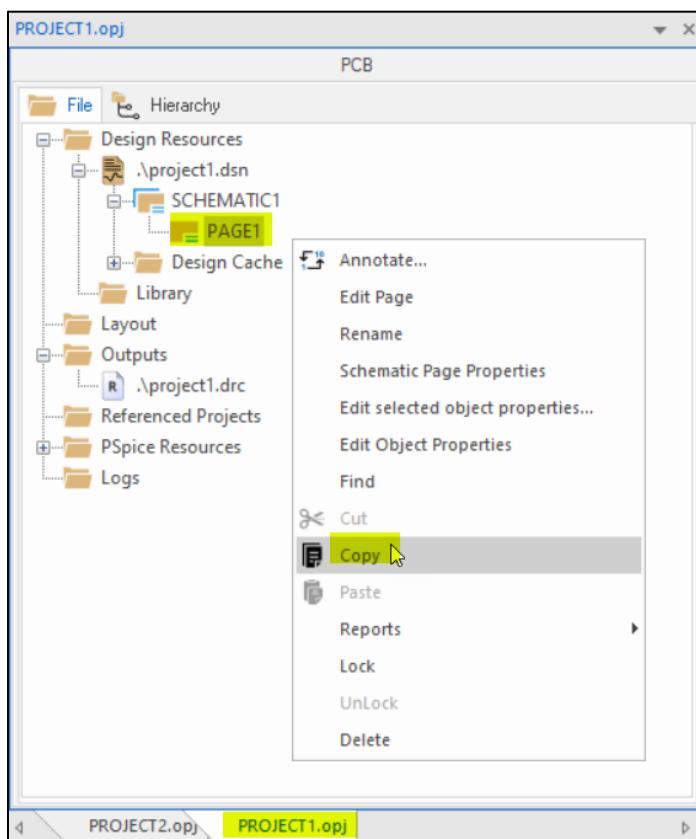
### Opening Two Projects at Once

Project2 should still be open from the previous lab. You will reopen Project1 so you can copy a schematic page.

1. Choose **File – Open – Project**.
2. In the Open Project window, navigate to this directory *C:\User1\Capture\Project1* and select **Project1.opj**. Click **Open**.

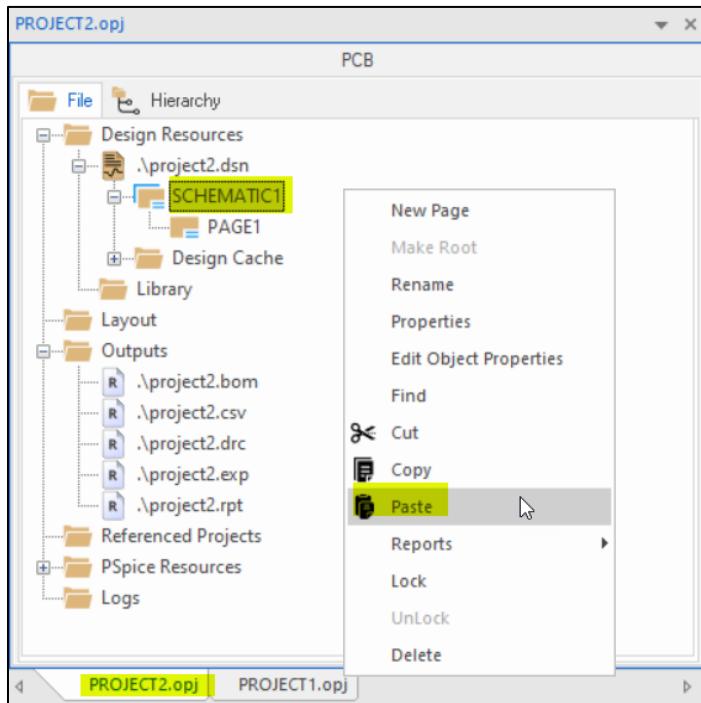
### Copying Between Projects

1. Click on the **Project1** tab at the bottom of the Project Manager window.
2. Right-click the **PAGE1** entry in the **SCHEMATIC1** folder and select **Copy** (or press **Ctrl+C**).

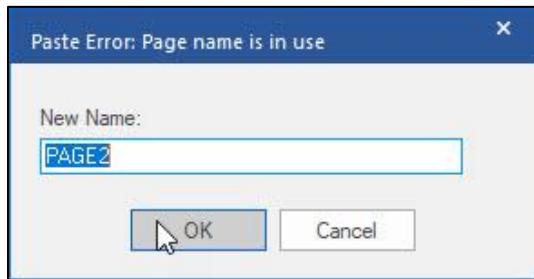


### Building a Multi-Sheet Schematic

- Click on the **Project2** tab, right-click the **SCHEMATIC1** folder, and select **Paste** (or press **Ctrl+V**).



The Paste Error window prompts you to rename the pasted page because the Project2 schematic already contains PAGE1.



- Click **OK** to accept PAGE2 as the new name.

### Saving Project2

- In the Project Manager window, select **project2.dsn** and choose **File – Save**.

### Closing Project1

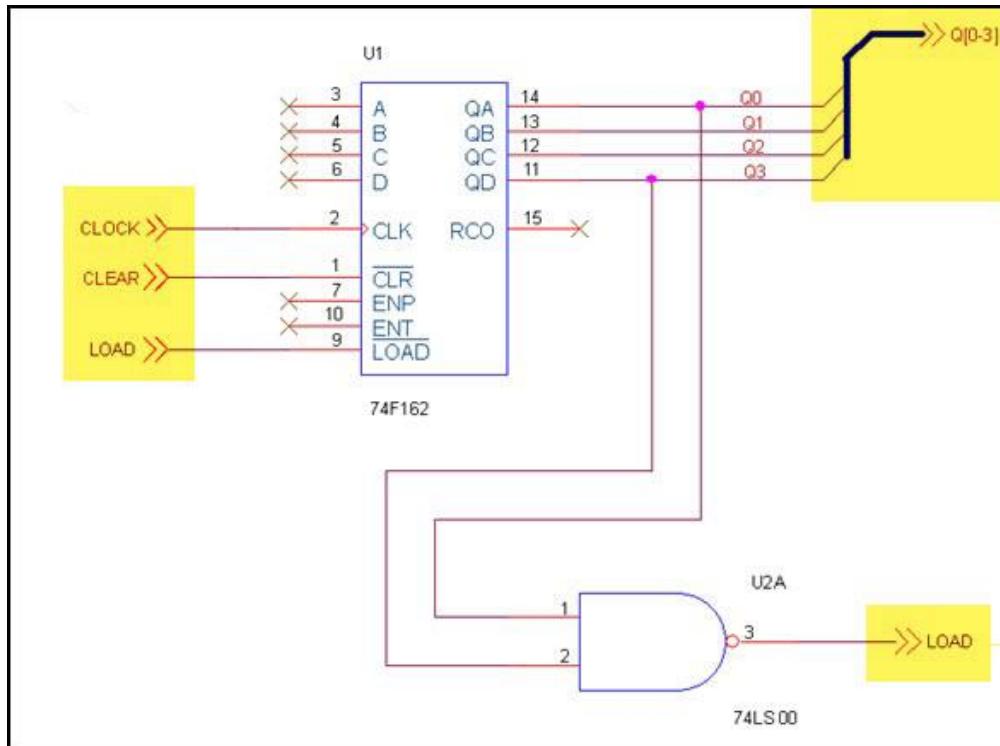
- Click on the **Project1** window tab and choose **File – Close**.



## Lab 6-4 Completing the Schematic

**Objective:** To modify the copied page.

This is the schematic page you copied. You will make changes in the highlighted areas.



### Modifying the Copied Page

1. Double-click on PAGE2 of the Project2 schematic.

This is the page you just copied from Project1.

2. Add bus entries to the Q0 through Q3 nets.

Press the **r** key to rotate the bus entry symbols to the correct position.

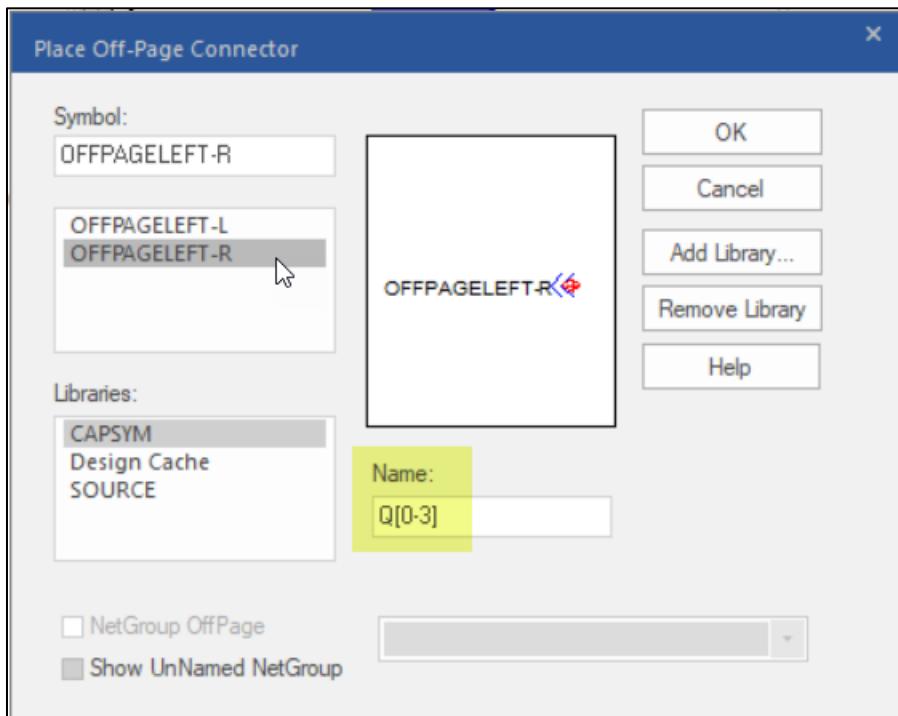
3. Add a bus wire to bundle the Q0–Q3 bus entries together.

**Tip:** Press **Shift** to draw a diagonal bus wire.

## Building a Multi-Sheet Schematic

4. Choose **Place – Off-Page Connector** to add an off-page connector to the end of the bus wire.

- a. Use the **OFFPAGELEFT-R** symbol from the *CAPSYM* library and rotate it to the correct position. Make sure you name the off-page connector with the correct syntax.



5. Add off-page connectors to the CLOCK, CLEAR, and LOAD nets.

The LOAD net has two off-page connectors (see illustration above). You must use both types of off-page symbols on this net, and each one must be named and rotated.

6. Notice that the CLOCK, CLEAR, and LOAD wires contain both net aliases and off-page connector names. It is recommended that you delete the wire aliases because the off-page connector names take precedence.
7. Zoom in to the title block and **double-click** the **Project1** title.  
The Display Properties window opens.
8. Change the Title property value to **Project2** and click **OK**.

## Saving the Design

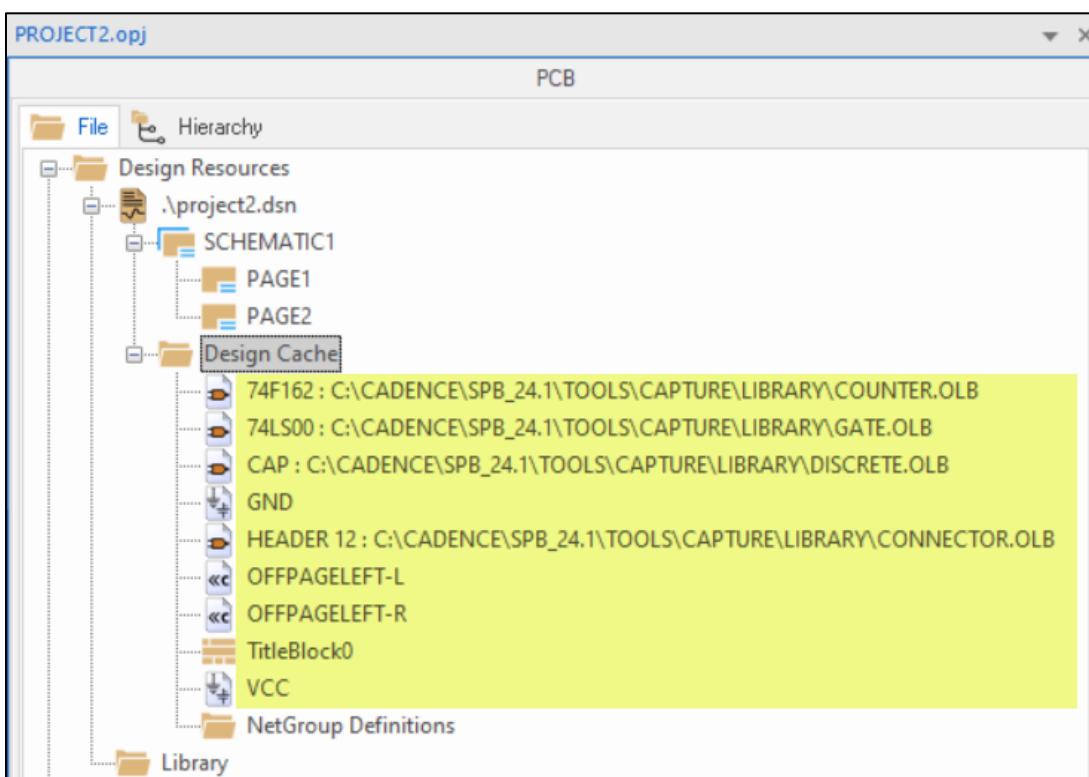
1. Click the **Zoom to all** icon.
2. Choose **File – Save**.

## Closing the Schematic

1. Choose **File – Close** to close the schematic window.

## Viewing Design Cache

1. In the Project Manager, click the plus sign (+) next to the Design Cache folder and examine the list of parts.
2. Notice that this list now includes the parts contained on the copied page.



3. Collapse the Design Cache folder.



## Lab 6-5 Annotating a Multi-Sheet Design

**Objective:** To add reference designators to the design.

---

### Opening the Schematic

1. Double-click to open both pages of the Project2 schematic.
2. Use the page tabs to toggle between **PAGE1** and **PAGE2** and click the **Zoom to all** icons to fit the contents of the work area.
3. Notice that PAGE2 already has reference designators assigned.
4. Also, notice that both pages have title blocks that display *Sheet 1 of 1*.

### Annotating Part References

1. Click in the Project Manager window and select the design name **project2.dsn**.
2. Choose **Tools – Annotate**.
3. In the Action section of the Annotate window, click either **Incremental reference update** or **Unconditional reference update**.  
When you use the Unconditional Reference Update option, all parts are processed (even ones with existing reference designators). This automatically resolves any duplicate reference designator problems that can occur when pages are copied from other designs.
4. Click **OK** to start and **OK** to continue.

### Viewing Results

1. Toggle between PAGE1 and PAGE2.
2. Notice that all parts have reference designators assigned. Also, notice that the title blocks now display *Sheet 1 of 2* and *Sheet 2 of 2*.

## Using Reference Designator Controls

1. Click in the Project Manager window and select the design name **project2.dsn**. Choose **Tools – Annotate**.

This time, we set a range of reference designators for each of the pages.

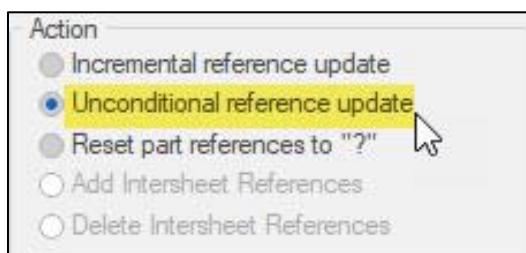
2. Select **Refdes control required** in the top-left corner of the window.



3. In the Scope section, there is a table of schematic pages and a reference designator range you can set for each page.
  - a. For page1, set Start Value to **100** and End Value to **199**.
  - b. For page2, set Start Value to **200** and End Value to **299**.

Scope		Pages	Start Value	End Value
<input checked="" type="radio"/>	Schematic Pages	SCHEMATIC1:PAGE1	100	199
<input type="radio"/>	Hierarchical Blocks	SCHEMATIC1:PAGE2	200	299

4. In the Action section, select **Unconditional reference update**.



5. Click **OK** to annotate the design and **OK** to continue.
6. View the schematic pages to see the results.
7. Click in the Project Manager window and choose **Tools – Annotate**.

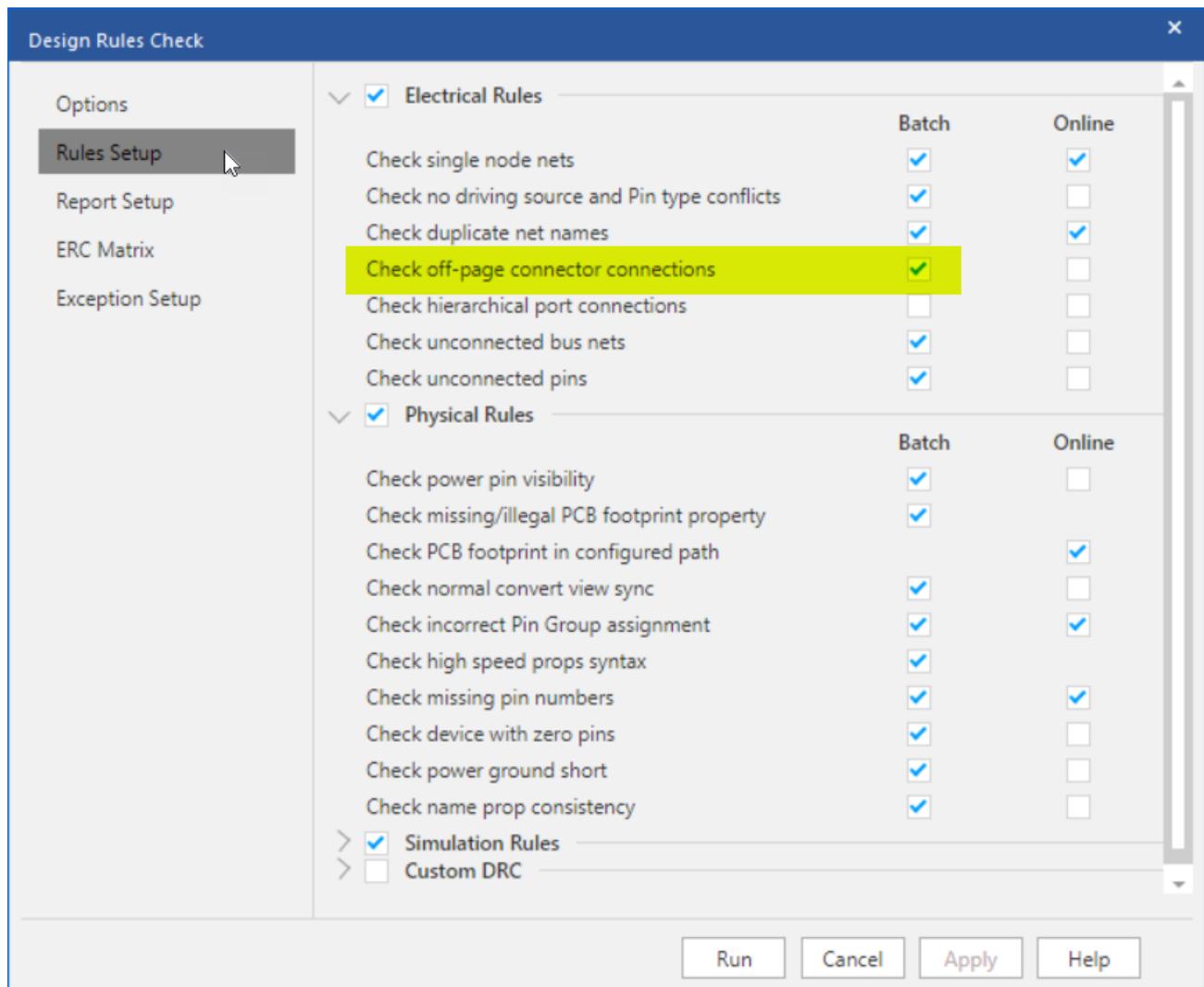
8. Turn off the **Refdes control required** option and annotate the design once more. Remember, the Action must be set to Unconditional Reference Update for your change to take effect.
  
9. Save the design.



## Lab 6-6 Checking the Design for Errors

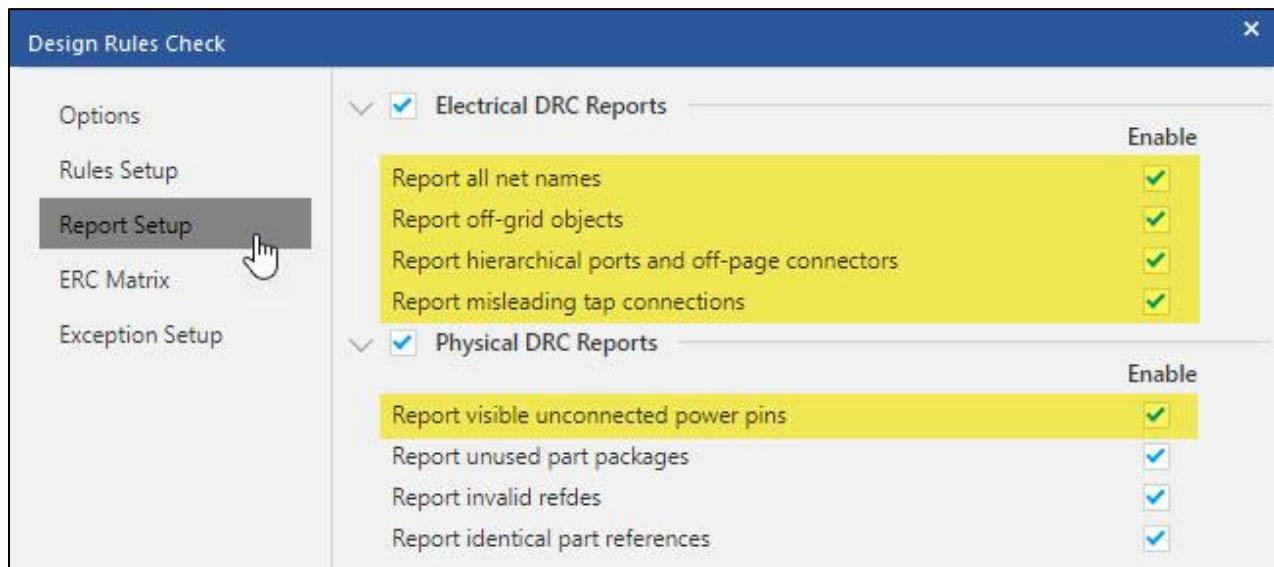
**Objective:** To run a design rule check on a multi-sheet design.

1. Click on the design name in the Project Manager window.
2. Choose **PCB – Design Rules Check**.
3. Click the **Rules Setup** tab and select these electrical and physical rule checks.

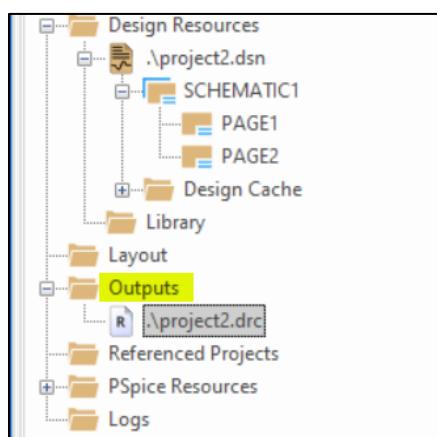


## Building a Multi-Sheet Schematic

4. Click the **Report Setup** tab and select these reporting options.



5. Click **Run** to check the design.
6. Click **No** when prompted to view messages in the session log.
7. Notice the DRC window shows several errors.  
We'll be adding the missing PCB Footprint properties later in the course.
8. Close the DRC window.
9. You can **double-click** to open the DRC report from the Project Manager window.



10. Close the **DRC** report window.



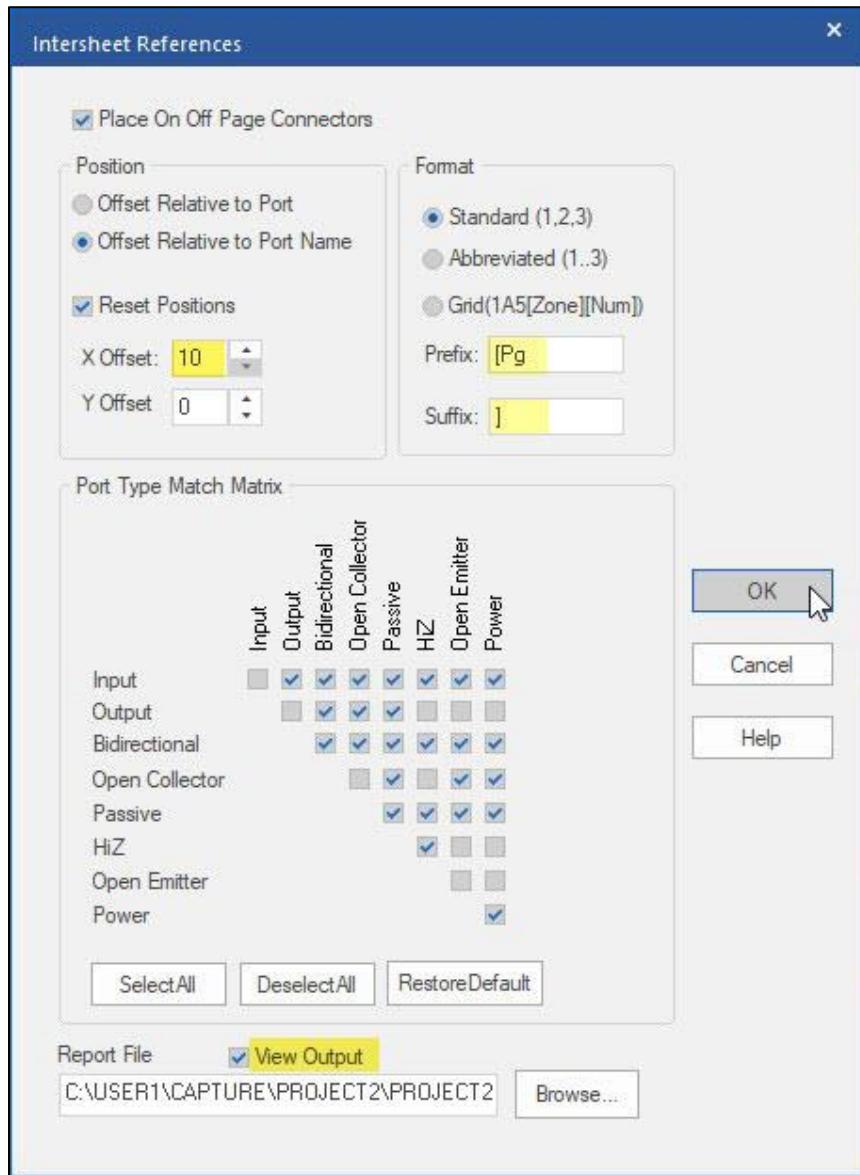
## Lab 6-7 Cross Referencing Multi-Sheet Nets

**Objective:** To add intersheet references for multi-sheet nets.

1. Click on the design name in the Project Manager window and choose **Tools – InterSheet References**.

The Intersheet References window appears.

2. Set the options in the Intersheet References window, as shown below.



The matrix section of the setup window generates intersheet references for hierarchical ports, which are not present in this design.

## Building a Multi-Sheet Schematic

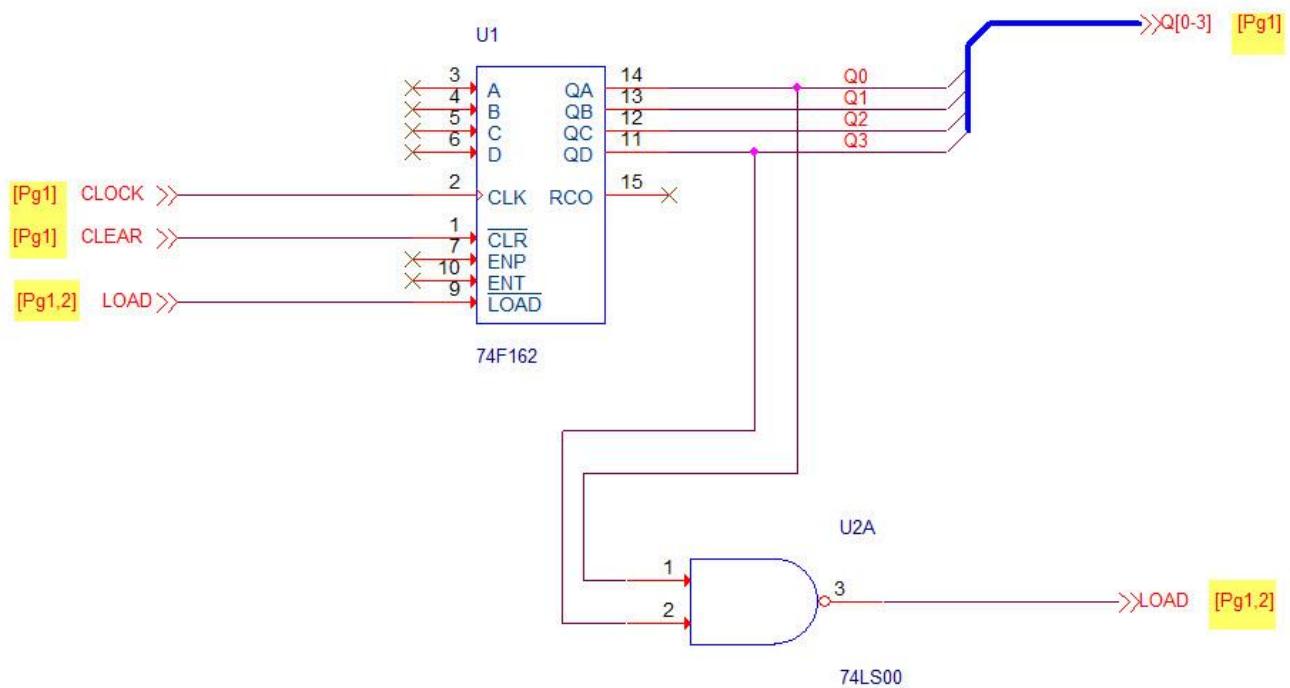
3. Make sure you have the **View Output** switch turned on (at the bottom of the window) and click **OK**.

The Intersheet References report is displayed in Excel. This report shows where each of the nets in the design can be found.

4. View and close the Excel spreadsheet.

You can reopen this report by clicking on the *project2.csv* file in the Outputs folder of the Project Manager window.

5. View the cross-referencing results in the schematic.

**Saving and Closing the Design**

1. Select the design name in the Project Manager window and choose **File – Save**.
2. Close both pages of the schematic.

End of Lab

## Lab 6-8 Searching for Objects in the Schematic

**Objective:** To search for parts and nets in the design.

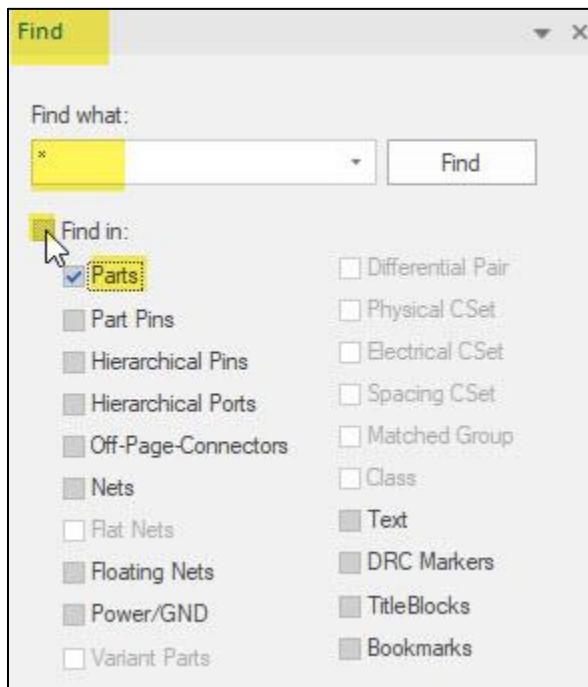
### Searching the Current Page

1. Reopen both pages of the schematic.
2. Click on the page tab to activate PAGE1 of the schematic.
3. Click on the **Search** icon to open the **Find** tab.



You can also **right-click** and select **Find**.

4. Use the **Find in** checkbox to toggle all object types off, then turn on just **Parts**.



5. Click **Find**.

The three parts on PAGE1 are listed in the Find Results window.

6. **Double-click** on the entries in the Find Results window to highlight the corresponding object on the schematic page.

7. Click in an open area or use the **Esc** key to clear any selected items.

8. Click on the page tab to activate PAGE2 of the schematic.

9. Click **Find**.

The two parts on PAGE1 are listed in the Find Results window.

10. Notice that the three parts on PAGE2 are not listed. By default, the search is limited to the active page.

## Searching the Entire Design

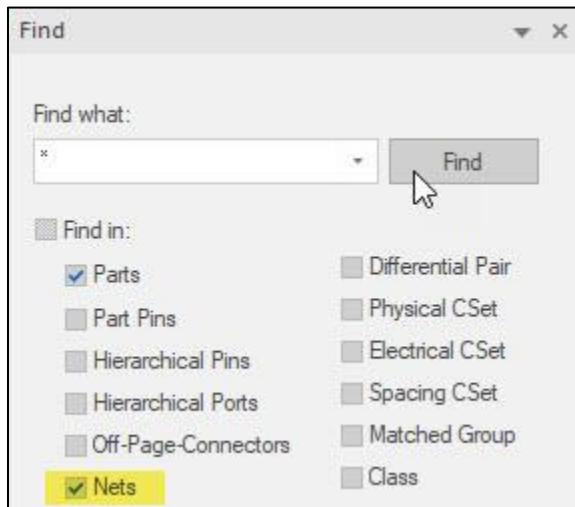
1. In the Project Manager, click on the **project2.dsn** entry.

2. Click **Find** and notice all five parts are listed in the Find Results window.

3. **Double-click** on the entries in the list to highlight the part on any schematic page.

4. Click in an open area to clear all selected items.

5. In the **Find** tab, click on **Nets**.



Both Parts and Nets are now selected.

6. In the Project Manager, click on the **project2.dsn** entry.

7. In the Find tab, click **Find** and notice the Find Results window contains two tabs: one for Parts and one for Nets.

8. In the Find Results window, click on the **Parts** tab to see all five parts in the design.

9. Click on the **Nets** tab to see all nets in the design.

You can click on any column header to sort the nets by name or page number.

10. **Double-click** to visit any net in the schematic.

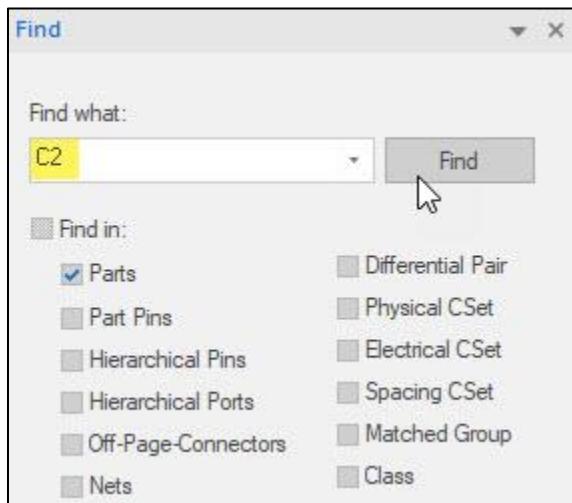
11. Click in an open area to clear all selected items.

## Searching for Specific Parts and Nets

1. In the Project Manager window, select the **project.dsn** entry.

2. In the **Find** tab, turn off the Nets object type.

3. In the Find what field, enter **C2** and click **Find**.



4. Notice the Find Results window lists capacitor C2.

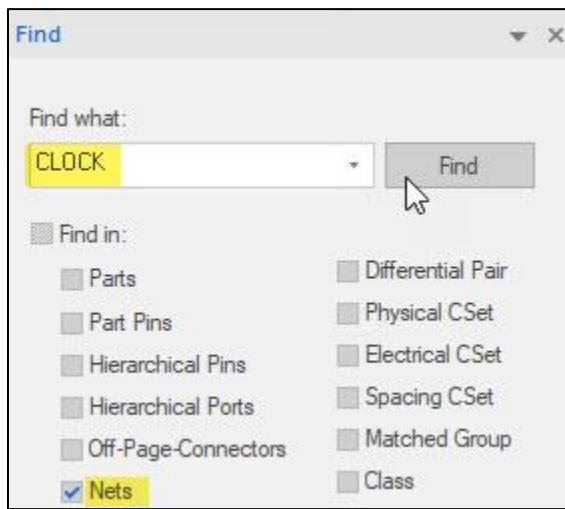
You can **double-click** to view the part in the design.

5. In the Project Manager window, select the **project.dsn** entry.

6. In the **Find** tab, turn off **Parts** and turn on **Nets**.

Building a Multi-Sheet Schematic

7. In the Find what field, enter **CLOCK** and click **Find**.



8. Notice the Find Results window lists two entries for net CLOCK.
9. **Double-click** to view the net in the design.
10. Click in an open area to clear the selected set.

### Closing All Pages

1. **Right-click** on a page tab and choose **Close All Tabs**.  
All schematic pages are closed.
2. Close the **Find** tab.
3. Close the Find Results pane.  
The Capture session window is still running, and project2 is still open.

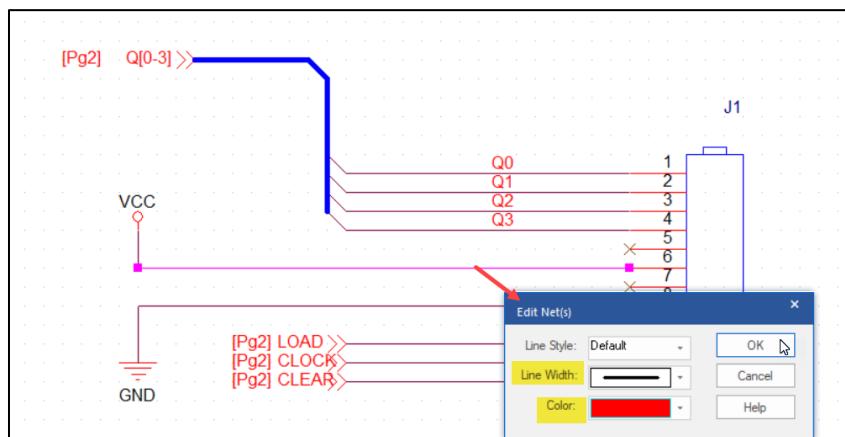


## Lab 6-9 Modifying Wire Attributes

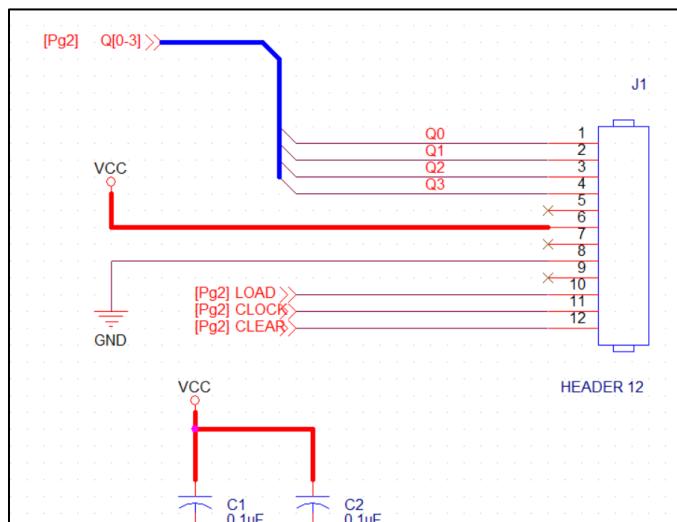
**Objective:** To change the graphics of all wires in a net.

### Assigning Attributes to the VCC Net

1. Open PAGE1.
2. Click on the VCC wire, right-click and choose **Edit Net Properties** from the pop-up menu.
3. In the Edit Net(s) window, toggle the Line Width field to a thicker line and change the Color field to red.

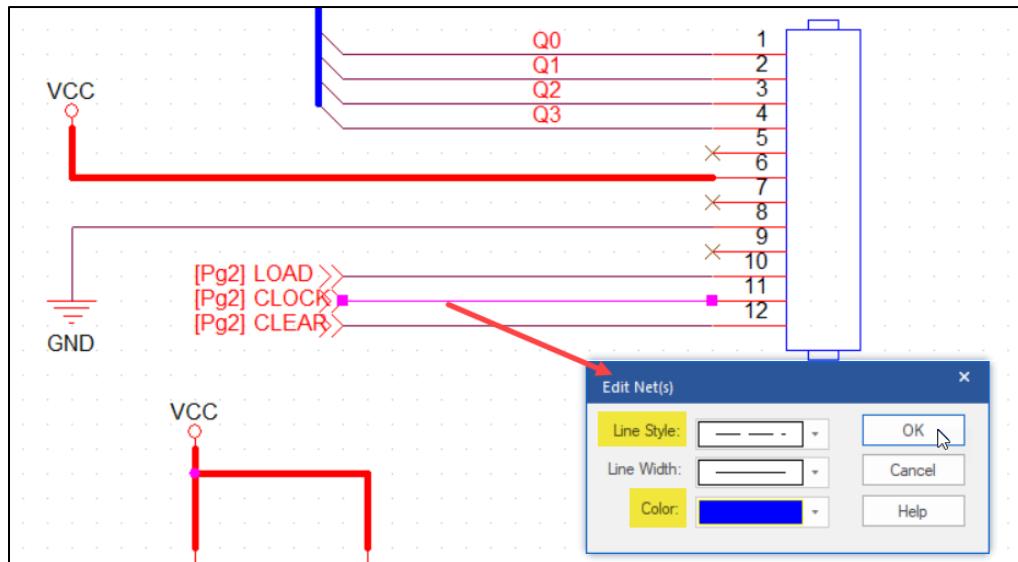


4. Click **OK** and press **Esc** to deselect.
5. Notice the change was applied to all VCC wires on the page.



### Assigning Attributes to the CLOCK Net

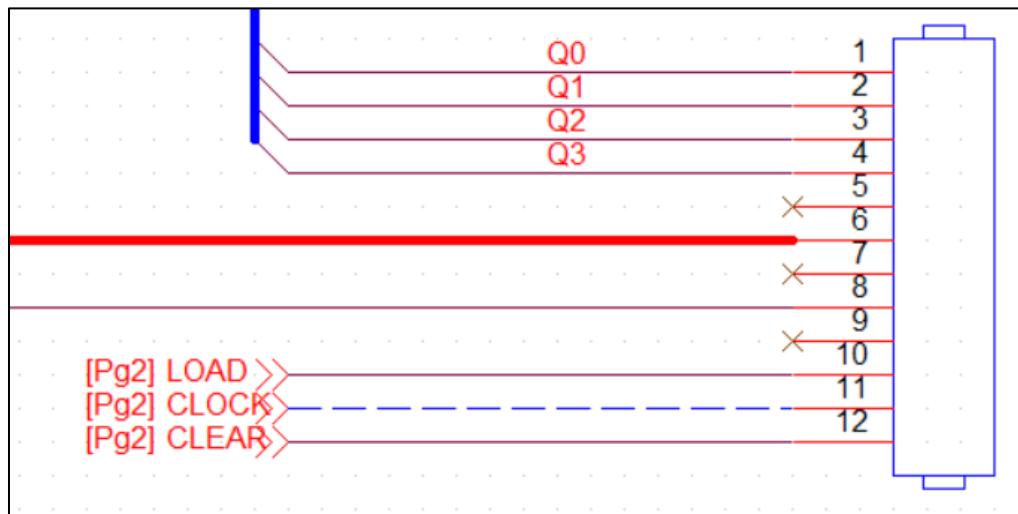
- Click on the CLOCK wire and choose **Edit Net Properties** from the right mouse pop-up.



- Toggle the Line Style field to dashed and change the Color field.
- Click **OK** and press **Esc** to clear the selected wire and view the changes.

Since this change was applied to the entire CLOCK net, the same changes should be visible everywhere in the design.

- Open PAGE2 to view the CLOCK net.



## Saving the Design

1. In the Project Manager, click on the **project2.dsn** design file and choose **File – Save**.

## Closing All Pages

1. **Right**-click on a page tab and choose **Close All Tabs**.

All schematic pages are closed.



(c) Cadence Design Systems Inc. Do not distribute.

## **Module 7: Editing Part Properties**

(c) Cadence Design Systems Inc. Do not distribute.

## Lab 7-1 Using the Property Editor

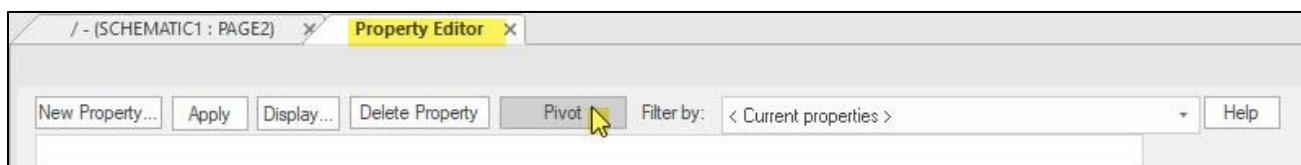
**Objective:** To view part and pin properties.

1. Open the **project2.dsn** schematic and **double-click** on the Project Manager to open PAGE2.
2. Select the **74F162** part.
3. **Right-click** and select **Edit Properties**.

You can also **double-click** on the part to open the Property Editor. The Property Editor shows the selected object (U1) and all properties currently on the part.

### Pivoting the Spreadsheet

1. At the top of the Property Editor, click on the **Pivot** button to see how it affects the format of the property table.



Pivoting the spreadsheet causes the property names and the selected object(s) to switch positions along the left and top edges of the spreadsheet.

2. Pivot the spreadsheet so the property names are along the left (as rows) and the selected object across the top (as a column).

	A
	SCHEMATIC1 : PAGE2 : U1
Color	Default
Designator	
Graphic	74F162.Normal
ID	
Implementation	
Implementation Path	
Implementation Type	<none>
Last Value	200

## Filtering by Object Type

1. Notice the tabs along the bottom edge of the Property Editor window.
  2. Click the **Pins** tab at the bottom of the window.



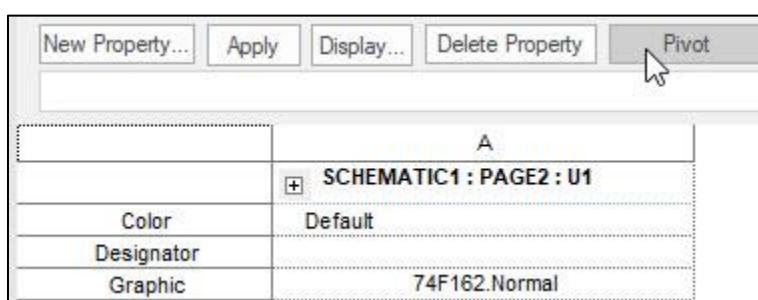
All the pin properties for the 74F162 part are displayed.

- Pivot the property table so the pin names are rows and pin properties are columns, as shown below.

		Is No Connect	Name	Net Name	Number	Order	Swap Id	Type
1	SCHEMATIC1 : PAGE2 : U1 : A	<input checked="" type="checkbox"/>	A		3	0	-1	Input
2	SCHEMATIC1 : PAGE2 : U1 : B	<input checked="" type="checkbox"/>	B		4	1	-1	Input
3	SCHEMATIC1 : PAGE2 : U1 : C	<input checked="" type="checkbox"/>	C		5	2	-1	Input
4	SCHEMATIC1 : PAGE2 : U1 : CLVR	<input type="checkbox"/>	CL\ R\	CLEAR	1	12	-1	Input
5	SCHEMATIC1 : PAGE2 : U1 : CLK	<input type="checkbox"/>	CLK	CLOCK	2	4	-1	Input
6	SCHEMATIC1 : PAGE2 : U1 : D	<input checked="" type="checkbox"/>	D		6	3	-1	Input
7	SCHEMATIC1 : PAGE2 : U1 : ENP	<input checked="" type="checkbox"/>	ENP		7	13	-1	Input
8	SCHEMATIC1 : PAGE2 : U1 : ENT	<input checked="" type="checkbox"/>	ENT		10	14	-1	Input
9	SCHEMATIC1 : PAGE2 : U1 : GND	<input type="checkbox"/>	GND	GND	8	11	-1	Power
10	SCHEMATIC1 : PAGE2 : U1 : LIOVAD	<input type="checkbox"/>	LIOVAD\	LOAD	9	15	-1	Input
11	SCHEMATIC1 : PAGE2 : U1 : QA	<input type="checkbox"/>	QA	Q0	14	5	-1	Output
12	SCHEMATIC1 : PAGE2 : U1 : QB	<input type="checkbox"/>	QB	Q1	13	6	-1	Output
13	SCHEMATIC1 : PAGE2 : U1 : QC	<input type="checkbox"/>	QC	Q2	12	7	-1	Output
14	SCHEMATIC1 : PAGE2 : U1 : QD	<input type="checkbox"/>	QD	Q3	11	8	-1	Output
15	SCHEMATIC1 : PAGE2 : U1 : RCO	<input checked="" type="checkbox"/>	RCO		15	9	-1	Output
16	SCHEMATIC1 : PAGE2 : U1 : VCC	<input type="checkbox"/>	VCC	VCC	16	10	-1	Power

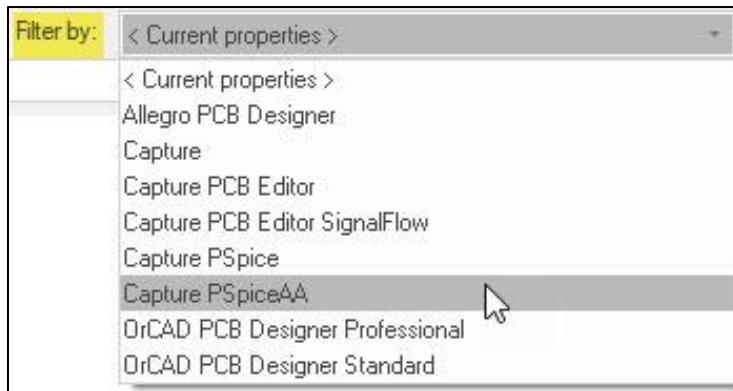
Depending on what you’re viewing, you can pivot the property table at any time to make the content easier to work with.

4. Select the **Parts** tab at the bottom of the Property Editor spreadsheet.
  5. Pivot the table so the part properties are displayed as rows.



## Selecting a Property Filter

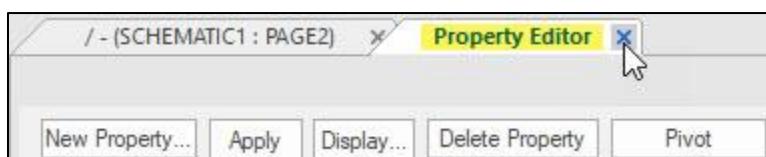
1. At the top of the Property Editor window, click in the **Filter by** field and select **Capture PSpiceAA**.



2. Pivot the table so all properties appear as rows.

This filter contains a list of PSpice part properties. A property filter can contain both part and net properties. When you have a net selected, just the net properties in the filter will be displayed in the Property Editor.

3. Click on the **Property Editor** tab to close the Property Editor.



4. In the schematic, click on an open area to deselect the part.



## Lab 7-2 Using the Allegro X PCB Designer Property Filter

**Objective:** To add part properties using the Property Editor.

---

### Applying the Property Filter

1. Double-click on the **74F162** part to open the Property Editor.
2. At the top of the Property Editor window, click in the **Filter by** field and select **Allegro PCB Designer**.



A specialized list of part properties is displayed. This filter contains properties that you can use with the Allegro® PCB Editor.

### Assigning a PCB Footprint Name

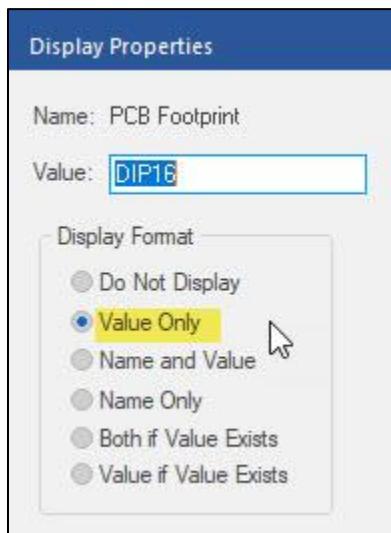
1. With the property list pivoted as shown below, click in the **PCB Footprint** field and enter **DIP16**.

	A
	SCHEMATIC1 : PAGE2 : U1
NO_SWAP_PIN	
PART_NUMBER	
PCB Footprint	DIP16
PIN_ESCAPE	
PINUSE	
PLACE_TAG	
POWER_GROUP	
Power Pins Visible	

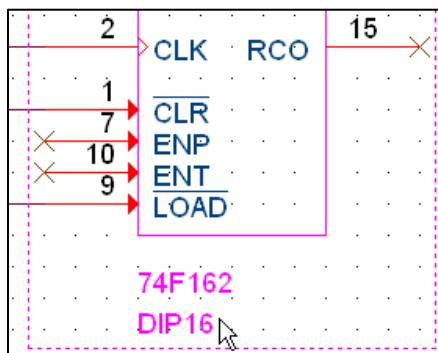
2. Click the **Display** button located at the top of the spreadsheet.

The Display Properties window appears.

3. In the Display Format section of the window, select **Value Only**.



4. Click **OK**.
5. Close the Property Editor window.



6. Notice the PCB Footprint property value **DIP16** is now visible in the schematic.
7. Click in an open area to deselect the 74F162 part.
8. Choose **File – Save**.

**Note:** You can use **Ctrl+Z** to undo a change while in the Property Editor. Once you close the Property Editor, you can't undo the change.

## Checking Missing or Illegal PCB Footprint Property

1. Choose **View – Others – Online DRCs** to toggle this DRC window on and off.

Online DRCs			
Severity	DRC Type	Description	Detail
Error	Physical	ERROR(ORCAP-36002): Property "PCB Footprint" missing from instance U2A: SCHEMATIC1, PAGE2 (5.20, 3.50).	/U2A
Warning	Physical	WARNING(ORCAP-2434): Footprint 'DIP16' specified in PCB Footprint for instance 'U1' is missing. Ensure 'DIP16' is in the library path.	/U1
Error	Physical	ERROR(ORCAP-36002): Property "PCB Footprint" missing from instance J1: SCHEMATIC1, PAGE1 (4.90, 1.60).	/J1
Error	Physical	ERROR(ORCAP-36002): Property "PCB Footprint" missing from instance C1: SCHEMATIC1, PAGE1 (6.60, 2.30).	/C1
Error	Physical	ERROR(ORCAP-36002): Property "PCB Footprint" missing from instance C2: SCHEMATIC1, PAGE1 (7.30, 2.30).	/C2

2. Notice the DIP16 footprint you specified for U1 is invalid because it cannot be found in the library.

## Multiple Object Property Editing

1. Press **Ctrl+click** to select both the **74F162** and **74LS00** parts.

2. **Right-click** and select **Edit Properties**.

Notice that the properties for both parts are displayed.

3. Click in the **PCB Footprint** field for the 74F162 part and change the value from DIP16 to **SOIC16**.

	A	B
	+ SCHEMATIC1 : PAGE2 : U1	+ SCHEMATIC1 : PAGE2 : U2A
NO_SWAP_PIN		
PART_NUMBER		
PCB Footprint	SOIC16	DIP20

4. Click in the **PCB Footprint** field for the 74LS00 part.

- a. Enter the value to **DIP20**.

- b. Click the **Display** button, set Display Format to **Value Only**, and click **OK**.

This makes the value of the PCB Footprint property visible in the schematic.

5. Close the Property Editor window and click in an open area to deselect both parts.

## Checking Missing or Illegal PCB Footprint Property

- Notice the warning for the 74F162 part is gone, and the footprint you specified for the 74LS00 is invalid because the pin count doesn't match.

Online DRCs			
Severity	DRC Type	Description	Detail
Warning	Physical	WARNING(ORCAP-2435): Number of pins in footprint 'DIP20' and instance 'U2A' does not match.	/U2A
Error	Physical	ERROR(ORCAP-36002): Property "PCB Footprint" missing from instance J1: SCHEMATIC1, PAGE1 (4.90, 1.60).	/J1
Error	Physical	ERROR(ORCAP-36002): Property "PCB Footprint" missing from instance C1: SCHEMATIC1, PAGE1 (6.60, 2.30).	/C1
Error	Physical	ERROR(ORCAP-36002): Property "PCB Footprint" missing from instance C2: SCHEMATIC1, PAGE1 (7.30, 2.30).	/C2

- Double-click on the **74LS00** part and change the PCB Footprint to **SOIC14**.
- Close the Property Editor.
- Choose **File – Save**.
- Notice the footprint warning for the 74LS00 part is gone.

Online DRCs			
Severity	DRC Type	Description	Detail
Error	Physical	ERROR(ORCAP-36002): Property "PCB Footprint" missing from instance J1: SCHEMATIC1, PAGE1 (4.90, 1.60).	/J1
Error	Physical	ERROR(ORCAP-36002): Property "PCB Footprint" missing from instance C1: SCHEMATIC1, PAGE1 (6.60, 2.30).	/C1
Error	Physical	ERROR(ORCAP-36002): Property "PCB Footprint" missing from instance C2: SCHEMATIC1, PAGE1 (7.30, 2.30).	/C2

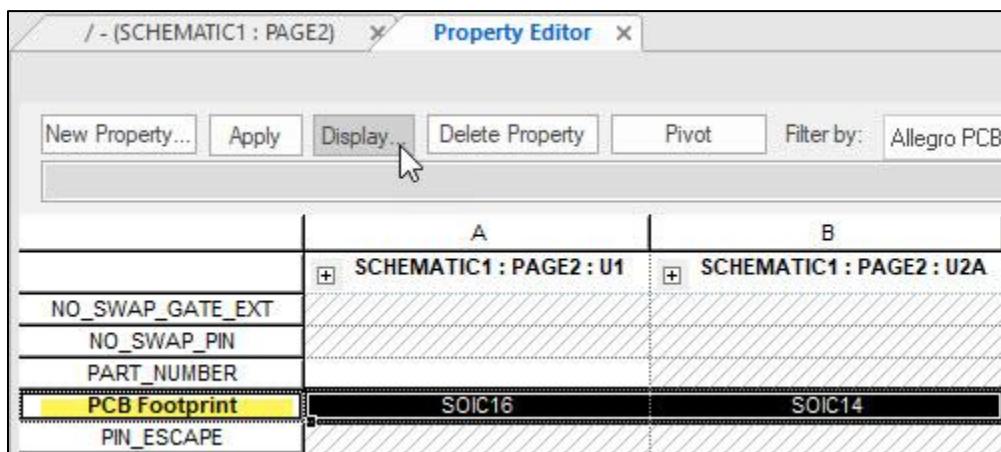
The remaining errors are caused by the three parts having no PCB footprint assigned yet. You will resolve these errors in the next lab.

## Multiple Object Property Display

- Select both the **74F162** and **74LS00** parts.
- Press **Ctrl+E** to display the Property Editor (or right-click and select **Edit Properties**).

## Editing Part Properties

3. Select the **PCB Footprint** property name box on the left and click the **Display** button.



4. In the Display Properties window, select **Do Not Display** and click **OK**.
5. Close the Property Editor window and click in an open area to deselect all parts.
6. Notice that both PCB footprint properties are now invisible.

### Adding a New Property to Multiple Objects

1. Select both the **74F162** and **74LS00** parts.
2. **Right-click** and select **Edit Properties** (or press **Ctrl+E**).
3. At the top of the Property Editor window, click **New Property**.
4. In the Name field, enter **VENDOR** and click **OK**.

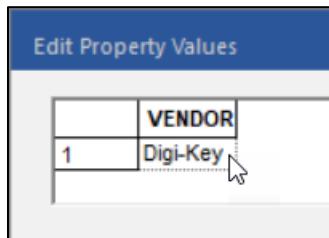
The VENDOR property is added to the property table.

5. Click on the VENDOR property name to select the entire row. Then right-click and choose **Edit**.

	A	B
Power Pins Visible	SCHEMATIC1 : PAGE2	SCHEMATIC1 : PAGE2
Primitive	DEFAULT	DEFAULT
Reference	U1	U2
Source Library	C:\CADENCE\SPB_23.1...	C:\CADENCE\SPB_23.1...
Source Package	74F162	74LS00
Source Part	74F162.Normal	74LS00.Normal
Value	74F162	74LS00
VENDOR		

This lets you set the value for the entire row.

6. Click on the VENDOR field, enter Digi-Key, and click **OK**.



The VENDOR name is applied to both parts.

7. Close the Property Editor window.

8. Click to deselect all parts.

**Note:** You can also press **Ctrl+C** and **Ctrl+V** to copy and paste property values between cells in the Property Editor.

## Saving and Closing the Page

1. Choose **File – Save** to save PAGE2.
2. Close the schematic page.



## Lab 7-3 Using an Update Properties File

**Objective:** To add part properties using a text file.

---

### Viewing the Parts Update File

- With a text editor, such as Notepad, view the contents of the *Parts.upd* file located in your *C:\User1\Capture\data\_files* directory.

This tab-delimited file attaches six properties to each part type specified in the first column. The following table is for display purposes only (to help you see the property names and values).

"<Value>"	"PART_NUMBER"	"PCB Footprint"	"CLASS"	"ROOM"	"VENDOR"	"COST"
"74LS00"	"20-12345"	"SOIC14"	"IC"	"DATA"	"ABC CO"	"\$1.20"
"7400"	"20-12345"	"SOIC14"	"IC"	"DATA"	"ABC CO"	"\$1.20"
"74F162"	"20-67890"	"SOIC16"	"IC"	"DATA"	"ABC CO"	"\$3.95"
".1UF"	"30-10293"	"SMC_6032"	"DISCRETE"	"CHAN1"	"XYZ INC"	"\$0.75"
"0.1UF"	"30-10293"	"SMC_6032"	"DISCRETE"	"CHAN2"	"XYZ INC"	"\$0.75"
"HEADER 12"	"40-98743"	"HEADER12"	"IO"	""	"ACME INC"	"\$5.86"
"12HEADER"	"40-98743"	"HEADER12"	"IO"	""	"ACME INC"	"\$5.86"

- Close the *Parts.upd* file.

### Viewing the Session Log Window

- Choose **View – Session Log Window**.

This step displays a Session Log at the bottom of the Capture work area.

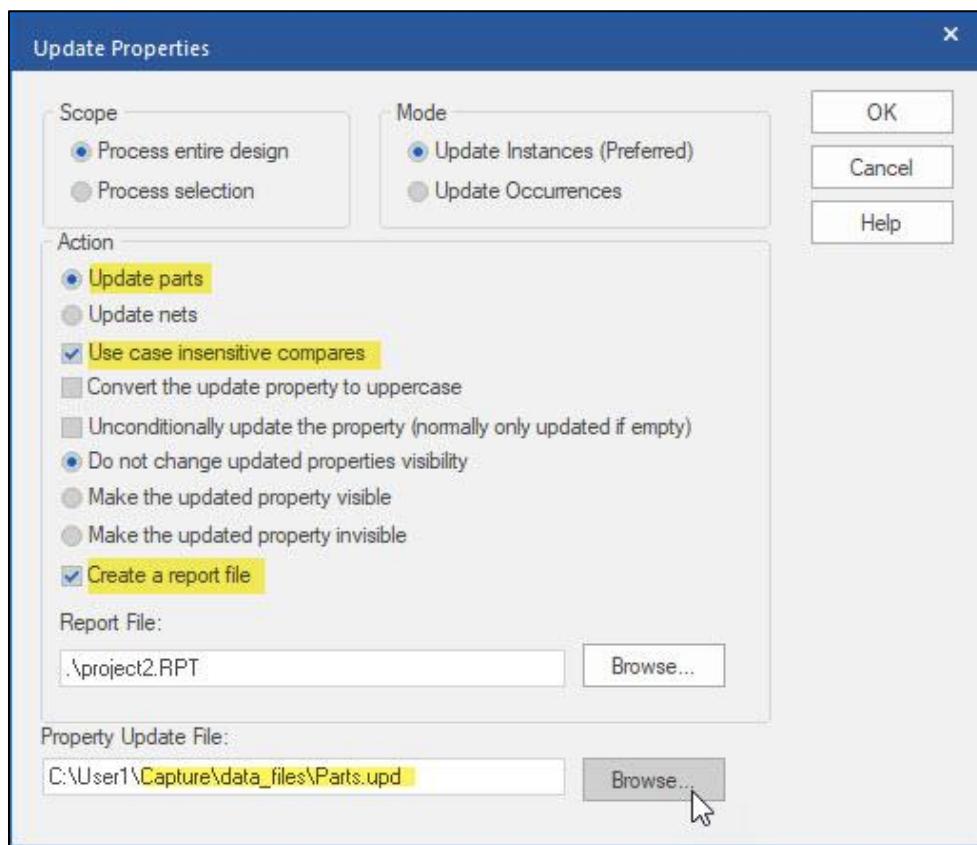
- Choose **Edit – Clear Session Log**.

You will use this session log window to view some results later in this lab.

### Updating Part Properties

- In the Project Manager window, select the design file.
- Choose **Tools – Update Properties**.

3. In the Action section, make sure **Update parts** is selected.
4. Choose **Use case insensitive compares**.
5. Choose **Create a report file**.
6. To specify the Property Update File, click **Browse**. Navigate to the *C:\User1\Capture\data\_files* directory.  
Remember to change the above path to reflect the actual location on your system.
7. Select the **Parts.upd** file and click **Open**.



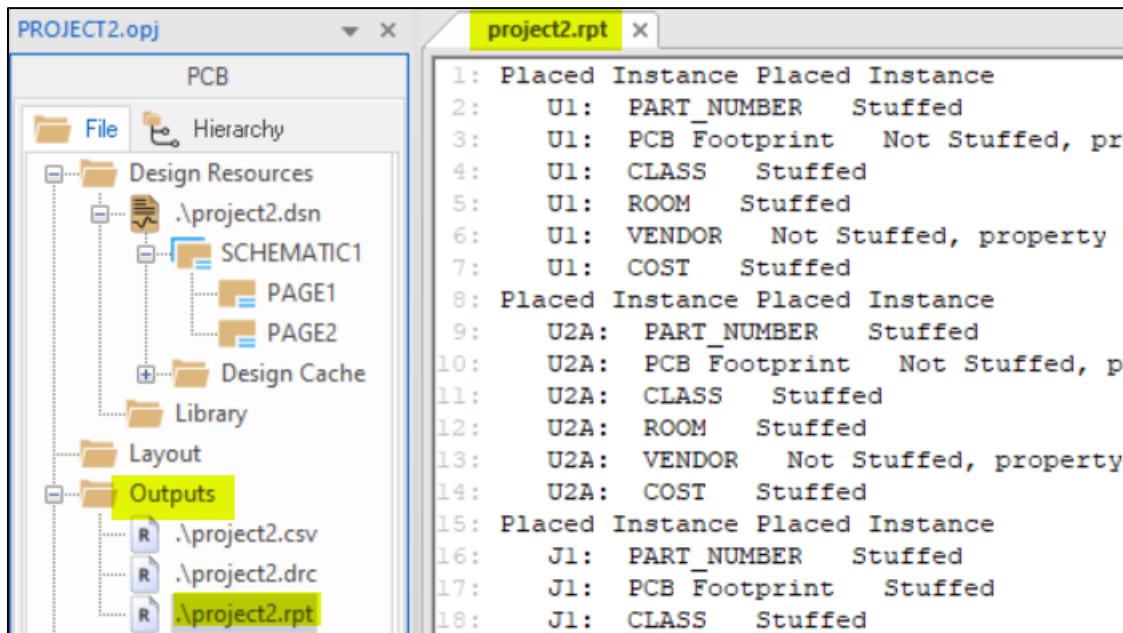
8. In the Update Properties window, click **OK**.  
The part properties file is applied to the design.

## Saving the Design

1. Select the design file in the Project Manager window and choose **File – Save** and **Yes** to confirm.

## Viewing the Session Log and Report

1. View the contents of the Session Log window and notice at the end that it shows which lines in the update file did not match any parts in the design.
2. Close the Session Log window.
3. In the Outputs folder of the Project Manager window, **double-click** on **project2.rpt** to view the same information in a report file.



The screenshot shows the Cadence Project Manager interface. On the left, the Project Manager window titled 'PROJECT2.opj' displays a tree structure of files and folders under 'PCB'. The 'Outputs' folder is expanded, showing three files: '.\project2.csv', '.\project2.drc', and '.\project2.rpt'. The file '.\project2.rpt' is highlighted with a yellow selection bar. To the right, a separate window titled 'project2.rpt' contains the following text:

```

1: Placed Instance Placed Instance
2: U1: PART_NUMBER Stuffed
3: U1: PCB Footprint Not Stuffed, pro
4: U1: CLASS Stuffed
5: U1: ROOM Stuffed
6: U1: VENDOR Not Stuffed, property
7: U1: COST Stuffed
8: Placed Instance Placed Instance
9: U2A: PART_NUMBER Stuffed
10: U2A: PCB Footprint Not Stuffed, p
11: U2A: CLASS Stuffed
12: U2A: ROOM Stuffed
13: U2A: VENDOR Not Stuffed, property
14: U2A: COST Stuffed
15: Placed Instance Placed Instance
16: J1: PART_NUMBER Stuffed
17: J1: PCB Footprint Stuffed
18: J1: CLASS Stuffed

```

4. Notice the report shows that existing property values were not overridden.
5. Close the report.

## Viewing the Resulting Properties in the Schematic

1. Open PAGE1 of the design and **double-click** one of the capacitors.
2. In the Property Editor, set the *Filter by* field to <Current properties> and pivot the spreadsheet so properties are in a column on the left.
3. Locate the *CLASS*, *COST*, *PART\_NUMBER*, *PCB Footprint*, *ROOM*, and *VENDOR* properties.

These properties have been added to all 0.1uF capacitors in the design.

4. Close the Property Editor.

5. Close the schematic page.



## Lab 7-4 Using an Export/Import Properties File

**Objective:** To export part properties from a design, edit the export file in Excel and import it back into the design.

---

### Exporting Part Properties

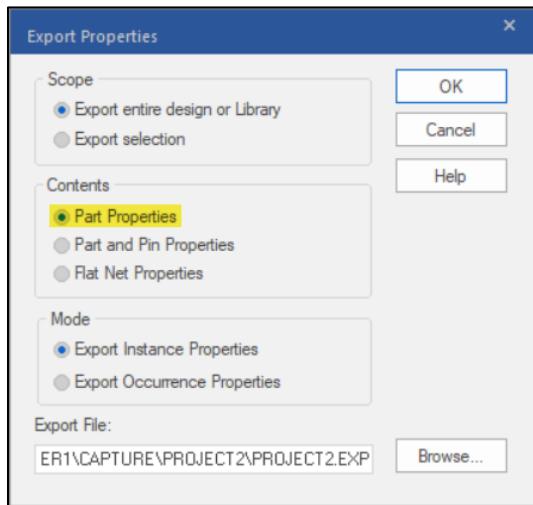
1. Select the design file in the Project Manager window.

2. Choose **Tools – Export Properties**.

The Export Properties window appears.

3. In the Contents section, notice that Part Properties is on by default.

This means that all existing part properties will be exported to a text file named *project2.exp*.

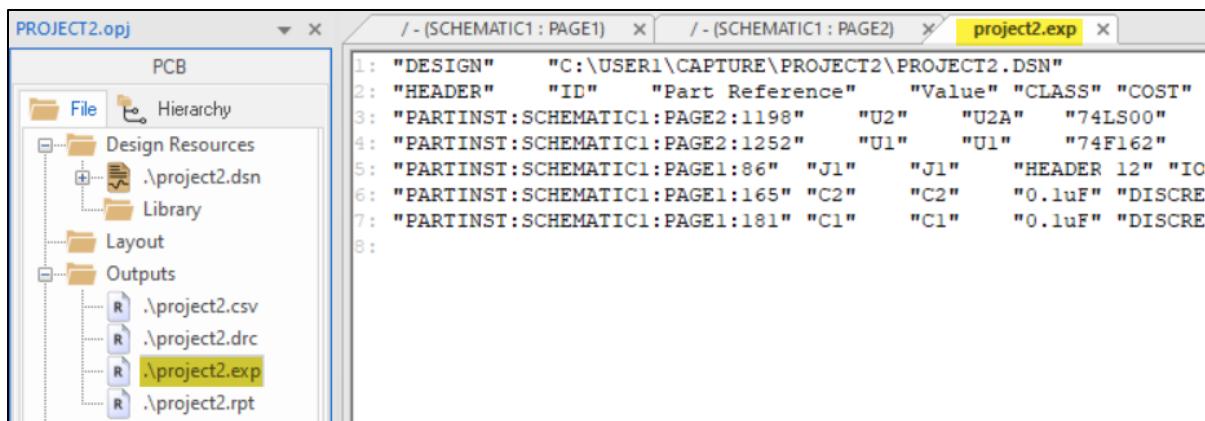


4. Click **OK**.

5. Notice that the *project2.exp* file is listed under the *Outputs* folder in Project Manager.

6. In the Project Manager window, double-click the **project2.exp** file.

The exported file opens in a text editor window. This file lists the five parts in the design and shows all the properties currently on each of the parts.



7. View and close the export file. (Do **NOT** edit.)

This *project2.exp* file is stored in the project folder.

## Viewing the Export File with Excel

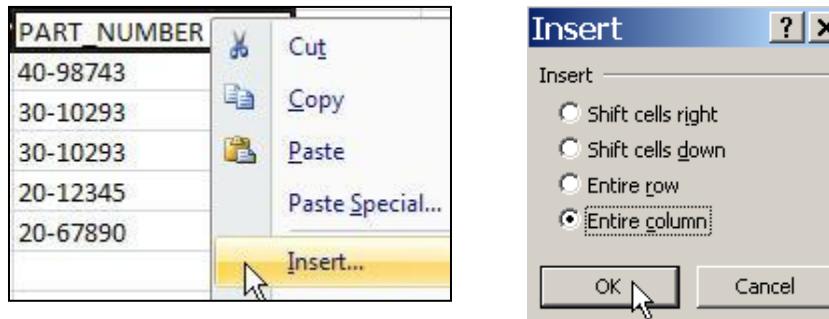
1. Start **Microsoft Excel**.
  2. In Excel, click **Open** and click **Browse**.
  3. Browse to the directory *C:\User1\Capture\Project2*.
  4. Toggle the file type field to **All Files (\*.\*)**.
  5. Select the **project2.exp** file and click **Open**.
  6. In the Text Import Wizard – Step 1 of 3, click **Next**.  
This tells Excel that the export file is tab-delimited.
  7. In the Text Import Wizard – Step 2 of 3, click **Finish**.  
The export file is loaded.
  8. Click and drag to increase the column width for the PART\_NUMBER property (so you can clearly see the column header).
- Caution:** Do *not* rearrange the file by sorting any columns.

Editing Part Properties

## Editing the Export File

**Important:** Do not delete any rows or columns. Do not save the file in Excel format.

1. Right-click on the **PART\_NUMBER** column header and select **Insert**.



This step adds a new column to the left of the PART\_NUMBER column.

2. Click in the header row at the top of the new column and enter **DESCRIPTION**.

DESCRIPTION	PART_NUMBER
	40-98743

3. Assign part descriptions as shown below.

Part Reference	Value	CLASS	COST	Graphic	Location X	Location Y	DESCRIPTION	PART_NUMBER	PCB Footprint
U1	74F162	IC	\$3.95	74F162.N	360	180	IC 74F162	20-67890	SOIC16
U2A	74LS00	IC	\$1.20	74LS00.N	520	350	IC 74LS00	20-12345	SOIC14
J1	HEADER 12	IO	\$5.86	HEADER	490	160	HEADER 12 PIN	40-98743	HEADER12
C1	0.1uF	DISCRETE	\$0.75	CAP.Nor	660	230	CAP_0.1uF	30-10293	SMC_6032
C2	0.1uF	DISCRETE	\$0.75	CAP.Nor	730	230	CAP_0.1uF	30-10293	SMC_6032

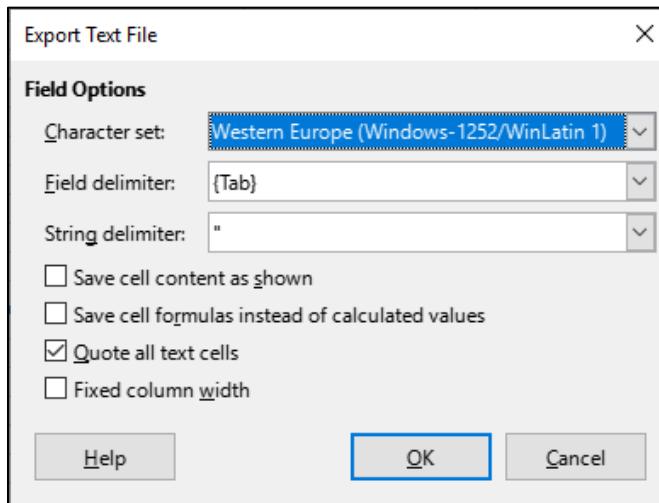
## Saving the Export File

1. If you have Excel available on your computer, perform the following steps:
  - a. In Excel, choose **File – Close** (*not* the File – Save command).
  - b. Click **Save** to indicate you want to save the **PROJECT2.EXP** file.
  - c. Exit Excel.
2. If you have Libre Office available on your computer, perform the following steps:
  - a. Choose **File – Save As**.
  - b. Change the File name to **PROJECT2.exp**

- c. Disable **Automatic file name extension**.
- d. Enable **Edit filter Settings**. Your window should look similar to the following.



- e. Click **Save**.
- f. Click **Yes** to overwrite the existing file.
- g. In the Export Text File window, only enable **Quote all text cells**.



- h. Click **OK** to save the file.
- i. Close Libre Office.

## Importing the File

1. In the Project Manager window, select the design filename and choose **Tools – Import Properties**.
2. In the Import Properties window, navigate to the directory *C:\User1\Capture\Project2*.

3. Select the **PROJECT2.EXP** file and click **Open**.

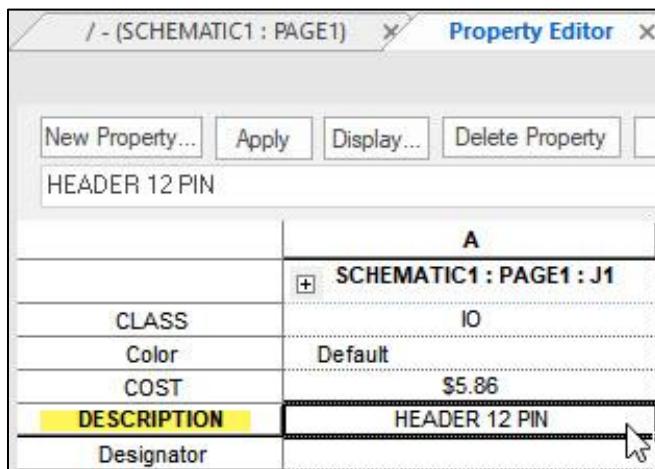
The modified property file is loaded into the design.

## Saving the Design

1. Choose **File – Save**.

## Viewing Resulting Properties in the Schematic

1. Open a schematic page and use the Property Editor to verify that all parts now have a DESCRIPTION property.



2. Close the Property Editor.

3. Close the schematic page.



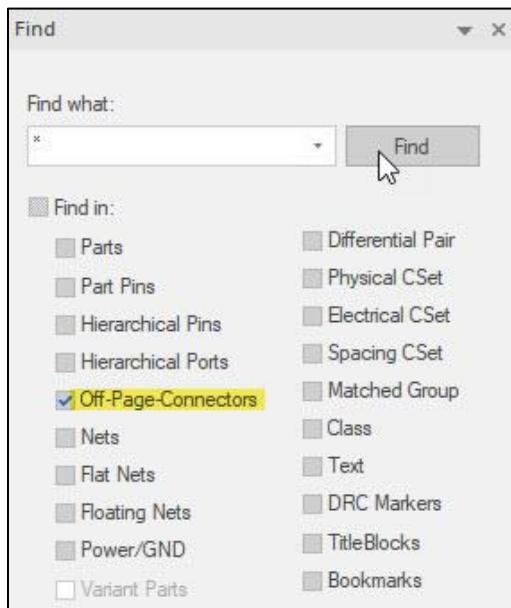
## Lab 7-5    Multiple Object Editing with the Browse Spreadsheet

**Objective:** To edit off-page connector and title block properties.

---

### Searching for Off-Page Connectors

1. In the Project Manager window, right-click on the design name and select **Find**.
2. In the **Find** tab, clear all object types. Then turn on just **Off-Page-Connectors**.
3. Enter an asterisk wildcard in the Find what field and click **Find**.



4. The Find Results window lists all off-page connectors in the design.

Find Results									
Off-Page-Connectors									
Name	Page	Page Number	Schematic	PartPin	LocationX	LocationY	Zone	IREF	
CLEAR	PAGE1	1	SCHEMATIC1	J1.12	330	280	B2	[Pg2]	
CLEAR	PAGE2	2	SCHEMATIC1	U1.1	210	250	B2	[Pg1]	
CLOCK	PAGE1	1	SCHEMATIC1	J1.11	330	270	B2	[Pg2]	
CLOCK	PAGE2	2	SCHEMATIC1	U1.2	210	230	B2	[Pg1]	
LOAD	PAGE1	1	SCHEMATIC1	J1.10	330	260	B2	[Pg2]	
LOAD	PAGE2	2	SCHEMATIC1	U2.3,U1.9	210	280	B2	[Pg1,2]	
LOAD	PAGE2	2	SCHEMATIC1	U2.3,U1.9	710	360	D3	[Pg1,2]	
Q[0-3]	PAGE1	1	SCHEMATIC1		270	140	B1	[Pg2]	
Q[0-3]	PAGE2	2	SCHEMATIC1		620	150	D1	[Pg1]	

The entries are sorted by net name.

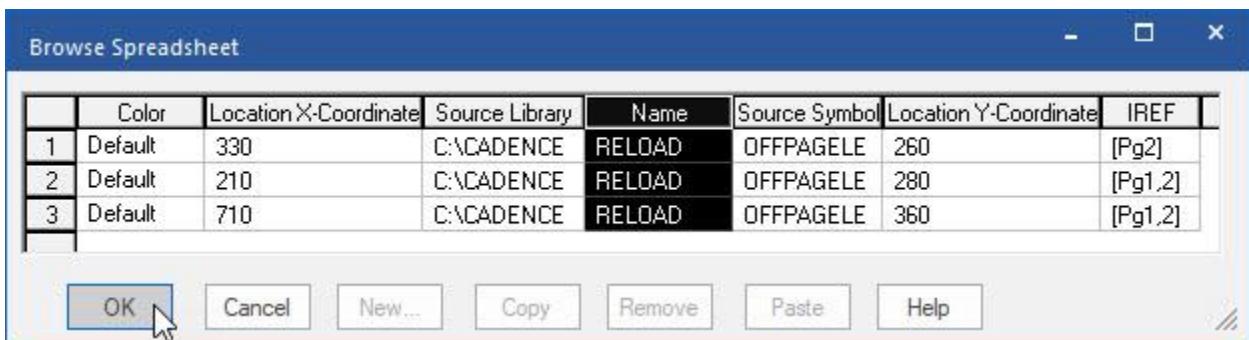
## Editing Part Properties

5. In the Find Results window, **Ctrl+click** to select all the off-page connectors named **LOAD**, right-click and select **Edit Properties**.

Off-Page-Connectors								
Name	Page	Page Number	Schematic	PartPin	LocationX	LocationY	Zone	IREF
CLEAR	PAGE1	1	SCHEMATIC1	J1.12	330	280	B2	[Pg2]
CLEAR	PAGE2	2	SCHEMATIC1	U1.1	210	250	B2	[Pg1]
CLOCK	PAGE1	1	SCHEMATIC1	J1.11	330	270	B2	[Pg2]
CLOCK	PAGE2	2	SCHEMATIC1	U1.2	210	230	B2	[Pg1]
LOAD	PAGE1	1	SCHEMATIC1	J1.10	330	260	B2	[Pg2]
LOAD	PAGE2	2	SCHEMATIC1	U2.3,U1.9	210	280	B2	[Pg1,2]
LOAD	PAGE2	2	SCHEMATIC1	U2.3,U1.9	710	360	D3	[Pg1,2]
Q[0-3]	PAGE1	1	SCHEMATIC1		270	140	B1	[Pg2]
Q[0-3]	PAGE2	2	SCHEMATIC1		620	150	D1	[Pg1]

This step opens the Browse Spreadsheet, where you can edit all selected entries at once.

6. In the Browse Spreadsheet, change the Name field to **RELOAD**.



7. Click **OK**.

The Find Results window now shows the new off-page connector names.

## Saving the Design

- In the Project Manager, click **project2.dsn** and choose **File – Save**.
- In the Find Results window, **double-click** the RELOAD entries to visit the changes in the schematic.

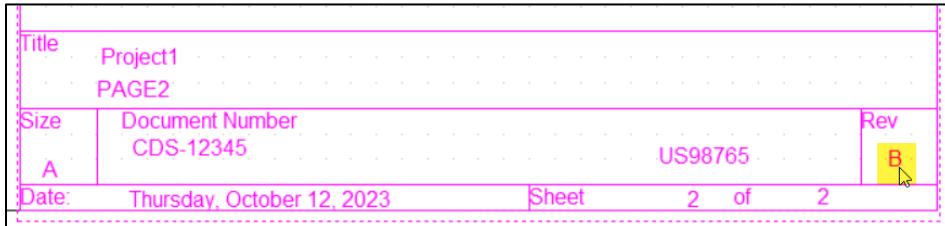
## Searching for Title Blocks

- In the Project Manager window, select the design name.
- In the **Find** tab, clear all object types. Then, turn on **TitleBlocks** and click **Find**.

3. The Find Results window lists both title blocks in the design.
4. In the Find Results window, select both title block entries, right-click and select **Edit Properties**.
5. In the Browse Spreadsheet, change the RevCode field to **B** and click **OK**.

Browse Spreadsheet														
	Design Create Date	Page Size	Page Number	Title	OrgAddr4	Cage Code	Page Count	OrgAddr1	Hemetic P	RevCode	OrgAddr2	Doc	OrgAddr3	OrgName
1	Wednesday, Dece	A	1	Project2		US98765	2	2655 S		B	San Jose	CDS-12		Cadence
2	Wednesday, Dece	A	2	Project2		US98765	2	2655 S		B	San Jose	CDS-12		Cadence

6. In the Find Results window, double-click the title block entries to view the RevCode changes in the schematic.



## Saving the Design

1. In the Project Manager, click **project2.dsn** and choose **File – Save**.
2. Close all schematic pages.
3. Close the Find tab and the Find Results window.

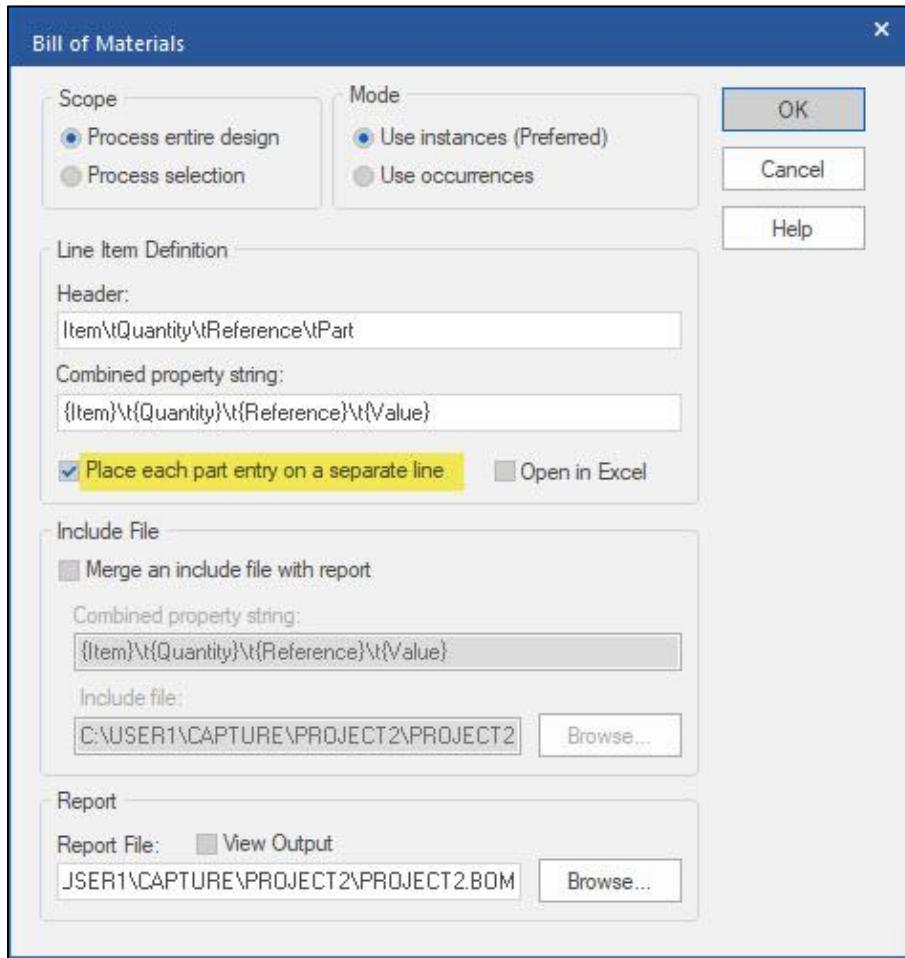
The Capture session window is still running, and project2 is still open.



## Lab 7-6 Creating a Bill of Materials Report

**Objective:** To create a standard and custom Bill of Materials.

1. Select the design name in the Project Manager window and choose **Tools – Bill of Materials**.
2. Select the **Place each part entry on a separate line** checkbox.



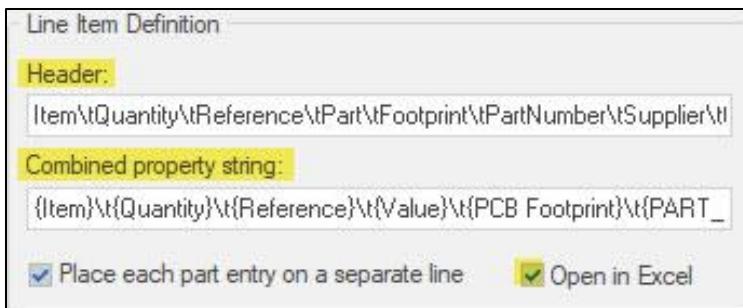
3. Click **OK**.
4. Double-click on the **project2.bom** file in the Outputs folder of the Project Manager window.

The Bill of Materials report is displayed. Notice that the report contains four columns (Item, Quantity, Reference, and Part).

5. Close the report.

## Customizing the Format of the BOM Report

1. Select the design name in the Project Manager window and choose **Tools – Bill of Materials**.
2. In the Line Item Definition section of the Bill of Materials window, locate the **Header** field and specify the titles of the columns that will be in the BOM report.



**Tip:** You can use the *Bill-of-Materials-settings.txt* file located in the *C:\User1\Capture\data\_files* directory to copy and paste the **Header** and **Combined property string** fields, as shown in the example above.

The full Header should be as follows:

Item\tQuantity\tReference\tPart\tFootprint\tPartNumber\tSupplier\tCost

The \t inserts a tab space between the fields of data.

**Important:** If you do not have Excel loaded on your computer, do not enable the **Open in Excel** option.

3. In the **Combined property string** field, specify the properties whose values will go into the columns you defined in the previous step. The full string is as follows:

```
{Item}\t{Quantity}\t{Reference}\t{Value}\t{PCB  
Footprint}\t{PART_NUMBER}\t{VENDOR}\t{COST}
```

Property names are case-sensitive. The property names in the string *must* be enclosed in curly braces, {}. The sequence of property names corresponds to the sequence of column titles in the Header list.

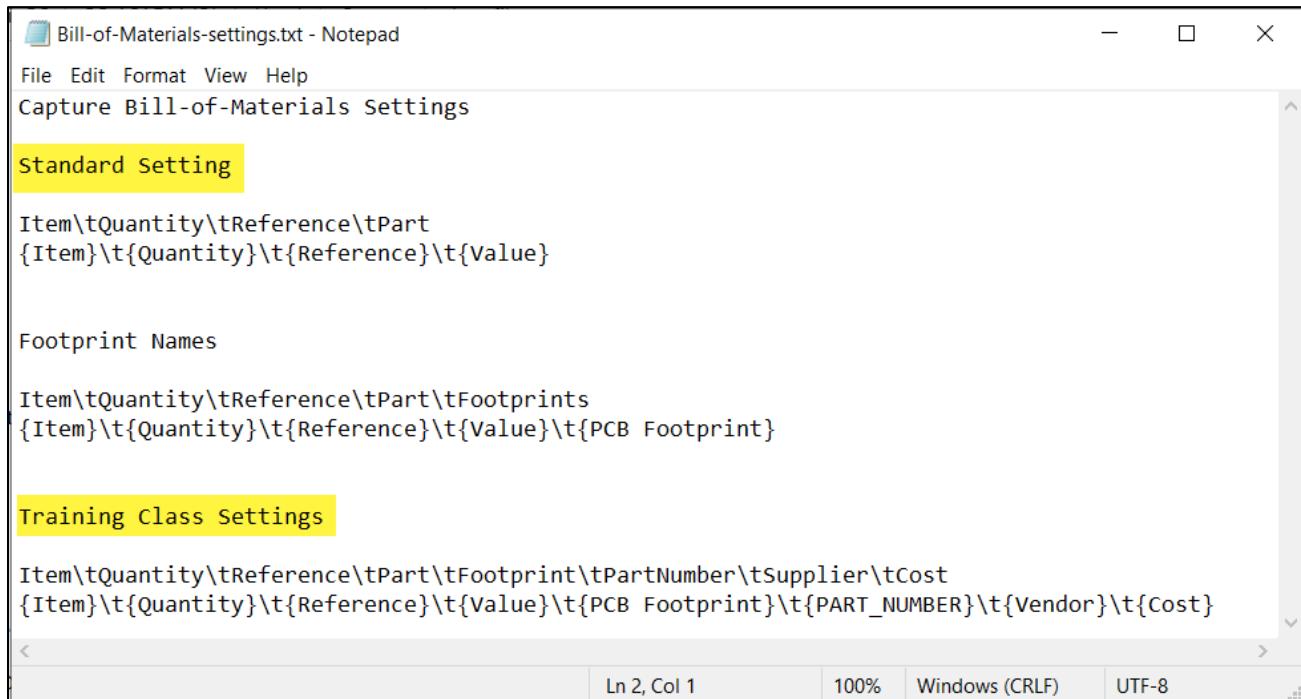
## Creating a Custom BOM Report

1. Turn on the **Open in Excel** option and click **OK** to display the Bill of Materials report in Excel.
2. Notice the new columns for Footprint, Part Number, Supplier, and Cost data.
3. Close the report.

### Saving Line Item Definitions (Optional Information)

The Header and Combined Property String values are saved in the *ProjectName.opj* file and will load automatically when the project is opened.

You can copy the Line Item Definitions from the BOM menu and save them in a text file to reuse in another design. You could have multiple BOM headers and line item definitions in the text file for different BOM requirements.



Bill-of-Materials-settings.txt - Notepad

File Edit Format View Help

Capture Bill-of-Materials Settings

**Standard Setting**

```
Item\tQuantity\tReference\tPart
{Item}\t{Quantity}\t{Reference}\t{value}
```

Footprint Names

```
Item\tQuantity\tReference\tPart\tFootprints
{Item}\t{Quantity}\t{Reference}\t{Value}\t{PCB Footprint}
```

**Training Class Settings**

```
Item\tQuantity\tReference\tPart\tFootprint\tPartNumber\tSupplier\tCost
{Item}\t{Quantity}\t{Reference}\t{Value}\t{PCB Footprint}\t{PART_NUMBER}\t{Vendor}\t{Cost}
```

Ln 2, Col 1 100% Windows (CRLF) UTF-8

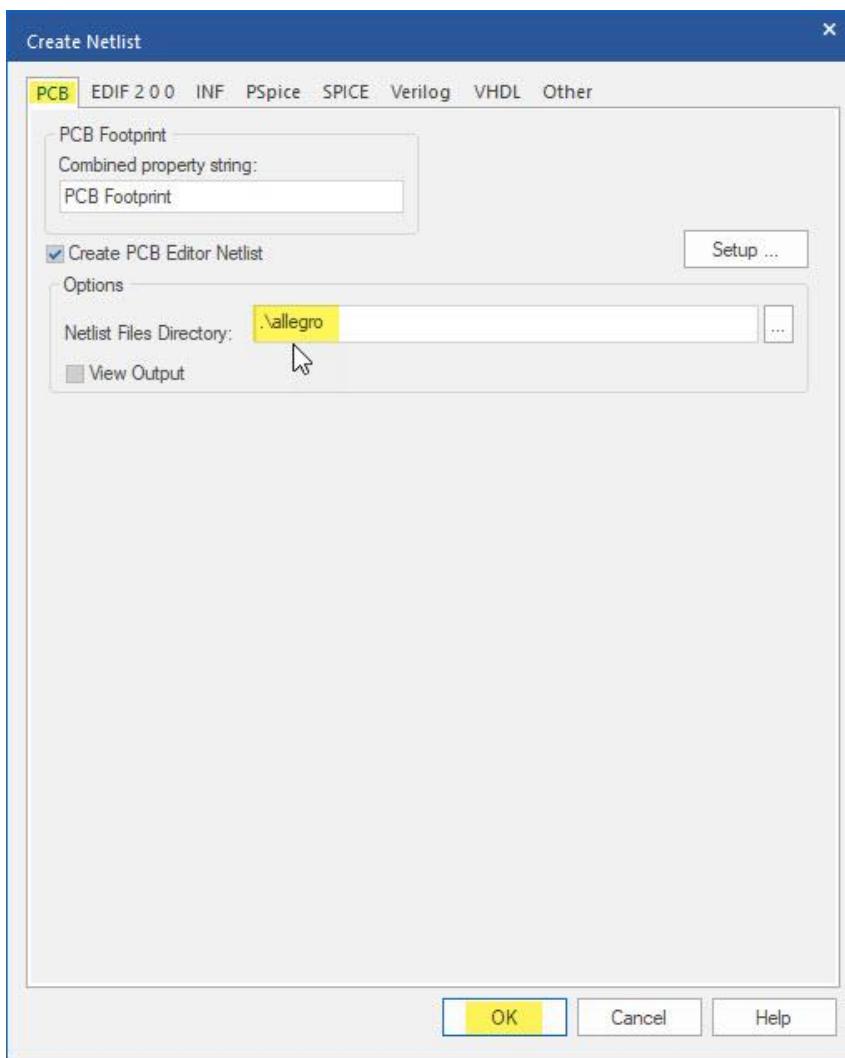
This screenshot shows a Notepad window titled "Bill-of-Materials-settings.txt". The content of the file is captured BOM settings. It includes sections for "Standard Setting" and "Training Class Settings", each with their respective property strings. The "Standard Setting" section contains the string "Item\tQuantity\tReference\tPart" followed by a template "{Item}\t{Quantity}\t{Reference}\t{value}". The "Training Class Settings" section contains the string "Item\tQuantity\tReference\tPart\tFootprint\tPartNumber\tSupplier\tCost" followed by a template "{Item}\t{Quantity}\t{Reference}\t{Value}\t{PCB Footprint}\t{PART\_NUMBER}\t{Vendor}\t{Cost}". The Notepad window also shows standard file menu options like File, Edit, Format, View, and Help, and status bar information like Ln 2, Col 1, 100%, Windows (CRLF), and UTF-8.



## Lab 7-7 Creating a Netlist for Allegro X PCB Editor/OrCAD X Presto

**Objective:** To create a netlist for Allegro® X PCB Editor/OrCAD X Presto.

1. Select the design name in the Project Manager window.
2. Choose **Tools – Create Netlist**.
3. Click the **PCB** tab and click **OK**.



4. When prompted to create an *allegro* subdirectory, click **Yes**.

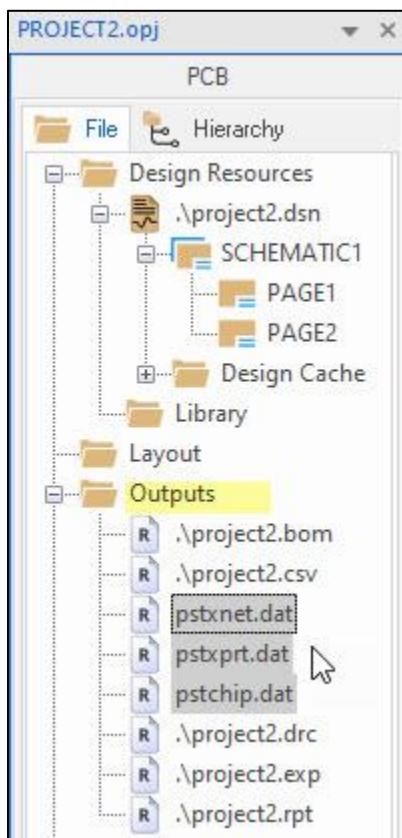
## Saving the Design

1. In the Project Manager window, select the design name **project2.dsn** and choose **File – Save**.

## Viewing Files in the Project Manager

Capture creates three netlist files in the *allegro* subdirectory; *pstchip.dat*, *pstxnet.dat*, *pstxprt.dat*.

1. Notice the outputs folder in Project Manager lists the three netlist files.



2. **Double-click** to open the *pstxnet.dat* file.  
This file contains all the signals in the schematic.
3. **Double-click** to open the *pstxprt.dat* file.  
This file contains all the parts in the schematic.
4. **Double-click** to open the *pstchip.dat* file.  
This file contains the library information for parts in the schematic design.

5. Locate the JEDEC\_TYPE property in this file and notice it corresponds to the PCB Footprint properties you assigned in the schematic.
6. Close the netlist files.

### Closing the Project

1. Click in the Project Manager window and choose **File – Close** to close the project.



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# **Module 8: Building a Hierarchical Design**

(c) Cadence Design Systems Inc. Do not distribute.

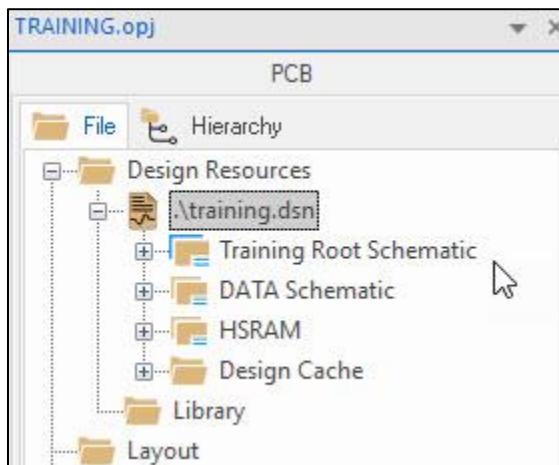
## Lab 8-1 Opening and Viewing a Hierarchical Design

**Objective:** To view an existing hierarchical design.

### Opening the Training Project

1. Choose **File – Open – Project**.
2. Navigate to the *C:\User1\Capture\training* directory and open the *training.opj* file.
3. In the Project Manager window, **double-click** *.\training.dsn* to expand the contents of the design file.
4. Notice that the design contains three schematic folders (*Training Root Schematic*, *DATA Schematic*, and *HSRAM*).
5. Notice the folder icon for *Training Root Schematic* looks slightly different.

The difference indicates the schematic is the root or top level of the hierarchy.



6. Click to expand each schematic folder.

Each of these folders contains a single schematic page, except *Training Root Schematic*, which has two.

### Viewing the Training Root Schematic

1. In the *Training Root Schematic* folder, **double-click** **PAGE2**.
2. Enlarge the session window and zoom to all.

## Building a Hierarchical Design

3. Notice the Online DRCs window along the bottom of the Capture work area.

This design contains some warnings that will be fixed later in this lesson.

4. Choose **View – Others – Online DRCs** to close the Online DRCs window.

You will resolve the warnings about one-pin nets later in the lab.

## Viewing the HSRAM Schematic

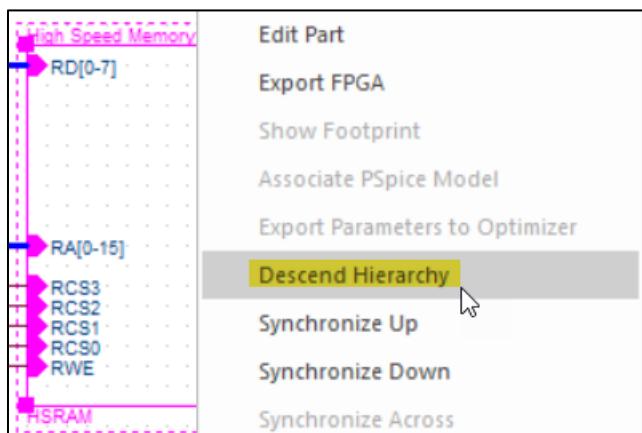
1. In the schematic window, locate the HSRAM and Data Schematic hierarchical blocks.

You can push through these block symbols to display their lower-level schematics.

2. In the schematic window, select the **HSRAM** block symbol.

3. **Right-click** and select **Descend Hierarchy**.

A second schematic window opens and displays the HSRAM schematic. This is the circuitry that the hierarchical block represents.



4. Close the HSRAM schematic window.

The Training Root Schematic window is still open.

## Viewing the Data Schematic

1. In the schematic window, select the **Data Schematic** block symbol.

2. **Right-click** and select **Descend Hierarchy** (or **double-click** to descend).

A second schematic window opens and displays the **Data Schematic**.

3. Close the **Data Schematic** window.

4. Close the **Training Root Schematic** window.

In this lesson, you will edit the Root and Data schematics.



## Lab 8-2 Editing the Training Root Schematic

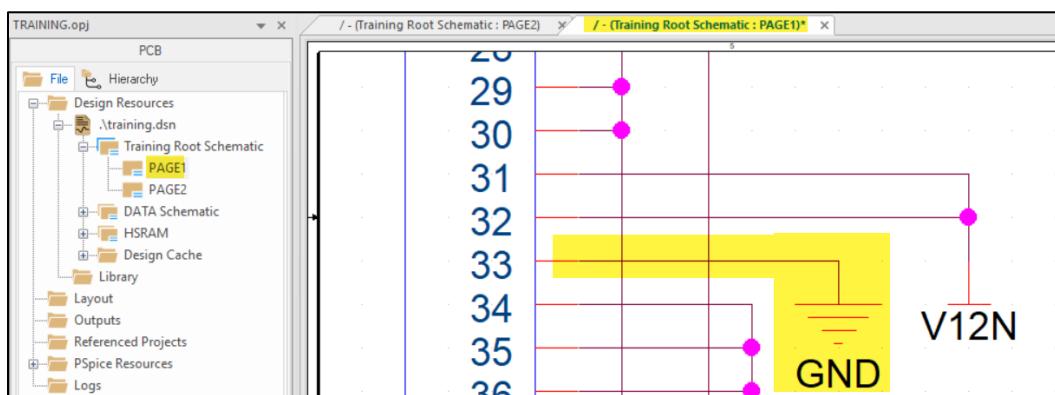
**Objective:** To complete the hierarchical design.

### Opening the Training Root Schematic

1. In the *Training Root Schematic* folder, double-click **PAGE1**.

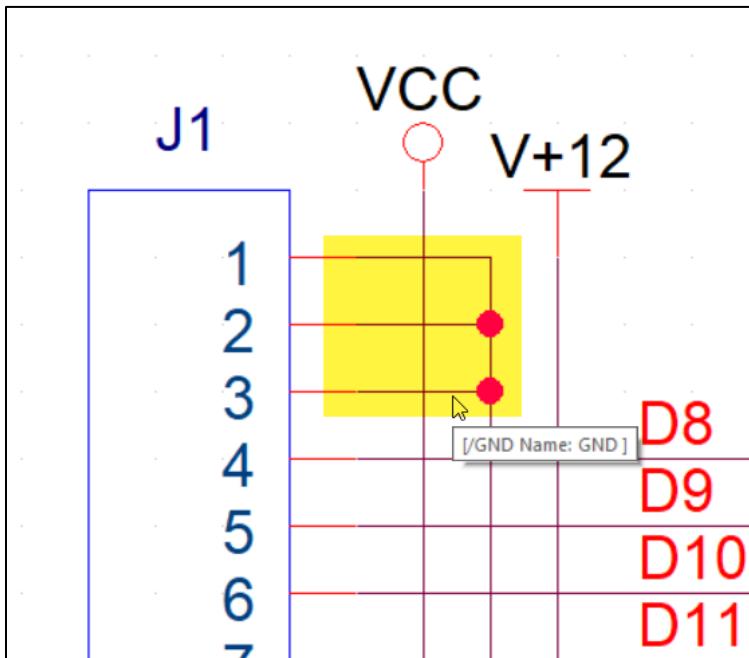
### Adding Ground to Connector J1

1. Locate the 64-pin connector (**J1**) along the left side of the page.
2. Notice that pins 1, 2, 3, and 33 are missing connections.
3. There are several ground symbols already on this page. Copy one of them and place it near pin 33, as shown below.



4. Click the **Place Wire** icon and connect pin **33** to the GND symbol.
5. Notice that when you connect a pin, the unconnected box at the end of the pin disappears.

6. Connect pins 1, 2, and 3 to the GND symbol, as shown below. If necessary, use the **i**, **o**, and **c** keys to zoom in or out and pan while adding the wire.



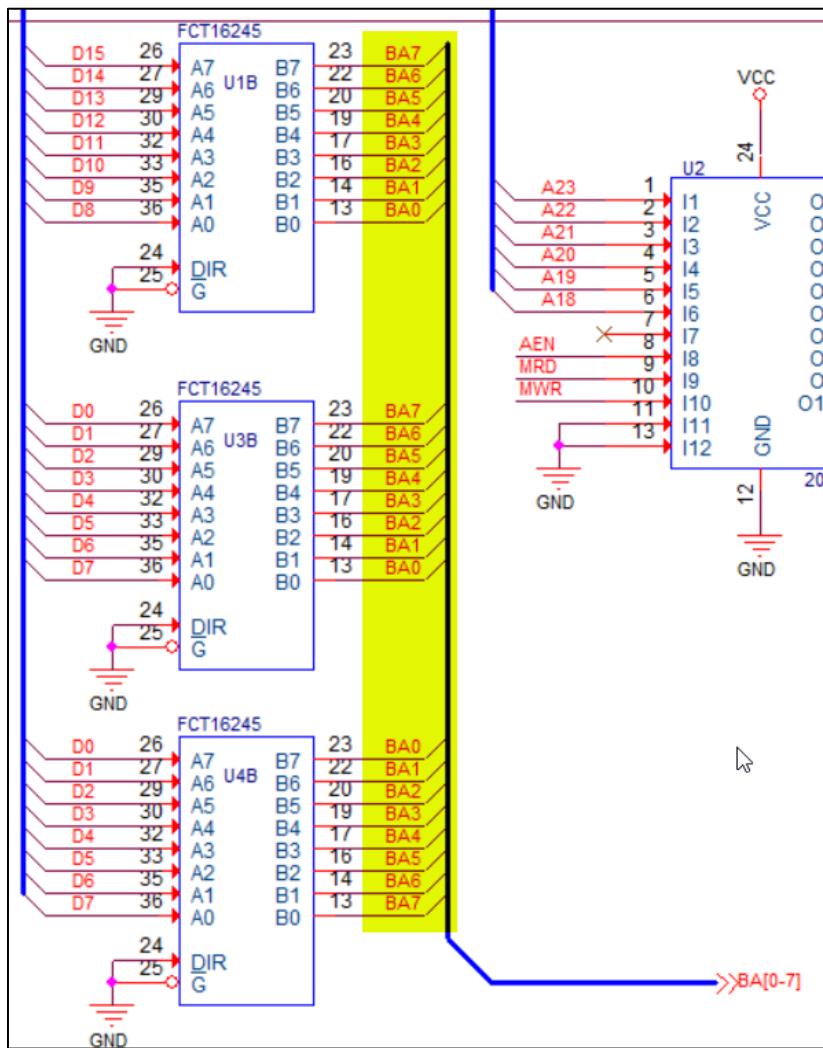
When a connection between two wires is made, a junction dot appears at the intersection.

7. Press **Esc** twice to end the command and deselect all objects.
8. Save the design.

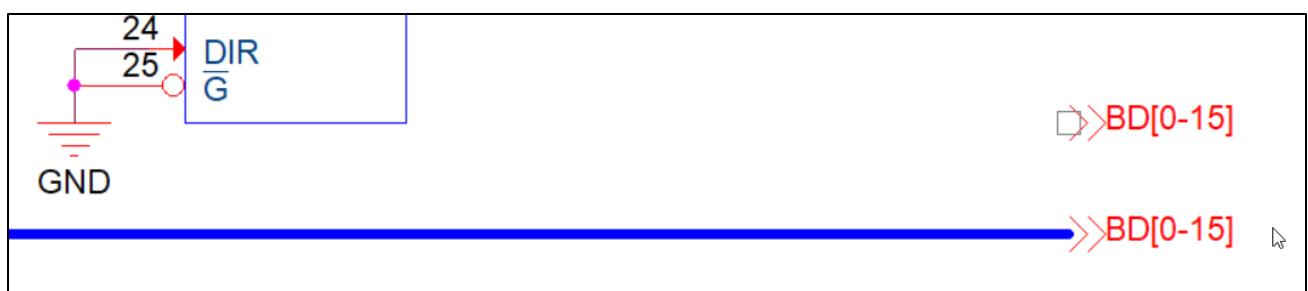
Building a Hierarchical Design

**Adding the BA[0-7] Bus**

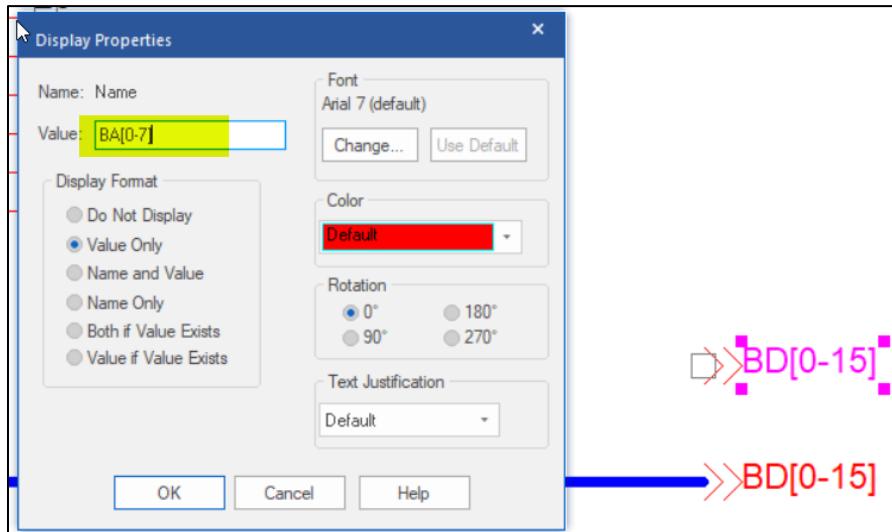
Page 1 of the training schematic contains six FCT16245 parts. Three of these parts are missing connections. You will add a bus to these three parts, as shown in the example below.



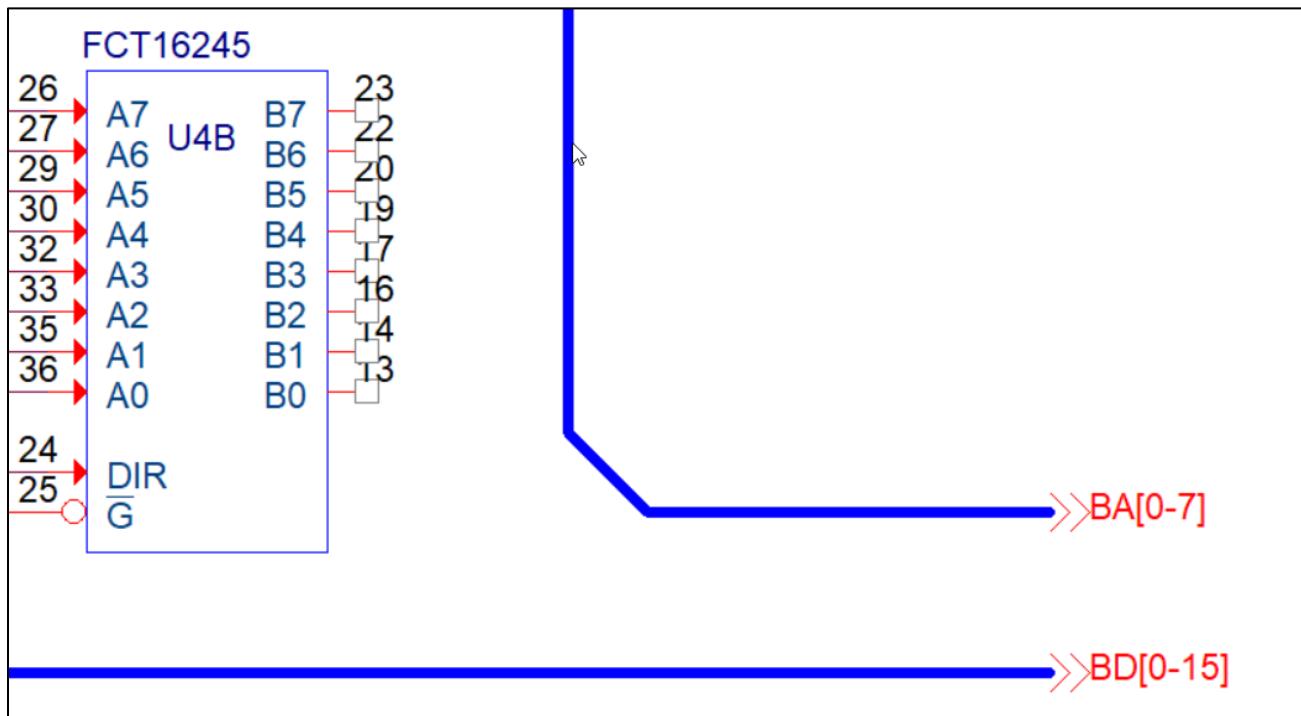
1. The first thing you will do is copy the existing BD[0-15] off-page symbol located in the lower-right corner. You can use Ctrl+C and Ctrl+V to copy and paste.



2. Double-click on just the associated text and change the value to **BA[0-7]**.

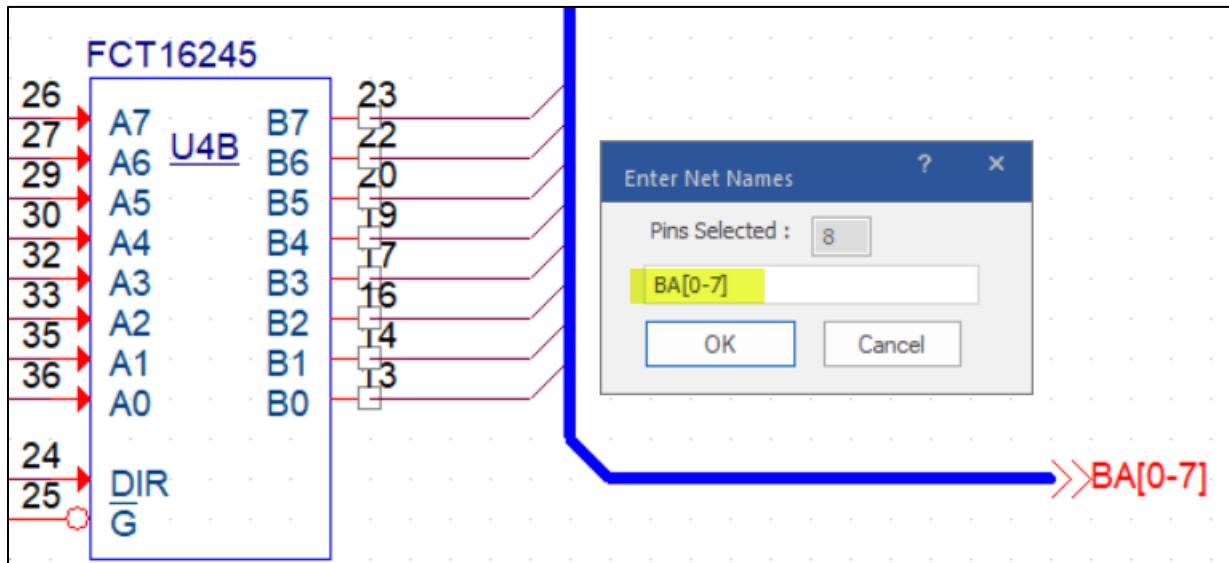


3. Choose **Place – Bus** (or use the Place Bus icon) and draw a bus wire from the Off-Page Connector symbol over to the FCT16245 part.



## Building a Hierarchical Design

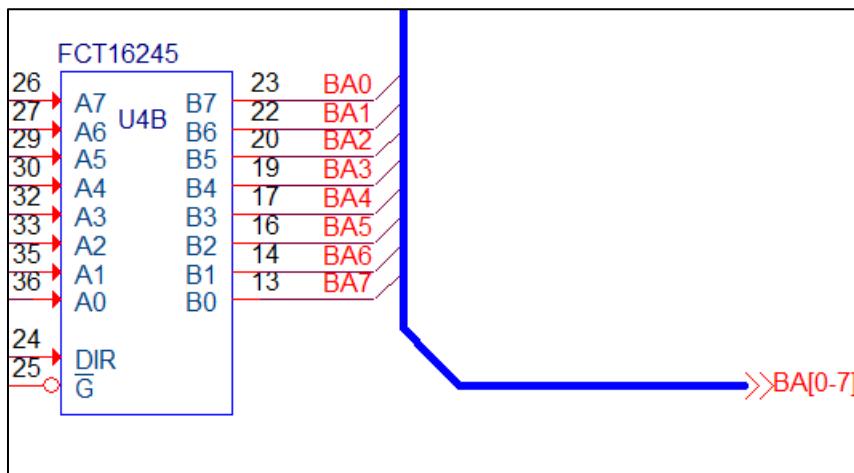
4. Choose **Place – Auto Wire – Connect to Bus** (or use the Auto Connect to Bus icon). Click to select each of the 8 pins of the FCT16245, then click on the bus wire.



The pins are automatically connected to the bus wire, and you are prompted for the net names of the new wires.

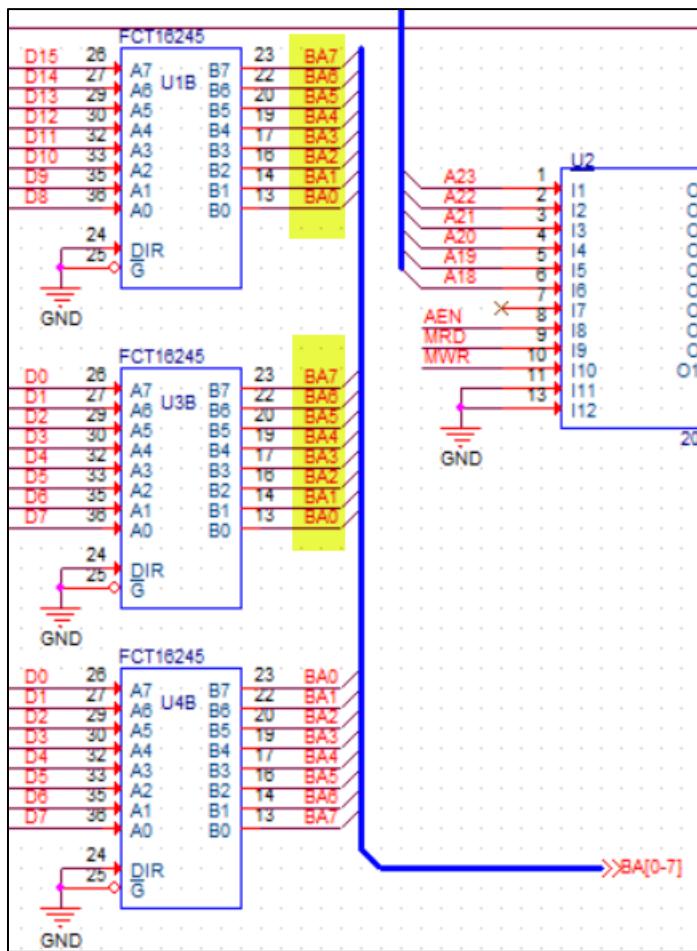
**Note:** The net names you provide will be assigned in a top-to-bottom order regardless of how you select the pins.

5. Enter **BA[0-7]** and click **OK**.



The net names are applied to the bus connections (always in the top to bottom order).

6. Next, you will similarly connect to the other two FCT16245 parts, as shown below.



## Saving Your Changes

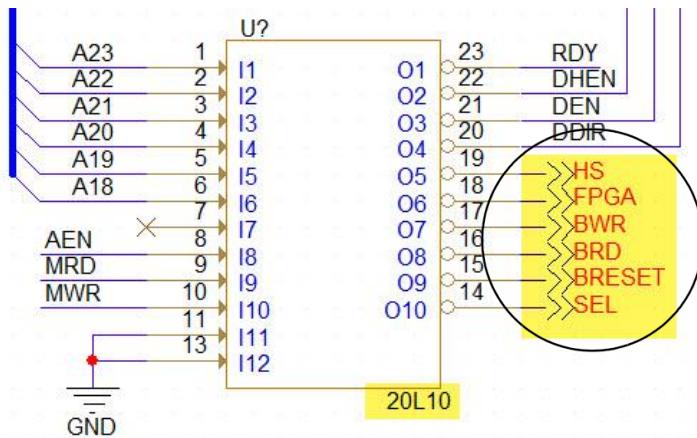
1. Choose **File – Save**.

Building a Hierarchical Design

## Adding Off-Page Connectors

1. Zoom into the **20L10** part in the upper-right corner of the page.

Use this example and the following steps to add the off-page connectors, as shown below.



2. Select the **Place Off-Page Connector** icon.



3. In the Place Off-Page Connector window, click the **CAPSYM** library and select **OFFPAGELEFT-R**.
4. In the Name field, enter **HS**.

5. Click **OK**.

The connector attaches to your cursor and is pointing left.

6. Press **r** twice to rotate it to point right.



7. Click to place the symbol near pin 19 of the 20L10 part. Leave at least one grid space to add a wire to the symbol.

**Note:** If you place the symbol directly on the pin, a connection is still created between the pin and the off-page connector. If you move the off-page connector, a wire is automatically added to maintain its connection to the pin.

8. Repeat this operation to place five more off-page connectors.

After placing each connector, press **Ctrl+E** and use the **Edit Off-Page Connector** window to specify the name of the next connector to be placed; use the names shown in the example above.

If you need to correct an off-page connector name, **double-click** on it.

9. Place a wire segment between the off-page connectors and the pins of the part.

## Saving Your Changes

1. Choose **File – Save**.

## Viewing Online DRC Warnings

1. Choose **View – Others – Online DRCs**.
2. Notice that the warnings about one-pin nets in the design have been removed from the Online DRCs window.

These warnings were resolved when you added the off-page connectors.
3. Close the Online DRCs window.

## A Note About Net Names

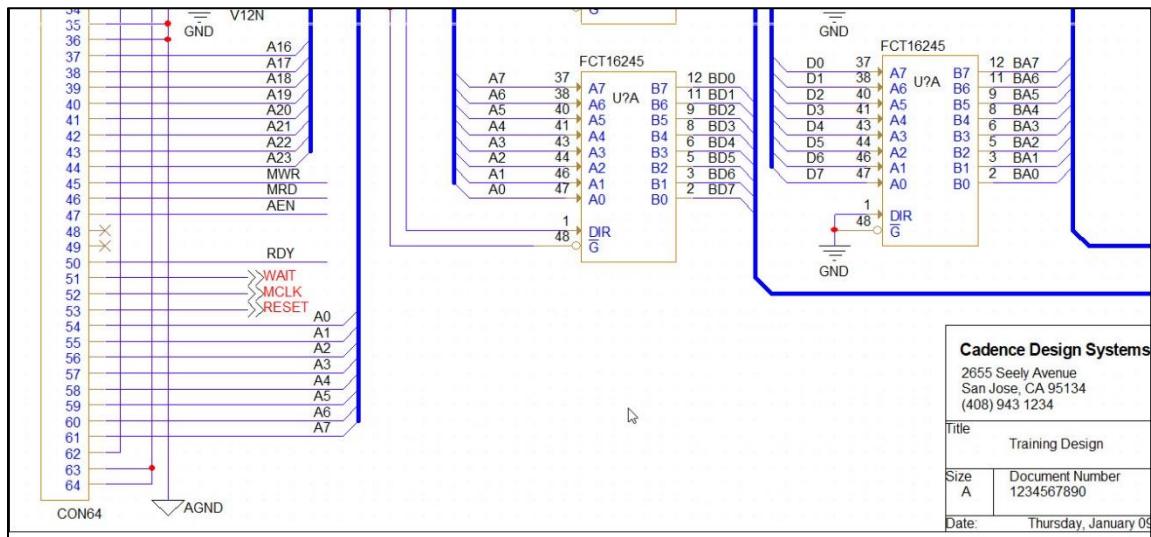
Beware of special characters in net names.

For the Allegro® X PCB Editor, avoid the exclamation point (!) and the single quotation mark ('). Also, avoid spaces and the use of the asterisk character in net names.

Building a Hierarchical Design

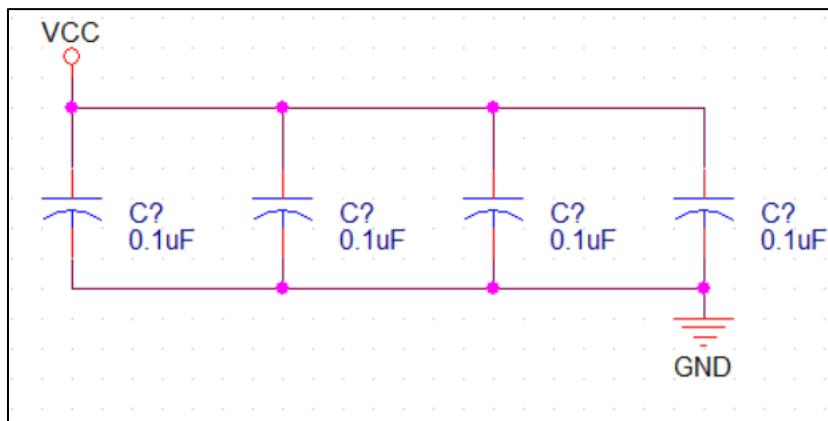
**Adding Bypass Capacitors**

1. Zoom in to the area shown below.



2. Click the **Place Part** icon.
3. In the Place Part pane, select the **DISCRETE** library and select **CAP** from the Part List.
4. Press **Enter**.  
*Do not place the part yet.*
5. Right-click and select **Edit Properties**.
  - a. In the Part Value field, enter **0.1uF**.
  - b. In the PCB Footprint field, enter **SM\_1206**.
6. Click **OK**.

7. Place four capacitors and add wires, as shown below.



You can copy existing **VCC** and **GND** symbols to complete the circuit.

8. Close the Place Part pane.

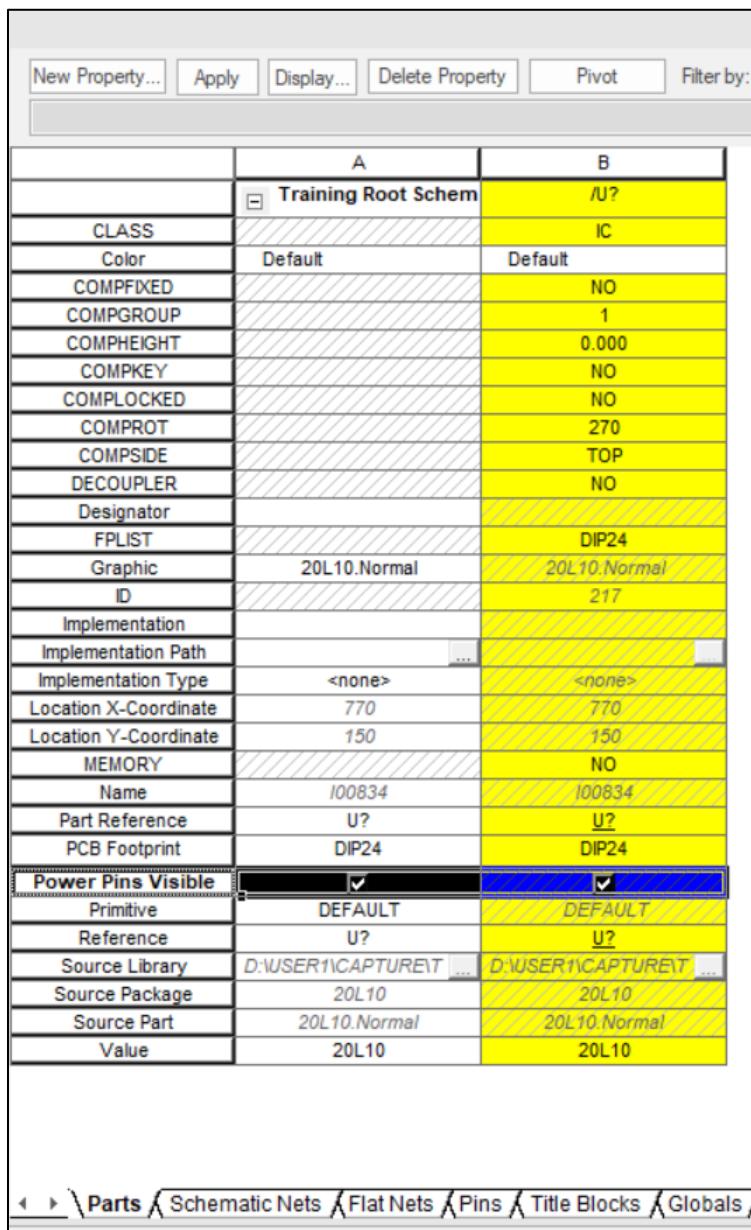
9. Save the design.



Building a Hierarchical Design

**Lab 8-3 Making Power Pins Visible****Objective:** To edit the visibility attribute of power pins.

1. Zoom into the upper-right corner of the page and **double-click** the **20L10** part.
2. Locate the **Power Pins Visible** property.
3. In the white column, select the **Power Pins Visible** checkbox, as shown below.



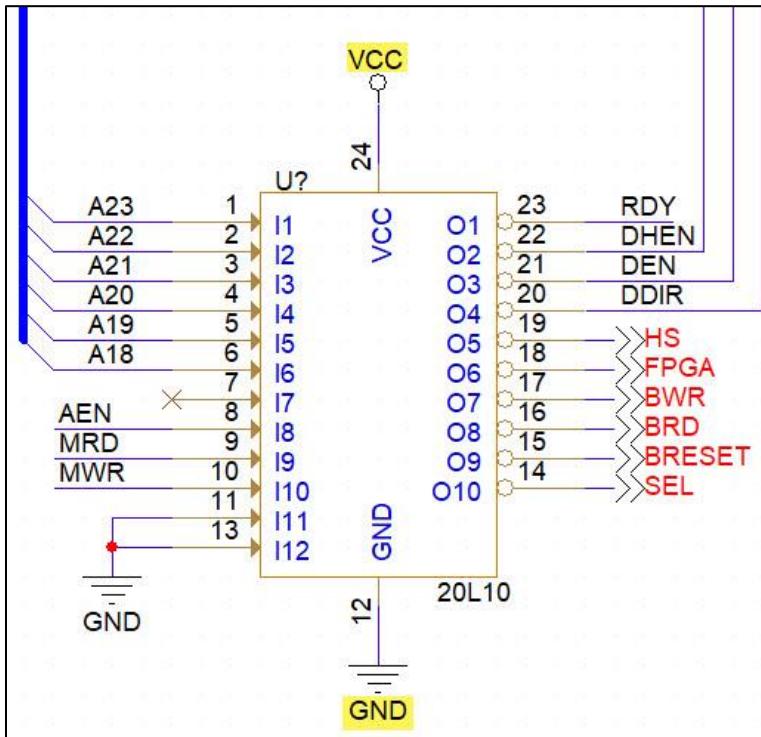
The screenshot shows the Cadence Property Editor window. At the top, there are buttons for 'New Property...', 'Apply', 'Display...', 'Delete Property', 'Pivot', and 'Filter by:'. Below this is a table with two columns, A and B. Column A lists properties, and Column B lists their values. The 'Power Pins Visible' property is located in the bottom section of the table. In Column A, it is listed under 'Implementation Path'. In Column B, it has a checked checkbox in the white column and a checked checkbox in the yellow column. Other properties listed include CLASS, Color, COMPFIXED, COMPGROUP, COMPHEIGHT, COMPKEY, COMPLOCKED, COMPROT, COMPSIDE, DECOUPLER, Designator, FPLIST, Graphic, ID, Implementation, Implementation Type, Location X-Coordinate, Location Y-Coordinate, MEMORY, Name, Part Reference, PCB Footprint, and Value. The 'Power Pins Visible' property is highlighted with a blue border.

	A	B
	A	B
Training Root Schema	Training Root Schema	/U?
CLASS		IC
Color	Default	Default
COMPFIXED		NO
COMPGROUP		1
COMPHEIGHT		0.000
COMPKEY		NO
COMPLOCKED		NO
COMPROT		270
COMPSIDE		TOP
DECOUPLER		NO
Designator		
FPLIST		DIP24
Graphic	20L10.Normal	20L10.Normal
ID		217
Implementation		
Implementation Path		
Implementation Type	<none>	<none>
Location X-Coordinate	770	770
Location Y-Coordinate	150	150
MEMORY		NO
Name	I00834	I00834
Part Reference	U?	U?
PCB Footprint	DIP24	DIP24
Power Pins Visible	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Primitive	DEFAULT	DEFAULT
Reference	U?	U?
Source Library	D:\USER1\CAPTURE\1...	D:\USER1\CAPTURE\1...
Source Package	20L10	20L10
Source Part	20L10.Normal	20L10.Normal
Value	20L10	20L10

At the bottom of the window, there is a navigation bar with icons for Parts, Schematic Nets, Flat Nets, Pins, Title Blocks, and Globals. The 'Parts' icon is highlighted.

The Secondary or yellow column shown in the Property Editor is explained later in the course.

4. Close the Property Editor.
5. Notice the power pins on the 20L10 part are now visible (top and bottom).
6. Copy a **VCC** symbol and connect it to pin 24 (at the top of the 20L10 part).
7. Copy a **GND** symbol and connect it to pin 12.



### Saving and Closing the Schematic

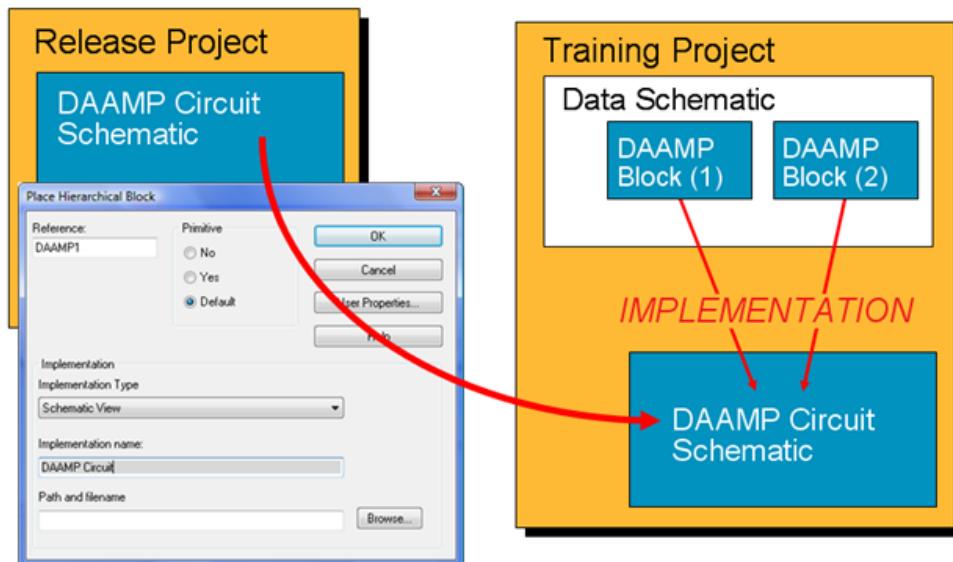
1. Choose **File – Save** to save the schematic page.
2. Close the schematic window.  
Do not close the project.

End of Lab

Building a Hierarchical Design

## Lab 8-4 Reusing a DAAMP Block

**Objective:** To reuse part of another design.

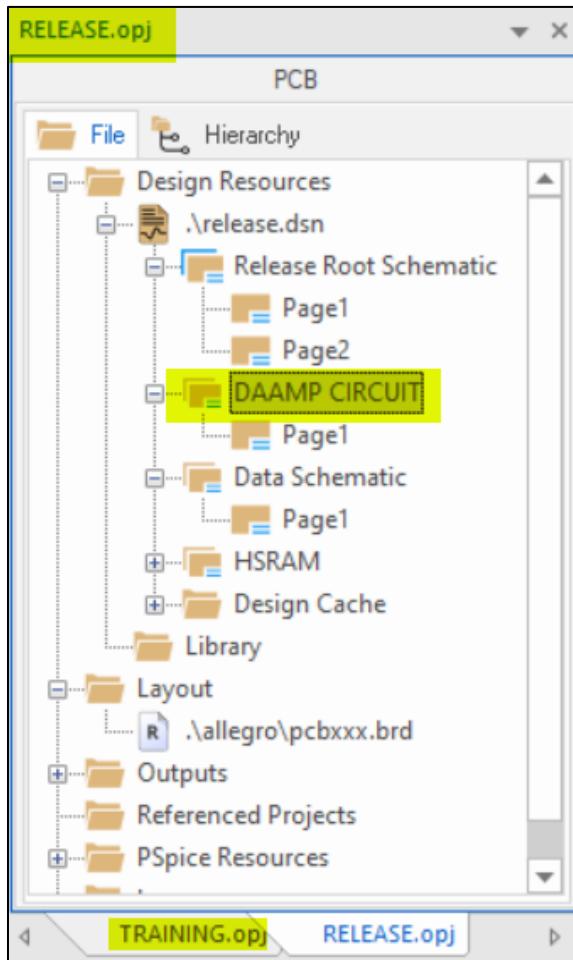


### Copying Between Projects

You should still have the *training* project open. You will now open a second project.

1. Choose **File – Open – Project**.
  2. Navigate to the *C:\User1\Capture\Release* directory and open the **release.opj** file.
- You now have two projects open.

3. Notice the Release project was loaded into the new tabbed window in the Project Manager and that it includes a **DAAMP CIRCUIT** folder.



4. **Right-click** on the **DAAMP CIRCUIT** folder and choose **Copy**.
5. Click on the **TRAINING.opj** tab at the bottom of the Project Manager window.
6. **Right-click** on the **training.dsn** file and choose **Paste**.
7. Save the training design.
8. Click on the **RELEASE.opj** tab and close the source project.

### Viewing the Copied DAAMP Design

1. **Double-click** the **DAAMP CIRCUIT** folder.

Building a Hierarchical Design

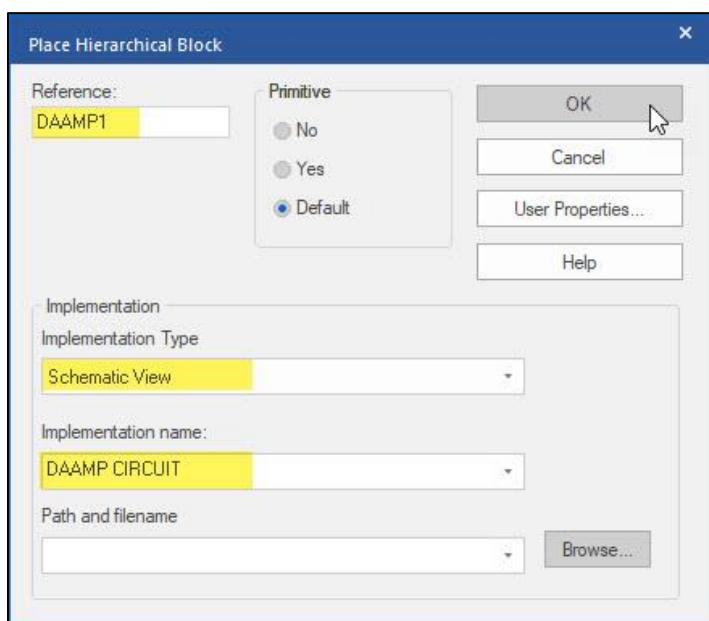
2. **Double-click** to open **PAGE1** of the DAAMP CIRCUIT.
3. Notice that this schematic contains hierarchical port symbols.  
These ported signals will tie to the pins of a hierarchical block symbol.
4. Close the DAAMP CIRCUIT schematic.

### Opening the DATA Schematic

1. **Double-click** **DATA Schematic** to expand the folder contents.
2. **Double-click** to open **PAGE1** of the DATA Schematic.

### Adding a DAAMP Block Symbol to the DATA Schematic

1. Click the **Place Hierarchical Block** icon, or choose **Place – Hierarchical Block**.   
The Place Hierarchical Block window opens. Use this window to define the schematic that the hierarchical block represents.
2. In the Reference field, enter **DAAMP1**.
3. Toggle the Implementation Type field to **Schematic View**.
4. Toggle the Implementation name field to **DAAMP CIRCUIT**.



**Note:** Because DAAMP CIRCUIT was copied to the training project, you will leave the Path and filename field blank. This is called an *internal reference*. If the DAAMP CIRCUIT were not copied into the training project, you would use the Path and filename field to define the location of the *release.dsn* file. This is called an *external reference*.

5. Click **OK**.

You are now ready to draw the rectangle for a hierarchical block.

6. To the right of one of the **74ACT574** parts, click and drag a rectangle for the hierarchical block.

The block automatically contains a hierarchical pin for each of the ported signals in the **DAAMP CIRCUIT** schematic.

7. Press **Esc** to deselect the hierarchical block.

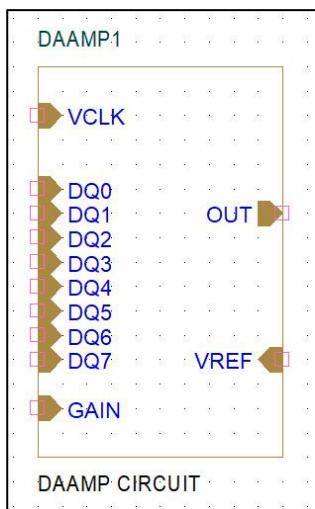
8. Zoom in to see the block symbol.

9. To change the size of the rectangle, select the **DAAMP1** symbol. Drag one of the corners to resize the rectangle.

10. Press **Esc** to deselect.

11. To move a pin, press and hold the mouse button and drag it to a new location along the edge of the rectangle.

12. Arrange the pins as shown.



Building a Hierarchical Design

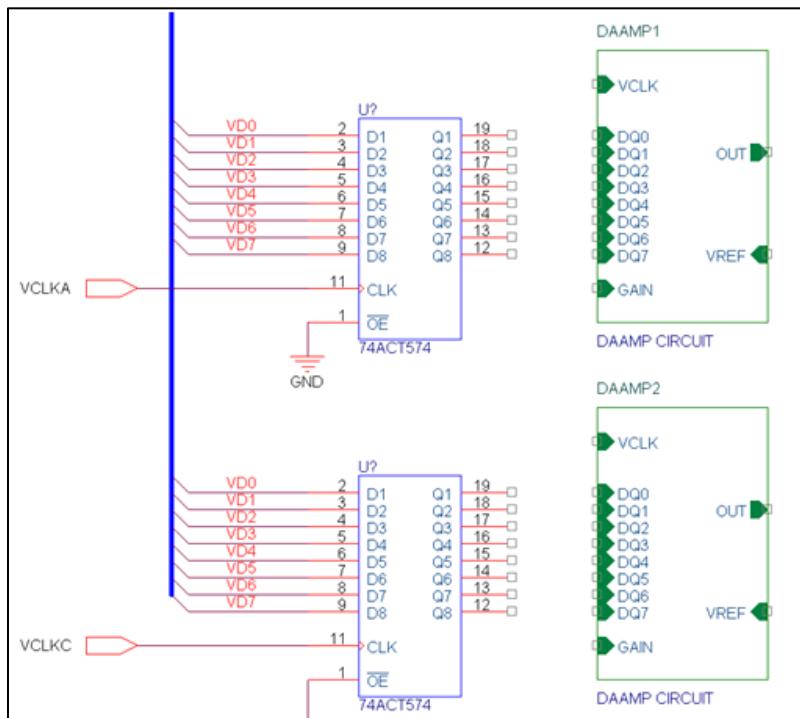
**Instantiating Another DAAMP Block**

1. Select the **DAAMP1** symbol. **Right-click** and select **Copy**.

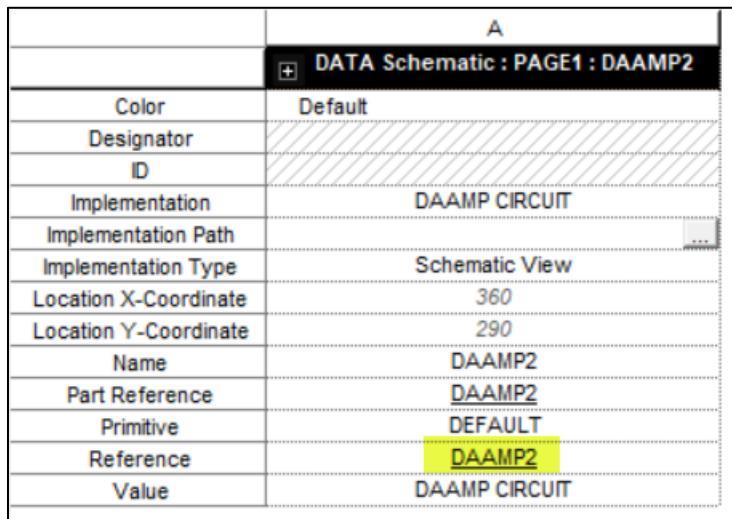
2. Press **Esc** to deselect the symbol. **Right-click** and select **Paste**.

A copy of the block symbol is attached to your cursor.

3. Click to place the copy to the right of the other 74ACT574 part, as shown below.



4. Edit the properties of the second block symbol and set its Reference to **DAAMP2**.



5. Close the Property Editor and press **Esc** to deselect.

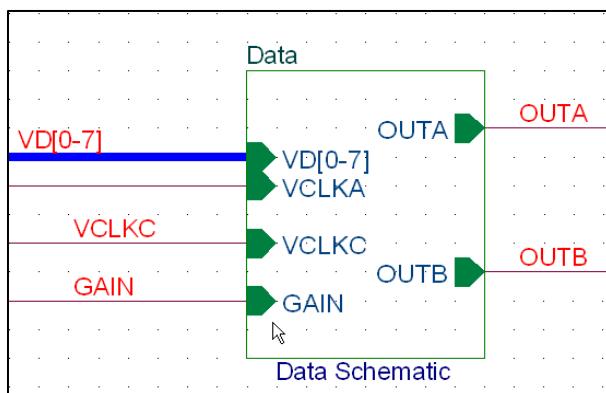
If the *Automatically reference placed parts* option was selected in the **Options – Preferences – Miscellaneous** window, Capture would have automatically named the second hierarchical block **DAAMP2**. This option has not been selected for this lab.

## Saving Your Work

1. Save the Data schematic.

## Synchronizing the DATA Schematic and Block Symbol

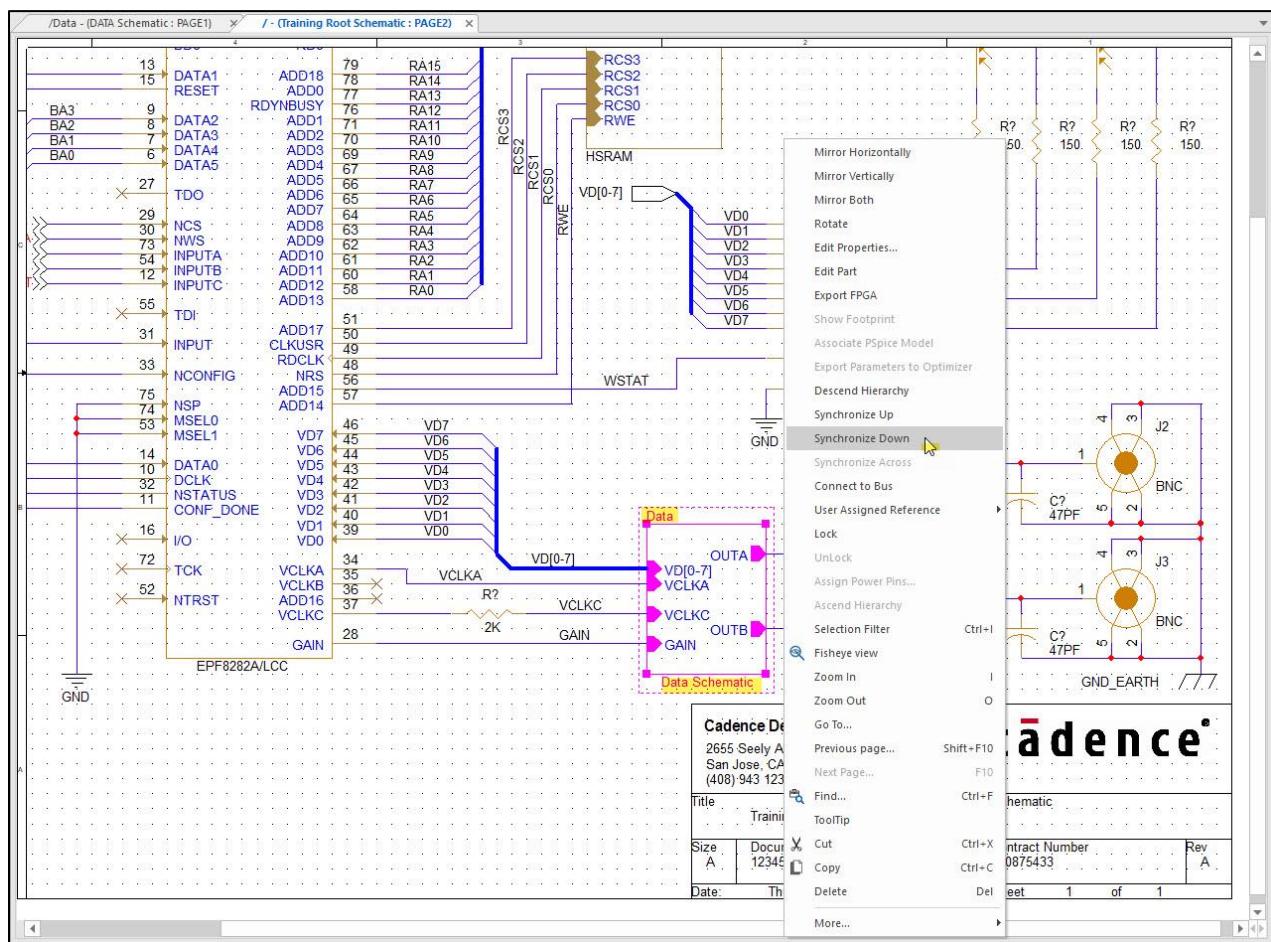
1. Click the **Zoom to All** icon in the toolbar.
2. Notice that the DATA schematic you are currently editing has three port symbols. These port symbols correspond to pins on a DATA block symbol, which is already in the Training Root Schematic.
3. To view the DATA block symbol from the Project Manager window, open **PAGE2** of the Training Root Schematic.
4. Locate the DATA block symbol located at the bottom-center portion of the page and notice the hierarchical pins on this block symbol.



The DATA block symbol contains six pins; three of these pins do not exist in the DATA schematic (yet). You will now synchronize the DATA schematic to this DATA block symbol.

## Building a Hierarchical Design

5. Select the DATA block symbol, right-click and select **Synchronize Down**.



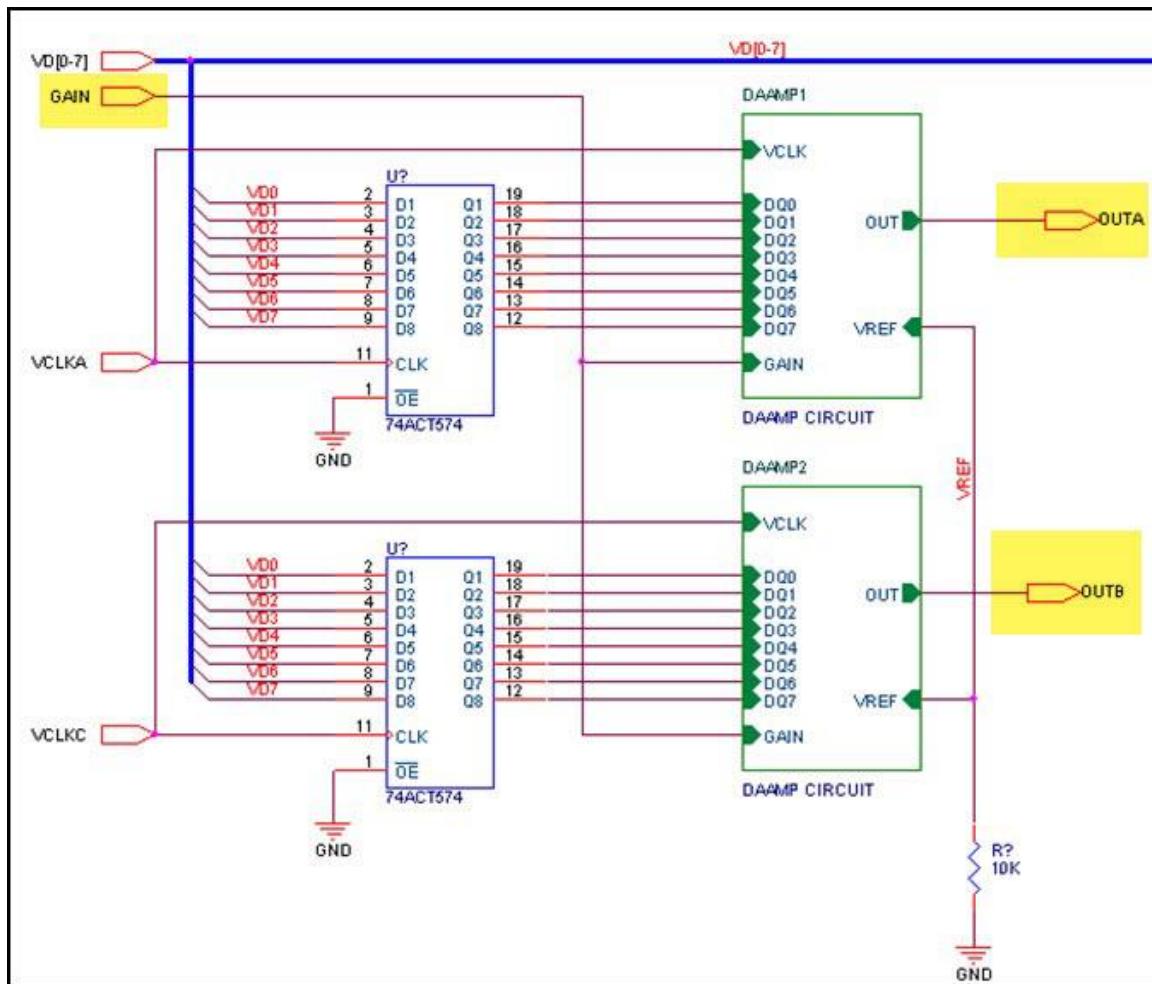
The modified DATA schematic is displayed. It was missing ports but is now in sync with the DATA block symbol. The new ports *OUTA* and *OUTB* are located on the right side of the page, and *GAIN* is situated on the left side of the page.

### Saving Your Work

1. Click on the design file in the Project Manager and choose **File – Save**.
2. Close PAGE2 of the Training Root Schematic.

## Finishing the DATA Schematic

A portion of *PAGE1* of the *DATA* schematic is shown below. Use this as a guide to help you follow lab instructions and complete the schematic.

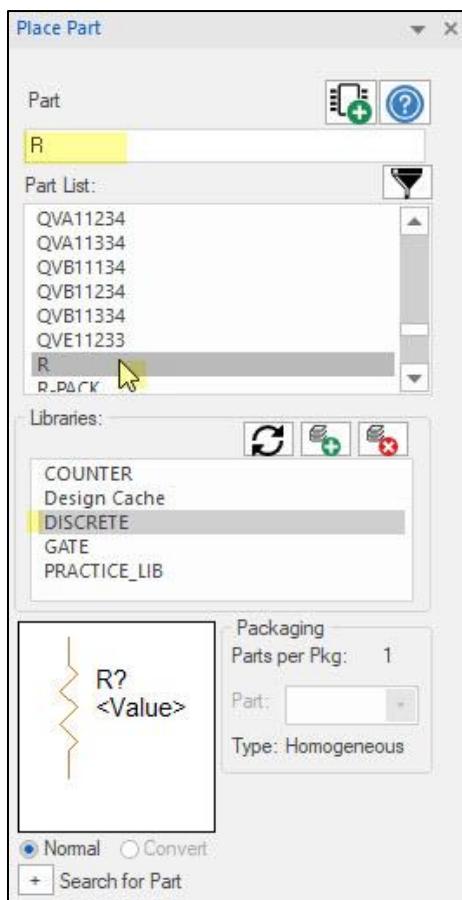


1. Move the *GAIN*, *OUTA*, and *OUTB* port symbols as shown in the example.
2. Add connections from the *DAAMP1* and *DAAMP2* blocks to each of the *74ACT574* parts.
 

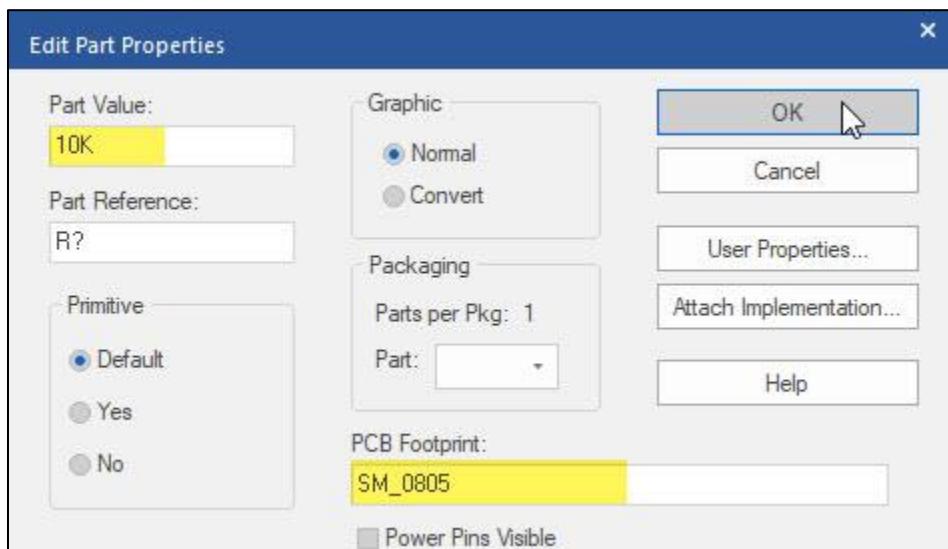
**Tip:** A quick way to add connections is to move a block symbol so that its pins touch the pins of a *74ACT574*. (This creates a connection between the overlapping pins.) Then, move the block symbol back and notice that wires are automatically added between the two parts.
3. Add wires to hierarchical ports *OUTA* and *OUTB* of both blocks.
4. Add wires from the *GAIN* input port to the *GAIN* pin of *DAAMP1* and *DAAMP2*.

## Building a Hierarchical Design

5. Connect the VCLKA port to the **VCLK** pin on DAAMP1. Connect the VCLKC port to the **VCLK** pin on *DAAMP2*.
6. Select a resistor from the *DISCRETE* library, as shown below.



- a. Right-click and set the Part Value to **10K** and PCB Footprint to **SM\_0805**.



- b. Place near the lower-right corner of *DAAMP2*.
  - c. Connect one end of the resistor to the *VREF* pins on both blocks.
  - d. Copy a **GND** symbol and connect it to the other end of the resistor.
7. Close the Place Part window.

### Saving the Design

1. Choose **File – Save**.
2. Close the DATA schematic.
3. In the Project Manager, click on the design file and choose **File – Save**.  
Do not close the training project.

### Optional Lab

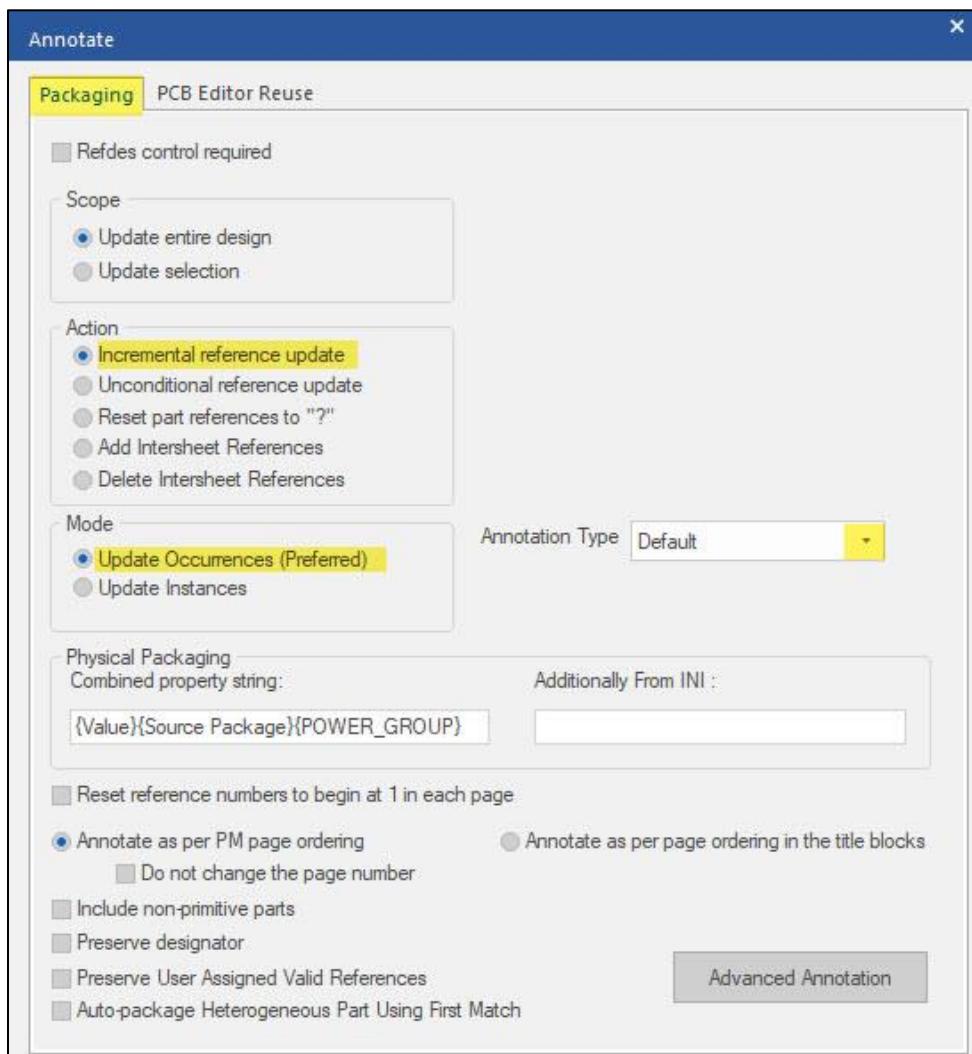
After class, see **Appendix A: Optional Topics, Lab A-4: Manually Creating a Hierarchical Block Symbol**.



## Lab 8-5 Annotating the Design

**Objective:** To assign reference designators to the hierarchical design.

1. In the Project Manager window, select **training.dsn** and choose **Tools – Annotate**.
2. In the Action section, select **Incremental Reference Update**.  
This choice maintains any designators that are already in the design. Connectors J1, J2, and J3 are already annotated.
3. Under Mode, the **Update Occurrences (Preferred)** option should be selected by default. If not, select it.
4. Toggle the Annotation Type field to **Default**.



5. Click **OK** to annotate the design. Click **OK** again to continue.  
The design is annotated and saved to disk.

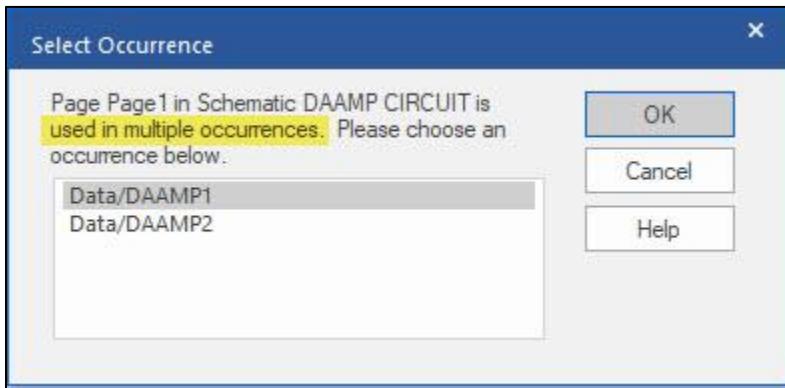
## Viewing Reference Designator Assignments

When annotating a hierarchical design, Capture annotates the root schematic first, followed by the other schematic folders in the order they appear in the Project Manager (sorted alphabetically).

1. Open **PAGE1** of the *DATA* schematic.  
Notice all the parts now have reference designators.
  - a. Select the **DAAMP1** block symbol. **Right-click** and select **Descend Hierarchy** (**double-click** or press **Shift+D**).  
The underlying schematic is displayed.
  - b. Notice some of the reference designators assigned to these parts.
  - c. **Right-click** and select **Ascend Hierarchy**.
  - d. Descend into the **DAAMP2** block.  
Both schematics for the *DAAMP* blocks should now be open.
2. Use the tabs at the top of the work area to toggle between the two occurrences of the *DAAMP CIRCUIT* schematic.
3. Notice that each page is the same schematic but with different reference designators.  
The parts in the *DAAMP CIRCUIT* schematic occur twice in the design because there are two *DAAMP* blocks in the hierarchy. This is known as a *complex hierarchy* and is the reason Capture differentiates between instances and occurrences.
4. Close all three schematic windows.
5. In the Project Manager, **double-click** **PAGE1** of the *DAAMP CIRCUIT* folder.

Building a Hierarchical Design

6. Notice that you are prompted for a specific occurrence of the schematic page (*DAAMP1* or *DAAMP2*), as shown below.



7. Select the **Data/DAAMP1** entry and click **OK**.

The schematic associated with the *DAAMP1* block symbol is displayed.

8. Close the schematic window.

9. In the Project Manager, select **training.dsn** and save the design.

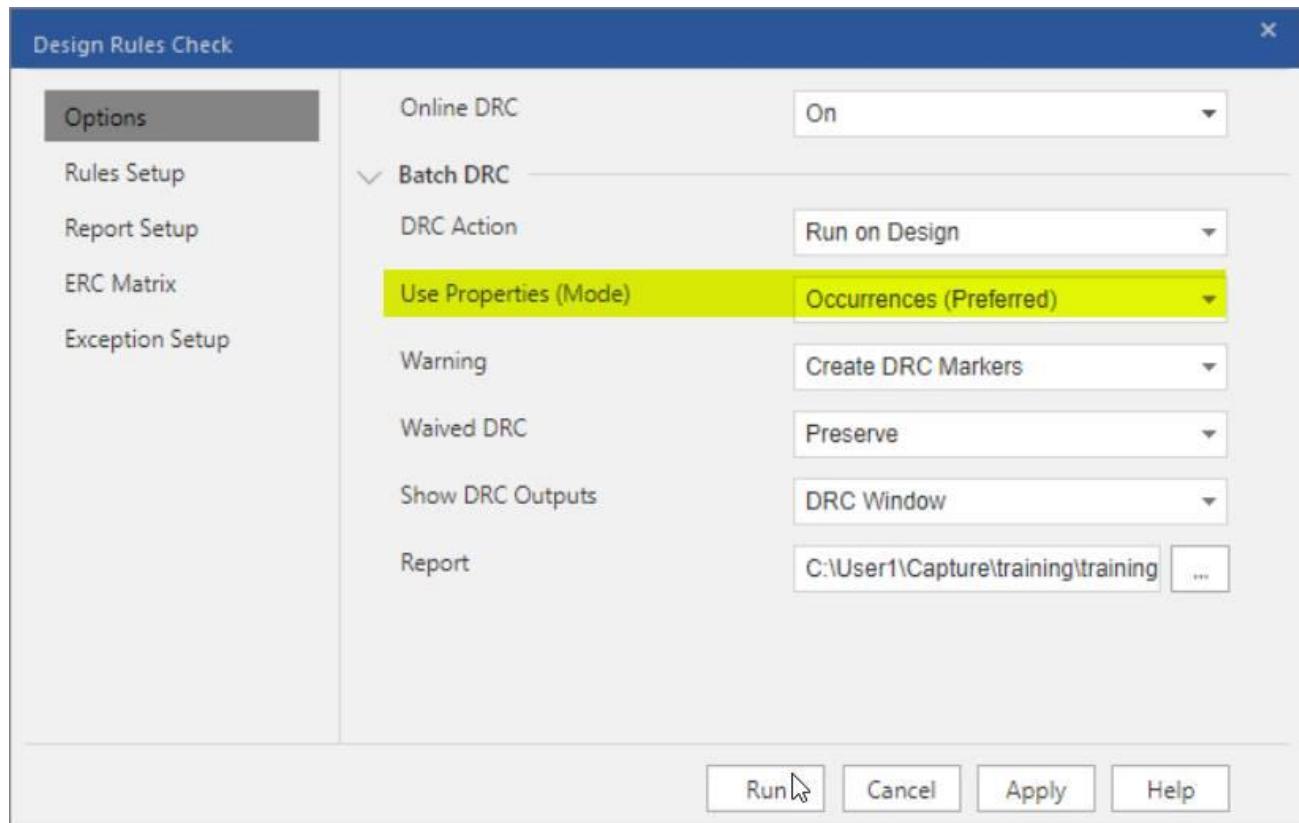


## Lab 8-6 Running Design Rules Check

**Objective:** To check the hierarchical design for design rule violations.

### Setting Up the Design Rules Check

1. Select **training.dsn** in the Project Manager window.
2. Choose **PCB – Design Rules Check**.
3. In the Options tab of the Design Rules Check window, set the options shown below.

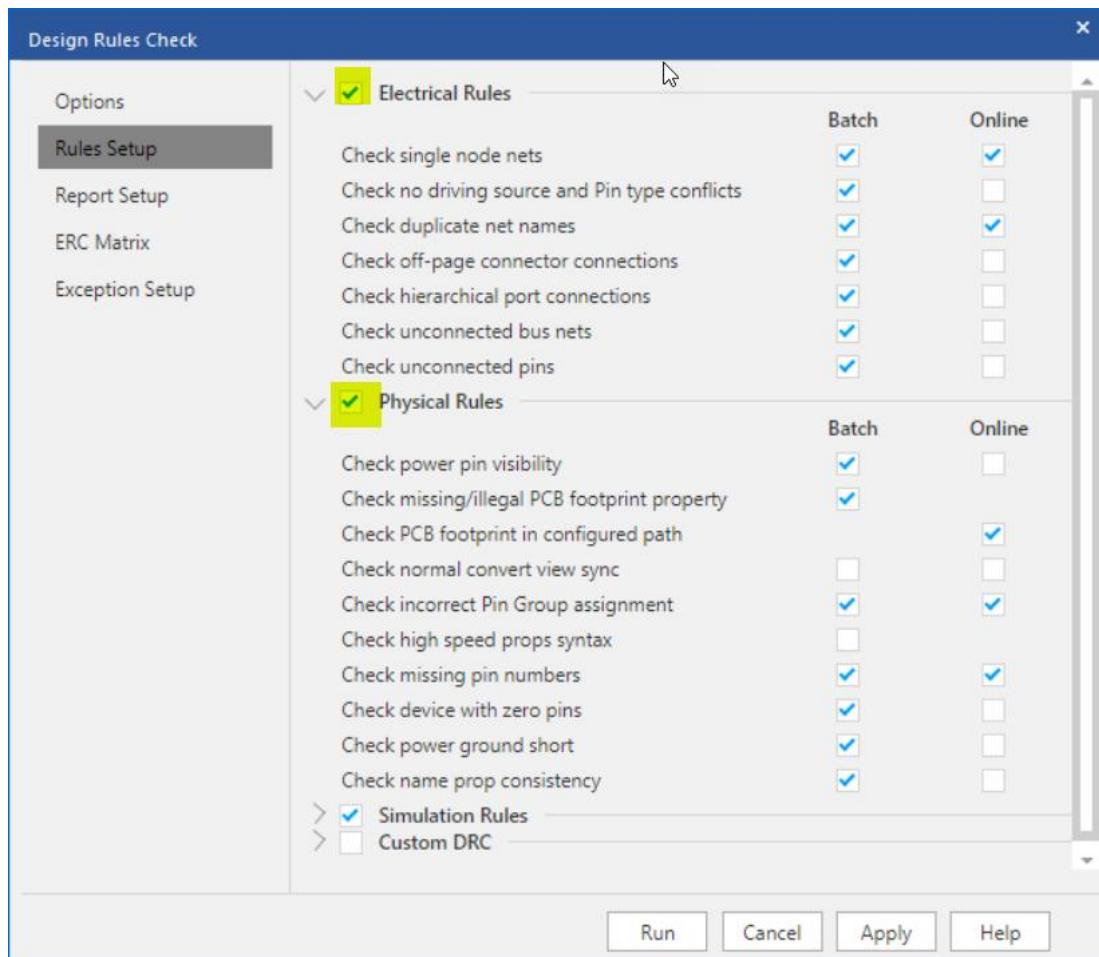


4. Make sure you have *C:\User1\Capture\training\training.drc* listed in the Report File field. If not, enter it or click **Browse** to add the directory.

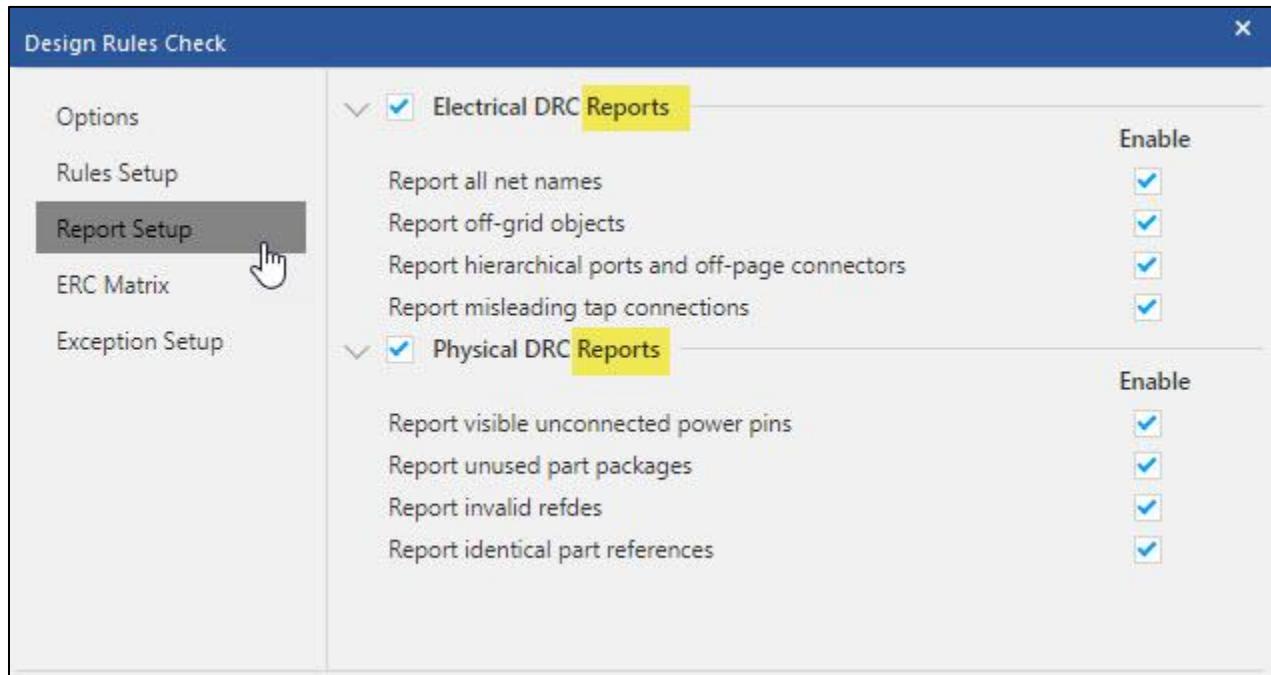
**Note:** Remember to adjust the path so it reflects the location of the *Capture* folder on your system.

## Building a Hierarchical Design

5. Click the **Rules Setup** tab and set the Electrical and Physical Rules, as shown below.



6. Click the **Report Setup** tab and set the Electrical and Physical Reports, as shown below.



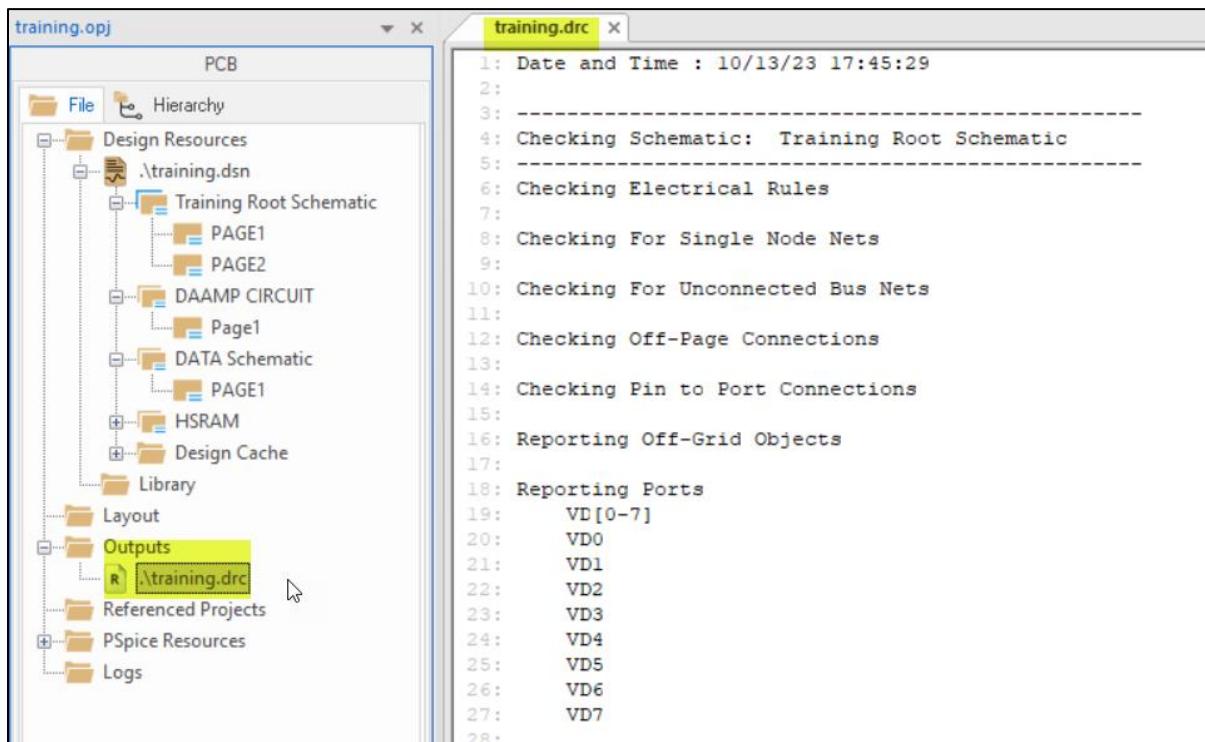
7. Click **Run**.
8. When prompted to view messages in the session log, click **No**.

### Reviewing the DRC Report

1. Notice the DRC window at the bottom of the session window shows warnings about possible shorted nets.  
You will resolve these warnings in the next lab.
2. Close the DRC window.

## Building a Hierarchical Design

3. Double-click the training DRC report in the Project Manager's Outputs folder.



4. Notice this report contains five sections, one for each of the schematic folders in the design. Scroll through the report to locate these five sections:
  - Training Root Schematic
  - HSRAM
  - DATA\_Schematic
  - DATA/DAAMP1 Circuit
  - DATA/DAAMP2 Circuit
5. Notice the end of the report lists the same warnings about possible shorted nets.
6. Close the **DRC** report window.

End of Lab

## Lab 8-7 Waiving DRCs

**Objective:** To suppress DRC errors in the schematic and report.

---

### Viewing the Error Markers

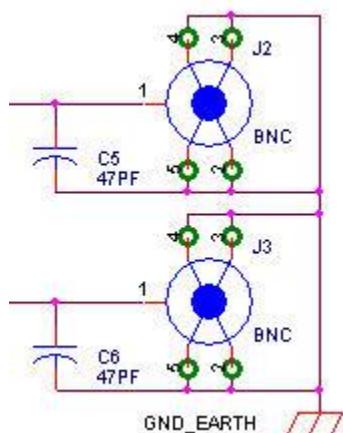
1. Choose **View – Others – DRCs**.

The DRC window shows 12 warnings for nets that have two or more aliases. There are DRC markers on the schematic pages for errors and warnings.

2. In the DRC window, **double-click** on a warning to highlight it in the schematic.

For example, many of the DRC markers are on PAGE2 of the Training Root Schematic.

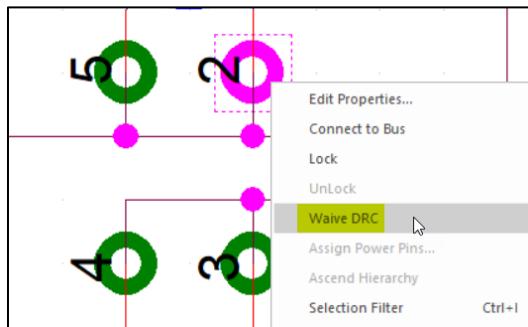
3. Zoom into the DRC markers in the lower-right corner of the page.



Each of these BNC connectors has four voltage pins. In the library part, each of these voltage pin names must be unique; for example, G2, G3, and G4, and the pin name represents the voltage net name. In the design, they all tie to the GND\_EARTH voltage symbol. Once you've verified that these connections don't represent shorts, you can waive these DRC errors.

## Waiving DRCs in Schematic and Report

1. Click on a DRC marker.
2. Right-click and select **Waive DRC**.



3. Press **Esc**.  
The DRC marker disappears.
4. Use **Ctrl+left** click to select the other DRC markers on this page and waive them also.
5. Save the page.
6. In the Project Manager, select the design name **training.dsn**.
7. Choose **PCB – Design Rules Check** and click **Run**.
8. Click **No** to continue.
9. Notice the DRC window contains a Waived column at the far right.  
The warnings you waived now show **Yes** in the Waived column.
10. Close the DRC window.

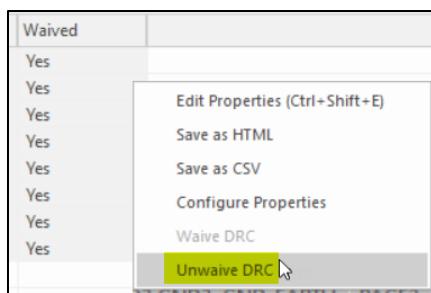
## Restoring Waived DRC Markers

1. In the Project Manager, select the design name **training.dsn**, then right-click and choose **Find**.
2. In the Find tab, set the search filter to **DRC Markers** only.

3. Enter an asterisk (\*) in the search field and click **Find**.

The DRC window reopens.

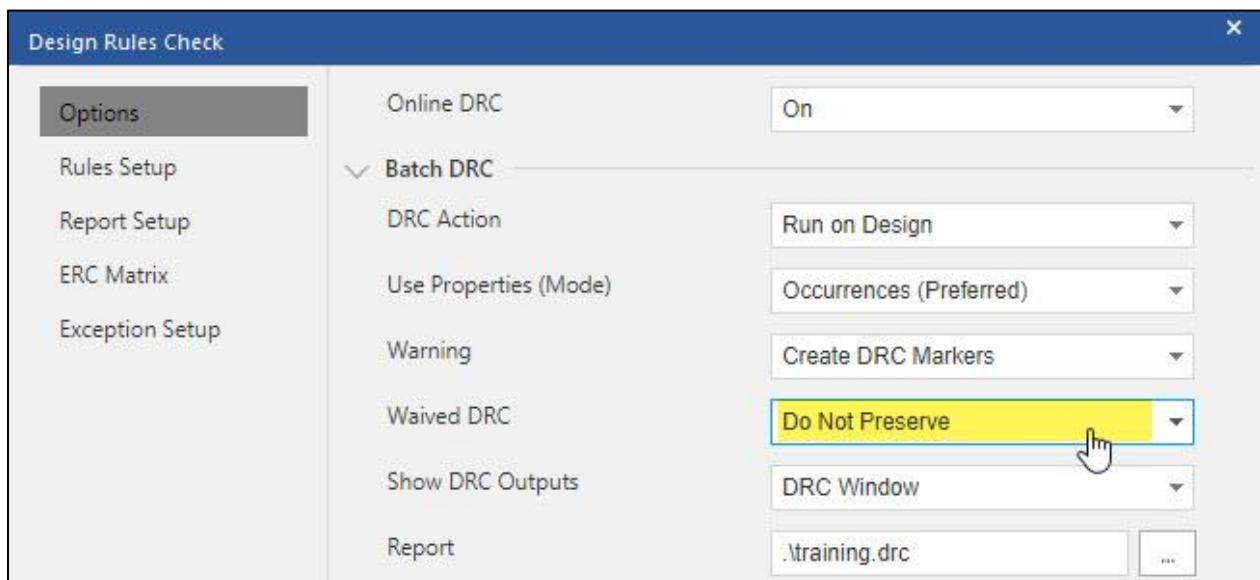
4. In the DRC window, **Shift+Click** to select all waived warnings, then **right-click** and select **Unwaive DRC**.



5. Notice on the schematic page the 8 DRC markers are restored, and the DRC window shows **No** in the Waived column.
6. Close the Find window and close the DRC window.
7. Save and close the schematic page.

### Alternate Method for Restoring Waived DRCs

1. Another way to restore waived DRCs is to choose **PCB – Design Rules Check**.
2. In the **Options** tab, toggle the Waived DRC option to **Do Not Preserve**.



When you run DRC with this setting, all waived DRC markers will be restored.

3. Click **Cancel**.



## Lab 8-8 Hierarchical Cross Referencing and Plotting

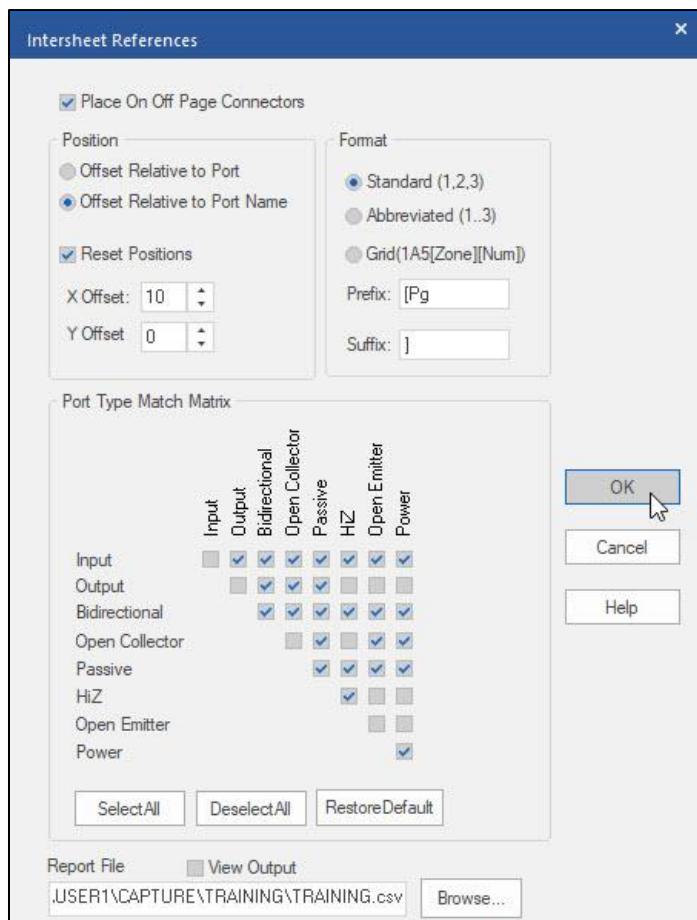
**Objective:** To generate hierarchical cross references for nets.

### Adding Intersheet References

1. Select the design name in the Project Manager window and choose **Tools – InterSheet References**.

The Intersheet References window appears.

2. Set the options as shown.



The matrix section of the setup window specifies which port-to-port combinations will be evaluated when generating intersheet references.

3. Click **OK** and **No** when prompted to view the warnings in the Session log.

Building a Hierarchical Design

## Saving the Design

1. In the Project Manager, select **training.dsn** and choose **File – Save**.

## Viewing the Intersheet Reference Report

1. In the Project Manager, click on **training.csv** in the Outputs folder.  
These are the intersheet references that were added to the schematic pages.  
The caret (^) symbol means that the signal can be found one level higher in the hierarchy.
2. Notice some entries in the report contain **Property Not Present** warnings.

```
"AEN","Input","PAGE1","1","Training Root Schematic","J1.47,U5.8","690","220","2C","[Pg1]"  
"AEN","Input","PAGE1","1","Training Root Schematic","J1.47,U5.8","170","490","5B","[Pg1]"  
"AEN","Input","PAGE2","2","Training Root Schematic","U6.16","180","450","5B","Property Not Present"  
"OUTB","Output","PAGE1","5","DATA Schematic","DAAMP2.OUT","580","330","2C","[Pg2^]"  
"OUT","Output","PAGE1","4","DAAMP CIRCUIT","U13.6","870","320","1C","[Pg2,5]"  
"OUTA","Output","PAGE1","5","DATA Schematic","DAAMP1.OUT","580","120","2D","[Pg2^]"  
"OUT","Output","PAGE1","3","DAAMP CIRCUIT","U10.6","870","320","1C","[Pg2,5]"  
"DQ0","Input","Page1","3","DAAMP CIRCUIT","U9.12","110","320","5C","[Pg5^]"  
"DQ1","Input","Page1","3","DAAMP CIRCUIT","U9.13","110","330","5C","[Pg5^]"  
"DQ2","Input","Page1","3","DAAMP CIRCUIT","U9.14","110","340","5C","[Pg5^]"  
"DQ3","Input","Page1","3","DAAMP CIRCUIT","U9.15","110","350","5B","[Pg5^]"  
"DQ4","Input","Page1","3","DAAMP CIRCUIT","U9.16","110","360","5B","[Pg5^]"  
"DQS","Input","Page1","3","DAAMP CIRCUIT","U9.17","110","370","5B","[Pg5^]"  
"DQ6","Input","Page1","3","DAAMP CIRCUIT","U9.18","110","380","5B","[Pg5^]"  
"DQT","Input","Page1","3","DAAMP CIRCUIT","U9.19","110","390","5B","[Pg5^]"  
"DQ0","Input","Page1","4","DAAMP CIRCUIT","U12.12","110","320","5C","[Pg5^]"  
"DQ1","Input","Page1","4","DAAMP CIRCUIT","U12.13","110","330","5C","[Pg5^]"  
"DQ2","Input","Page1","4","DAAMP CIRCUIT","U12.14","110","340","5C","[Pg5^]"  
"DQ3","Input","Page1","4","DAAMP CIRCUIT","U12.15","110","350","5B","[Pg5^]"  
"DQ4","Input","Page1","4","DAAMP CIRCUIT","U12.16","110","360","5B","[Pg5^]"  
"DQS","Input","Page1","4","DAAMP CIRCUIT","U12.17","110","370","5B","[Pg5^]"  
"DQ6","Input","Page1","4","DAAMP CIRCUIT","U12.18","110","380","5B","[Pg5^]"  
"DQT","Input","Page1","4","DAAMP CIRCUIT","U12.19","110","390","5B","[Pg5^]"  
"VD [0-7]","Input","PAGE2","2","Training Root Schematic","Data.VD[0-7]","550","220","3C","Property Not Present"  
"VD [0-7]","Input","PAGE1","5","DATA Schematic","","60","30","5D","[Pg2^]"  
"RD [0-7]","Input","PAGE1","6","HSRAM","","50","10","5D","[Pg2^]"  
"RA [0-15]","Input","PAGE1","6","HSRAM","","50","30","5D","[Pg2^]"
```

3. Make a note of the net names associated with these warnings.  
These messages show 2 buses that were not given intersheet references.
4. Close the report.

## Viewing the Intersheet References in the Hierarchical Design

1. Open PAGE1 of the DAAMP CIRCUIT. Choose either the DAAMP1 or DAAMP2 occurrence and click **OK**.
2. Notice that the VCLK net points up to page 2 and page 5 of the hierarchical design.



- Click on the port symbol for the VCLK net, right-click and select **Signals** from the pop-up menu.

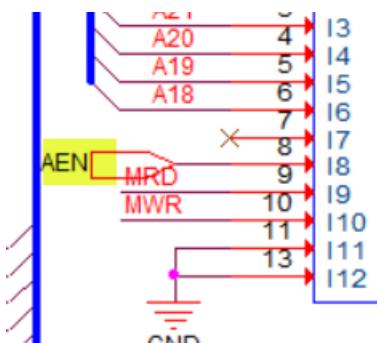
The navigation window displays the other locations on this net.

Navigation Window						
Signals		Name	Page	Page Number	Schematic	Part Pin
Object ID	VCLKA(Wire Alias)	VCLKA	PAGE2	2	Training Root Schematic	U5.34,Data.VCLKA
	Data/VCLKA(Port)	VCLKA	PAGE1	5	DATA Schematic	U14.11,DAAMP1.VCLK
	Data/DAAMP1/VCLK(Port)	VCLKA	Page1	3	DAAMP CIRCUIT	U8.11
Ready						

- Double-click to trace this signal through the design and view the intersheet references for this net.
- Notice how the signal name changes to VCLKA in the DATA and Root schematics.
- Close the Navigation window.
- Close all schematic pages.

## Fixing the Intersheet Reference Warnings

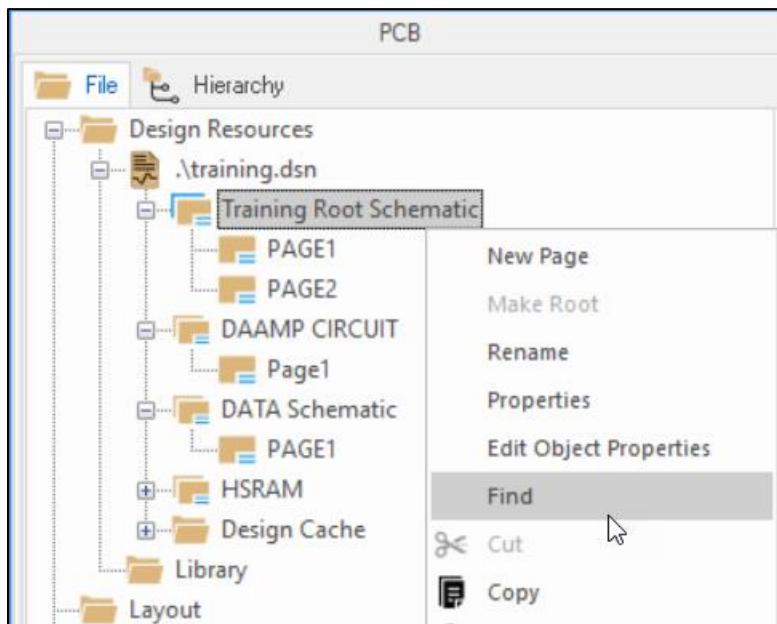
- Open PAGE1 of the Training Root Schematic and notice that the ports mentioned in the report were not cross referenced, as shown below.



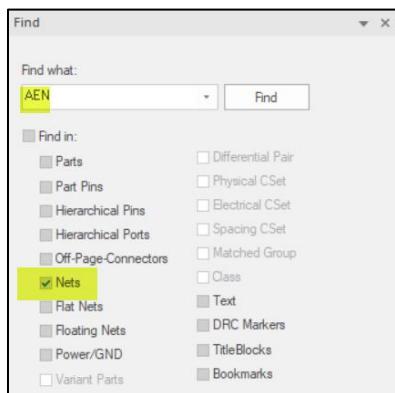
This port was not cross referenced because the system could not find corresponding block pins. The warning you saw in the cross reference report is due to the incorrect use of these port symbols at the top level of the hierarchy.

## Building a Hierarchical Design

2. In the Project Manager, right-click on the Root Schematic and select **Find**.



3. Set the Find window, as shown below, and click **Find**.



4. The Find Results window shows that these nets go to pages of the Training Root Schematic.

Find Results						
Nets						
Object ID	Net Name	Page	Page Number	Schematic	Pin	
AEN(Wire Alias)	AEN	PAGE1	1	Training Root Schematic\	J1.47,U5.8	
AEN(Port)	AEN	PAGE2	2	Training Root Schematic\	U6.16	
AEN(Port)	AEN	PAGE1	1	Training Root Schematic\	J1.47,U5.8	
AEN(Port)	AEN	PAGE1	1	Training Root Schematic\	J1.47,U5.8	

These nets do not go anywhere else in the hierarchy. They should be using Off-Page Connector symbols instead of ports.

5. Close the Find Results window and the **Find** tab.
6. Delete the **AEN** port symbol on PAGE1 and PAGE2 of the Training Root Schematic and replace them with off-page connectors, as shown below.

### Saving the Design

1. In the Project Manager, select the design name and choose **File – Save**.
2. Close all the schematic pages.

### Updating Intersheet References

1. Select the design name in the Project Manager and choose **Tools – Intersheet References**.
2. Click **OK** and **No** to continue.

### Saving Your Work

1. Save the design.

### Viewing Results

1. Double-click on the **training.csv** file in the *Outputs* folder of the Project Manager and notice there is still one Property Not Present warning for the VD[0-7] nets in the Training Root Schematic.  
It isn't necessary to fix this warning right now, but can you think of how you might fix it?  
*Hint:* This is not a multi-sheet net (no Off\_Page Connector required), and port symbols should not be used at the top level of the hierarchy.

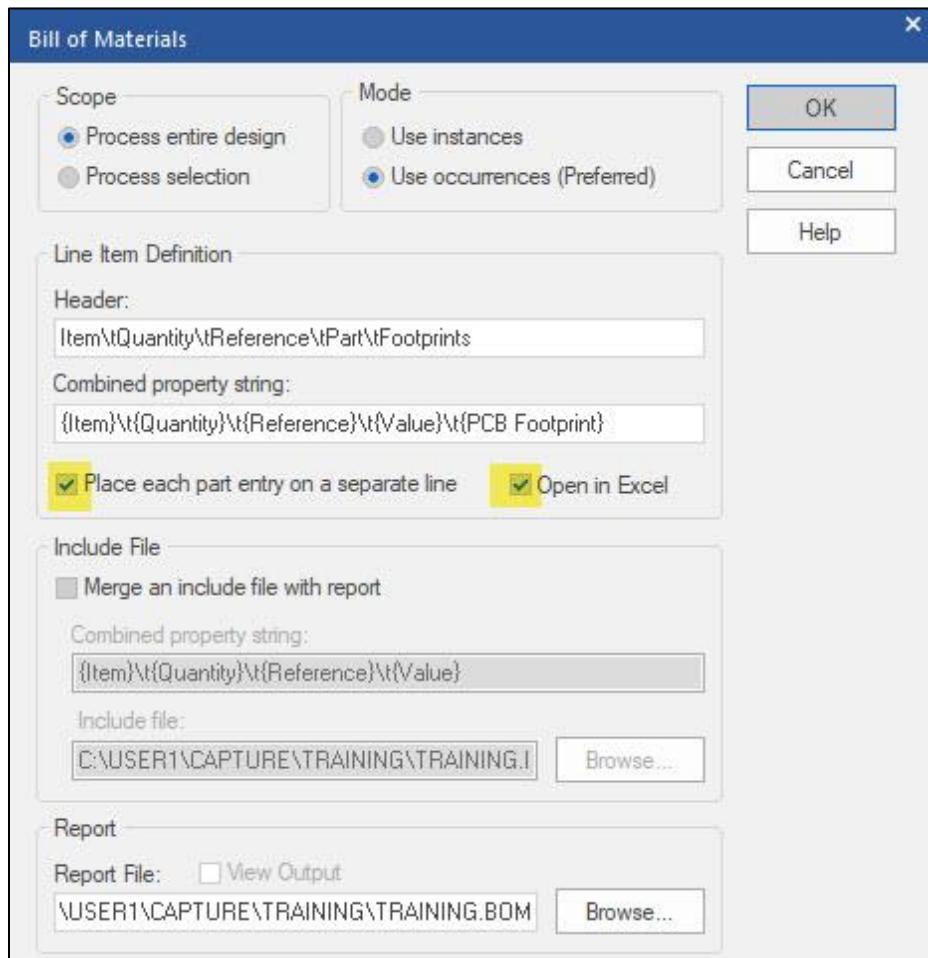
2. Close the log file.
3. Close all schematic pages.



## Lab 8-9 Creating a Bill of Materials Report

**Objective:** To create a custom Bill of Materials.

1. Select the design name in the Project Manager window and choose **Tools – Bill of Materials**.
2. Select the **Place each part entry on a separate line** checkbox.



3. Turn on the **Open in Excel** option and click **OK** to display the Bill of Materials report in Excel.
4. Notice that the report contains five columns (Item, Quantity, Reference, Part, and Footprint).  
This custom format is based on information stored in the *training.opj* file.
5. Close the report.



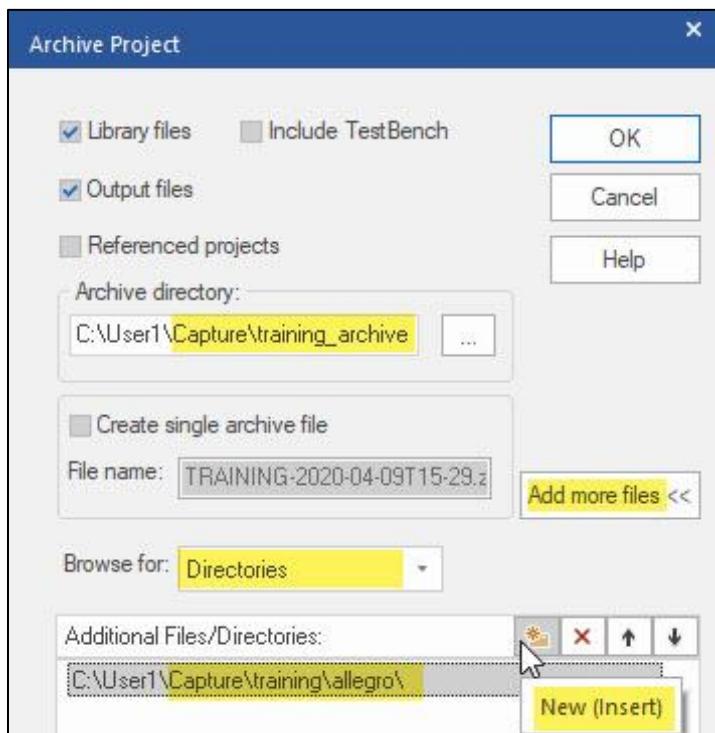
## Lab 8-10 Archiving a Project

**Objective:** To store the final schematic, board layout, and associated library parts for future use.

1. In the Project Manager, select the **training.dsn** file and choose **File – Archive Project**.

### Setting the Archive Directory

1. You will output the archived project into the *Capture* directory. Use the **Browse** button to set the Output Directory field to the *C:\User1\Capture\training\_archive*.



### Including the Layout Files in the Archive

1. Click the **Add more files** button and toggle the **Browse for** field to **Directories**.
2. Use the New icon to insert a new line, then browse to select the *C:\User1\Capture\training\allegro* folder, as shown above.

## Running the Archiver

1. Click **OK** to begin the archive process.
2. Use a Windows Explorer or terminal window to view the contents of the *training\_archive* directory. It should be located directly beneath the *Capture* folder.
3. Notice how it includes an *Additional Files* folder where the Allegro files are stored.

## Opening and Closing the Archived Project

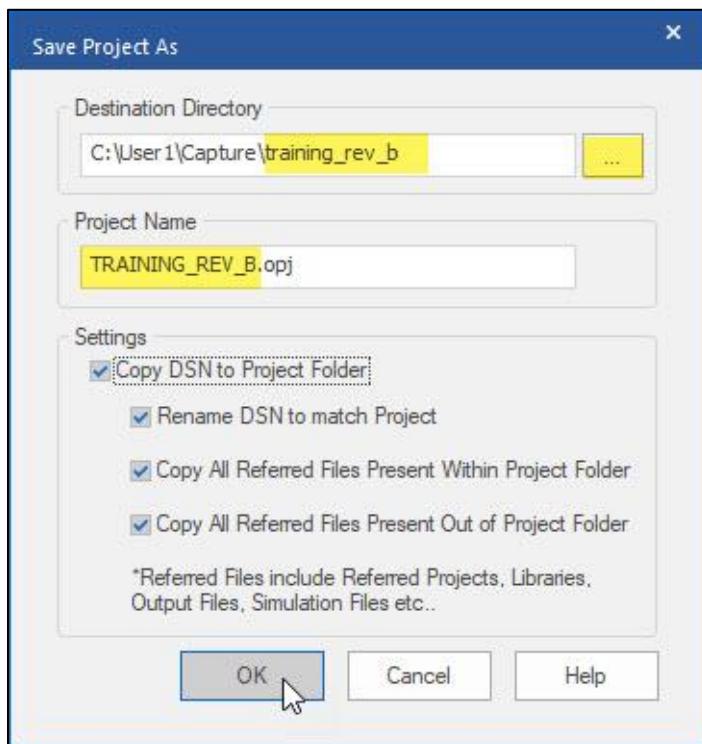
1. In the Project Manager, choose **File – Close**.  
The Capture session window is still running.
2. Choose **File – Open – Project**.
3. Navigate to the *C:\User1\Capture\training\_archive* directory.
4. Select the *training.opj* file and click **Open**.  
The archived project is loaded.
5. Open the archived schematic.
6. Click on the Project Manager window and choose **File – Close** to close the project.



## Lab 8-11 Creating a New Project from an Existing One

**Objective:** To copy and rename the training project.

1. Choose **File – Open – Project** and select *C:\User1\Capture\training\training.opj* file.
2. In the Project Manager, select the design file and choose **File – Save Project As**.
3. In the Save Project As window, set the options as shown below.

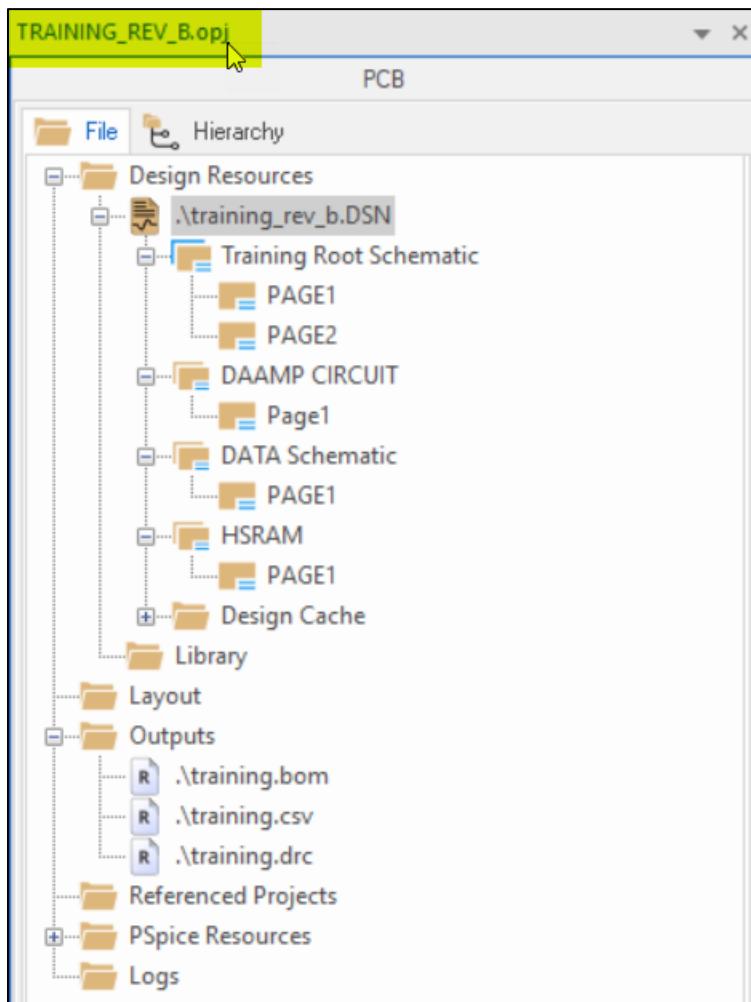


Remember always to replace paths shown in lab instructions with actual paths to the *Capture* folder on your system.

4. Click **OK**.

## Building a Hierarchical Design

The project is copied, renamed, and loaded into the Project Manager.



Your original project has been closed. You are now working on the copied project.

5. Notice the Outputs folders contain files from the original project.
6. Use Windows Explorer to view the contents of the *training\_rev\_b* project folder in the file system.

This is the project that is loaded in the Project Manager. The original source project is in the *training* folder.

## Closing the Copied Project

1. Choose **File – Close** to close the project.

### Exiting the Software

1. Choose **File – Exit** to close the Capture session window.



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## **Appendix A: Optional Topics**

(c) Cadence Design Systems Inc. Do not distribute.

## Lab A-1 Customizing Toolbars

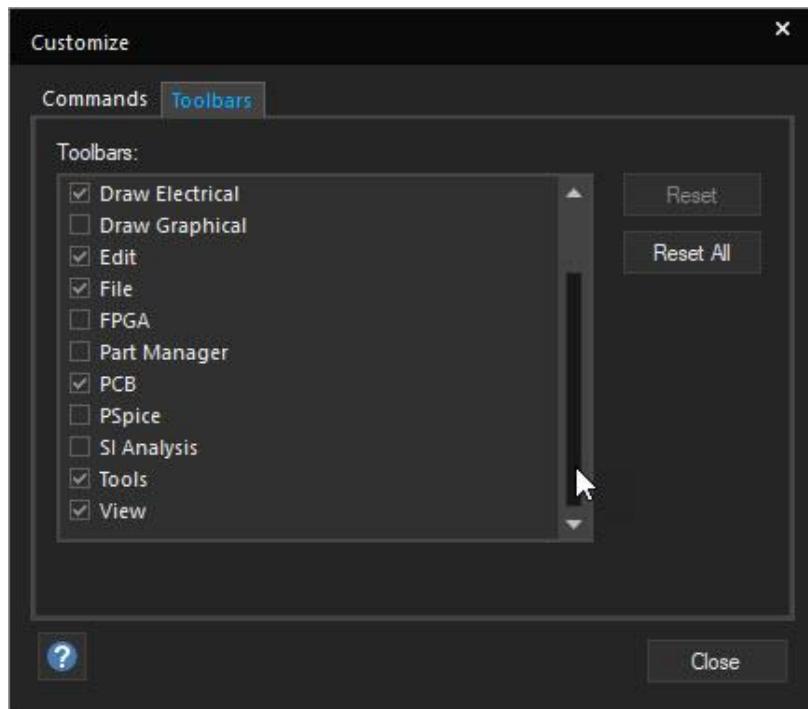
**Objective:** To add or remove icons from toolbars and create your own toolbar.

---

### Opening and Closing the Toolbars

1. With the Capture session window open, choose **Tools – Customize**.

The Customize window opens, as shown below.



2. In the **Toolbars** tab, select or unselect the checkbox for an icon toolbar.

Notice the toolbar is added or removed in the session window.

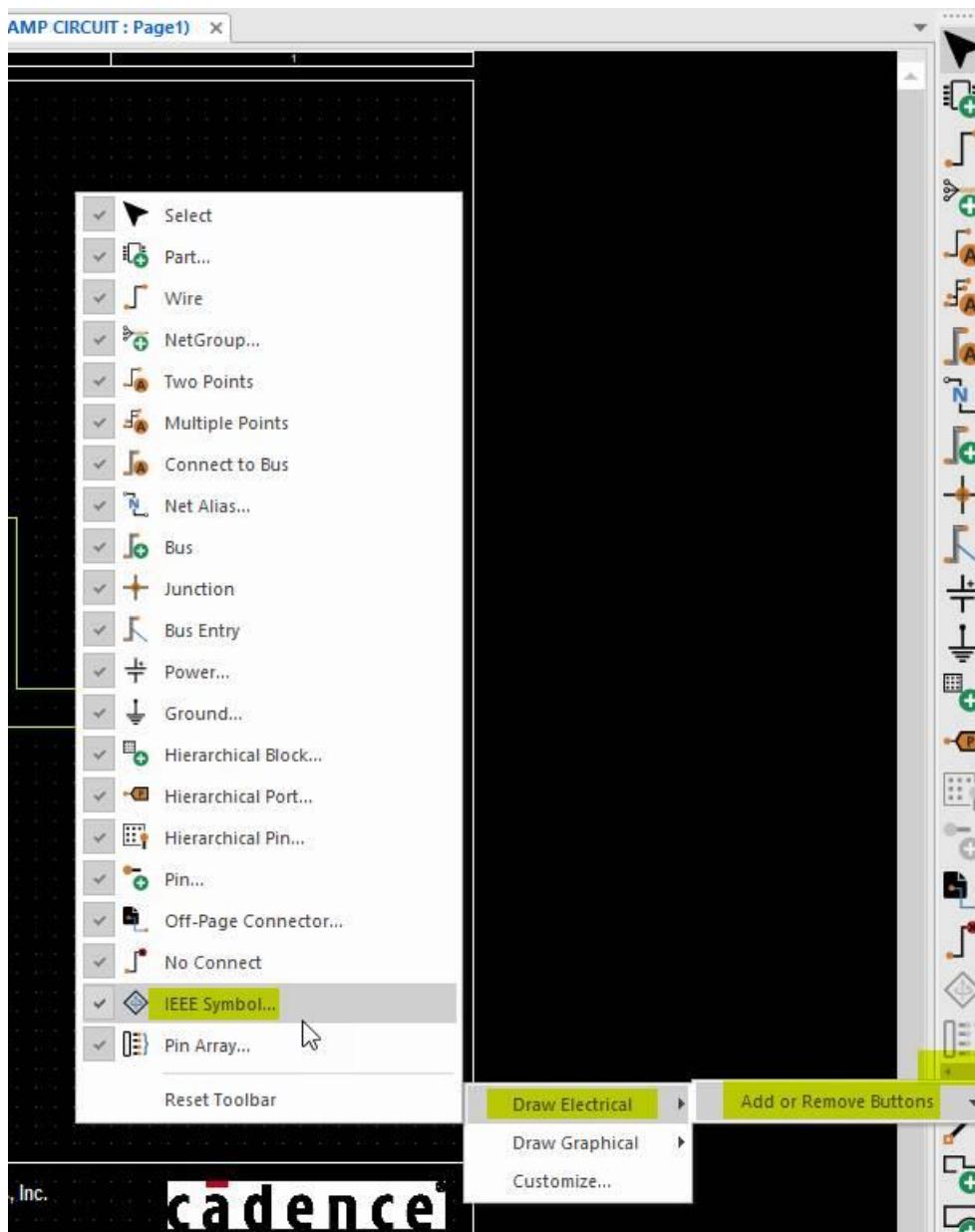
3. Click **Close**.

### Adding or Removing Icons from Toolbars

Let's remove and add an icon to the Draw toolbar.

## Optional Topics

1. Click at the bottom of the Draw Electrical icon toolbar and choose **Add or Remove Buttons – Draw Electrical – IEEE Symbol.**



2. Notice the checkbox for the icon is toggled off, and the IEEE icon is removed from the toolbar.
3. Click to toggle the checkbox back on.

The IEEE icon is added to the toolbar again.



## Lab A-2 Testing the LM324 Part

**Objective:** To annotate a heterogeneous part.

---

### Creating a Test Design

1. Choose **File – New – Project**.
2. In the Name field, enter **test\_lm324**.
3. Click the **Browse** button, navigate to the **C:\User1\Capture** folder, and click the **Select Folder** button.
4. In the Location field, add **test\_lm324** to the path, as shown below.



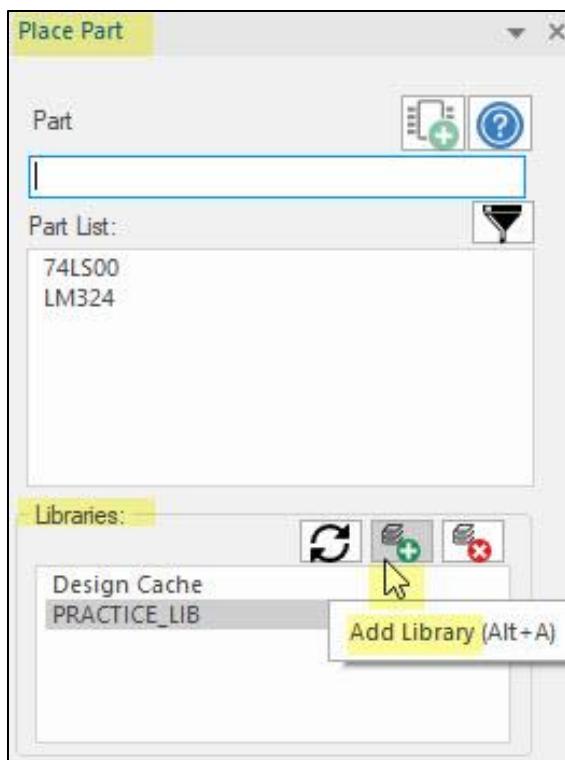
**Note:** Always replace **C:\User1** with the actual path to the *Capture* folder on your system.

5. Click **OK** in the New Project window.

The new project is created, and page one of the *test\_lm324* design is displayed.

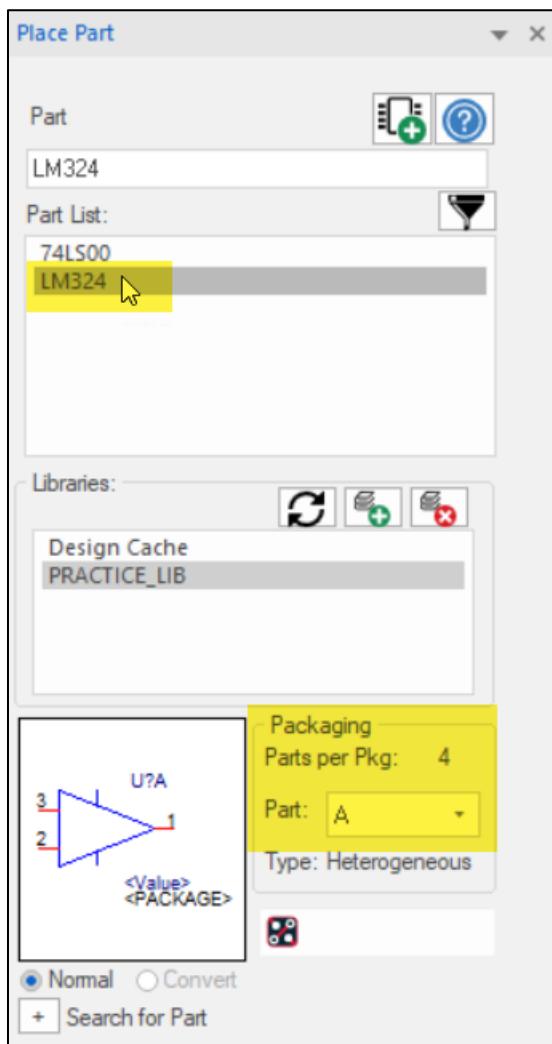
## Adding the *PRACTICE\_LIB* to Your Project Setup

1. Choose **Place – Part**.
2. When the **Place Part** tab opens, use the Add Libraries icon to add *C:\User1\Capture\training\_libs\PRACTICE\_LIB.OLB* to the Libraries list of the Place Part form.



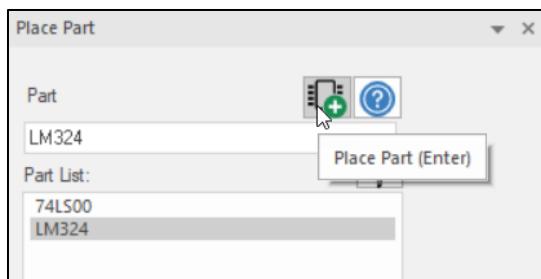
## Placing the LM324

1. Double-click the **LM324** part from the *PRACTICE\_LIB* library, as shown below.



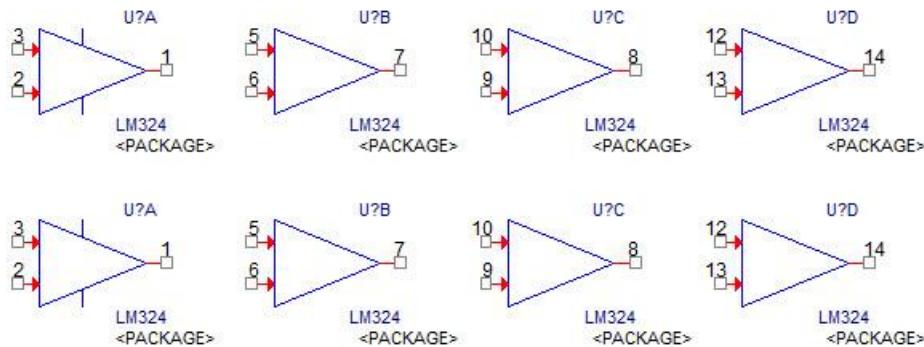
Notice that the Packaging section of the Place Part form shows four parts per package. The Part field defaults to A or Section 1 of the package.

2. Place the part on the schematic page using the **Place Part** icon.



## Optional Topics

3. Add sections **B**, **C**, and **D** of the LM324 package to the schematic by toggling the Part field in the Place Part form.
4. Copy and paste the first set so you have eight gates on the page (see the example below).

**Editing the PACKAGE Property**

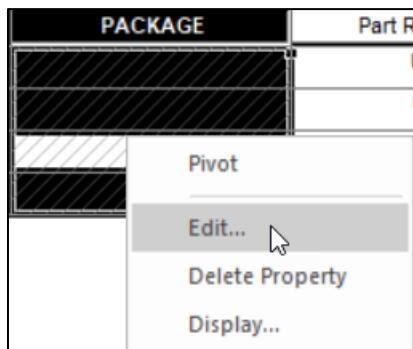
In the above example, instantiating any gate of a heterogeneous part more than once (for example, two U?A or U?B gates) will cause annotation errors unless we add a property that shows how to group the gates into packages.

1. Choose four gates (U?A, B, C, and D).
2. **Right-click** and select **Edit Properties**.
3. Pivot the property table so the selected parts are on the left and properties are across the top. Then, scroll the table horizontally to locate the PACKAGE property column.

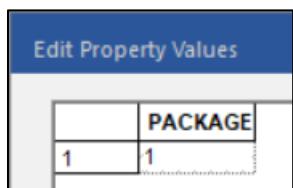
The screenshot shows the Cadence Property Editor window with a table containing four rows of properties for U?A, U?B, U?C, and U?D. The columns are labeled "Name" and "PACKAGE". The "PACKAGE" column contains a hatched pattern.

	Name	PACKAGE
1	SCHEMATIC1 : PAGE1 : U?A	/INS63
2	SCHEMATIC1 : PAGE1 : U?B	/INS140
3	SCHEMATIC1 : PAGE1 : U?C	/INS197
4	SCHEMATIC1 : PAGE1 : U?D	/INS232

4. Click on the **PACKAGE** column header, then right-click and choose **Edit**.



5. In the Edit Property Values window, set the PACKAGE property value to **1** and click **OK**.



The property value is applied to all four parts.

		Name	PACKAGE
1	[+] SCHEMATIC1 : PAGE1 : U?A	INS63	1
2	[+] SCHEMATIC1 : PAGE1 : U?B	INS140	1
3	[+] SCHEMATIC1 : PAGE1 : U?C	INS197	1
4	[+] SCHEMATIC1 : PAGE1 : U?D	INS232	1

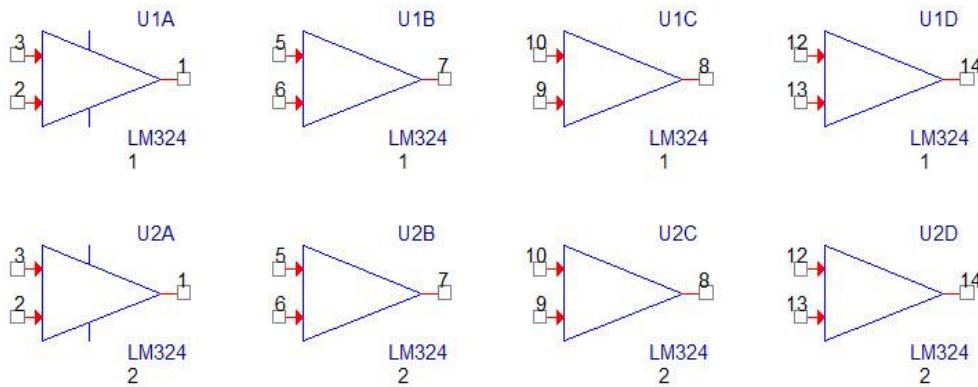
6. Click **Apply** and **Yes** to continue.
7. Close the Property Editor window.
8. In the schematic, notice the PACKAGE property value is displayed for the selected gates.
9. Select the second set of gates and assign a PACKAGE value of **2**.
10. Save the schematic page.

## Annotating the Test Design

1. In the Project Manager window, select the design name **test\_lm324.dsn**.
2. Choose **Tools – Annotate**.
3. In the **Physical Packaging** section of the Packaging tab, add the PACKAGE property to the end of the combined property string. Make sure to enclose the property name in curly braces {}, as shown below.



4. Click **OK**.
5. In the schematic, notice the LM324 parts with the same PACKAGE value were placed in the same package.



**Important:** If the PACKAGE property had not been added to the combined property string, it would have been ignored during annotation, resulting in packaging errors.

6. Choose **File – Close** to close the schematic.
7. Choose **File – Close** to close the *test\_lm324* project.



## Lab A-3 Creating a Custom Title Block

**Objective:** To create a company title block.

---

### Opening the Title Block Symbol

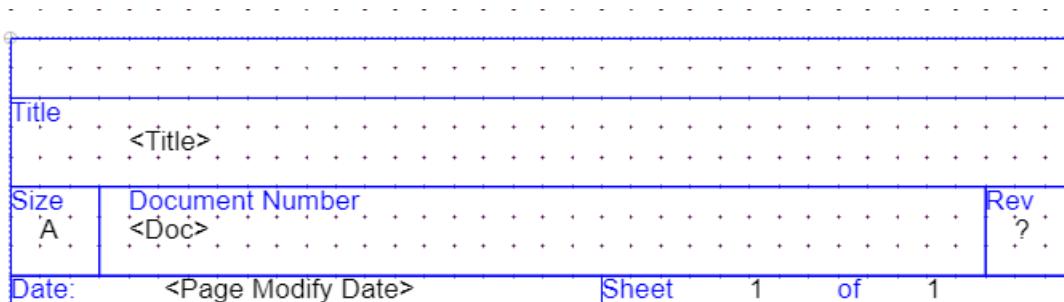
1. In the Capture session window, choose **File – Open – Library** and navigate to the *D:\User1\Capture\training\_libs* directory.
2. Select the **PRACTICE\_LIB.OLB** library and click **Open**.

This is the library you created earlier in class.

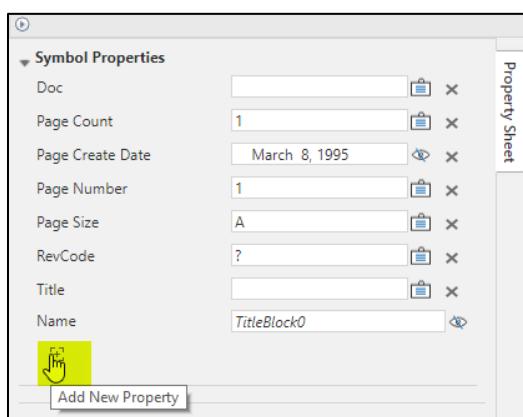
### Adding Reserved Title Block Properties

1. From the Project Manager, double-click **TitleBlock0**.

The title block symbol appears. Notice that the symbol already contains properties for title, revision, document number, modified date, page number, and page count.



2. In Symbol Properties Pane, click **Add New Property**.

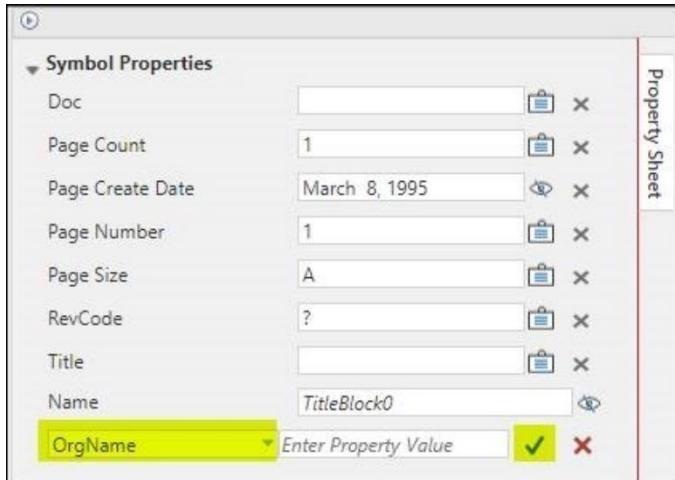


## Optional Topics

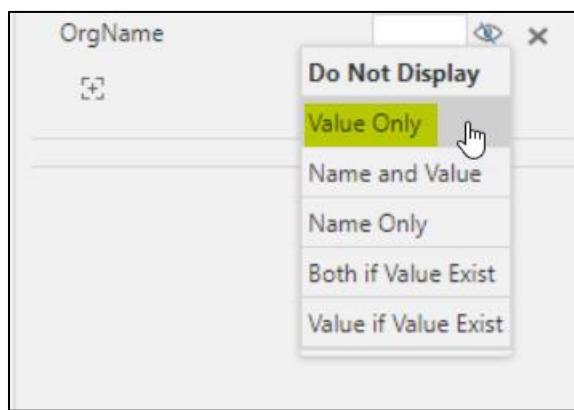
- Add the reserved property **OrgName**, as shown below.

You *must* enter the name of this case-sensitive property *exactly* as shown.

In order for this property to obtain a value from your design template, you *must* leave the Value field blank.



- Click **OK**.
- With the OrgName property selected, click the **Display Property** button and select **Value Only** and click **OK**.



- In the Symbol Properties window, click **Add New Property** again.
  - Add **OrgAddr1** through **OrgAddr3** properties or as many that match your design template.
- Note:** Normally, you add only as many OrgAddr properties as you need for your company address. Be sure to leave the Value field blank.
- For all OrgAddr properties, set the Display Property to **Value Only**.

9. In the Symbol Properties window, click **Add New Property** again.
  10. Add the **Cage Code** property. Leave the Value field blank.
  11. Under Display Property, select **Value Only**.

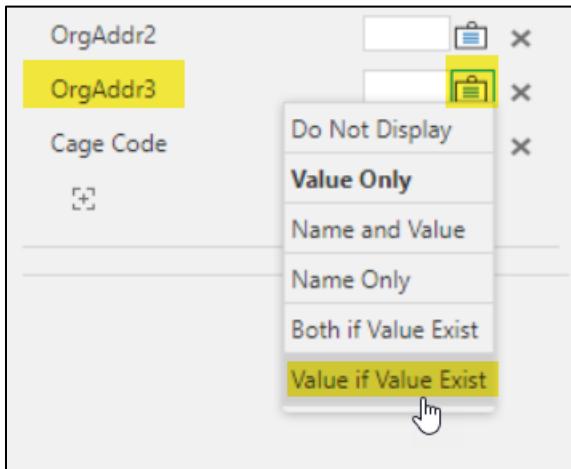
Title		<Title>		
Size A	Document Number <Doc>		Rev ?	
Date:	<Page Modify Date>		Sheet 1	of 1
<OrgName> <OrgAddr1> <OrgAddr2> <OrgAddr3> < Cage Code>				

12. Enlarge the upper rectangle of the title block to accommodate these properties. Click and drag the properties to their proper locations in the title block, as shown below.

<OrgName>		
<OrgAddr1> <OrgAddr2> <OrgAddr3>		
<b>Title</b> <Title>		
Size A	Document Number <Doc>	Rev ?< Cage Code >
Date:	<Page Modify Date>	Sheet 1 of 1

## Optional Topics

13. For the **OrgAddr3** property in the title block, change the Display Property to **Value if Value Exist**.



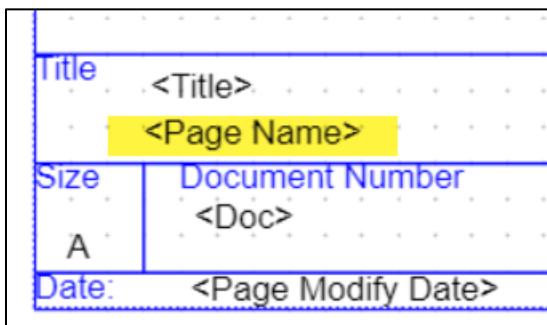
14. Choose **File – Save**.

**Note:** For hierarchical designs, it's recommended to add the Schematic Path property to title block symbols. This ensures that every page in the design displays a path showing its relative position in the hierarchy.

### Adding Page Name Property

- Under the Symbol Properties, click **Add New Property**
- Add the **Page Name** Property, change the Display Property to **Value Only**
- Place the Page Name property under the Title property, as shown below.

**Tip:** Temporarily disable Snap to Grid, move the properties into position, and then turn Snap to Grid back on. You can also change font sizes if you want to. 



4. Choose **File – Save**.

## Adding a Company Logo

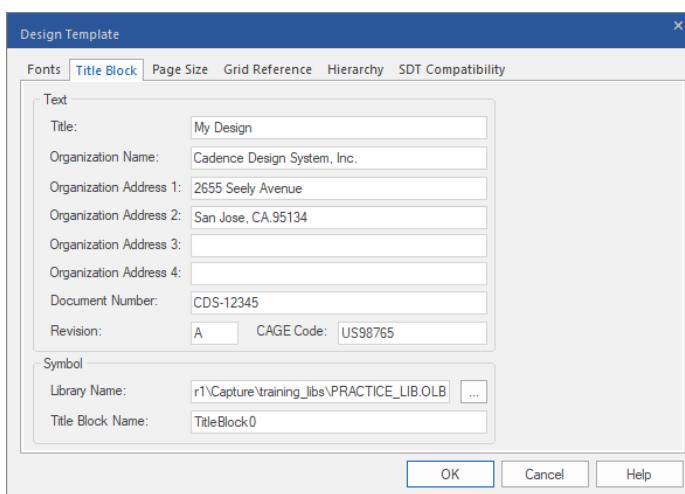
1. Choose **Place – Picture**.
2. In the Place Picture window, navigate to the *D:\User1\Capture\data\_files* directory.
3. Set the files in the type field to JPEG, select the *Cadence\_Logo\_Red\_Reg.jpg* file, and click **Open**.
4. Drag and place the logo inside the title block.



5. Choose **File – Save**. Choose **File – Close** to close the title block symbol.

## Specifying Default Title Block Content

1. Choose **Options – Design Template**.
2. In the Design Template window, click the **Title Block** tab.
3. Add the title block text data as shown below (or add your own company name and address).



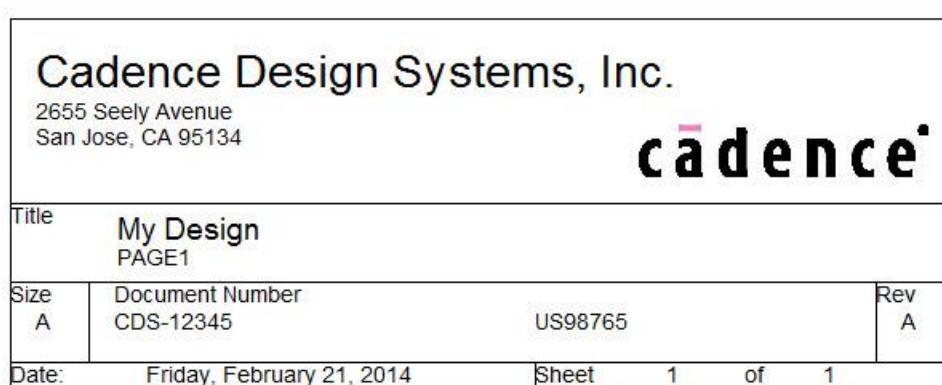
Optional Topics

4. Click the **Browser** button to the right of the Library Name field and navigate to the *D:\User1\Capture\training\_libs* directory.
5. Select the **PRACTICE\_LIB.OLB** library file and click **Open**.
6. In the Title Block Name field, enter **TitleBlock0**.
7. Click **OK**.

### Testing the Title Block

To test your title block symbol and the design template information you just specified, you must create a new design.

1. Choose **File – New – Design**.
2. When the new schematic page opens, click the **Zoom to all** icon to see if your title block appears on the new page.



If the title block does not appear on the new page, check the title block settings in the design template. Make sure that the library name, path and title block name are correct. Make the necessary changes and create another new design.

3. Close the schematic window without saving.
4. Close the *PRACTICE\_LIB* library. Do not save the test design.



## Lab A-4 Manually Creating a Hierarchical Block Symbol

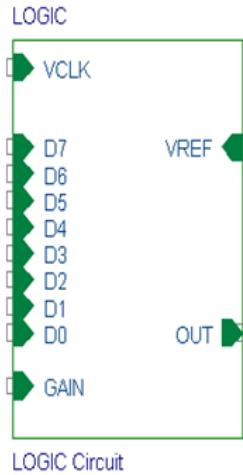
**Objective:** To illustrate the top-down approach to hierarchical design.

### Top-Down Method

If an existing schematic is already part of the design folder and has hierarchical ports for inputs and outputs, when you create a hierarchical block referencing that schematic, Capture automatically places the appropriate pins on the block symbol, as demonstrated earlier in this course.

If you want to create the hierarchical block first and create a schematic view later, you must build the block symbol manually (this is known as top-down).

In this optional lab exercise, you will manually build a hierarchical block in the Data schematic, as shown below.



### Drawing the Rectangle

1. In the Project Manager, double-click PAGE1 of the DATA schematic.
2. Zoom into the lower-right corner of the DATA schematic and click the Place Hierarchical Block icon. 
3. In the Reference field, enter **LOGIC**.
4. Toggle the Implementation Type to **Schematic View**.
5. In the Implementation name field, enter **LOGIC Circuit** and click **OK**.

Optional Topics

6. In the lower-right corner of the page, drag to create a rectangle to define a hierarchical block symbol.

7. Press **Esc**.

Because there is no *LOGIC CIRCUIT* schematic yet, the hierarchical block you draw does not have any hierarchical pins created automatically, as in the previous exercise.



### Adding Block Pins D0-D7

1. Select the **LOGIC Circuit** block symbol. Click the **Place H Pin** icon.



The Place Hierarchical Pin window appears.

2. In the Name field, enter **D0**.

3. Set the Type field to **Input** and click **OK**.

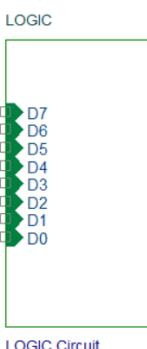
A hierarchical pin is attached to the edge of the rectangle. As you move your pointer, the block pin moves along the perimeter of the rectangle.

4. Click to place the pin along the left edge of the rectangle, near the lower-left corner.

5. Move your pointer up one grid and click to add another block pin.

Capture automatically increments the pin name to D1.

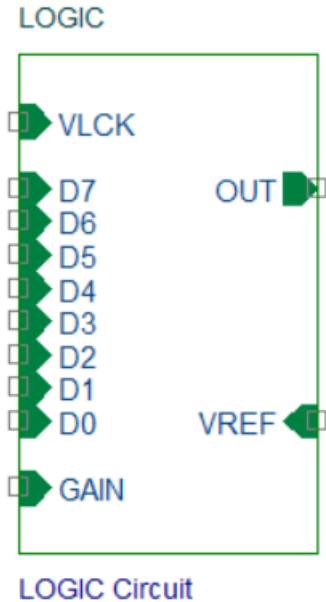
6. Continue adding block pins **D0** through **D7**.



7. Press **Esc** to exit the command. Press **Esc** again to deselect.

### Adding Block Pins VCLK, GAIN, VREF, and OUT

1. Select the block symbol. Click the **Place H Pin** icon and add a **VCLK** pin two grids above pin D7.
2. While in add pin mode, **right-click** and select **Edit Properties**.
3. In the Place Hierarchical Pin window, change the Name field to **GAIN** and click **OK**.
4. Add a **GAIN** pin 2 grids below pin D0.
5. Add a **VREF** pin on the right edge of the rectangle.
6. After adding the VREF pin, **right-click** and select **Edit Properties**.
  - a. Change the Name field to **OUT**.
  - b. Set the Type field to **Output** and click **OK**.
7. Add the **OUT** pin below the **VREF** pin.



8. Press **Esc** twice.
9. Save the design.

## Creating the LOGIC Circuit Schematic

1. Select the **LOGIC Circuit** block symbol, right-click and select **Descend Hierarchy**.

Capture prompts you for the name of the new LOGIC CIRCUIT schematic page.

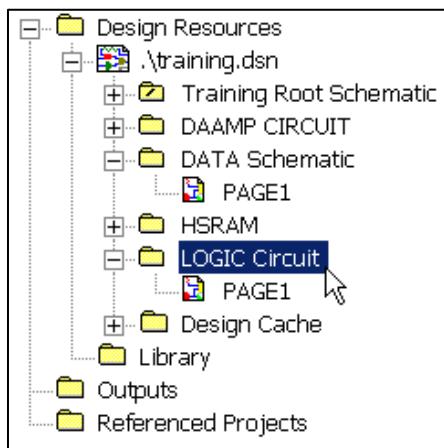
2. Click **OK**.

The LOGIC CIRCUIT schematic window opens. Notice how Capture automatically adds hierarchical port symbols to the new schematic page. These ports correspond to the pins you added to the block symbol.

3. Save the design.

4. Close both the *LOGIC CIRCUIT* and *DATA* schematic pages.

5. In the Project Manager window, notice that a new schematic folder was added for *LOGIC CIRCUIT*.



**Note:** The *LOGIC CIRCUIT* block symbol and its associated schematic are unconnected. The DRC program would flag these errors.

### **Deleting the LOGIC Circuit**

1. Because you do not use this block symbol in the next labs, open the DATA schematic and remove the LOGIC block symbol from your schematic page. Save and close the DATA schematic.
2. In the Project Manager, delete the LOGIC schematic folder.
3. Save the training design.



## Lab A-5 Using the Fisheye View

**Objective:** To view the design through a fisheye lens.

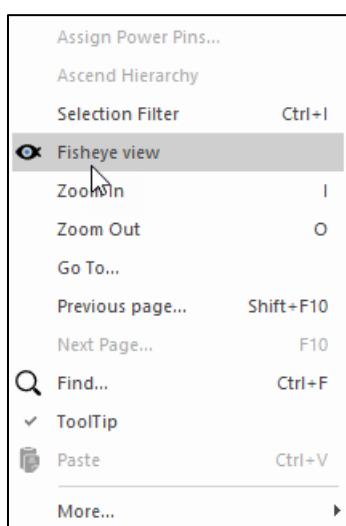
---

### Opening a Sample Project

1. Choose **File – Open – Project**.
2. Navigate to the *D:\User1\Capture\sample* directory.
3. Select **sample.opj** and click **Open**.
4. In the Project Manager window, **double-click .\sample.dsn**.
5. **Double-click Schematic**.
6. **Double-click PAGE1**. Page one of the Sample design opens.
7. Enlarge the schematic window. Click the **Zoom to all** icon.

### Switching to Fisheye Mode

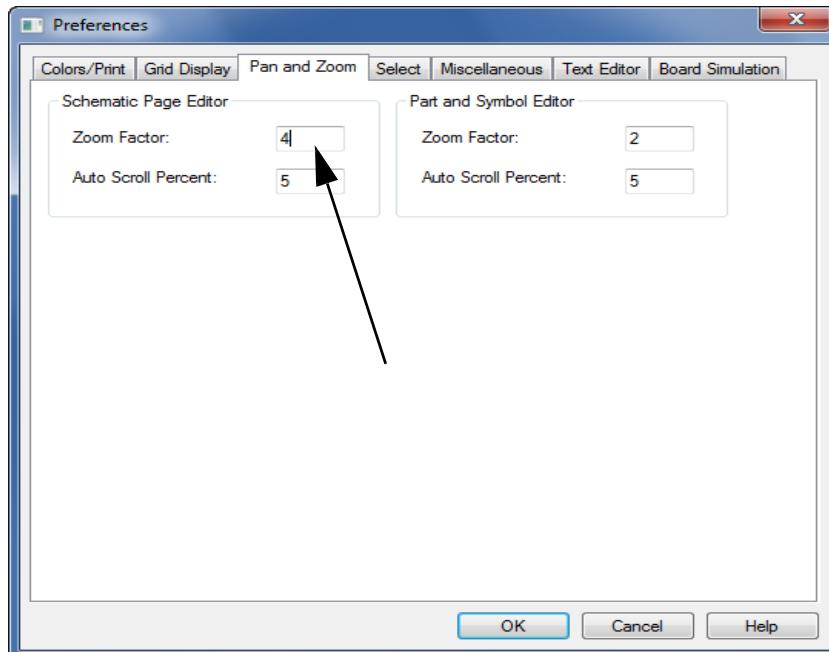
1. To switch to the fisheye mode, **right-click** the page.
2. Choose **Fisheye view**.



## Setting the Fisheye Focus

You can set the fisheye focus to selected objects on your schematic, causing only these objects to zoom while the rest of the viewable area remains in view but is zoomed out.

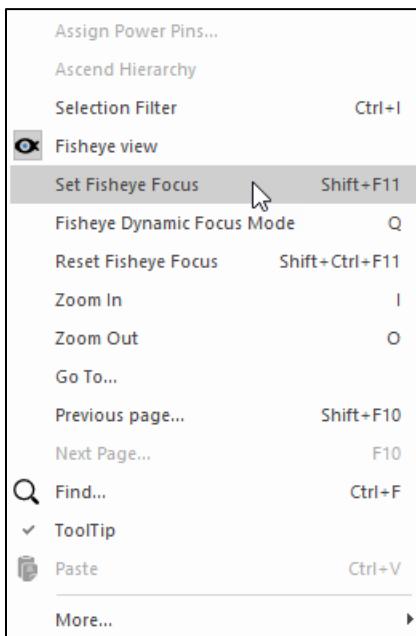
1. The focus is set in the **Options – Preferences – Pan and Zoom** settings. In the Schematic Page Editor section, set **Zoom Factor** to 4 (for this example).
2. Click **OK**.



3. To set the fisheye focus, select one or more objects on the page. (Hold **Ctrl** and then click to select multiple objects.)
4. **Right-click** the page.

## Optional Topics

5. Choose **Set Fisheye Focus** (shortcut: **Shift+F11**).



The view now zooms into that part (or parts) while the rest of the viewing area remains in a standard view.

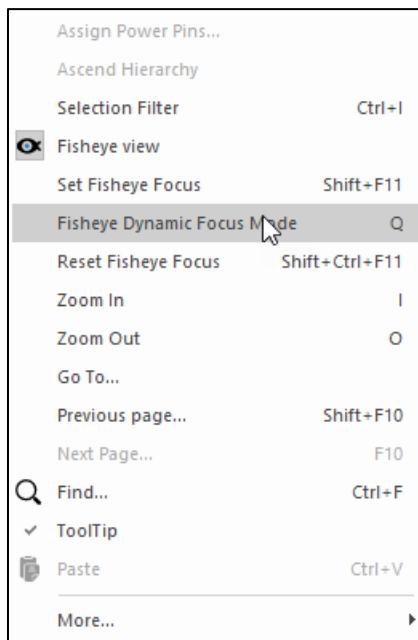
**Note:** To remove fisheye focus, **right-click** the page and select **Reset Fisheye Focus** (shortcut: **Ctrl + Shift + F11**).

### Setting the Fisheye Dynamic Focus Mode

In dynamic fisheye focus, the focus of the page shifts as you move the mouse pointer across the page. As the mouse hovers over a part of the page, only that part of the page comes into focus. The focus area is magnified, while the rest of the viewable area loses relative magnification.

1. To set the fisheye dynamic focus mode, **right-click** the page.

2. Choose **Fisheye Dynamic Focus Mode** (shortcut: **Q**).



3. Move your mouse around the page to pan from area to area.

## Fisheye Zoom Levels

While in the dynamic fisheye mode, you can use the following hotkeys to adjust the fisheye zoom level from a minimum of 2 to a maximum of 10.

1. Press **Ctrl + +** (Ctrl and plus key combination) to increase the zoom level.
2. Press **Ctrl + -** (Ctrl and minus key combination) to decrease the zoom level.

## Returning to Normal View Mode

1. To turn off the fisheye mode, click the **Fisheye** icon at the top of the main toolbar or from the pop-up menu; while on the schematic page, select **Fisheye view**.

## Closing the Project

1. To close the schematic page, choose **File – Close**.

Optional Topics

2. To close the project, choose **File – Close Project**.

The Project Manager window closes, but the main session window remains open.



## **Appendix B: Keyboard Shortcuts (Hot Keys)**

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The Capture program provides two types of keyboard shortcuts for common tasks:

**Shortcut keys** provide a quick way to perform other types of actions, such as scrolling across an editor's window. Shortcut keys include <Ctrl+key>, such as <Ctrl+Delete> to delete; shift keys, such as <Shift+A> to ascend the hierarchy; and function keys, such as <F4> to repeat a command.

**Menu access keys** are a quick way to issue menu commands. For example, pressing <Alt>, then <E>, then <R> executes the Rotate command found on the Edit menu. When you select a tool in the part editor or schematic page editor, the tool palette becomes active. As a result, many keyboard shortcuts are not available until you make the editor window active again. The easiest way to do this is to click on the title bar of the editor window as soon as you have the tool selected.

You don't have to press the **Shift** key to use most of the Shift key shortcuts. For example, pressing either **p** or **Shift+P** has the same result. These shortcuts are marked with **Shift** in Help and on Capture menus for visibility. The description of each menu command includes keyboard, mouse, and other shortcuts.

Many shortcuts are available while you use another command. For example, you can use <I> and <O> to zoom in and out while you move and place objects.

The tables in this Appendix group keyboard shortcuts by the Capture structures in which they are available. The conventions for representing key combinations are as follows:

- ◆ <Key1+Key2> means you press these keys simultaneously.
- ◆ <Key1>, <Key2> means you press these keys sequentially.

## Keyboard Shortcuts (Hot Keys)

Environment	Action	Keyboard Shortcut
All OrCAD Capture Windows	Exit	<ALT+F4>
	Exit	<ALT>, <F>, <X>
	Exit	<ALT+Spacebar>, <C>
Schematic Page Editor	Select All	<Ctrl+A>
	Ascend hierarchy	<Shift+A>
	Descend hierarchy	<Shift+D>
	Place bus	<B>
	Place bus entry	<E>
	Place ground	<G>
	Place junction	<J>
	Place net alias	<N>
	Place no-connect	<X>
	Place part	<P>
	Place power	<F>
	Place text	<T>
	Place wire	<W>
	Place polyline	<Y>
	Record macro	<F7>
	Play macro	<F8>
	Configure macro	<F9>
Part Editor	Previous part	<Ctrl+B>
	Next part	<Ctrl+N>
Property Editor	Add a new column or row	<Ctrl+N>
	Apply a change	<Ctrl+P>
	Edit the Display Properties for a selected cell	<Ctrl+D>
	Delete a property	<Ctrl+L>
	Give focus to the Filter by drop-down list	<Ctrl+B>

<b>Environment</b>	<b>Action</b>	<b>Keyboard Shortcut</b>
Schematic Page and Part Editors	Edit a cell	<Ctrl+E>
	Find a value in a column	<Ctrl+F>
	Delete the contents of a cell	<Delete>
	Copy	<Ctrl+C>
	Edit properties	<Ctrl+E>
	Find	<Ctrl+F>
	Go to	<Ctrl+G>
	Print	<Ctrl+P>
	Rotate	<R>
	Save	<Ctrl+S>
	Cursor snap to grid (identical to the Preferences dialog box Grid display tab option).	<Ctrl+T>
	Ungroup	<Ctrl+U>
	Paste	<Ctrl+V>
	Cut	<Ctrl+X>
	Redo	<Ctrl+Y>
Schematic Page and Part Editors	Undo	<Ctrl+Z>
	Repeat	<F4>
	Delete (Design and Edit menus)	<Del>
	Delete (Design and Edit menus)	<Delete>
	Delete (Design and Edit menus)	<Backspace>
	Double-click left mouse button	<Enter>
	Deselect all and switch to selection tool (arrow pointer)	<Escape> or <Esc>
	Click left mouse button	<Space>
	Move 1 grid up (grid on) or 0.1 grid up (grid off)	<Up Arrow>
	Move 1 grid down (grid on) or 0.1 grid down (grid off)	<Down Arrow>

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## Keyboard Shortcuts (Hot Keys)

Environment	Action	Keyboard Shortcut
	Move 1 grid left (grid on) or 0.1 grid left (grid off)	<Left Arrow>
	Move 1 grid right (grid on) or 0.1 grid right (grid off)	<Right Arrow>
	Snap pointer to nearest grid and then move 5 grids up	<Ctrl+Up Arrow>
	Snap pointer to nearest grid and then move 5 grids down	<Ctrl+Down Arrow>
	Snap pointer to nearest grid and then move 5 grids left	<Ctrl+Left Arrow>
	Snap pointer to nearest grid and then move 5 grids right	<Ctrl+Right Arrow>
	Pan up	<Page Up>
	Pan down	<Page Down>
	Pan left	<Ctrl+Page Up>
	Pan right	<Ctrl+Page Down>
	Redraw	<F5>
	Center the view at the pointer's current position	<C>
	Mirror horizontally	<H>
	Zoom in	<I>
	Zoom out	<O>
	Rotate	<R>
	Mirror vertically	<V>
	Begin a wire, bus, or polyline (corresponding tool active)	<Shift+B>
	End a wire, bus, or polyline (corresponding tool active)	<Shift+E>
Session Log	Clears the session log	<Ctrl+Del>
	Clears the session log	<Ctrl+Delete>
Text boxes	Delete the selected text	<Backspace>
	Delete the selected text	<Del>
	Delete the selected text	<Delete>
	Copy selected text to the Clipboard	<Ctrl+C>

Environment	Action	Keyboard Shortcut
	Paste the Clipboard contents	<Ctrl+V>
	Cut the selected text to the Clipboard	<Ctrl+X>
	Undo the last edit	<Ctrl+Z>
	Select word and any following space	<Double Click>
	Extend selection from the insertion point to cursor	<Shift+Click>
	Jump right one word	<Ctrl+Right Arrow>
	Jump left one word	<Ctrl+Left Arrow>
	Jump to the beginning of the line	<Home>
	Jump to the end of the line	<end>
	Jump to the beginning of the text box	<Ctrl+Home>
	Jump to the end of the text box	<Ctrl+End>
	Extend selection from insertion point to beginning of multiple-line text box	<Shift+Home>
	Extend selection from insertion point to end of multiple-line text box	<Shift+End>

