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OrCAD® X Capture

Course Version 24.1

Lecture Manual

Revision 1.0

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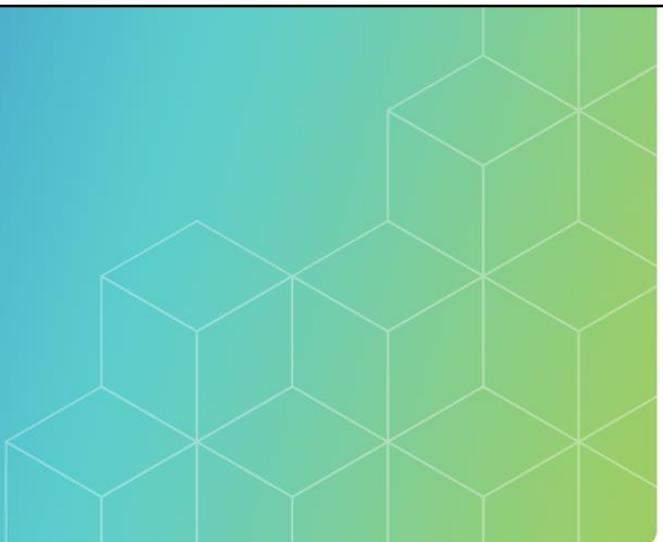
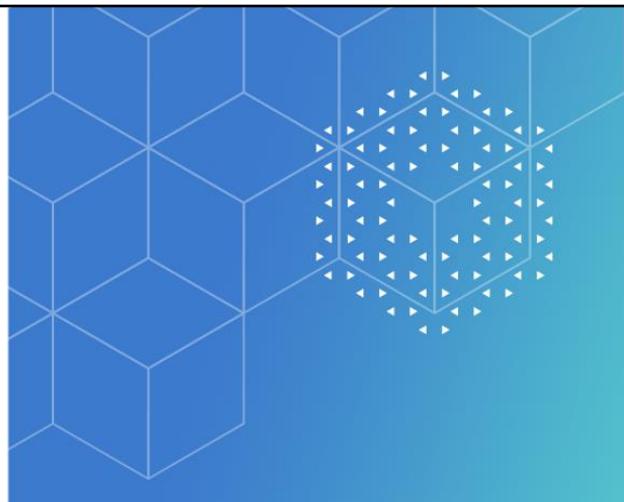
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The background of the slide features a 3D hexagonal grid pattern. Several translucent, colored cubes (red, orange, yellow, green, blue) are scattered throughout the space, some appearing to float or move. In the top left corner, there is a faint mathematical equation: $P_{(1)} \approx e^{-\eta} \left(\frac{g}{g_0} \right)$. In the bottom right corner, the Cadence logo is visible.

OrCAD® X Capture

Version	24.1
Revision	1.0
Estimated time:	2 Days

Welcome to the OrCAD X Capture course.



Module 1

About This Course

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Course Prerequisites

This course has no prerequisites.



This page does not contain notes.

Course Objectives

In this course, you

- Set up user interface preferences and design template data
- Build Capture library parts
- Create multi-sheet flat and hierarchical designs
- Check designs for errors
- Work with part properties
- Create netlist files for Allegro® X PCB Editor and OrCAD® X Presto layout tools

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This is an introductory level course for new Cadence® OrCAD® X Capture users. The course begins with some basic schematic library development. This course shows you how to create and process a simple schematic, then progresses into multi-sheet and hierarchical designs. Part properties are also covered.

Course Agenda

- Introduction to OrCAD X Capture
- Setting Up Your Environment
- Working with Libraries
- Building a Simple Schematic
- Building a Multi-Sheet Schematic
- Editing Part Properties
- Building a Hierarchical Design
- Course Conclusions



Here is a list of the modules in this course.

Software and Licenses

For the software and licenses used in the labs for this course, go to:

https://www.cadence.com/en_US/home/training/all-courses/85037.html

If there is additional information regarding the specific software, it is detailed in the lab document and/or the README file of the database provided with this course.



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Digital badges indicate mastery in a certain technology or skill and give managers and potential employers a way to validate your expertise.

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How do I register to take the exam?

- Log in to our [Learning Management System](#), click on the course in your transcript, and go to the Content tab to locate the exam.

How long will it take to complete the exam?

- Most exams take 45 to 90 minutes to complete. You may retake the exam multiple times to pass the exam.

How do I access and use the digital badge?

- After you pass the exam, you get a digital badge and instructions on how to place it on social media sites.

How is the digital badge validated?

- [Credly](#) validates the digital badge as issued to you by Cadence and includes the details of the criteria you completed to earn the badge.



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Icons Used in This Class



Best Practice



Language/
Command Syntax



Concept/
Glossary



Frequently Asked
Questions/
Quiz



Error Message



Problem & Solution



Quick Reference



GUI and Command



How To

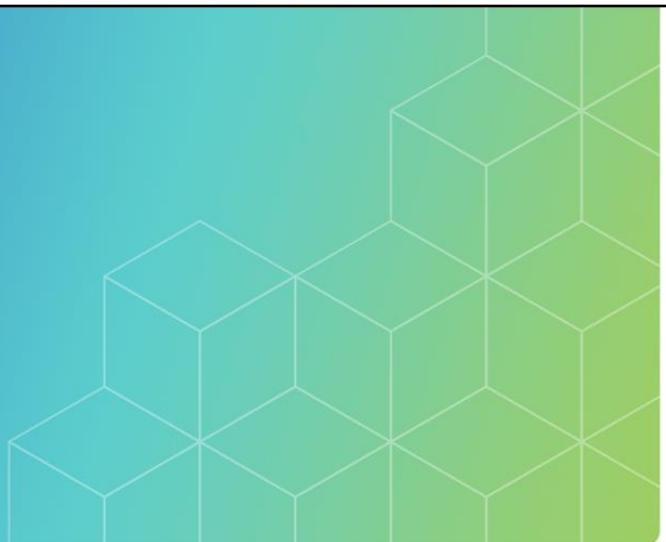
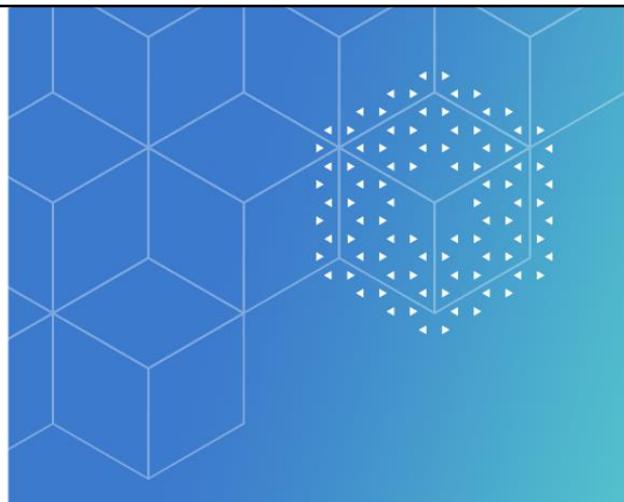


Lab List

Throughout this class, we use icons to draw your attention to certain kinds of information. Here are the icons we use, and what they mean.



This page does not contain notes.



Module 2

Introduction to OrCAD® X Capture

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Welcome to Module 2: Introduction to OrCAD® X Capture.

Module Objectives

In this module, you

- Start the Capture software
- Open an existing project
- Operate the Project Manager
- View schematic pages
- Enable and use toolbar icons
- Select and edit objects

Introduction to OrCAD X Capture

Setting Up Your Environment

Working with Libraries

Building a Simple Schematic

Building a Multi-Sheet Schematic

Editing Part Properties

Building a Hierarchical Design

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This is where you are in the course flow.

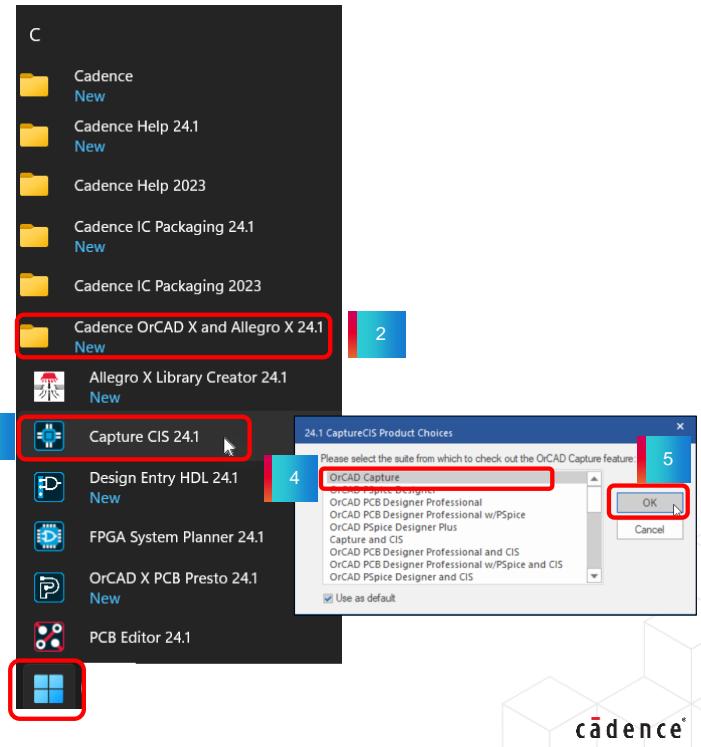
Starting OrCAD X Capture



OrCAD® X Capture is one of the most widely used **schematic design** software tools to create complex designs, hierarchical designs, reuse blocks, and variant design capabilities.

To start OrCAD X Capture, you

1. Click on the **Windows Start Menu**.
2. Select **Cadence OrCAD X and Allegro X 24.1**.
3. Click on **Capture CIS 24.1**.
4. Select a product – **OrCAD Capture** or **OrCAD X Capture**.
5. Click **OK** to open the OrCAD X Capture tool.



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OrCAD X Capture is one of the most widely used schematic design software tools to create complex designs, hierarchical designs, reuse blocks, and variant design capabilities.

Use the integrated OrCAD X tools to verify your design electronically by performing signal integrity or circuit analysis, and then export a physical board to Allegro X PCB Editor or OrCAD X presto layout tools.

To start the OrCAD X Capture tool, first click on the **Windows Start Menu**. Next, select **Cadence OrCAD X and Allegro X 24.1**, then click **Capture CIS 24.1**. When the Product Choices window is displayed, select a product – **OrCAD Capture** or **OrCAD X Capture**. Finally, click **OK** to open the OrCAD X Capture tool.

Starting OrCAD X Capture (continued)

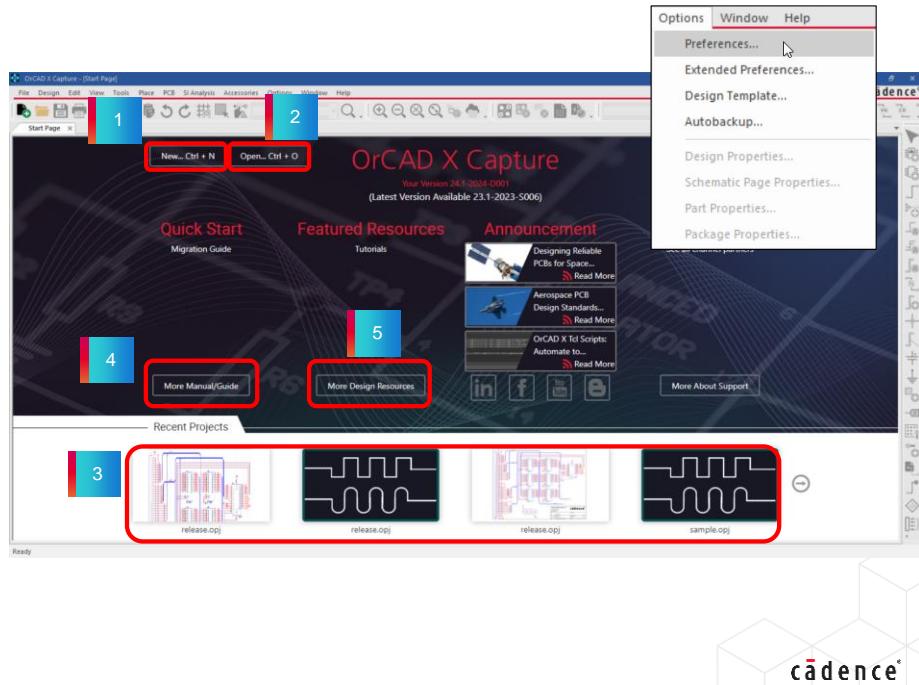
When you start OrCAD X Capture, the main window displays the Start Page.

Use the Start Page to:

1. Create a new project.
2. Browse to an existing project.
3. Open a recent project.
4. Open a user tool manual/guide.
5. View design resources.

OrCAD X Capture supports the .DSN Design file extension.

OrCAD X Capture supports the .OLB Library file extension.



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When you start OrCAD X Capture, the main window displays the Start Page. Use the Start Page to create a new project or to browse an existing one. You can also open the recent projects from the Recent Projects tab.

For more information about OrCAD X Capture or if you run into any issues, use the manual/guide or view the design resources.

Note that the OrCAD X Capture supports the .DSN design file extension. Capture also supports the .OLB library file extension.

Use the Options menu to set up preferences and the design template.

Note: You can disable the Start Page by editing your *Capture.ini* file and setting *EnableStartPage=False*. You can enable the Start Page by selecting the **Start Page** option from the pop-up **Help** menu.

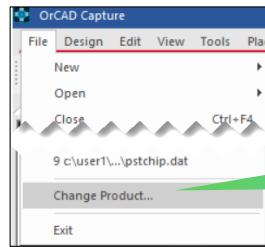
Opening a Capture Project



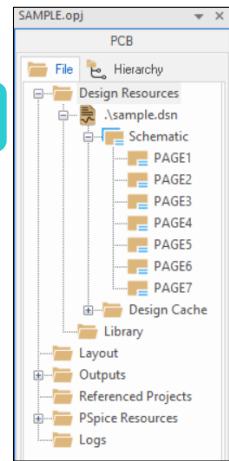
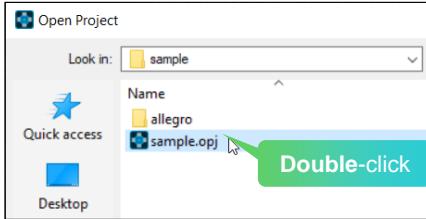
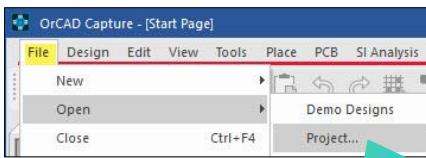
Choose **File – Open – Project –**
select **.opj** file or **.dsn** file.

Use the Open Project window to select an existing project .opj file or .dsn file.

- Capture reads the project file and opens the Project Manager window.
- You can also **double-click** on a .opj file to open the project.



To change the Cadence product license.



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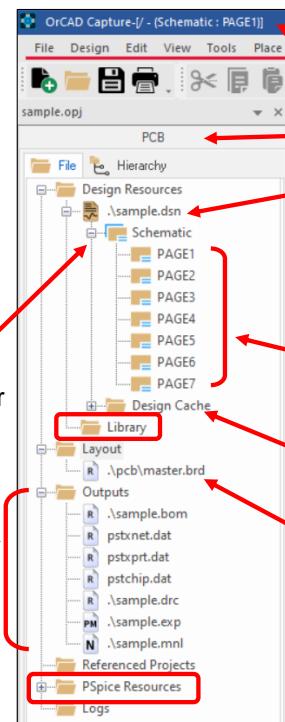
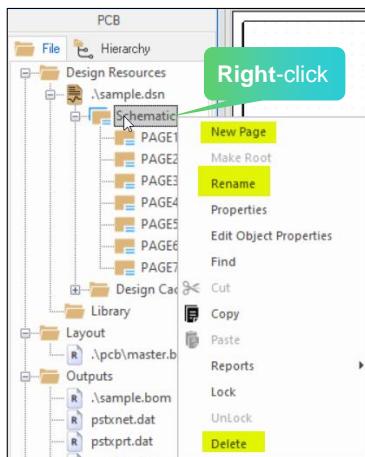
Before opening a project, you can use the **File – Change Product** command to select a Cadence license. Once a project has been opened, this command is grayed out.

To open the existing project, choose **File – Open – Project**, select an existing project **.opj** file, and **double-click** to open. Capture reads the project file and opens the Project Manager window.

Using the Project Manager



The Project Manager is a window that displays a directory tree of all the files related to your design or project.



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Click to expand a schematic folder, then double-click to open a schematic page.

The project name and project type are shown at the top of the Project Manager window.

You can use the Project Manager to open schematic pages and view reports or other project files (which open when you **double**-click on a page or filename). You can also use the right mouse pop-up menu to add, delete, or rename schematic pages.

You can open multiple projects at the same time and copy designs or schematic pages between Project Manager windows. You can also use the Project Manager to add libraries to your project setup.

When you exit a project, the settings and preferences are saved. For example, if a schematic page was open when you saved and exited the project, that schematic page will automatically display when you reopen that project.

A PSpice® Resources folder might also be present for use with PSpice.

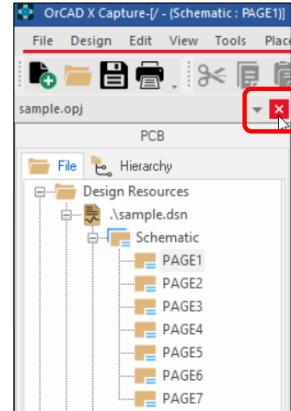
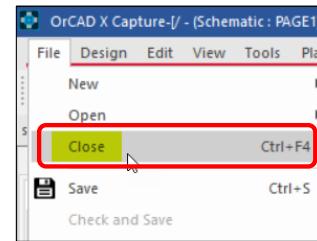
Closing a Project



With the Project Manager window active, choose **File – Close**.

You can also click on the Close icon in the upper-right corner of the Project Manager window.

- Everything about the open windows is recorded in the project file when you close a project.
- When the project is reopened, all windows are exactly as they were the last time the project was closed.
- This includes any expansion of the objects in the Project Manager window and any schematic page windows that were open when the project was closed (including zoom level).

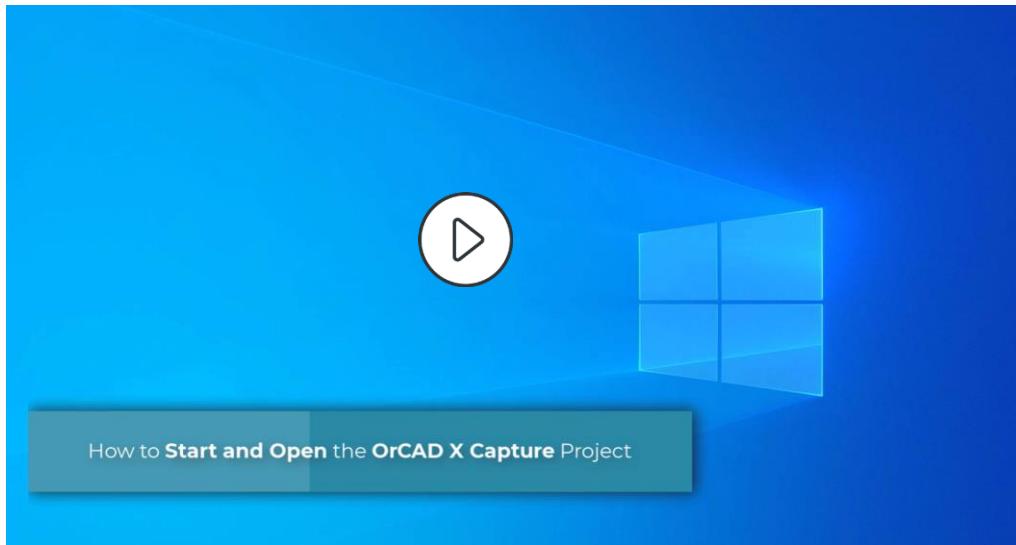


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With the Project Manager window active, choose **File – click on Close**, to close a project. You can also click on the Close icon in the upper-right corner of the Project Manager window.

When you close a project, everything about the open windows is recorded in the project file. When the project is reopened, all windows are exactly as they were the last time the project was closed. This includes any expansion of the objects in the Project Manager window, and also any schematic page windows that were open when the project was closed (including zoom level).

Demo: How to Start and Open the OrCAD X Capture Project



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Video Play Time: 3.33 minutes

Click the Play button to start the video.

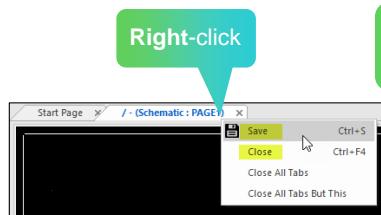
The Capture User Interface



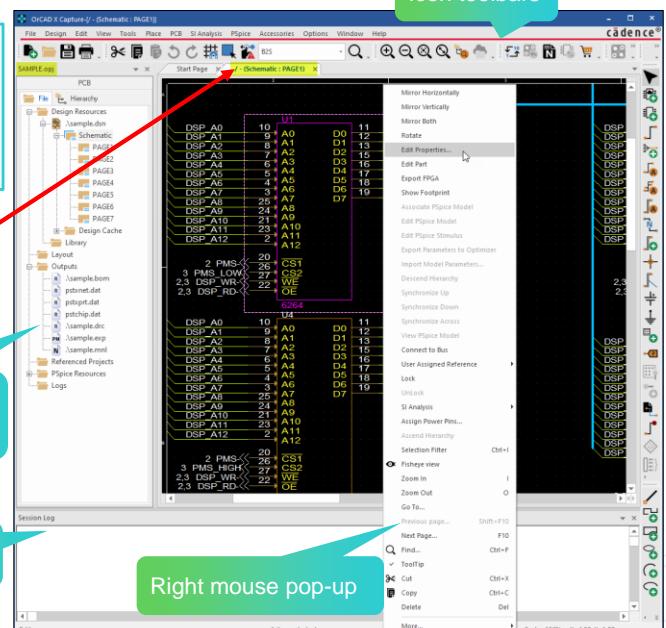
Capture is completely menu-driven.

All Capture commands are in pull-down menus, icon toolbars, right mouse pop-up menus, and keyboard shortcuts.

Click on any tabbed window to make it active, then **right-click** to access pop-up commands.



The Project Manager can be undocked.



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All the open documents are tabbed windows. You can **right-click** the tabs to save or close the windows.

Capture commands are context-sensitive. Access to commands will vary with different active windows, such as the Project Manager or schematic page.

When either window is selected, buttons and menu commands not relevant to the active window are grayed out or missing. You can only perform tasks that are relevant to the current or active window. You can apply a process to a specific page of the design by preselecting it before you perform the task. Menu choices are also affected by the project type.

The toolbars default to the top and right side of the Capture session window, but you can move them to any edge, make them float free of the session window, or change their shape.

The Session Log is a window that displays messages and errors. You can save the contents of the Session Log window to a file. The Session Log window does not create a log file that can be replayed.

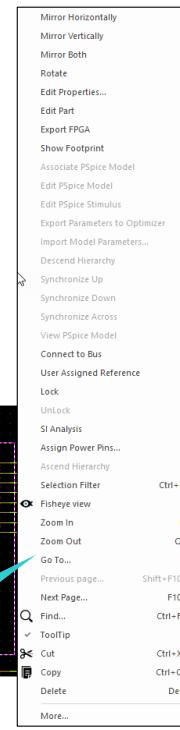
Context-Sensitive Right Mouse Pop-Up



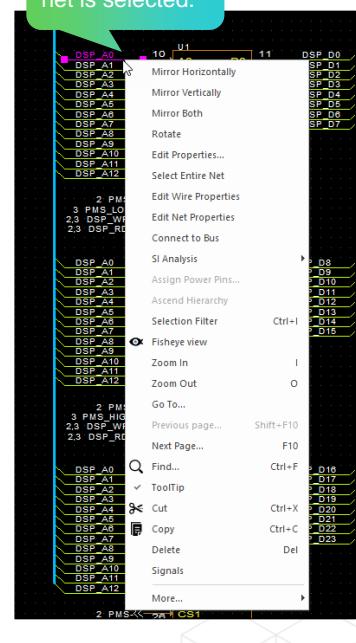
You can access editing commands from the right mouse pop-up menu.

These commands will vary depending on the object you've selected.

Use the right mouse button to apply commands to a selected object.



Pop-up when a net is selected.



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You can access editing commands from the right mouse pop-up menu. For example, if you select and **right-click** on the part, the command pop-up menu will be displayed. These commands will vary depending on the object you've selected.

Selecting and Deselecting Objects

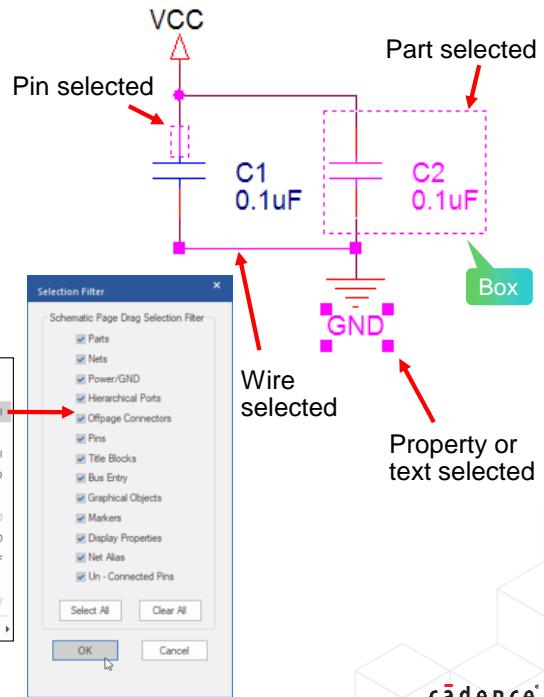
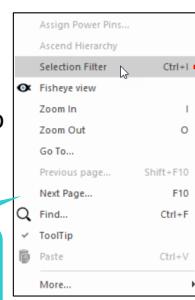


Selection Filter helps fine-tune a selection to only specific types of schematic or block objects, such as parts, nets, ports, pins, net alias, and many other options.

Access the Selection Filter from the right mouse pop-up on the Active Document Window.

- To select a single object, **left-click** on the object.
- To select multiple objects, press and hold the **Control** key while selecting individual objects.
- To select all objects in an area, click and drag to draw a selection rectangle around an area.

Right mouse on the active document window.



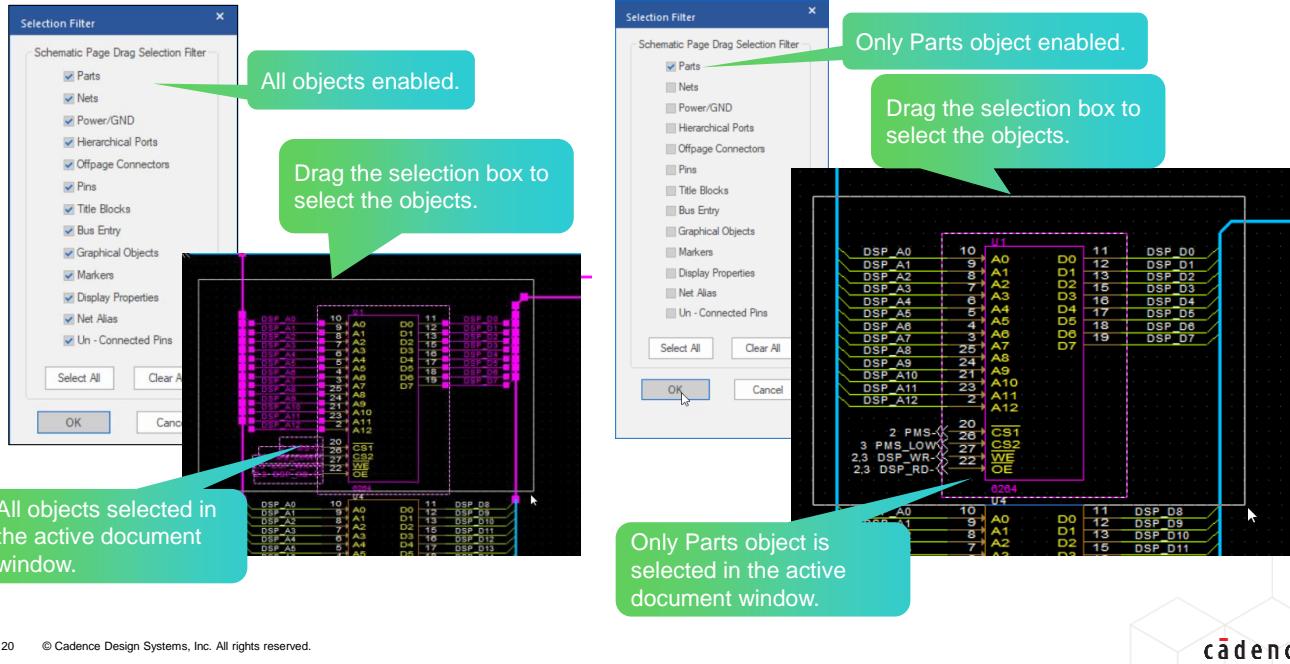
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The selection and deselection of Capture objects control your ability to edit, move, copy, delete, or edit properties. The accompanying illustration shows a selected part, wire, pin and text. When selecting parts, be sure you see the rectangular selection box around the entire symbol, not just one of its elements, such as a pin or text.

- To select a single object, **left-click** on the object (the selected object will be highlighted). **Tip:** While selecting, press and hold the **Tab** key to toggle between overlapping objects.
- To select multiple objects, press and hold the **Control** key while selecting individual objects.
- To select all objects in an area, click and drag to draw a selection rectangle around an area.
- To select all objects on a page, choose **Edit – Select All**.
- To select all objects of a given type, choose **Edit – Find** and specify search criteria for the objects you want to select.
- To deselect all selected objects, click in an open area, or use the **Esc** key.
- To remove an object from a selected set, use the **Control** key.

To access the Selection Filter, right mouse on the Active Document Window. Selection Filter pop-up provides checkbox options to select or exclude Parts, Nets, Power/Gnd, Title Blocks, etc. Only specific objects are selected when you perform the window or block-select operation.

Selecting and Deselecting Objects (continued)



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Click **Select All** to enable all the objects in the Selection Filter. If you draw or drag the selection box within its boundaries, all the objects are selected on the Active Document Window.

For example, to select only a part on the Active Document Window, on the Selection Filter, deselect all the options except the parts option; drag a selection box across the Active Document Window. Now, you will see only the parts object is selected.



Common Shortcut Keys

OrCAD X Capture comes with many helpful keyboard shortcuts.

I To zoom in, press the I keyboard key.

O To zoom out, press the O key.

R rotate

P place part

W place wire

N place net alias

T place text

H horizontal mirror

Ctrl +**scroll wheel** = zoom in and out

J place junction

X place no-connect

B place bus

E place bus entry

Ctrl + **E** edit properties

V vertical mirror

Use **F6** to toggle to full screen cursor mode.

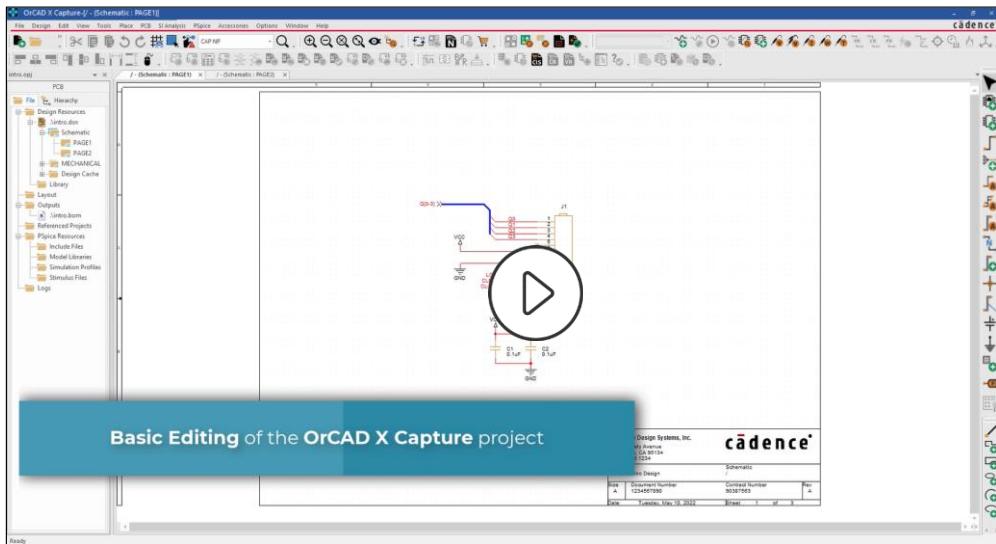
Use standard Windows® shortcut keys like:

Ctrl **C** **V** **Z**



In addition to the standard Windows shortcut keys like **Ctrl+C**, **Ctrl+V**, and **Ctrl+Z**, OrCAD X Capture comes with many helpful keyboard shortcuts. You cannot customize the function keys or create your own keyboard shortcuts.

Demo: Basic Editing of the OrCAD X Capture Project



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Video Play Time: 5.40 minutes

Click the Play button to start the video.



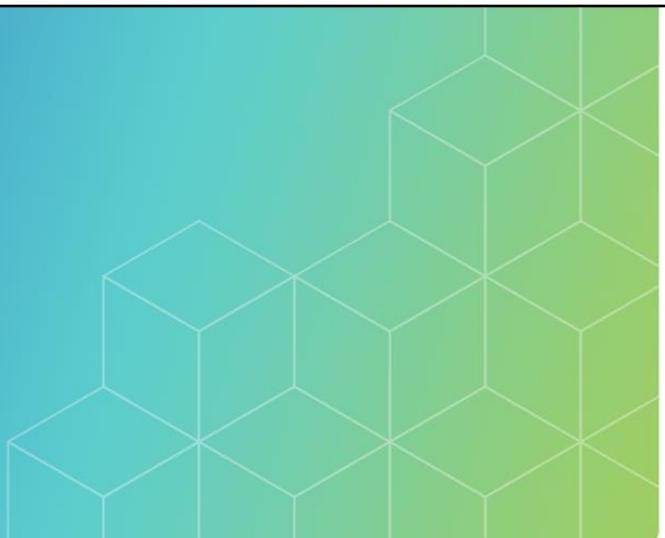
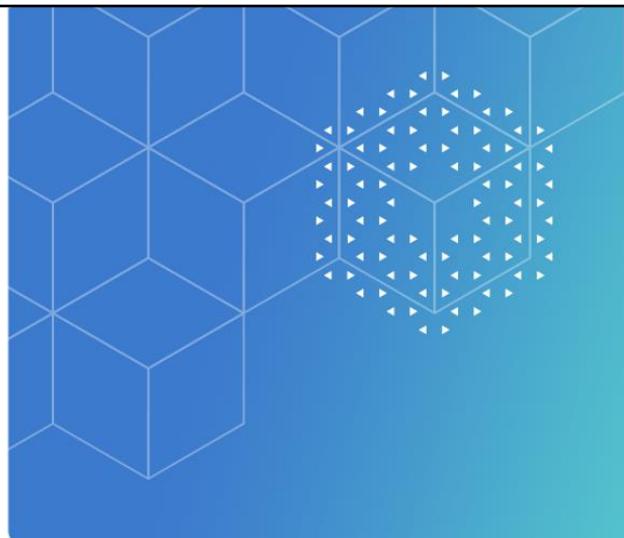
Labs

- Lab 2-1 Setting Environment Variables
- Lab 2-2 Opening the Sample Project
- Lab 2-3 Selecting Objects
- Lab 2-4 Editing Objects
- Lab 2-5 Using the Help System (Optional)

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You will now have the opportunity to perform some self-paced labs to reinforce the ideas presented in this module.



Module 3

Setting Up Your Environment

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Welcome to Module 3: Setting Up Your Environment.

Module Objectives

In this module, you

- Set user preferences
- Create a design template

Introduction to OrCAD X Capture

Setting Up Your Environment

Working with Libraries

Building a Simple Schematic

Building a Multi-Sheet Schematic

Editing Part Properties

Building a Hierarchical Design

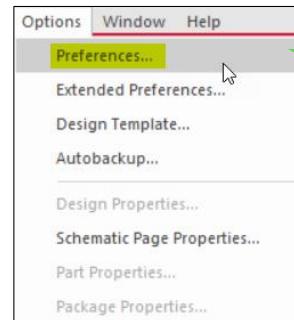


This is where you are in the course flow.

Setting User Preferences



Choose **Options – Preferences** in the Capture main session window to open the Preferences menu.



User preferences help you to set:

- Color assignments
- Grid display
- Pan and Zoom
- Area selection
- Line and fill style and many more

User preferences are saved in the *Capture.ini* file. These settings are immediately applied to the current design and all other designs you open (even designs created by others).

The default *Capture.ini* file is located at `$CDSROOT/tools/bin`.

When you make changes to the default user preferences, a local *Capture.ini* file is created in the `$HOME/cdssetup/OrCAD_Capture/<release_version>`.

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Use the Preferences menu to set user preferences. User preferences are workstation-specific. For example, if you copy a design from another machine and open it on your machine, your user preferences (color assignments, grid display) are applied.

To set the user preferences in the Capture main session window, choose **Options – Preferences**.

User preferences are stored in the *Capture.ini* file (not in the design database). Changes to user preferences take effect immediately.

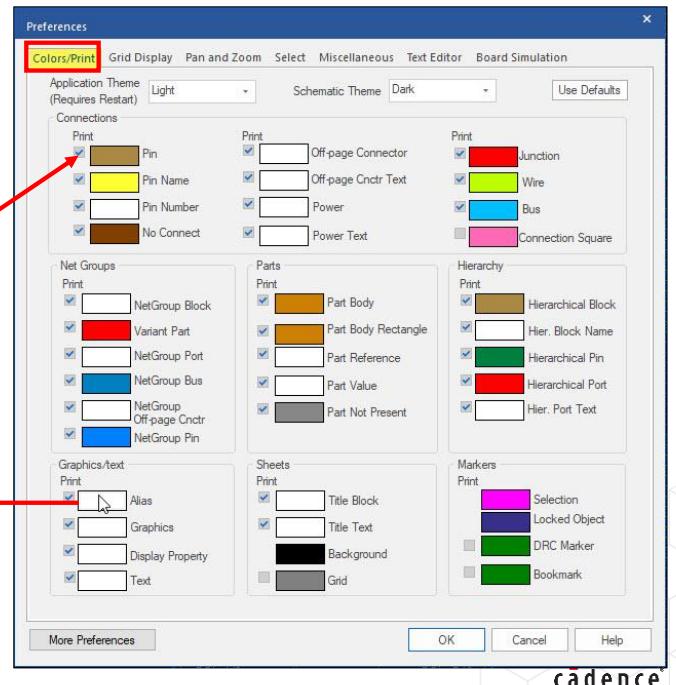
The default *Capture.ini* file is located at `$CDSROOT/tools/bin`. When you change to the default user preferences, a local *Capture.ini* file is created in the `$HOME/cdssetup/OrCAD_Capture/<release_version>`, where CDSROOT is where you installed the Cadence software, and <release_version> is the version of Cadence software you have installed. The HOME variable is defined during software installation (for example, D:\SPB_Data).

Color Assignments



In the **Colors/Print** tab of the Preferences menu, click on the color square for an object type (for example, Alias) and select a new color from the color palette.

The checkboxes next to each object type are used to control the visibility of design objects on hardcopy prints.



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Use the **Colors/Print** tab to assign colors to design objects, and The checkboxes next to each object type are used to control the visibility of design objects on hardcopy prints.

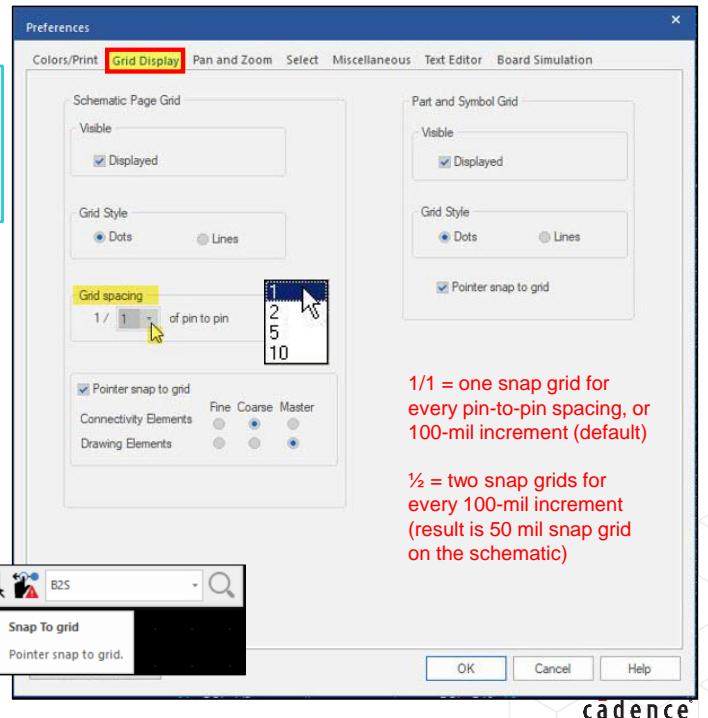
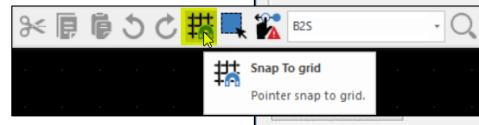
Grid Display



Click in the **Grid Display** tab of the Preferences menu to control grid style and spacing.

For the schematic page editor and the part editor, specify:

- Whether to display the grid.
- Whether the grid uses dots or lines.
- The grid spacing (the space between each point on the grid).
- Whether the pointer snaps to the grid as you place objects.



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Click in the Grid Display tab of the Preferences menu to control grid style and spacing.

For the schematic page editor and the part editor, specify:

- Whether to display the grid.
- Whether the grid uses dots or lines.
- The grid spacing (that is, the space between each point on the grid). Capture uses the default 100-mil grid.
- Whether the pointer snaps to the grid, the pointer snaps to the grid option and forces all parts, wires, and text to snap to this grid. The snap to grid option is available from the main toolbar.

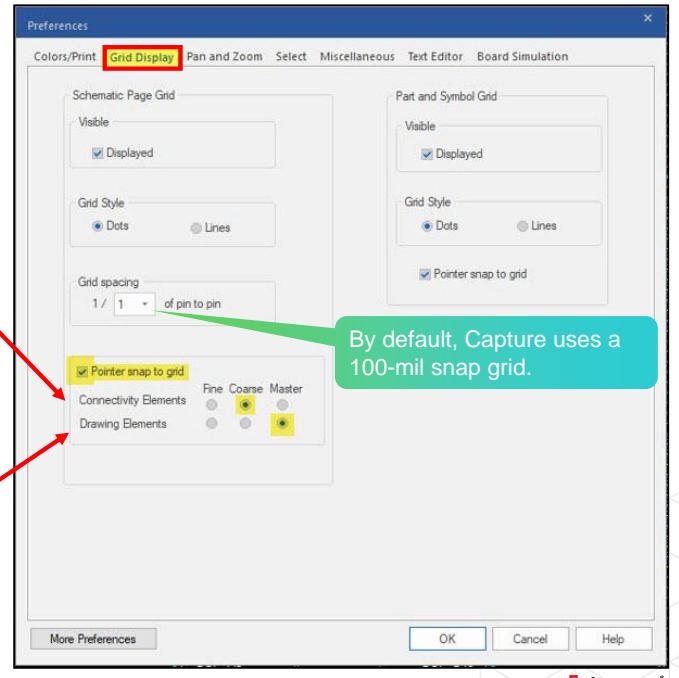
When you are using part and wire pointer snap to grid is on default, use this option to turn off when adjusting the location of text and properties only.

The **View – Grid** command can also be used to toggle the grid on or off.

Grid Display (continued)

Click the **Coarse** radio button for Connectivity Elements in the Pointer snap to the grid section of the Grid Display tab.

- This will force all parts and wires onto the 100-mil snap grid, even when snap to grid is turned off.



Click the **Master** radio button for Drawing Elements in the Pointer snap to the grid section of the Grid Display tab.

- When the snap to grid is on, text and graphics will use the 100-mil snap grid. When the snap to grid is off, text and graphics use a fine grid.

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By default, Capture uses a 100-mil snap grid spacing. The Pointer snap to grid option is on by default.

The Pointer snap to grid option controls grid snapping for connectivity elements (parts and wires) and drawing elements (text, lines and other graphics).

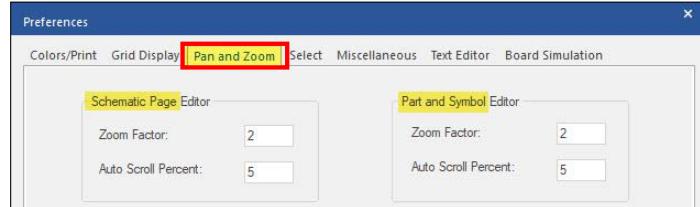
Set a Coarse snap grid for Connectivity Elements to move parts and wires based on the snap grid spacing. Set a Fine snap grid for Drawing Elements to have almost gridless movement of text, lines and rectangles. The Master setting works in conjunction with the Pointer snap to grid setting. When the Pointer snap to grid is on, a setting of Master snaps drawing elements to the snap grid. When the Pointer snap to grid is off, the Master setting snaps drawing elements to a fine grid.

Pan and Zoom Preferences



Click on the **Pan and Zoom** tab of the Preferences menu and set the Zoom Factor to an integer between 2 and 10.

- When you use the Zoom In or Zoom Out icons, Capture uses this setup menu to determine how far to zoom in or out.
- Similarly, the amount of zoom performed by the View – Zoom menu or the I (Zoom In) and O (Zoom Out) shortcut keys is also controlled here.



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When you use the Zoom In or Zoom Out icons, Capture uses this setup menu to determine how far to zoom in or out. Similarly, the amount of zoom performed by the View – Zoom menu or the I (Zoom In) and O (Zoom Out) shortcut keys is also controlled here. The zoom factor must be an integer between 2 and 10 (no fractions or decimals).

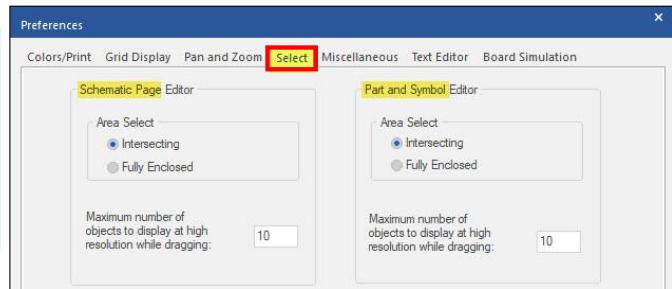
The Auto Scroll Percent option controls how fast the schematic page scrolls when you drag an object into the border area of the schematic window. This is an old feature that has been replaced by selecting the C key, holding it down, and moving the mouse to pan the work area.

Area Selection Preferences

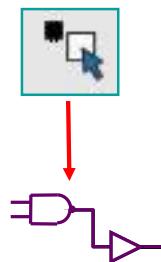


Click the **Select** tab of the Preferences menu and choose the **Intersecting** or **Fully Enclosed** radio buttons in the Area Select section of the form to control how the selection by rectangle command works.

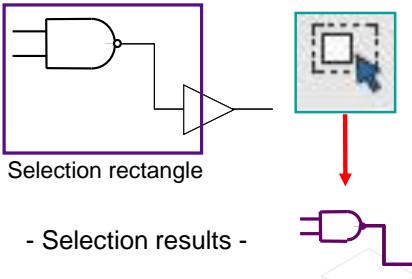
- When you drag a rectangle to select multiple objects, all objects intersected by the rectangle are selected by default.
- Use the Select tab to modify preference settings so that only objects fully enclosed within the rectangle are selected.
- In the accompanying illustration, the same selection rectangle yields different results depending on your preference settings.



Intersecting icon ON



Fully Enclosed icon ON



- Selection results -

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When you drag a rectangle to select multiple objects, all objects intersected by the rectangle are selected by default. Use the Select tab to modify preference settings so that only objects fully enclosed within the rectangle are selected.

After selecting multiple objects within an area, you may plan to move them. The *Maximum Number of Objects to display* option is an older setting that, with the advent of high-resolution graphics cards, is no longer needed.

When you drag a number of objects greater than this value, a simple box replaces the symbol graphic for each part.

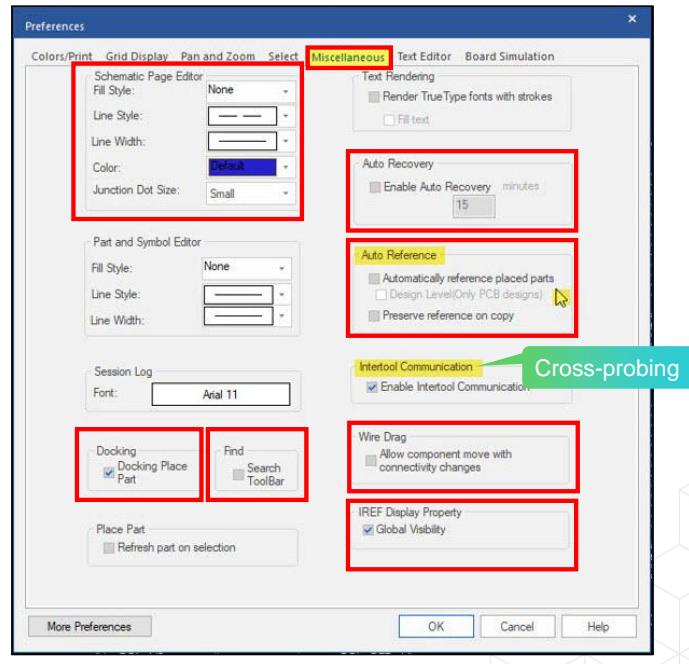
Miscellaneous Preferences



Click in the **Miscellaneous** tab of the Preferences menu to define the characteristics of nonelectrical graphics such as polygons and lines.

Use the Miscellaneous tab to set:

- Schematic Page Editor
- Docking
- Find
- Auto Recovery
- Intertool Communication
- Auto Reference
- Wire Drag
- IREF Display Property



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Set the default line draw mode for the schematic page by choosing **Schematic Page Editor – Fill** and **Line Style** and **Line Width**.

Docking lets you open and dock the Place Part command box and leave it open as you find and place parts on the schematic page.

Find lets you open and dock the find command or Search toolbar.

The **Auto Recovery** option protects you from loss of work due to a system crash or power failure. OrCAD Capture automatically saves design changes at the end of each Auto Recovery interval (in minutes). These backup files are saved to the current working directory and are automatically deleted when you exit normally. If no changes have occurred since the last save, no auto-recovery (backup) is performed.

The **Intertool Communication** option lets Capture interact with the OrCAD and Allegro® PCB Editor tools. For example, you can cross-probe parts and nets in the schematic and correspond them to parts and nets in the PCB design.

The **Auto Reference** option automatically gives you the next reference designator in a sequence.

Preserve reference on copy enables part references to be preserved while pasting apart into a schematic. When you copy a part and paste it on a schematic page, the part will retain the same reference designator as that of the copied part. But, if you place a new part on a schematic page, Capture will assign the reference designator found in the library, such as U?A or J??P.

The **Wire Drag** controls what happens when you drag a connected object. This is explained in the next slide.

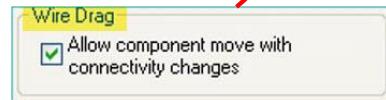
The **IREF Display Property** setting displays the Intersheet Reference text after it is generated.

Drag Connected Object

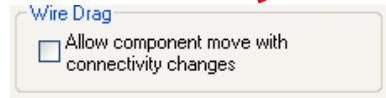


Click the Wire Drag checkbox in the Miscellaneous tab of the Preferences menu to control what happens when you drag a connected object.

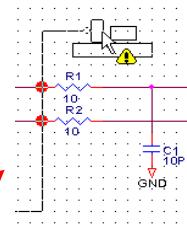
When the Wire Drag option is enabled, error markers are displayed where the connectivity changes are occurring, and the move is allowed to finish.



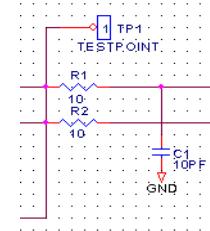
With this option turned off, there are no error markers to indicate connectivity changes are going to take place, and you are not allowed to place the part until the yellow warning icon is cleared.



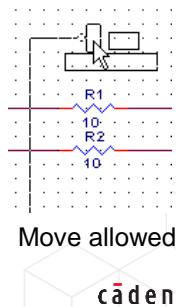
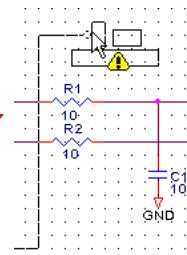
During move



After move



You can also use this icon in Capture to toggle Wire Drag on/off.



Move not allowed

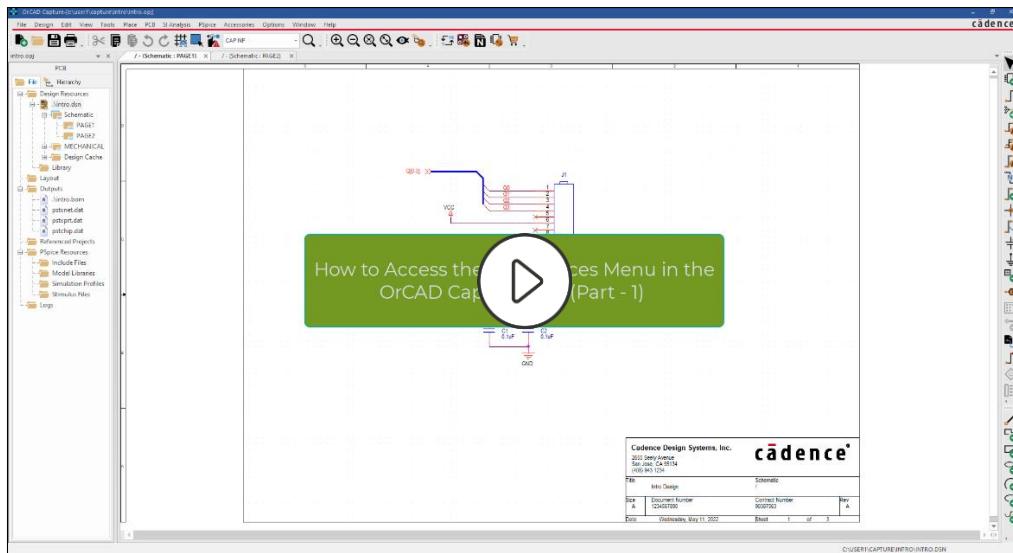
Move allowed

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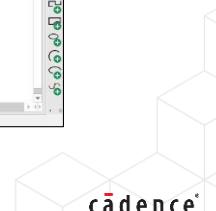
33 © Cadence Design Systems, Inc. All rights reserved.

When the Wire Drag option is enabled, error markers are displayed where the connectivity changes are occurring, and the move is allowed to finish. With this option turned off, there are no error markers to indicate connectivity changes are going to take place, and you are not allowed to place the part until the yellow warning icon is cleared.

Demo: Accessing the Preferences Menu (Part 1)



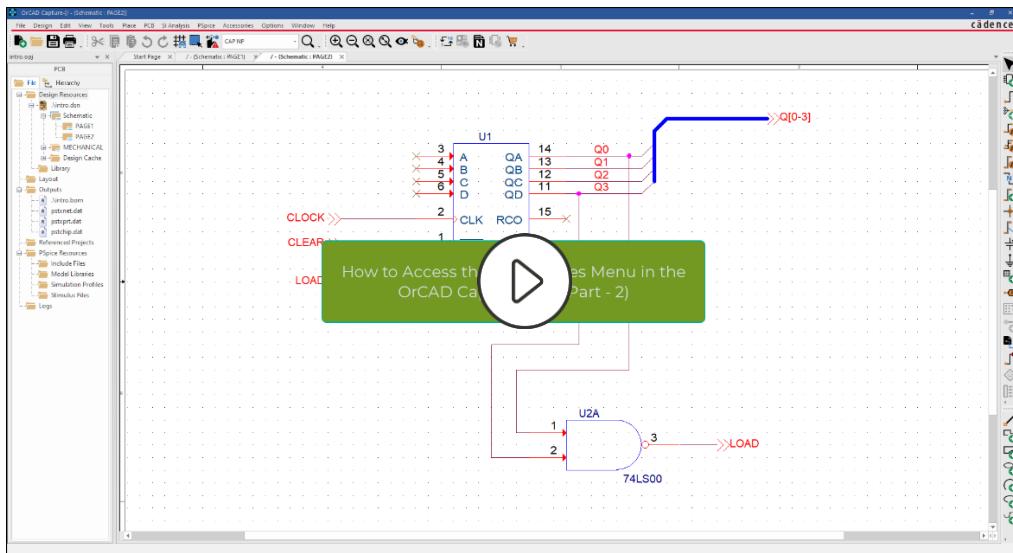
34 © Cadence Design Systems, Inc. All rights reserved.



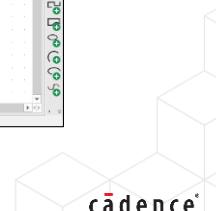
Video Play Time: 5.19 minutes

Click the Play button to start the video.

Demo: Accessing the Preferences Menu (Part 2)



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Video Play Time: 4.56 minutes

Click the Play button to start the video.

Setting Up the Design Template



Choose **Options – Design Template** to access the Design Template window.

Choose **Options – Design Properties** to access the Design Template window for the current design only.

Choose **Options – Schematic Page Properties** to override some of the design template settings for the current page only.

The design template is automatically applied whenever you create a new design.

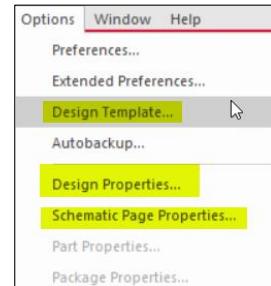
A design template controls:

- Text fonts and size
- Title block
- Page size
- Grid settings

These settings are saved in a **Capture.ini** file and applied to new designs only.

Changes to your design template settings do not affect existing designs.

Once applied, these settings are retained in the design even when transferred.



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The design template is used whenever you create a new design. These settings are retained in the design even when it's transferred to another workstation.

Design template settings are stored in the *Capture.ini* file. When you create a new design, these settings in the *Capture.ini* file are only applied. When you change the design template, existing designs are not affected.

You can use the **Options – Design Properties** command to change some of the design template settings for the current design only.

You can also use the **Options – Schematic Page Properties** command to override some of the design template settings for the current page only.

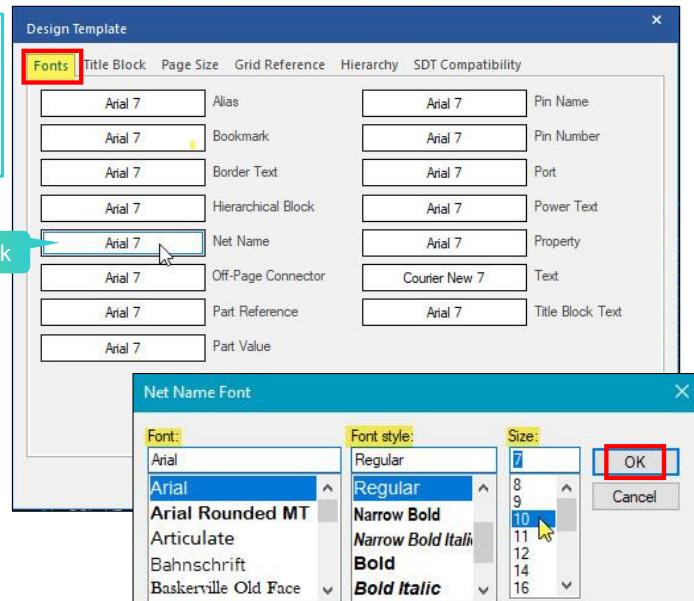
Fonts Tab



Click the **Fonts** tab in the Design Template window to control the text style and size for net names, reference designators and properties.

- You can define the fonts for schematic page objects that contain text, such as part references and values.
- In new designs, you can define the fonts assigned to the text associated with different schematic page objects.
- The fonts specified here do not affect existing designs.

Left-click



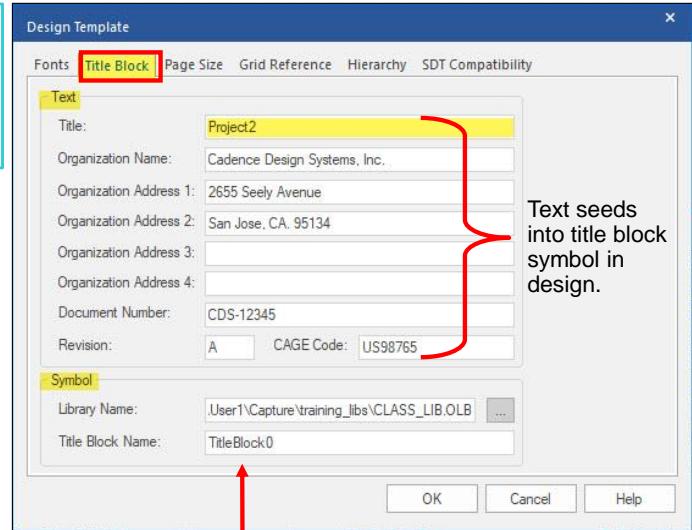
- From the Options menu, choose **Design Template – Fonts**.
- Click the left mouse button on the font of an object. A standard Windows font dialog box appears.
- Select a Font, Font style, and Size.
- Click **OK** to apply the changes.

Title Block Tab



Click the **Title Block** tab in the Design Template window to specify a title block symbol and associated title block text.

- Once these design template settings have been applied to a new design, the specified title block symbol and associated title block text will appear on all schematic pages.
- Remember to change the Title field before starting a new Capture design.



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Use the **Title Block** tab to specify which title block symbol you want to be added to schematic pages. You can also fill in your company name and address.

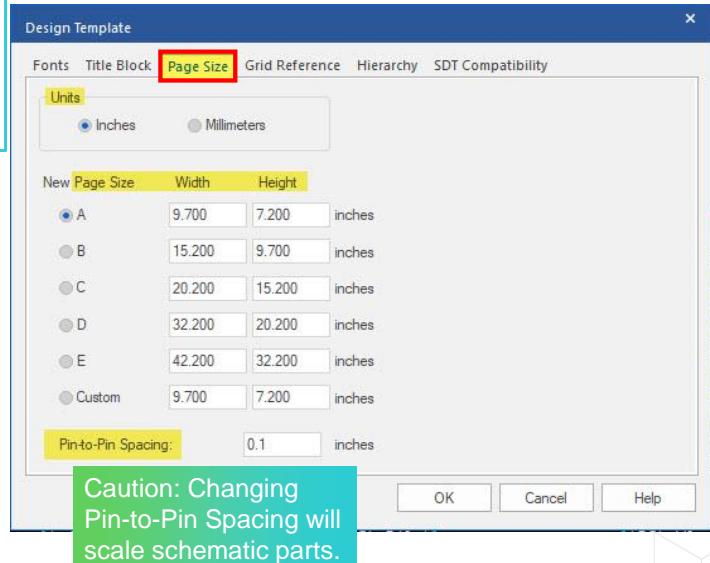
If you specify Title, Document Number, or Revision information in the template, remember to change these fields before starting a new design.

Page Size Tab



Click the **Page Size** tab in the Design Template window to set up the default page size.

- Do not change the Pin-to-Pin Spacing field. (Always use a 100-mil spacing or 0.1 inches.)
- The Pin-to-Pin Spacing field scales the schematic. For example, a Pin-to-Pin Spacing of 200 mils changes the size of parts by a factor of 2 to 1 because the distance between adjacent pins is 200 mils.
- By default, your snap grid spacing is equal to the Pin-to-Pin Spacing (see also the Grid Display tab in the **Options – Preferences** command).



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Use the **Page Size** tab to set the default page size for new schematic pages. Also, use this tab to specify a unit of measure and the page dimensions.

Capture always maintains one pin-to-pin spacing increment between pins. The default size of the pin-to-pin spacing increment is 100 mils. The *Pin-to-Pin Spacing* field changes the size of the pin-to-pin increment (which changes the distance between pins). Do not change the *Pin-to-Pin Spacing* field. (Always use a 100-mil spacing or “tenth of an inch”.)

For example, a Pin-to-Pin Spacing of 200 mils changes the size of parts by a factor of 2 to 1 because the distance between adjacent pins is 200 mils. Thus, the Pin-to-Pin Spacing field scales the schematic.

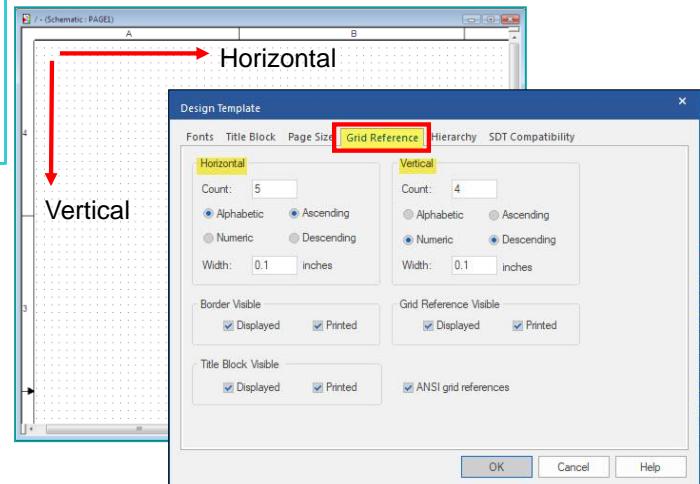
By default, your snap grid spacing is equal to the Pin-to-Pin Spacing (see also the Grid Display tab in the **Options – Preferences** command).

Grid Reference Tab



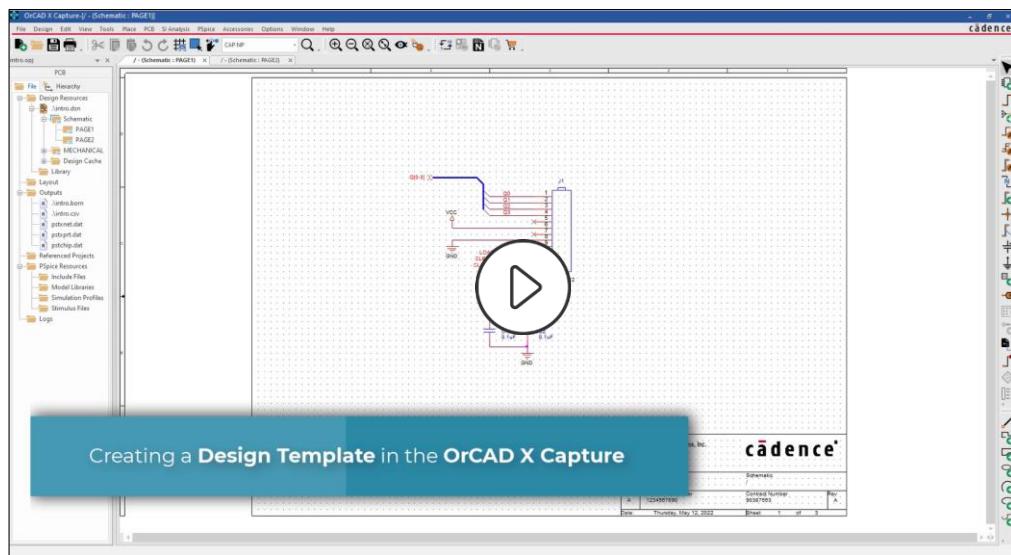
Click the **Grid Reference** tab in the Design Template window to define the alpha-numeric grid zones that start from the upper-left corner and appear across the top and left edges of the schematic pages.

This page formatting is helpful for locating a part in the design given its intersheet reference, its page number, and its position in the matrix grid.



Use the **Grid Reference** tab to define the grid zones across the top and left edges of schematic pages. Also, use this tab to control the visibility of the title block.

Demo: Creating a Design Template



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Video Play Time: 6.24 minutes

Click the Play button to start the video.

Labs



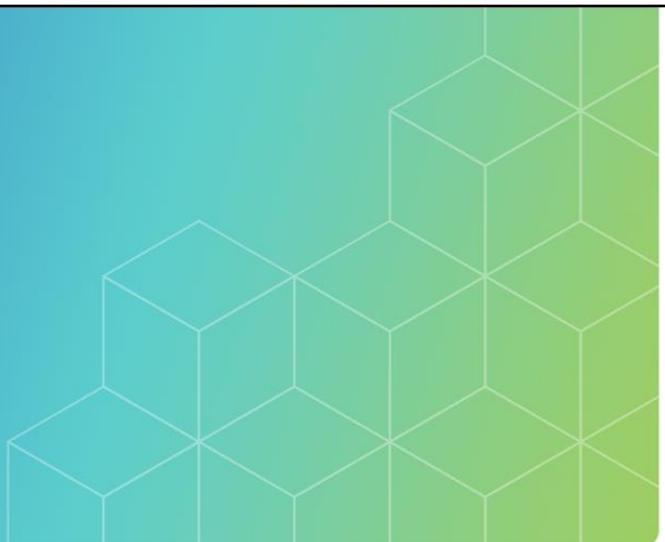
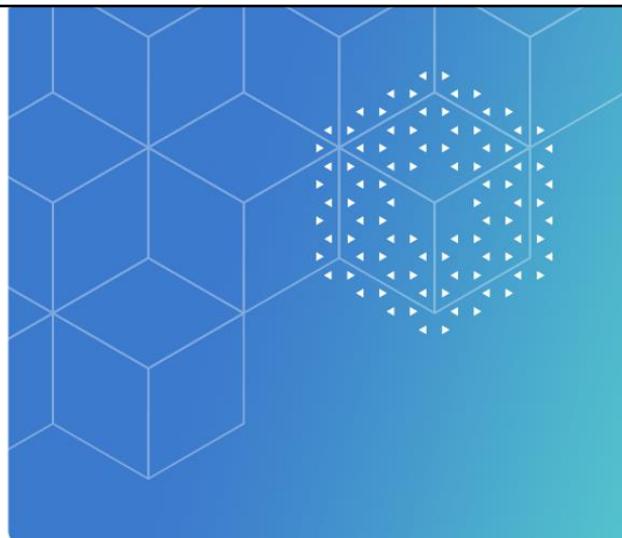
Lab 3-1 Setting Up Preferences

Lab 3-2 Setting Up the Design Template

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You will now have the opportunity to perform some self-paced labs to reinforce the ideas presented in this module.



Module 4

Working with Libraries

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Welcome to Module 4: Working with Libraries.

Module Objectives

In this module, you

- Open an existing library
- Create a new library
- Copy and rename parts and symbols
- Create a homogeneous part
- Create a heterogeneous part
- Create a power symbol
- Create a part from a spreadsheet
- Split an existing part
- Generate a part from a text file

Introduction to OrCAD X Capture

Setting Up Your Environment

Working with Libraries

Building a Simple Schematic

Building a Multi-Sheet Schematic

Editing Part Properties

Building a Hierarchical Design

This module covers various tasks including opening an existing library, creating a new library, copying and renaming parts and symbols, creating homogeneous and heterogeneous parts, creating a power symbol, creating a part from a spreadsheet, splitting an existing part, and generating a part from a text file.

This is where you are in the course flow.

Browsing an Existing Library

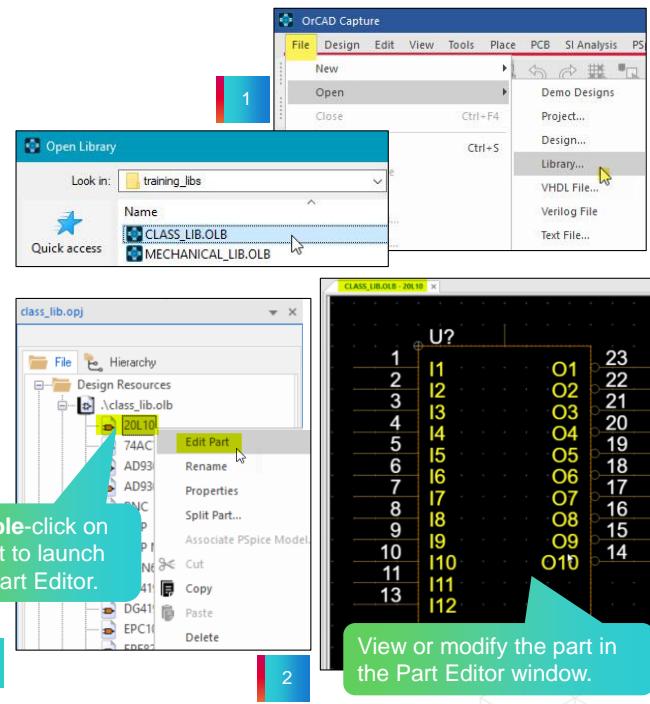


When working with libraries, it's common to open many parts to see how they were built. As a librarian, you may be interested in copying the part and modifying it to make a new part.

To browse an existing library, you:

1. Choose **File – Open – Library** and select a <library_name>.olb file to open an existing library.
2. Use the right mouse pop-up menu in the Project Manager to view a part in the Part Editor.

OrCAD® X Capture supports the .OLB Library file extension.



This page does not contain notes.

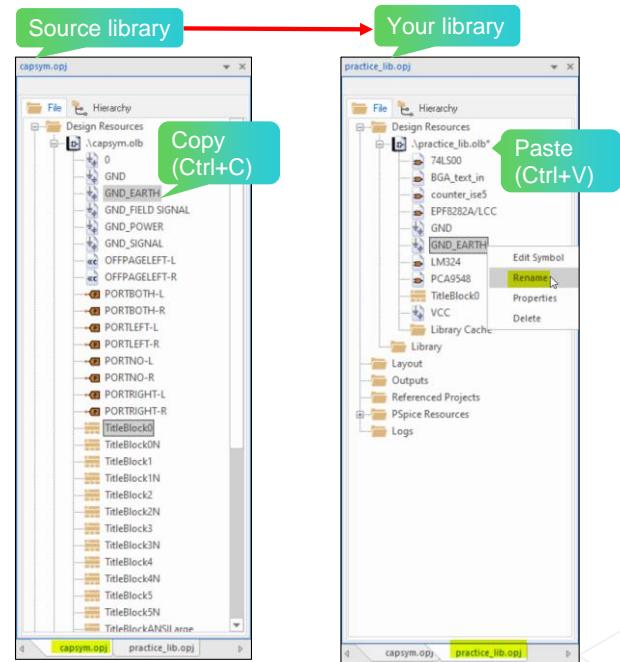
Copying Parts Between Libraries



It's common to copy parts from a Cadence®-supplied library and modify them for use in your library.

- One way to copy and paste a part from one library to another is to open both libraries first.
- After you have selected the part(s), choose **Edit – Copy** to copy from the source library, click on the target library, and choose **Edit – Paste** to paste the part from the source library to the target library.
- You can also open a part in one library and use the **File – Save As** command to save the part in another library.

Never modify the **default libraries** supplied with the Capture software. Instead, use them as source libraries.



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To copy and rename a part in the same library, select the part and use the **Edit – Copy** command.

Then choose **Design – Rename** to change the name of the original part. Next, paste the copied part back into the library. Finally, open the renamed part and modify it.

Creating a New Library

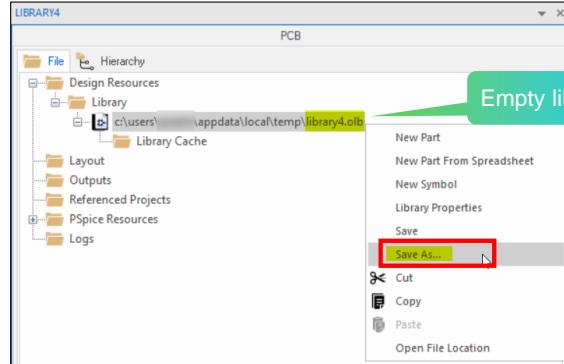
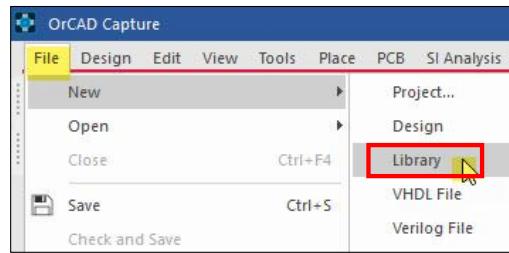


Choose **File – New – Library** in the Capture main session window to create a new library.

When you create a new library, its location defaults to a directory in the Cadence software hierarchy.

After the new library is created, use the **Save As** command to change the name and/or location of the library.

Note: Do not use spaces in directory names, library names, design names, net names, pin names, pin numbering, footprint names, or property names and values.



Choose **File – New – Library** to create a new Part Library. This creates a library *shell or empty library*.

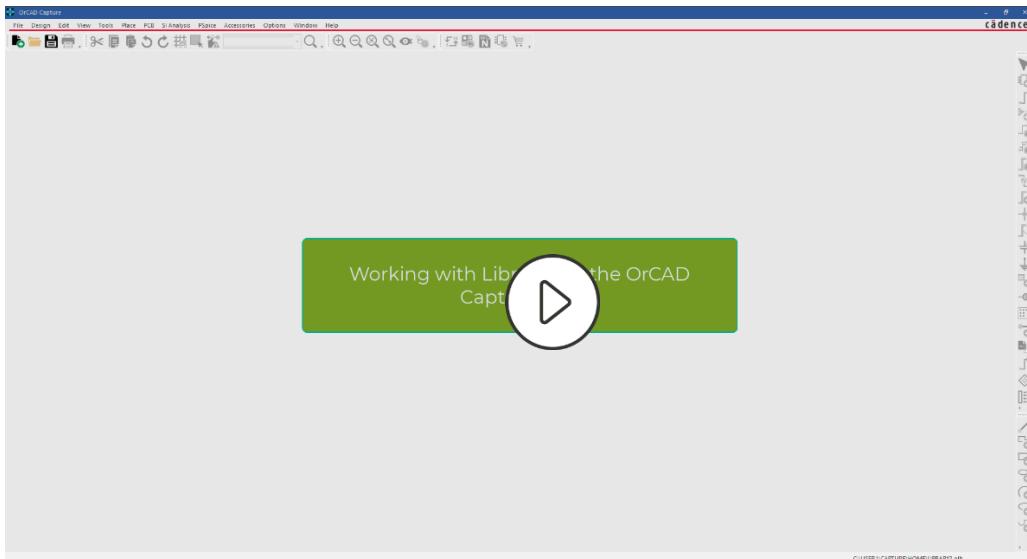
Never create or save your own libraries in the same directory where the OrCAD X Capture libraries are loaded. Make sure you keep them in an entirely different location.

The OrCAD X Capture libraries supplied by Cadence are organized by part function (such as OpAmp, Discrete, Gate). It is recommended that you organize your new libraries in a similar fashion.

If you choose **File – New – Library** while a project is open, the new library location defaults to the current project directory. This *project* library appears in the *Library* folder in the Project Manager window and is automatically accessible whenever you open the project.

After the new library is created, use the **Save As** command to change the name and/or location of the library.

Demo: Working with the Libraries



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Video Play Time: 4.15 minutes

Click the Play button to start the video.

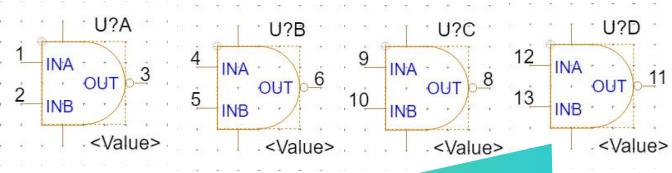
What Is a Homogeneous Part?



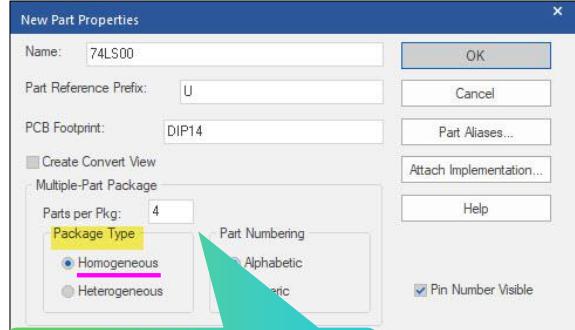
A homogeneous part is a part whose physical package contains identical schematic symbols.

The simplest and most common type of part is a homogeneous part. Homogeneous parts have either of the following:

- A Parts per Pkg field set to 1 and a single schematic symbol that represents the entire physical package for the part (called single-section).
- A Parts per Pkg field set to 2 or more and all the schematic symbols in the package are identical (same number of pins with the same logical pin name called multi-section).



The package holds identical logic parts, each with its own unique physical pin numbers.



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A homogeneous part is a part that has only one part graphic. If you define the part as having two or more parts per package, this means the package holds two or more identical logic parts, each with its own unique physical pin numbers.

When you create a homogeneous part, you create one part graphic only. If the part graphic represents the entire package (called single-section), then Parts per Pkg is set to 1. If the part graphic represents just a portion of the entire package (called multi-section), then Parts per Pkg is set to 2 or more.

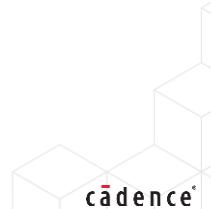
How to Create a New Part?



There is always a need to create new library parts to support the design process. The part creation process defines symbol graphics, electrical data, and properties used by different tools in the PCB design flow.

- The Cadence-supplied libraries are saved in `%CDSROOT%\tools\capture\library`.
- Never edit the Cadence-supplied libraries.
- Never create or save your own libraries in the same directory where the OrCAD X Capture libraries are loaded. Make sure you keep them in an entirely different location.

- 1 Adding a New Part to a Library
- 2 Adding Graphics
- 3 Adding Pins
- 4 Adding Power Pins
- 5 Editing a Pin
- 6 Defining the Physical Packaging
- 7 Adding User Properties

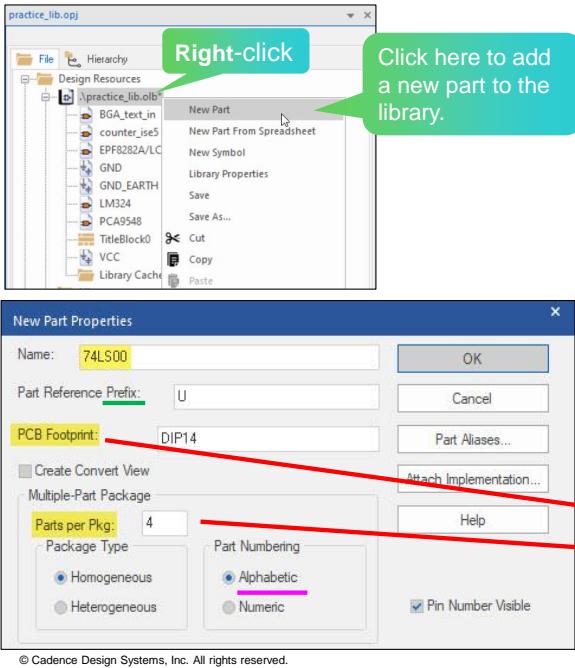


To create a new Part, follow these steps:

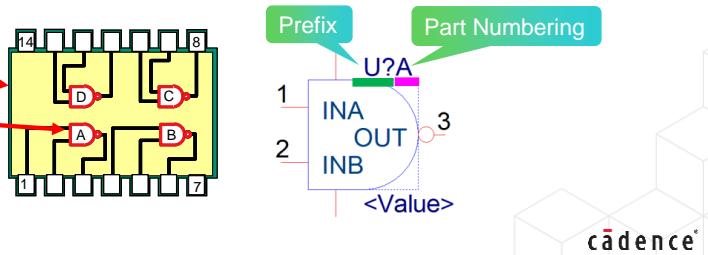
1. Adding a New Part to a Library
2. Adding Graphics
3. Adding Pins
4. Adding Power Pins
5. Editing a Pin
6. Defining the Physical Packaging
7. Adding User Properties

After adding the user properties, save and close the part editor window.

Step 1: Adding a New Part to a Library



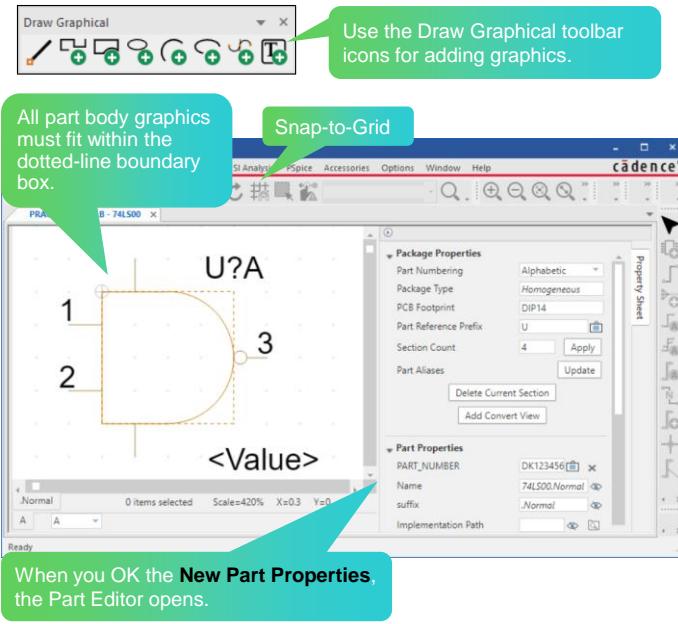
- | | |
|---|---------------------------------|
| 1 | Adding a New Part to a Library |
| 2 | Adding Graphics |
| 3 | Adding Pins |
| 4 | Adding Power Pins |
| 5 | Editing a Pin |
| 6 | Defining the Physical Packaging |
| 7 | Adding User Properties |



Use the New Part Properties dialog box to create a new part in a current or active library.

- **Name** – Specifies the part's name. This is used as the default part value when the part is placed on a schematic page. Part names can be up to 31 characters long (for example, R1206, RN55).
- **Part Reference Prefix** – Specifies the first letter of the reference designator (“C” for capacitor or “R” for resistor).
- **PCB Footprint** – Specifies the name of the footprint pattern used during the PCB layout process (for example, SM_1206).
- **Create Convert View** – Controls the creation of an alternate version. You might use the convert option to define a DeMorgan equivalent. A part with this option specified will have two views (a normal and a convert) that you can switch between once the part has been placed in the schematic.
- **Parts per Pkg** – Specifies whether or not there are multiple parts in the package (for example, gates).
- **Package Type** – Specifies whether all the logical parts in the package are symmetrical (homogeneous) or asymmetrical (heterogeneous). This setting cannot be changed once the part has been created.
- **Part Numbering** – Specifies whether the logical parts in the package are identified by letter or number. For example: U?A (alphabetic) or U?-1 (numeric).
- **Part Aliases** – Lets you add technology-specific aliases for the current part (such as 5400, 7400, 74LS00, and so on). Do not use part aliases to create your parts library for PCB design or Capture CIS.
- **Attach Implementation** – Specifies a behavioral model for simulation or an underlying schematic for a hierarchical block.

Step 2: Adding Part Graphics



- | | |
|---|---------------------------------|
| 1 | Adding a New Part to a Library |
| 2 | Adding Graphics |
| 3 | Adding Pins |
| 4 | Adding Power Pins |
| 5 | Editing a Pin |
| 6 | Defining the Physical Packaging |
| 7 | Adding User Properties |

Note: Do NOT turn off Snap-to-Grid when placing pins on the part. Pins MUST fall on a 100-mil grid.



The **Draw Graphical** toolbar is usually located on the right side of the Capture window but can be moved to any location. Only the icons used to create part bodies will be activated. You can also access the same commands from the Place pull-down menu. Most of these graphic commands are also available when editing a schematic.

Initially, the Part Editor contains a dotted-line part boundary box and placeholder properties for the reference designator and part value.

All part body graphics must fit within the dotted-line boundary box (except for pins that anchor along the edges of the part boundary box).

The **boundary box** also defines the selection area for the part when used in the schematic.

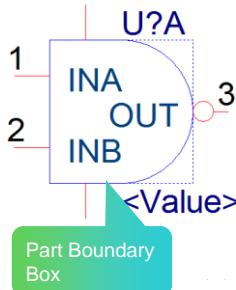
The dotted boundary box automatically enlarges to surround the part graphics you create. If the part graphics are smaller than the boundary box, the box size must be reduced manually.

All part graphics snap to a 100-mil grid in the Part Editor window. If you do not want to use the snap feature, click the **Snap-to-Grid** icon in the main toolbar to create off-grid graphics. This is also helpful when adding or relocating text and properties. Do **NOT** turn off Snap-to-Grid when placing pins on the part. Pins **MUST** fall on a 100-mil grid.

Step 3: Adding Pins



Pins	Length	Illegal Characters
pin number	30	! : " ' , ~ * <> Space
pin name	255	Same as above

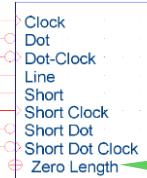


- 1 Adding a New Part to a Library
- 2 Adding Graphics
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The pin name is used in the simulation, and the pin number is used by the netlist.

Pins can only be placed on the boundary box edges and must be placed on a 100-mil grid.

Choose a pin shape – this is what they look like on a symbol.



Choose **Place – Pin** or click the Place Pin icon from the Draw Electrical toolbar.

Pins can only be placed on the boundary box edges and must be placed on a 100-mil grid. Pins cannot be added to the corner of the part boundary box. If you need to add a pin on a corner, then enlarge the boundary box before adding the pin, and shrink the box, so the pin is on the corner.

Name – Specifies the pin name. If the name ends with a digit (0 – 9), each pin is incremented by one each time you place a pin. You can create a pin name with an overbar by adding a backslash (\) after every letter in the pin name. You get errors if you create duplicate pin names on the same symbol. The only duplicate pin names on a symbol should be power pins (see *Adding Power Pins*). By default, all pin names (except power) are visible. Pin names are used in the simulation.

Number – Specifies the pin number. The pin number can be alphanumeric. If it ends in a number, it is incremented by one after each pin is placed. If the Pin Number field is left blank, no error occurs. During annotation, no pin number data is added to the schematic. A pin number is required by the Allegro® PCB Editor netlist. Capture will flag duplicate pin number assignments on the same section only. For example, in a multi-section part, you can map a shared enable pin to the same pin number as long as it is in a different section. By default, all pin numbers (except power) are visible. Pin number text cannot be moved except in the Edit Part command at the schematic page level.

Width – Specifies whether the pin connects to a single or multi-bit bus wire. Bus pins cannot be used directly as netlisting pins. Their main purpose is to make it possible to use non-primitive parts more easily by connecting large numbers of signals to a child schematic folder.

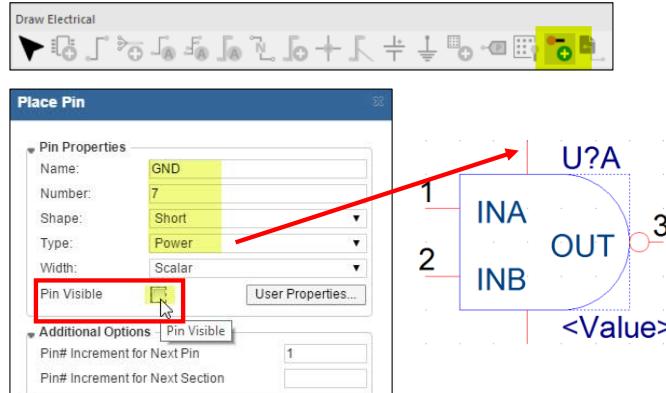
Shape – Select the pin shape from the list of nine pin shapes.

Type – Select the pin type from the list of eight-pin types: 3 State, Bidirectional, Input, Open Collector, Open Emitter, Output, Passive, and Power. Be careful to enter the correct pin type, as this will affect design rule checking and simulation. If a part has no voltage pins (for example, a discrete resistor), then its pins should be defined as Passive.

Pin Visible – Specifies whether the pin is visible on the schematic page. All pins (except power pins) are visible (the Pin Visible toggle is grayed out). Power pins are invisible by default but can be visible if you choose. (The Pin Visible toggle is accessible for power pins only.)

User properties dialog box – Adds and edits the pin properties.

Step 4: Adding Power Pins



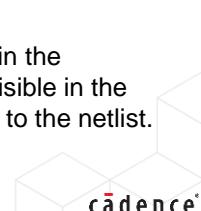
This step is optional for discrete parts.

If the Pin Type is Power, no duplicate pin errors will occur when you save the part.

- 1 Adding a New Part to a Library
- 2 Adding Graphics
- 3 Adding Pins
- 4 Adding Power Pins
- 5 Editing a Pin
- 6 Defining the Physical Packaging
- 7 Adding User Properties

- The name of the power pin is used as the name of the power net.
- By default, power pins are invisible in the schematic. When a power pin is invisible in the schematic, it is automatically added to the netlist.

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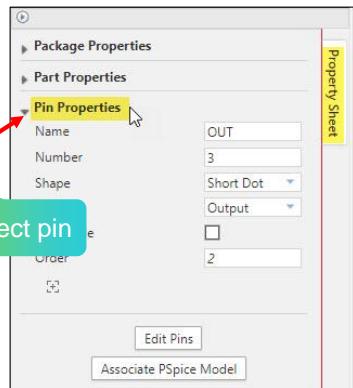
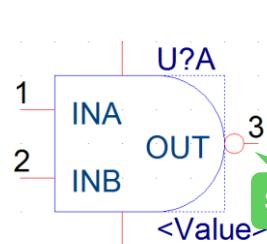
To add a power pin, set the *Type* field to **Power**. The name of the power pin is used as the name of the power net.

When you set the pin type to Power, the *Pin Visible* field is activated (this field is grayed out for all other pin types). By default, the **Pin Visible** option is unchecked, which means power pins are invisible in the schematic. When a power pin is invisible in the schematic, it is automatically added to the netlist.

To override the default signal defined for a power pin, edit the part properties in the design and make the power pin visible. Then, connect it to an appropriate voltage symbol in the schematic. If you check the **Pin Visible** option when building the part, then the power pin is always visible in the schematic and will always need to be explicitly tied to a voltage symbol or wire in order to appear in the netlist.

It is common to add power pins using the *Zero Length* pin shape. Multiple power pins tied to the same voltage should be added with duplicate pin names (for example, pin name +5V) because the pin name is used as the net name. As long as the Pin Type is Power, no duplicate pin errors will occur when you save the part.

Step 5: Editing a Pin



- | | |
|---|---------------------------------|
| 1 | Adding a New Part to a Library |
| 2 | Adding Graphics |
| 3 | Adding Pins |
| 4 | Adding Power Pins |
| 5 | Editing a Pin |
| 6 | Defining the Physical Packaging |
| 7 | Adding User Properties |

Click on a pin and use the Pin Properties section in the right pane to edit the pin properties.



Use the Pin Properties section in the right pane to edit the pin properties.

Step 6: Defining the Physical Packaging for the Part

Single-section

Multi-section

Use the Package Properties section of the Property Sheet to manage package properties.

Choose **Edit – Edit Pins** to edit the pin mapping information.

Normal View: Pin Name	Section: A Pin Num.	Section: B Pin Num.	Section: C Pin Num.	Section: D Pin Num.	Section: D Pin Ignore	Order	Pin Group
INA	1	4	9	12	No	0	1
INB	2	5	10	13	No	1	1
OUT	3	6	8	11	No	2	
GND	7	7	7	7	No	3	
VCC	14	14	14	14	No	4	

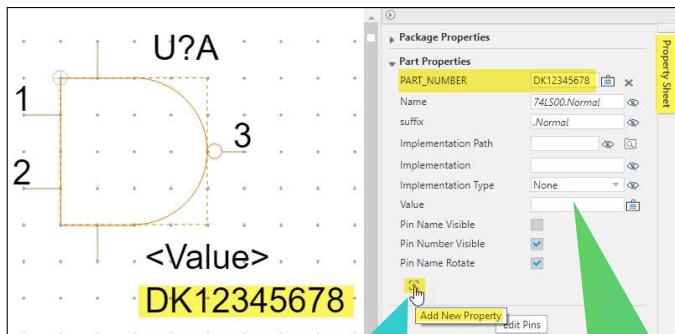
1 Adding a New Part to a Library
2 Adding Graphics
3 Adding Pins
4 Adding Power Pins
5 Editing a Pin
6 Defining the Physical Packaging
7 Adding User Properties

A package is a grouping of one or more circuit elements.

If a symbol represents the entire package, the part is said to be a *single-section*. If the symbol represents only a portion of the physical package, the part is called *multi-section* (other terms are multi-gate or multi-slot).

A part has both logical and packaging-related characteristics. For example, the symbol defines the part graphics and pin names. However, packaging information is required to define the number of times the symbol fits into a package, and the packaging data includes the logical-to-physical pin mapping and swapping information. This packaging data is used to annotate the part in the schematic with pin numbers, assign a reference designator, and create entries for the part in the schematic netlist.

Step 7: Adding User Properties



Use the Part Properties section in the Property Sheet to add a user property.

Leave the Value field blank when adding a property placeholder to control property position and visibility at the library level.

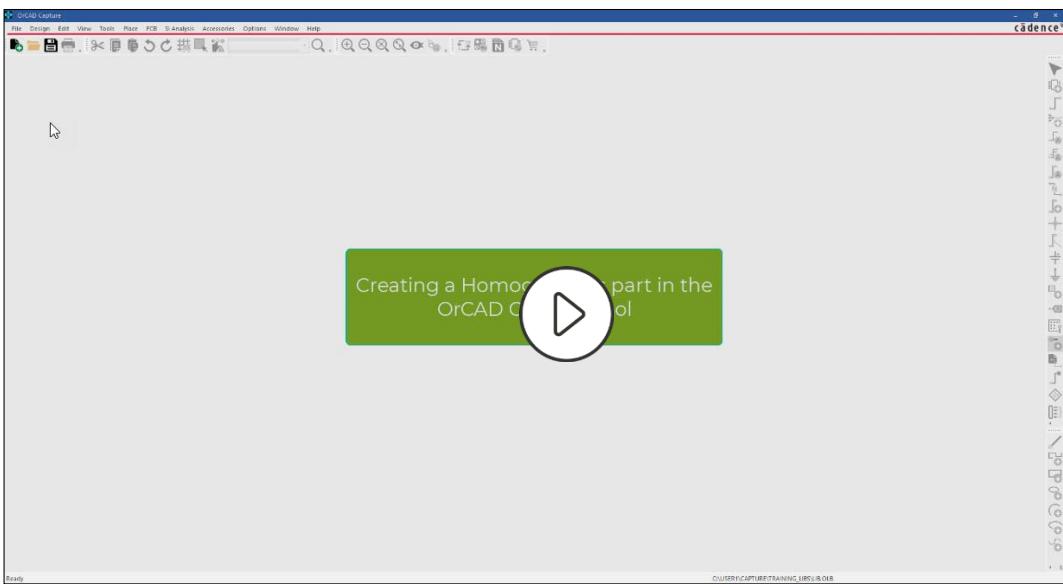
- 1 Adding a New Part to a Library
- 2 Adding Graphics
- 3 Adding Pins
- 4 Adding Power Pins
- 5 Editing a Pin
- 6 Defining the Physical Packaging
- 7 Adding User Properties



Use the Part Properties section in the right pane to add a user property.

Leave the Value field blank to add a property *placeholder* that controls positioning and visibility at the library level.

Demo: Creating a Homogeneous Part



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Video Play Time: 8.09 minutes

Click the Play button to start the video.

What Is a Heterogeneous Part?



A heterogeneous part is a part whose physical package contains two or more unique schematic symbols.

Heterogeneous parts:

- Have a minimum of two parts per package
- Have gates that do not look alike
- Can have different pin counts in each gate



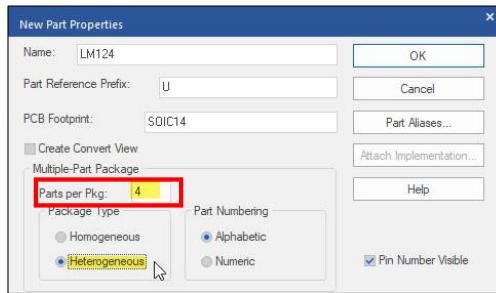
This page does not contain notes.

Example: Heterogeneous Part

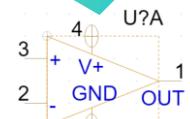
The part in the accompanying illustration shows two unique graphical symbols; one gate with Power and GND pins and the other gate without.

Each part graphic represents a different portion of the package.

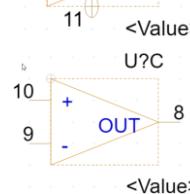
For example, an OPAMP can contain four gates, with just one of the gates showing the Power and Ground pins for the package. You would define this heterogeneous part as having four parts per package.



This gate includes the voltage pins.



This gate does not have voltage pins.

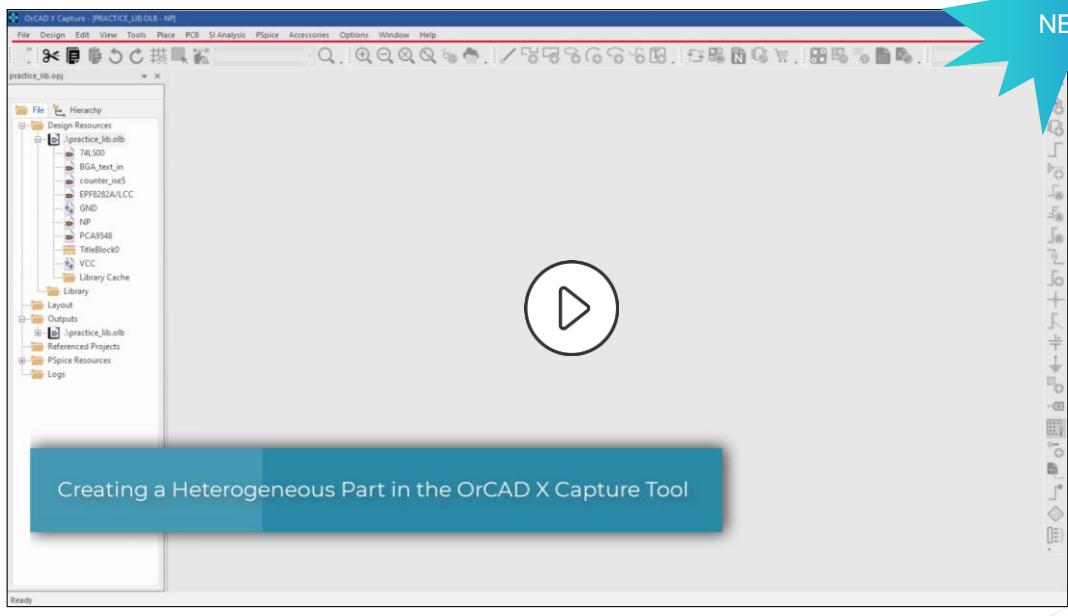


<Value>

<

Demo: Creating a Heterogeneous Part

NEW



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Video Play Time: 4.52 minutes

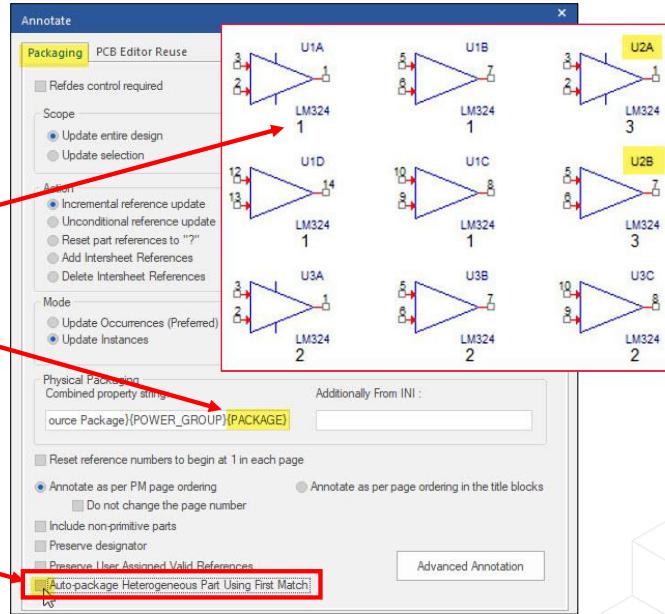
Click the Play button to start the video.

Annotating Heterogeneous Parts



When a heterogeneous part is used in a design, you can use a grouping property to control how these part symbols go together in a package.

- **Attach** a grouping property named PACKAGE to heterogeneous parts in the design to control package creation.
- **Choose Tools – Annotate** and add the PACKAGE property to the Combined property string field when annotating the schematic.
- Annotation errors will occur if no grouping property is added or if grouping is invalid.
- Optionally **select the Auto-package Heterogeneous Part Using First Match** option as an alternative to the grouping property method.



Auto-Package Heterogeneous Part Using First Match – Select this option to annotate heterogeneous split parts without specifying any grouping property. With this option enabled, Capture decides the grouping of heterogeneous split parts using the first match option.

Parts Versus Symbols

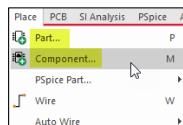


A *part* corresponds to a device on the PC board.

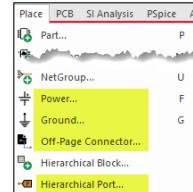


A *symbol* carries information about the design, but it does not represent a device on the PC board.

- ICs, Discretes, Connectors, etc.
- A *part* is added to the schematic using the **Place – Part** command.
- A *part* is also added to the schematic from external content partners (SamacSys, Ultra librarian, SanpEDA) using the **Place – Component** command.



- Power and ground symbols
- Off-page connectors
- Hierarchical ports
- Title blocks
- A *symbol* is added to the schematic using the **Place – click on respective** commands.



The OrCAD X Capture system differentiates between library *parts* and library *symbols*.



OrCAD X Capture lets you create special symbols that carry information about the design but do not represent physical parts on the PCB.

For example, you can create your own power symbols or title block symbols. You can create these symbols from scratch or copy existing symbols and modify them for use in your libraries.

The Capture Symbol Library



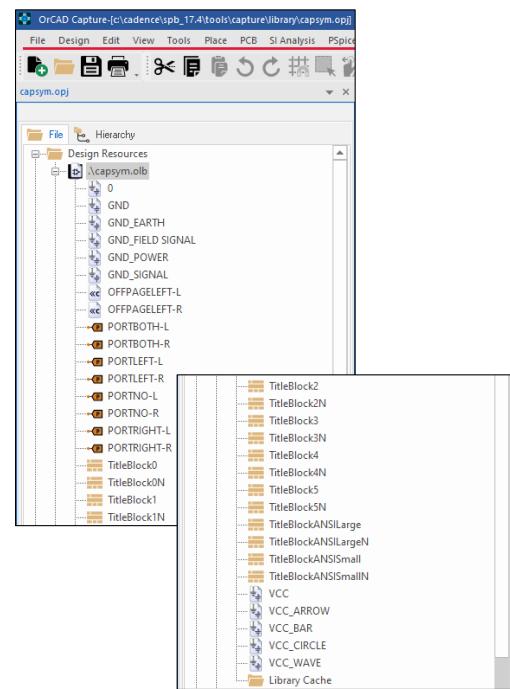
Capture comes with a library of symbols.

The CAPSYM library is located in your Cadence software installation hierarchy.

For example –

`%CDSROOT%\tools\capture\library`

It's common to copy a Cadence-supplied title block or voltage symbol to your company library and modify it.



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Cadence provides many symbols in the *CAPSYM.OLB* library. This library is located in your software installation hierarchy (for example, `$CDSROOT\tools\capture\library`).

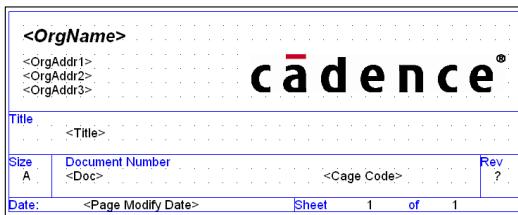
Creating Custom Symbols



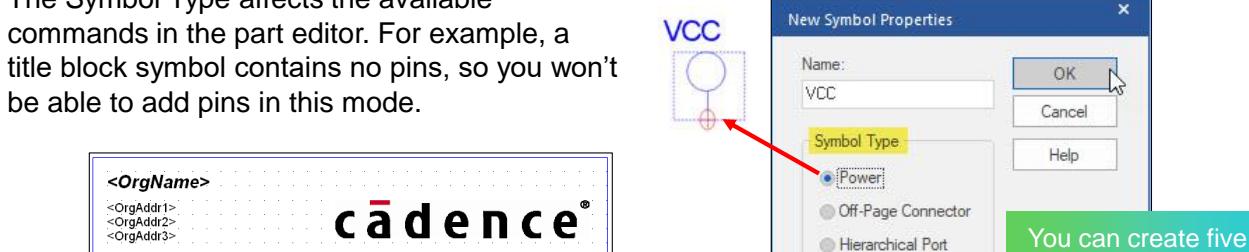
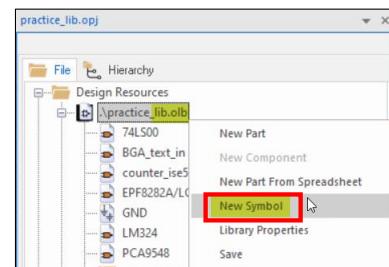
Choose **Design – New Symbol** to access the New Symbol Properties menu.

You can create your own symbols.

The Symbol Type affects the available commands in the part editor. For example, a title block symbol contains no pins, so you won't be able to add pins in this mode.



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You can create five types of symbols.

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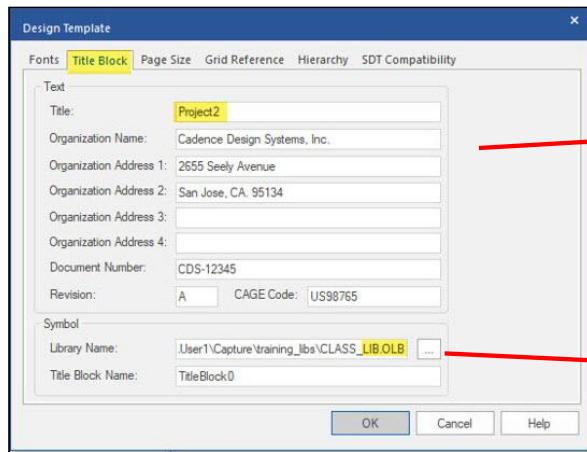
When you set the Symbol Type to Power, Off-Page Connector, or Hierarchical Port, the part editor automatically gives you a single pin as a connection point. The Symbol Type affects the available commands in the part editor. For example, a title block symbol contains no pins, so you won't be able to add pins in this mode.

- **Power** – Includes all power and ground symbols.
- **Off-Page Connectors** – Links the nets from Page-to-page only.
- **Hierarchical Ports** – Connects the net through the levels of a hierarchical design.
- **Title Blocks** – Contains information about the design on each page, including page numbering, title, revision, page size, etc.
- **Pin Shape** – You can create your own pin shapes in Capture. You can then use these pin shapes on new or existing parts. To place a user-defined pin shape on a part, the pin shape must be available in the CAPSYM.OLB library in the `$CDSROOT\tools\capture\library\capsym.olb`. If you create your pin shape in a user-defined library, you need to copy that symbol into the CAPSYM.OLB library. Capture reads the user-defined pin shapes from this location and populates the pin shape names in the *Shape* cell of the *Pin Properties* dialog box in Part Editor. When the part is placed on the design and the pin shapes are found in the CAPSYM.OLB library, the pin shapes are cached to the design cache. If a pin shape is not available in the CAPSYM.OLB library, the default pin shape, which is a line, will display on the part.

What Is a Title Block Symbol?

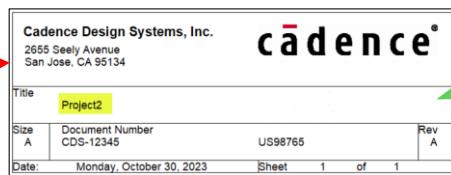


A title block symbol is used to specify important information about the design document.

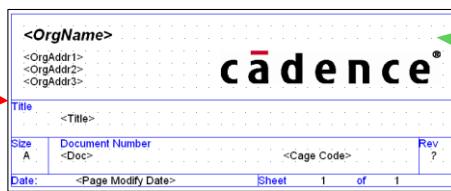


A title block symbol contains **graphics, text, and a company logo**.

A title block symbol also contains reserved property names. Some of these properties define your **company name and address** and can get their values from the design template, while other properties obtain their values directly from the design database.

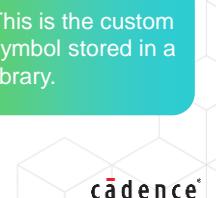


This is how the title block symbol looks when used in a design.



This is the custom symbol stored in a library.

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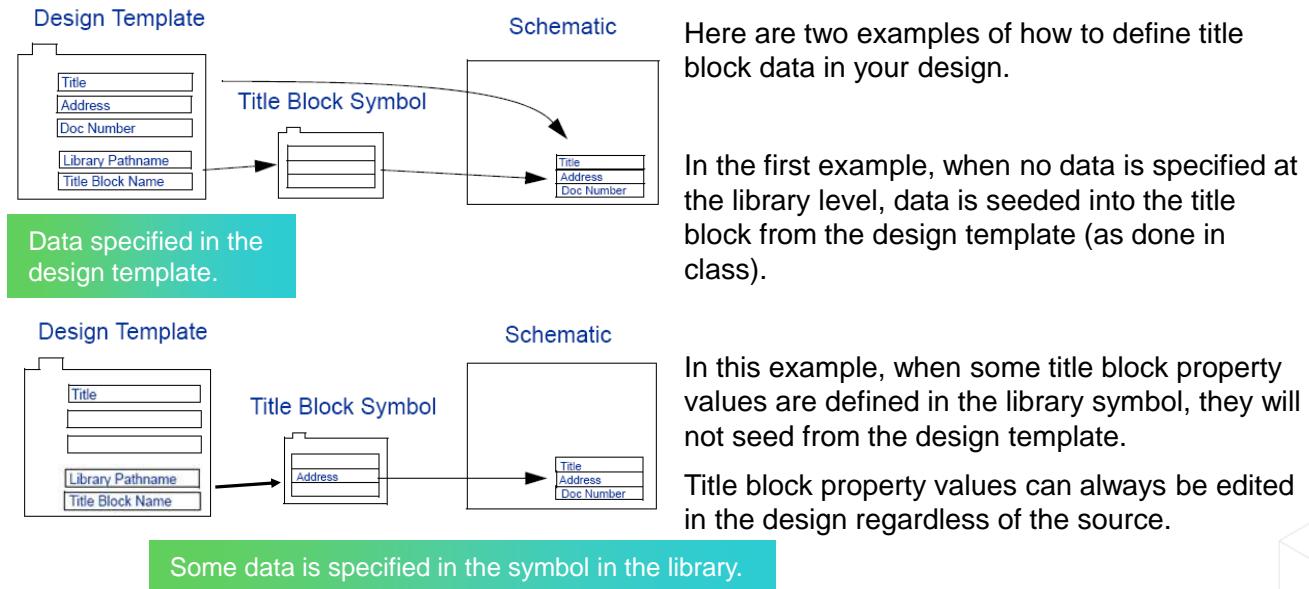


The title block symbol is composed of graphics, text, and a company logo.

The title block symbol also contains reserved property names. Some of these properties define your company name and address and can get their values from the design template, while other properties obtain their values directly from the design database. If you want a property to get its value from the design, then it must have a null value in the library.

Choose **Place – Picture** to add a logo to the company title block symbol (at the library level). This command accepts *.bmp*, *.tif*, *.jpg*, *.gif*, and *.png* files.

Various Ways to Define Title Block Data



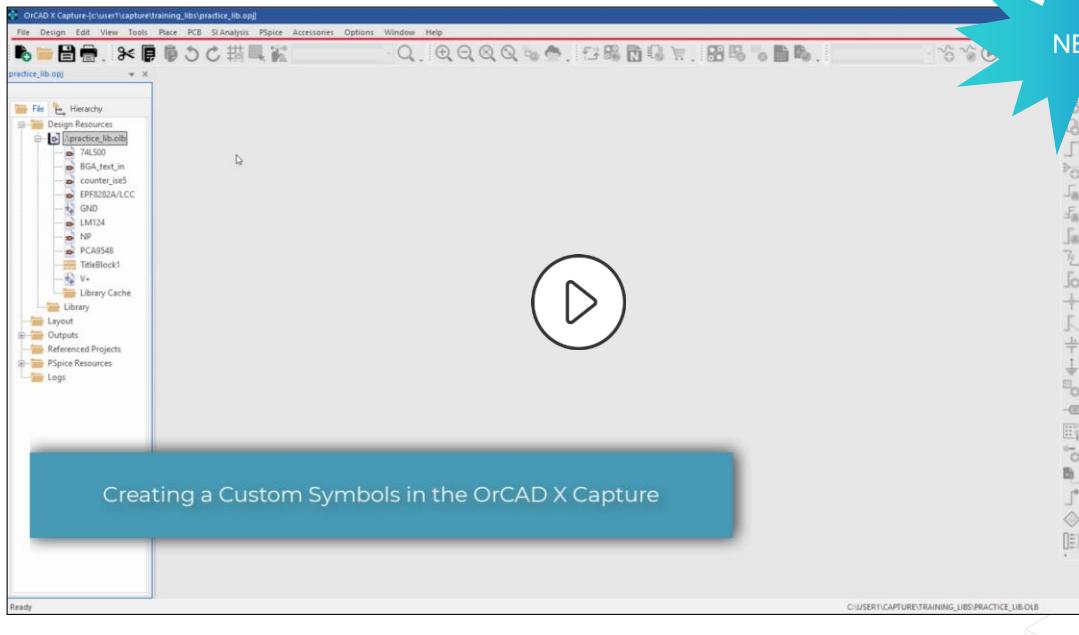
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If the title block property values are defined in the library symbol, they will not seed from the design template. Title block property values can be edited in the design regardless of where the source value originates.

You can also use the **Place – Title Block** command to manually add a title block symbol to a schematic page.

Demo: Creating a Custom Symbols



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C:\USERT\CAPTURE\TRAINING_LIB\PRACTICE_LIB.DLB

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Video Play Time: 3.52 minutes

Click the Play button to start the video.

Creating a Part Using a Spreadsheet Interface



Use the New Part From Spreadsheet form to enter data for a new part into a spreadsheet-like interface.

In the Project Manager, right-click on the library name and choose the **New Part From Spreadsheet** command to define the following:

- Number of sections in the package
- Pin name and number
- Pin type and shape
- Pin section

This tool does not import a spreadsheet file. However, you can copy and paste from a spreadsheet into this spreadsheet-like interface.

The screenshot shows the Cadence Project Manager interface. In the Project Manager window, a context menu is open over the 'practice.lib.olb' library node. The 'New Part From Spreadsheet' option is highlighted with a red arrow. Below the Project Manager is the 'New Part Creation Spreadsheet' dialog box. This dialog has fields for 'Part Name: PCA9548', 'No. of Sections: 3', and 'Part Ref Prefix: U'. It also has a 'Pin Grouping' section with radio buttons for 'Numeric' and 'Alphabetic'. The main area is a table with columns: Number, Name, Type, Pin Visibility, Shape, PinGroup, Position, and Section. The table contains 24 rows of pin definitions. At the bottom of the dialog are buttons for 'Add Pins...', 'Delete Pins...', 'Save', 'Cancel', and 'Help'. A green callout bubble with the text 'Click here to create a part.' points to the 'Save' button.

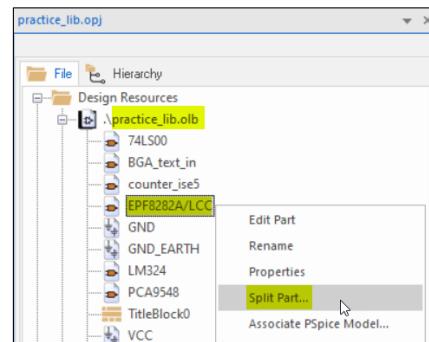
Number	Name	Type	Pin Visibility	Shape	PinGroup	Position	Section
1	A0	Input	<input checked="" type="checkbox"/>	Short		Left	A
2	A1	Input	<input checked="" type="checkbox"/>	Short		Left	A
3	RESET	Input	<input checked="" type="checkbox"/>	Short		Left	A
4	SD0	Output	<input checked="" type="checkbox"/>	Short		Right	A
5	SD0	Output	<input checked="" type="checkbox"/>	Short		Right	A
6	SD1	Output	<input checked="" type="checkbox"/>	Short		Right	A
7	SC1	Output	<input checked="" type="checkbox"/>	Short		Right	A
8	SD2	Output	<input checked="" type="checkbox"/>	Short		Right	A
9	SC2	Output	<input checked="" type="checkbox"/>	Short Clock		Right	A
10	SD3	Output	<input checked="" type="checkbox"/>	Short		Right	A
11	SC3	Output	<input checked="" type="checkbox"/>	Short Dot Cl		Right	A
12	GND	Power	<input type="checkbox"/>	Short		Bottom	C
13	SD4	Output	<input checked="" type="checkbox"/>	Short		Right	B
14	SC4	Output	<input checked="" type="checkbox"/>	Short Clock		Right	B
15	SD5	Output	<input checked="" type="checkbox"/>	Short		Right	B
16	SC5	Output	<input checked="" type="checkbox"/>	Short Dot Cl		Right	B
17	SD6	Output	<input checked="" type="checkbox"/>	Short		Right	B
18	SC6	Output	<input checked="" type="checkbox"/>	Short Clock		Right	B
19	SD7	Output	<input checked="" type="checkbox"/>	Short		Right	B
20	SC7	Output	<input checked="" type="checkbox"/>	Short Dot Cl		Right	B
21	A2	Input	<input checked="" type="checkbox"/>	Short		Left	B
22	SCL	Input	<input checked="" type="checkbox"/>	Short Clock		Left	B
23	SDA	Input	<input checked="" type="checkbox"/>	Short		Left	B
24	VDD	Power	<input type="checkbox"/>	Short		Top	C

Use the **New Part From Spreadsheet** command to enter data for a new part into a spreadsheet-like interface. This tool does not import a spreadsheet file. However, you can copy and paste from a spreadsheet into this spreadsheet-like interface. Be careful to paste the correct columns of data from the spreadsheet into the corresponding columns in the New Part Creation Spreadsheet window.

If no pin position is specified, the default position is Left edge, regardless of pin type.

Splitting an Existing Part

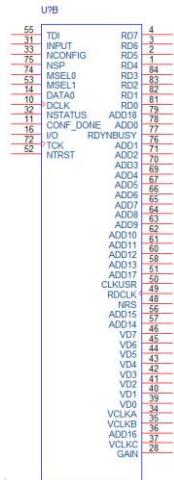
The Split Part command lets you split an existing part into multiple sections.



In the Project Manager, right-click on the part and choose **Split Part** to open the Split Part Section Input Spreadsheet form.

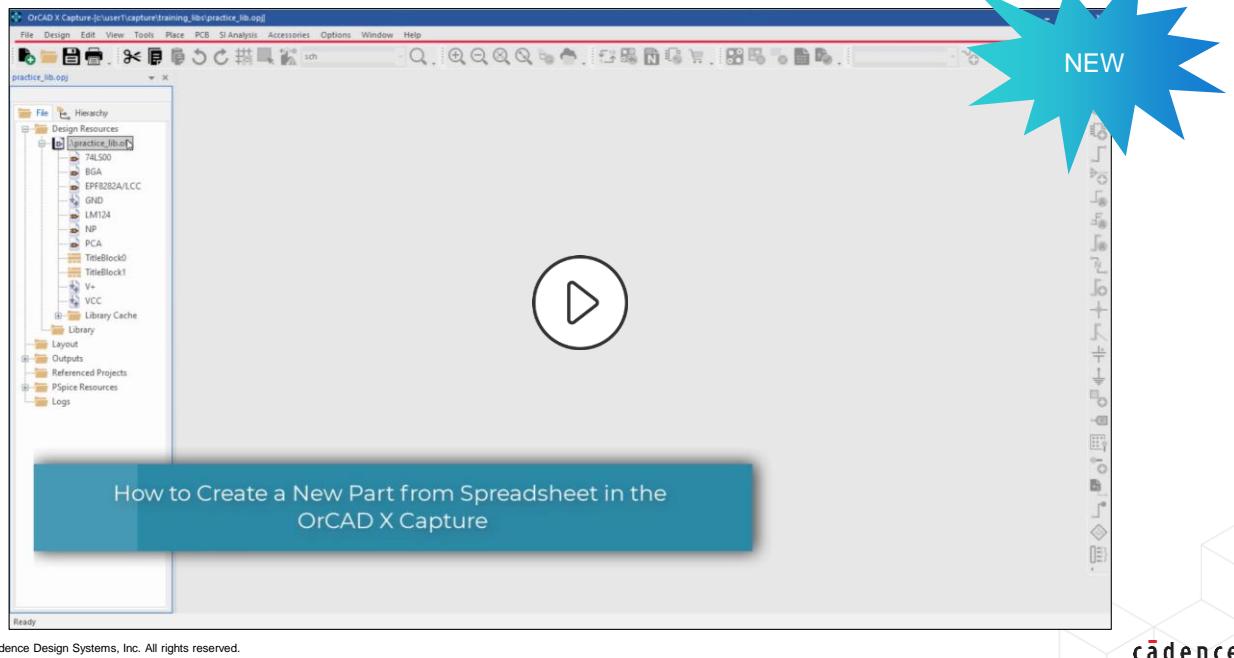
	Number	Name	Type	Pin Visibility	Shape	PinGroup	Position	Section
36	10	DCLK	Input	<input checked="" type="checkbox"/>	Clock		Left	A
37	28	GAIN	Output	<input checked="" type="checkbox"/>	Line		Right	A
38	5	GND	Power	<input checked="" type="checkbox"/>	Short		Bottom	C
39	26	GND	Power	<input checked="" type="checkbox"/>	Short		Bottom	C
40	47	GND	Power	<input checked="" type="checkbox"/>	Short		Bottom	C
41	68	GND	Power	<input checked="" type="checkbox"/>	Short		Bottom	C
42	16	VO	Input	<input checked="" type="checkbox"/>	Line		Left	A
43	31	INPUT	Input	<input checked="" type="checkbox"/>	Line		Left	B
44	73	INPUTA	Input	<input checked="" type="checkbox"/>	Line		Left	A
45	54	INPUTB	Input	<input checked="" type="checkbox"/>	Line		Left	B
46	12	INPUTC	Input	<input checked="" type="checkbox"/>	Line		Left	C

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The **Split Part** command lets you split an existing part into multiple sections. Set the total number of sections to split the part into and the reference designator numbering format for the gates, then assign pins to sections. A split part is a heterogeneous part.

Demo: Creating a New Part from Spreadsheet



Video Play Time: **3.11** minutes

Click the Play button to start the video.

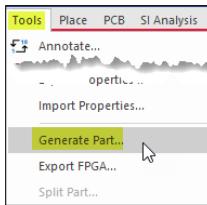
Generating a Part from Imported Data



Choose **Tools – Generate Part** to import various types of data to create library parts.

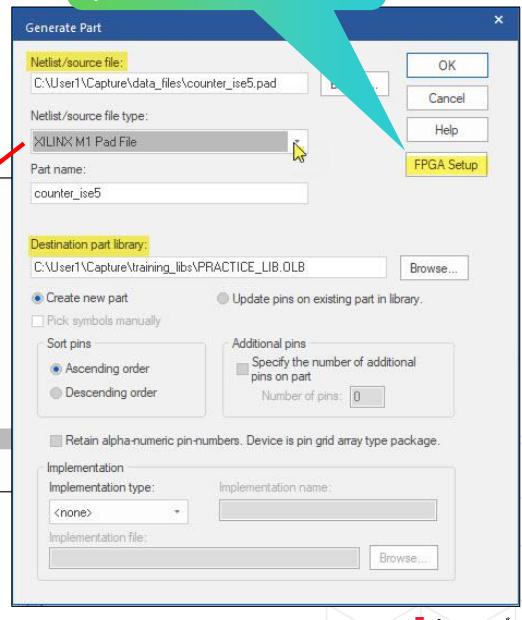
Capture can import a variety of vendor pin report formats to create library parts.

You can create library parts by importing Verilog, VHDL, or PSpice models.



You can also create a block symbol from a Capture schematic design.

Use the FPGA Setup button to specify settings for FPGA symbols.



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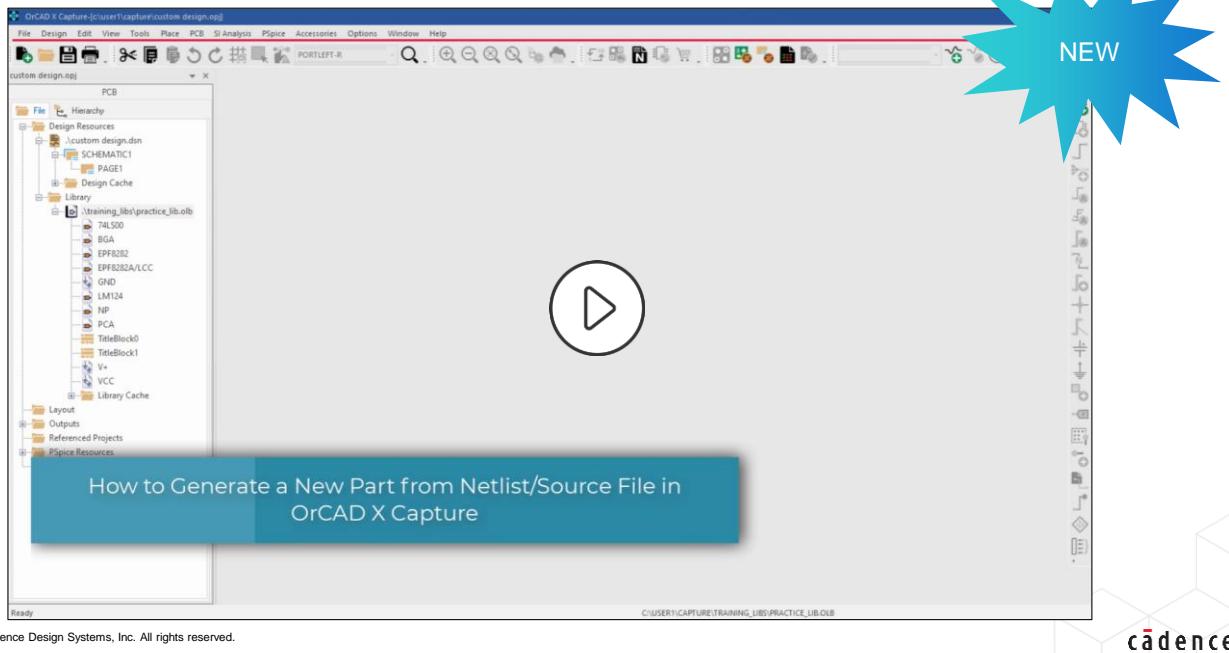
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Capture reads a variety of PLD vendor pin reports to create library parts for the Capture schematic system. Most PLD vendor pin reports describe the pin number, signal name, and direction (or mode) of a package pin programmed by the place-and-route process. Pins are sorted alphabetically by name, with input type pins located on the left-hand side and output or bidirectional pins on the right-hand side. The Generate Part program can update the pin numbers of an existing part, which lets you incorporate engineering changes from a programmable logic project.

Use the FPGA Setup button to specify settings for FPGA symbols, FPGA pins, FPGA pin swapping, and pin shape or pin direction.

You can also create library parts by importing Verilog, VHDL, or PSpice® models or create a block symbol from a Capture schematic design.

Demo: Generating a New Part from Netlist/Source File



Video Play Time: **4.04** minutes

Click the Play button to start the video.



Labs

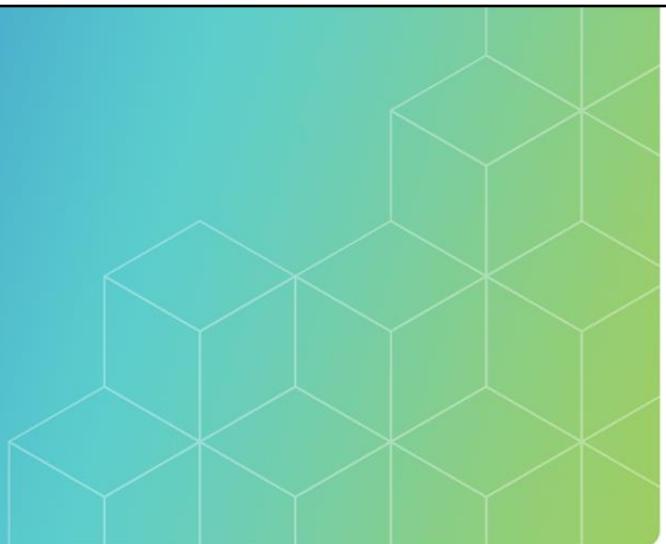
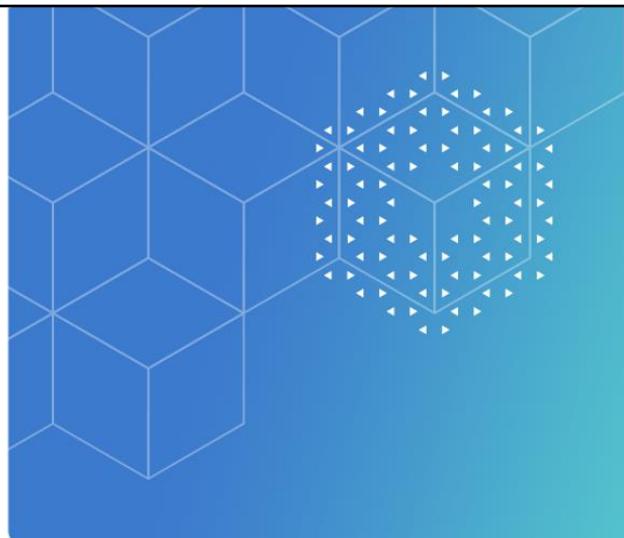
- Lab 4-1 Opening and Viewing an Existing Library
- Lab 4-2 Creating a New PRACTICE_LIB Library
- Lab 4-3 Copying and Renaming Parts and Symbols
- Lab 4-4 Creating a Homogeneous Part
- Lab 4-5 Creating a Heterogeneous Part
- Lab 4-6 Creating a Power Symbol
- Lab 4-7 Creating Parts Using a Spreadsheet Interface
- Lab 4-8 Splitting an Existing Part
- Lab 4-9 Generating Parts from Imported Data

See the Lab Appendix for additional topics

- Testing the LM324 Part
- Creating a Custom Title Block



You will now have the opportunity to perform some self-paced labs to reinforce the ideas presented in this module.



Module 5

Building a Simple Schematic

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Welcome to Module 5: Building a Simple Schematic

Module Objectives

In this module, you

- Create a new project
- Select and place schematic library parts
- Add wires and net names
- Assign reference designators
- Check the design for errors

Introduction to OrCAD X Capture

Setting Up Your Environment

Working with Libraries

Building a Simple Schematic

Building a Multi-Sheet Schematic

Editing Part Properties

Building a Hierarchical Design

This is where you are in the course flow.

Creating a New Project

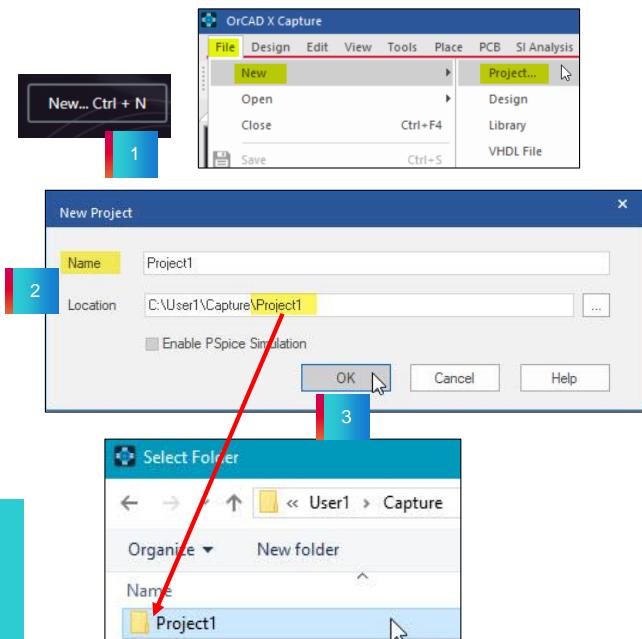


The Create New Project functionality requires you to provide only the bare minimum data to create a new project in the OrCAD® X Capture tool.

To create a new project:

1. In the OrCAD X Capture Start Page, click on **New** or use the shortcut key **Ctrl+N** or choose **File – New** and click on **Project**.
2. Enter the Project Name and Location.
3. Click **OK** to create a project.

Note: Do not use spaces in directory names, library names, design names, net names, pin names, pin numbering, footprint names, or property names and values.

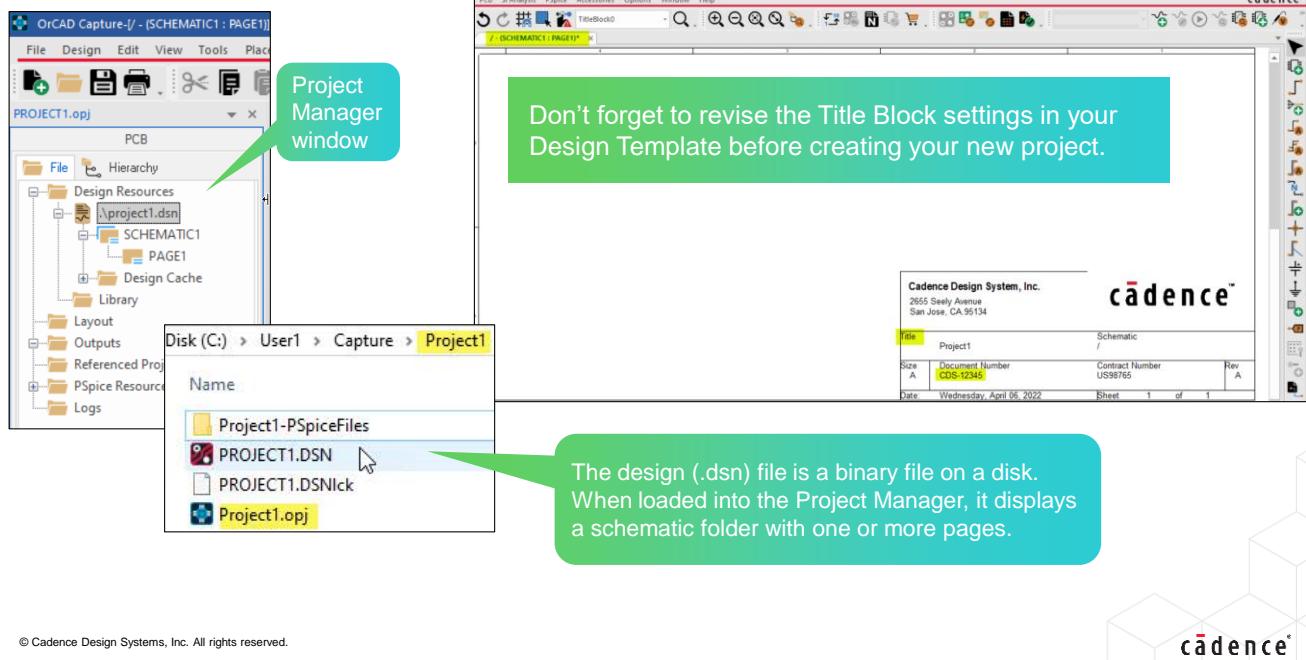


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This page does not contain notes.

Resulting New Project and System Files



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After the new project is created, Capture displays the Project Manager window. A default schematic folder named SCHEMATIC1 is added to the design file. Capture also opens a default schematic page named PAGE1. You can rename the schematic folder and page name.

The design (.dsn) file is a binary file on a disk. When loaded into the Project Manager, it displays a schematic folder with one or more pages.

Don't forget to revise the Title Block settings in your Design Template before creating your new project.

To save the project file, choose **File – Save**.

To close the project, choose **File – Exit**.

Placing Parts



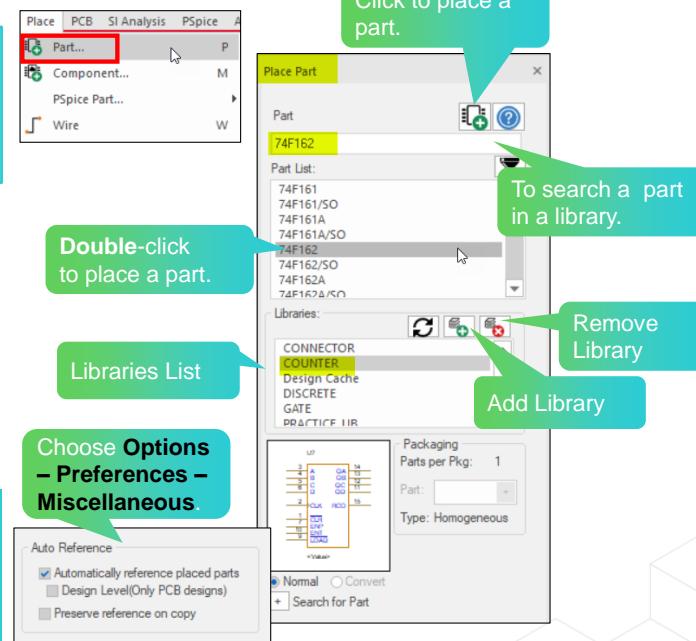
Choose Place – Part.



Or press the P shortcut key.

- Use the Place Part window to select a part from a Capture library.
- Use the Libraries field to add any libraries you need.
- Libraries added to the Place Part window are also added to your *Capture.ini* file in the `%HOME%\cdssetup\OrCAD_Capture` directory.

System Cadence provides libraries for use with Capture. `<install_dir>\tools\capture\library` – where `<install_dir>` is the location of the Cadence software PSpice libraries – `<install_dir>\tools\capture\library\pspice`.



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Before you can add a part to your design, you need access to the library it is in. If this library was not configured during the initial project setup, you can press the **Add Library** button and add it to your library setup. Once you've added the new library, select it in the **Libraries List** to see the parts in the Part List.

When a library is added using the Place Part window, this setup is stored in the *Capture.ini* file in the `$HOME\cdssetup\OrCAD_Capture` directory. Libraries in the *Capture.ini* file automatically load into the Place Parts window during subsequent Capture sessions. Click the **Remove Library** button to delete the library name from the Place Part window and the *Capture.ini* file.

You can scroll through the Part List or type the name of a part in the Part field. As you enter each character, the data is matched against the parts in the selected library, and the Part List automatically scrolls to show the matches. When more than one library is selected in the Libraries list, the Part List displays the part and library name for each part, such as COUNTER/74F162. When you choose a part from the Part List, a graphic of the part IS displayed in the Place Part window.

Cadence provides libraries for use with Capture. These libraries are located at:

`<install_dir>\tools\capture\library`, where `<install_dir>` is the location of the Cadence software. If you're planning to run a PSpice simulation, you must use parts from the PSpice libraries located at `<install_dir>\tools\capture\library\pspice`.

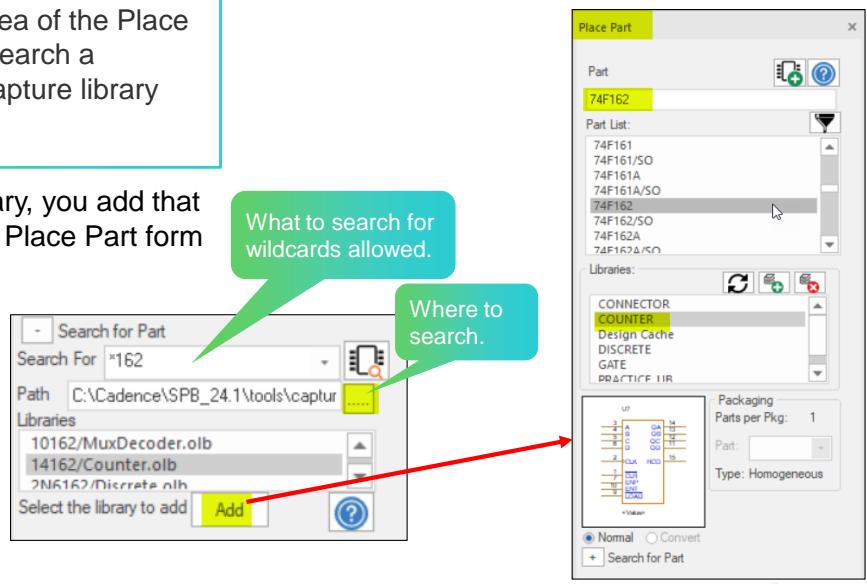
When placing parts in the design, you can have the system automatically assign a reference designator for you. Choose **Options – Preferences – Miscellaneous** to set this user preference.

Searching for a Part

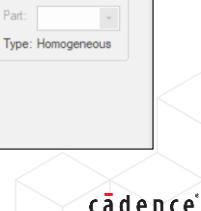


The Search for Part area of the Place Part window lets you search a directory containing Capture library (.olb) files.

When the part is found in a library, you add that library to the Libraries list in the Place Part form and to the *Capture.ini* file.



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You can use wildcard characters (*) and (?) in the Search For field. Use the Path field to define the directory containing the Capture library file(s).

When a part is found, its library is added to the Place Part window, and you are ready to add the part to the design.

What Is a Single-Section Versus a Multi-Section Part?

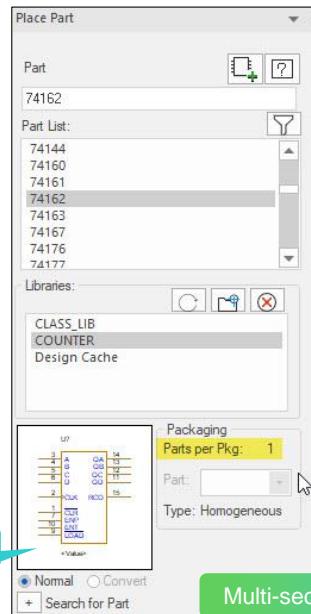


A single-section part is a part that represents the entire physical package.

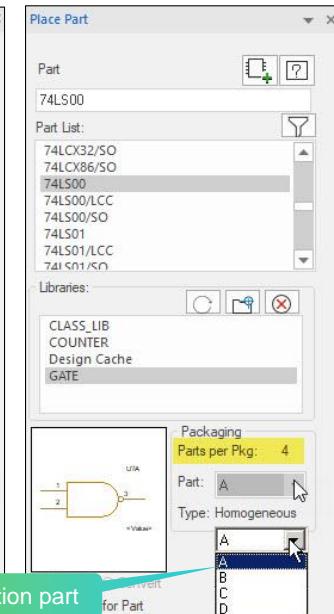
A multi-section part is a part that represents only a portion of the physical package.

During part placement, use the Packaging section of the Place Part form to select a preferred section of the package. This is used to add the pin numbers to the part.

Single-section part



Multi-section part



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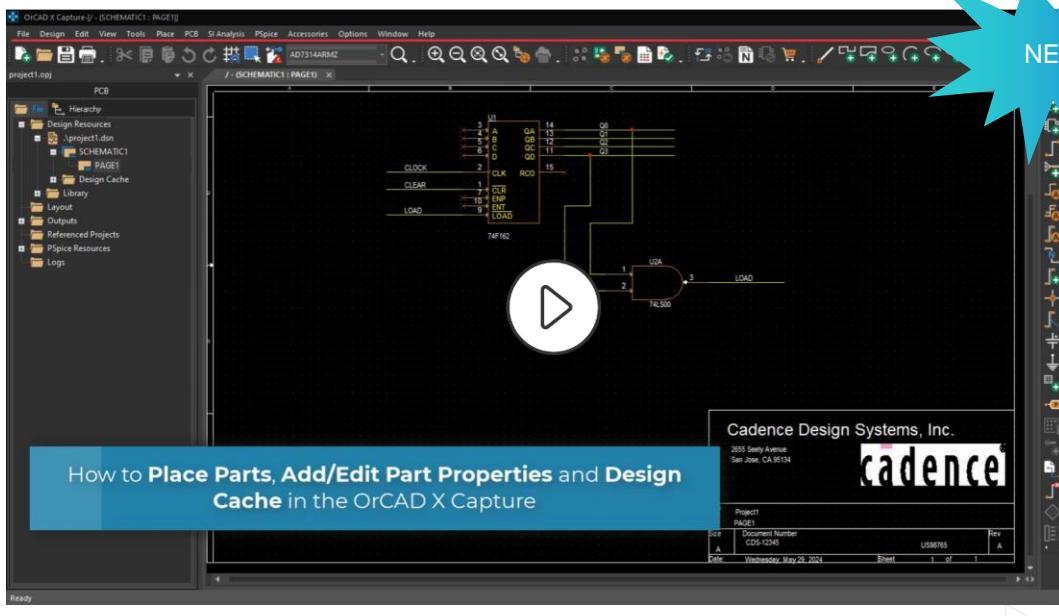
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The Packaging section of the Place Part form reflects the number of sections (or slots) in the physical package.

For a multi-section (gate-level) part:

- If the Packaging section of the Place Part form is not used, a temporary part reference and pinouts will default to section A (repetitively).
- If the Packaging section of the Place Part form is used, then a temporary part reference and pinouts will coincide with the selected section. Pinouts always match the section.
- If the part is homogeneous, you can manually change the section once the part is placed (for example, from U?A to U?B). This causes the pinouts to change automatically. You cannot manually assign a section that does not exist.
- If the part is heterogeneous, all you can do is change the question mark (?) to show grouping into a specific package. The pinout is locked at placement based on the section you selected in the Place Part form.
- When you manually edit a multi-section part reference, Capture does not let you remove the section indicator.
- When you use the Packaging section of the Place Part form to select a specific section, the Annotate program does not maintain the selected section (even in Incremental mode) unless you also supply a part reference.

Demo: Place Parts, Add/Edit Part Properties and Design Cache



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Video Play Time: **4.31** minutes

Click the Play button to start the video.

Placing Parts from External Content Providers



Choose **Place – Component**.

Or press the **M** shortcut key.



You can add parts from Cadence-supplied libraries (**PSpice**) or download parts directly from Cadence library content partners (**SamacSys**, **Ultra Librarian**, **SnapMagic**).

Use the free-text search field to find a part.

Cadence-supplied library
<install_dir>\tools\capture
library\pspice

Cadence library content
partners

To place the part, right-click on the part row and click on **Place**.

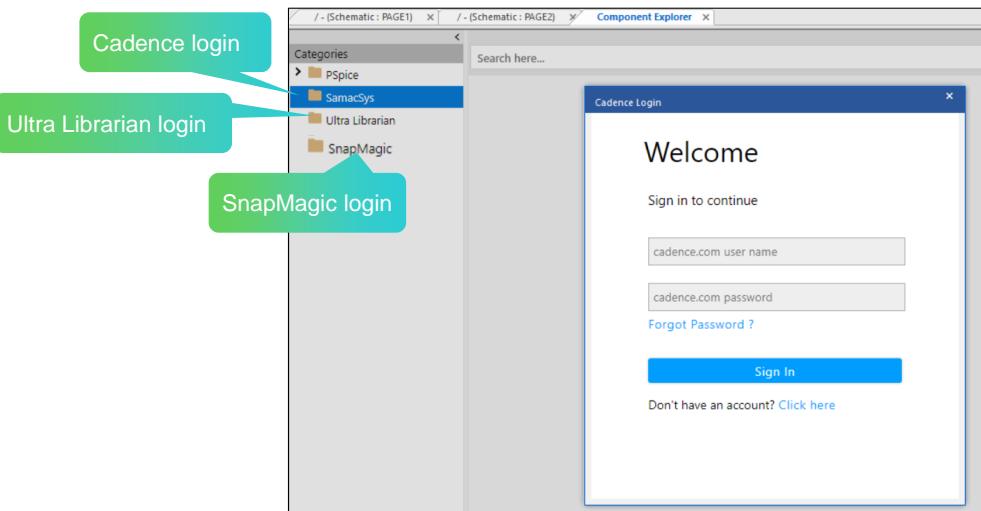
Each part row has icons to indicate if a symbol, PCB footprint, and 3D model are available.

Click here to place the part.

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Choose **Place – Component** or press the **M** shortcut key to open the Component Explorer window. By default, you have access to the Cadence-supplied libraries. You can add parts or download parts directly from Cadence library content partners (SamacSys, Ultra Librarian, SnapMagic). Use the free-text search field to find a part. You can search through and download thousands of parts, symbols, footprints, and 3D images.

Placing Parts from External Content Providers (continued)



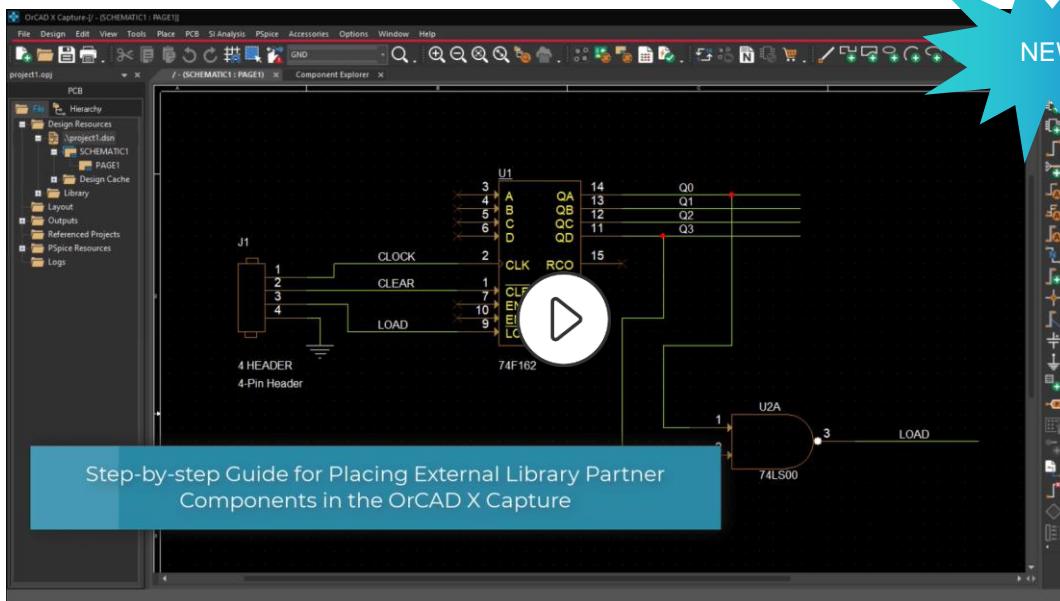
Placed part is downloaded as a zip file and stored in
%HOME%\cdssetup\OrCAD_Capture\<Install_Version>\downloaded_parts.



Use your Cadence.com login and password in the Sign in window to access SamacSys part libraries.

To access the Ultra Librarian and SnapMagic part libraries, you will need an additional username and account password. When you place a part in an OrCAD X Capture design, the part is downloaded as a zip file to a temp folder and is unzipped in a folder called downloaded_parts in the location defined by your <HOME> environment variable.

Demo: Placing External Library Partner Components



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Video Play Time: **3.10** minutes

Click the Play button to start the video.

Adding Wires

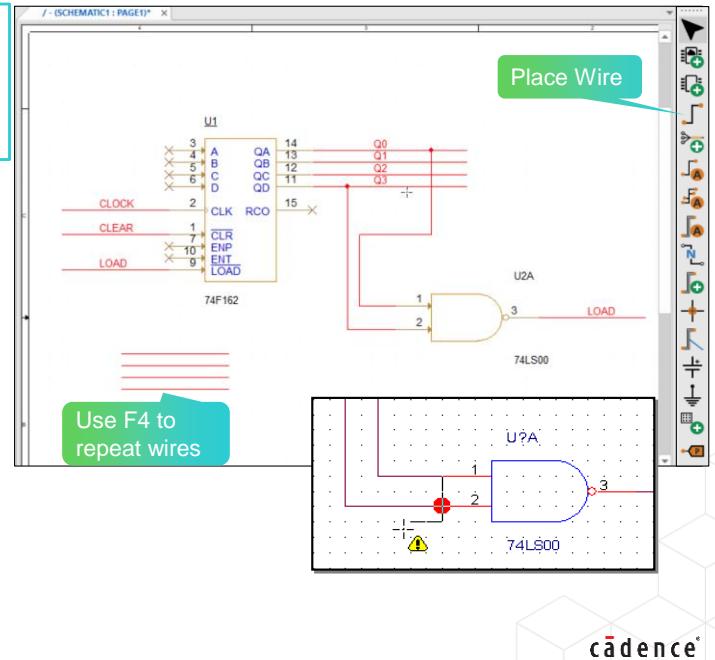
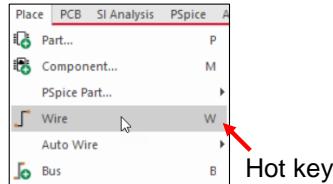


Choose **Place – Wire**.

Or press the **W** shortcut key.



Use wires and net names to define connectivity in the design.



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Use wires and net names to define connectivity in the design.

Here are some things to remember when adding wires:

- Leave Grid Snap enabled (located on the main toolbar above the work area).
- Capture displays a red warning dot when your wire endpoint contacts another wire or pin (indicating that, if you click, you will create a connection). If the new wire path creates a problem (for example, short two pins together), then Capture also displays a warning symbol.
- Wire junctions are marked with junction dots. The absence of the junction dot means the wires are not connected. To remove a junction dot, use the Junction icon in the schematic toolbar to place another junction dot on top of it.
- When you tie a wire to a pin, the connection square at the end of the pin should disappear. If not, the pin is not connected.

Naming Wires



Choose Place – Net Alias.

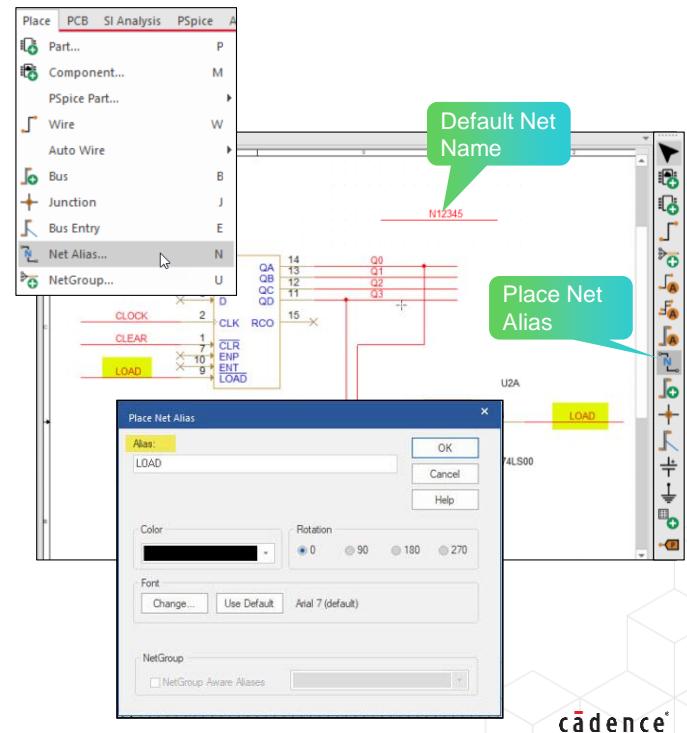


Or press the **N** shortcut key.

Use wires and net names to define connectivity in the design.

Two wires with the same name on the same page are connected by name, even though the wires may not be physically connected to each other.

The use of periods(.), slashes(/), and spaces in net names is not recommended. The percent sign (%) is a reserved PSpice character. The asterisk (*) is considered a wildcard character by Allegro® PCB Editor.



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Two wires with the same name on the same page are connected by name, even though the wires may not be physically connected to each other. When you draw a wire, it is given a default net name, such as N12345. You can change the default net name using a net alias.

If the last character of a net alias is a number, such as DATA7, after the net alias has been placed on the schematic, Capture automatically increments the last character of the net alias (for example, to DATA8) so you can easily place successive aliases in sequence. If the last character is not a number, then the same net name is assigned with each mouse click.

Net aliases can contain any alphanumeric character, including dashes and underscores. The use of periods, slashes, and spaces in net names is not recommended. The percent sign (%) is a reserved PSpice character. The asterisk (*) is considered a wildcard character by Allegro PCB Editor.

It's possible to add two different aliases to the same wire or short two wires with different aliases together. Such errors are not immediately flagged by Capture when they occur but can be found later during a design rule check. (More on design rule checking later in the course.)

Auto Connecting Two Points

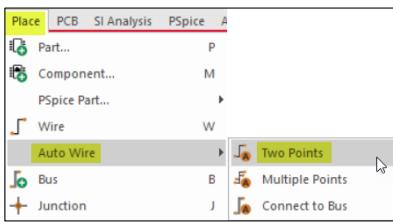


Use the auto-wire feature to connect any two points on a schematic – (part pins or wires) just by picking the start and end points.

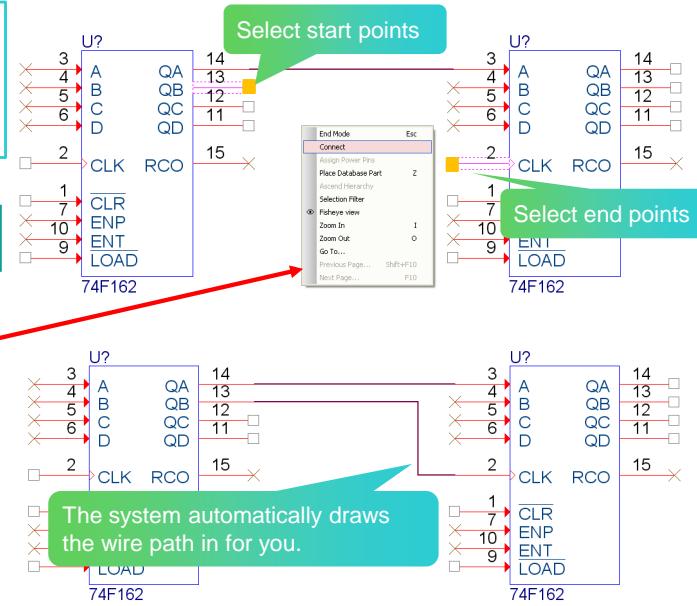
1. Choose Place – Auto Wire – Two Points.



2. Select the start and end points, right-click and choose Connect.

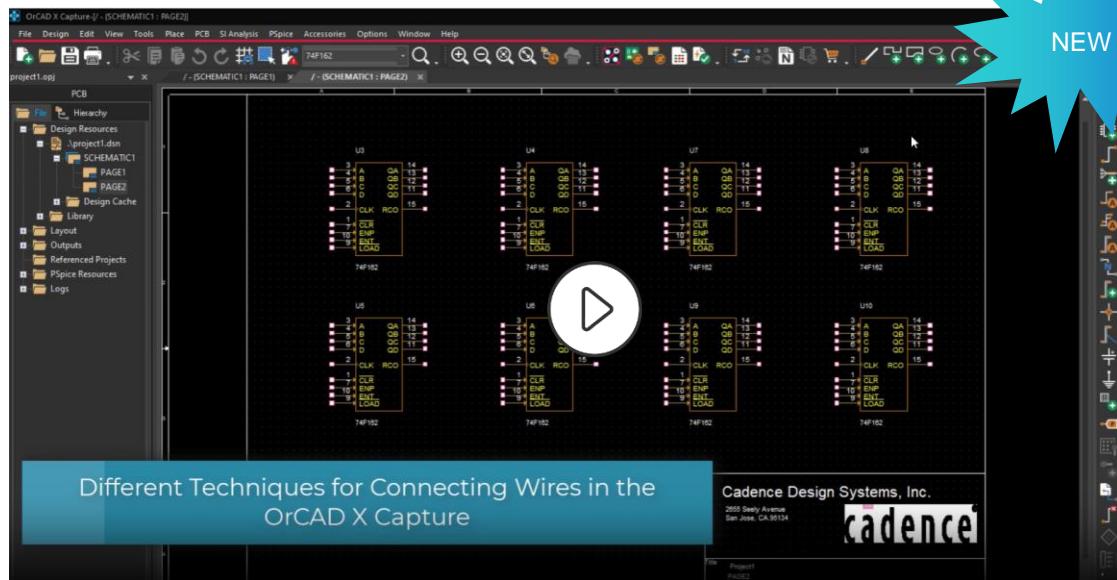


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The auto-wire feature lets you connect any two points on a schematic (part pins and/or wires) just by picking the start and end points. The system automatically draws the wire path in for you. You can access this command from the schematic toolbar icon or from the **Place – Auto Wire** pull-down menu.

Demo: Connecting Wires in the OrCAD X Capture



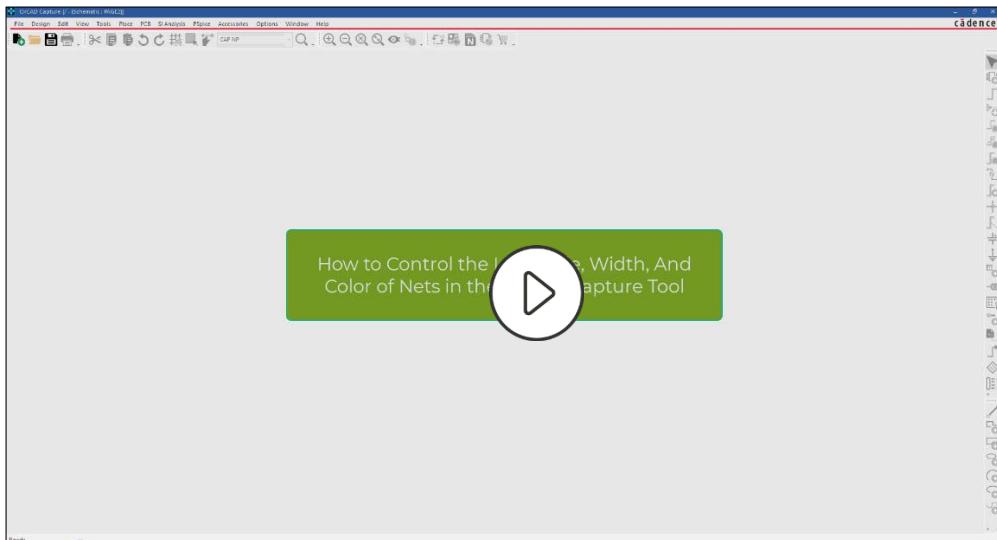
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Video Play Time: **3.38** minutes

Click the Play button to start the video.

Demo: Controlling the Line Style, Width, and Color of the Nets



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Video Play Time: 3.52 minutes

Click the Play button to start the video.

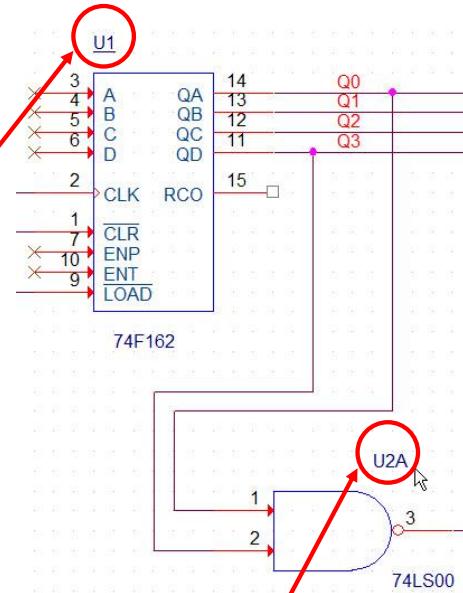
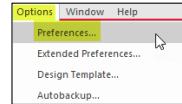
What Is a Part Reference?



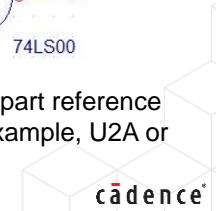
Every part must have a unique identifier to distinguish it from other parts in the design.

This identifier is known as a **part reference**.

- **Part references** can be assigned manually or automatically.
- A manually-assigned part reference will be underlined in the schematic.
- By default, user-assigned references are underlined in the schematic per the **Options – Preferences – More Preferences – Schematic** setup.



When you have a multi-section part, the part reference represents a gate-level reference. For example, U2A or U2B.



Every part must have a unique identifier to distinguish it from other parts in the design. This identifier is known as a part reference. You can assign a part reference manually or automatically.

A manually-assigned part reference will be underlined in the schematic. By default, user-assigned references are underlined in the schematic per the **Options – Preferences – More Preferences – Schematic** setup.

When you have a single-section part, the part reference represents a package-level reference. For example, U1.

When you have a multi-section part, the part reference represents a gate-level reference. For example, U2A or U2B.

Part references must be assigned before you can check the design for errors or create a netlist for PCB design.

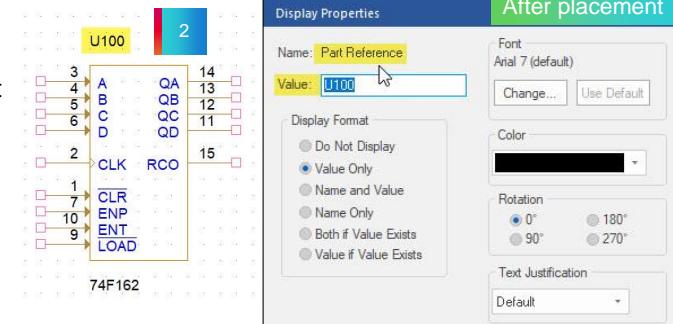
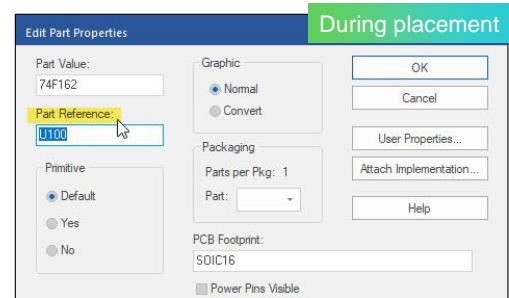
Assigning a Part Reference Manually



You can manually assign a part reference:

- While adding the part to the design.
- Or it can be assigned after the part has been added.

1. After you select the part from the library, **right-click** and select **Edit – Properties** to set a part reference before you place it. When you set the part reference during placement, no user-assigned flag is set, so the part reference will not be underlined.
2. After placement, **double-click** on the part reference text to open the Display Properties form. Any change to the part reference will set the user-assigned flag, and the part reference will be underlined in the schematic.



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1

You can assign a part reference while adding the part to the design. After you select the part from the library, **right-click** and select **Edit – Properties** before you place it. This will open an Edit Part Properties window.

When you set the part reference during placement, no user-assigned flag is set, and the part reference is not underlined.

If you've already added the part to the design, and it currently has no part reference, click on its temporary part reference and edit the value. You can also use this technique to change an existing part reference.

Once the part is placed into the schematic, any change to the part reference will set the user-assigned flag, and the part reference will be underlined.

Here are some things to remember about manually assigning a part reference:

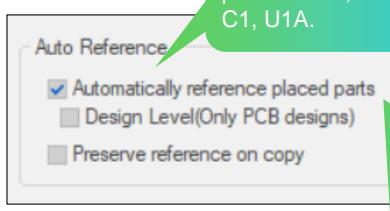
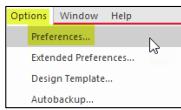
- All parts come into a design with pinouts assigned.
- All parts come into a design with a temporary part reference (for example, U? if single-section or U?A if multi-section). You can manually override this temporary part reference before or after placing the part (as previously described).

Automatic Assignment During Placement



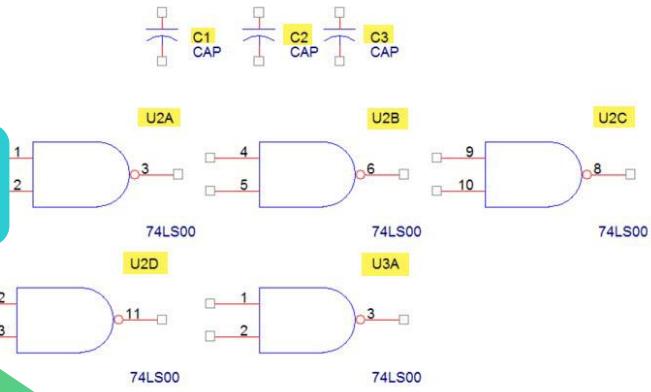
Choose Options – Preferences – Miscellaneous.

Set the following user preference to automatically assign a part reference as you place it into your design.



Option Enable: RefDes patterns are, for example, C1, U1A.

If automatic part referencing is enabled, when a part is placed on the schematic page, the next available reference designator is automatically assigned.



Option Disable: RefDes patterns are, for example, C?, U?A.



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You can set your user preferences to automatically assign a part reference as you place it into your design.

Choose **Options – Preferences – Miscellaneous – Auto Reference** option is OFF by default.

If automatic part referencing is enabled, when a part is placed on the schematic page, the next available reference designator will automatically be assigned. If disabled, parts placed on the schematic will be assigned the temporary reference designator found in the library. For example, C? or U?A.

If the preserve reference on copy option is enabled, when you copy a part and paste it on a schematic page, the part will retain the same reference designator as that of the copied part. But, any new part that you place on a schematic page will not be annotated. This option is not supported for complex hierarchical designs.

You can select only one option at a time. If both the checkboxes are disabled, the new part that you place on a schematic page will not be annotated, and the part reference of a copied part will not be preserved.

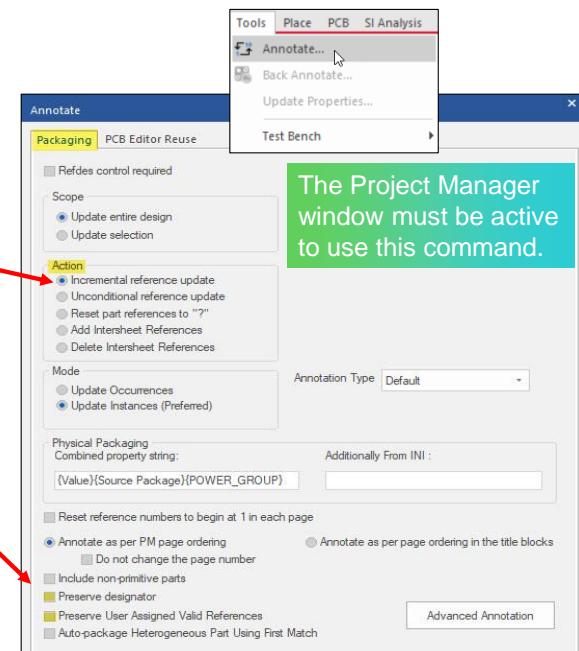
Automatic Assignment After Placement



Choose **Tools – Annotate**. Use this command to automatically assign part references after placing parts.



- In **Incremental mode**, the Annotate program will not change manually or auto-assign a part reference.
- In the **Unconditional mode**, the Annotate program overwrites all existing part references, regardless of how they were assigned.
- Use the **Preserve designator** option to maintain existing designators for homogeneous parts (A, B, C, D) during Unconditional update, or Reset part references to "?".
- Use the **Preserve User Assigned** option to maintain the user-assigned references during Unconditional updates or Reset part references to "?".



To automatically assign part references after placing parts, use the **Tools – Annotate** command.

In **Incremental mode**, the Annotate program will not change manually or auto-assign a part reference, even if duplicate part references exist. The incremental mode only processes parts that have no assigned part references. The incremental mode starts with the next highest part reference. (For example, if the design already has a U100, then the next part reference will be U101.)

In the **Unconditional mode**, the Annotate program overwrites all existing part references, regardless of how they were assigned. Unconditional mode optimizes all multi-section parts into a minimum number of physical packages. The unconditional mode starts with U1, R1, C1, and so forth, and works its way through the sequence, processing parts in the order they appear on the schematic page (left to right, top to bottom). This mode eliminates all duplicate part references in the design.

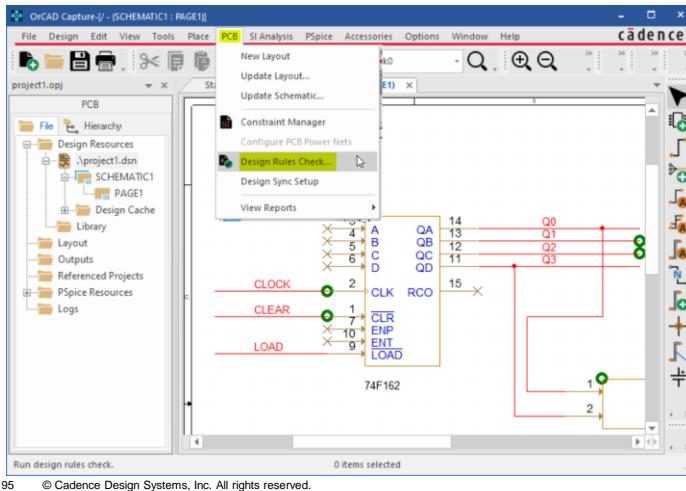
Use the **Preserve designator** option to maintain existing designators for homogeneous parts (A, B, C, D) when using Unconditional reference update, or Reset part references to ?. Use the **Preserve User Assigned** option to maintain the user-assigned references during Unconditional reference update or Reset part references to ?.

Auto-package Heterogeneous Part Using First Match – Select this option to annotate heterogeneous split parts without specifying any grouping property. With this option enabled, Capture decides the grouping of heterogeneous split parts using the first match option.

Using Design Rules Check



Use Design Rules Check to flag connectivity and packaging problems as well as electrical rule violations.



- 1 Setting Options
- 2 Rules Setup
- 3 Report Setup
- 4 ERC Matrix Setup

A Design Rule Check (DRC) is simply a set of rules a designer can use to ensure their schematic matches the rules.

To check the design for errors, choose **PCB – Design Rules Check**.

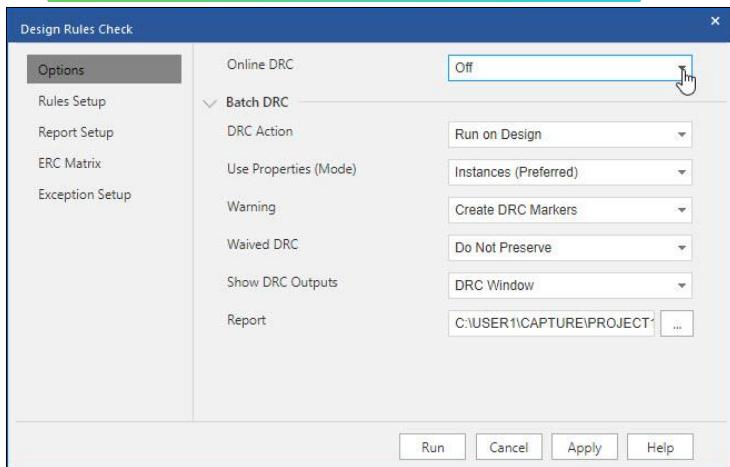


To check the design for errors, choose **PCB – Design Rules Check**. For example, you can flag nets with no driving source or nets with fewer than two connections.

Step 1: Setting Options



Use the Options tab to specify batch or online checking.



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- 1 Setting Options
- 2 Rules Setup
- 3 Report Setup
- 4 ERC Matrix Setup

For batch DRC, this tab controls DRC markers in the schematic and whether you want the DRC report displayed in a window or saved in a file (or both).

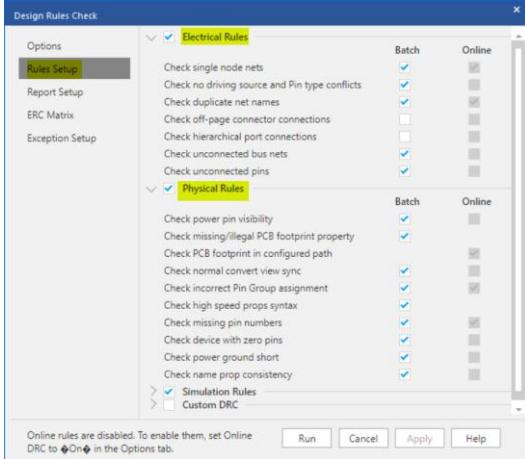


In the Online DRC mode, use the ON mode to check the DRCs online while working on the design.

Step 2: Rules Setup



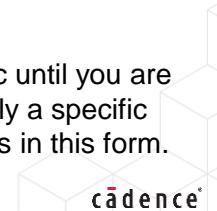
Use the Rules Setup tab to turn on checking for electrical and physical rules, and to pick the rules you want to be applied to the design.



- 1 Setting Options
- 2 Rules Setup
- 3 Report Setup
- 4 ERC Matrix Setup

If you have online checking enabled in the Options tab, then you can specify which rules you want to be applied in batch mode versus which rules you want to be checked online.

This lets you work with the schematic until you are ready to enable online DRC and apply a specific subset of rules based on the switches in this form.

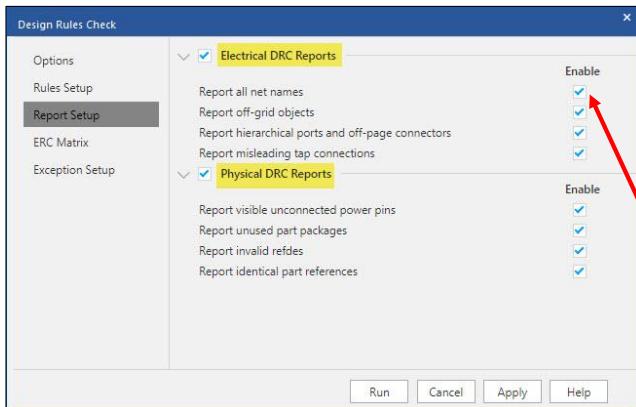


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Step 3: Report Setup



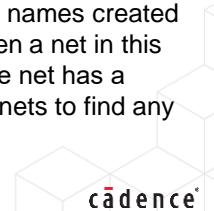
Use this tab to control what information is included in the batch DRC report. This information is useful for locating problems in the design.



1	Setting Options
2	Rules Setup
3	Report Setup
4	ERC Matrix Setup

For example, when two nets have been shorted together, Capture simply uses the net that has the lowest alphanumeric value. No error or warning message is generated by the DRC program. You must use the DRC program to flag these connectivity errors in your design.

To find shorted nets, look at the list of net names created by the **Report all net names** option. When a net in this list contains an “alternate,” that means the net has a second name. Check the list of alternate nets to find any shorted or mislabeled signals.



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Capture does not prevent you from assigning more than one signal name to the same wire or physically shorting two different nets together. You must use the DRC program to flag these connectivity errors in your design. When two nets have been shorted together, Capture uses the net that has the lowest alphanumeric value. No error or warning message is generated by the DRC program.

Capture does not prevent you from manually assigning duplicate or invalid part references. The Annotate program ignores these errors in Incremental mode (or resolves them in Unconditional mode). You must use the DRC program to flag manual annotation errors. For example, the DRC program flags invalid packaging (such as unlike devices assigned to the same physical package), as well as duplicate part references.

Step 4: ERC Matrix Setup



Use the ERC (Electrical Rules Check) Matrix tab to define which pin-type to pin-type connections are valid.

Design Rules Check

- Options
- Rules Setup
- Report Setup
- ERC Matrix**
- Exception Setup

	Input	Bidirectional	Output	Open Collector	Passive	3State	Open Emitter	Input Port	Bidirectional Port	Output Port	Open Collector Port	Passive Port	3State Port	Open Emitter Port	Power	Unconnected
Input																
Bidirectional																
Output																
Open Collector																
Passive																
3State																
Open Emitter																
Input Port																
Bidirectional Port																
Output Port																
Open Collector Port																
Passive Port																
3State Port																
Open Emitter Port																
Power																
Unconnected																

Restore Defaults

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1	Setting Options
2	Rules Setup
3	Report Setup
4	ERC Matrix Setup

Click on any box in the matrix and toggle it to warning or error.

The pin combination is valid

Flagged as a warning

Flagged as an error

Use this row to set the severity for various types of unconnected pins.



The Electrical Rules Check Matrix tab will flag invalid pin-to-pin connections in the design. Use this tab to define which pin-type to pin-type connections are valid. Each pin-to-pin combination can be defined as valid (no error or warning) or invalid (error or warning flag generated).

The matrix includes a row used to define the error severity when various types of pins are left unconnected.

The severity settings have no effect on your ability to create a netlist.

The ERC Matrix settings are stored in the *Capture.ini* file. Use the **Restore Defaults** button to reset the matrix.

Viewing the DRC Report



You can **double**-click on the file in the Outputs folder of the Project Manager to view the report.

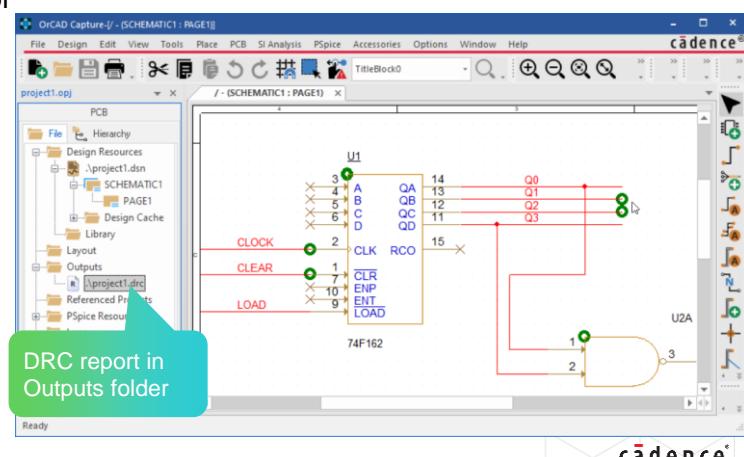
The Design Rules Check generates a report of all the objects checked and any violations found.

DRC report
(Project1.drc)

```
Checking Schematic: SCHEMATIC1
-----
Checking Electrical Rules
WARNING (ORCAP-1608): Net has no driving source CLEAR
SCHEMATIC1, PAGE1 (3.10, 2.80)
WARNING (ORCAP-1608): Net has no driving source CLOCK
SCHEMATIC1, PAGE1 (3.10, 2.60)

Checking For Single Node Nets
WARNING (ORCAP-1600): Net has fewer than two connections CLEAR
SCHEMATIC1, PAGE1 (3.10, 2.80)
WARNING (ORCAP-1600): Net has fewer than two connections Q1
SCHEMATIC1, PAGE1 (5.60, 2.20)
WARNING (ORCAP-1600): Net has fewer than two connections Q2
SCHEMATIC1, PAGE1 (5.60, 2.30)
WARNING (ORCAP-1600): Net has fewer than two connections CLOCK
SCHEMATIC1, PAGE1 (3.10, 2.60)
```

The results of the DRC check can also be displayed in a DRC window.



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The Design Rules Check generates a report of all the objects checked, and any violations found. This report is listed under the *Outputs* folder in the Project Manager window. You can **double**-click on the filename to view the report.

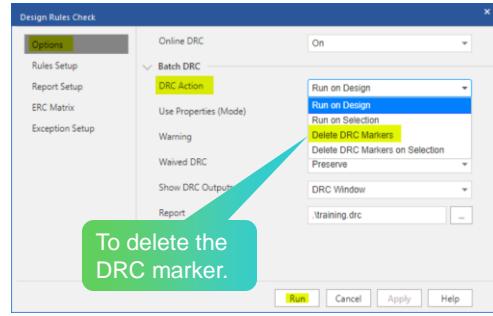
Querying a DRC Marker



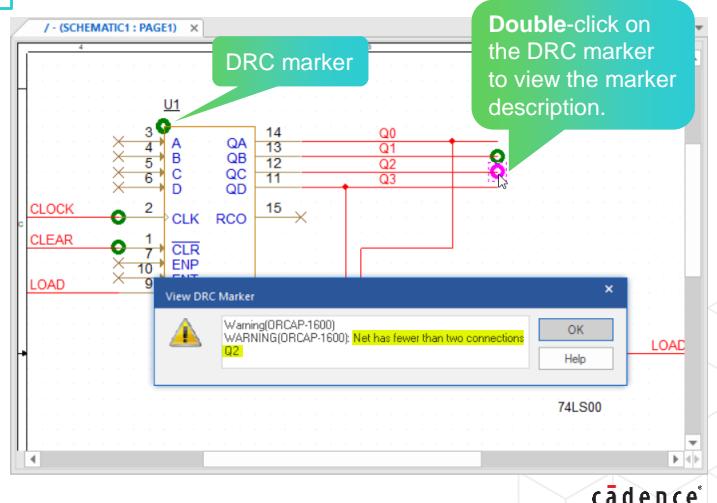
You can **double**-click on a DRC marker to see a description of the problem.

Design Rules Check adds warning and error markers to the schematic pages.

The design must be saved to retain the new markers.



Each time you start the DRC program, it automatically clears existing markers and creates new markers.

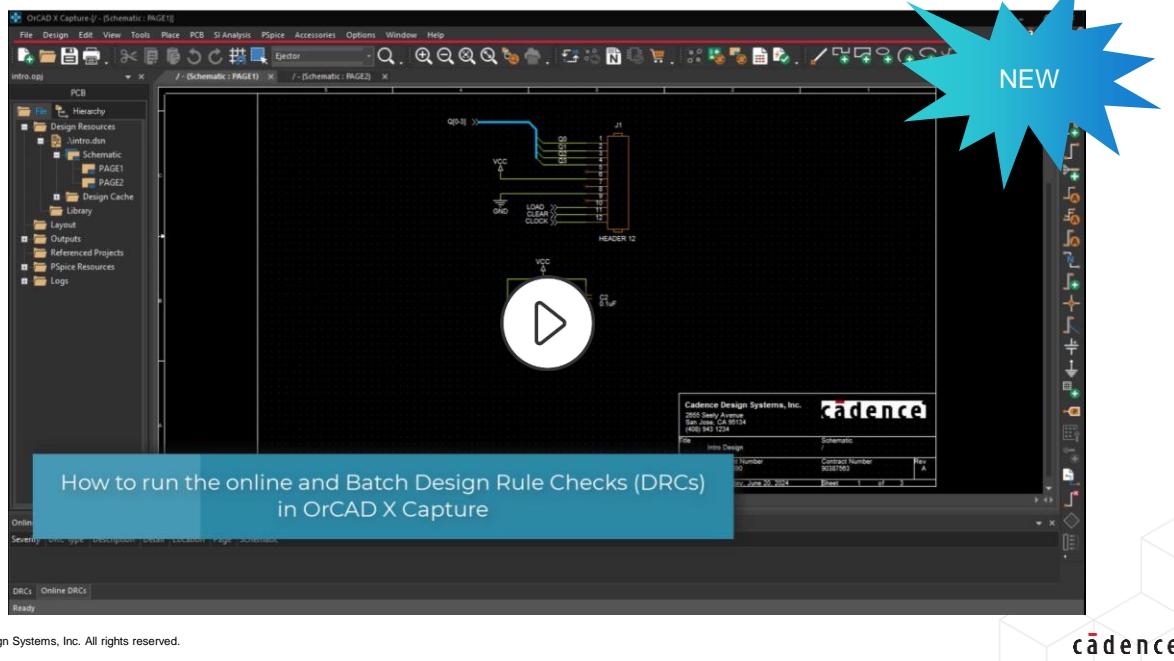


Design Rules Check adds warning and error markers to the schematic pages. You can **double**-click on a DRC marker to see a description of the problem.

When you save the design, the DRC markers are also saved. Each time you start the DRC program, it automatically clears existing markers and creates new markers. The design must be saved to retain the new markers.

You can delete the DRC markers interactively or delete them automatically by using the **Delete DRC Markers** option in the DRC Action field of the Design Rules Check Options tab.

Demo: How to Run the Online and Batch Design Rule Checks (DRCs)



Video Play Time: **4.41** minutes

Click the Play button to start the video.



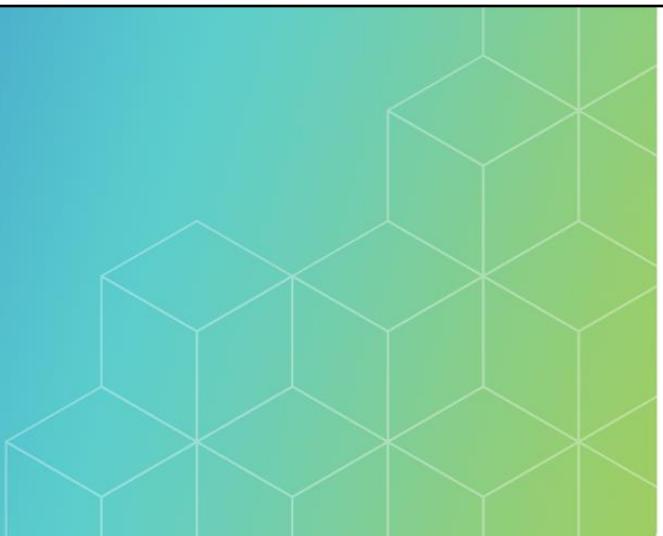
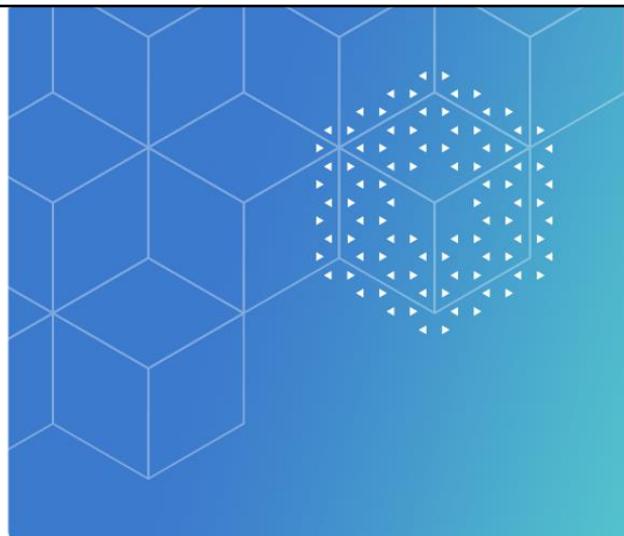
Labs

- Lab 5-1 Creating a New Project
- Lab 5-2 Placing Parts
- Lab 5-3 Adding and Naming Wires
- Lab 5-4 Assigning Reference Designators
- Lab 5-5 Running Design Rules Check

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You will now have the opportunity to perform some self-paced labs to reinforce the ideas presented in this module.



Module 6

Building a Multi-Sheet Schematic

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Welcome to Module 6: Building a Multi-Sheet Schematic.

Module Objectives

In this module, you

- Create a new project and add parts and wires to page one
- Copy a page from another design
- Annotate the multi-sheet design
- Check the design for errors
- Add intersheet signal references
- Create a part cross reference report

Introduction to OrCAD X Capture

Setting Up Your Environment

Working with Libraries

Building a Simple Schematic

Building a Multi-Sheet Schematic

Editing Part Properties

Building a Hierarchical Design

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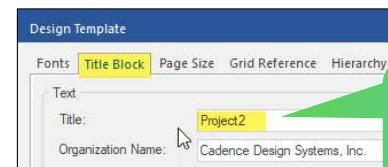


This is where you are in the course flow.

Creating a New Project

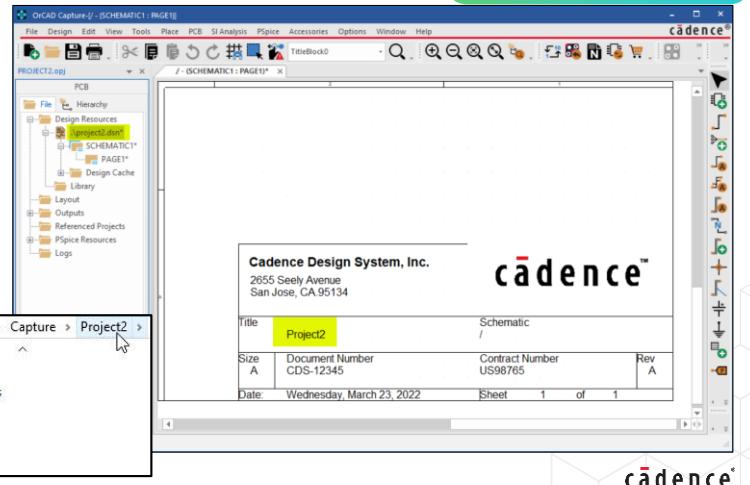
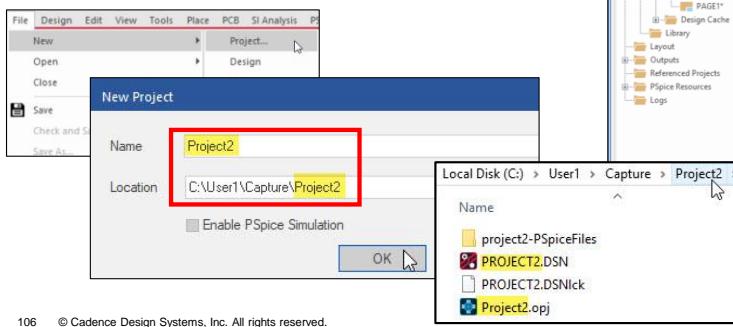


Choose **File – New – Project** to create a new project folder to hold your design.



Don't forget to revise the Title Block settings in your Design Template *before* creating your new project.

The project name is used to name both the project and design files. This name will also appear in the Title Block on each schematic page.



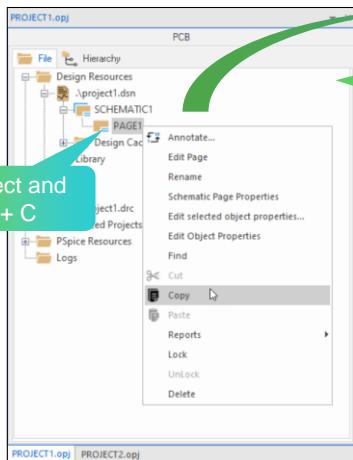
Create a project directory for each new project. OrCAD® X Capture keeps all the project files together in one place. The folder you specify in the Location field doesn't need to exist (the New Project Wizard will create it for you).

Don't forget to revise the Title Block settings in your Design Template before creating your new project.

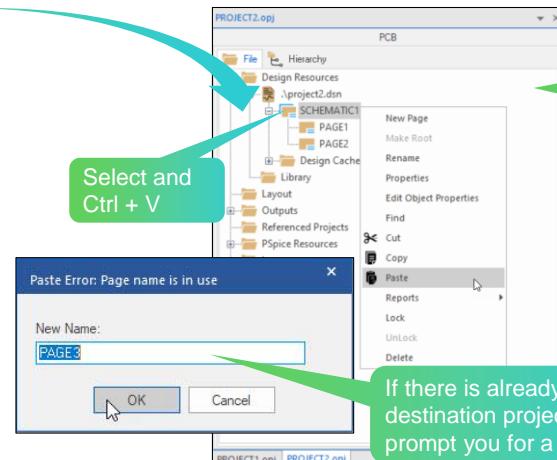
Copying Between Projects



Use the right mouse pop-up menu in the Project Manager to copy schematic pages between projects.



Source Project



Destination Project

If there is already a PAGE1 in the destination project, Capture will prompt you for a new page name.

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Use the Project Manager window to copy an existing schematic page (or folder) from another project. For example, you can copy PAGE1 from the Project1 window into the Project2 window. The page or folder you copy must be uniquely named. If there is already a schematic page in the destination project called PAGE1, Capture will prompt you for a new page name.

Drawing and Connecting Bus Wires Manually



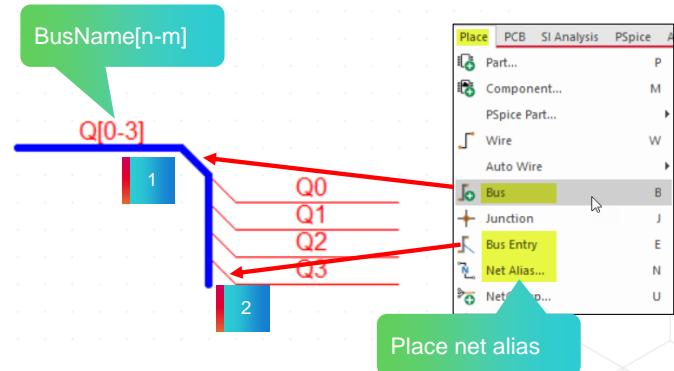
A bus wire is a vector (multiple-bit wires) used to graphically bundle a group of scalar (single-bit) wires together.

This makes it easier to draw the schematic and makes it easier to read.

- 1 Use the **Place – Bus** command to draw the bus wire.

A bus wire is graphically thicker than a regular wire.

Use special syntax to name the bus wire.



- 2 Use the **Place – Bus Entry** command to connect wires to a bus.

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A bus wire must be labeled to reflect the scalar nets it represents (otherwise, it would be assigned a system-generated net name like any other unlabeled wire in the design). If you mislabeled the wire, the DRC program would flag any connectivity errors that may result. For example, Q[0-3] has no driving source, fewer than two connections, etc.

Select the **Place net alias** icon in the toolbar and follow the special bus naming syntax to assign an alias to a bus wire.

The variable [n-m] represents the range of signals carried by the bus (n can be greater or less than m). The brackets must be square brackets; otherwise, Capture won't let you attach the alias to a bus wire. Other (alternate) bus name formats are BASENAME[n-m] or BASENAME[n..m].

Whatever naming convention you choose, use it consistently.

A *bus entry* is a library symbol used to connect wires to buses. You may need to rotate the bus entry symbol before placing it.

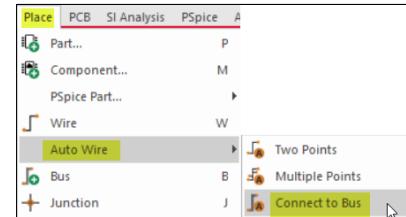
You can use a bus entry symbol to merge or split like-named buses. When a bus entry is used in this way, it appears thicker than a normal (single-bit) bus entry.

In the above example, if you want the bus to appear as a Bus object in the PCB Editor Constraint Manager Net folder, you can **double-click** on the bus wire, then select the **User Properties** button in the Net Properties window to add the **BUS_NAME=<any name>** property (else PCB Editor Constraint Manager Net folder lists member nets only – no higher-level bus object).

Auto Connect to Bus

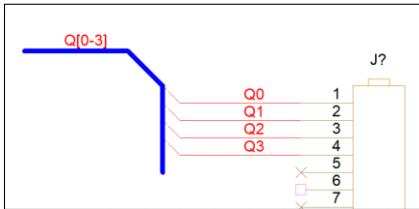


Choose Place – Auto Wire – Connect to Bus.

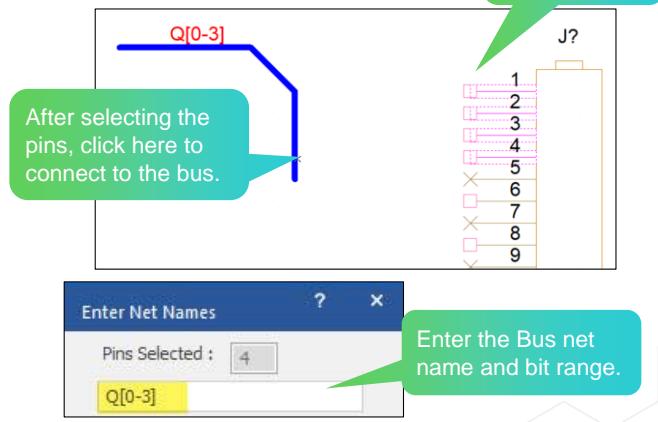


Use the **Connect to Bus** command to automatically connect selected pins or wires to a bus.

The net name range is always distributed top to bottom or left to right and is not affected by the order in which you selected the pins.



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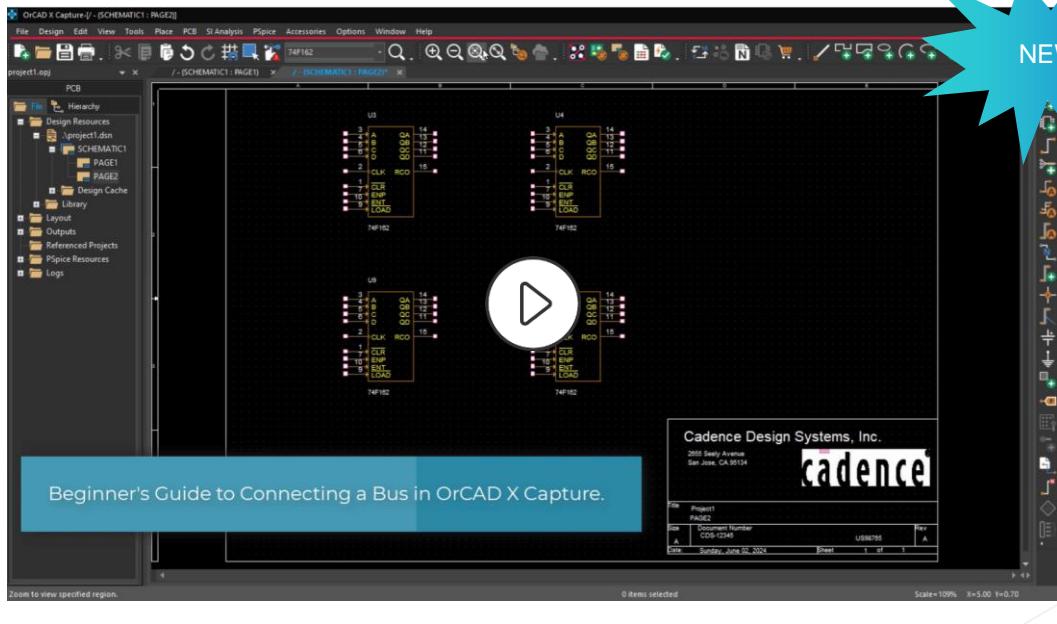
Choose the **Auto Wire – Connect to Bus** command to automatically connect pins or wires to a bus.

To connect to the bus, you

1. Draw a Bus.
2. Click on the **Connect to Bus** command.
3. Select all the pins and tap to the bus.
4. Enter the Bus net name and bit range.
5. Click **OK** to connect pins to the bus.

The net name range is always distributed top to bottom or left to right and is not affected by the order you selected the pins.

Demo: Connecting a Bus in OrCAD X Capture



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Video Play Time: **2.21** minutes

Click the Play button to start the video.

Adding Voltage Symbols



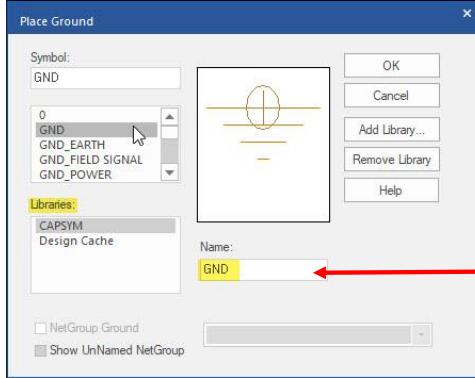
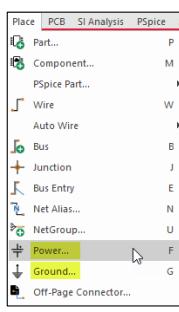
Choose **Place – Power**.

or

Choose **Place – Ground**.

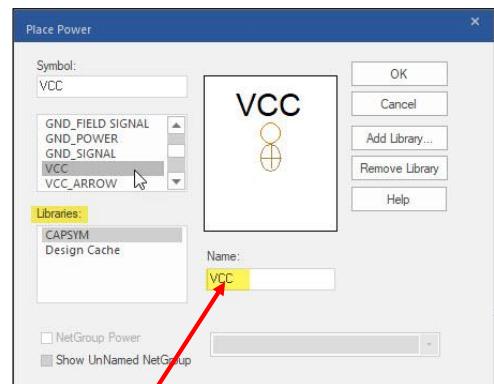


Use these commands to add power and ground nets to your design.

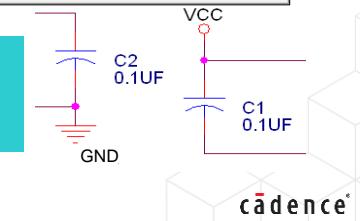


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Cadence® supplies voltage and GND symbols in the *capsym.olb* library.



Use the Name field to specify the voltage signal name.



Choose the **Place – Power** or **Place – Ground** command to add voltage symbols to the design. These symbols are also located in the CAPSYM library.

Use the Name field to specify the name of the voltage signal.

All voltage symbols represent global nets. This means that any wires tied to voltage symbols having the same name will be connected together, regardless of which page they are on or which schematic folder they are in.

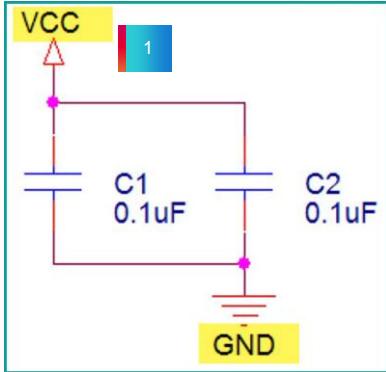
Another source of global nets is the hidden voltage pins defined in a library part.

When you connect two voltage symbols together, the voltage symbol with the alphanumerically lowest net name takes precedence. For example, if you connect an AGND symbol to a GND symbol, all GND connections will appear in the netlist as AGND.

Use symbols from the PSpice library, *Source.olb*, to designate a signal as high or low during simulation. You could also set the net name on a voltage symbol to 0 (zero).

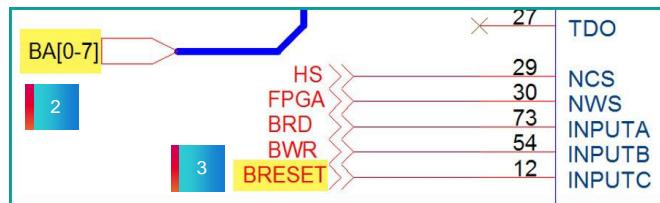
How Is the Name of a Symbol Used?

Any wire (or bus) attached to a symbol inherits the name of that symbol as its net name.



This applies to the following types of symbols:

- 1 Power and ground symbols
- 2 Hierarchical ports
- 3 Off-Page connectors



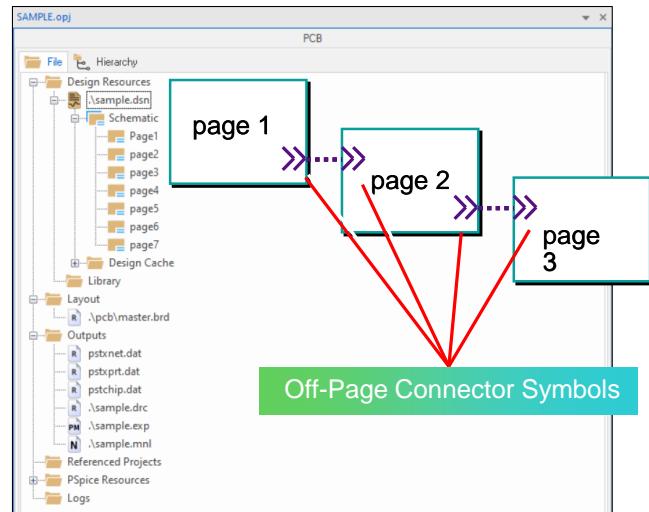
This page does not contain notes.

What Are Off-Page Connector Symbols?



Off-page connector symbols connect nets from one page to another.

When two wires with the same name appear on different pages, you must add an off-page connector to each page to establish connectivity between the two wires.



Two wires with the same net alias are automatically connected by name when they appear on the same page. But when these two wires exist on different pages, you must add an off-page connector to each page to establish connectivity between the two wires.

Each off-page connector you add must be named. This name identifies the net that needs to be connected to the other page.

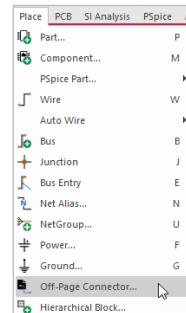
The name of the off-page connector overrides the net alias of the wire it is attached to. When an off-page connector is tied to an unlabeled wire, that wire inherits the off-page connector name.

Off-page connectors do not connect nets from one hierarchical folder to another. You must use a hierarchical port for this.

Adding Off-Page Connectors



Choose **Place** – click on **Off-Page Connector**.

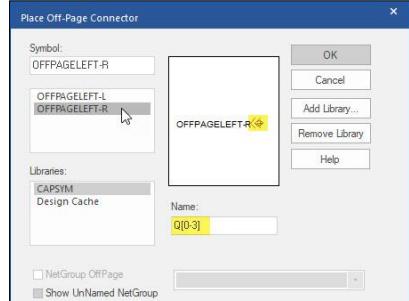
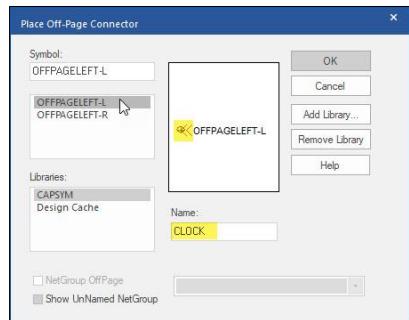


CLOCK ➤

Q[0-3] ➤

➤ CLOCK

➤ Q[0-3]



The accompanying example shows how to use two off-page connectors from the *capsym.olb* library to establish connectivity between pages for the CLOCK and Q[0-3] signals.

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Choose **Place** – click on **Off-Page Connector** to add off-page connectors to the design. There are two off-page connector symbols in the CAPSYM library.

When placing an off-page connector, you must consider two things:

- The direction you want the off-page connector to point.
- Which side of the off-page symbol do you want the pin (or connection point) to be ON.

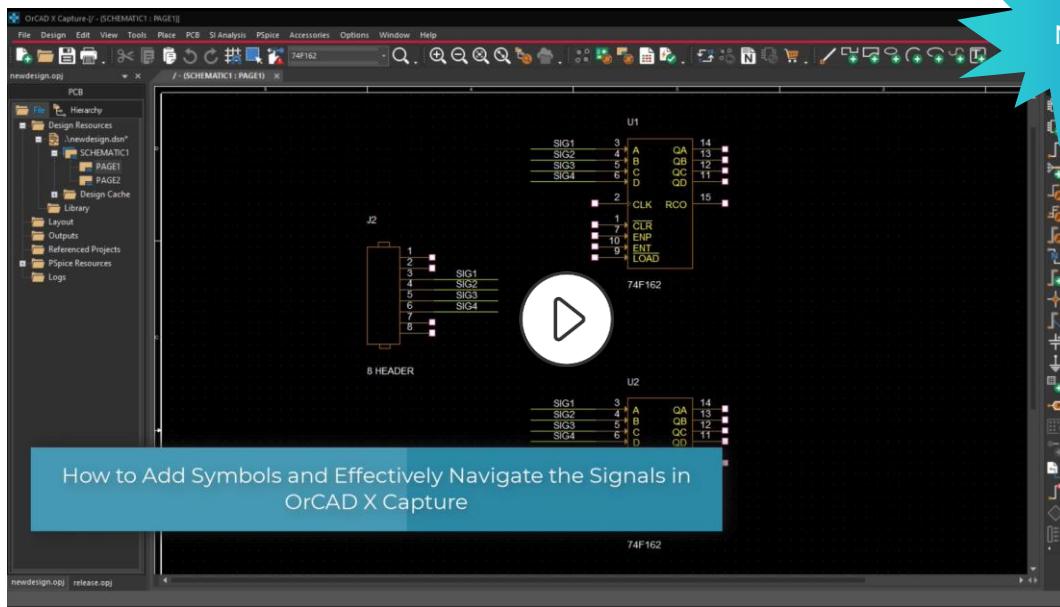
The name of the off-page connector symbol reflects its pointed direction and pin location.

For example, the OFFPAGELEFT-L symbol points to the left, with its connection point on the left. The other off-page connector in the CAPSYM library is called OFFPAGELEFT-R (it also points to the left, but the pin is on the right).

As you can see, both off-page connector symbols point to the left. If you draw a schematic with input signals on the left side of the page and output signals on the right side, you will probably rotate both these off-page connector symbols before placing them in the design (as demonstrated in the accompanying illustration).

From a logic standpoint, off-page connectors do not define any directional information about the nets; they just represent the net name only.

Demo: Adding Symbols and Effectively Navigate the Signals



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Video Play Time: **4.40** minutes

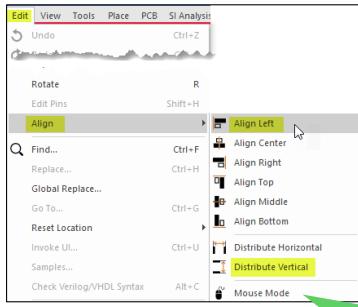
Click the Play button to start the video.

Aligning Components

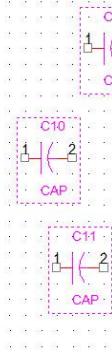


Choose **Edit – Align...**

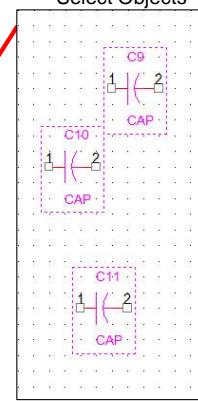
Use this command to align and distribute selected objects using the following submenu commands.



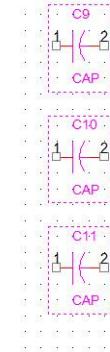
Distribute Vertical



Select Objects



Align Left



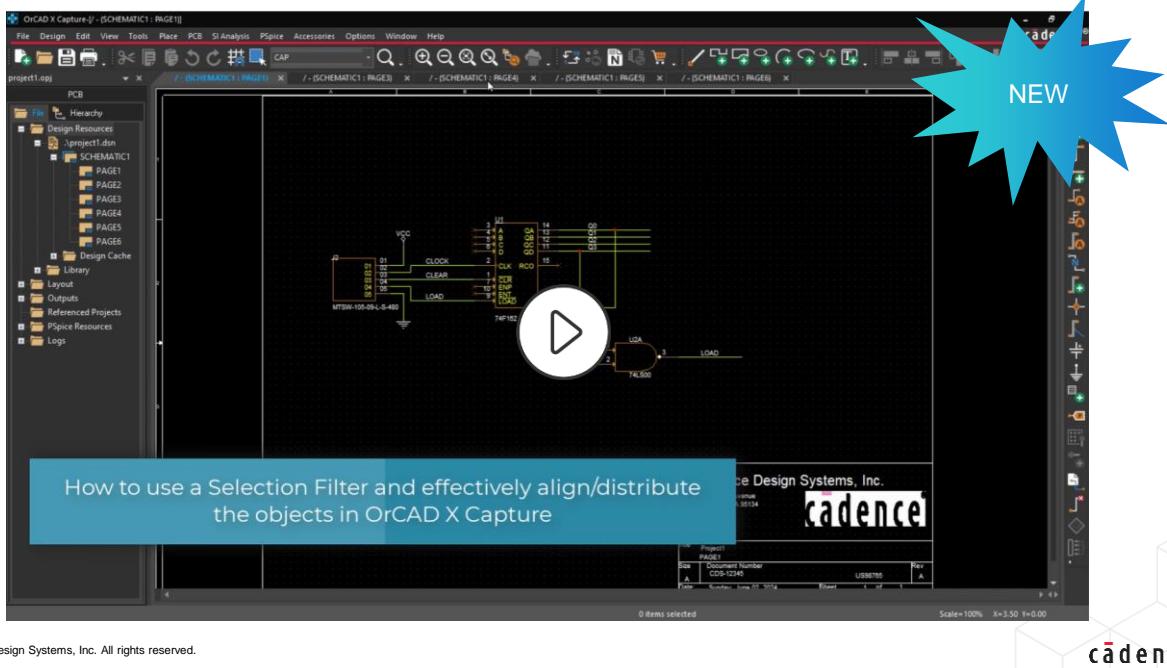
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Mouse Mode lets you click to specify an alignment point.

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Use this command to align all selected objects to the farthest left, farthest right, topmost, or bottommost object in the selected set. You can enable Mouse Mode to specify an alternate alignment point. You can also use this command to equally distribute the selected objects. To distribute objects within a specified area, see the **Options – Preferences – Colors/Print tab** – click on the **More Preferences – Extended Preferences** menu.

Demo: Selection Filter and Effectively Align/Distribute the Objects



Video Play Time: **4.26** minutes

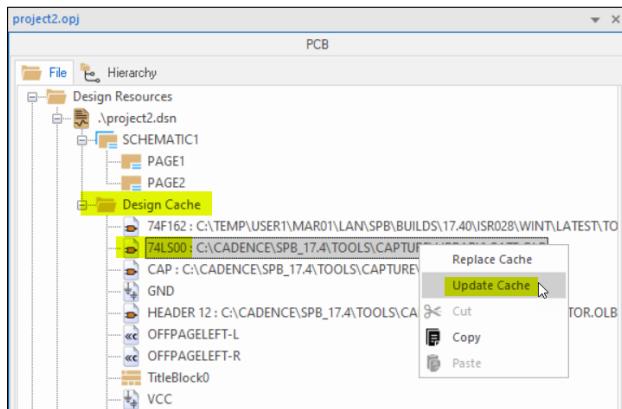
Click the Play button to start the video.

What Is the Design Cache?



Design Cache is like an onboard library.

When you add a part to a design, Capture automatically stores a copy of the part in a Design Cache folder.

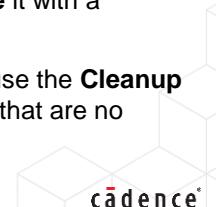


If a part you've added to the design is later modified in the library, when you try to add the modified part, Capture compares it to the part stored in Design Cache and issues a warning saying the part is different from the one already in your design.

You can choose to update the cache part with the latest version in the company library or add the older version of the part from Design Cache.

You can also perform these operations:

- Select a part in the Design Cache folder of the Project Manager window and **replace** it with a completely different part.
- Select the Design Cache folder and use the **Cleanup Cache** command to remove all parts that are no longer used in the design.



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When you add a part to a design, Capture automatically stores a copy of the part in a Design Cache folder. This makes the Capture design completely self-contained (not dependent on any supporting libraries) because copies of the parts are in the design file.

This makes it easy to place more instances of a part that is already in the design. To do this, select the Most Recently Used (MRU) drop-down list box in the main toolbar. This field lists the last 25 parts.

If a part you've added to the design is later modified in the library, when you try to add the modified part, Capture compares it to the part stored in Design Cache and issues a warning saying the part is different from the one already in your design.

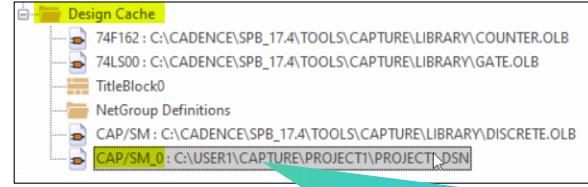
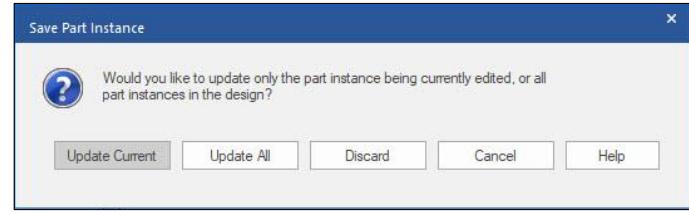
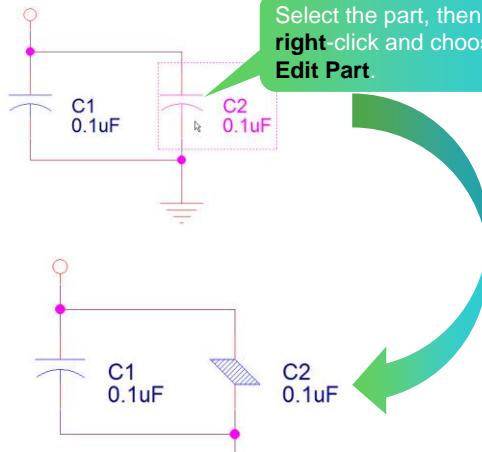
You can choose **Design – Update Cache** to update the part in Design Cache to match the edited version in the library, or you can decide against this and add a copy of the part from the Design Cache instead (using the MRU list box).

When you delete a part from the design, a copy remains in Design Cache. Choose **Design – Cleanup Cache** to remove parts from Design Cache that are no longer in the design. You can also choose **Design – Replace Cache** to replace a part in cache with a completely different part (such as a global part replacement).

Editing a Part in the Design



There may be a need to modify a part in the design only (not in the company library). This means you are changing the part in Design Cache (the onboard design library).



If you apply the change to just the selected part (instead of all instances in the design), this will create a hybrid part in Design Cache.

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You can edit a part in the design. This means you are changing the part in Design Cache only (not in the library). When you finish editing the part instance, the Save Part Instance dialog box lets you do the following:

Update Current – Apply the changes only to the selected part instance. This will create a hybrid part in Design Cache.

Update All – Apply the changes to all instances of the selected part. If you have an identical part from another library, the instances of the part from the second library won't be affected.

Discard – Return to the schematic page editor without applying any changes to the selected part instance.

Cancel – Return to the part editor and continue editing the part.

Annotating a Multi-Sheet Design

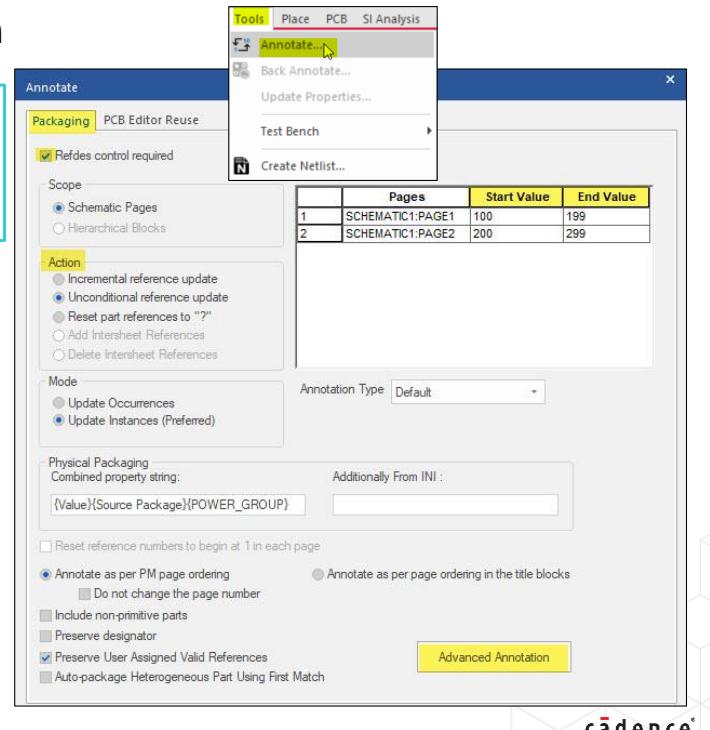


Choose Tools – Annotate.



Use this command to automatically assign part references after placing parts.

- You can process the entire design or just select pages.
- The Annotate command can be run in Incremental or Unconditional mode.
- Use the Advanced Annotation button to access enhanced controls for reference designator ranges.



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If you've copied a page from another design and the page had part references assigned, you could end up with duplicate part references. When you run the Annotate program in **Incremental mode**, this problem won't be resolved because Incremental mode ignores parts with assigned part references, even if duplicates exist.

The **Unconditional reference update** option assigns new part references to all parts in the design (like starting over from the beginning). This mode resolves all invalid packaging or duplicated part reference problems.

The **Reset part references to “?”** option is useful when copying pages from other designs. For example, you can select just the copied pages in the Project Manager window and run the Annotate program to reset the part references on just those selected pages. Then, run the Annotate program in Incremental mode to process just the parts that were previously reset (without affecting existing assignments on other pages of the design).

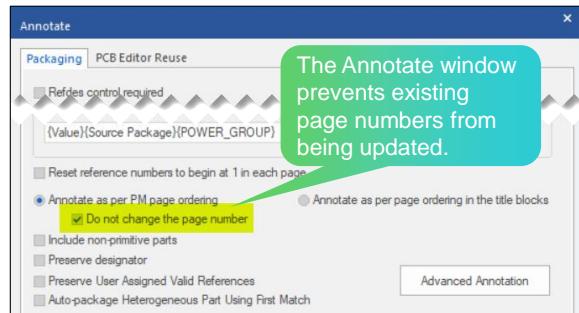
Controlled annotation lets you annotate the design based on a range you set for each page. When the **RefDes Control Required** box is selected, a Scope section displays the **Schematic Pages** and **Hierarchical Blocks**. You can set the range for each page in a flat design and the range for each block in a hierarchical design.

Automatic Page Numbering

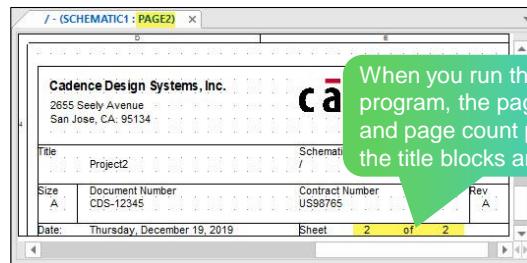
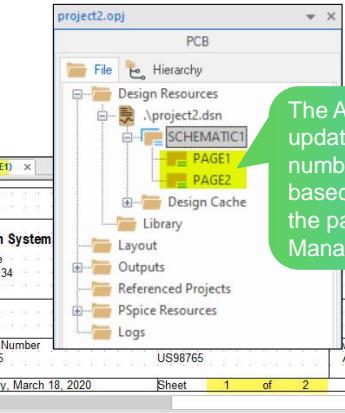


Schematic pages are sorted by name in the Project Manager window.

This page order affects the automatic page numbering in the Title Block during Annotation.



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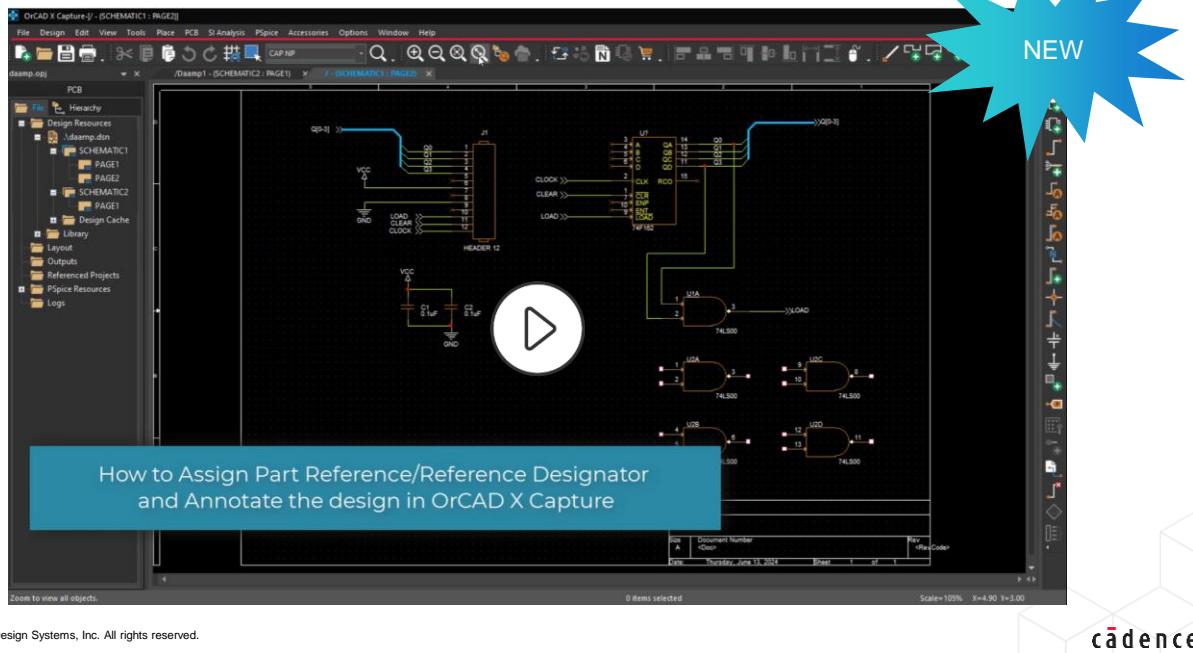


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When you add a new schematic page, the page number and page count properties in the title block default to 1 (for example, Sheet 1 of 1).

Adding, deleting, or renaming pages can change the page order. Use the **Do not change the page number** option in the Annotate window to prevent existing page numbers from being updated. This can result in a page ordering in the Project Manager that may not match the page numbering in the title block.

Demo: Assigning Part Reference/Reference Designator and Annotating the Design



Video Play Time: **5.17** minutes

Click the Play button to start the video.

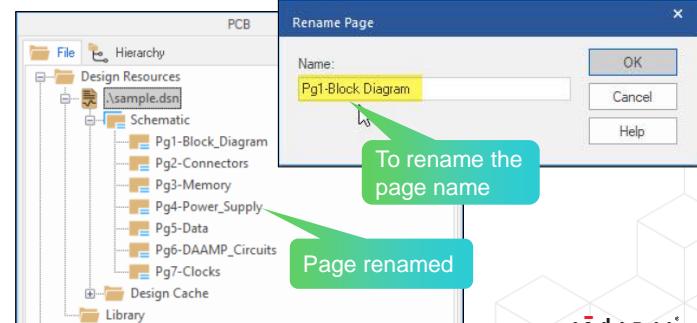
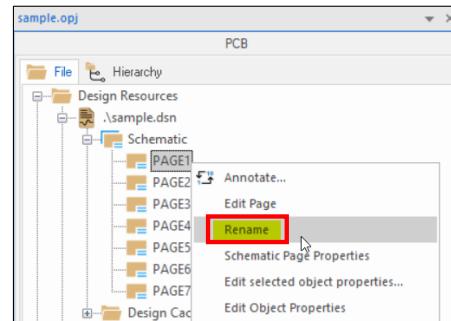
Naming Pages to Control Page Order



Pages are sorted alphanumerically in the Project Manager.

Sequential page numbers are assigned based on this alphanumeric sorting.

- Right-click on the page in the schematic folder and select the **Rename** option to rename a page.
- When you rename a page, it may move to a new position in the page tree based on its new name.
- To maintain control of page sequence and still name your pages functionally, use a numeric prefix such as Pg1 followed by a logical page name.



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By default, the system automatically names new pages as PAGE1, PAGE2, and so on. You can change the name of the new page as you add it to the schematic, or you can rename it later.

To rename a page, right-click on the page in the schematic folder and select the Rename option. You cannot use a name that already exists in the schematic folder.

Please be aware that pages are sorted alphanumerically in the schematic folder. When you rename a page, it may move to a new position in the page tree based on its new name. To maintain control of page sequence and still name your pages functionally, use a numeric prefix such as Pg1 followed by a logical page name (as shown in the accompanying illustration).

DRC Checking for Off-Page Connections



Choose PCB – Design Rules Check.



The following setup options may help you locate the source of a connectivity error in the design.

- In the Rules Setup tab, use the **Check off-page connector connections** option in the Design Rules Check window to ensure each off-page connector has at least one match on another page.
- In the Report Setup tab, use the **Report hierarchical ports and off-page connectors** option to list all the off-page connector names in the design.

Design Rules Check

Options

- Rules Setup (selected)
- Report Setup
- ERC Matrix
- Exception Setup

Electrical Rules

	Batch	Online
Check single node nets	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Check no driving source and Pin type conflicts	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Check duplicate net names	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Check off-page connector connections	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Check hierarchical port connections	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Check unconnected bus nets	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Check unconnected pins	<input checked="" type="checkbox"/>	<input type="checkbox"/>

Design Rules Check

Options

- Rules Setup
- Report Setup** (selected)
- ERC Matrix

Electrical DRC Reports

	Enable
Report all net names	<input checked="" type="checkbox"/>
Report off-grid objects	<input checked="" type="checkbox"/>
Report hierarchical ports and off-page connectors	<input checked="" type="checkbox"/>
Report misleading tap connections	<input checked="" type="checkbox"/>

Check alternate in these reports.

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Use the **Check off-page connector connections** option in the Design Rules Check window to ensure each off-page connector has at least one match on another page.

Use the **Report hierarchical ports and off-page connectors** option to list all the off-page connector names in the design. This list may help you locate the source of an off-page connector error (such as a misspelled name).

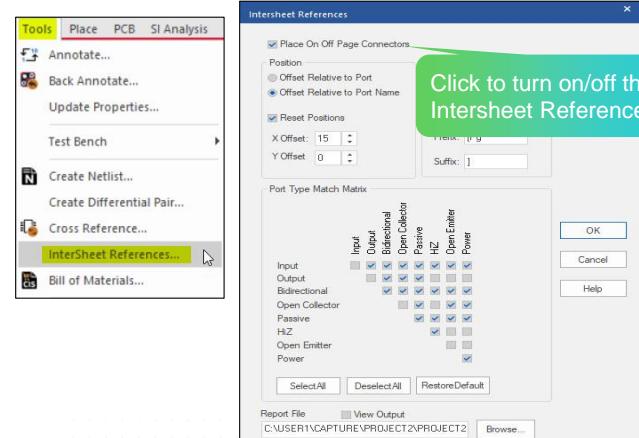
When there's a mismatch between a wire alias and an off-page connector name, DRC does not flag an error. The off-page connector name overrides the wire alias. Use the **Report all net names** option to list all net names in the design and check all alternate net names for problem overrides.

Adding Intersheet References

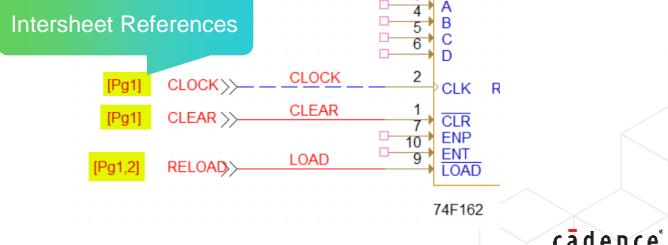


Choose Tools – InterSheet References.

- Use **Intersheet References** to display the destinations of all signals tied to off-page connectors.
- This information is useful for tracking a net from one page to another.
- The Project Manager window must be active to use this command.



The Intersheet References are not hyperlinks.



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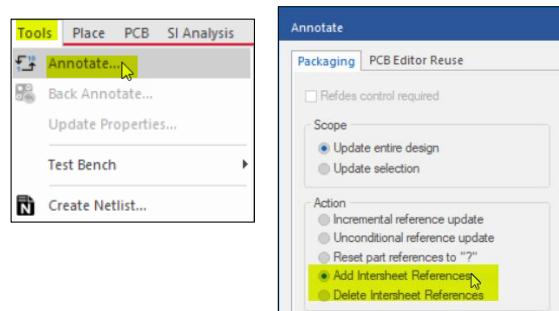
All multi-sheet nets must have an off-page connector in order to connect across pages. If a net has no off-page connector, then it won't be connected to any other page.

The page numbers in the intersheet cross-references come from the page numbers in the title block. Intersheet References can also include page zone information taken from the Grid Reference you defined in the Design Template.

Choose **Tools – InterSheet References** to set up and add intersheet references to your design. Turn on the **Place On Off Page Connectors** option to add the intersheet references and turn this option off to delete them from the design.

Adding Intersheet References (continued)

- Choose Tools – InterSheet References.
- Choose Tools – Annotate – Add Intersheet References.
- When pages are added, deleted, or renamed – the Annotate program, by default, changes the numbers in the title block, which makes the existing intersheet references obsolete.



The screenshot shows the Cadence PCB Editor interface. On the left, the 'project2.opj' project browser displays a hierarchy of files: 'File', 'Hierarchy', 'Design Resources', 'Design Cache', 'Library', 'Layout', 'Outputs', and 'Referenced Projects'. A callout bubble from the previous slide points to the 'Outputs' folder. On the right, a table titled 'PROJECT2' lists 11 rows of intersheet reference data. The columns are labeled A through J. The data includes information such as Name, Type, Page, Page Num, Schematic, PartPin, LocationX, LocationY, Zone, and IREF. Rows 10 and 11 show 'RELOAD' entries for both PAGE1 and PAGE2. The bottom right corner of the interface features the Cadence logo.

	A	B	C	D	E	F	G	H	I	J
1	Name	Type	Page	Page Num	Schematic	PartPin	LocationX	LocationY	Zone	IREF
2	O[0-3]	OffPage	PAGE1	1	SCHMATIC1		140	90	5D	[Pg2]
3	Q[0-3]	OffPage	PAGE2	2	SCHMATIC1		650	160	2D	[Pg1]
4	CLOCK	OffPage	PAGE1	1	SCHMATIC1	U1.11	240	230	4C	[Pg2]
5	CLOCK	OffPage	PAGE2	2	SCHMATIC1	U1.2	210	250	4C	[Pg1]
6	CLEAR	OffPage	PAGE1	1	SCHMATIC1	U1.12	240	240	4C	[Pg2]
7	CLEAR	OffPage	PAGE2	2	SCHMATIC1	U1.1	210	270	4C	[Pg1]
8	RELOAD	OffPage	PAGE1	1	SCHMATIC1	U1.10	240	220	4C	[Pg2]
9	RELOAD	OffPage	PAGE2	2	SCHMATIC1	U1.9,U2A.	710	340	2C	[Pg1,2]
10	RELOAD	OffPage	PAGE2	2	SCHMATIC1	U1.9,U2A.	210	300	4C	[Pg1,2]
11										

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After generating intersheet references, the tool generates the two output files (as shown in the accompanying illustration).

You can add and delete intersheet references using the **Tools – Annotate** command.

You can use the **Delete Intersheet References** option in the Annotate window to delete all intersheet references while annotating the design.

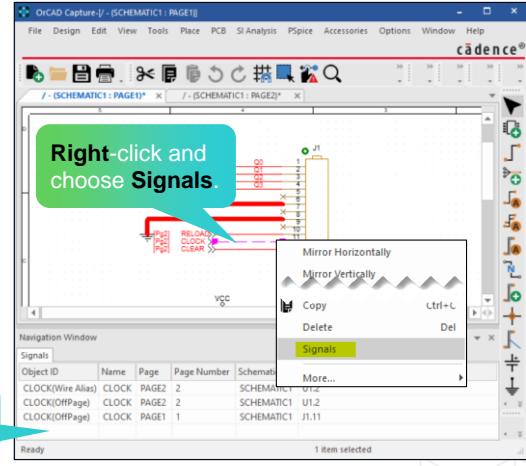
Navigating Nets in the Design



Tracing a signal through a multi-sheet schematic can be helpful when checking connectivity or debugging an error.

- Use the **Signals** command on the right mouse pop-up menu to search for all instances of a selected net in the design.
 - For example, select the CLOCK net, right-click and choose **Signals**.
- All instances of the CLOCK net are displayed in a Navigation window, which you can use to visit each instance of the net in the design.

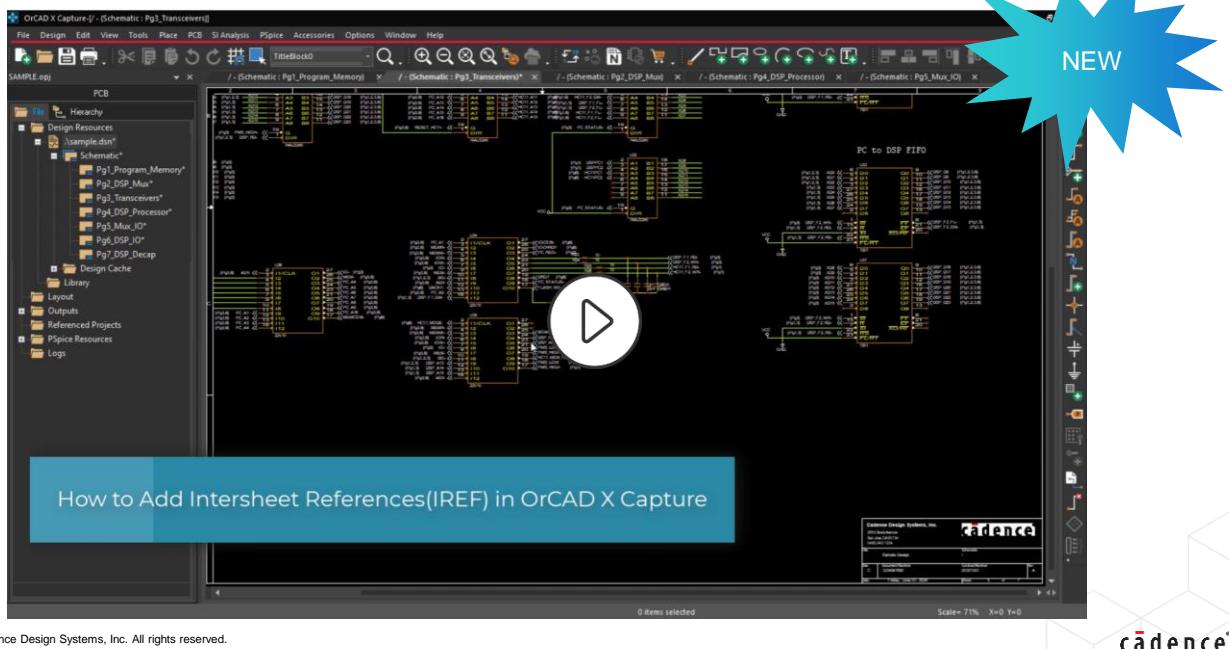
Navigation window



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Use the **Signals** command on the right mouse pop-up menu to search for all instances of a selected net in the design. The search results are displayed in a Navigation window, which you can use to visit each instance of the net in a flat or hierarchical design.

Demo: Adding Intersheet References (IRef) and Navigating Signals



Video Play Time: **3.56** minutes

Click the Play button to start the video.



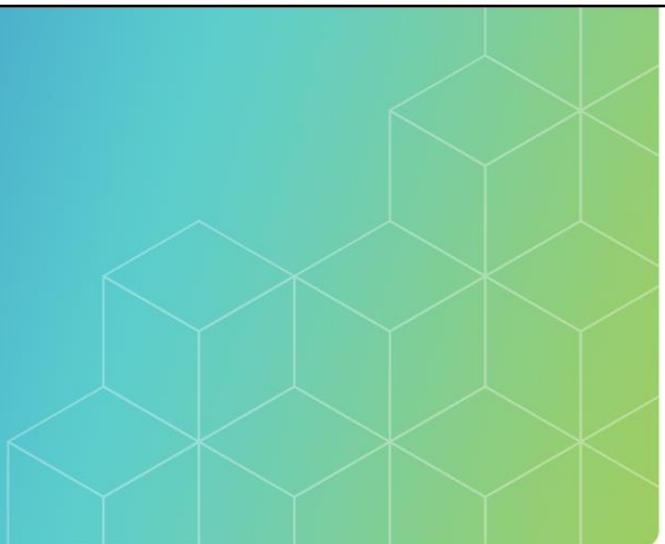
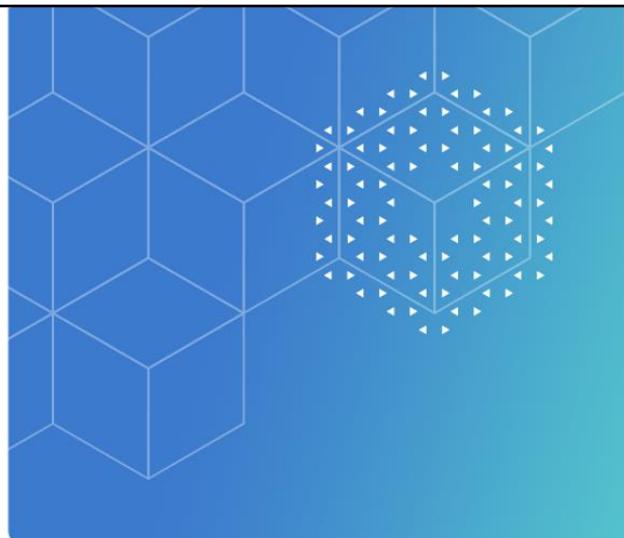
Labs

- Lab 6-1 Creating a New Project
- Lab 6-2 Creating Page1
- Lab 6-3 Copying from One Design to Another
- Lab 6-4 Completing the Schematic
- Lab 6-5 Annotating a Multi-Sheet Design
- Lab 6-6 Checking the Design for Errors
- Lab 6-7 Cross Referencing Multi-Sheet Nets
- Lab 6-8 Searching for Objects in the Schematic
- Lab 6-9 Modifying Wire Attributes

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You will now have the opportunity to perform some self-paced labs to reinforce the ideas presented in this module.



Module 7

Editing Part Properties

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Welcome to Module 7: Editing Part Properties.

Module Objectives

In this module, you

- Use the Property Editor to add part properties
- Use filters to control what is displayed in the Property Editor
- Use the Search toolbar
- Use different text files to modify part and net properties
- Create a custom Bill of Materials
- Generate a netlist for PCB design

Introduction to OrCAD X Capture

Setting Up Your Environment

Working with Libraries

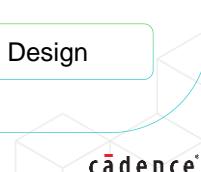
Building a Simple Schematic

Building a Multi-Sheet Schematic

Editing Part Properties

Building a Hierarchical Design

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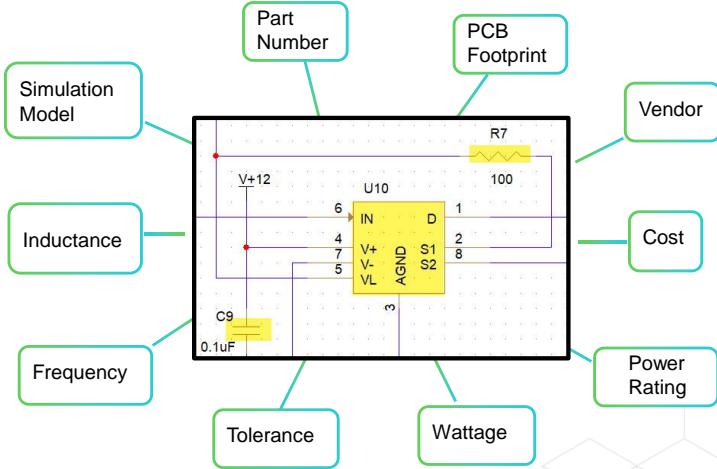
This is where you are in the course flow.

Part Properties



Depending upon the type of device (discrete, analog, digital, IC), some parts need more properties than others.

Each part in the design needs certain properties defined. These properties support design processes like simulation and PCB layout, as well as the purchasing of materials for production.



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Each part in the design needs certain properties defined. These properties support design processes like simulation and PCB layout, as well as the purchasing of materials for production.

For example, every part needs a PCB footprint and a company part number. Depending upon the type of device (discrete, analog, digital, IC), some parts need more properties than others.

Some part properties can be defined in the library. In an earlier module, you assigned PCB Footprint and Part Number properties as part of the library development process.

Accessing the Property Editor from the Schematic Window



Select a part and choose **Edit – Properties**.

Or press the **Ctrl+E** shortcut key.

Or **double-click** on a part.

Or press the **Enter** key.

Use the Property Editor to add, delete, or modify properties for parts, wires, and text.

You can also use the right mouse button to launch the Property Editor on a selected part(s) in the schematic window.

	Part Reference	PART_NUMBER	PCB Footprint	Power Pins Visible	Primitive	Reference	ROOM	Source Library	Source Package	Source Part	Value	VENDOR	
1	SCHEMATIC1 : PAGE2 : U1	U1	20-67890	DIP16	<input type="checkbox"/>	DEFAULT	U1	DATA	C:\CADENCE\ISPB_17.4...	74F162	74F162.Nor	74F162	ABC CO

The Property Editor window lets you add, delete, or modify properties for parts, wires, and text. To access the Property Editor, click on an object, **right-click** and select **Edit Properties**. You can also **double-click** on the part, wire, or text.

Null Versus Blank Property Values

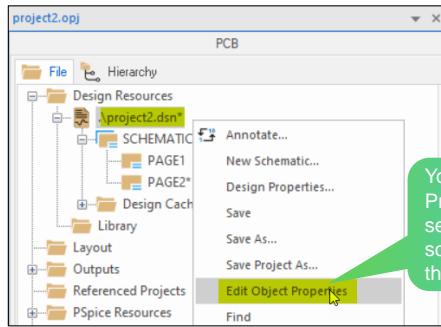
When a cell in the spreadsheet displays a pattern of diagonal lines, that means the property has a null (or no) value. When a cell in the spreadsheet is completely empty, that means the property has a blank value.

To set a property value to *null*, meaning no value, select the property value cell in the spreadsheet and click the **Delete Property** button. If you use the **Delete** or **Backspace** keys to clear a property value from a cell, then the selected property will have a blank value instead of a no (null) value.

Accessing the Property Editor from the Project Manager



Select an object in the Project Manager window and choose **Edit – Object Properties** or use the right mouse pop-up menu.



You can launch the Property Editor on a selected page, schematic folder, or the entire design.

	A	B	C	D	E
CLASS	SCHMATIC1 : PAGE1	SCHMATIC1 : PAGE1	SCHMATIC1 : PAGE1	SCHMATIC1 : PAGE2	SCHMATIC1 : PAGE2
Color	Default	Default	Default	\$5.86	Default
COST	CAP_0.1uF	CAP_0.1uF	HEADER 12 PIN		\$1.20
DESCRIPTION					IC 74LS00
Designator					A
Graphic	CAP Normal	CAP Normal	HEADER 12.Normal	74F162.Normal	74L500.Normal
ID					
Implementation					
Implementation Path					
Implementation Type	<none>	<none>	<none>	<none>	<none>
Location X-Coordinate	250	330	370	340	530
Location Y-Coordinate	370	370	120	200	330
Name	IN5157	IN5173	IN587	IN53928	IN51050
Part Reference	C1	C2	J1	U1	U2A
PART_NUMBER	SMC_6032	SMC_6032	HEADER12	40-98743	20-12345
PCB Footprint					SOIC14
Power Pins Visible	✓	✓	✓	✓	✓
Primitive	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
Reference	C1	C2	J1	U1	U2
ROHM					
Source Library	C:\CADENCE\SPB_17.4	C:\CADENCE\SPB_17.4	C:\CADENCE\SPB_17.4	C:\CADENCE\SPB_17.4	C:\CADENCE\SPB_17.4
Source Package	CAP	CAP	HEADER 12	74F162	74L500
Source Sheet	CAP.Normal	CAP.Normal	HEADER 12.Normal	74F162.Normal	74L500.Normal
Value	0.1uF	0.1uF	HEADER 12	74F162	74L500
VENDOR				ACME INC	Digi-Key

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Use tabs to filter the property table by object type.

You can launch the Property Editor on a page (or set of pages) you have selected in the Project Manager window. You can also do this for a selected schematic folder or the entire design.

Use the tabs along the bottom of the window to filter the property table by object type. For example, use the Title Blocks tab to change the Rev Code on all pages of the design.

Pivoting and Filtering the Property Spreadsheet



Pivoting the property spreadsheet in the Property Editor makes it easier to find the property name you want to edit for the selected part.

You can also filter the property spreadsheet to load just the properties contained in a custom property list and filter all other properties out of the table.

1. Click the **Pivot** button in the Property Editor to display property names as rows instead of columns.
2. Click in the **Filter by** field to pick a specialized property list known as a 'filter'.

	A	Schematic1 : Page2 : U1
NO_SWAP_GATE		
NO_SWAP_GATE_EXT		
NO_SWAP_PIN		
PART_NUMBER	20-67890	
PCB_Footprint	DIP16	
PIN_ESCAPE		
PINUSE		
PLACE_TAG		
POWER_GROUP		
Power Pin Visible	Primitive	DEFAULT
RATED_MAX_TEMP		
REFERENCE		U1
REUSE_INSTANCE		
REUSE_MODULE		
ROOM		DATA
SIGNAL_MODEL		C:\CADENCE\ISPB_17.4\TOOL
Source Library		
SWAP_GROUP		
T_TEMPERATURE		
TOL		
VALUE		74F162
VOLTAGE		
propagation_delay		
VENDOR		ABC CO

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By default, the Property Editor displays a spreadsheet with the selected object(s) along the left side (as rows) and a list of properties across the top (as columns). You can pivot the spreadsheet to display the properties as rows and the selected object(s) as columns (as shown in the accompanying illustration).

When the spreadsheet is pivoted with property names as rows, the **New Column** button becomes the **New Row** button (see illustration).

Use the *Filter by* field at the top of the Property Editor window to load just the properties in a custom property list and filter all other properties out of the table. Each property list has a name and is known as a 'filter.' All filter names are displayed in the *Filter by* field. Select a filter name to switch from one property list to another.

The properties in the Cadence-supplied filters target specific design tools. For example, there is a property list called OrCAD® PCB Designer Standard and Allegro PCB Designer.

The **<Current properties>** filter lists all properties currently assigned to the selected object(s). Think of this setting as having no custom property list loaded and no filtering applied to the spreadsheet.

Searching for Different Objects

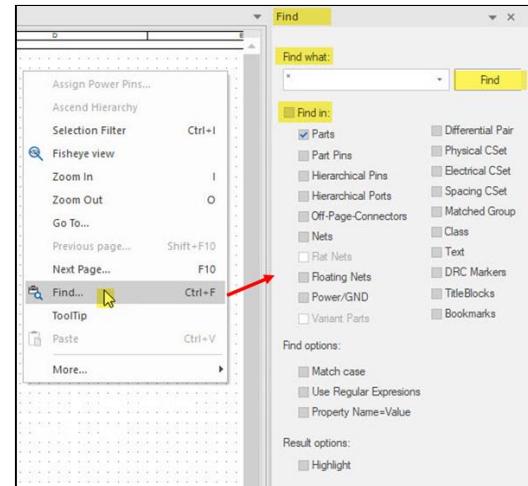


Use the Find tab to search for different types of objects in the design.

You can apply the search to an active schematic window or to your selection in the Project Manager – design, folder, or page(s).

To find objects:

1. Choose **Edit – Find** or right-click on the window – **Find**.
2. In the **Find tab**, use the object type checkboxes to restrict the search – for example, to target just parts or nets.
3. Use the **Find what** field to refine the search to a specific part or net.



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Use the Find tab to search for different types of objects in the design.

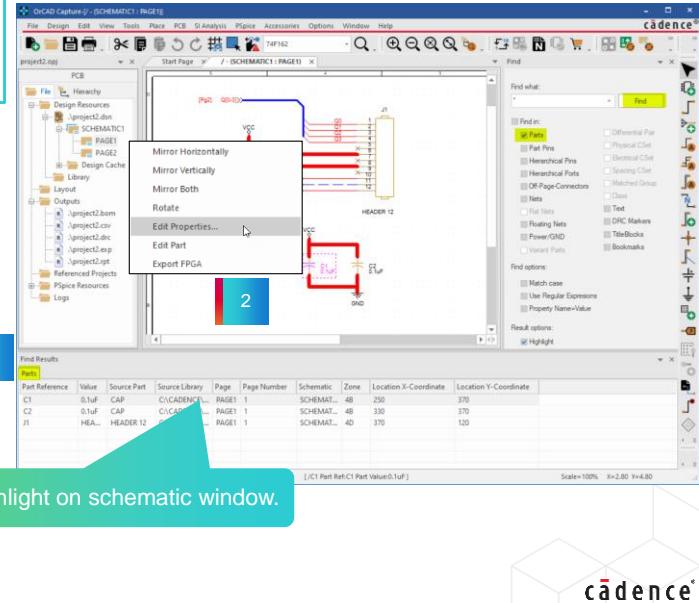
You can apply the search to an active schematic page or to your selection in the Project Manager – to the whole design, a schematic folder, or selected page(s).

Using the Find Results Window



When you click **Find**, the search results are displayed in the Find Results window.

1. Click in the Find Results window to navigate to objects in the design.
2. Once selected, you can use the right mouse pop-up menu to start the Property Editor.



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Search results are displayed in a Find window along the bottom of the session window (you can reposition the Find window anywhere you like).

When you select an object in the Find window, Capture navigates to and selects the object in the design. Once selected, you can use the Property Editor to modify its properties.

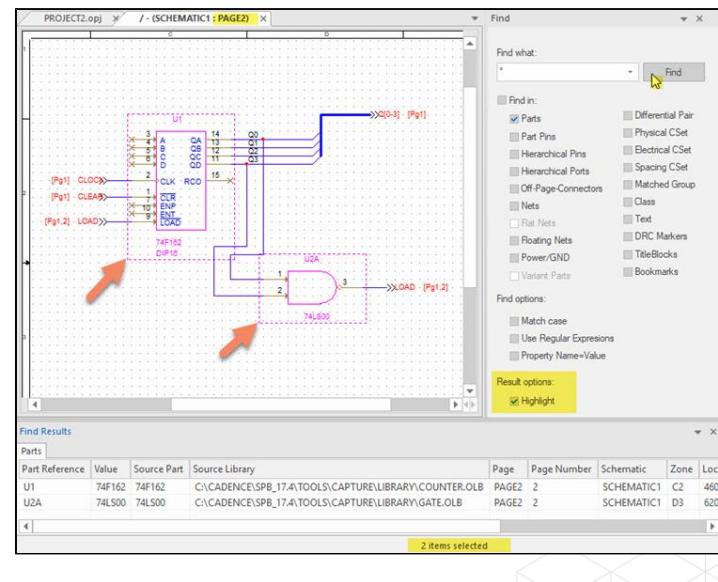
Using the Search Highlight Option in an Active Page



When you apply a search to an active schematic page window, you can select the **Highlight** option in the Find tab.

All objects on the active page that match your search criteria are automatically highlighted and selected so you can then invoke the Property Editor on the selected set.

1. Click **Edit – Find**.
2. In the Find tab, under Result options, click the **Highlight** checkbox.
3. Click **Find**.



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When you apply a search to an active schematic page window, you can select the **Highlight** option in the Find tab.

All objects on the active page that match your search criteria are automatically highlighted and selected, so you can then invoke the Property Editor on the selected set.

Using the Browse Spreadsheet for Multiple Object Editing



Sometimes, you may need to make the same property edit to many objects in the design.

For example, you need to change the Revision level in the title blocks on all pages of the design.

1. Use the **Find** tab to search for objects like Title Blocks or Off-Page Connectors or any object.
2. Then make multiple selections in the Find Results window and select **Edit Properties** to edit them at once in a Browse Spreadsheet.

	OrgAdd2	RevCode	Doc	OrgAdd3	OrgName
1	San Jose, CA.	B	CDS-12345		Cadence
2	San Jose, CA.	B	CDS-12345		Cadence

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You can make multiple selections in the Find Results window, then select **Edit Properties** to edit them at once in a Browse Spreadsheet window. For example, you can search for objects like Off-Page Connectors or TitleBlocks, then load them into the Browse Spreadsheet for editing.

With one or more objects selected in the Find window, you can use the right mouse pop-up menu to save the selected set to an HTML or CSV format file.

Changing a Net Name Throughout the Design

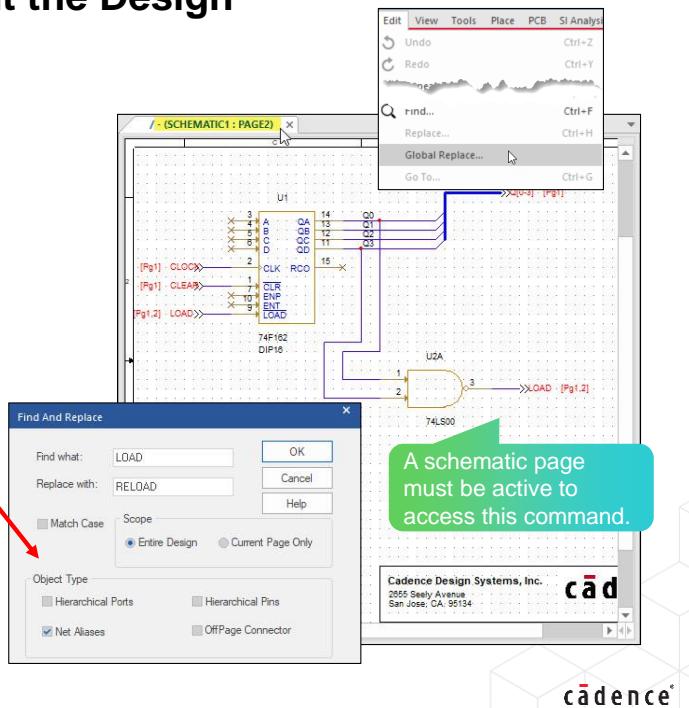


Choose **Edit – Global Replace**.

Use this command to locate and replace text properties associated with net names and other object types in the schematic editor.

For example, select the **Net Aliases** checkbox under Object Type and enter the old and new net names to replace a net alias with a new alias on the current page or across the entire design.

You cannot use this command to replace a part with another part.



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Choose **Edit – Global Replace** to change the name of a net throughout a design. You cannot use this command to replace a part with another part. Wildcards are not supported in this menu. A schematic window must be active to access this command.

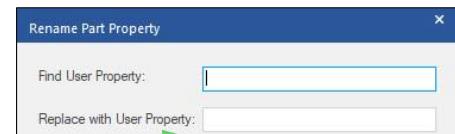
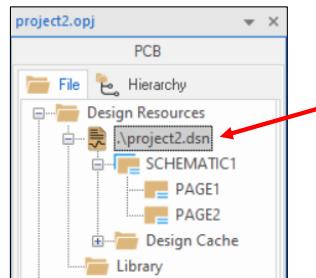
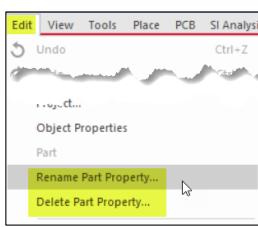
Renaming or Deleting a Part Property Throughout the Design



Choose **Edit – Rename Part Property**.

Choose **Edit – Delete Part Property**.

When a schematic page, folder, or design is selected in the Project Manager window, the Edit pull-down menu contains some unique commands.



Use this command to rename a part property for every placed part that includes the property for an entire design.



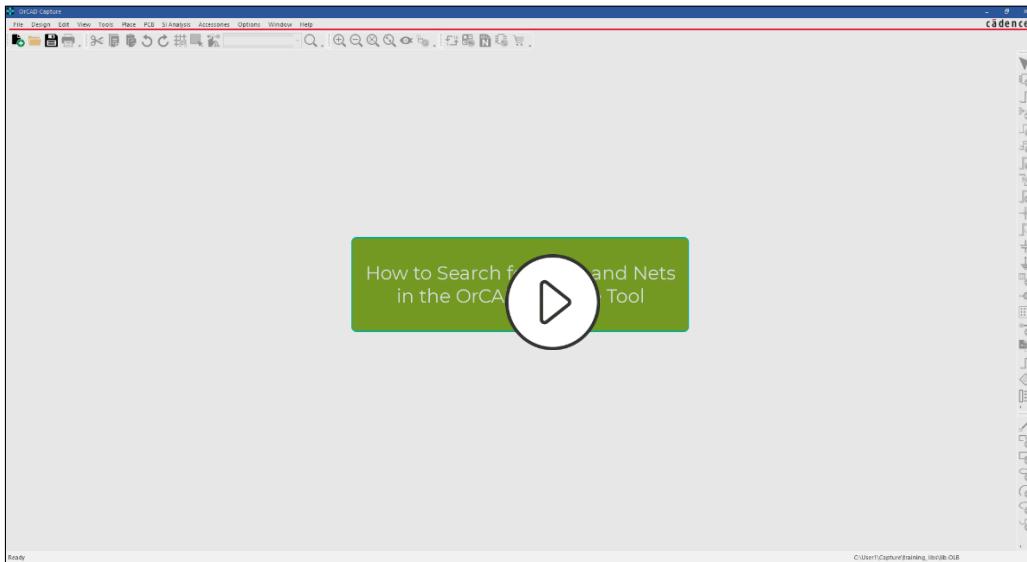
Use this command to remove a part property from the design.



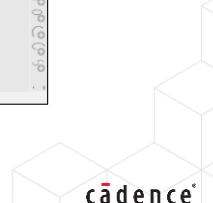
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When the Project Manager window is active, the **Edit** pull-down menu contains some commands not available elsewhere. For example, you can use the **Edit** pull-down menu to rename or delete a user-defined property on the selected page(s), schematic folder, or the entire design.

Demo: Searching for Parts and Nets



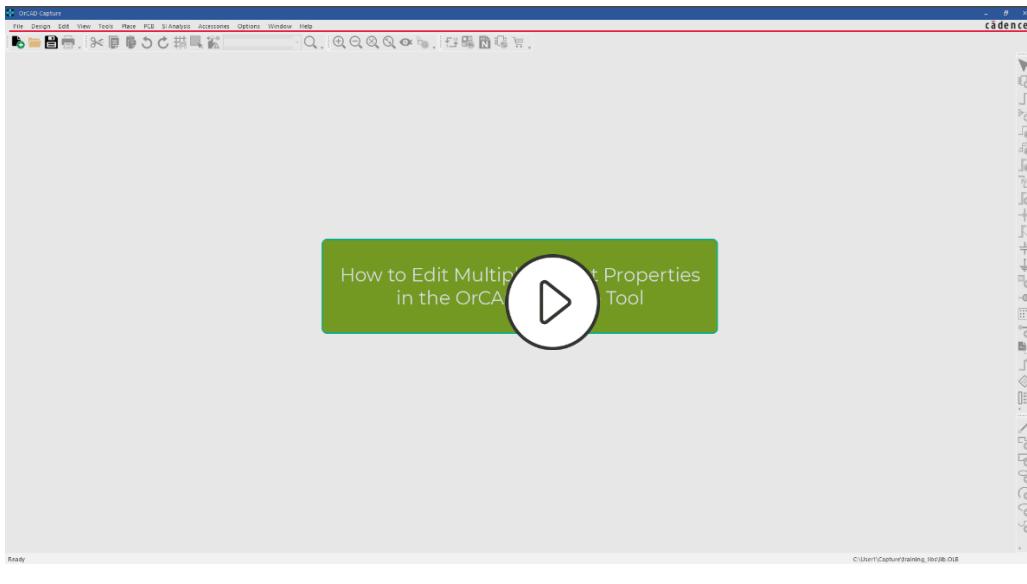
142 © Cadence Design Systems, Inc. All rights reserved.



Video Play Time: 4.50 minutes

Click the Play button to start the video.

Demo: Editing Multiple Object Properties



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Video Play Time: 3.40 minutes

Click the Play button to start the video.

Using Text Files to Edit Properties

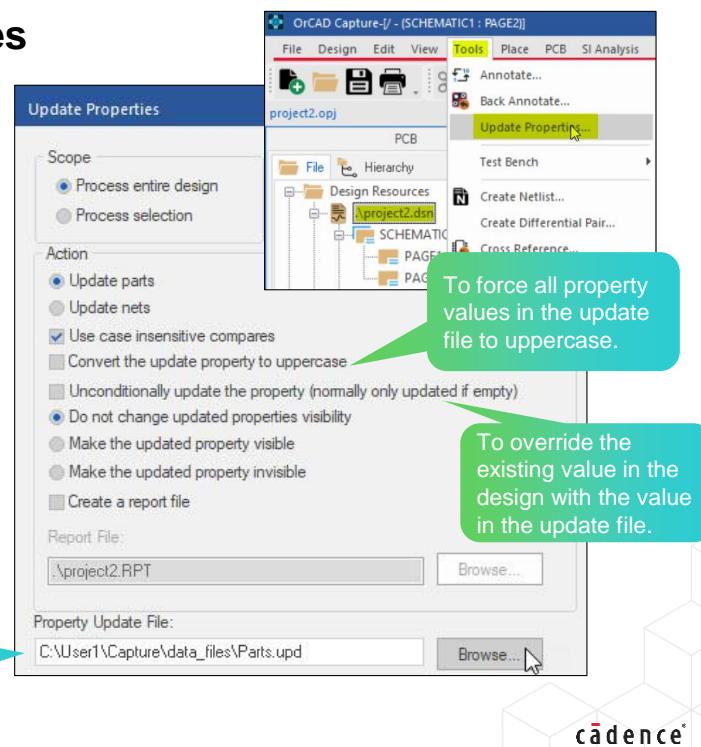


Choose Tools – Update Properties.

You can automate the property editing process by loading a tab-delimited text file containing property assignments into the design.

You can apply the update process to the entire design or just the selected object in the Project Manager window.

The update properties file is created with a text editor and has a .upd extension.



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With the Project Manager window active, choose **Tools – Update Properties** to load a text file containing property assignments into a design. You can preselect specific pages in the Project Manager window to control which portions of the design are affected.

Capture compares the property names in the header line of the update file to the property names in the design. This comparison ignores all case differences. If the property is found in the design and it already has an assigned value, no change is made. (By default, an existing value in the design overrides the update file.) A warning message is sent to the session log.

Use the **Unconditionally update the property** option to override the existing value in the design with the value in the update file. Capture updates the property value exactly as shown in the update file. Use the **Convert the update property to uppercase** option to force all property values in the update file to uppercase. This option has no effect on the property names.

When a property is in the update file but is not in the design, the property is always added to the design. The property name is always added exactly as it appears in the header line of the update file. Once the property is added, you cannot change its case.

What Is the Combined Property String?



The first line in an update properties file is the header line, and the first field in the header line is called the **combined property string**. This field contains the key property that selects the object you want to update.

For example, to update parts by type, set the combined property string to <VALUE>.

To update parts by reference (such as U1, R2), use <PART REFERENCE>.

To the right of the combined property string is a list of properties you want to attach or update.

Each of the lines following the header contains values for the combined property string, as well as values for the update properties.

Example
Header
<> "PCB FOOTPRINT" "PART_NUMBER" "VENDOR"
"74LS00" "SOIC14" "CDN_12345" "ABC Co." Value

Use one tab space between each property name or value. Property names are case-sensitive, whereas property values are not.

The Capture tool tries to match the combined property string values in the update file to the property values in the design.

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Header

The first line in the update file is the header line. The first field in the header line is called the *combined property string*. This is the key property that selects the object you want to update.

To the right of the combined property string is a list of updated properties (each property name is quoted). These are the properties you want to attach or update. You can update any part or net property except for part value, part reference, and net name.

Each of the lines following the header contains values for the combined property string, as well as values for the update properties. Each of these lines must have an entry for each of the properties in the header.

Combined Property String

The first field in the header line is called the combined property string. This is the key property that is used to select the object you want to update.

For example, to update a net, the combined property string field should be <NET NAME>. To update parts by reference (such as U1, R2), use <PART REFERENCE>. To update parts by type (such as 74F162, HEADER 12, or 0.1UF), set the combined property string to <VALUE>.

The Capture tool tries to match the combined property string values in the update file to the property values in the design. This comparison is case-sensitive. If the net name in the design is *LOAD* (all uppercase), but the net name in the combined property string field of the update file is *load* (all lowercase), Capture assumes they are different nets. A message is sent to the session log for each line in the update file that doesn't match an object in the design. Turn on the **Use case insensitive compares** option to ignore case differences between the combined property string values in the update file and the property values in the design.

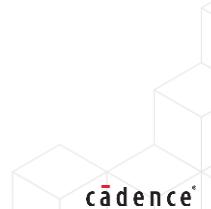
Update Properties (UPD) File: Example

This part properties file will add six properties to parts based on the part names shown in the <VALUE> column.

Each line in the file must have an entry for each of the update properties in the header.

```
"<Value>" "PART_NUMBER" "PCB Footprint" "CLASS" "ROOM" "VENDOR" "COST"  
"741800" "20-12345" "DIP14" "IC" "DATA" "ABC CO" "$1.20"  
"7400" "20-12345" "DIP14" "IC" "DATA" "ABC CO" "$1.20"  
"74F162" "20-67890" "SO16" "IC" "DATA" "ABC CO" "$3.95"  
".1UF" "30-10293" "1206S" "DISCRETE" "CHAN1" "XYZ INC" "$0.75"  
"0.1UF" "30-10293" "1206S" "DISCRETE" "CHAN2" "XYZ INC" "$0.75"  
"HEADER 12" "40-98743" "HEADER12" "IO" "" "ACME INC" "$5.86"  
"12HEADER" "40-98743" "HEADER12" "IO" "" "ACME INC" "$5.86"
```

Use double quotes (as a placeholder) to indicate a null value for that property, or to remove the current value and set it to null.



Things to Remember

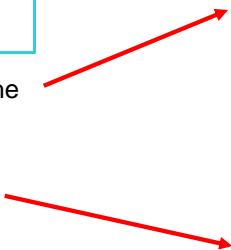
- The update property file is created manually using a text editor.
- The update property file is a tab-delimited file. Do not insert additional tabs or spaces in this file.
- Each line in the file must have an entry for each of the update properties in the header. Use double quotes (as a placeholder) to indicate a null value for that property or to remove the current value in the design and set it to null.

Export, Modify, and Import Properties



You can export existing part properties to a tab-delimited text file and use a spreadsheet editor to add or modify properties in the exported file.

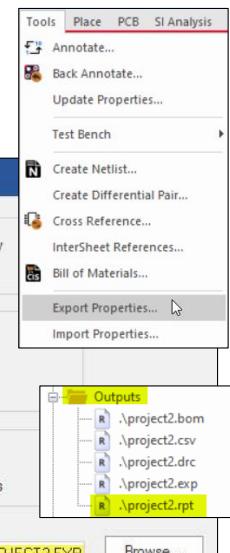
1. Export properties for the whole design or just the object selected in the Project Manager window.
2. Choose **Tools – Export Properties** to export existing part properties to a .EXP file.



Use Excel® to edit the exported file.

	A	B	C	D	E	H	I
1	DESIGN	D:\USER1\CAPTURE\PROJECT2\PROJECT2.DSN			PART_NUMBER	PCB Footprint	Part Ref Power Pins Room
2	HEADER	ID	CLASS	COST	Graphic	J1	FALSE
3	PARTINST:SCHEMATIC1:PAGE2:117	J1	IO	\$5.86	HEADER 12.Normal	40-98743	CONN12
4	PARTINST:SCHEMATIC1:PAGE2:178	C1	DISCRETE	\$0.75	CAP.Normal	30-10293	SM_1206
5	PARTINST:SCHEMATIC1:PAGE2:194	C2	DISCRETE	\$0.75	CAP.Normal	30-10293	SM_1206
6	PARTINST:SCHEMATIC1:PAGE1:1065	U2	IC	\$1.20	74LS00.Normal	20-12345	DIP14
7	PARTINST:SCHEMATIC1:PAGE1:1119	U1	IC	\$3.95	74F162.Normal	20-67890	SOIC16

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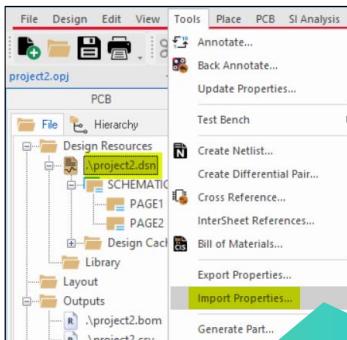


Choose **Tools – Export Properties** to export existing parts or net properties to a tab-delimited text file. The exported file is a table with rows for parts or nets and columns for properties.

Things to remember while exporting the files:

- The first row of the file identifies the source of the file as either a design or a library. Do not change or delete this row.
- In each of the part or net rows following the Header line, the first two fields in these lines contain a keyword and an identifier. Do not change or delete these first two fields, as this information is used to locate the part or net to be updated when the file is imported back in.
- When adding new information, don't skip over any columns. Enter “” as a null value placeholder instead.

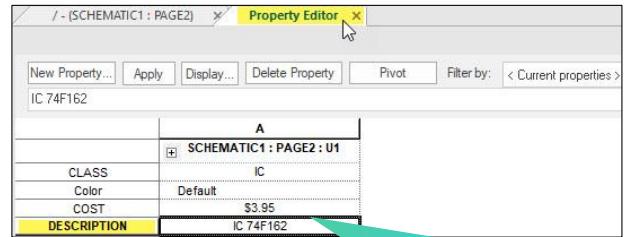
Import Properties



Use this command to reload the modified .EXP file back into the design after editing in Excel.

DESCRIPTION	PART_NUMBER	PCB Footprint	Part Ref
HEADER 12 PIN	40-98743	CONN12	J1
CAP_0.1uF	30-10293	SM_1206	C1
CAP_0.1uF	30-10293	SM_1206	C2
IC 74LS00	20-12345	DIP14	U2A
IC 74F162	20-67890	SOIC16	

In this example, a new property DESCRIPTION is added to .EXP file in Excel.



After importing the modified .EXP file, the new DESCRIPTION property, is shown in the Property Editor on a part in the design.

Choose **Tools – Import Properties** to reload the modified file back into the design.

In this example, a new property DESCRIPTION is added to .EXP file in Excel. After importing the modified .EXP file, the new DESCRIPTION property, is shown in the Property Editor on a part in the design.

Generating a Bill of Materials (BOM) Report



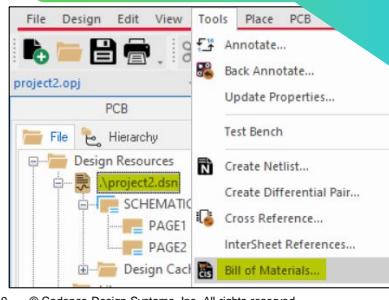
Choose Tools – Bill of Materials.



Here, you can add a custom header and property value.

A BOM is a list of all the assembly items needed for your design.

A standard BOM contains Item, Quantity, Part Reference, and Part Value columns.



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PROJECT2.BOM			
A	B	C	D
CDS-12345	Revision: A		
5	Cadence Design Systems, Inc.		
6	2655 Seely Road		
7	San Jose, CA, 95134		
8	Bill Of Materials	Page1	
10	Item	Quantity	Reference
11			Part
13	1	2 C1	0.1uF
14		C2	0.1uF
15	2	1 J1	HEADER 12
16	3	1 U1	74F162
17	4	1 U2	74LS00

To add Additional Property.

Bill of Materials

Scope: Process entire design
Mode: Use instances (Preferred)

Line Item Definition

Header: Item\Quantity\Reference\Part

Property value format: {{Item}}\{{Quantity}}\{{Reference}}\{{Value}}

Place each part entry on a separate line

Include File

Report: Report File: View Output! JSER1\CAPTURE\PROJECT2\PROJECT2.BOM

Outputs: \project2.bom, \project2.csv

Choose **Tools – Bill of Materials** to create a Bill of Materials (BOM) report. The company name and address at the top of the report come from the title block.

The BOM report is a delimited text file. Use the *Open in Excel* option to load the BOM output file into Microsoft Excel.

Use the **Include File** option to attach additional properties in a text file to parts in the design. You can also create non-electrical parts, such as screws, washers, or sockets, that will appear in the BOM report but not in the netlist.

An empty field in the BOM report indicates one of the following:

- The property was not attached to that part.
- The property was attached to the part, but its value was null for that part.
- The property name you specified in the Combined property string field does not match the property name attached to the part in the design.
- In an include file, you specified the property for a part that is not in the design.

What Is a Custom BOM?



A custom BOM includes additional columns of information needed by your company.

The additional columns in the BOM report contain company-specific data required to properly document the parts for assembly.

Displayed using the *Open in Excel* option.

PROJECT2.BOM							
A	B	C	D	E	F	G	H
1 Project2 Revised:							
2 CDS-12345	Revision: A						
3							
4 Cadence Design Systems, Inc.							
5 2655 Seely Road							
6 San Jose, CA. 95134							
7							
8 Bill Of Materials	Page1						
9							
10 Item	Quantity	Reference	Part	PCB Footprint	PartNumber	Supplier	Cost
11							
12 1	2	C1	0.1uF	SM_1206	30-10293	XYZ INC	\$0.75
13		C2	0.1uF	SM_1206	30-10293	XYZ INC	\$0.75
14 2	1	J1	HEADER 12	CONN12	40-98743	ACME INC	\$5.86
15 3	1	U1	74F162	SOIC16	20-67890	Digi-Key	\$3.95
16 4	1	U2	74LS00	DIP14	20-12345	Digi-Key	\$1.20

Custom Header and property value add it in the choose Tools – Bill of Materials tab.

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A custom BOM includes additional columns of information needed by your company to properly document the parts required for assembly.

This is a sample of a customized BOM report. This custom BOM includes additional columns for PCB Footprint, Part Number, Supplier, and Cost.

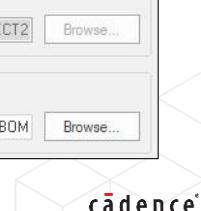
Creating a Custom Bill of Materials



Creating a custom BOM involves the use of the Header and Combined property string fields in the Bill of Materials form.

1. Choose Tools – Bill of Materials.
2. In the Header field, **specify** a line of titles to be used as column headers for the columns of data you plan to have in your custom report.
 - These are simply the user-defined titles you want at the top of each column.
3. In the Combined property string field, **define** which design properties load into which columns of the report (under the titles you defined in the Header field).
 - This field is considered an *extractor*. You can list any part property in the Combined property string field and extract that information into the report.

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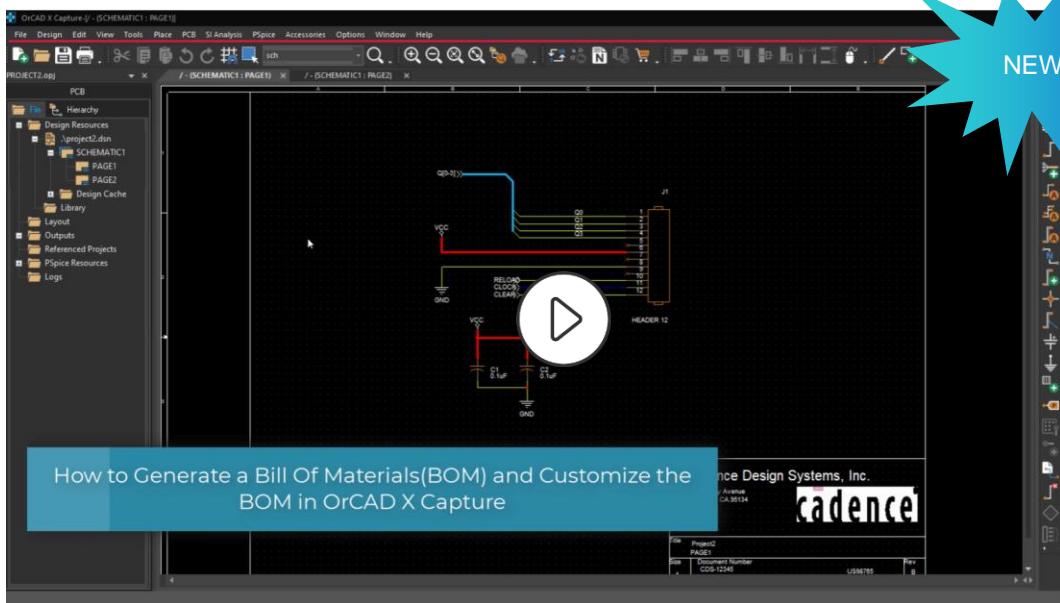
Use the Header and Combined property string text boxes to customize the BOM.

In the **Header** field, The `\t` inserts a tab between fields of data in the BOM report for both the Header line and the property string line.

In the **Combined property string** field, the property names must be enclosed in curly braces `{ }` and must match the property names on the parts in the design (not case-sensitive).

Use **Options – Preferences – Text Editor** to increase tab settings in the report.

Demo: Generating a Bill of Materials (BOM) and Customizing the BOM



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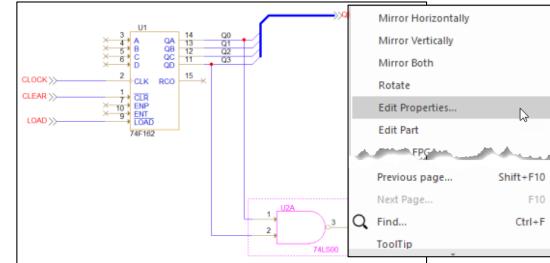
Video Play Time: **2.38** minutes

Click the Play button to start the video.

How to Exclude Parts from the Capture BOM

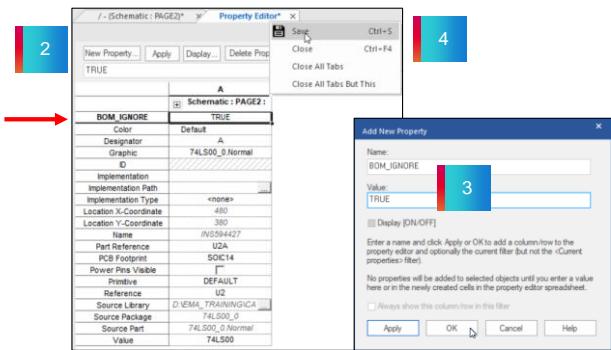


You can exclude a part from the Bill of Materials (BOM), by defining a "BOM_IGNORE" property and assigning it the value as "TRUE"



To exclude the part from the BOM:

1. Right-click on the Part and choose **Edit Properties** or double-click on the part.
2. In the Property Editor window, click On **New Property**.
3. Specify the Name **BOM_IGNORE** property with the value **TRUE**.
4. Save and close the properties.



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To exclude a component from the Bill of Materials (BOM), right-click on the respective part and select **Edit Properties** or double-click on the part. Within the Property Editor window, click on **New Property** to add a new property. Then, specify the name as **BOM_IGNORE** and the value as **TRUE**. Click **OK** to add the property in the property editor window. Save and subsequently close the Property Editor window.

How to Exclude Parts from the Capture BOM (continued)

5. Choose Tools – click on Bill of Materials.
6. Click OK to generate the BOM.

The screenshot illustrates the workflow for generating a Bill of Materials (BOM) in Cadence Capture. It shows the Tools menu open with 'Bill of Materials...' selected, the 'Bill of Materials' dialog box, and two versions of the BOM report: 'BEFORE' and 'AFTER'.

Tools Menu:

- Scope: Process entire design (selected)
- Mode: Use instances (Preferred)
- Header: Item/(Quantity)/Reference\Part
- Combined property string: (Item)/(Quantity)/(Reference)/(Value)
- Place each part entry on a separate line (unchecked)
- Include File: Merge an include file with report (unchecked)
- Combined property string: (Item)/(Quantity)/(Reference)/(Value)
- Include file: D:\EMA TRAINING\CAPTURE\INTRO\INTRO
- Report: View Output (checked)
- Report File: D:\User\VCapture\Intro\INTRO.BOM

BEFORE Report Content:

Intro Design Revised: Monday, June 24, 2024
1234567890 Revision: A

Cadence Design Systems, Inc.
2655 Seely Avenue
San Jose, CA 95134
(408) 943 1234

Bill Of Materials June 24,2024 Page1

Item	Quantity	Reference	Part
1	1	U1	74F162
2	1	U2	74LS00

AFTER Report Content:

Intro Design Revised: Monday, June 24, 2024
1234567890 Revision: A

Cadence Design Systems, Inc.
2655 Seely Avenue
San Jose, CA 95134
(408) 943 1234

Bill Of Materials June 24,2024 Page1

Item	Quantity	Reference	Part
1	1	U1	74F162

Legend:

- Number 5: Points to the 'Bill of Materials...' option in the Tools menu.
- Number 6: Points to the 'OK' button in the Bill of Materials dialog box.

After setting the BOM_IGNORE property in the property editor window, navigate to the Tools menu and select Bill of Materials. Click OK to generate the BOM. Notice that the specified component will be excluded from the generated BOM report.

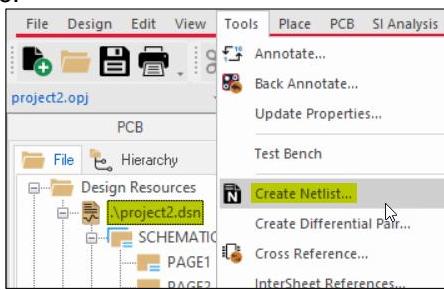
Creating a Netlist for PCB Layout



Choose Tools – Create Netlist.

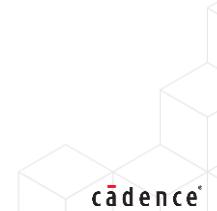
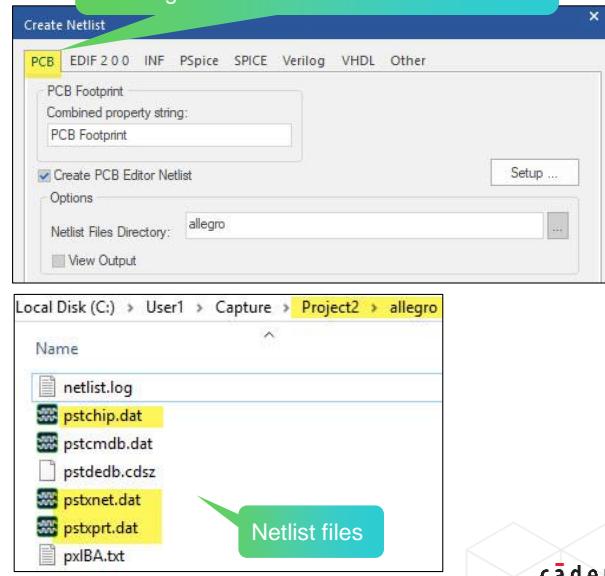


These netlist files contain all the parts and connectivity defined in the schematic. This information is required to begin the board layout process using Allegro® X PCB Editor and OrCAD X Presto.



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Click the **PCB** tab to generate netlist files for the Allegro X PCB Editor/OrCAD X Presto.



Choose **Tools – Create Netlist** and click the **PCB** tab to generate netlist files for Allegro X PCB Editor and OrCAD X Presto. These netlist files contain all the parts and connectivity defined in the schematic. This information is required to begin the board layout process using Allegro X PCB Editor and OrCAD X Presto.

Cadence provides a configuration file `<install directory>/tools/capture/allegro.cfg` that controls which part and net properties are extracted from the Capture schematic and added to the netlist.



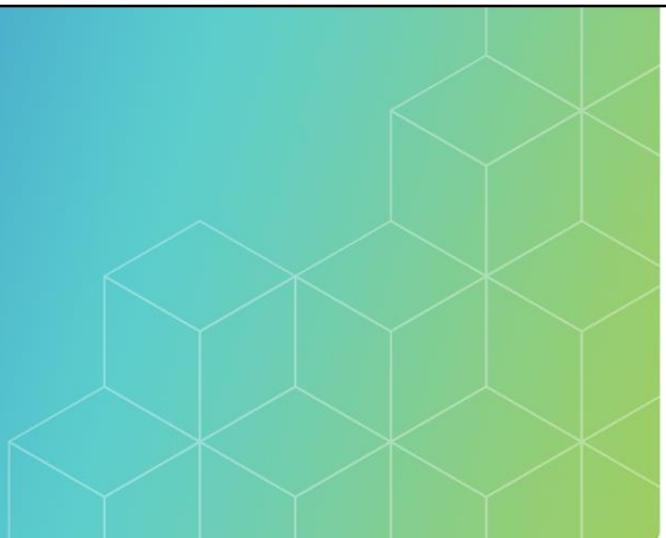
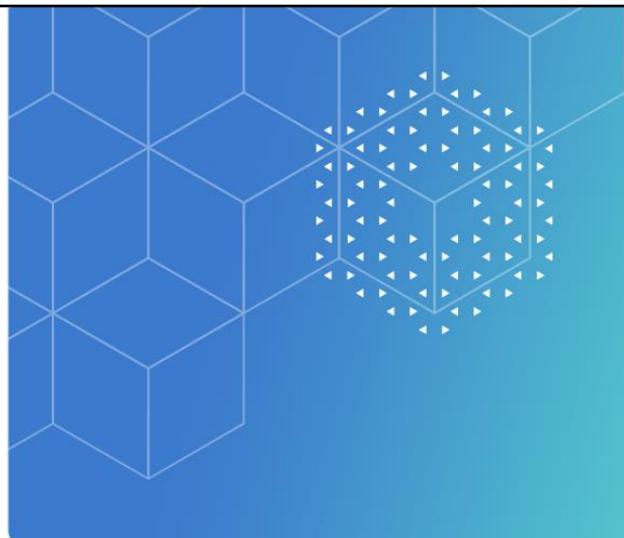
Labs

- Lab 7-1 Using the Property Editor
- Lab 7-2 Using the Allegro X PCB Designer Property Filter
- Lab 7-3 Using an Update Properties File
- Lab 7-4 Using an Export/Import Properties File
- Lab 7-5 Multiple Object Editing with the Browse Spreadsheet
- Lab 7-6 Creating a Bill of Materials Report
- Lab 7-7 Creating a Netlist for Allegro X PCB Editor/OrCAD X Presto

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You will now have the opportunity to perform some self-paced labs to reinforce the ideas presented in this module.



Module 8

Building a Hierarchical Design

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Welcome to Module 8: Building a Hierarchical Design.

Module Objectives

In this module, you

- Describe the structure of a hierarchical design
- Copy a schematic folder from another project and create a hierarchical block
- Use port symbols to connect blocks to their lower-level schematics
- Annotate a hierarchical design
- Run a design rules check on a hierarchical design
- Add intersheet references to a hierarchical design
- Generate a netlist for Allegro® X PCB Editor and OrCAD® X Presto
- Copy and rename an existing project

Introduction to OrCAD X Capture

Setting Up Your Environment

Working with Libraries

Building a Simple Schematic

Building a Multi-Sheet Schematic

Editing Part Properties

Building a Hierarchical Design



This is where you are in the course flow.

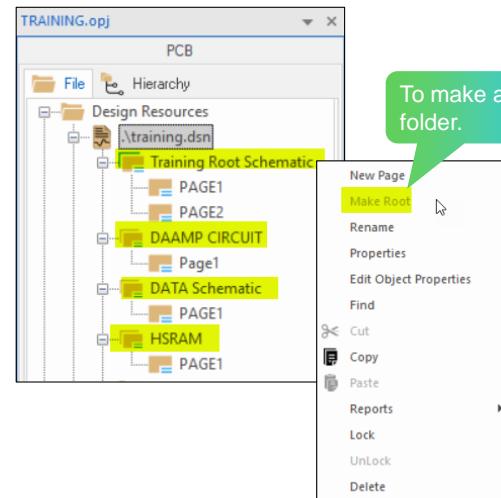
What Is a Hierarchical Design?



When you embed a schematic folder inside another schematic folder, you've created a hierarchical design.

When viewed in Project Manager, a hierarchical design will have two or more schematic folders.

- Flat designs have only one schematic folder.
- Use a hierarchical block symbol to embed one schematic folder into another.
- Each hierarchical block symbol on a schematic page represents an embedded schematic folder.
- The root schematic represents the top of the hierarchy and is displayed in the Project Manager window.



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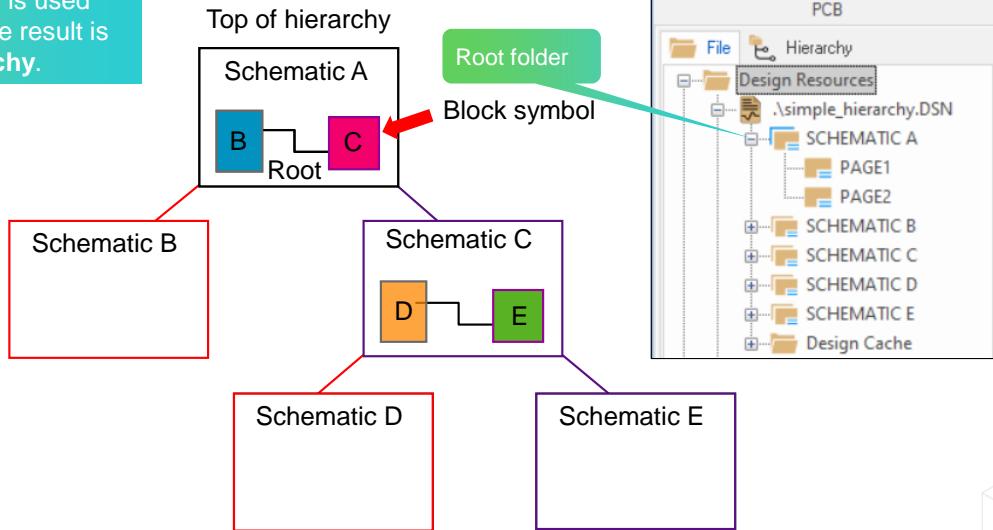


In flat designs, all the schematic pages are at the same level (in the same schematic folder). Signals leave one page and enter another through the use of off-page connectors.

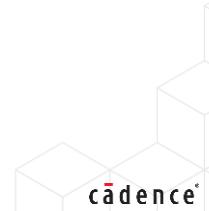
By contrast, hierarchical designs have two or more schematic folders. One schematic folder can be embedded into another using a hierarchical block symbol.

Example 1: Simple Hierarchy

When the block symbol is used once in a schematic, the result is called a **simple hierarchy**.



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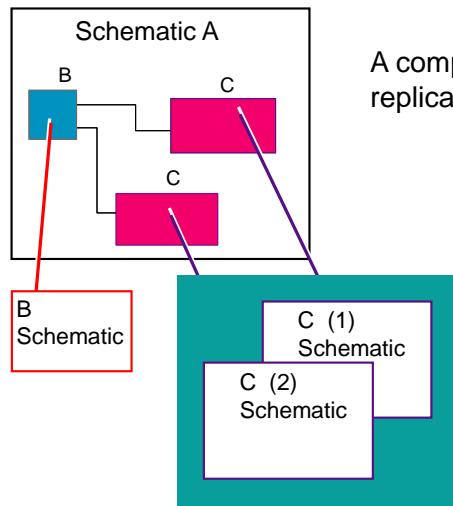
When you embed a schematic folder inside another schematic folder, you've created a hierarchical design. The process requires a block symbol, which represents a schematic or functional model. When the block symbol is used once in a schematic, the result is called a simple hierarchy (shown in the accompanying diagram).

The root schematic represents the top of the hierarchy and is displayed in the Project Manager window.

A hierarchical design has several advantages. Its block diagram structure shows how the functional units interact, and each block can be reused in other designs.

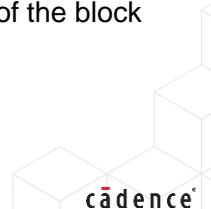
Example 2: Complex Hierarchy

When the block symbol is used two or more times, the design is called a **complex hierarchy**.



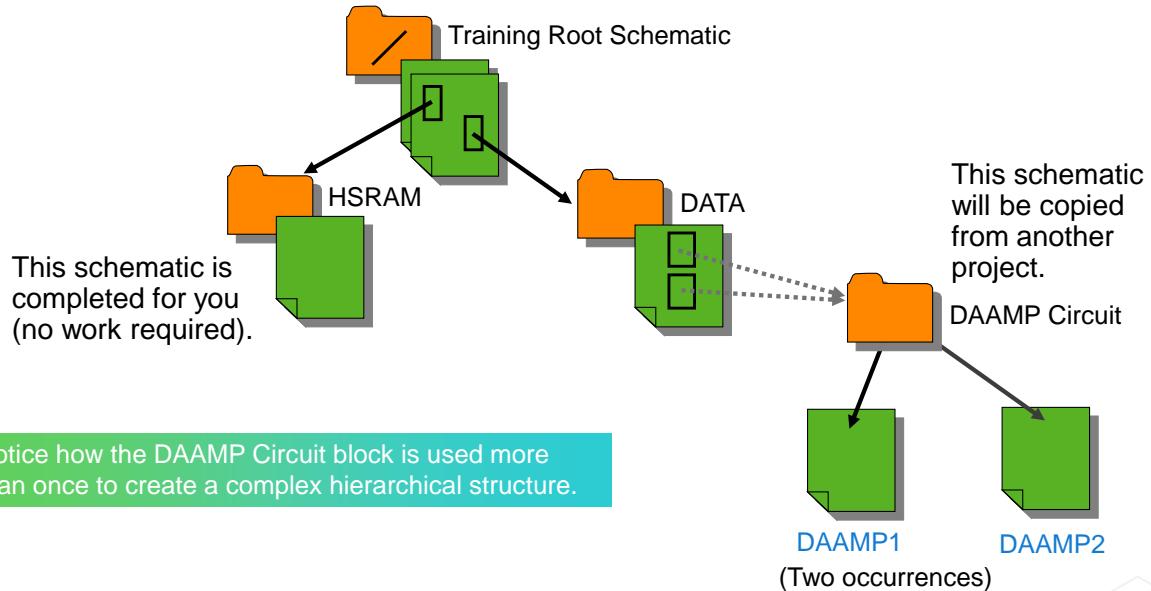
A complex hierarchy contains replicated blocks.

Capture automatically maintains multiple copies of the schematic in its database, one for each occurrence of the block symbol.



In a complex hierarchical design, Capture automatically maintains multiple copies of the schematic in its database, one for each instantiation of the block symbol. When you edit a block, all instances of the replicated block are changed throughout the hierarchical design.

Example 3: Your Existing Training Project



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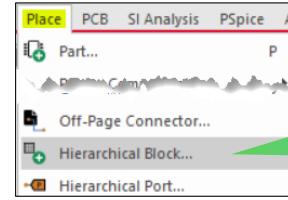


This illustration provides an overview of the hierarchical design used in an upcoming lab session.

Placing a Hierarchical Block



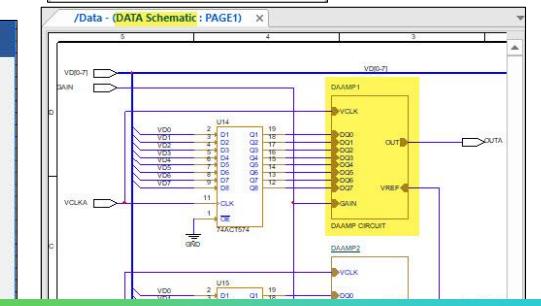
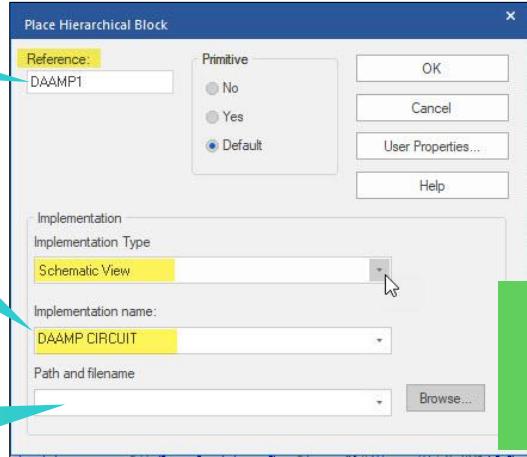
Choose Place – Hierarchical Block.



Name of the block symbol.

Name of the schematic folder.

Path to design (external reference only).



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Use the **Place – Hierarchical Block** command to add a block symbol to a schematic.

Use the *Reference* field to specify the name of the block symbol. This is like a reference designator for the block instance and will be used to identify it from other blocks in the hierarchy.

Use the *Implementation Type* field to specify what the block symbol represents (schematic, VHDL, or PSpice® model).

The *Implementation name* field contains the name of the schematic folder.

Instead of copying a schematic folder between projects, you can place a hierarchical block and use the *Path and filename* field to link the block symbol to the design that contains the schematic folder it represents. If the schematic folder is part of the current project, then this field is left blank.

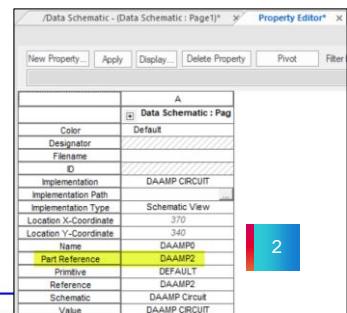
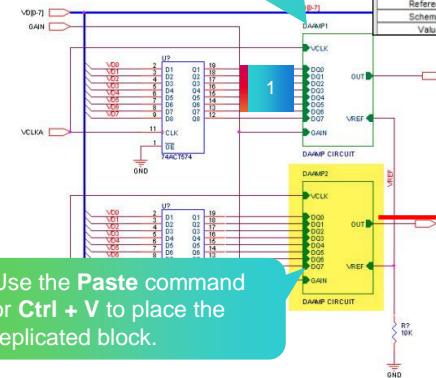
Replicating the Block



One of the main advantages of the hierarchical design is being able to place multiple instances of the same block to easily replicate a logical function.

1. Use the Copy command to add more instances of the same block to the design.
2. Edit the properties of each replicated block and assign a unique reference. For example, DAAMP1 or DAAMP2.

Use the **Copy** command or **Ctrl + C** to replicate the block.



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One of the main advantages of the hierarchical design is being able to place multiple instances of the same block to easily replicate a logical function.

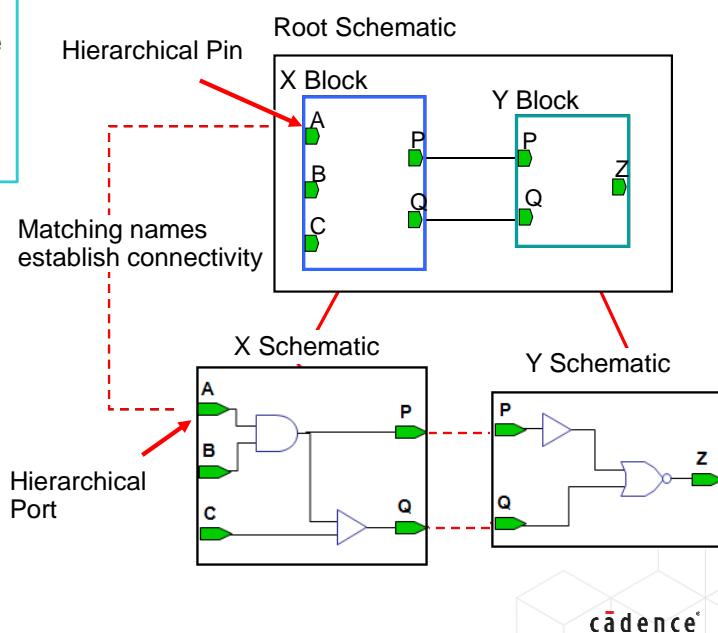
Once you've placed a block symbol, use the **Copy** command to add more instances of the same block to the design. Edit the properties of each replicated block and assign a unique reference. For example, DAAMP2 or DAAMP3.

Connectivity in Hierarchical Designs



The hierarchical pins on the block symbol and the hierarchical ports in the schematic are used to establish connectivity between the schematic folders in a hierarchical design.

- When you create a netlist for PCB design, the hierarchy is flattened. This means that the highest level of connectivity, at the highest level in the hierarchy, takes precedence in the netlist.
- For example, a net alias on a wire at the top (or root) of the hierarchy will override the port symbol name in the lower-level schematic.



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The hierarchical pins on the block symbol and the hierarchical ports in the schematic are used to establish connectivity between the schematic folders in a hierarchical design.

When you create a netlist for PCB design, the hierarchy is flattened. This means that the highest level of connectivity, at the highest level in the hierarchy, takes precedence in the netlist.

For example, a net alias on a wire at the top (or root) of the hierarchy will override the port symbol name in the lower-level schematic. The net name from the root schematic is passed down into the schematic below.

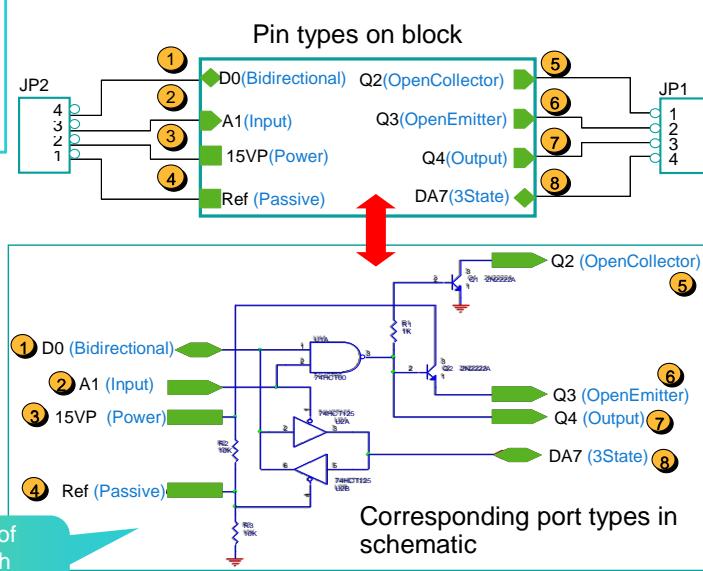
Hierarchical Pins and Ports



To establish connectivity, a hierarchical pin on the block symbol must have a matching hierarchical port with the same Name and Type in the corresponding schematic.

- The Capture symbol library (*capsym.olb*) has eight port symbols to choose from. The names of the port symbols names reflect the direction in which the symbol is pointing (graphically) and the location of the pin (connection point).
- You can enter the name while placing the port or change the name after you've placed it.
- The port type provides a logical description of the net it represents, such as input, output, or bidirectional.

There are eight types of hierarchical ports, each with its own corresponding hierarchical pin type.



There are eight types of hierarchical ports, each with its own corresponding hierarchical pin type (as shown in the accompanying illustration). To establish connectivity, a hierarchical pin on the block symbol must have a matching hierarchical port with the same Name and Type in the corresponding schematic.

The Capture symbol library (*capsym.olb*) has eight port symbols to choose from. The names of the port symbols names reflect the direction in which the symbol is pointing (graphically) and the location of the pin (connection point). For example, PORTLEFT-R is a port symbol that points to the left, with a pin on the right. You might need to rotate a port symbol before you place it.

You need to name the port to define the signal it represents. You can enter the name while placing the port or change the name after you've placed it. The name on the port symbol takes precedence over the alias on the wire it is connected to.

When adding a port, you must specify the port type. The port type provides a logical description of the net it represents, such as input, output, or bidirectional.

Each of the eight symbols has a default typesetting. You can select the port type while placing it or change it after it has been added.

- PORTRIGHT-L and PORTRIGHT-R (Input)
- PORTELEFT-L and PORTELEFT-R (Output)
- PORTBOTH-L and PORTBOTH-R (Bidirectional)
- PORTNO-L and PORTNO-R (Passive)

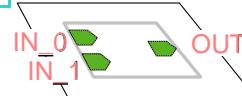
Synchronizing a Hierarchical Design



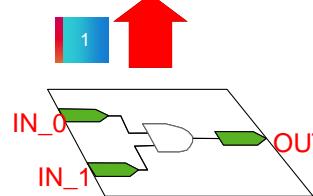
You can synchronize a hierarchical design in two ways: from the bottom-up or from the top-down.

1. If you add hierarchical ports in the schematic, you can synchronize its associated block symbol.
2. Similarly, changes to the block symbol can be synchronized to the corresponding schematic.

Bottom-up

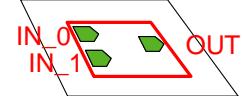


Hierarchical pins are automatically added to the higher-level block symbol.



(This method is used in class)

Top-down



Hierarchical ports are automatically added to the underlying schematic.



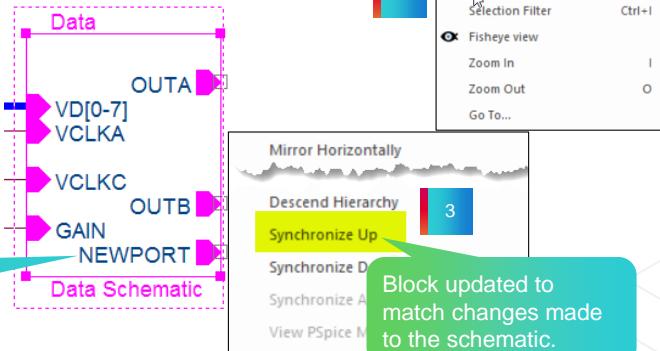
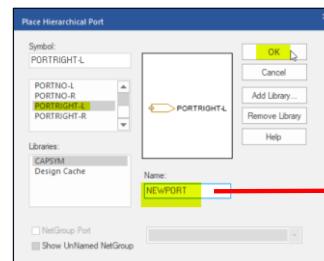
(See the Lab Appendix for optional labs)

You can approach hierarchical design in two ways: from the bottom-up or from the top-down. If you add hierarchical ports in the schematic, you can synchronize its associated block symbol. Similarly, changes to the block symbol can be synchronized to the corresponding schematic.

Synchronizing Changes Up to the Block Symbol



Use the **Synchronize Up** command to update the selected hierarchical block with all the changes made to the ports in the underlying schematic.



To add a new port to the block:

1. Add the new port to the lower-level schematic.
2. Right-click and choose **Ascend Hierarchy** to select the associated block symbol.
3. Right-click and choose **Synchronize Up**.

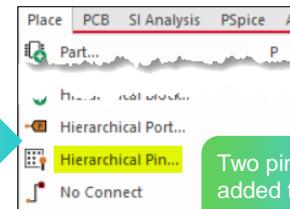
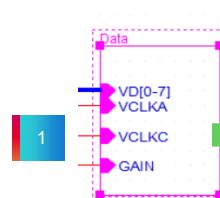
The hierarchical pin is automatically added to the block symbol.

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Synchronizing Changes Down to the Schematic



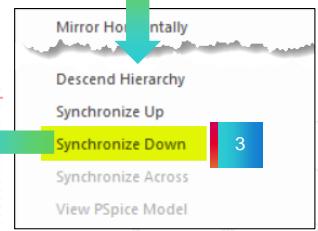
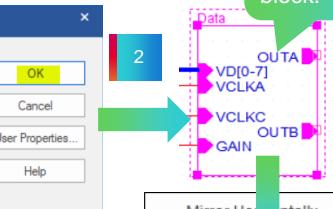
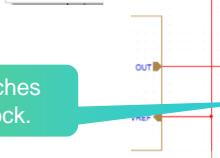
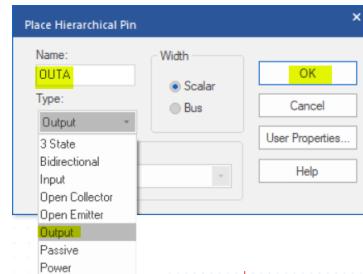
Use the **Synchronize Down** command to update the underlying schematic with all the changes made to the pins of the selected hierarchical block.



Two pins are added to the block.

To add a new port to the schematic:

1. Select **Block** and choose **Tools – Hierarchical Pin**.
2. Add the new pin(s) to the selected block symbol.
3. Right-click and choose **Synchronize Down**.



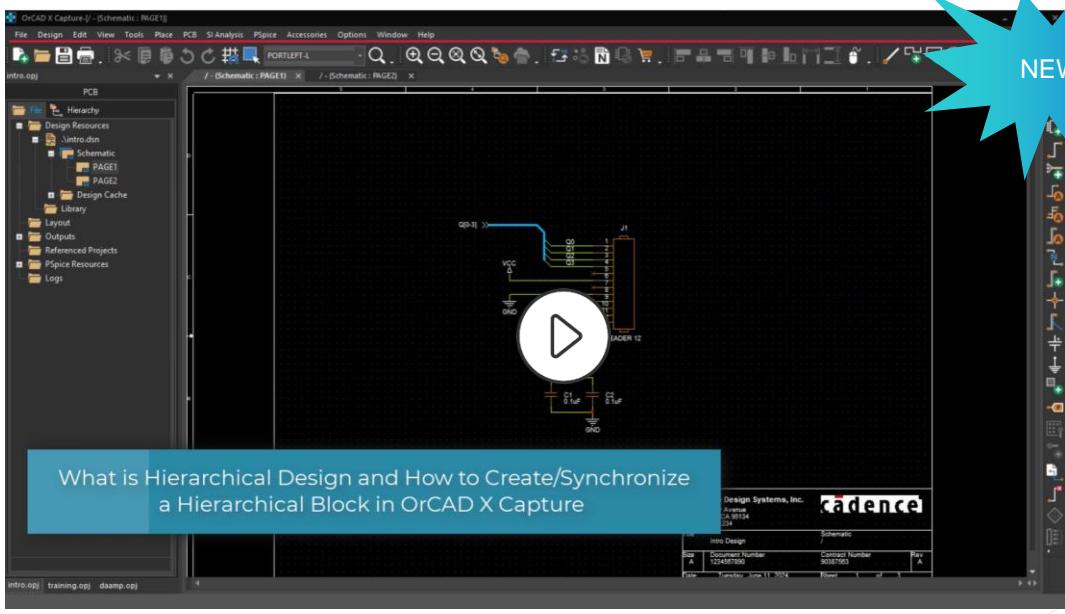
The schematic now matches changes made to the block.

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Demo: Hierarchical Design and How to Create/Synchronize a Hierarchical Block



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Video Play Time: **4.07** minutes

Click the Play button to start the video.

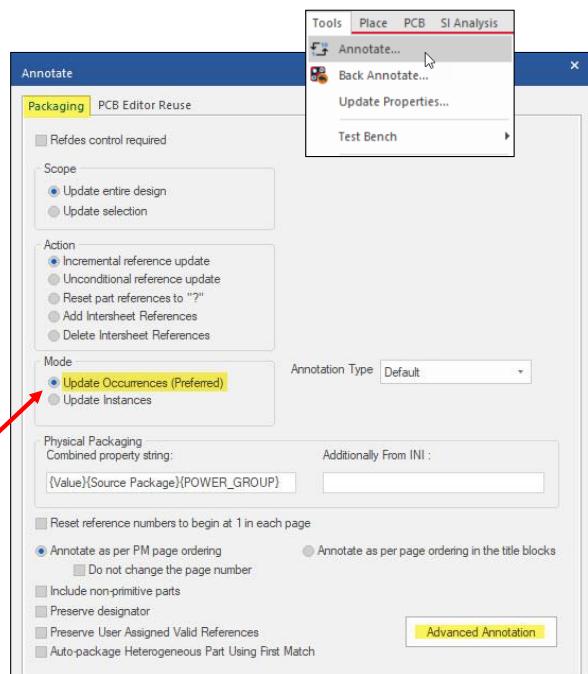
Annotating Hierarchical Designs



Choose Tools – Annotate.

The Annotate command adds reference designators to all parts of the design. This annotation is required in order to generate a netlist for the PCB layout.

- Use the Scope field to control how much of the design is annotated.
- Use Incremental mode if some Part References are already set or Unconditional to override existing assignments.
- Use Occurrence mode for hierarchical designs and Instance mode for flat designs.
- Use to update title block page numbers to match the page sequence in Project Manager.



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Instances Versus Occurrences in Hierarchical Design



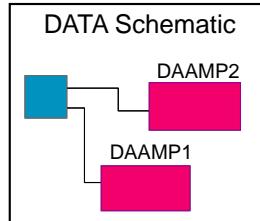
An instance is a part that appears once in a flat design. An occurrence applies to complex hierarchical designs only.

When a block symbol occurs more than once in a hierarchical design, the schematic it represents also occurs multiple times. Each instance in the schematic occurs multiple times, one occurrence in each block.

For hierarchical designs, occurrence mode is set automatically (preferred).

Mode

- Update Occurrences (Preferred)
- Update Instances



	DAAMP1	DAAMP2
CLASS	DISCRETE	DISCRETE
Color	Default	Default
COMP SIDE	BOTTOM	BOTTOM
Designator		
DEVICE	CAP_01uF	CAP_01uF
Graphic	CAP.Normal	CAP.Normal
ID	3459	3556
Implementation		
Implementation Path		
Implementation Type	<none>	<none>
Location X-Coordinate	370	370
Location Y-Coordinate	300	300
Name	INS646919	INS646919
Part Reference	C?	C8
PCB Footprint	SMC_6032	SMC_6032
Power Pin Visible	✓	✓
Primitive	DEFAULT	DEFAULT
Reference	C?	C8
Source Library	D:\ORCAD\ORCAD_16	D:\ORCAD\ORCAD_16
Source Package	CAP	CAP
Source Part	CAP.Normal	CAP.Normal
Value	.01uF	.01uF

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An *instance* is a part that appears once in a design. An instance of a part is found in a flat or simple hierarchical design.

An *occurrence* applies to complex hierarchical designs only. When a block symbol occurs more than once in a hierarchical design, the schematic it represents also occurs multiple times. Each instance in the schematic occurs multiple times, one *occurrence* in each block.

In the accompanying illustration, the DAAMP Circuit occurs twice, referenced by two hierarchical blocks in the Data Schematic. When you edit a part in the DAAMP Circuit, the Property Editor shows the instance properties in white and the properties on each occurrence in yellow.

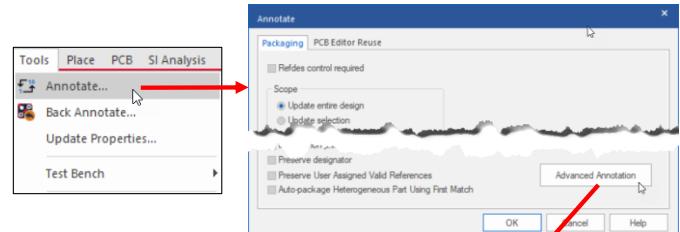
When processing a hierarchical design, each occurrence of a part must be processed. For example, the Annotate program must assign a part reference to each occurrence in a duplicated block.

In a complex hierarchical design, the Property Editor shows different Part Reference values for each occurrence.

Advanced Annotation

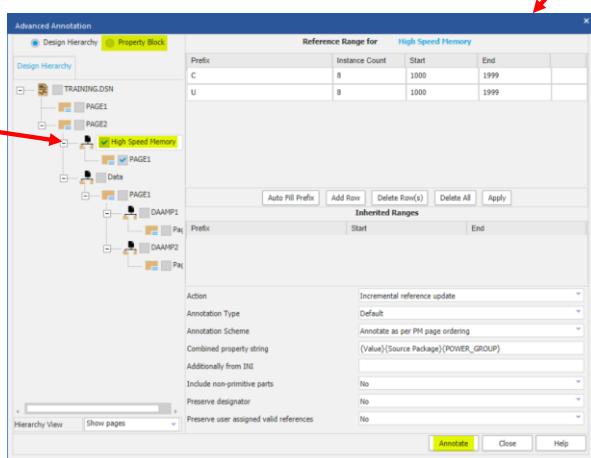


Choose Tools – Annotate – Advanced Annotation.



Use Advanced Annotation when you need more control over RefDes assignments.

- Checkboxes control which items are being annotated.
- Each item in the Design Hierarchy pane can have its own RefDes range controls.
- Parts with properties in common can be leveraged into selectable groups for annotation.



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Advanced Annotation lets you annotate one or more selected items in the Design Hierarchy pane. Each item in the Design Hierarchy pane can have its own assigned reference designator range controls.

You can also specify a RefDes range at the design level. If a RefDes range is specified at the page level, it overrides the design level set. If no range is specified at a lower level, the design level settings are automatically applied.

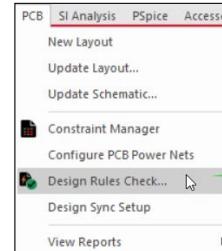
Common Property Annotation

The Advanced Annotation feature lets you specify RefDes ranges for parts that have an assigned property in common. This feature lets you select and annotate each group of qualifying parts using an assigned RefDes range. For example, the ROOM = Memory property can be leveraged into a part group and annotated using an assigned RefDes range.

How to Run Design Rules Check on a Hierarchical Design



Use **Design Rules Check** to verify that your electrical and physical rules are not being violated.



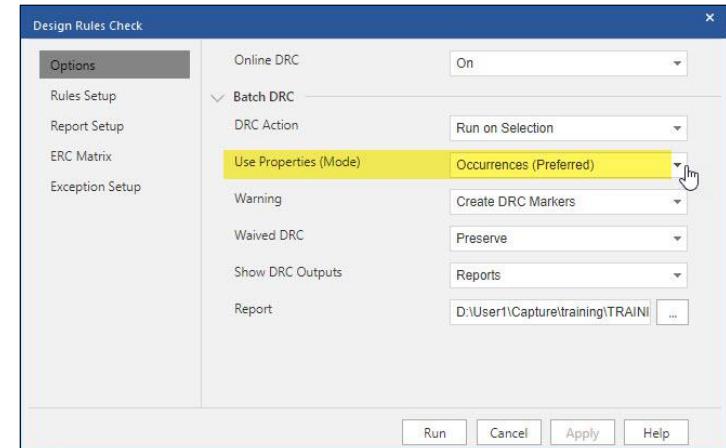
To run the DRC.



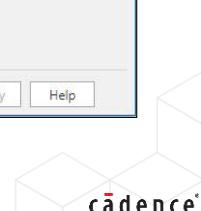
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Step 1: Setting Options

- Setting Options
- Setting Up Rules
- Setting Up Report



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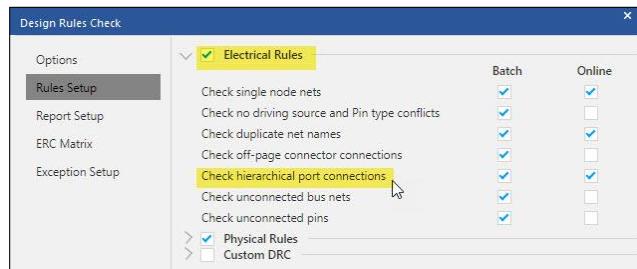


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Step 2: Setting Up Rules



- Hierarchical ports take precedence over all other types of connections, so it's important to make sure they are labeled correctly.
- Use the **Rules Setup** tab to generate errors if the number of ports in a schematic is different from the number of pins in the block symbol, or if the port types are not the same as the pin types.



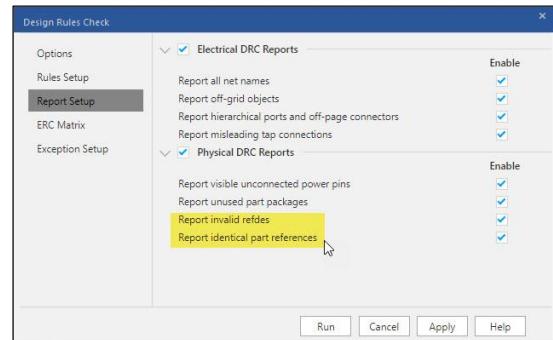
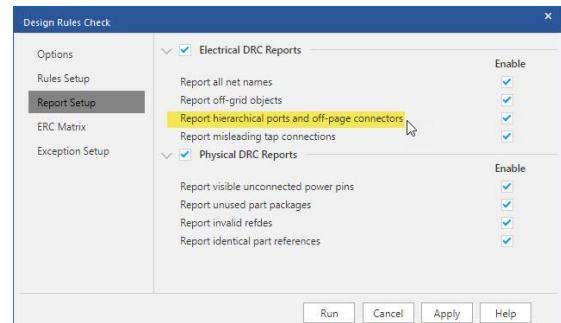
From highest to lowest, the precedence levels are listed here.

- Hierarchical port takes precedence over all other types of connections.
- The off-page connector takes precedence over a net alias or a voltage symbol.
- PWR/GND symbol takes precedence over a net alias. When multiple voltage symbols are wired together, the lowest net (alphanumerically) takes precedence.
- Net alias takes precedence over an unlabeled wire. When multiple net aliases are wired together, the lowest net (alphanumerically) takes precedence.
- Unlabeled wires are the lowest level of connectivity. It will inherit its name from all other levels or get a system-generated name.

Step 3: Setting Up the Report



- Use the Report Setup tab to generate a list of all port names used in the hierarchical design.
- If you've copied schematic folders from other designs, use the **Report Setup** tab to check for identical part references or invalid packaging in the design.
- Also, check the net names report for any overrides.



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Step 4: Setting Up the ERC Matrix

Setting Options

Setting Up Rules

Setting Up Report

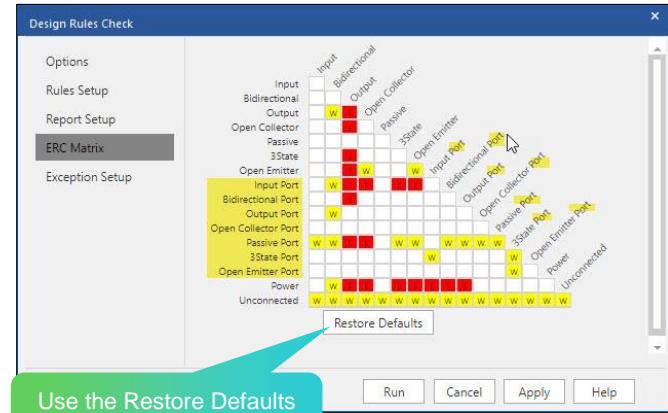
Setting Up ERC Matrix

Use the **ERC Matrix** tab to check for invalid port-to-port combinations.

Click on any box in the matrix and toggle it to warning or error.

- The pin combination is valid.
- Flagged as a warning.
- Flagged as an error.

Use the ERC Matrix settings stored in the *Capture.ini* file.



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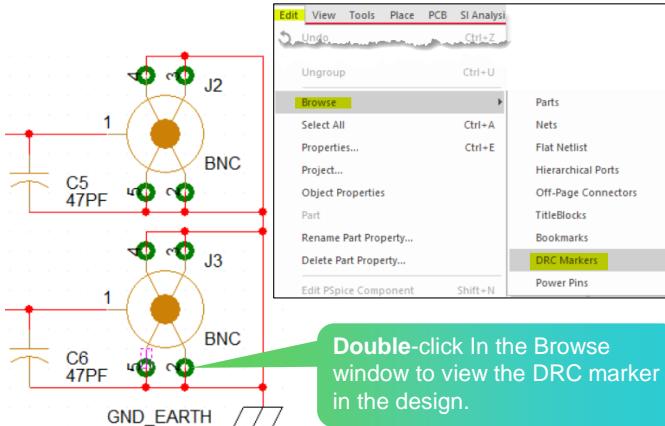
Browsing DRC Markers



Choose **Edit – Browse – DRC Markers**.

Use this command to view a list of DRC errors.

The Project Manager window must be active to access this command.



DRCs- C:\USER1\CAPTURE\TRAINING\TRAINING.DSN							
Severity	DRC Type	Description	Detail	Location	Page	Schematic	Waived
Warning	Electrical	WARNING(ORCAP-1589): Net has two or more aliases that might lead to a short. ...	J3_GND2 GND2 GND_EARTH	Training Root Schematic, PAGE2 (8.90, 5.30)	PAGE2	Training Root Schematic	No
Warning	Electrical	WARNING(ORCAP-1589): Net has two or more aliases that might lead to a short. ...	J3_GND5 GND5 GND_EARTH	Training Root Schematic, PAGE2 (8.70, 5.30)	PAGE2	Training Root Schematic	No
Warning	Electrical	WARNING(ORCAP-1589): Net has two or more aliases that might lead to a short. ...	J3_GND3 GND3 GND_EARTH	Training Root Schematic, PAGE2 (8.90, 4.70)	PAGE2	Training Root Schematic	No
Warning	Electrical	WARNING(ORCAP-1589): Net has two or more aliases that might lead to a short. ...	J3_GND4 GND4 GND_EARTH	Training Root Schematic, PAGE2 (8.70, 4.70)	PAGE2	Training Root Schematic	No
Warning	Electrical	WARNING(ORCAP-1589): Net has two or more aliases that might lead to a short. ...	J2_GND5 GND5 GND_EARTH	Training Root Schematic, PAGE2 (8.70, 4.40)	PAGE2	Training Root Schematic	No
Warning	Electrical	WARNING(ORCAP-1589): Net has two or more aliases that might lead to a short. ...	J2_GND2 GND2 GND_EARTH	Training Root Schematic, PAGE2 (8.90, 4.40)	PAGE2	Training Root Schematic	No
Warning	Electrical	WARNING(ORCAP-1589): Net has two or more aliases that might lead to a short. ...	J2_GND3 GND3 GND_EARTH	Training Root Schematic, PAGE2 (8.90, 2.00)	PAGE2	Training Root Schematic	No
DRCs		Online DRCS	Session Log				

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You can use the **Edit – Browse – DRC Markers** command to visit any warning or error markers in the design. The Project Manager window must be active to access this command.

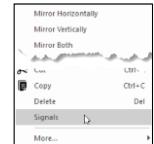
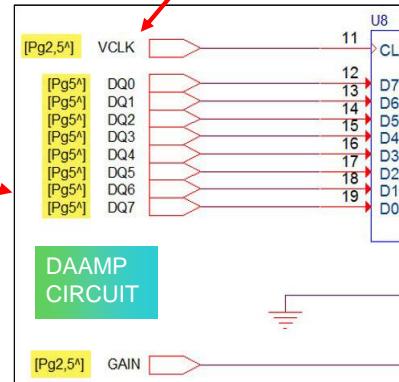
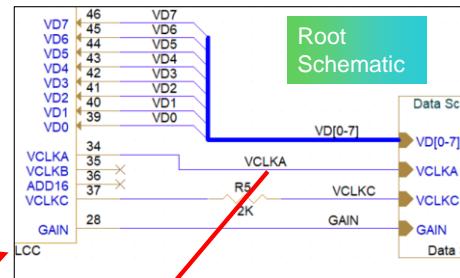
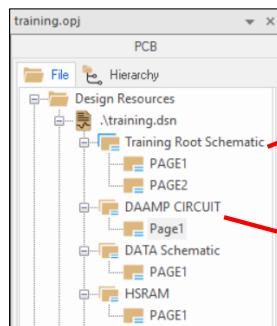
Click on a column header in the Browse window to sort the entries on that column.

You can also use the Search Toolbar to create a list of DRC errors to visit.

Intersheet References in a Hierarchical Design



Hierarchical cross references contain direction info (up or down the hierarchy) with respect to the current page.



The caret symbol (^) indicates that the signal exists one level higher in the hierarchy. An exclamation (!) symbol indicates that the signal exists one level lower in the hierarchy.

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Hierarchical cross references contain additional information about the direction a signal goes direction (up or down the hierarchy) with respect to the current page.

The caret symbol (^) indicates that the signal exists one level higher in the hierarchy. An exclamation (!) symbol indicates that the signal exists one level lower in the hierarchy.

In the illustration above, notice how the VCLKA net changes to the VCLK net in the DAAMP CIRCUIT schematic. When the netlist is created for PCB design, the VCLK net in the DAAMP CIRCUIT will be named VCLKA.

You can use the **Signals** command on the right mouse button to trace a signal through the design.

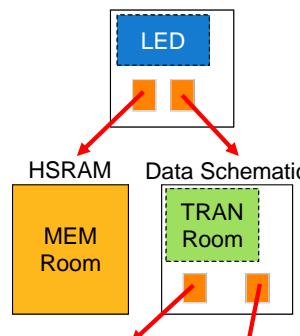
Adding PCB Editor/Presto Properties



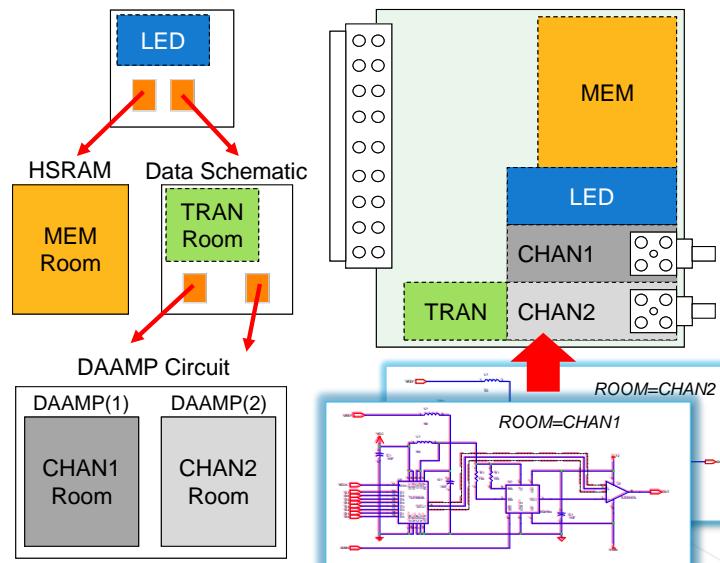
Use part properties to attach part information required for PCB layout.

- You can use part properties to designate certain parts to be placed in a specific area during layout.
- This floor planning helps control the flow of signals from one area of the layout to another.
- You can set up the room polygons in Allegro X PCB Editor/OrCAD X Presto to display error markers when a part is placed in the wrong room.

Capture Schematic



Allegro X PCB Editor/OrCAD X Presto



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Use the ROOM property in the schematic to assign parts to specific areas of the board layout. This graphic shows how a polygon on the board is used to control the placement of DAAMP1 and DAAMP2 parts into rooms named CHAN1 and CHAN2. You can set up the room polygons in Allegro X PCB Editor/OrCAD X Presto to display error markers when a part is placed in the wrong room.

Examples of PCB Editor/Presto Part Properties

The following are some Allegro X PCB Editor/OrCAD X Presto part properties to use in a Capture design.

PCB Footprint	Defines the footprint pattern used during layout. This is a mandatory property.
ALT_SYMBOLS	Defines a list of alternate footprint pattern.
CLASS	Classifies the part as an IC, IO, or discrete device.
ROOM	Assigns a part to a specific area of the PCB for placement.
SPLIT_INST	To identify sections belonging to a split part

In the Property Editor, set the Filter by field to **Allegro PCB Designer** to load a predefined list of properties.



Here is a list of some Allegro X PCB Editor/OrCAD X Presto part properties to use in the Capture schematic.

- **PCB Footprint** – Specifies the name of a footprint pattern in the Allegro library. This is a required property.
- **ALT_SYMBOLS** – Defines a list of alternate footprint patterns you can use during PCB layout. Each alternate footprint must have the same pin count.
- **CLASS** – Classifies the part as either an IC, IO, or a Discrete device. The Discrete and IO part classes affect the model assignment process in the Signal Integrity tool. If the Class property is unassigned, its value defaults to IC.
- **ROOM** – Assign the part to a specific area or room of the PCB.
- **SPLIT_INST** – the property must be added to all sections of a heterogeneous part. Set the **SPLIT_INST** property value to *TRUE*. There must be no duplicate pins across the sections of the split part.

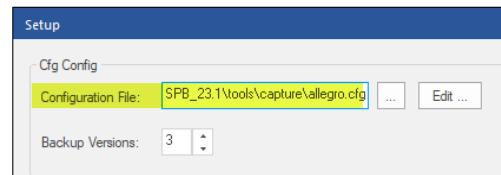
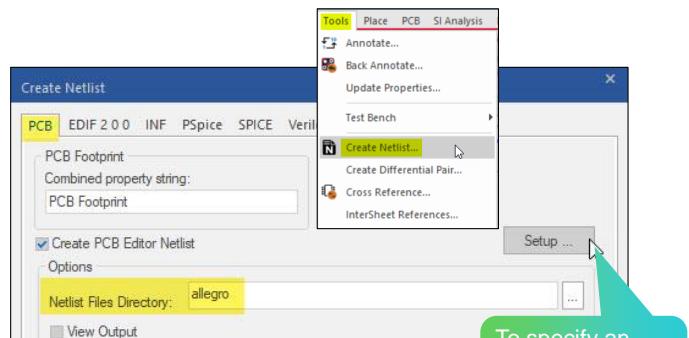
In the Property Editor, set the *Filter by* field to **Allegro PCB Designer** to load a predefined list of properties.

Creating a Netlist for PCB Editor/Presto

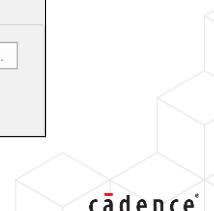


Choose Tools – Create Netlist.

- A netlist must be generated before the PCB layout process can begin.
- The netlist files contain parts and connectivity, as well as any properties required for PCB layout.
- You can use the **Setup** button in the Create Netlist form to specify an alternate configuration file used for customizing the transfer of properties to PCB Editor/Presto.



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Cadence provides a configuration file `<install directory>/tools/capture/allegro.cfg` that controls which part and net properties are extracted from the Capture schematic and added to the netlist. The properties listed in the configuration file are the same properties in the Cadence-Allegro property filter.

Use the Setup button in the Create Netlist window to specify an alternate configuration file.

Three netlist files are created and stored in the directory location you specify in the Netlist Files Directory field. In the above illustration, the netlist files are created in the `allegro` subdirectory under the project folder.

If any errors are found while producing the netlist, the netlist is not generated, and error messages are sent to the session log window. A `netlist.log` file is also written to the current working directory.

How to Keep Allegro Files in a Subdirectory

When generating the netlist, it's important to keep the Allegro .DSN file and the Capture .DSN file in separate folders.

The diagram illustrates the project structure:

- A folder structure is shown under "D:\My_Projects\":
 - "SAMPLE" (Project folder)
 - "SAMPLE.OPJ"
 - "SAMPLE.DSN"
 - "ALLEGRO" (Subdirectory)
 - "PST*.DAT (3)"
 - "SAMPLE.BRD"
 - "SAMPLE.DSN"

Annotations explain the file placement:
 - "Capture files" are grouped by curly braces around "SAMPLE.DSN" and "ALLEGRO\SAMPLE.DSN".
 - "Allegro files" are grouped by curly braces around "PST*.DAT (3)", "SAMPLE.BRD", and "ALLEGRO\SAMPLE.DSN".
 - A note says: "Use the Create Netlist menu to create this Allegro subdirectory."

To the right, a screenshot of the "Create Netlist" dialog box is shown. It has tabs for PCB, EDIF 2.00, INF, PSpice, SPICE, Verilog, VHDL, and Other. The PCB tab is selected. Under Options, there is a checked checkbox for "Create PCB Editor Netlist" and a dropdown for "Netlist Files Directory" set to "allegro". A note at the bottom of the slide states: "Note: The Capture schematic editor and the Allegro PCB router produce a <design_name>.dsn file."

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It's important to keep in mind that both the Capture schematic editor and the Allegro PCB router generate a file with the extension .dsn named after your design. To avoid overwriting your Capture schematic database, you should place the capture .dsn files in the sample project folder, and in the Allegro subdirectory, the Allegro board design files. This way, you can ensure that the Allegro PCB router does not overwrite your Capture schematic database.



Common Netlist Errors

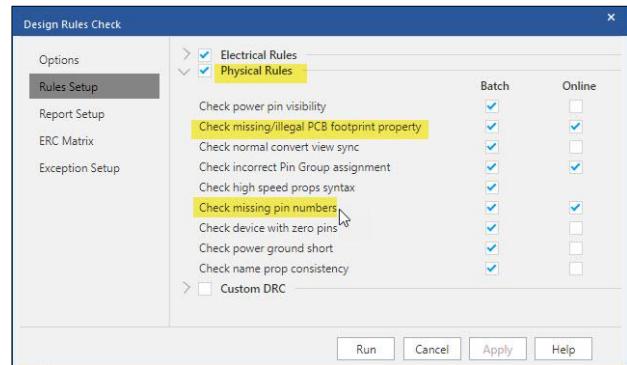
Here is a list of some common problems to be aware of so you can plan:

- PCB footprint property
- Pin name and number
- Pin count and pin numbers for part must match between libraries
- NC_PINS property
- Property lengths and character limits
- No spaces allowed

No spaces are allowed in directory names, library names, design names, net names, footprint names, pin names and numbers, and property names or values.

View these error messages in the Capture Session Log.

A *netlist.log* file is also written to the current working directory.



Some netlist problems can be flagged early in the design process using the Design Rules Check. Other problems would need to be addressed at the library level.

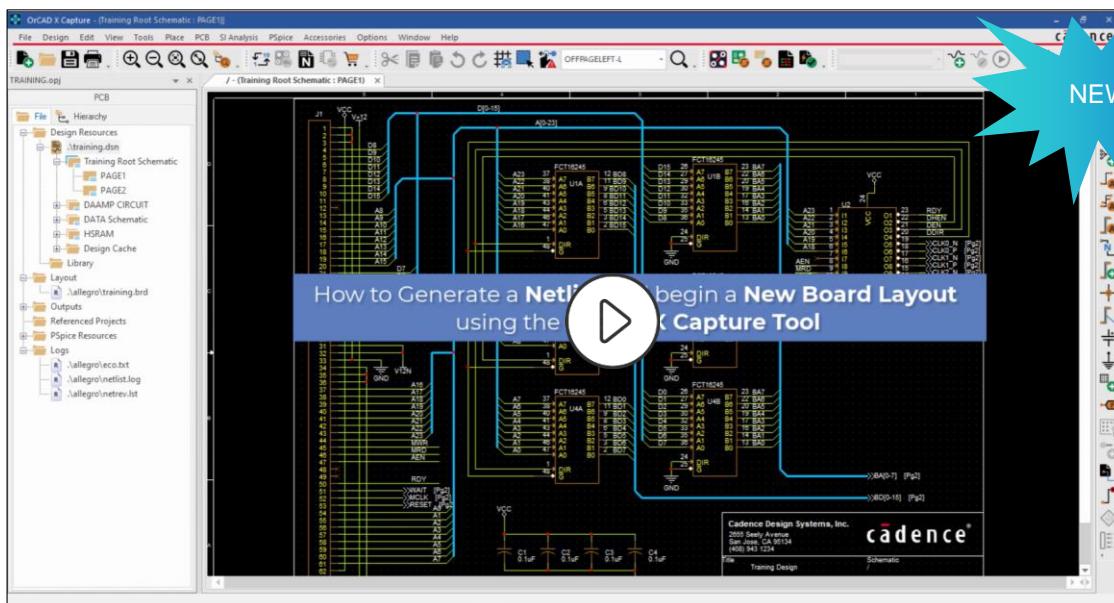
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Common Errors

- **PCB Footprint missing in Capture** – Make sure that all parts have a PCB footprint assigned.
- **Footprint does not match library (symbol) name** – Pin counts of the Capture part must match the physical symbol (footprint), and physical pins numbers must match.
- **Cannot find the symbol** – psm or pad path incorrect.
- **Pin mismatch** – Pin numbers or total pin counts do not match from footprint to component symbol.
- **Pin name not allowed** – There are property length and character limits for the Allegro X PCB Editor.
- **Pin Number missing in Capture part** – All pins must have a pin name and number in the Capture part.
- **No spaces are allowed** – There should be no space in directory names, library names, design names, net names, footprint names, pin names and numbers, and property names or values.

Demo: Generating a Netlist and Beginning a New Board Layout



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Video Play Time: **3.14** minutes

Click the Play button to start the video.

Cross-Probing



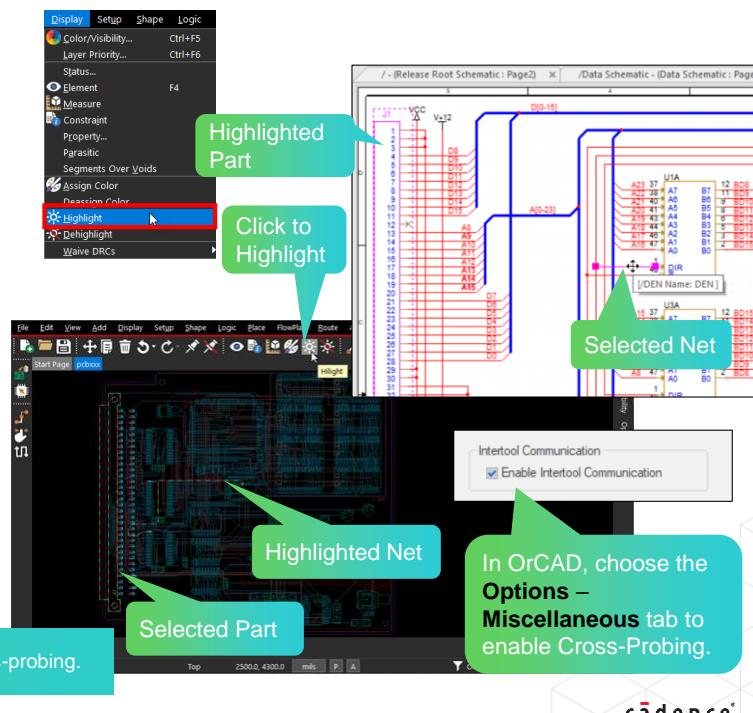
Choose **Display – Highlight** from the PCB Editor.

Both OrCAD X Capture and PCB Editor support cross-probing, which lets you pick an object in one tool and see it highlighted in the other tool.

- This is helpful when checking part placement or critical signal routing.

You can also use cross-probing with the **Place – Manually** command to pick a part in the schematic and place it on the board.

Similarly, OrCAD X Capture and OrCAD X Presto support cross-probing.



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Both OrCAD Capture and PCB Editor support cross-probing. When one tool broadcasts a message about selecting an object, the other tool receives the message and highlights or de-highlights the object.

To cross-probe between OrCAD X Capture and the PCB Editor, choose **Display – Highlight** from the PCB Editor, and click on a part in the layout.

The part you selected in the layout is highlighted in the OrCAD X Capture schematic. Next, select a part in the schematic to highlight it in the layout.

Click on a net in the schematic is highlighted in the layout.

Before cross-probing, import the netlist to the layout.

Backannotating the Schematic

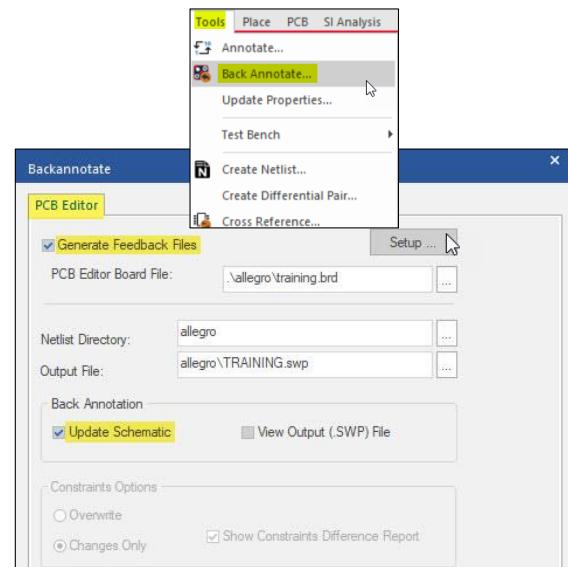
Choose Tools – Back Annotate.



Capture lets you backannotate schematics with changes made in Allegro X PCB Editor/OrCAD X Presto. These changes include:

- Renamed reference designators
- Part property changes
- Gate and pin swapping changes

In PCB Editor/Presto, four backannotation files are created, and these four files are processed into a single backannotation file in Capture, called a swap file.



The swap file is used to update the Capture schematic with new part references, part, and net properties.

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The *allegro.cfg* configuration file controls the backannotation of part and net properties.

When you choose **File – Export Logic** in the PCB Editor/Presto, four backannotation files are created:

- *pinView.dat* – Contains all pins and net connections.
- *netView.dat* – Contains all net properties.
- *compView.dat* – Contains all part properties.
- *funcView.dat* – Contains all gate properties.

These files can also be produced in Capture by choosing **Tools – Back Annotate** and selecting the **Generate Feedback Files** option.

In Capture, these four files are processed into a single backannotation file, called a swap file. The swap file is then used to update the Capture schematic with new part references and part and net properties. All gate and pin swapping data are also included in the swap file.

Important

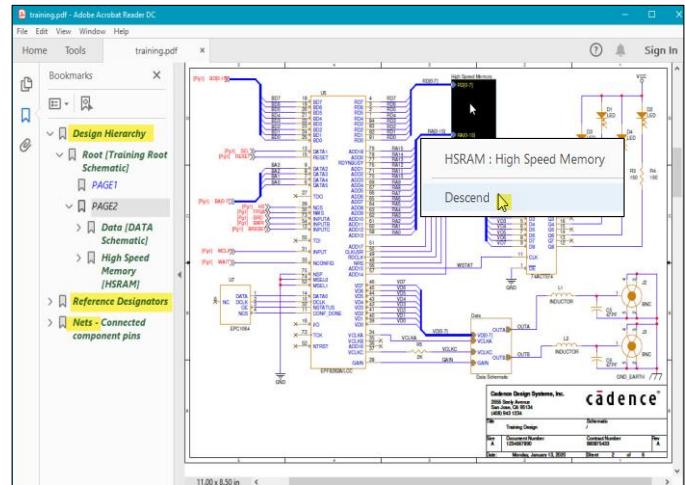
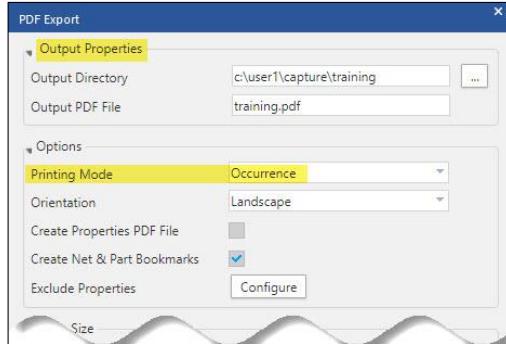
The four backannotation files must be in the same “Allegro” subdirectory as the original netlist files.

Exporting a PDF



Choose File – Export – PDF.

Use this command to export the Capture design as a PDF file to be viewed with Adobe Reader.



Use required postscript to pdf converters, such as Ghostscript 32-bit, Ghostscript 64-bit, or Adobe Acrobat Distiller.

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You can use the **File – Export – PDF** command to export a Capture design as a PDF file, provided you have the required postscript to pdf converters installed, such as Ghostscript 32-bit, Ghostscript 64-bit, or Adobe Acrobat Distiller.

The Capture design PDF:

- Displays design hierarchy tree
- Displays reference designators list
- Displays nets and connected component pins
- Descends hierarchical blocks
- Displays properties on clicking an object
- Displays navigation to off-page connectors

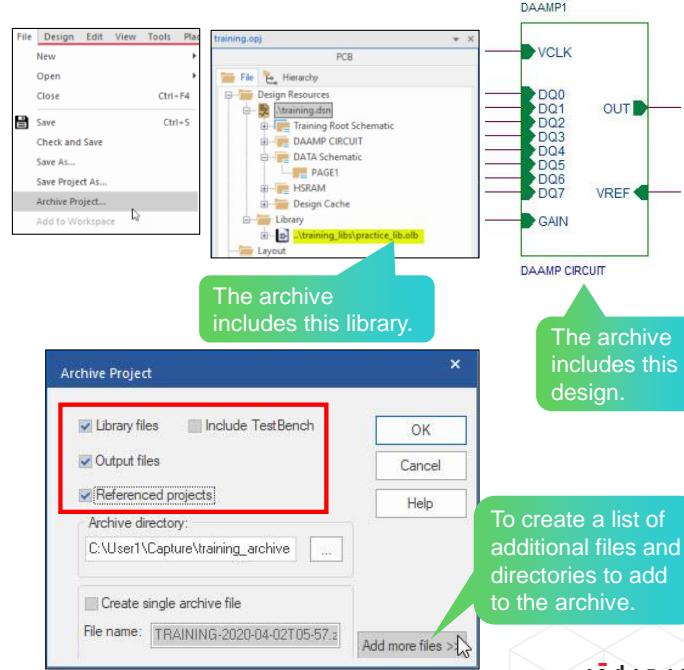
Archiving a Project



Choose File – Archive Project.

- You can save the project (.OPJ) and all the related files (design, library, output files, and referenced projects) in a different directory and create a zip file of this directory for archival purposes.
- Ensure that the project you want to archive is active and the schematic pages are not open.
- The path names of the files and directories in the archive are relative to the archive directory.
- When the archive file is unzipped on a different machine, the files and directories retain the original directory structure of the archive directory.

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You can also specify any additional files or directories you may want to be archived along with your project files.

The path names of the files and directories in the archive file are relative to the archive directory. This implies that when the archive file is unzipped on a different machine, the files and directories retain the original directory structure of the archive directory.

Select the files you want to be archived with your project. The **Libraries** option archives library files and related files located in the Library folder of the Project Manager (for example, the *practice_lib.olb*). The **Referenced projects** option includes any projects referenced from within the current project (for example, an external design file linked to a hierarchical block symbol as in the DAAMP CIRCUIT). If you do not select any of the options (Library files, Output files, or Referenced projects), Capture archives only your project (.OPJ) and design (.DSN) file.

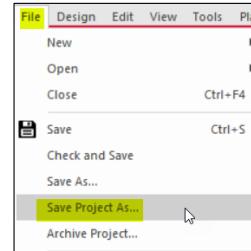
Use the **Add more files** button to create a list of additional files and directories to add to the archive. This data is placed in an *Additional files* subdirectory in the archive folder.

Creating a New Project from an Existing Project



Choose **File – Save Project As.**

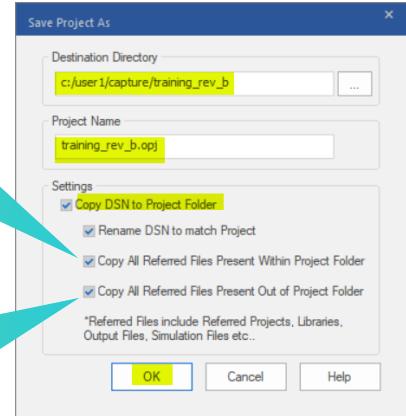
- When a design needs to be modified, the first step is to copy and rename the existing project.
- Use this command to save an existing project into a new project folder. The design and project files can be renamed.
- All associated files can be copied, including report and netlist files, project-specific libraries, and external design files linked to hierarchical blocks.



To get all files stored directly under the project folder (for example, all the report files shown in the Outputs folder in the Project Manager).

To get all files that are stored in subdirectories under the project folder (for example, the netlist files stored in the *allegro* subdirectory).

All project-specific libraries listed under the Libraries folder in the Project Manager are copied into a *MovedFiles* subdirectory.



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Use the Save Project As command to save an existing project into a new project folder. The design and project files can be renamed.

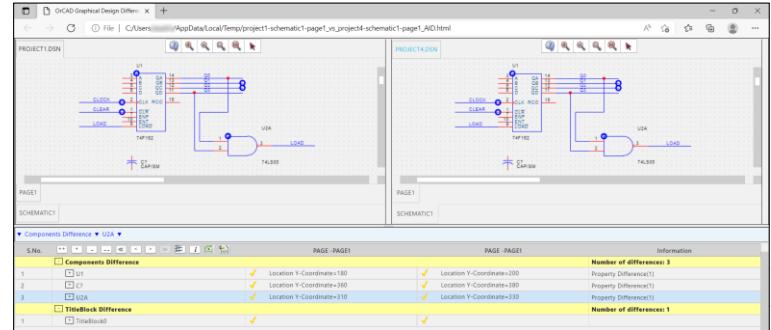
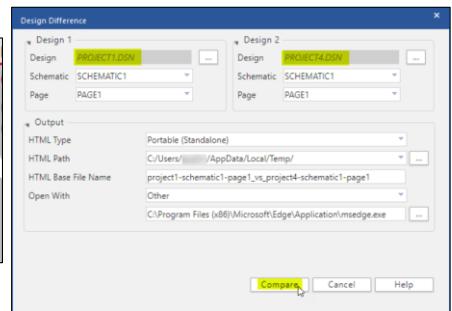
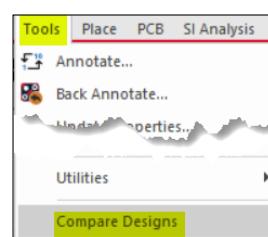
All external designs referenced in the Path and filename field of the Place Hierarchical Block window are also copied into the *MovedFiles* subdirectory.

Design Difference Viewer



Choose Tools – Compare Designs.

- Sometimes, you may need to compare two versions of the same design to determine or verify what was changed.
- Use this command to view logical and graphical differences between two designs, schematic folders, or pages.



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You can now view logical and graphical differences between two designs, schematic folders, or schematic pages using Capture. Choose from the **Tools – Compare Designs** menu in Capture to compare the designs or schematics.

Logical differences include the following categories: Components, Pin Net Connectivity, and FlatNet.

You can also compare the graphical x and y locations for components, wires, off-page connectors, hierarchical ports, and title block symbols in the schematic.



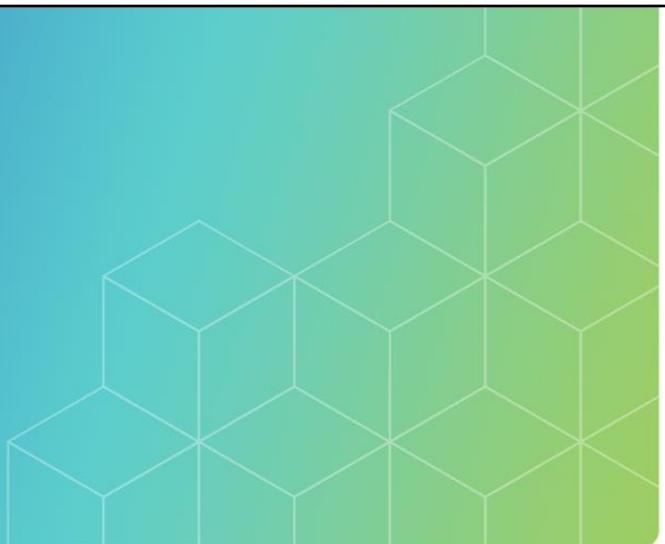
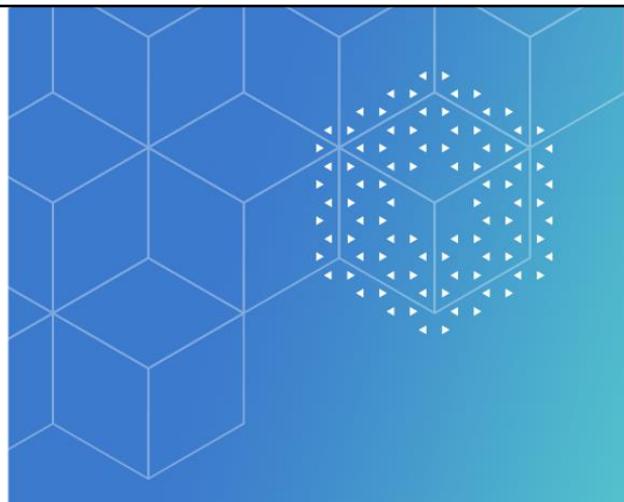
Labs

- Lab 8-1 Opening and Viewing a Hierarchical Design
- Lab 8-2 Editing the Training Root Schematic
- Lab 8-3 Making Power Pins Visible
- Lab 8-4 Reusing a DAAMP Block
- Lab 8-5 Annotating the Design
- Lab 8-6 Running Design Rules Check
- Lab 8-7 Waiving DRCs
- Lab 8-8 Hierarchical Cross Referencing and Plotting
- Lab 8-9 Creating a Bill of Materials Report
- Lab 8-10 Archiving a Project
- Lab 8-11 Creating a New Project from an Existing One

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You will now have the opportunity to perform some self-paced labs to reinforce the ideas presented in this module.



Module 9

Course Conclusions

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Summary

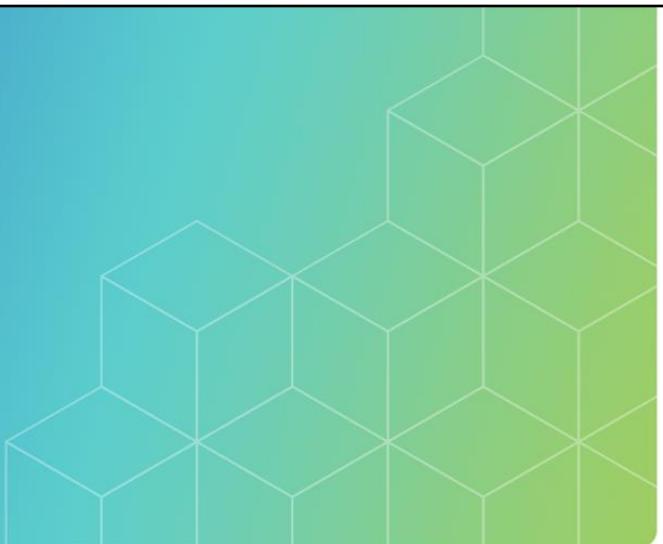
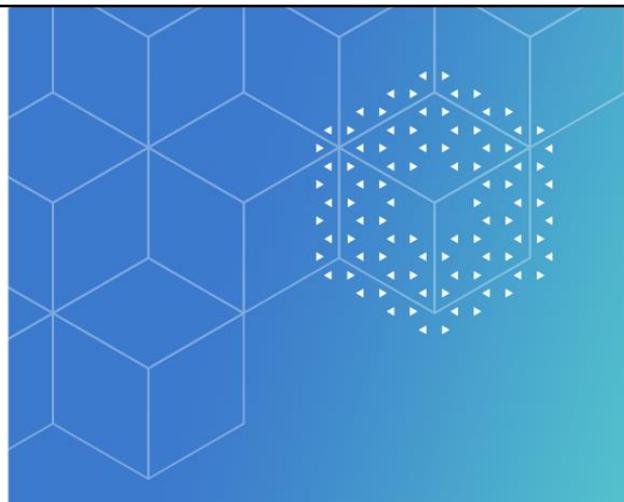
In this course, you learned how to:

- Set up user interface preferences and design template data
- Build Capture library parts
- Create multi-sheet flat and hierarchical designs
- Check designs for errors
- Work with part properties
- Create netlist files for Allegro® X PCB Editor and OrCAD® X Presto



This was an introductory level course for new Cadence® OrCAD® Capture users. The course began with some basic schematic library development. This course showed you how to create and process a simple schematic, then progressed into multi-sheet and hierarchical designs. Part properties were also covered.

Hope you enjoyed the course, and thanks for attending.



Module 10

Next Steps

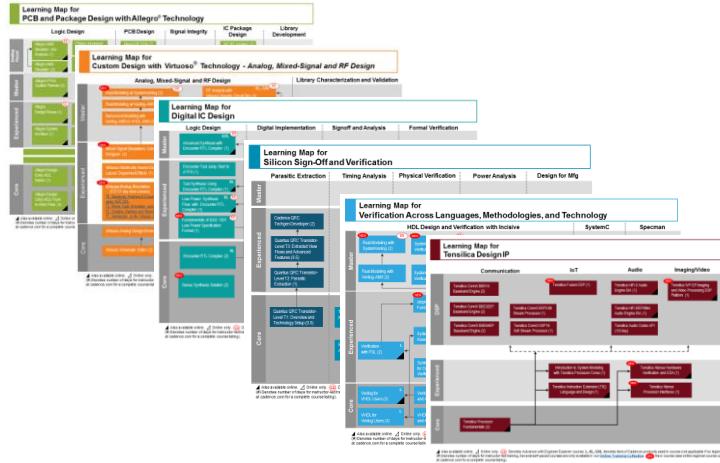
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Learning Maps

Cadence® Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers.

Click [here](#) to see all our courses in each technology area and the recommended order in which to take them.



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Go here to view the learning maps:

http://www.cadence.com/Training/Pages/learning_maps.aspx

Cadence Learning and Support

The screenshot shows the Cadence Learning and Support website. At the top, there's a navigation bar with links for Cases, Tools, IP, Resources, Learning, Software, My Support, and Contribute Content. To the right of the navigation are a bell icon and a user profile icon. Below the navigation is a search bar with a placeholder "Start your search here..." and a magnifying glass icon. A large play button icon is overlaid on the search bar. Below the search bar are two buttons: "View History" and "Documents Liked". The main content area features a background image of a circuit board with various icons like a wrench, a phone, and an '@' symbol. A blue banner at the bottom of the page says "Know more about a product: Choose a product...". Below this banner are six categories with icons: Installation & Licensing (gear), Product Manuals (book), Training Courses (document), What's New (lightbulb), Troubleshooting Information (wrench), and Video Library (play button). A text overlay in the center states: "Cadence Support now includes over 2000 product/language/methodology videos ("Training Bytes")!". At the bottom left, there's a copyright notice: "198 © Cadence Design Systems, Inc. All rights reserved." On the far right, there's a stylized 3D cube graphic with the word "cadence" written on it.

Click [here](#) to view the demo of Cadence Learning and Support.

Wrap Up

- Complete Post Assessment, if provided
- Complete the Course Evaluation
- Get a Certificate of Course Completion

Thank you!



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