74HC595D / 74HC595V / 74HC595P

RoHS COMPLIANT

8-Bit Shift Registers with Output Latches

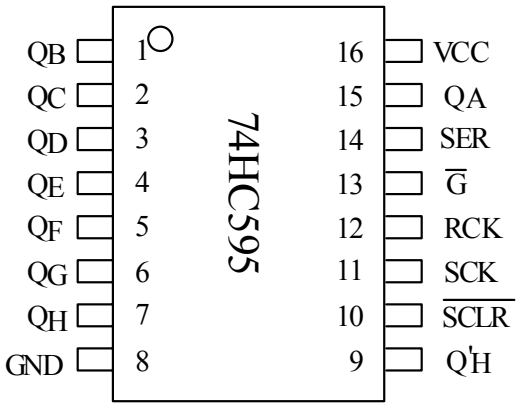
General Description

The 74HC595 high speed shift register utilizes advanced silicon-gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

Features

- Low quiescent current: 80μA maximum
- Low input current: 1μA maximum
- 8-bit serial-in, parallel-out shift register with storage
- Wide operating voltage range: 2V–6V
- Cascadable
- Shift register has direct clear
- Guaranteed shift frequency: DC to 30 MHz
- Package: SOP16(74HC595D), TSSOP16(74HC595V), DIP16(74HC595P)

Connection Diagram



SOP16(74HC595D), TSSOP16(74HC595V), DIP16(74HC595P)

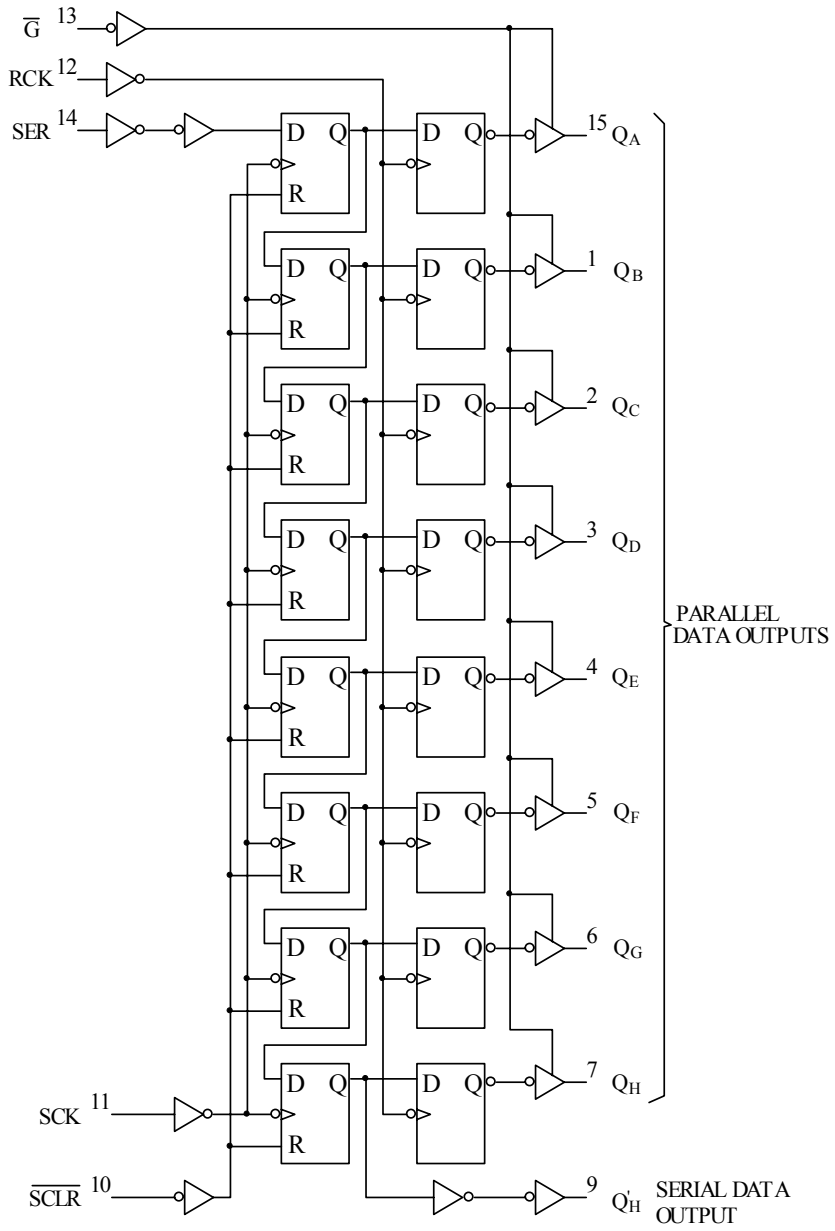
Pin Function

Pin	Name	I/O	Description
15，1～7	QA～QH	O	8 bit 3-STATE Output
8，16	GND，VCC	—	Grond, Supply
9	Q'H	O	Serial Output
10	$\overline{SCLR}$	I	Shift Register cleared
11	SCK	I	Shift Register clocked
12	RCK	I	Output Register clocked
13	$\overline{G}$	I	Output state control
14	SER	I	Data input

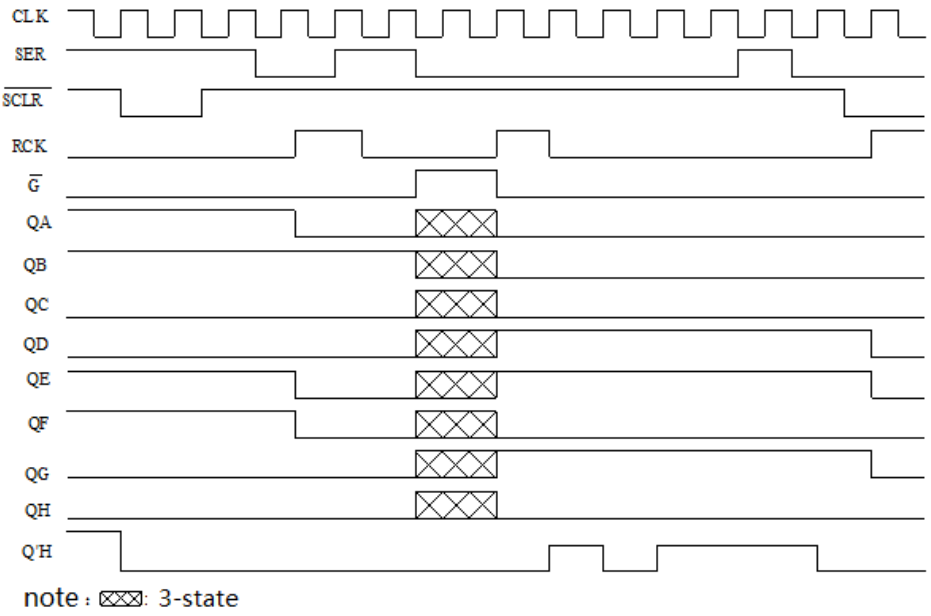
Truth Table

RCK	SCK	$\overline{SCLR}$	$\overline{G}$	Description
X	X	X	H	QA to QH = 3-STATE
X	X	L	L	Shift Register cleared,　Q'H =0
X	↑	H	L	Shift Register clocked,Q_N= Qn-1，Q0= SER
↑	X	H	L	Contents of Shift Register transferred to output latches

Logic Diagram



Timing Diagram



Absolute Maximum Ratings

Parameter	Symbol	Scope	Unit
Supply Voltage	V_{CC}	-0.5～7.0	V
DC Input Voltage	V_{IN}	-1.5～V_{CC}+1.5	V
DC Output Voltage	V_{OUT}	-0.5～V_{CC}+0.5	V
DC Output Current	I_{OUT}	±35	mA
DC V_{CC} or GND Current	I_{CC}	±70	mA
Power Dissipation	P_D	600	mW
Storage Temperature Range	T_{STG}	-65～150	℃

Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply Voltage	V_{CC}		2	6	V
DC Input or Output Voltage	V_{IN} ， V_{OUT}		0	V_{CC}	V
Input Rise or Fall Times	t_r , t_f	V_{CC}=2.0V		1000	ns
		V_{CC}=4.5V		500	
		V_{CC}=6.0V		400	
Operating Temperature Range	T_A		-40	+85	℃

Electrical Characteristics

DC Characteristics

Symbol	Parameter	Condition	V_{CC}	T_A=25℃		T_A=25 to 85℃	T_A=-55 to 125℃	Unit
				typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	
			6V		4.2	4.2	4.2	
V_{IL}	Maximum Low Level Input Voltage		2V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	
			6V		1.8	1.8	1.8	
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤20μA	2V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	
			6V	6	5.9	5.9	5.9	
	Q_H	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤4.0mA	4.5V	4.2	3.98	3.84	3.7	V
		| I_{OUT} | ≤5.2mA	6V	5.2	5.48	5.34	5.2	
	Q_A to Q_H	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤6.0mA	4.5V	4.2	3.98	3.84	3.7	V
		| I_{OUT} | ≤7.8mA	6.0V	5.7	5.48	5.34	5.2	
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤20μA	2V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	
			6V	0	0.1	0.1	0.1	
	Q_H	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤4.0mA	4.5V	0.2	0.26	0.33	0.4	V
		| I_{OUT} | ≤5.2mA	6V	0.2	0.26	0.33	0.4	
	Q_A to Q_H	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤6.0mA	4.5V	0.2	0.26	0.33	0.4	V
		| I_{OUT} | ≤7.8mA	6V	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3-STATE Output Leakage	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}	6V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT}= 0μA	6V		8.0	80	160	μA

AC Characteristics (V_{CC}=5V，T_A=25℃，t_r=t_f=6ns)

Symbol	Parameter	Condition	Typ	Guaranteed Limit	Unit
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL} t_{PLH}	Maximum Propagation Delay, SCK to QH'	C_L=45pF	12	20	ns
t_{PHL} t_{PLH}	Maximum Propagation Delay, RCK to QA thru QH	C_L=45pF	18	30	ns
t_{PZH} t_{PZL}	Maximum Output Enable Time from G to QA thru QH	R_L=1kΩ C_L=45pF	17	28	ns
t_{PHZ} t_{PLZ}	Maximum Output Disable Time from $\overline{G}$ to QA to QH	R_L=1kΩ C_L=5pF	15	25	ns
t_S	Minimum Setup Time from SER to SCK			20	ns
t_S	Minimum Setup Time from SCLR to SCK			20	ns
t_S	Minimum Setup Time from SCK to RCK			40	ns
t_H	Minimum Hold Time from SER to SCK			0	ns
t_W	Minimum Pulse Width of SCK or RCK			16	ns

AC Characteristics (V_{CC}=2.0～6.0V，C_L=50pF，t_r=t_f=6ns)

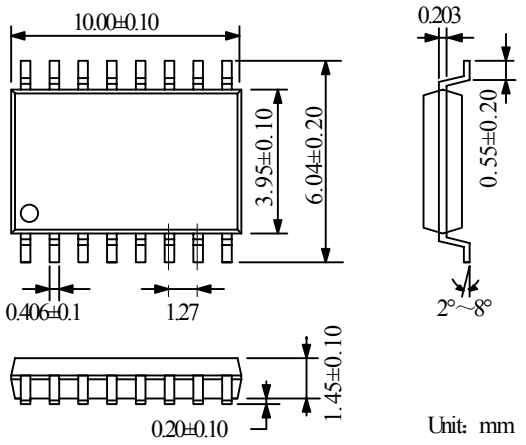
Symbol	Parameter	Condition	V_{CC}	T_A=25℃	T_A=25 to 85℃	T_A=-55 to 125℃		Unit
				Typ	Guaranteed Limit			
f_{MAX}	Maximum Operating Frequency	C_L=50pF	2V	10	6	4.8	4.0	MHz
			4.5V	45	30	24	20	
			6V	50	35	28	24	
t_{PHL} t_{PLH}	Maximum Propagation Delay from SCK to QH	C_L=50pF	2V	58	210	265	315	ns
		C_L=150pF	2V	83	294	367	441	
		C_L=50pF	4.5V	14	42	53	63	ns
		C_L=150pF	4.5V	17	58	74	88	
		C_L=50pF	6V	10	36	45	54	ns
		C_L=150pF	6V	14	50	63	76	
t_{PHL} t_{PLH}	Maximum Propagation Delay from RCK to QA thru QH	C_L=50pF	2V	70	175	220	265	ns
		C_L=150pF	2V	105	245	306	368	
		C_L=50pF	4.5V	21	35	44	53	ns
		C_L=150pF	4.5V	28	49	61	74	
		C_L=50pF	6V	18	30	37	45	ns

		C_L=150pF	6V	26	42	53	63	
t_{PHL} t_{PLH}	ximum Propagation delay from $\overline{SCLR}$ to QH		2V		175	221	261	ns
			4.5V		36	44	52	
			6V		30	37	44	
t_{PZH} t_{PZL}	Maximum Output Enable from $\overline{G}$ to QA thru QH	R_L=1kΩ C_L=50pF	2V	75	175	220	265	ns
		C_L=150pF	2V	100	245	306	368	
		C_L=50pF	4.5V	15	35	44	53	ns
		C_L=150pF	4.5V	20	49	61	74	
		C_L=50pF	6V	13	30	37	45	ns
		C_L=150pF	6V	17	42	53	63	
t_{PHZ} t_{PLZ}	Maximum Output Disable Time from $\overline{G}$ to QA thru QH	R_L=1kΩ C_L=50pF	2V	75	175	220	265	ns
			4.5V	15	35	44	53	
			6V	13	30	37	45	
t_S	Minimum Setup Time from SER to SCK		2V		100	125	150	ns
			4.5V		20	25	30	
			6V		17	21	25	
t_R	Minimum Removal Time from $\overline{SCLR}$ to SCK		2V		50	63	75	ns
			4.5V		10	13	15	
			6V		9	11	13	
t_S	Minimum Setup Time from SCK to RCK		2V		100	125	150	ns
			4.5V		20	25	30	
			6V		17	21	26	
t_H	Minimum Hold Time SER to SCK		2V		5	5	5	ns
			4.5V		5	5	5	
			6V		5	5	5	
t_W	Minimum Pulse Width of SCK or $\overline{SCLR}$		2V	30	80	100	120	ns
			4.5V	9	16	20	24	
			6V	8	14	18	22	
t_r t_f	Maximum Input Rise and Fall Time, Clock		2V		1000	1000	1000	ns
			4.5V		500	500	500	
			6V		400	400	400	
t_{THL} t_{TLH}	Maximum Output		2V	25	60	75	90	ns
			4.5V	7	12	15	18	

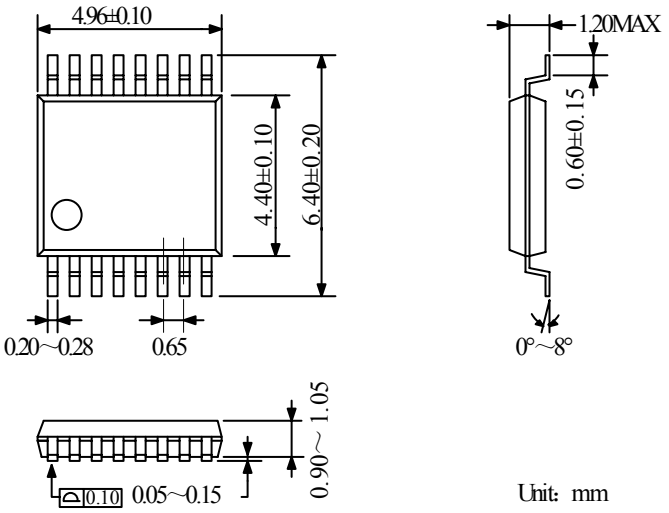
	Rise and Fall Time QA–QH		6V	6	10	13	15	
t_{THL} t_{TLH}	Maximum Output Rise & Fall Time QH		2V		75	95	110	ns
			4.5V		15	19	22	
			6V		13	16	19	
C_{PD}	Power Dissipation Capacitance, Outputs Enabled	$\overline{G}=V_{CC}$ $\overline{G}=GND$		90				pF
				150				
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Package Dimension

SOP16



TSSOP16



DIP16