Department of Computer Science & Engineering, NITK, Surathkal
Course Plan
CS250 – Computer Organization and Architecture

Course Objectives

1. Define the fundamental concepts in Architecture and Organization.
2. Introduce an Instruction Set Architecture and related concepts of a modern day computing device.
3. Provide a systematic treatment of the components in a modern Arithmetic Logic Unit, Processor Datapath, and Processor Control Unit.
4. Illustrate the various levels of the memory hierarchy and explain the concepts and the design of caches in detail.
5. Build a working system containing the fundamental units to execute simple programs

Course (Learning) Outcomes (COs)

CO1 – Outline the fundamental operations of a modern day computing device throught its Instruction Set Architecture.
CO2 – Explain the design and working of the different components in the ALU, Datapath and Control unit of a modern day computing device.
CO3 – Assess the use of various levels in the memory hierarchy of a modern day computing device.
CO4 – Design an ALU, Datapath and a Control unit for a modern day computing device in HDL.
CO5 – Design a full system for a modern day ISA and demonstrate working programs on it.

Table: CO200 – Course Coverage

Module – Title		**Content**
M1	Introduction to COA	Computer system and its submodules. Architecture vs. Organization. Frequency, Processor performance and power.
	PH-RV: Sections. 1.3-1.4, 1.6-1.7, Section A.7, Section 4.2, Sections 2.1 – 2.4.	
M2	Instruction Set Architecture	Addressing modes. Instruction classes. RISC-V ISA, MIPS and POWERPC LE ISA. Stages in compiling high level language programs. Structure of the object code. Procedure calls. Translating and starting a program. Assembly programming.
	PH-RV: Sections 2.5 – 2.10, 2.12, 2.18. PH-M: Sections 2.5 – 2.10, 2.12, 2.18. uPOWER ISA will be given in class.	
M3	Processor Datapath	Register File, Instruction memory, Data memory. A RISC-V datapath implementation. Datapath design using a HDL.
	PH-RV: Sections 4.1 – 4.4. Section A.8. PH-M: Sections 4.1 – 4.4. Section A.8.	
M4	Processor Control Unit	Instruction interpretation and execution. Combinatinal control, FSM Control, Microprogrammed control. Control Unit design using HDL.
	PH-RV: Appendix C. Section 4.4. PH-M: Appendix D. Section 4.4.	
M5	Memory Hierarchy	CPU – Memory interaction, organization of memory modules. Cache memory – Mapping and replacement policies.
	PH-RV: Sections 5.1 – 5.4.	
M6	I/O Subsystem	External Devices, I/O Modules, Programmed I/O, Interrupt-Driven I/O, Direct Memory Access, , I/O Channels and Processors, The External Interface: Thunderbolt and Infiniband.
	WS: Chapter 7	

Reference Texts

1. [PH-RV] David A Patterson and John L Hennessy. Computer Organization and Design – The Hardware/Software Interface. Elsevier, 2017, RISC-V edition).
2. [PH-M] David A Patterson and John L Hennessy. Computer Organization and Design – The Hardware/Software Interface. Elsevier, 2014, MIPS edition).
3. [WS] William Stallings, Computer organization and architecture - Designing for performance, 10th Ed. Pearson Ed. 2016.
4. [SRS] Smruti Ranjan Sarangi, Computer Organization & Architecture, McGraw Hill, 2014.
5. Noam Nisan and Shimon Schocken, The Elements of Computing Systems: Building a modern computer from first principles. MIT Press, 2005.
6. David M. Harris and Sarah L. Harris, Digital Design and Computer Architecture. 2e. Elsevier. 2013.

Related NPTEL Courses (http://www.nptel.ac.in):

- Matthew Jacob – High Performance Computing, IISc.
- Bhaskaran Raman – Computer Organisation and Architecture, IITB.
- V Kamakoti, Foundations of Computer Systems Design, IITM.

Course Evaluation (Tentative): Tutorials and Assignments – 30%, Quizzes – 10%, Midterm – 20%, Endsem – 40%.