Internal Memory

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Memory Technology Evolution

- All of the memory types that we will explore are random access, i.e., individual words of memory are directly accessed through wired-in addressing logic.
- In earlier computers, the most common form of random-access storage for computer main memory employed an array of doughnut-shaped ferromagnetic loops referred to as *cores*. Hence, main memory was often referred to as *core*.
- Today, the use of semiconductor chips for main memory is almost universal.

Key Aspects of Semiconductor Technology

- Organization
- RAM
- ROM
- Chip Logic
- Chip Packaging
- Module Organization
- Interleaved Memory

Organization

- The basic element of a semiconductor memory is the memory cell.
- All semiconductor memory cells share certain properties:
  a) They exhibit two stable (or semistable) states, which can be used to represent binary 1 and 0.
  b) They are capable of being written into (at least once), to set the state.
  c) They are capable of being read to sense the state.

Memory Cell Operation

- Figure 1 depicts the operation of a memory cell.
- The cell has three functional terminals capable of carrying an electrical signal.

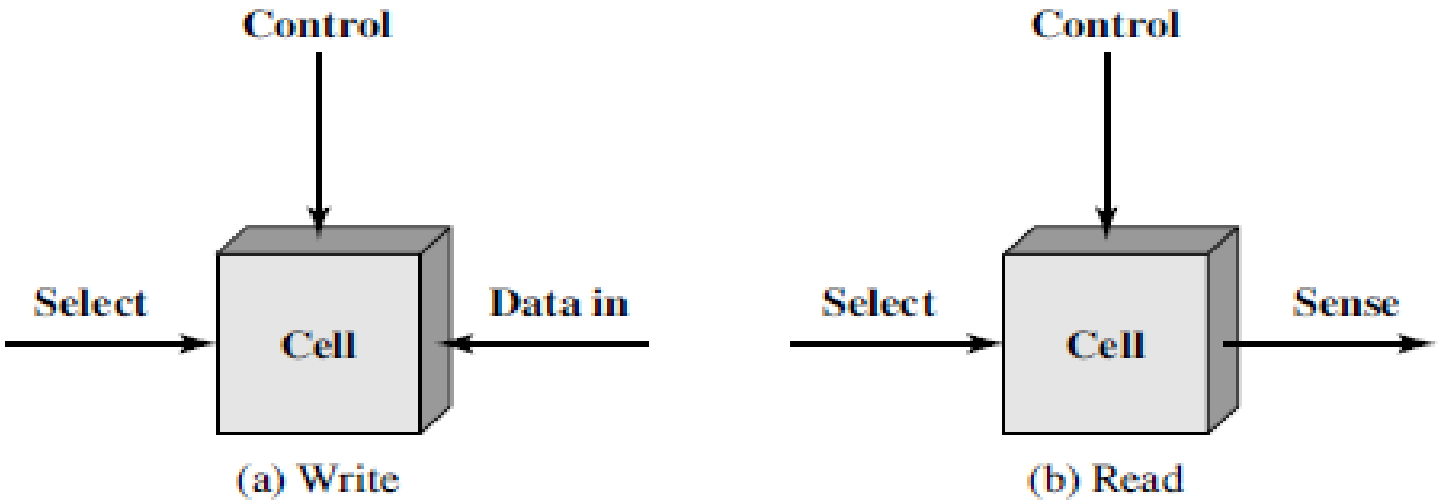

Figure 1: The operation of a memory cell.

Memory Cell Operation Contd…

- The select terminal selects a memory cell for a read or write operation.
- The control terminal indicates read or write.
- For writing, the other terminal provides an electrical signal that sets the state of the cell to 1 or 0.
- For reading, that terminal is used for output of the cell's state.

Random Access Memory

- The most common semiconductor memory is referred to as *random-access memory* (RAM).
- One distinguishing characteristic of RAM is that it is possible both to read data from the memory and to write new data into the memory easily and rapidly.
- Both the reading and writing are accomplished through the use of electrical signals.
- Another distinguishing characteristic is that it is volatile.
- A RAM must be provided with a constant power supply.
- If the power is interrupted, then the data are lost.
- RAM can be used only as temporary storage.

RAM Contd...

- The two basic forms of semiconductor random access memory are dynamic RAM (DRAM) and static RAM (SRAM).
- SRAM is faster, more expensive, and less dense than DRAM, and is used for cache memory.
- DRAM is used for main memory.
- Both static and dynamic RAMs are volatile.

SRAM

- A static RAM (SRAM) is a digital device that uses the same logic elements used in the processor.
- In a SRAM, binary values are stored using traditional flip-flop logic-gate configurations
- A static RAM will hold its data as long as power is supplied to it.

Static RAM Properties

- Bits stored as on/off switches
- No charges to leak
- No refreshing needed when powered
- More complex construction
- Larger per bit
- More expensive
- Does not need refresh circuits
- Faster
- Cache
- Digital
  - Uses flip-flops

DRAM

- DRAM is made with cells that store data as charge on capacitors.
- The presence or absence of charge in a capacitor is interpreted as a binary 1 or 0.
- Capacitors have a natural tendency to discharge.
- Dynamic RAMs require periodic charge refreshing to maintain data storage.
- The term *dynamic* refers to this tendency of the stored charge to leak away, even with power continuously applied.

Dynamic RAM Properties

- Bits stored as charge in capacitors
- Charges leak
- Need refreshing even when powered
- Simpler construction
- Smaller per bit
- Less expensive
- Need refresh circuits
- Slower
- Main memory
- Essentially analogue
  - Level of charge determines value

Refreshing

- Because capacitors have a natural tendency to discharge, DRAMs require periodic charge refreshing to maintain data storage.
- Refresh circuit included on chip
- A simple technique for refreshing is “Disable chip”, in effect, to disable the DRAM chip while all data cells are refreshed.
- The data are read out and written back into the same location.
- The technique takes time
- It slows down apparent performance.

Advanced DRAM Organization

- Basic DRAM same since first RAM chips
- Enhanced DRAM
  - Contains small SRAM as well
  - SRAM holds last line read
- Cache DRAM
  - Larger SRAM component
  - Use as cache or serial buffer

Synchronous DRAM (SDRAM)

- Access is synchronized with an external clock
- Address is presented to RAM
- RAM finds data (CPU waits in conventional DRAM)
- Since SDRAM moves data in time with system clock, CPU knows when data will be ready
- CPU does not have to wait, it can do something else
- Burst mode allows SDRAM to set up stream of data and fire it out in block
- DDR-SDRAM sends data twice per clock cycle (leading & trailing edge)

SRAM vs. DRAM

A. Both volatile
   - Power needed to preserve data

B. Dynamic cell
   - Simpler to build, smaller
   - More dense
   - Less expensive
   - Needs refresh
   - Larger memory units

C. Static
   - Faster
   - Cache

Read Only Memory

- A **read-only memory** (ROM) contains a permanent pattern of data that cannot be changed.
- A ROM is nonvolatile, i.e., no power source is required to maintain the bit values in memory.
- While it is possible to read a ROM, it is not possible to write new data into it.
- An important application of ROMs is microprogramming.
- Other potential applications include
  - Library subroutines for frequently wanted functions
  - System programs
  - Function tables

ROM Contd…

- The advantage of ROM is that the data or program is permanently in main memory and need never be loaded from a secondary storage device.
- The disadvantage of ROM includes
  - The data insertion step includes a relatively large fixed cost, whether one or thousands of copies of a particular ROM are fabricated.
  - There is no room for error. If one bit is wrong, the whole batch of ROMs must be thrown out.
- A less expensive alternative is the **programmable ROM** (PROM).
- Like the ROM, the PROM is nonvolatile and may be written into only once.

ROM Contd...

- There are three common forms of read-mostly memory:
  - erasable programmable read-only memory (EPROM)
  - electrically erasable programmable read-only memory (EEPROM).
  - flash memory.
- EPROM is read and written electrically, as with PROM.
- A more attractive form of read-mostly memory is EEPROM. This can be written into at any time without erasing prior contents; only the byte or bytes addressed are updated.
- The flash memory is intermediate between EPROM and EEPROM in both cost and functionality.

Major Types of Semiconductor Memory

<table>
<tr><th>Memory Type</th><th>Category</th><th>Erasure</th><th>Write Mechanism</th><th>Volatility</th></tr>
<tr><td>Random-access memory (RAM)</td><td>Read-write memory</td><td>Electrically, byte-level</td><td>Electrically</td><td>Volatile</td></tr>
<tr><td>Read-only memory (ROM)</td><td rowspan="2">Read-only memory</td><td rowspan="2">Not possible</td><td>Masks</td><td rowspan="6">Nonvolatile</td></tr>
<tr><td>Programmable ROM (PROM)</td><td rowspan="4">Electrically</td></tr>
<tr><td>Erasable PROM (EPROM)</td><td rowspan="3">Read-mostly memory</td><td>UV light, chip-level</td></tr>
<tr><td>Electrically Erasable PROM (EEPROM)</td><td>Electrically, byte-level</td></tr>
<tr><td>Flash memory</td><td>Electrically, block-level</td></tr>
</table>

Chip Logic

- As with other integrated circuit products, semiconductor memory comes in packaged chips.
- Each chip contains an array of memory cells.
- The array is organized into W words of B bits each. For example, a 16-Mbit chip could be organized as 1M 16-bit words.
- At the other extreme is the so-called 1-bit-per-chip organization, in which data are read/written 1 bit at a time.

Chip Packaging

- An integrated circuit is mounted on a package that contains pins for connection to the outside world.
- Figure 2 shows an example EPROM package.
- The package is an 8-Mbit chip organized as 1Mx8.
- In this case, the organization is treated as a one-word-per-chip package.
- The package includes 32 pins, which is one of the standard chip package sizes.

Chip Packaging Contd…

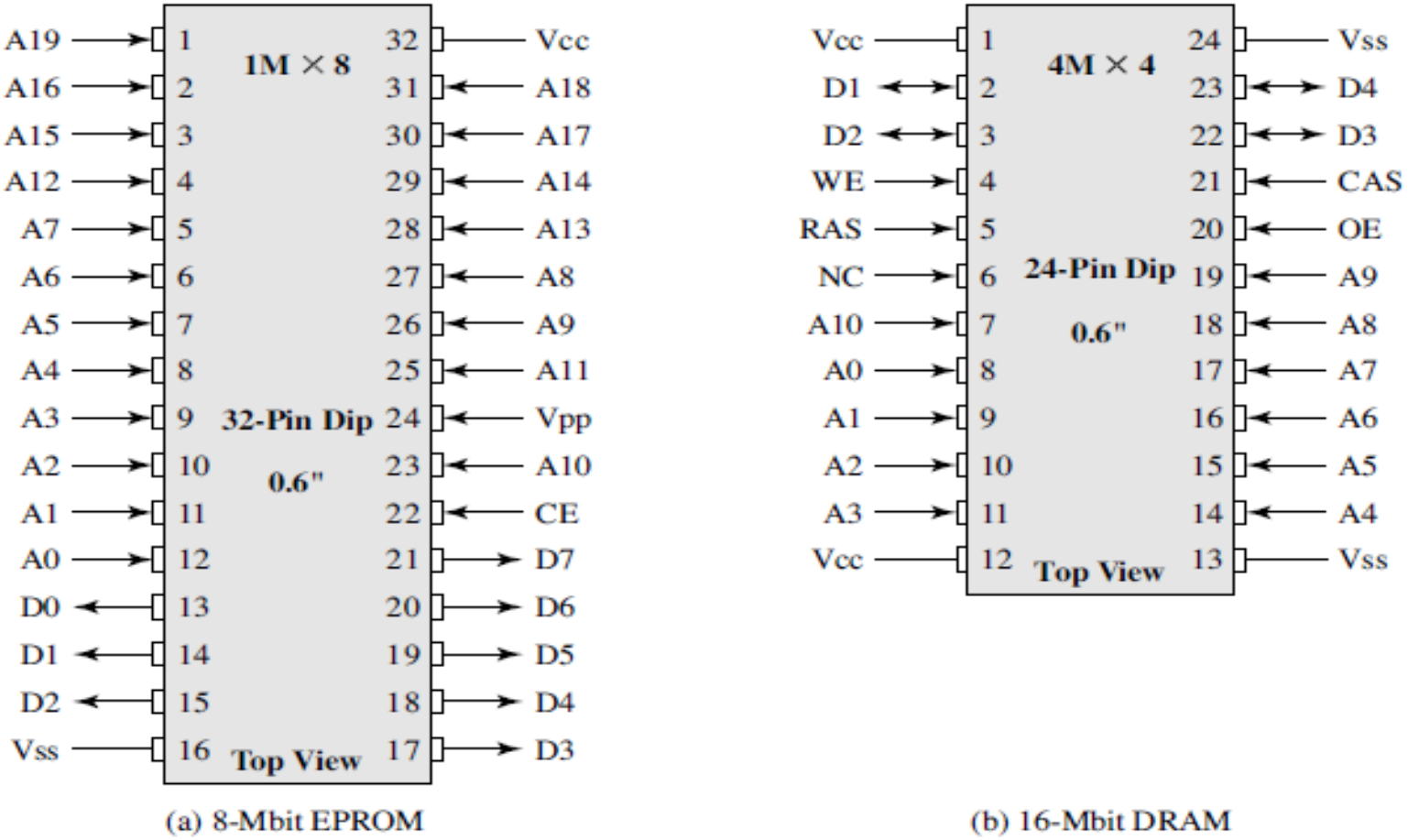

Figure 2. Typical Memory Package Pins and Signals

Module Organization

- If a RAM chip contains only 1 bit per word, then clearly we will need at least a number of chips equal to the number of bits per word.
- For 256K words, an 18-bit address is needed and is supplied to the module from some external source (e.g., the address lines of a bus to which the module is attached).
- The address is presented to 8 256Kx1-bit chips, each of which provides the input/output of 1 bit.
- This organization works as long as the size of memory equals the number of bits per chip.

Interleaved Memory

- Main memory is collection of DRAM chips.
- A number of chips can be grouped together to form a *memory bank*.
- Banks independently service read or write requests.
- K banks can service K requests simultaneously increasing memory read or write rates by a factor of K.
- If consecutive words of memory are stored in different banks, then the transfer of a block of memory is speeded up.
- It is possible to organize the memory banks in a way known as *interleaved memory*.
- Each bank is now independently able to service.

Thank You