Know all about Latches and Flip Flops

Latches and flip flops are the basic elements and these are used to store information. One flip flop and latch can store one bit of data. The main difference between the latches and flip flops is that, a latch checks input continuously and changes the output whenever there is a change in input. But, flip flop is a combination of latch and clock that continuously checks input and changes the output time adjusted by the clock. In this article, we are going to look at the operations of the numerous latches and flip-flops.

Latches and Flip Flops

Both Latches and flip flops are circuit elements wherein the output not only depends on the current inputs, but also depends on the previous input and outputs. The main difference between the latch and flip flop is that a flip flop has a clock signal, whereas a latch does not. Basically, there are four types of latches and flip flops: SR, D, JK and T. The major differences between these types of flip flops and latches are the number of inputs they have and how they change the states. There are different variations for each type of latches and flip-flops which can enhance their operations.

Difference between Latches and Flip Flops

Latches	Flip Flops
Latches are building blocks of sequential circuits and these can be built from logic gates	Flip flops are also building blocks oof sequential circuits. But, these can be built from the latches.
Latch continuously checks its inputs and changes its output correspondingly.	Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal
The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on	Flipflop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip flops are used as a register.
It is based on the enable function input	It works on the basis of clock pulses
It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.	It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.

What is Flip Flop?

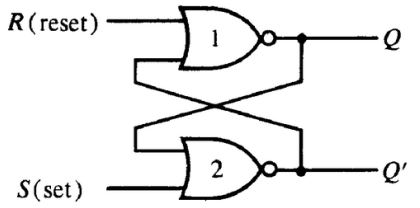
A flip flop can be designed by using two NOR gates or two NAND gates. A basic flip flop using NAND gate is shown below. Each flip flop has two inputs set and reset and also two outputs Q and Q'. This type of flip flop is referred to as an SR flip flop or SR latch.

The flip-flop has two states which are shown in the below figure. When Q=1; and Q'=0; it is in the set state. When Q=0 & Q'=1, it is in the clear state. The outputs of the flip flop Q & Q' are complements of each other and are referred to as the normal and complement outputs, respectively. The flip flop binary state is taken to be the value of the normal output.

When 1 is applied to the inputs of the flip flop, both the outputs go to 0, so both the outputs are complements of each other. In a normal operation, this condition must be avoided by making sure that 1's are not applied to both the inputs simultaneously.

SR Flip Flop

This SR flip-flop consists of two AND gates and a basic NOR flip-flop. The outputs of the two AND gates remain at 0 as long as the clock pulse is 0, irrespective of the input values of S & R. When the clock pulse is 1, information from the inputs S & R passes through to the basic flip-flop. When S=R=1, the occurrence of a clock pulse causes both the outputs go to 0. When the clock pulse is removed, the state of the flip-flop is unstated.



(a) Logic diagram

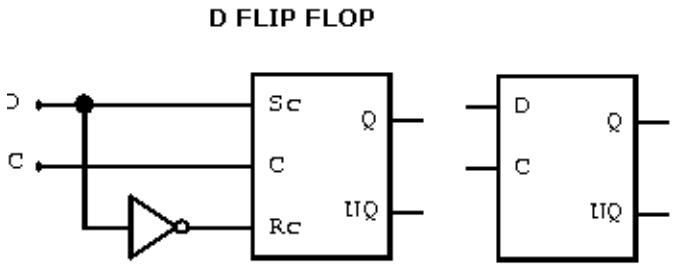
S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

(b) Truth table

SR Flip Flop

D Flip Flop

The D flip-flop is the modification of the SR flip flop which is shown in the figure. The input D goes directly into the input S and the complement of the input D goes to the input R. The D input is sampled during the existence of a clock pulse. If it is 1, then the flip-flop is switched to the set state. If it is 0, then the flip-flop switches to the clear state.

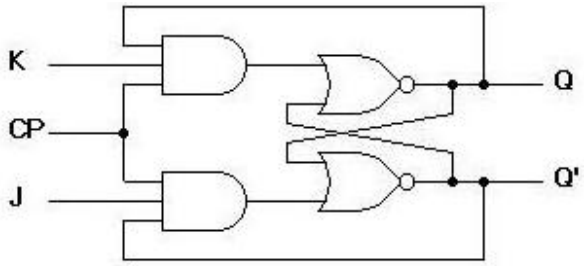


D	C	Q	$\overline{Q}$
x	0	no change	
0	p	0	1
1	p	1	0

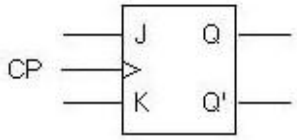
D Flip Flop

JK Flip Flop

A JK flip flop is a modification of the SR flip flop. The inputs of the flip flop J, K behave like the inputs S and R. When input 1 is applied to both J & K, the flip flop switches to its complement state (if Q=1, it switches to Q=0). The JK flip flop figure is shown below. The output of the flip flop Q is ANDed with inputs k and clock pulse. The flip flop would be cleared during a clock pulse only if the output Q was previously 1. Likewise, the output Q' is ANDed with inputs CP and J. So that the flip flop is set with a clock pulse only if Q' was previously 1.



(a) Logic diagram



(b) Graphical symbol

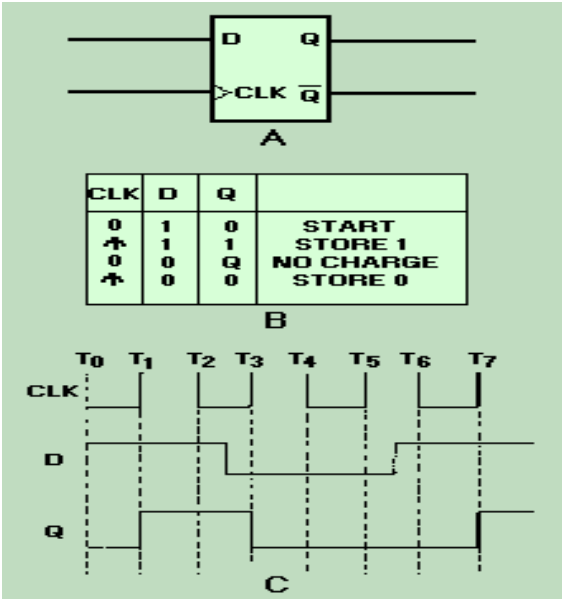
Q J K	Q(t+1)
0 0 0	0
0 0 1	0
0 1 0	1
0 1 1	1
1 0 0	1
1 0 1	0
1 1 0	1
1 1 1	0

(c) Transition table

JK Flip Flop

T Flip Flop

The T flip flop is a single input version of the JK flip flop. The operation of this T flip flop is as follows: When the input of the T is ‘0’ such that the ‘T’ will make the next state the same as the present state (i.e. T = 0 then, present state = next state = 0). However, if the input of the T is ‘1’ then the ‘T’ will change the next state to the inverse of the present state (i.e. T = 1 present state = 0 and next state = 1).



T Flip Flop

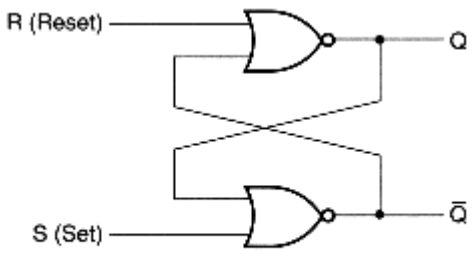
What is Latch?

Latches are asynchronous – which means, the output of the latch depends on its input; on the other hand, today, most computers are synchronous – which means, the outputs of all the sequential circuits change simultaneously to the rhythm of a global clock signal. There are four types of latches: D, T, SR and JK latch.

SR Latch

A set/ reset latch is an asynchronous device, which relies on the state of the S&R inputs. This latch can be made from NOR gates. The latch has memory and the output depends on the state of the latch. Therefore, the output at nth instant denoted by Qn is dependent on the output at (n-1)th instant, denoted by (Qn-1).

Note that when the SR=11 state, then both the outputs are 0, which seems absurd. Thus, the state SR=11 is said to be "not allowed". The latch $(SR)^{-}$ is a similar latch to SR which can be made from the NAND gates.



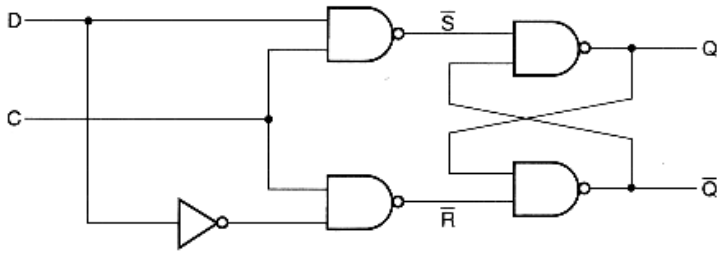
(a) Logic diagram

S	R	Q	$\bar{Q}$	
1	0	1	0	Set state
0	0	1	0	
0	1	0	1	Reset state
0	0	0	1	
1	1	0	0	Undefined

(b) Function table

D Latch

The D latch is the simple extension of the gated SR latch which removes the possibility of invalid input states. When the enable line of the D latch is high, the output will always reflect the logic level which is present at the D input. When the input of the D latch falls, the last state of the D latch input is trapped and held in the latch. That is why it is also called as a transparent latch. When enable is asserted, the latch is said to be transparent.



(a) Logic diagram

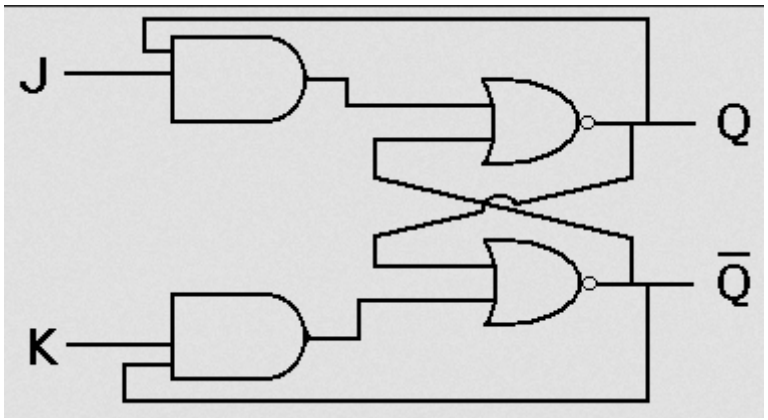
C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

(b) Function table

D Latch

JK Latch

JK latch is similar to RS latch. This latch consists of 2 inputs J and K as shown in the below figure. The ambiguous state has been eliminated here: when the inputs of Jk latch are high, then output toggles. The output feedback to inputs is the only difference we see here, which is not there in the RS latch.

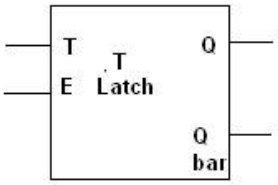


JK Latch

T Latch

T latch is formed when the inputs of the JK latch are shorted. When the input is high, then the output toggles.

		Previous		New	
T	E	Q	Q (bar)	Q	Q (bar)
X	0	X	X	PREVIOUS VALUES	
0	1	0	1	0	1
0	1	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1



T Latch

These are all different types of latches and flip flops.