Hardware Implementation of Addition and Subtraction

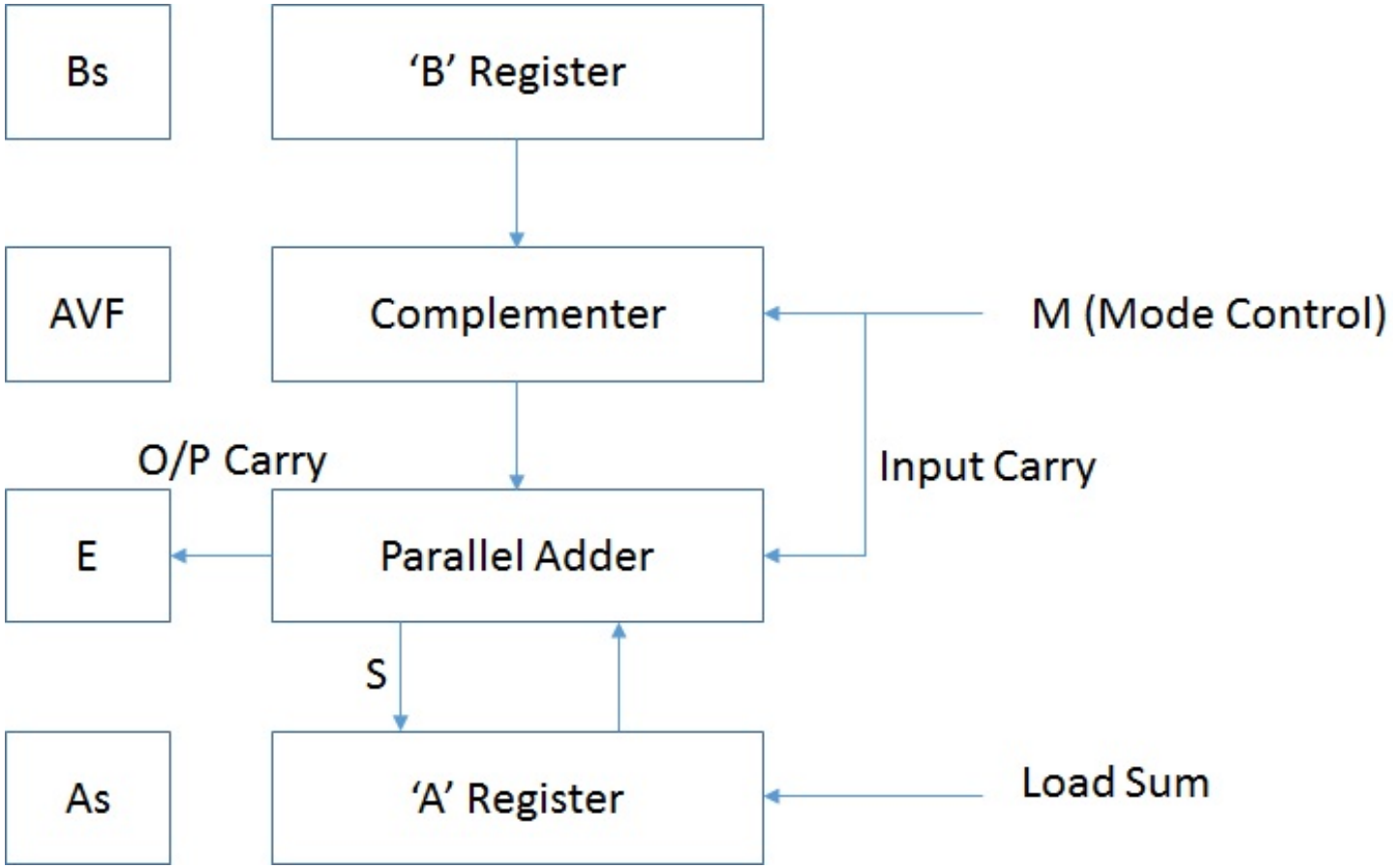

Figure: Hardware for Signed Magnitude Addition and Subtraction

Hardware for signed-2's complement addition and subtraction

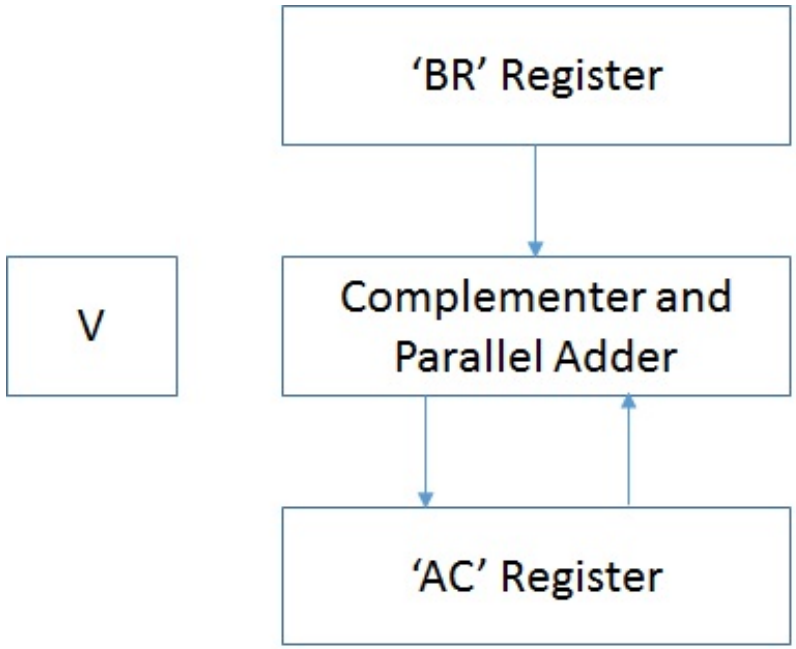

Figure: Hardware for signed-2's complement addition and subtraction

Algorithm for Addition and subtraction in signed 2's complement

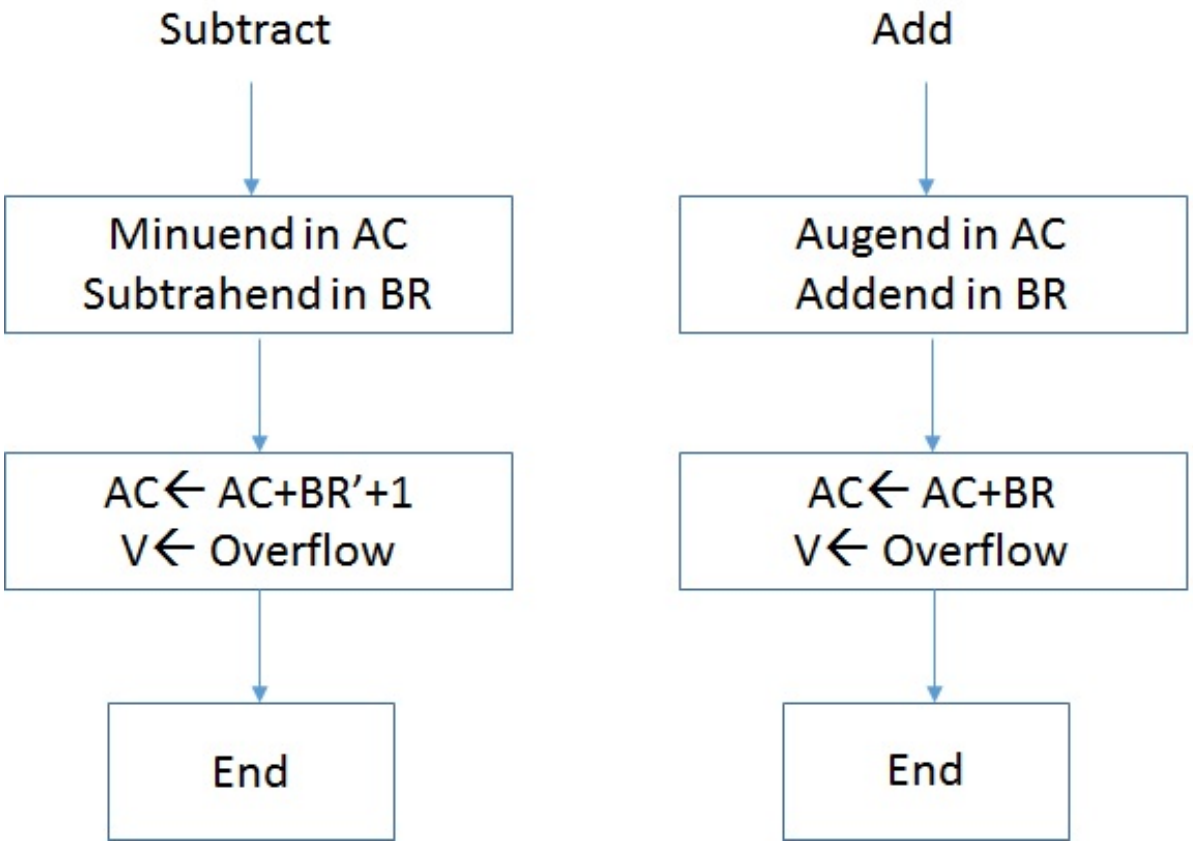

Figure: Algorithm for Addition and subtraction in signed 2's complement representation

Registers for floating point arithmetic operations

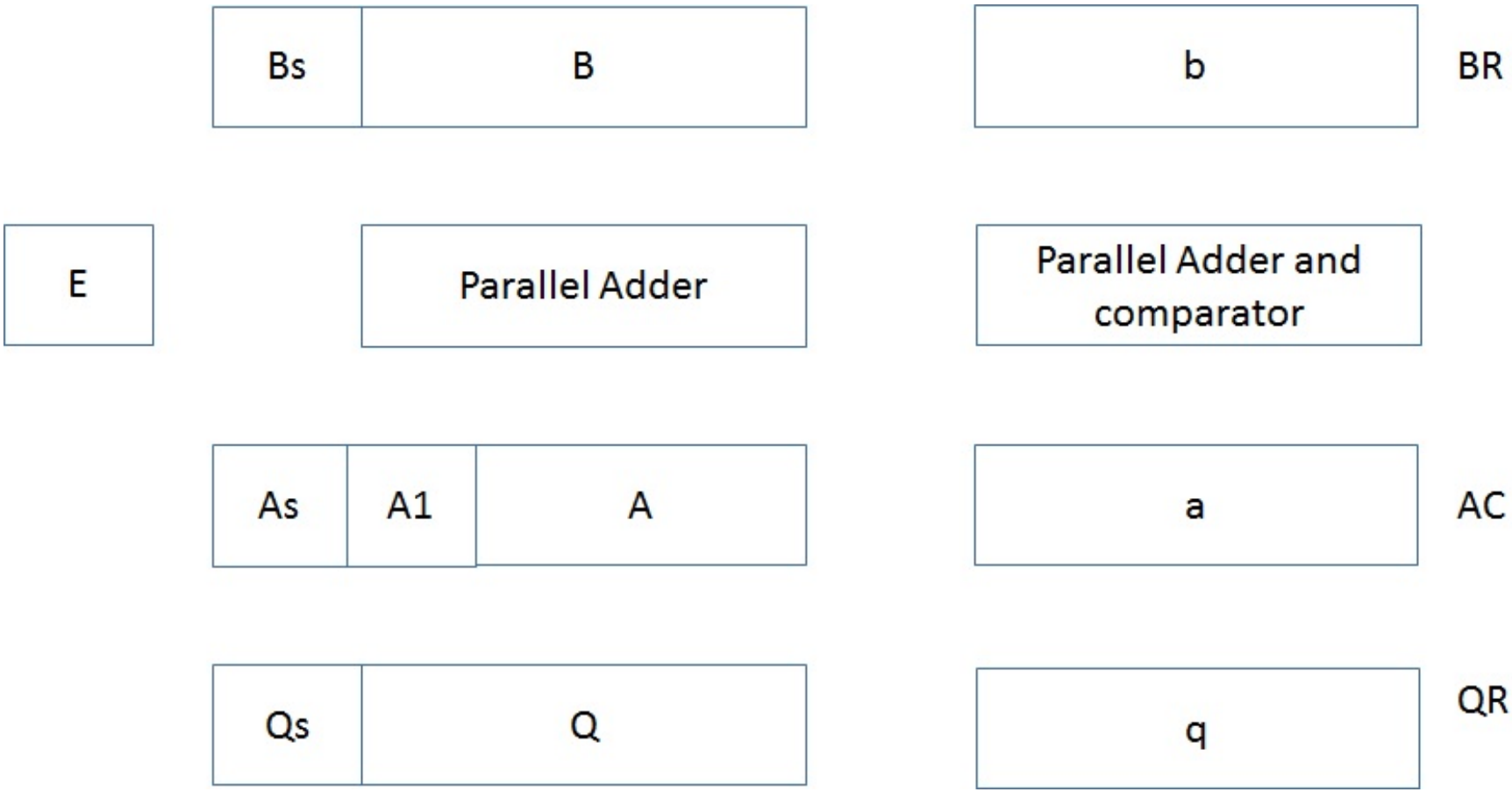

Figure: Registers for floating point arithmetic operations