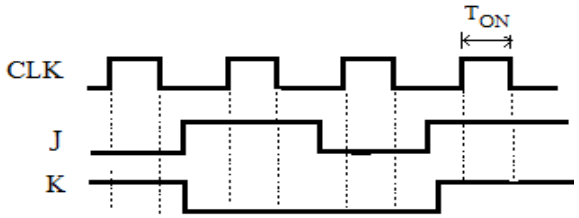
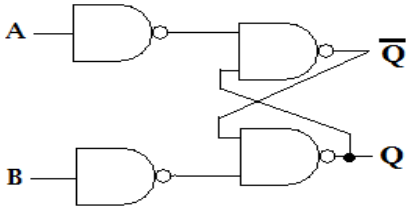
S. V. National Institute of Technology, Surat

B.Tech (II) CO **3rd** Semester Tuto –1 SEPT. 2016

EC207: DIGITAL CIRCUITS

Q.1	Draw the waveform of Q and Q' for following clocked J K latch. Assume that latch toggles only once in single clock cycle if latch finds itself in toggle state. 	
Q.2	Obtain characteristic table of following latch and briefly explain its operation. 	
Q.3	Draw clocked D latch using AND and NOR gates only. Obtain its characteristic table. Write its characteristic equation when clock is High and when clock is LOW.	