S.V. National Institute of Technology, Surat

B.Tech (II) CO,3RD Sem Endsem Exam Dec. 2014

EC207: DIGITAL CIRCUITS

Time: **3Hr**.] [Total Marks: **100**

Q.1 (a) Perform following operation without converting numbers to any other base. **[4]**
(1) $(345)_7 + (603)_7$ (2) $(538)_{13} - (203)_{13}$

(b) (i) Obtain 8x1 multiplexer using 2x1 multiplexers and inverters. **[6]**
(ii) Realize 4x16 decoder using only 1x2 decoders (having enable input).

(c) Draw octal to binary priority encoder. Include an output V to indicate that at least one input is 1. **[4]**

(d) Design logic circuit that generates 9's complement of input BCD digit. **[4]**

(e) Simplify following functions using tabulation (Quine-McCluskey) method. **[8]**
$F(A,B,C,D,E) = \sum m\,(6,9,13,18,19,25,27)$

Q.2 (a) Design a BCD to Excess-3 code converter using minimum number of NAND gates **[4]**

(b) Design and sketch singleb bit full adder/subtractor circuit with one additional control input M such that when M=0 it acts as full adder and when M=1 it acts as full subtractor. **[6]**

(c) Implement the following function using (i)8x1Mux (ii)4x1 Mux **[6]**
$f(w,x,y,z) = wx' + w' x z' + x'y'z + x'yz$

(d) Derive the PLA programming table for the combinational circuit that multiplies two 2-bit input binary numbers. Minimize the number of product terms. **[8]**

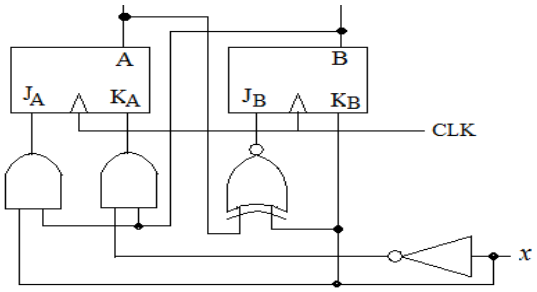
Q.3 (a) Draw the logic circuit *mod-13 ripple* counter using positive edge triggered T flip-flops. **[4]**

(b) Implement 4-bit shift register using D flip-flops and multiplexers that uses 2-bit control signal S_1S_0. Realize four register operations: 00 (parallel load), 01 (shift left), 10 (shift right) and 11 (no change) **[4]**

(c) Draw logic circuit of 3-bit synchronous parallel counter using JK flip-flops. Write expression of minimum clock period? Draw waveforms of clock and output of each flip-flop for 6 clock cycles. **[6]**

(d) Design and implement sequence generator that generate sequence **10011010** and repeat. **[8]**

(e) Obtain state table and draw state diagram for following logic circuit. Initial state of the circuit is **00**. **[6]**



Q.4 (a) Design synchronous counter that generates sequence 1,7,2,5,3 and repeat. Make sure that counter is automatically reset when any unused state occurs. **[8]**

(b) Draw the logic circuit of edge triggered D flip-flop that uses *three basic flip-flops* and explain its operation. What do you mean by setup time and hold time? **[6]**

(c) A 24-bit floating-point *binary* number has 9 bits for exponent and 15 bits for coefficient. The coefficient is assumed to be a normalized fraction. The binary numbers in coefficient and exponent are in sing-magnitude form. (i)What are the largest and smallest positive quantities that can be accommodated, excluding zero? (ii) Represent quantities $(+23.25)_{10}$ and $(-67.125)_{10}$ using this presentation. **[4]**

OR

Perform following arithmetic operations using 8-bit signed binary numbers represented in 2's complement form. Write binary value of carry into and out of sing-bit position, overflow bit and sign bit (8^{th} bit) of result in each case.
(i) $(+68)_{10} + (+76)_{10}$ (ii) $(+68)_{10} + (-76)_{10}$

(d) Using 4-bit registers with parallel load capability, a quadruple 4x1 multiplexer and logic gates, draw the logic diagram to implement following RTL statements. **[4]**

T_0: R1←R2, T_1: R1←$\overline{R2}$, T_2: R1←0000, T_3: R1←R1 ∧ R2