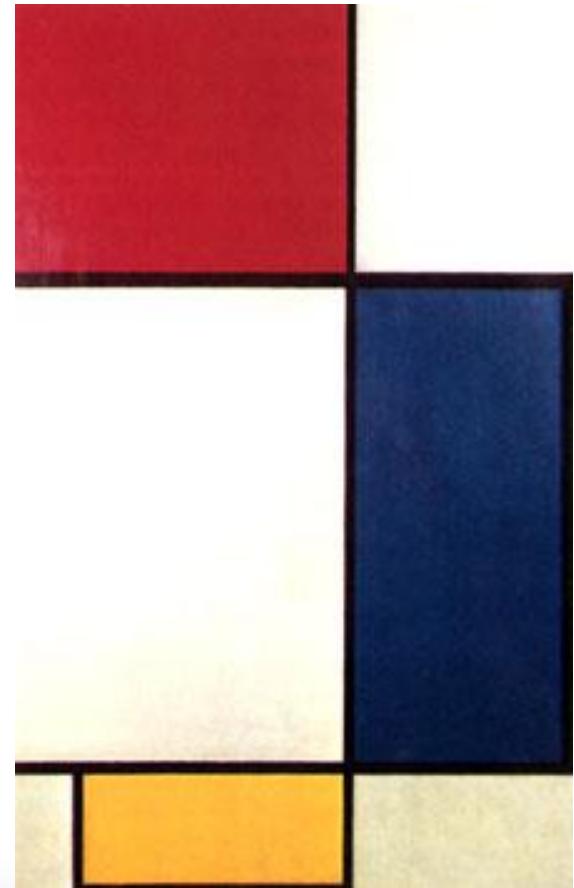


# *Design for Test*



# *Validation and Test of Manufactured Circuits*

## **Goals of Design-for-Test (DFT)**

**Make testing of manufactured part swift and comprehensive**

## **DFT Mantra**

**Provide controllability and observability**

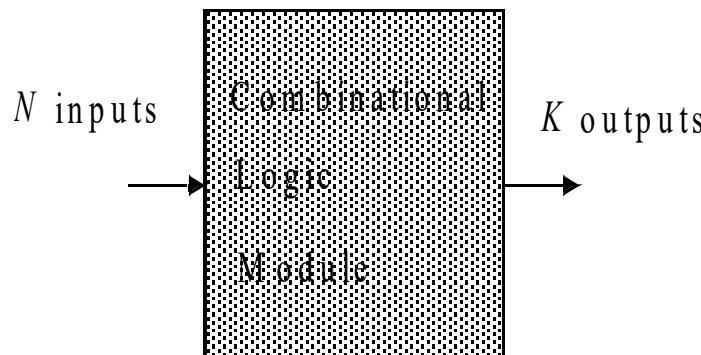
## **Components of DFT strategy**

- Provide circuitry to enable test**
- Provide test patterns that guarantee reasonable coverage**

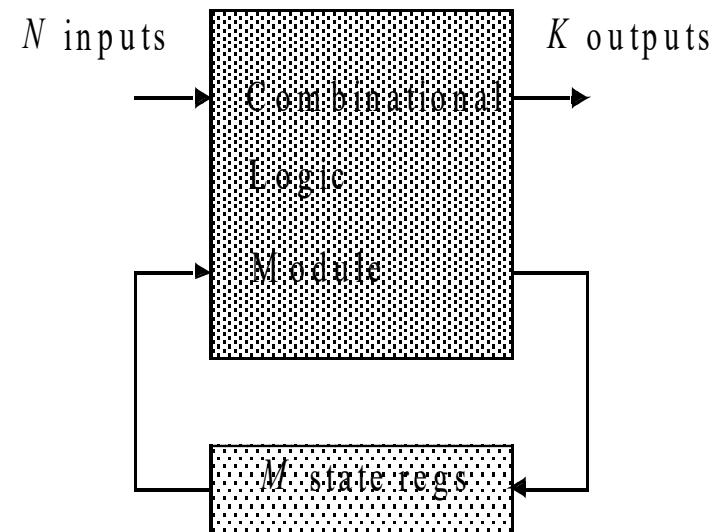
# *Test Classification*

- Diagnostic test
  - used in chip/board debugging
  - defect localization
- “go/no go” or production test
  - Used in chip production
- Parametric test
  - $x \in [v,i]$  versus  $x \in [0,1]$
  - check parameters such as NM,  $V_t$ ,  $t_p$ , T

# *Design for Testability*



(a) Combinational function



(b) Sequential engine

$2^N$  patterns

$2^{N+M}$  patterns

**Exhaustive test is impossible or unpractical**

# **Problem:**

## **Controllability/Observability**

- Combinational Circuits:  
controllable and observable - relatively easy to determine test patterns
- Sequential Circuits: State!  
Turn into combinational circuits or use self-test
- Memory: requires complex patterns  
Use self-test

# *Test Approaches*

- Ad-hoc testing
- Scan-based Test
- Self-Test

Problem is getting harder

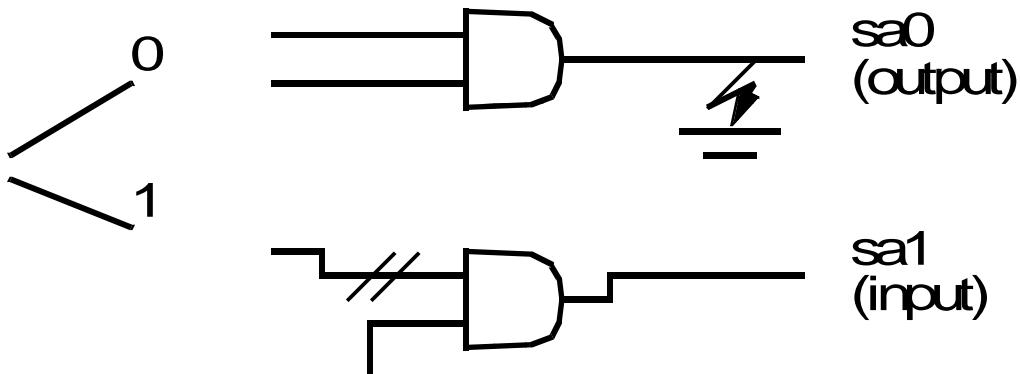
- increasing complexity and heterogeneous combination of modules in system-on-a-chip.
- Advanced packaging and assembly techniques extend problem to the board level

# *Generating and Validating Test-Vectors*

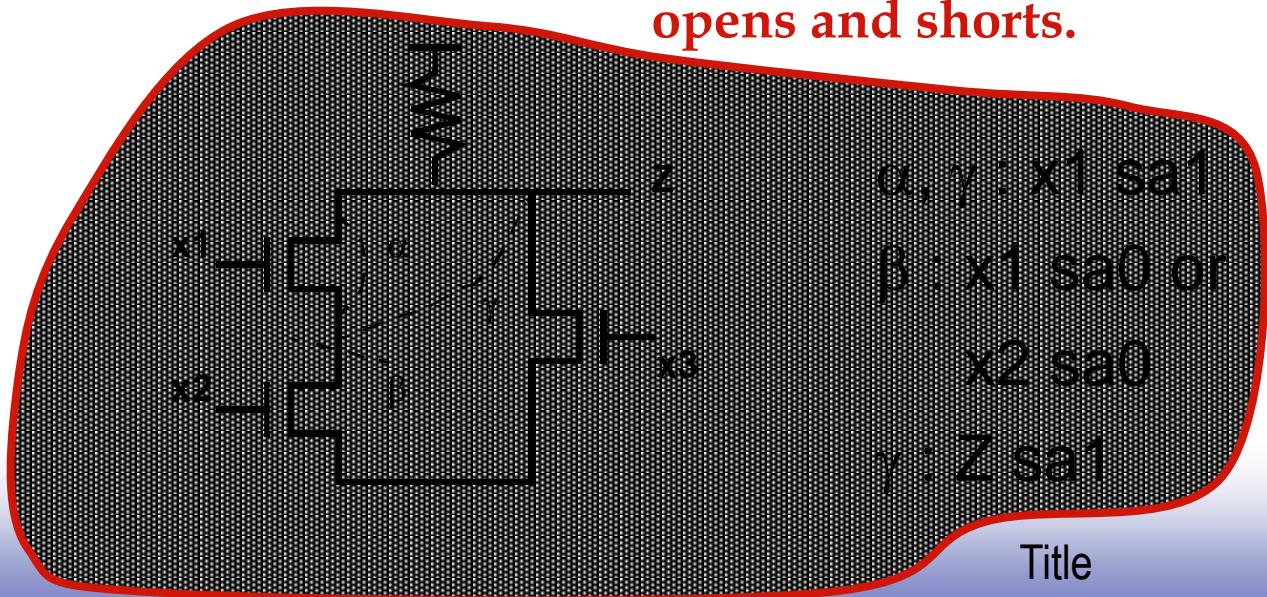
- Automatic test-pattern generation (ATPG)
  - for given fault, determine excitation vector (called **test vector**) that will propagate error to primary (observable) output
  - majority of available tools: combinational networks only
  - sequential ATPG available from academic research
- Fault simulation
  - determines **test coverage** of proposed test-vector set
  - simulates correct network in parallel with faulty networks
- Both require adequate models of faults in CMOS integrated circuits

# Fault Models

Most Popular - “Stuck - at” model



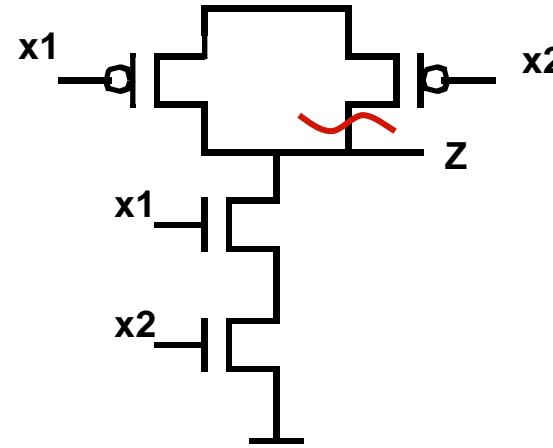
Covers almost all (other) occurring faults, such as opens and shorts.



# *Problem with stuck-at model: CMOS open fault*



$x_1$	$x_2$	$z$
0	x	1
1	1	0
1	0	$z_{n-1}$



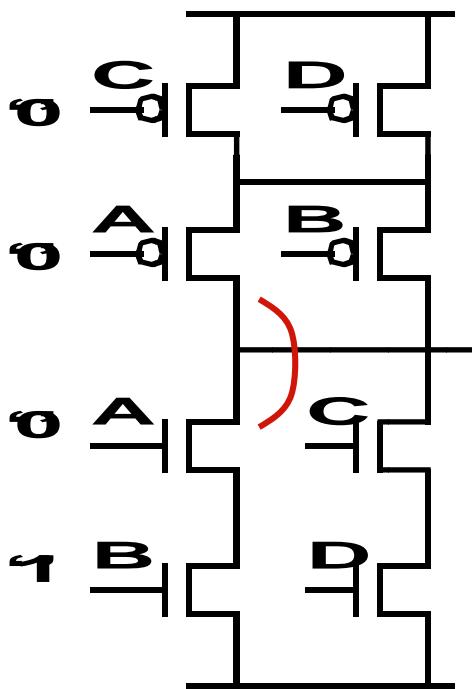
**Sequential effect**

**Needs two vectors to ensure detection!**

**Other options: use stuck-open or stuck-short models**

**This requires fault-simulation and analysis at the switch or transistor level - Very expensive!**

# *Problem with stuck-at model: CMOS short fault*

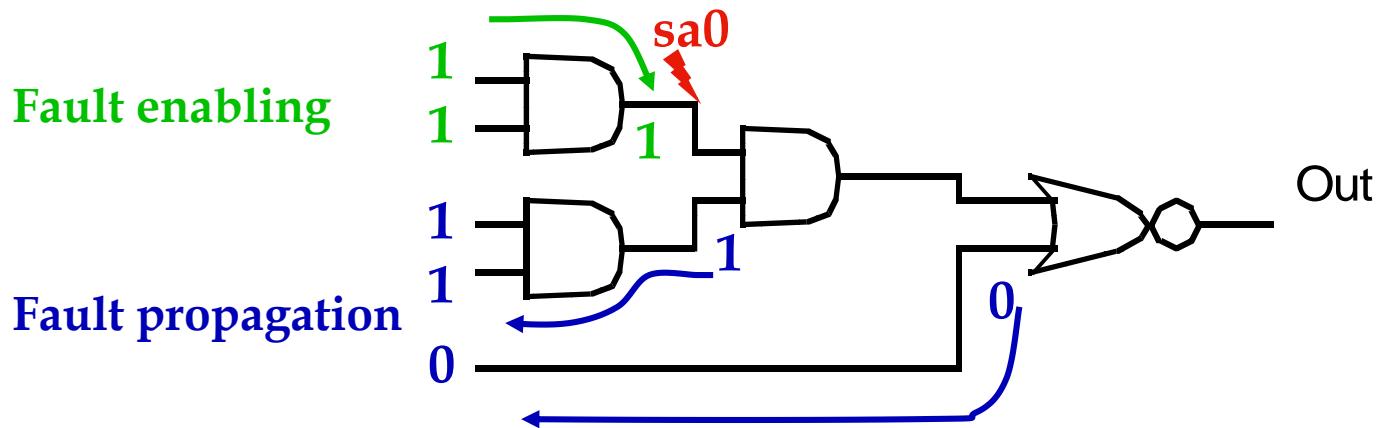


Causes short circuit between  
Vdd and GND for  $A=C=0, B=1$

Possible approach:  
Supply Current Measurement (IDQ)  
but: not applicable for gigascale  
integration

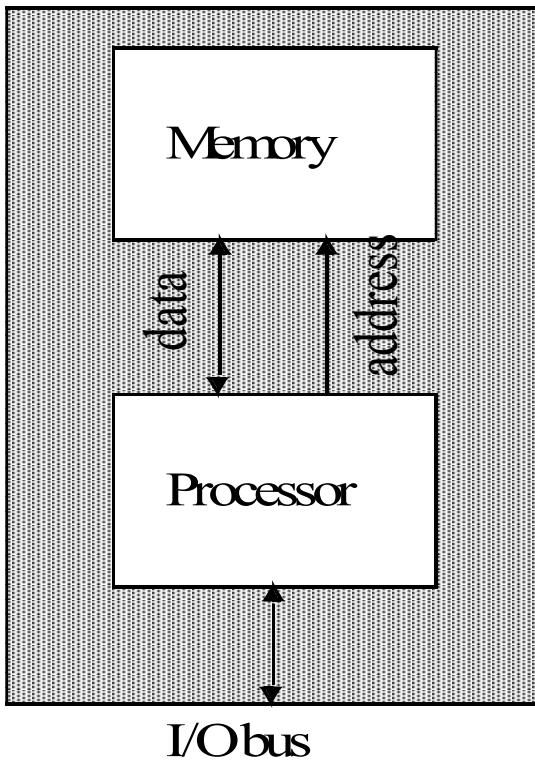
# Path Sensitization

Goals: Determine input pattern that makes a fault controllable (triggers the fault, and makes its impact visible at the output nodes)

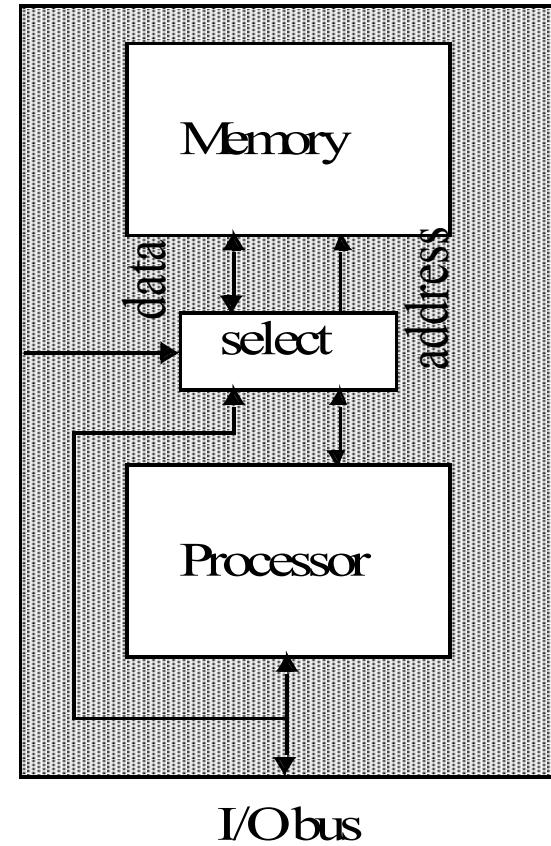


Techniques Used: D-algorithm, Podem

# Ad-hoc Test

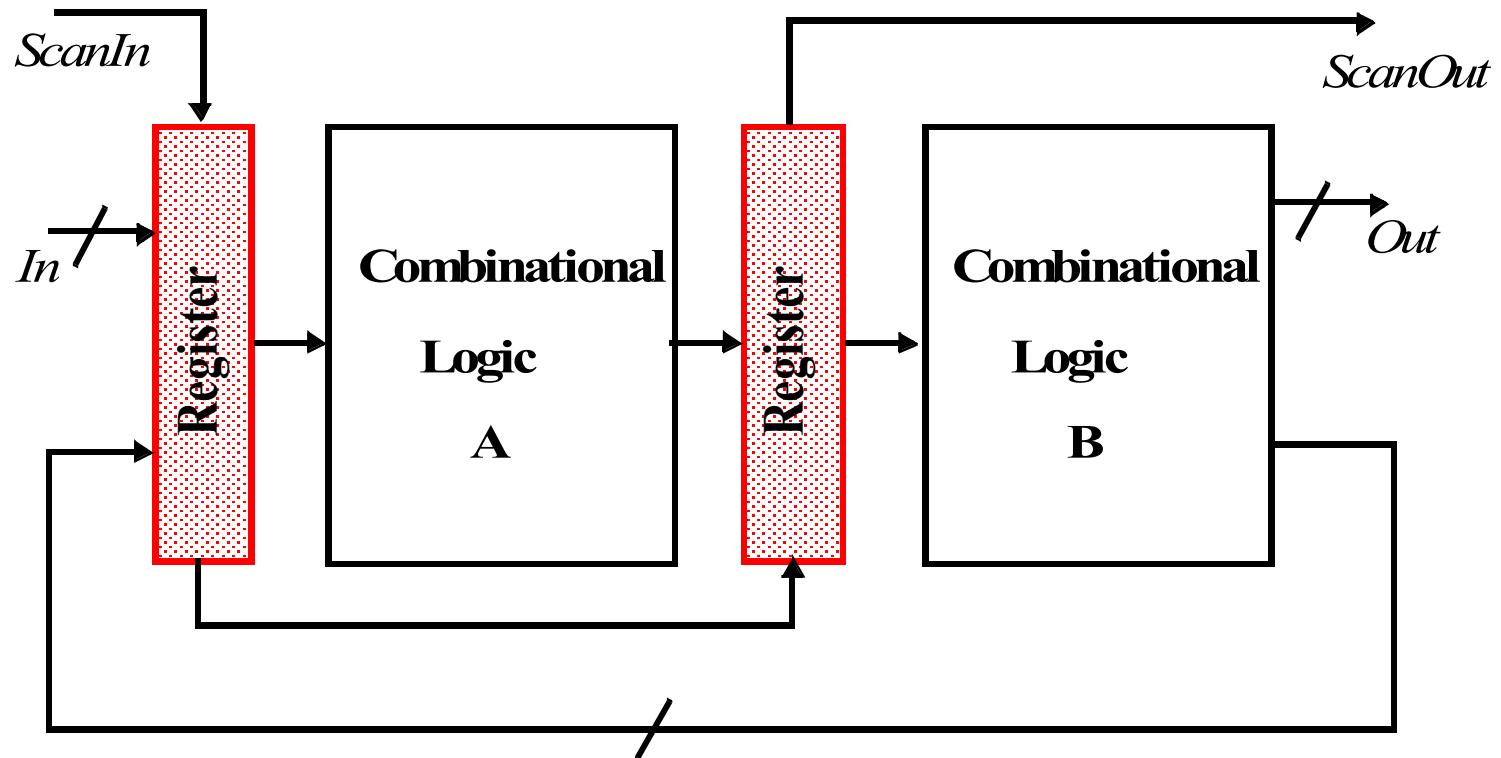


*test*

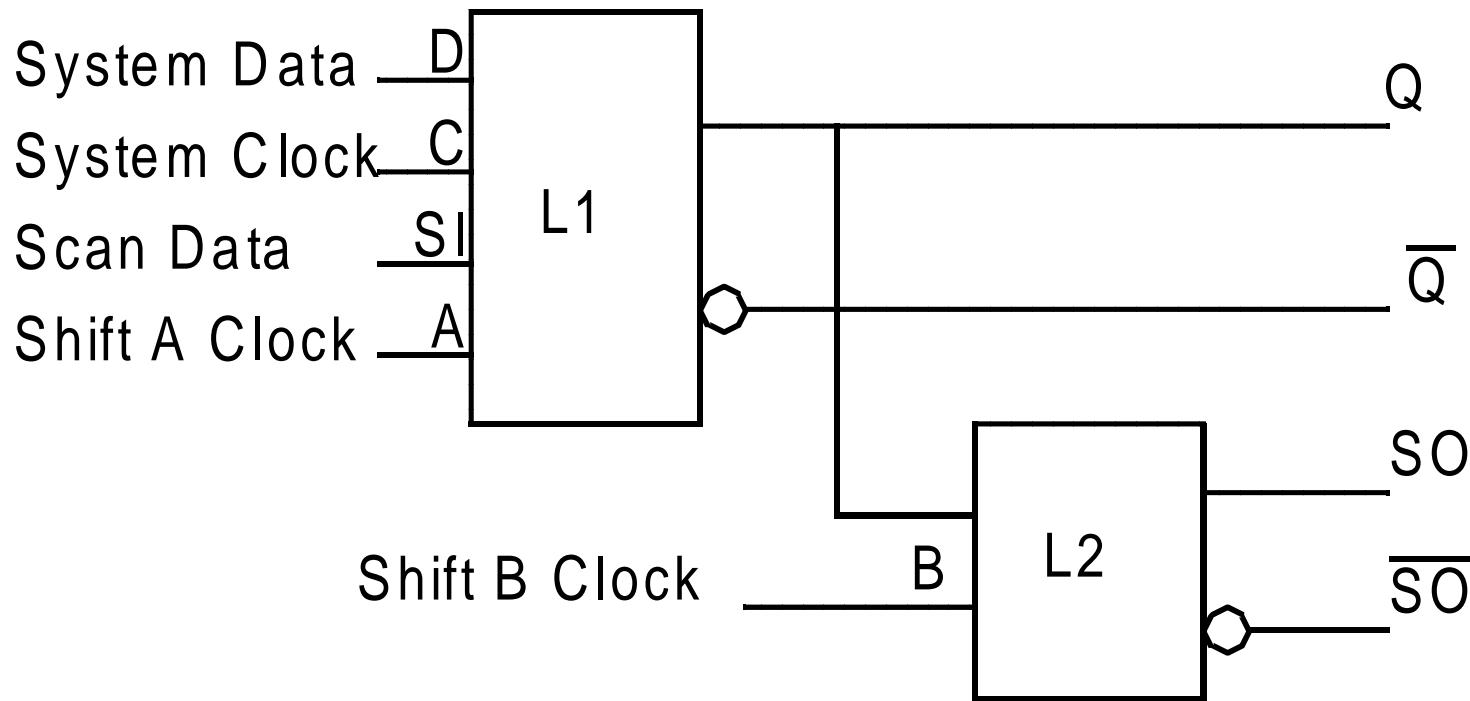


**Inserting multiplexer improves testability**

# *Scan-based Test*

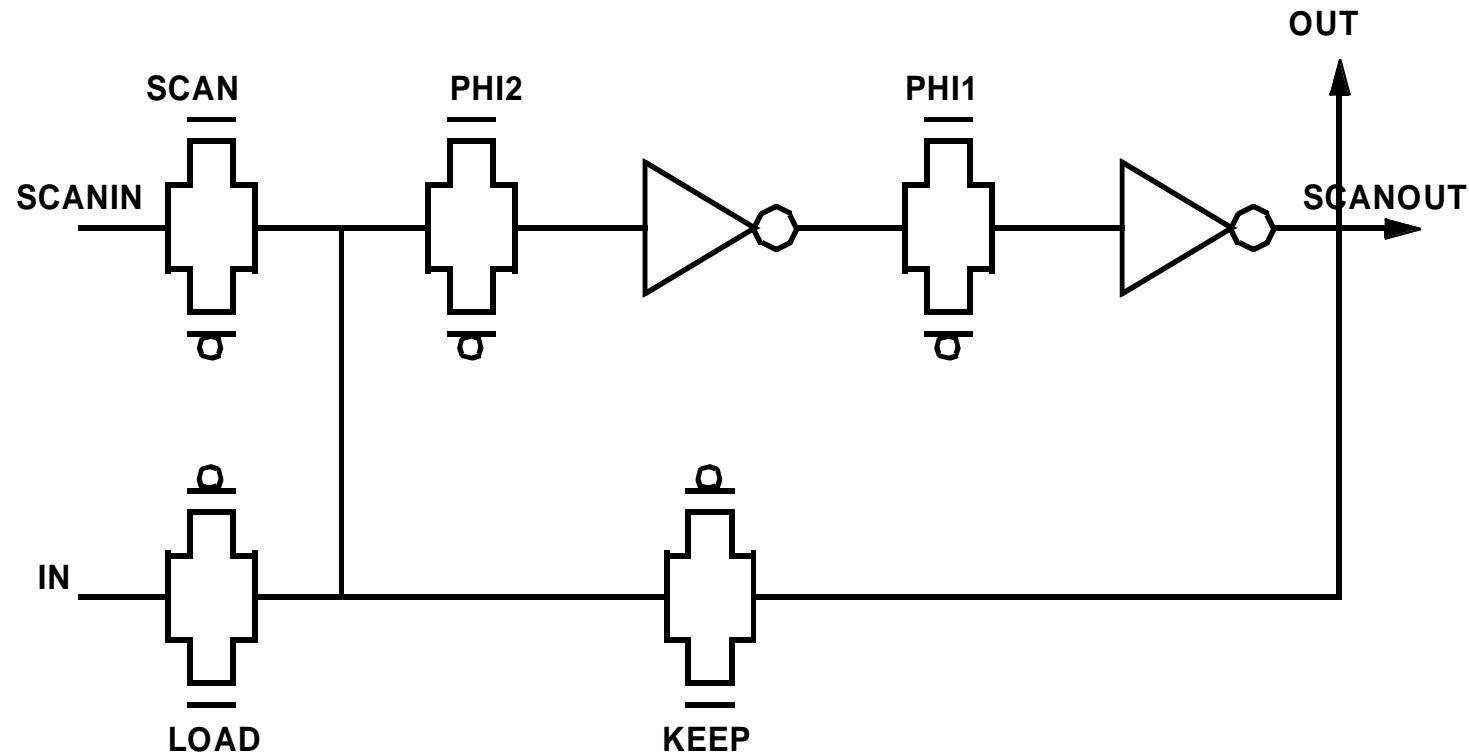


# Polarity-Hold SRL (Shift-Register Latch)

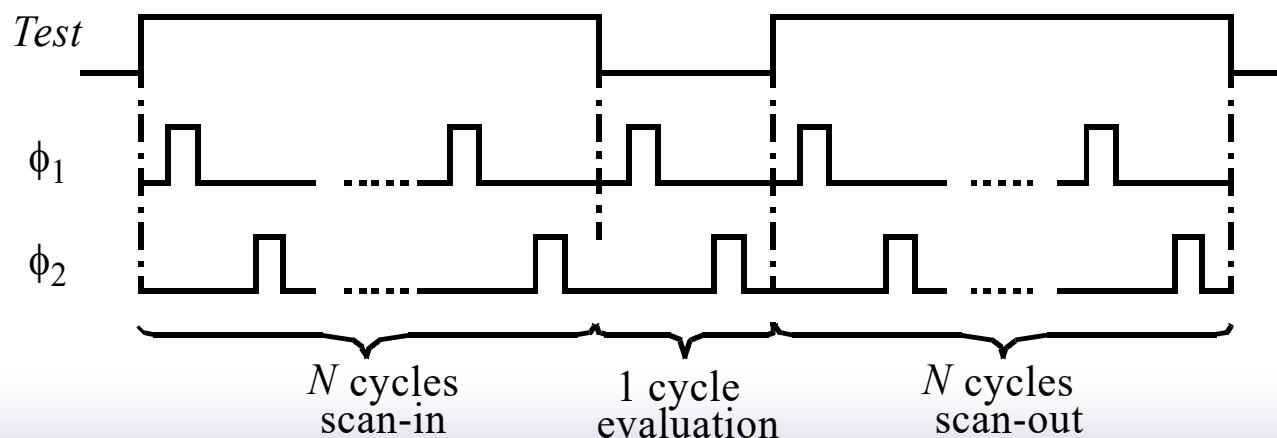
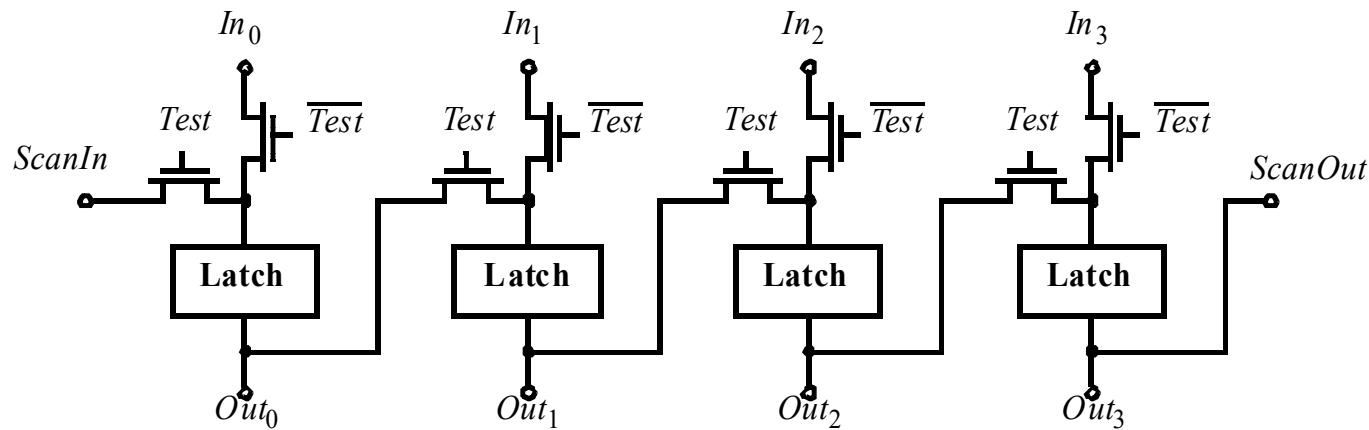


Introduced at IBM and set as company policy

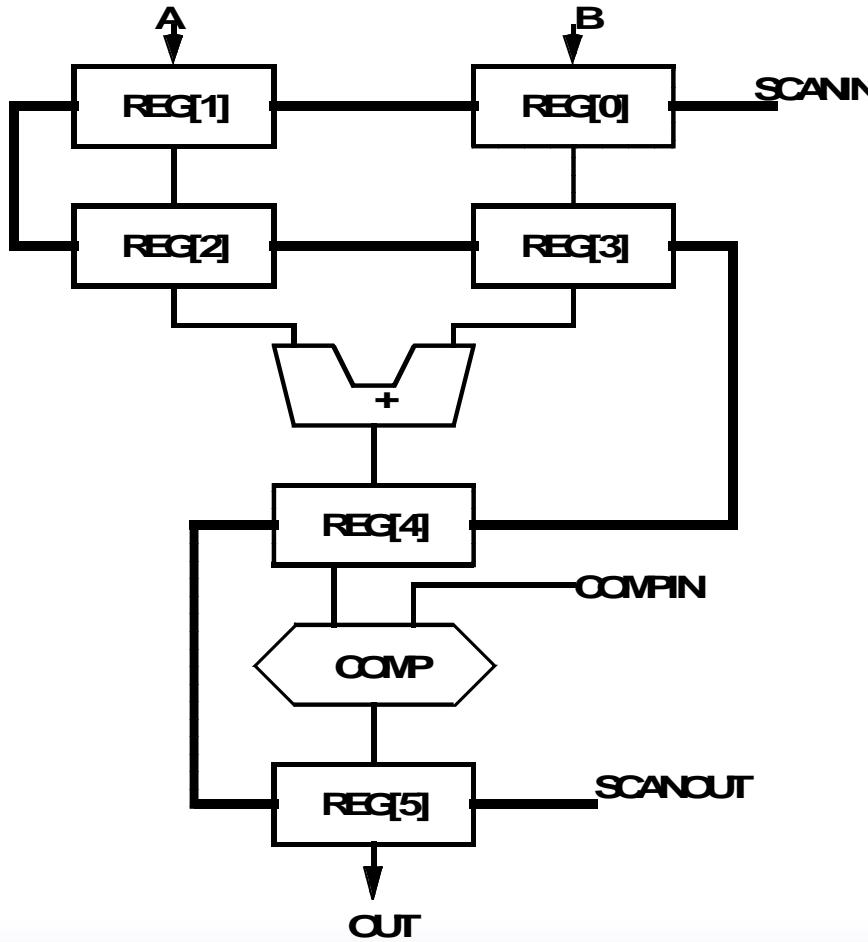
# *Scan-Path Register*



# Scan-based Test — Operation

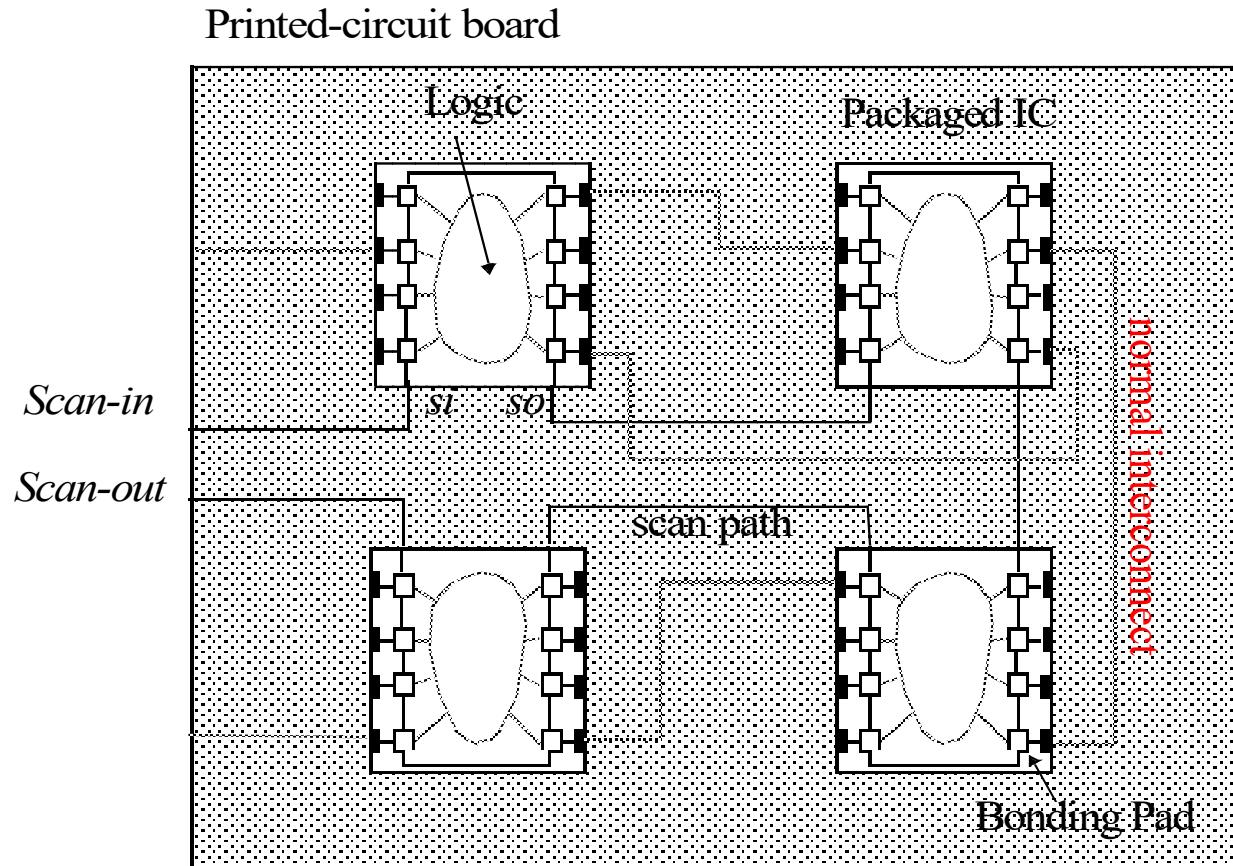


# Scan-Path Testing



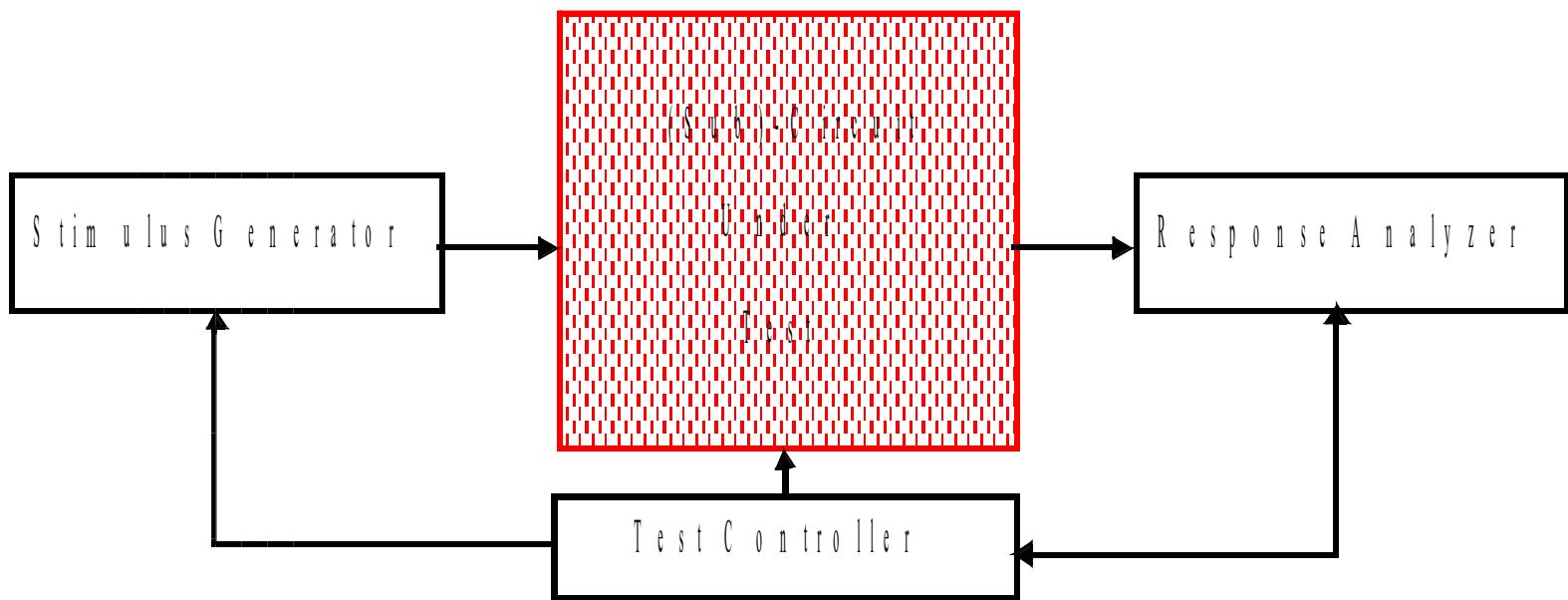
Partial-Scan can be more effective for pipelined datapaths

# *Boundary Scan (JTAG)*



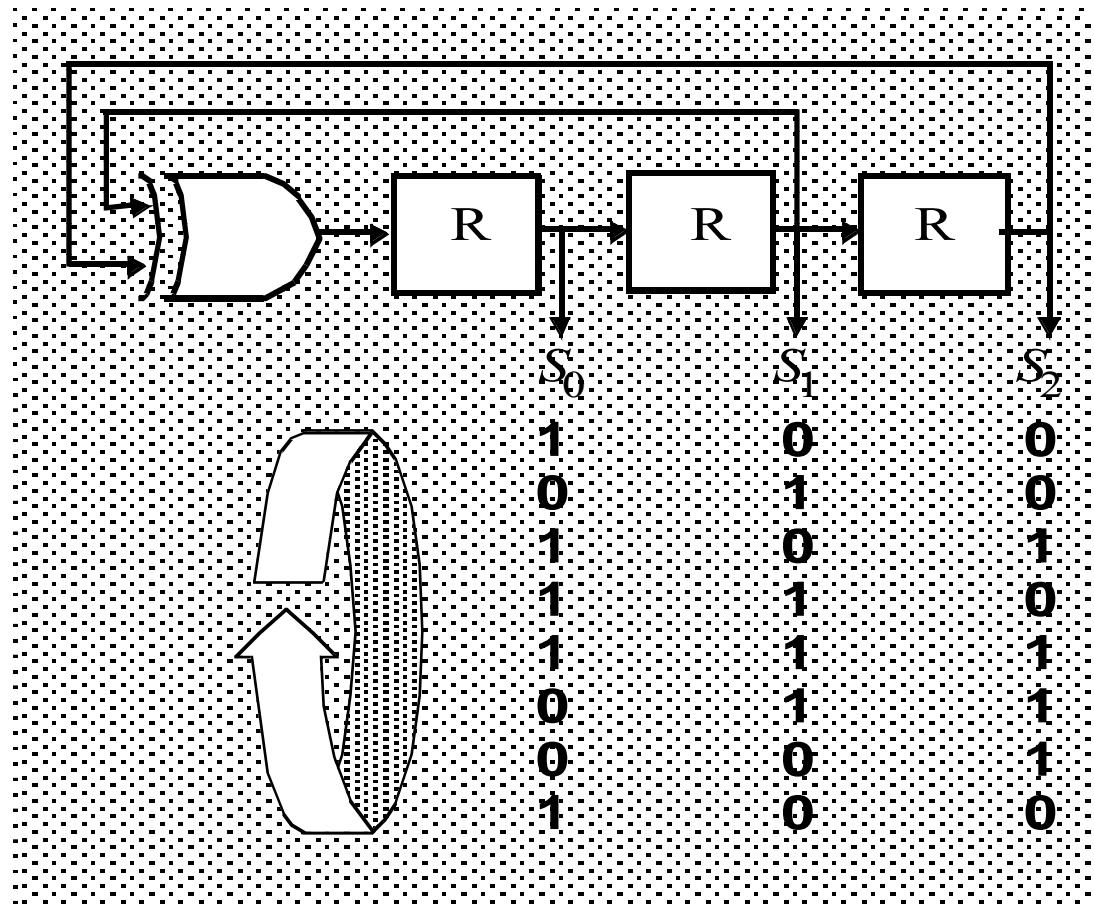
**Board testing becomes as problematic as chip testing**

# Self-test



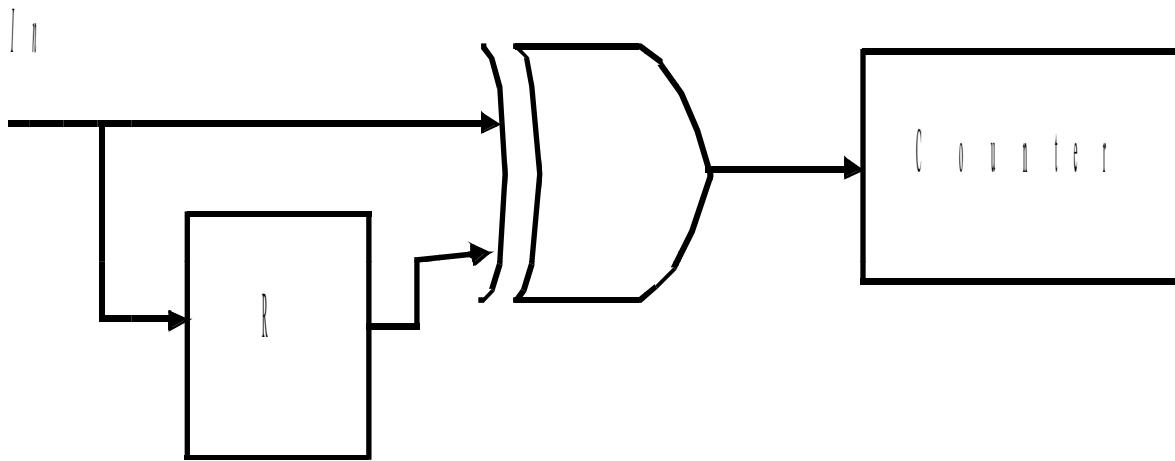
Rapidly becoming more important with increasing chip-complexity and larger modules

# Linear-Feedback Shift Register (LFSR)



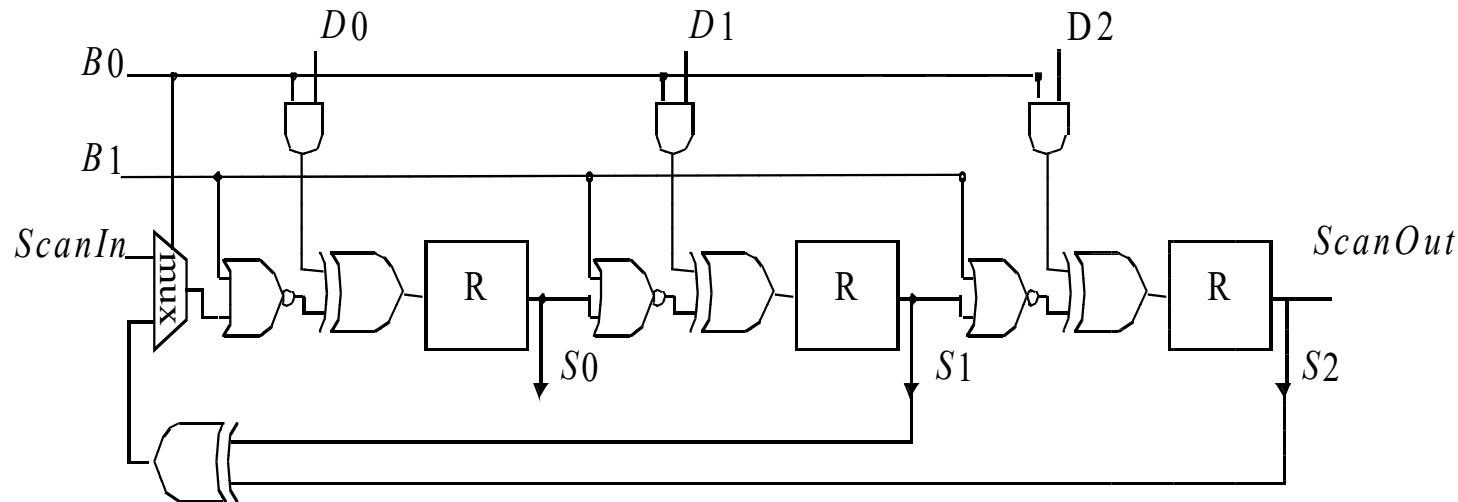
Pseudo-Random Pattern Generator

# *Signature Analysis*



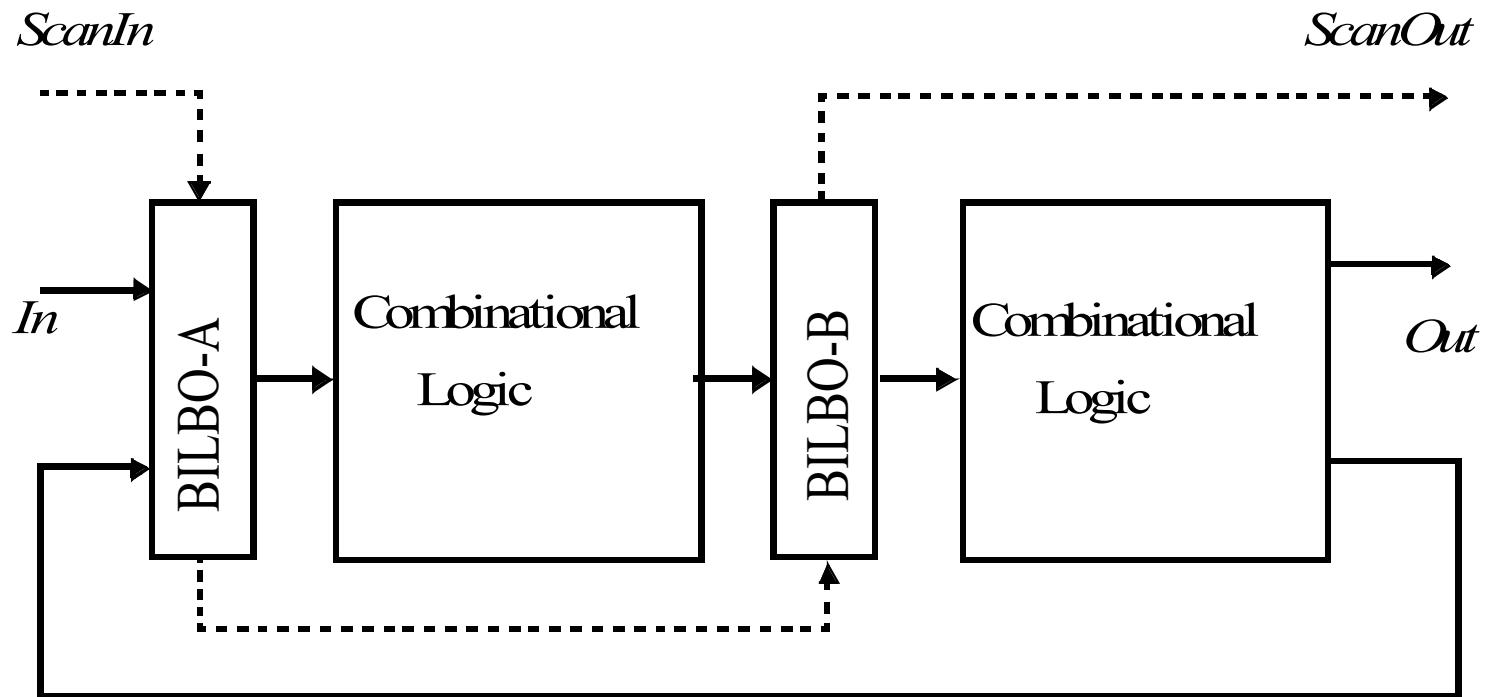
**Counts transitions on single-bit stream  
≡ Compression in time**

# BILBO

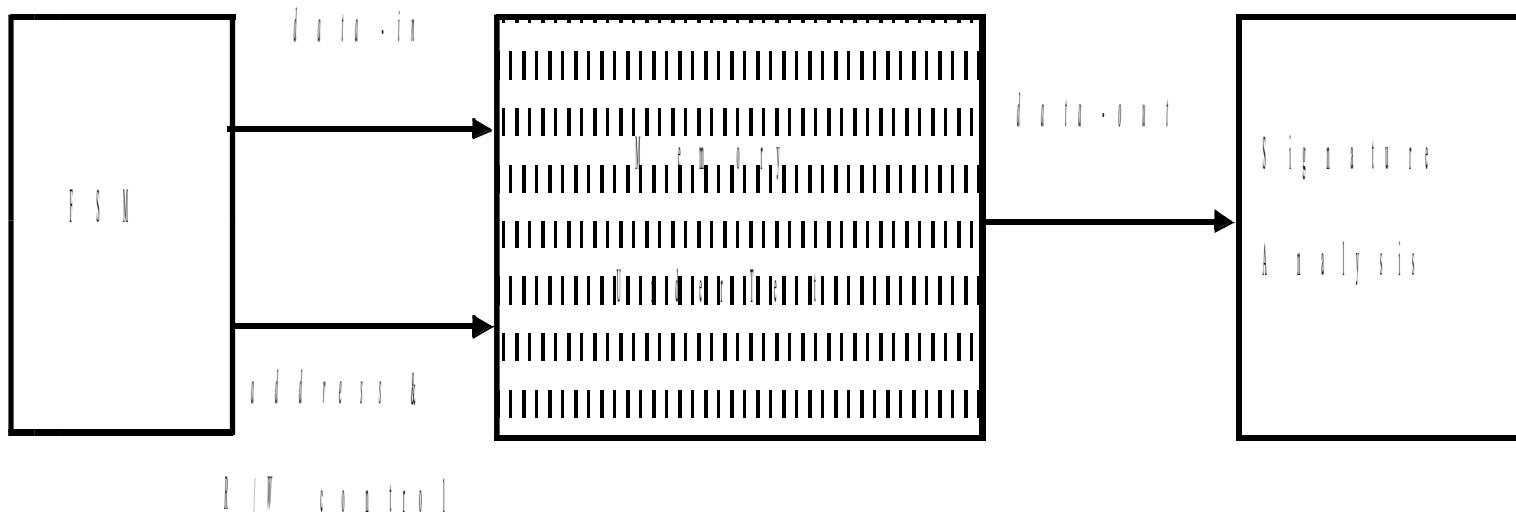


$B_0$	$B_1$	Operation mode
1	1	Normal
0	0	Scan
1	0	Pattern generation or Signature analysis
0	1	Reset

# *BILBO Application*



# Memory Self-Test



**Patterns: Writing/Reading 0s, 1s,  
Walking 0s, 1s  
Galloping 0s, 1s**