

Digital Integrated Circuits

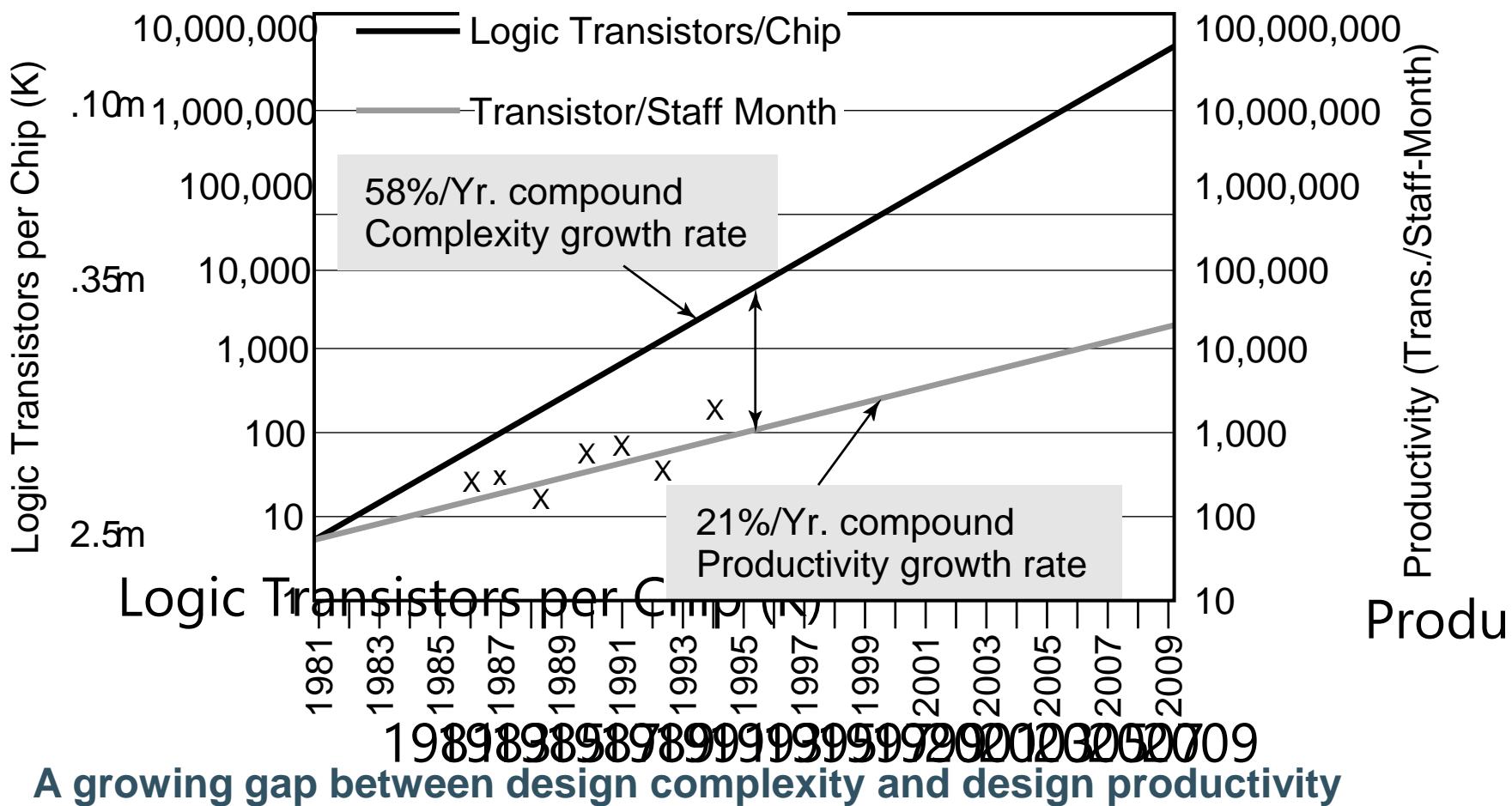
A Design Perspective

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Anantha Chandrakasan
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Design Methodologies

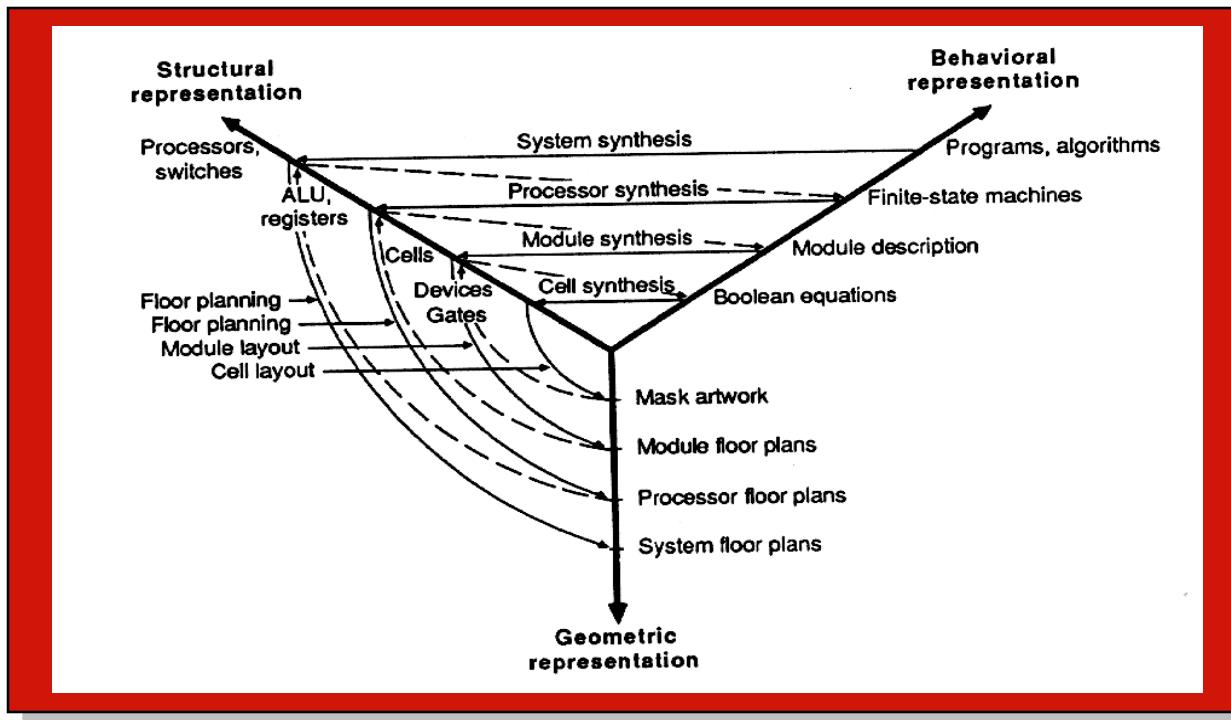
December 3, 2002

The Design Productivity Challenge



Source: sematech97

Design Methodology

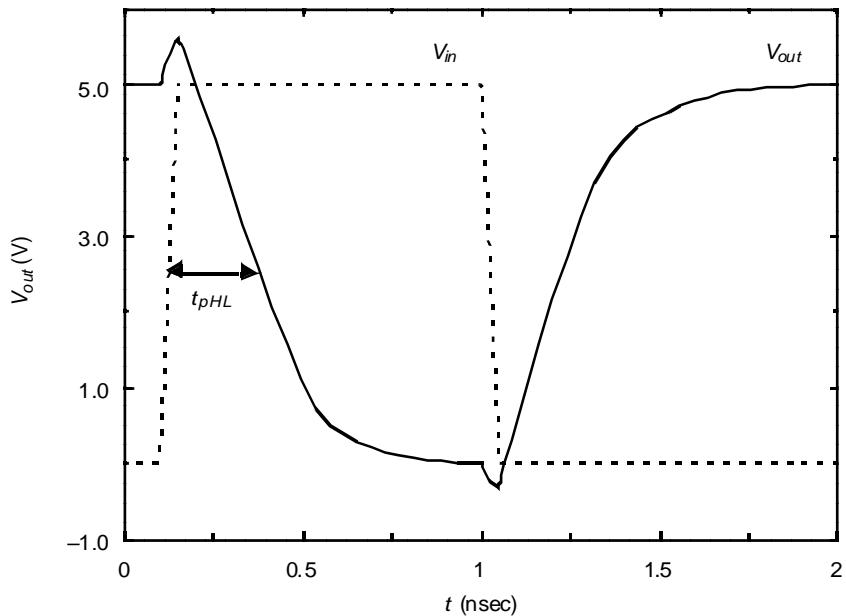
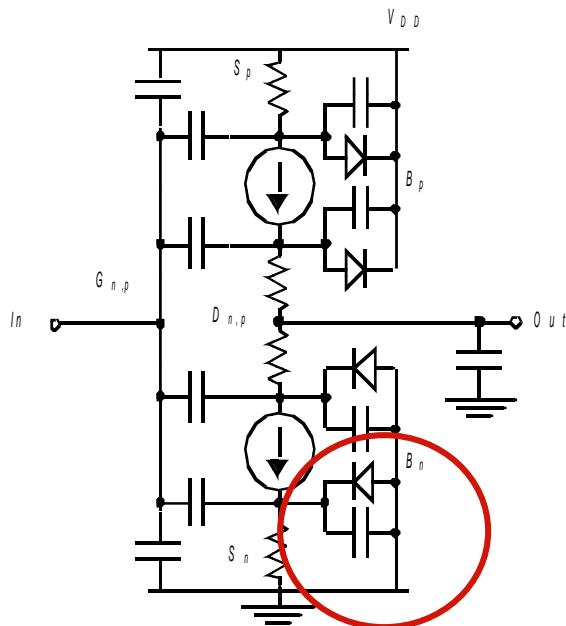


- Design process traverses iteratively between three abstractions: behavior, structure, and geometry
- More and more automation for each of these steps

Design Analysis and Verification

- Accounts for largest fraction of design time
- More efficient when done at higher levels of abstraction - selection of correct analysis level can account for multiple orders of magnitude in verification time
- Two major approaches:
 - Simulation
 - Verification

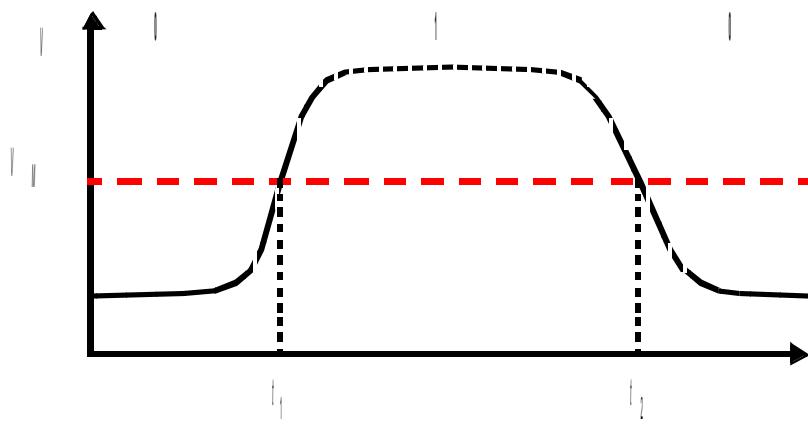
Digital Data treated as Analog Signal



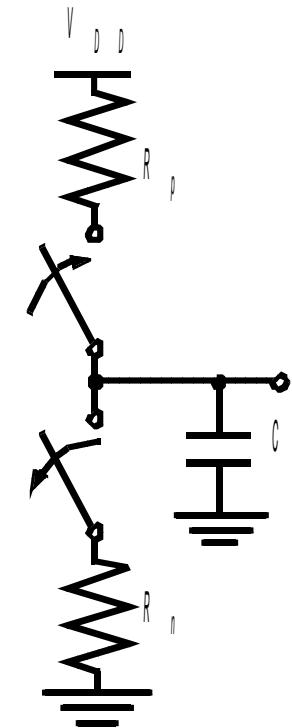
Circuit Simulation

Both Time and Data treated as Analog Quantities
Also complicated by presence of non-linear elements
(relaxed in timing simulation)

Representing Data as Discrete Entity



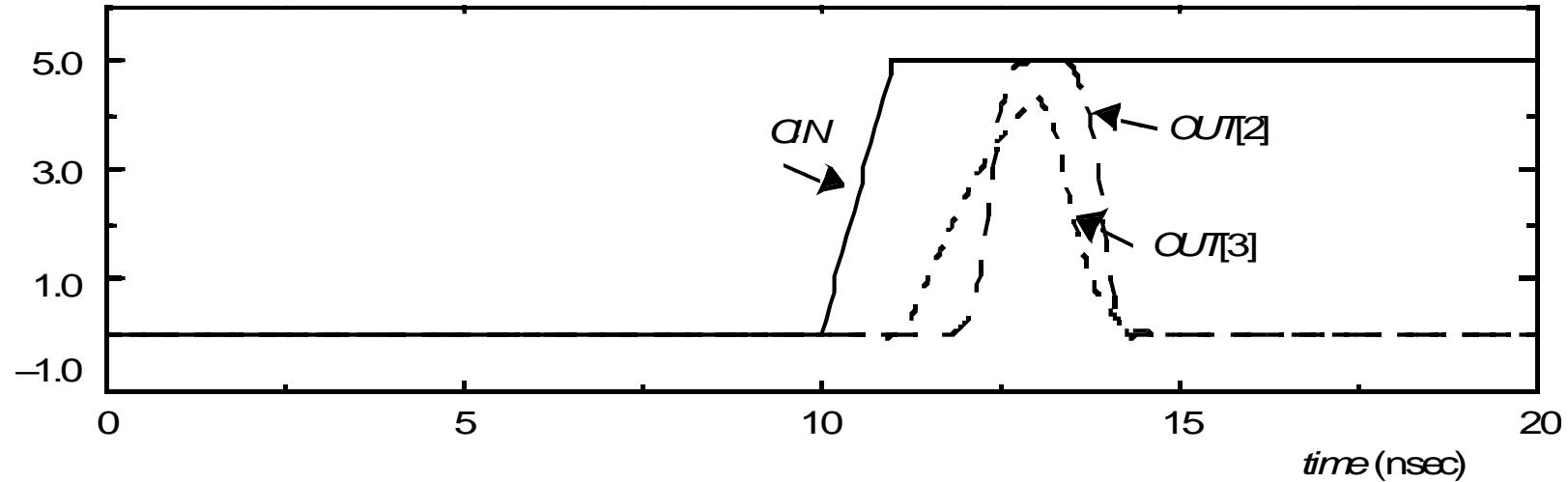
Discretizing the data using
switching threshold



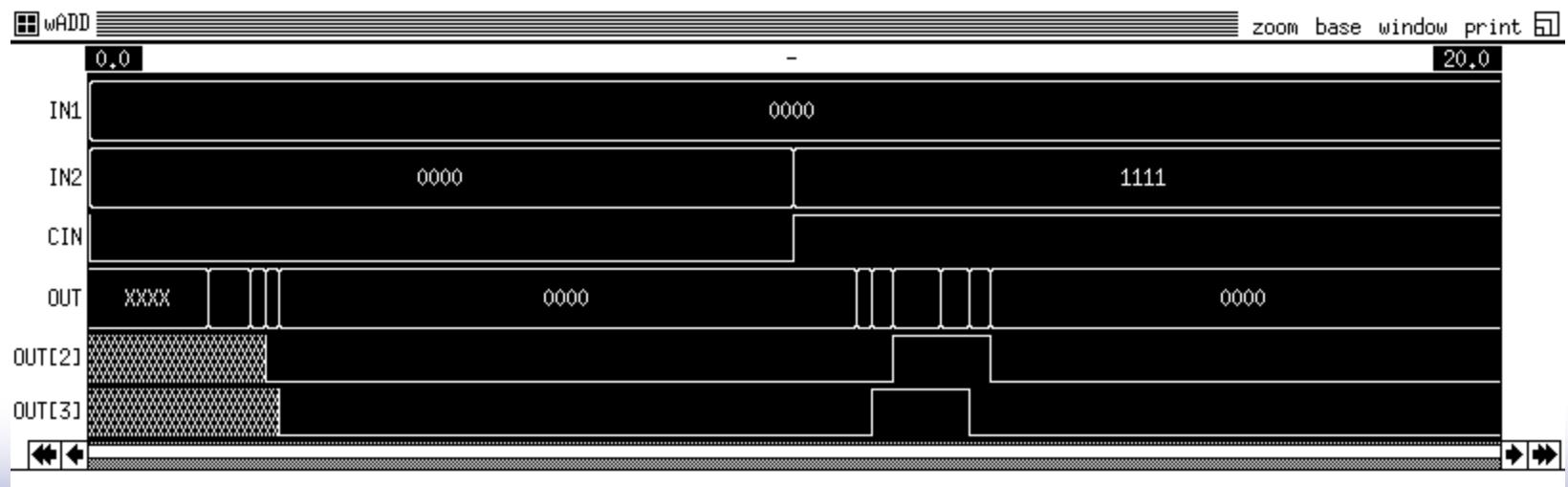
The linear switch model
of the inverter

Circuit versus Switch-Level Simulation

Circuit



Switch



Structural Description of Accumulator

```
entity accumulator is
    port( --definition of input and output terminals
        DI: in bit_vector(15 downto 0) -- a vector of 16 bit wide
        DO: inout bit_vector(15 downto 0);
        CLK: in bit
    );
end accumulator;

architecture structure of accumulator is
    component reg -- definition of register ports
        port(
            DI : in bit_vector(15 downto 0);
            DO : out bit_vector(15 downto 0);
            CLK : in bit
        );
    end component;
    component add -- definition of adder ports
        port(
            IN0 : in bit_vector(15 downto 0);
            IN1 : in bit_vector(15 downto 0);
            OUT0 : out bit_vector(15 downto 0)
        );
    end component;
    -- definition of accumulator structure
    signal X : bit_vector(15 downto 0);
begin
    add1 : add
        port map (DI, DO, X); -- defines port connectivity
    reg1 : reg
        port map (X, DO, CLK);
end structure;
```

Design defined as composition of register and full-adder cells (“netlist”)

Data represented as {0,1,Z}

Time discretized and progresses with unit steps

Description language: VHDL
Other options: schematics, Verilog

Behavioral Description of Accumulator

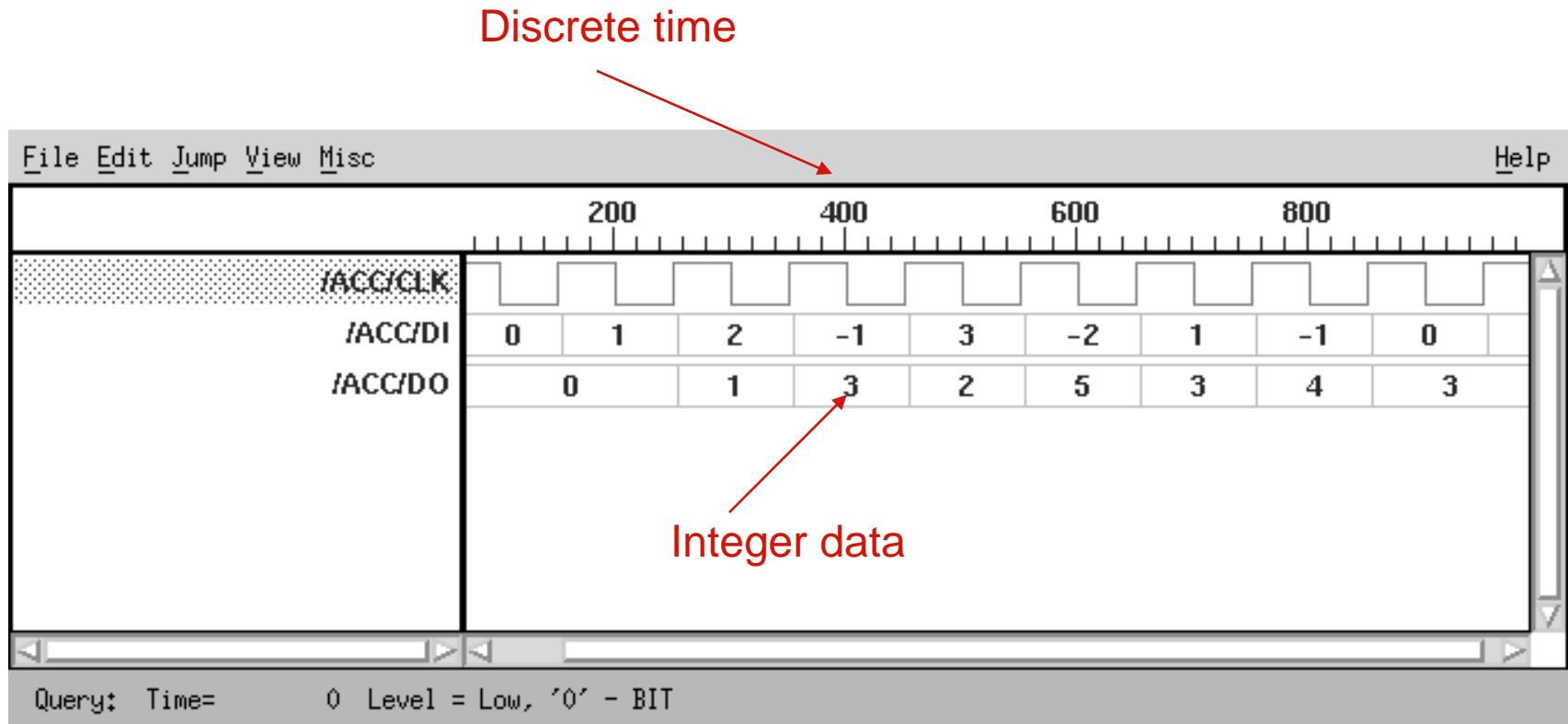
```
entity accumulator is
  port(
    DI : in integer;
    DO : inout integer := 0;
    CLK : in bit
  );
end accumulator;

architecture behavior of accumulator is
begin
  process(CLK)
    variable X : integer := 0; -- intermediate variable
  begin
    if CLK = '1' then
      X <= DO + D1;
      DO <= X;
    end if;
  end process;
end behavior;
```

Design described as set of input-output relations, regardless of chosen implementation

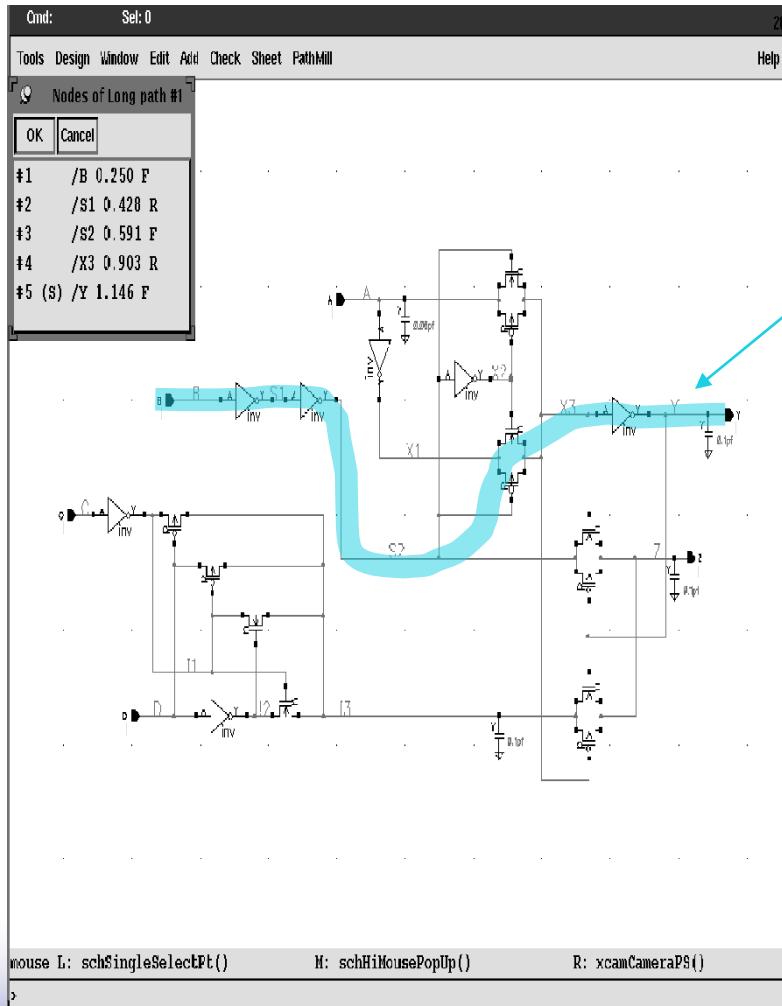
Data described at higher abstraction level (“integer”)

Behavioral simulation of accumulator



(Synopsys Waves display tool)

Timing Verification



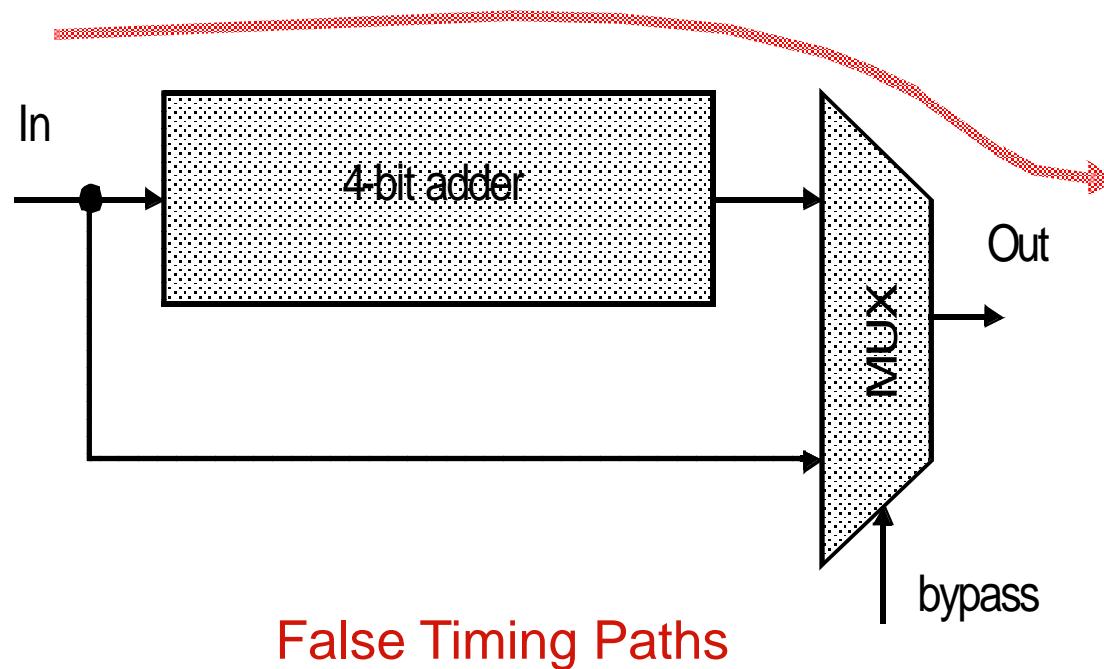
Critical path

Enumerates and rank
orders critical timing paths

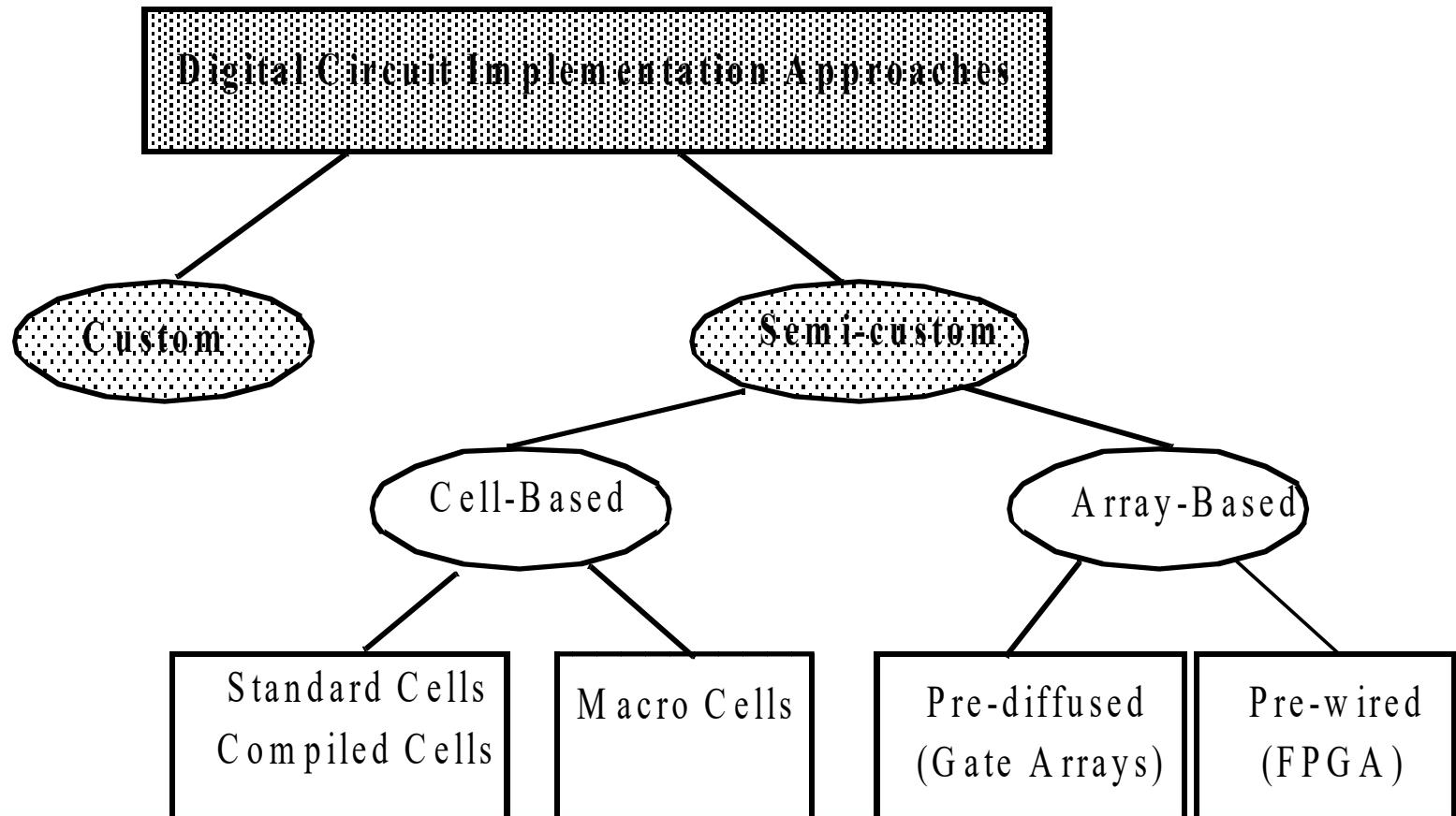
No simulation needed!

(Synopsys-Epic Pathmill)

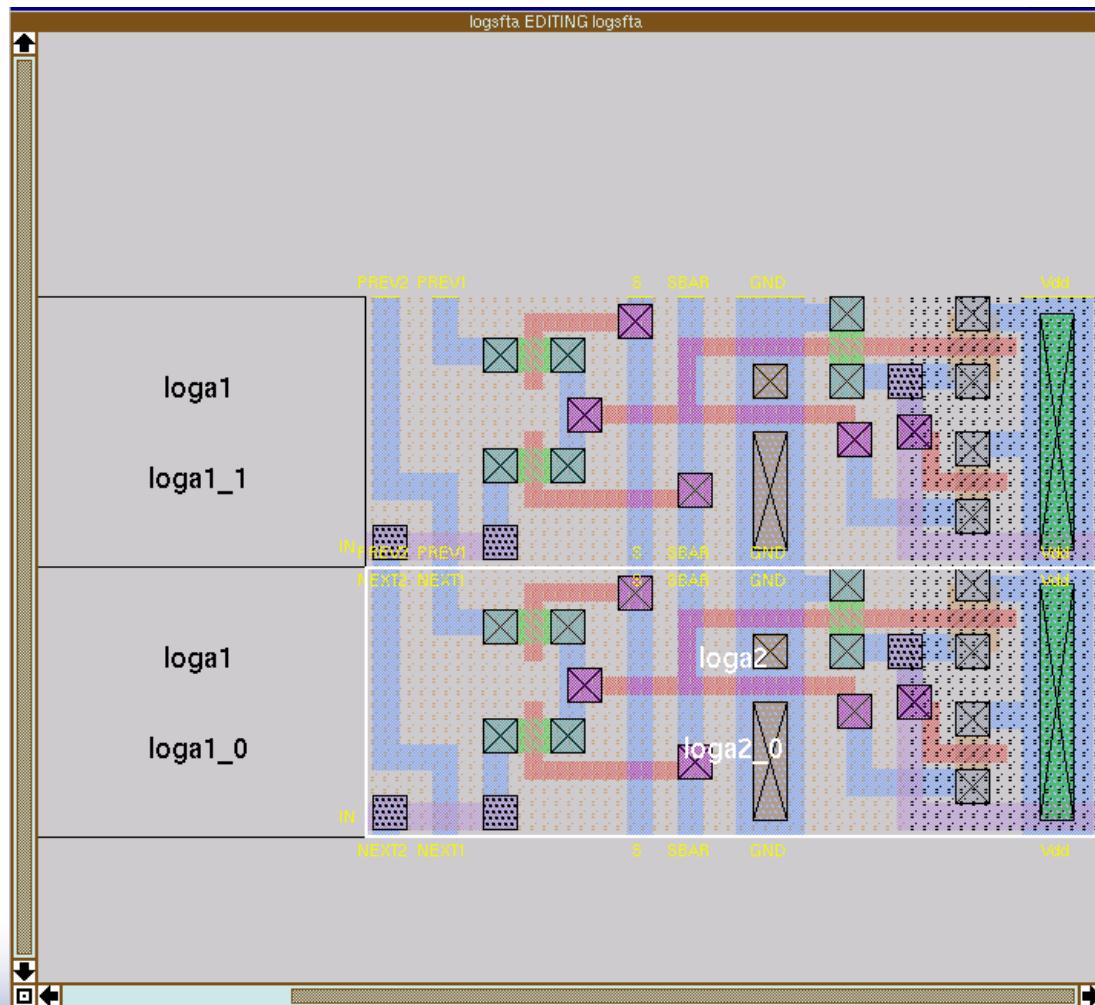
Issues in Timing Verification



Implementation Methodologies

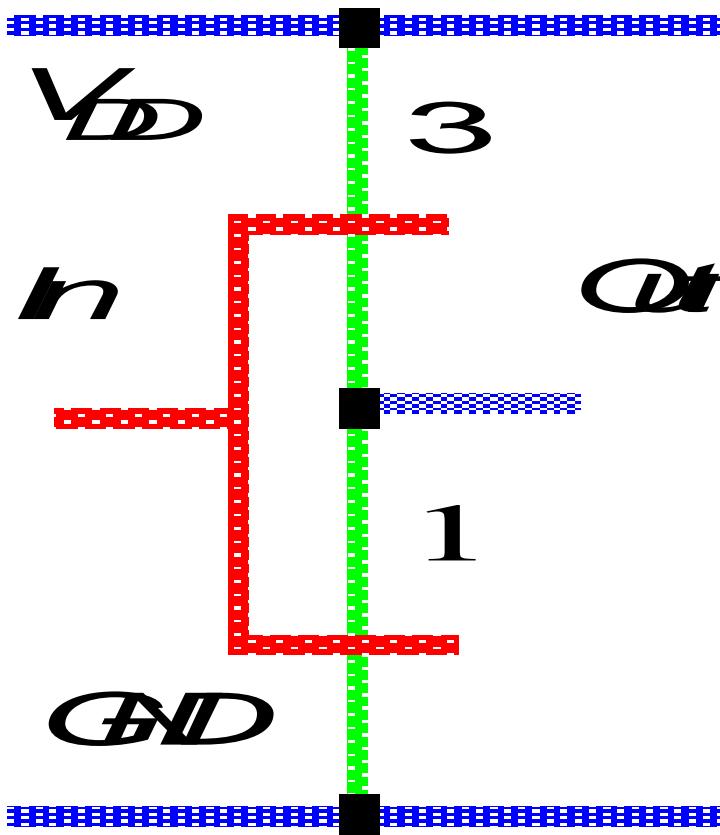


Custom Design – Layout Editor



Magic Layout Editor
(UC Berkeley)

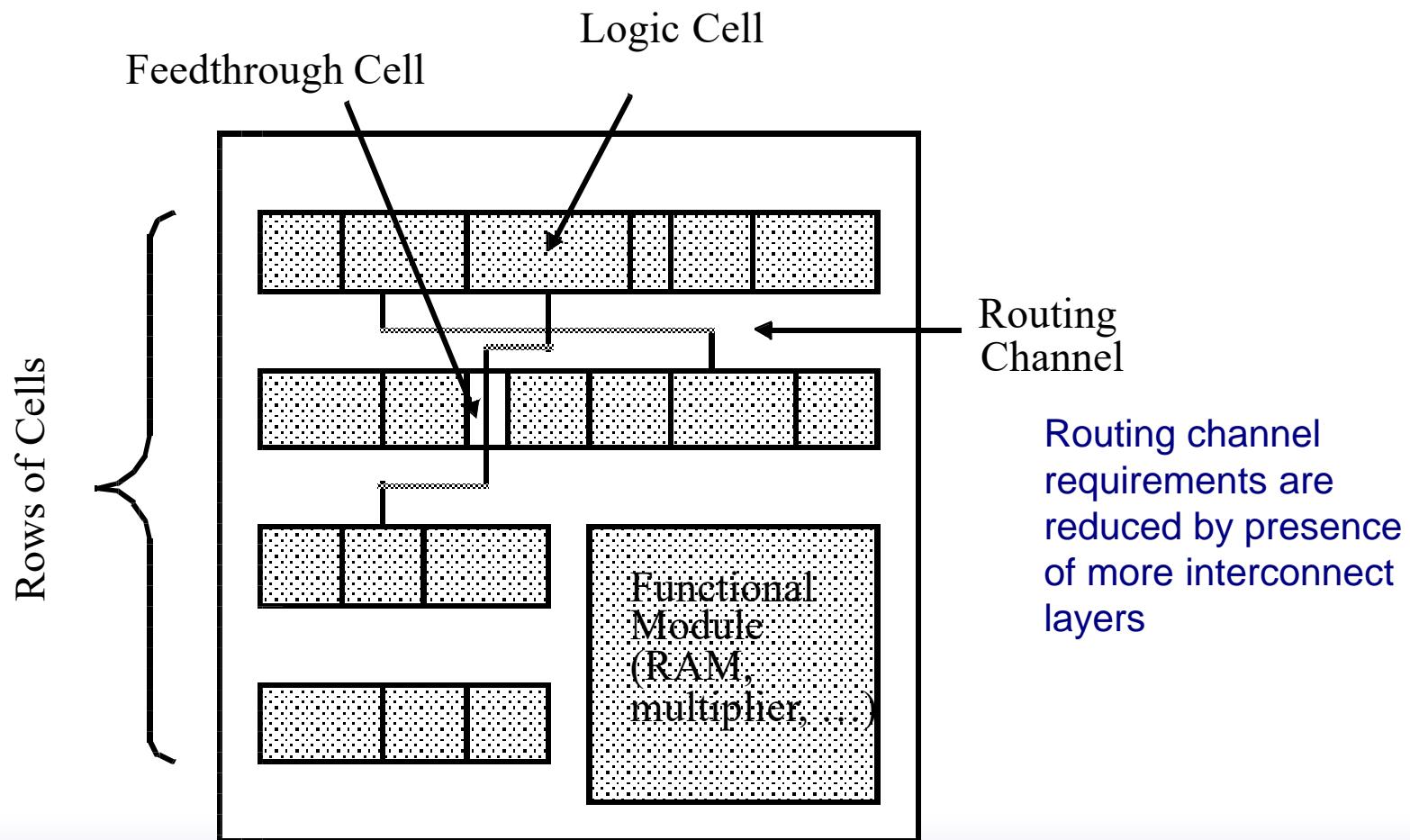
Symbolic Layout



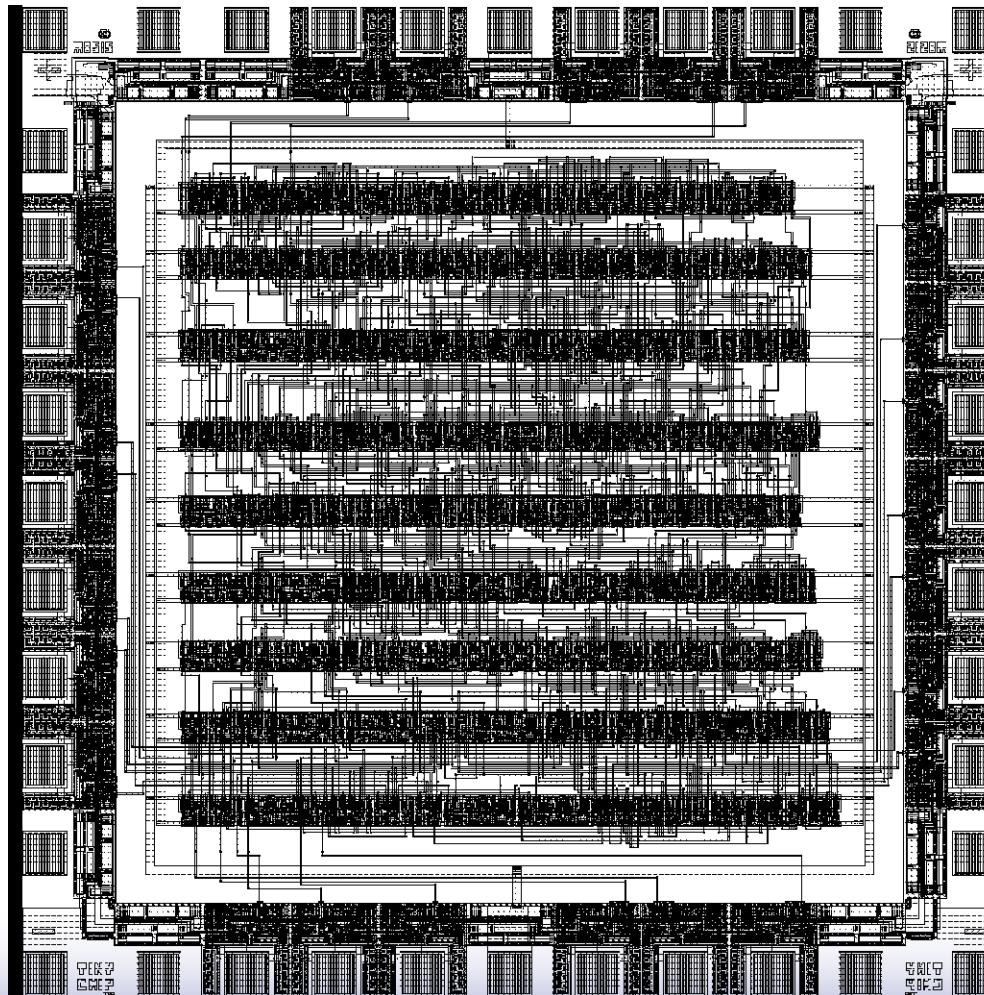
Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by “compaction” program

Cell-based Design (or standard cells)

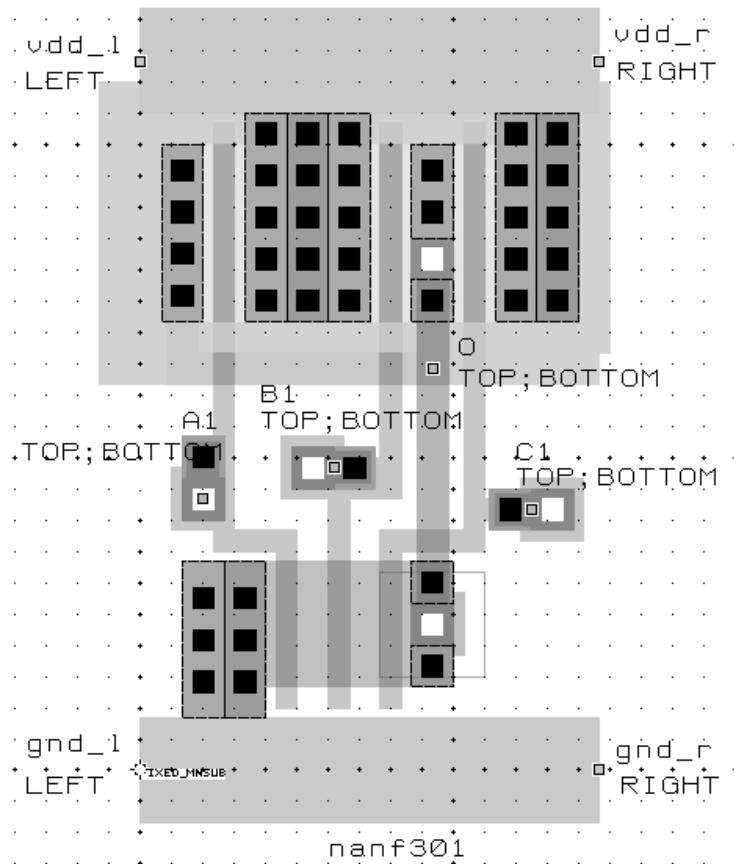


Standard Cell — Example



[Brodersen92]

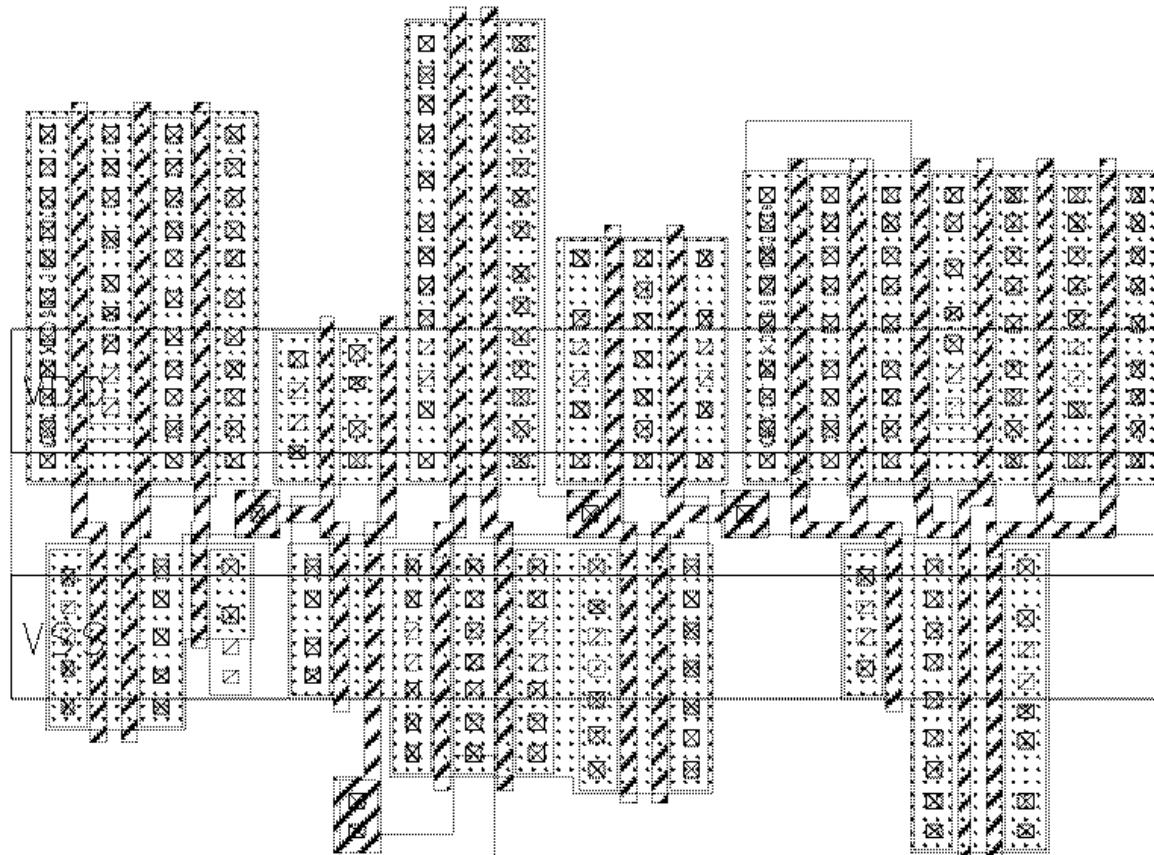
Standard Cell - Example



Fanout 4x	0.5 μm	1.0 μm	2.0 μm
A1_tphl	0.595	0.711	0.919
A1_tplh	0.692	0.933	1.360
B1_tphl	0.591	0.739	1.006
B1_tplh	0.620	0.825	1.1.81
C1_tphl	0.574	0.740	1.029
C1_tplh	0.554	0.728	1.026

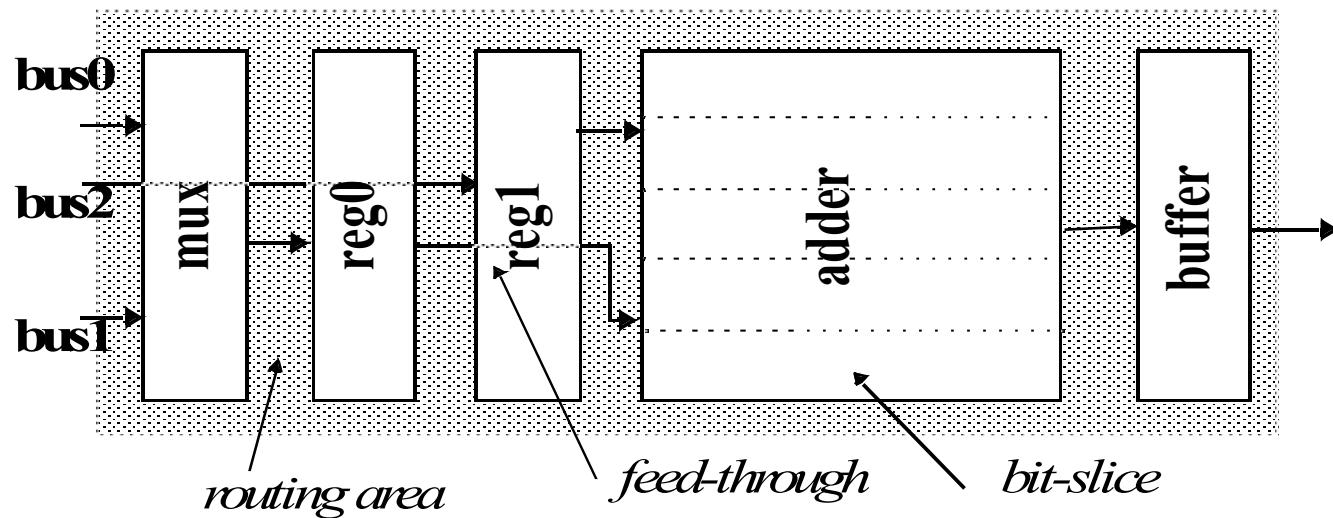
3-input NAND cell
(from Mississippi State Library)
characterized for fanout of 4 and
for three different technologies

Automatic Cell Generation



Random-logic layout
generated by CLEO
cell compiler (Digital)

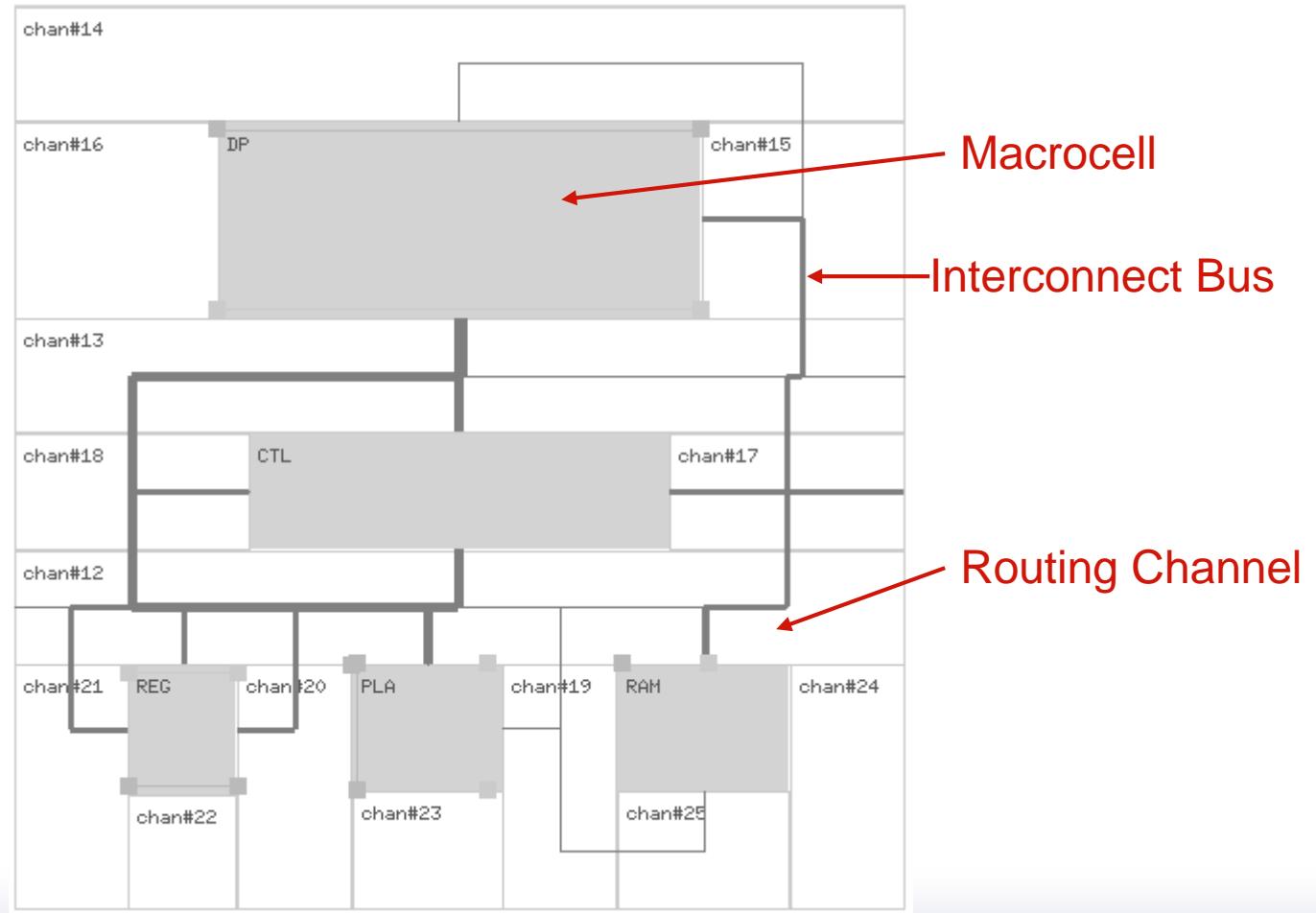
Module Generators – Compiled Datapath



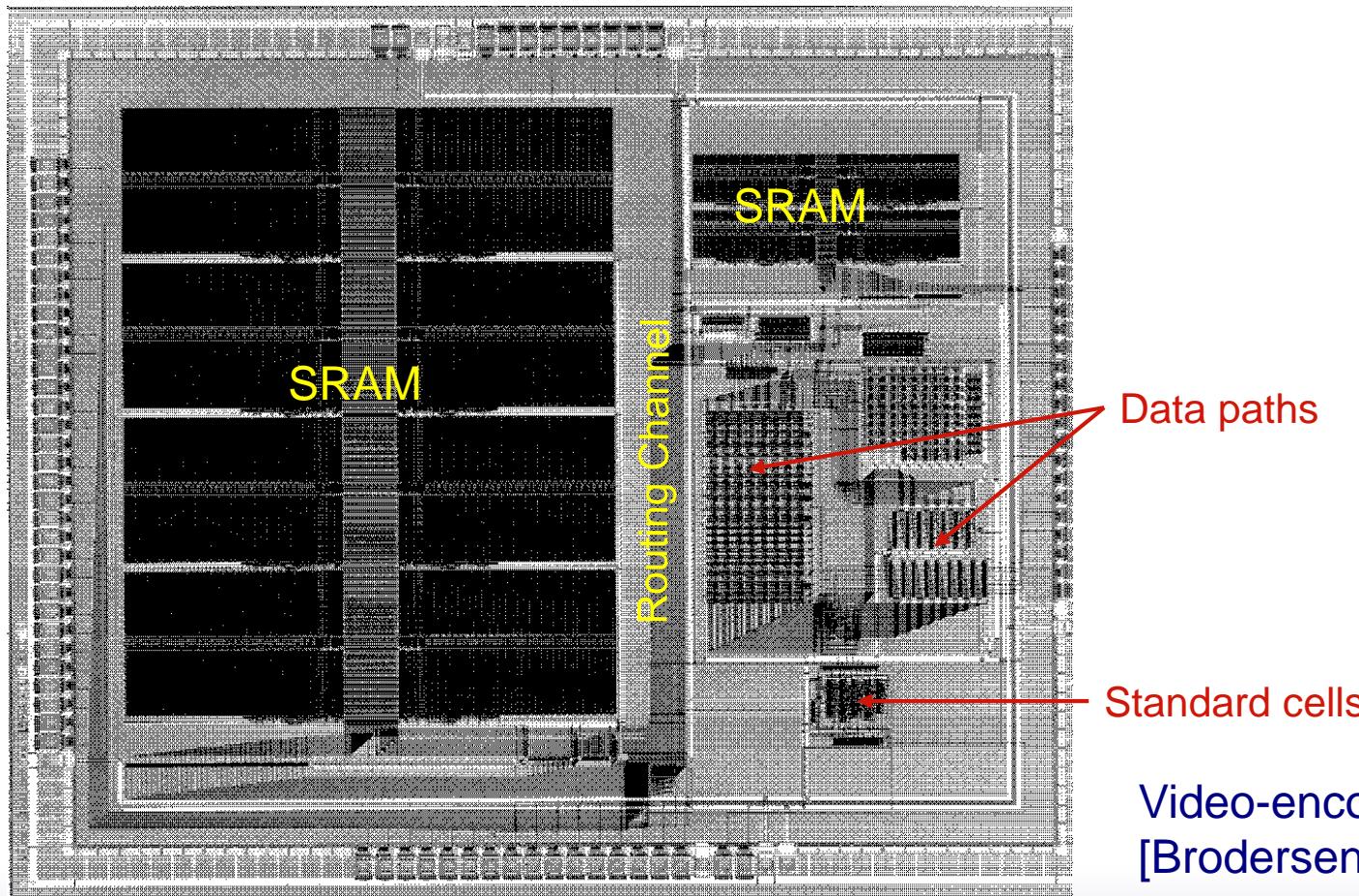
Advantages: One-dimensional placement/routing problem

Macrocell Design Methodology

Floorplan:
Defines overall topology of design, relative placement of modules, and global routes of busses, supplies, and clocks

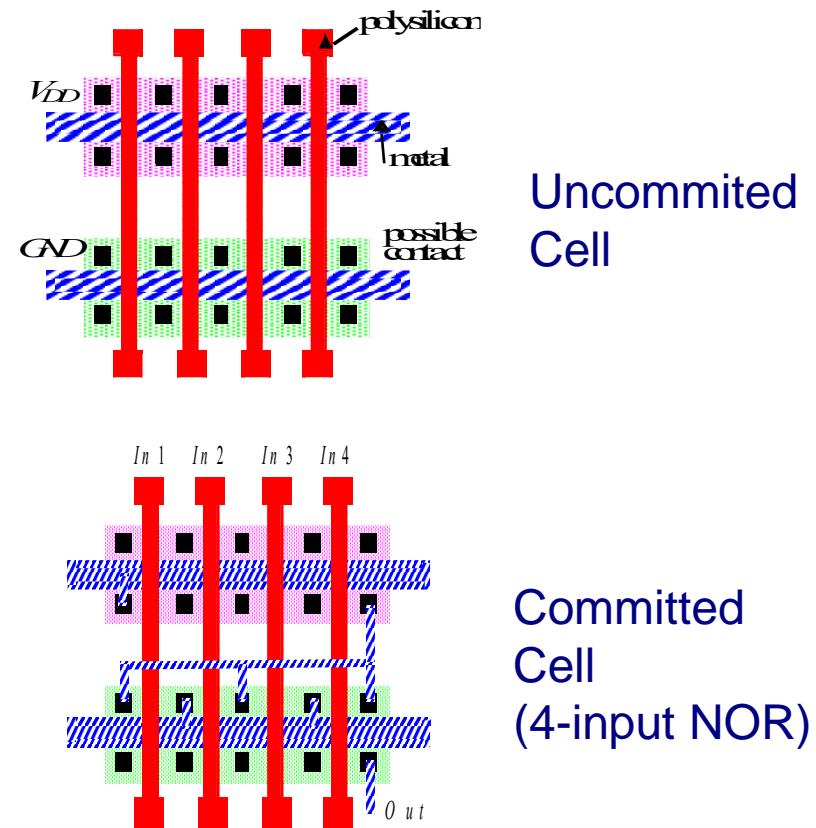
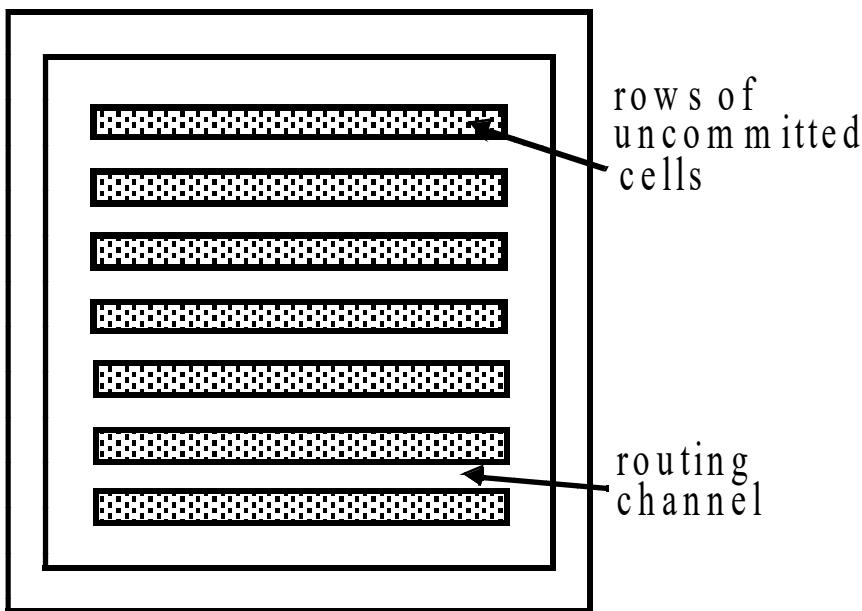


Macrocell-Based Design Example

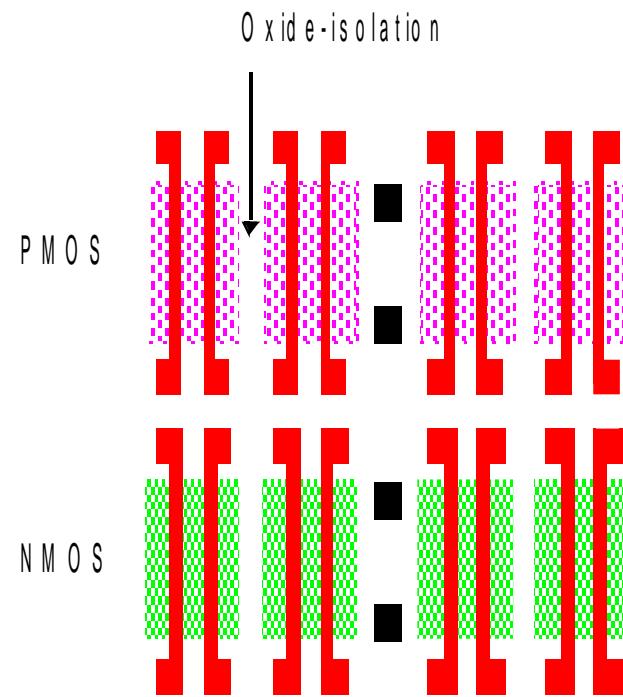


Video-encoder chip
[Brodersen92]

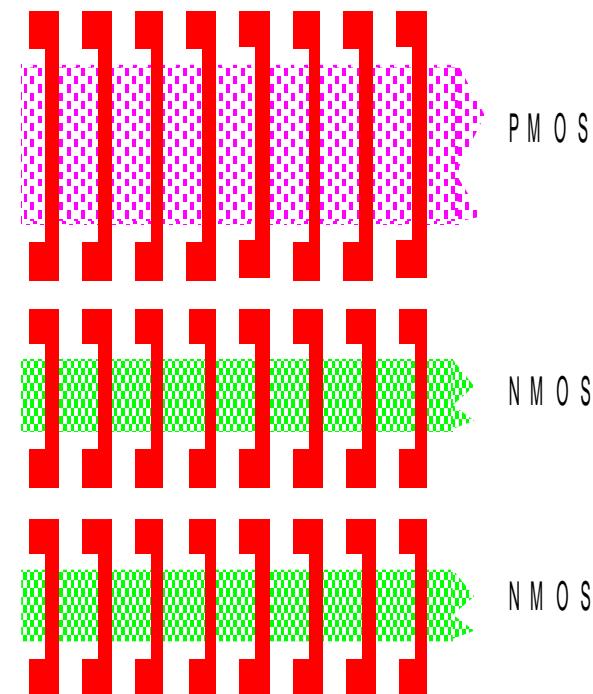
Gate Array — Sea-of-gates



Sea-of-gate Primitive Cells

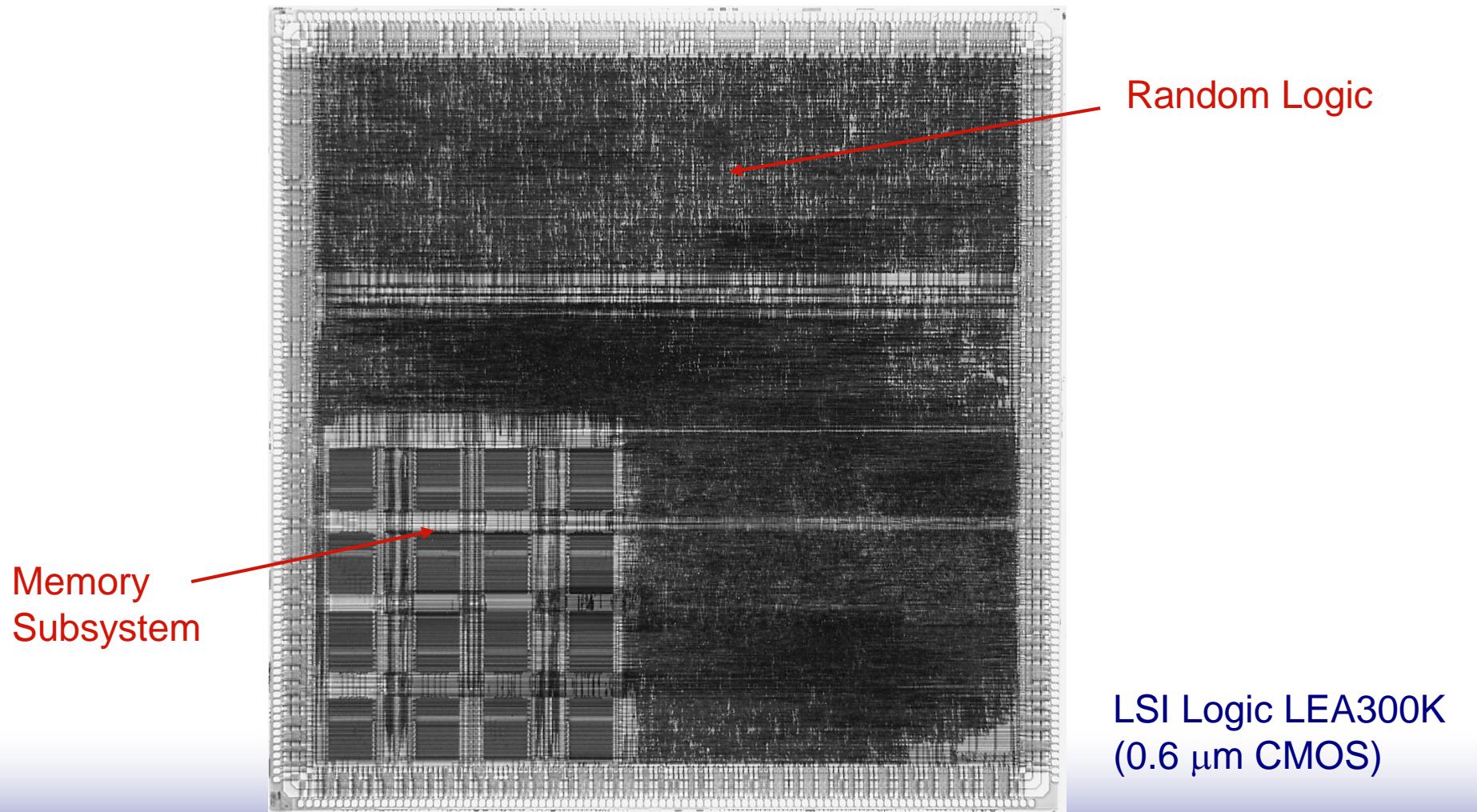


Using oxide-isolation



Using gate-isolation

Sea-of-gates

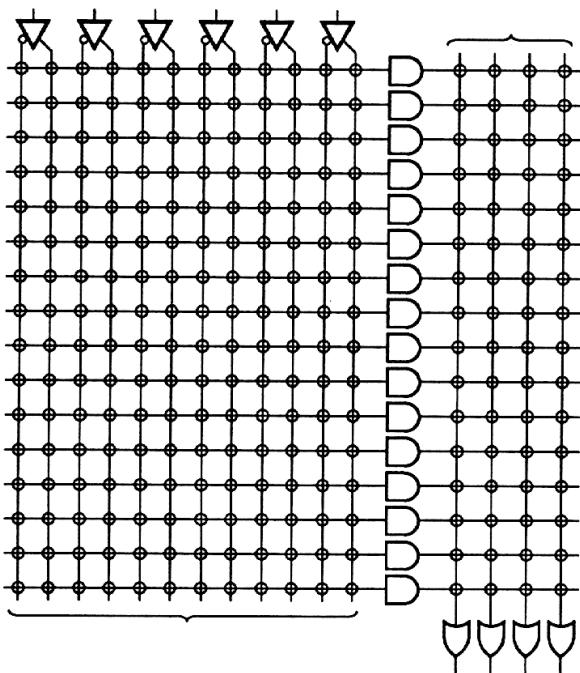


Prewired Arrays

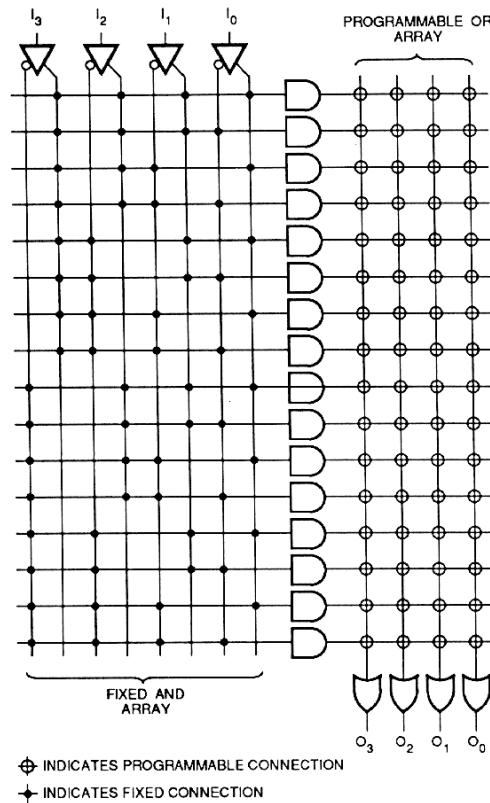
Categories of prewired arrays (or field-programmable devices):

- Fuse-based (program-once)
- Non-volatile EEPROM based
- RAM based

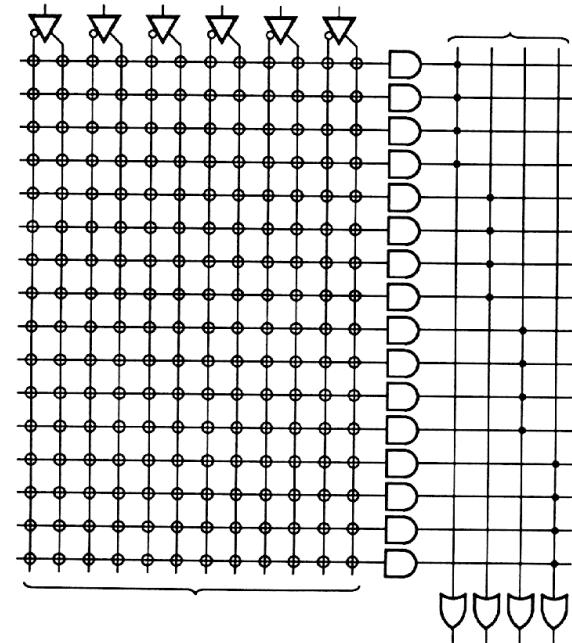
Programmable Logic Devices



PLA

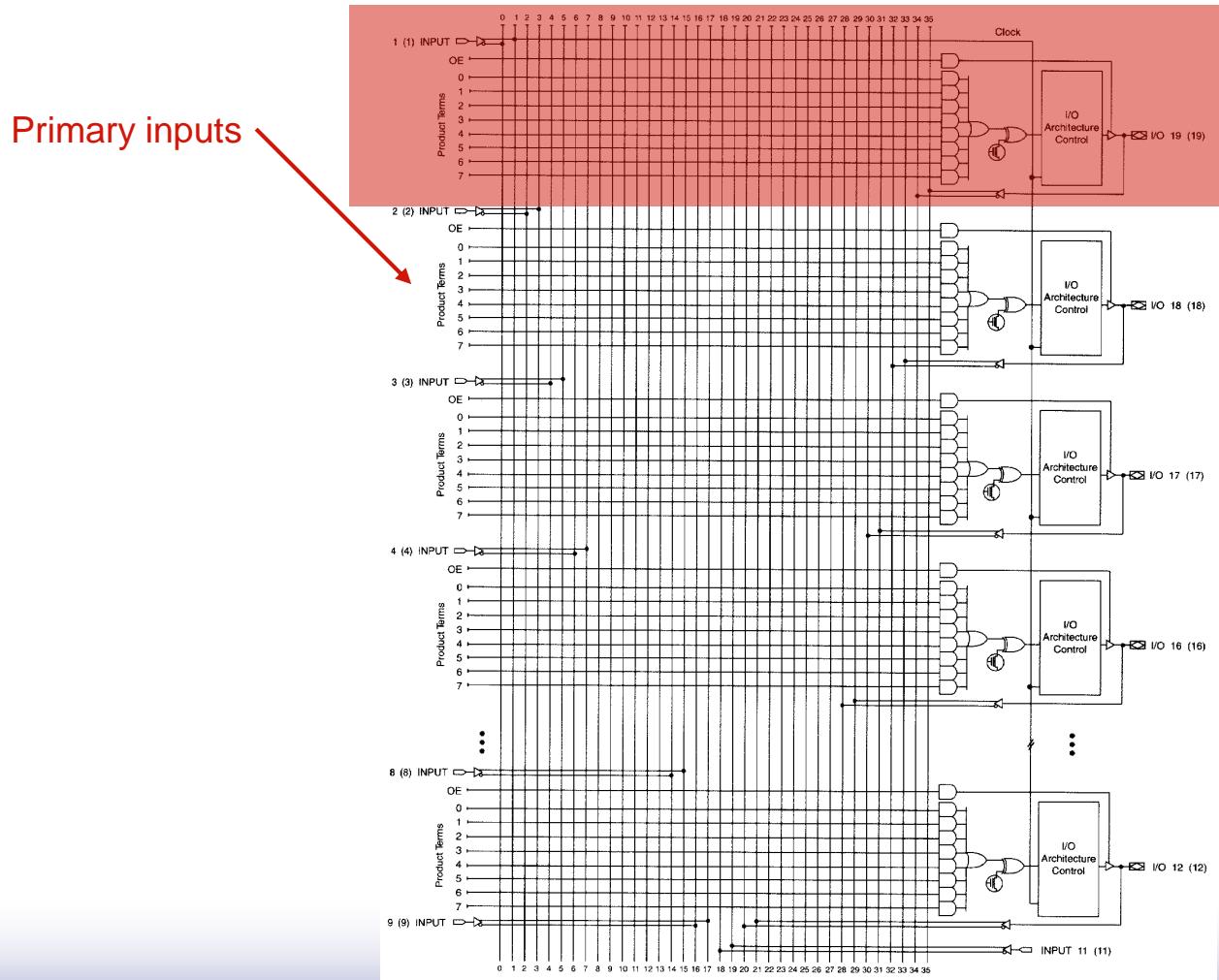


PROM



PAL

EPLD Block Diagram



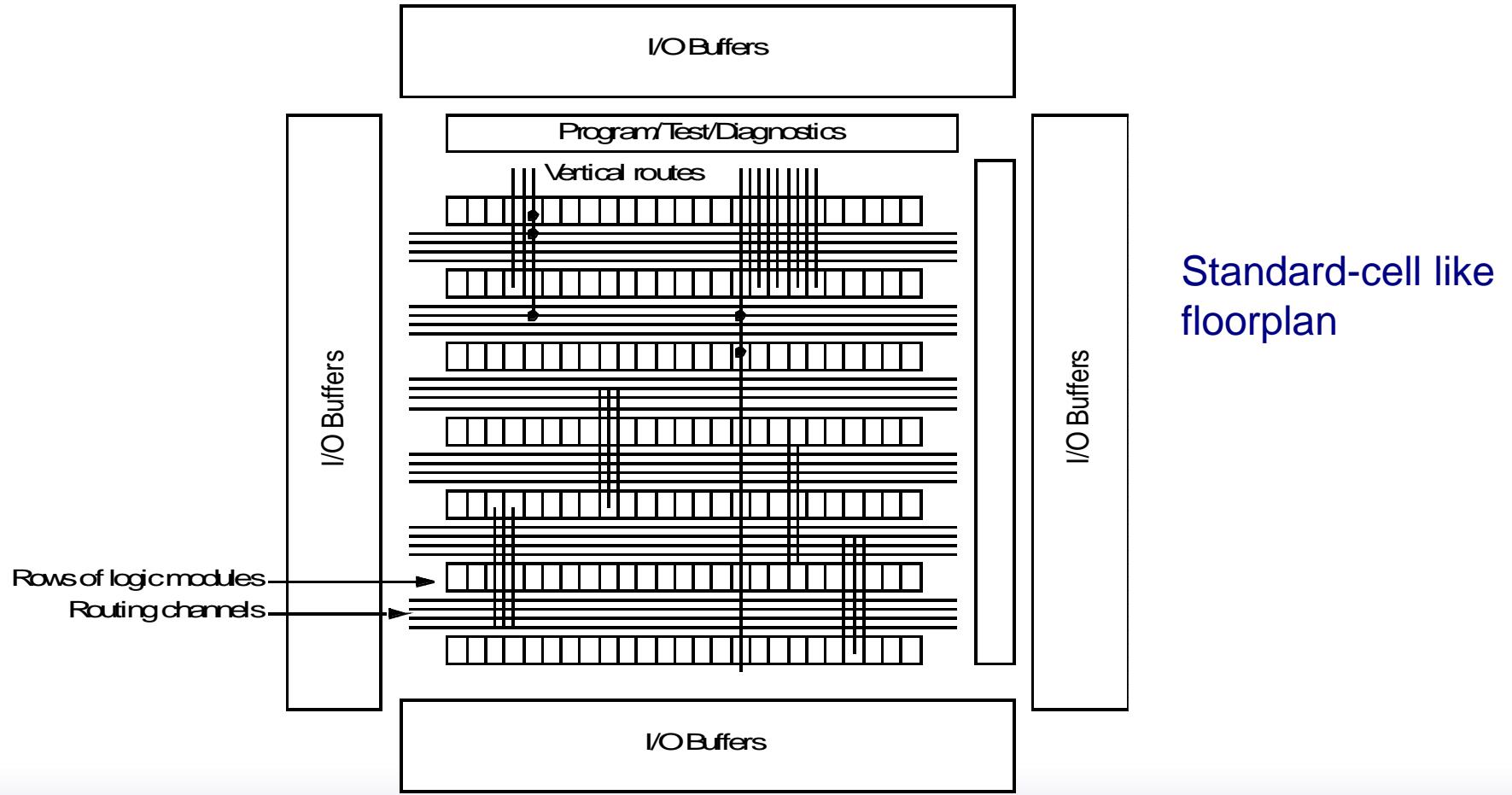
Macrocell

Courtesy Altera Corp.

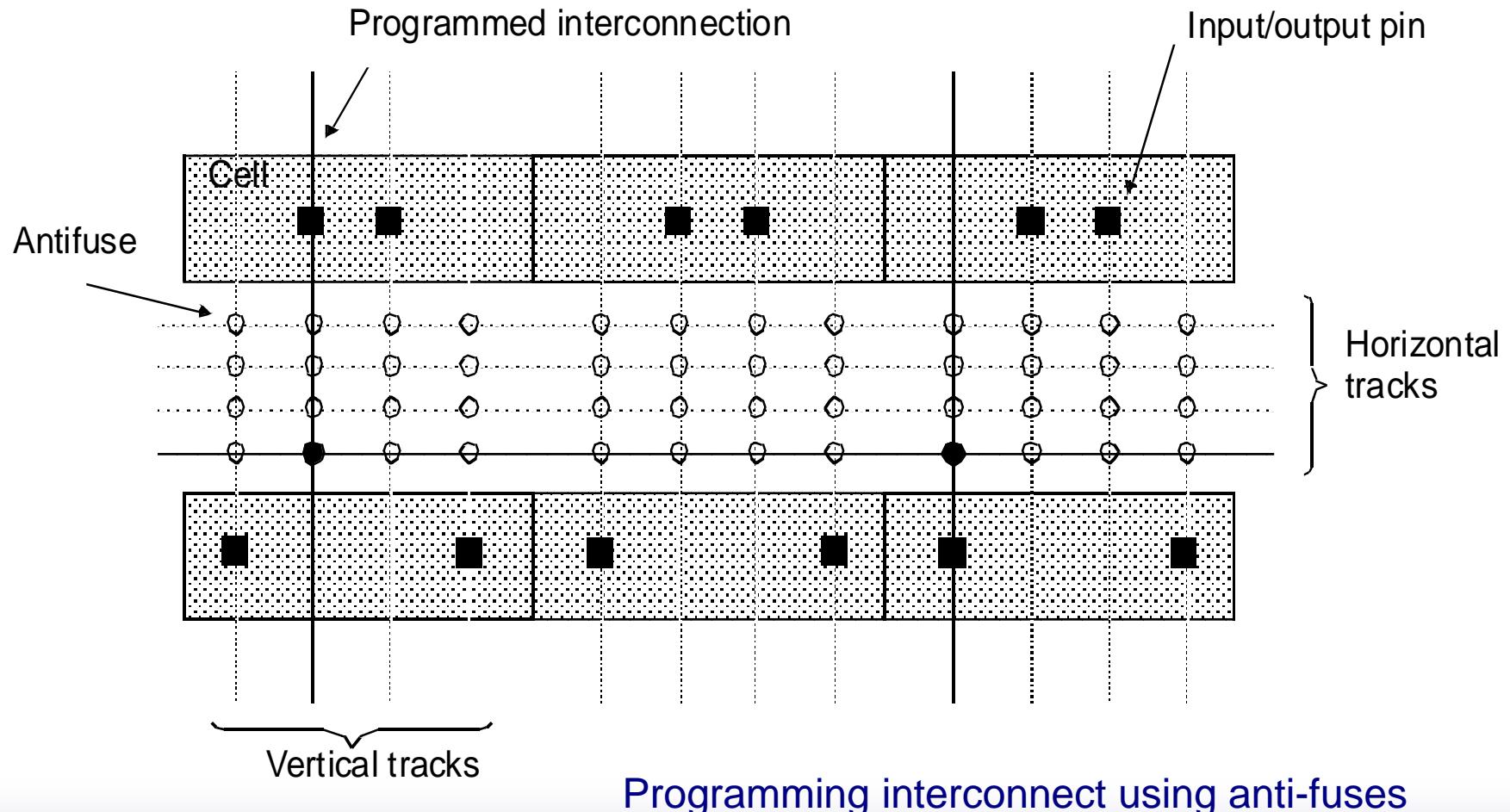
Design Methodologies

Field-Programmable Gate Arrays

Fuse-based

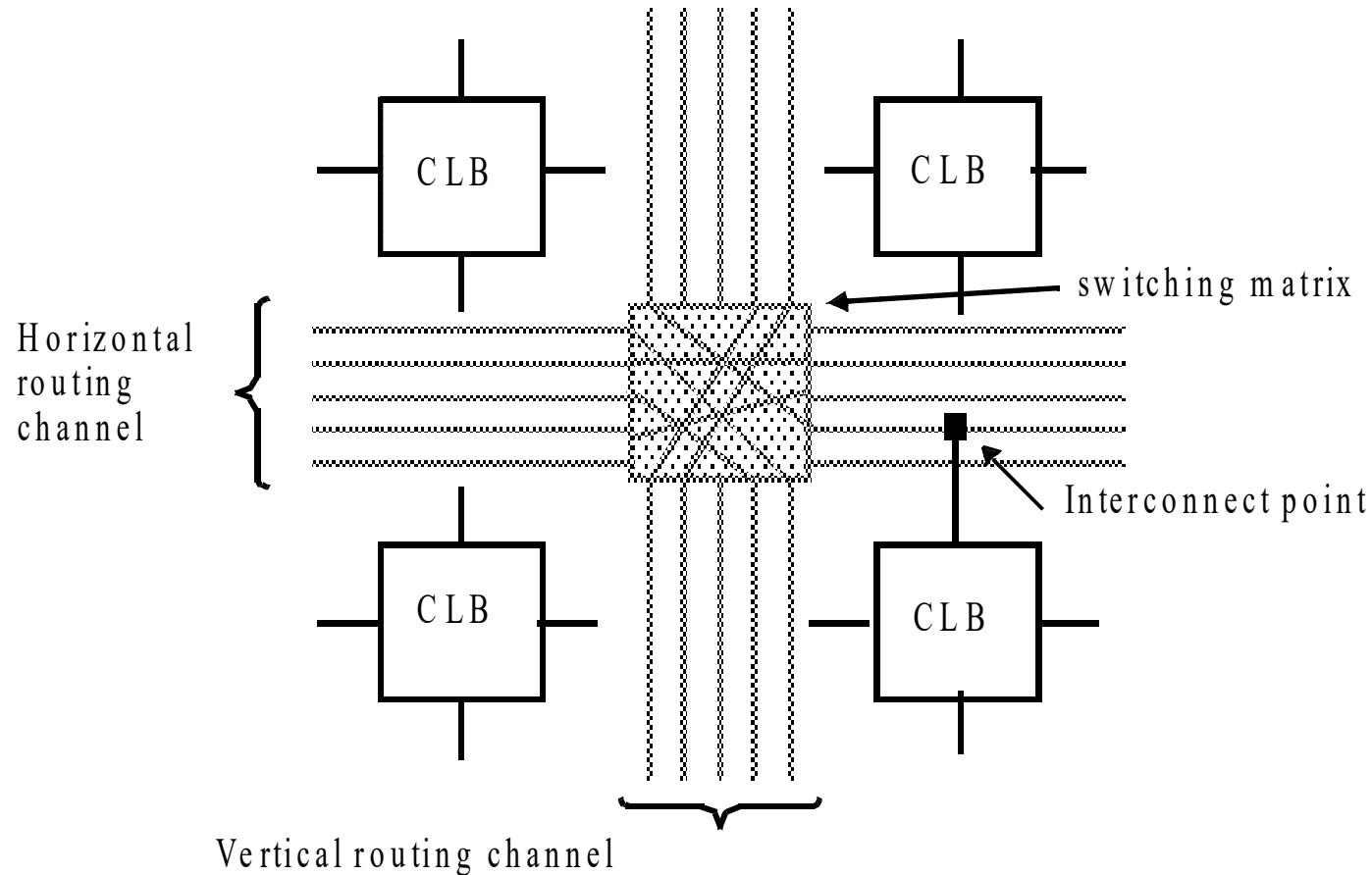


Interconnect

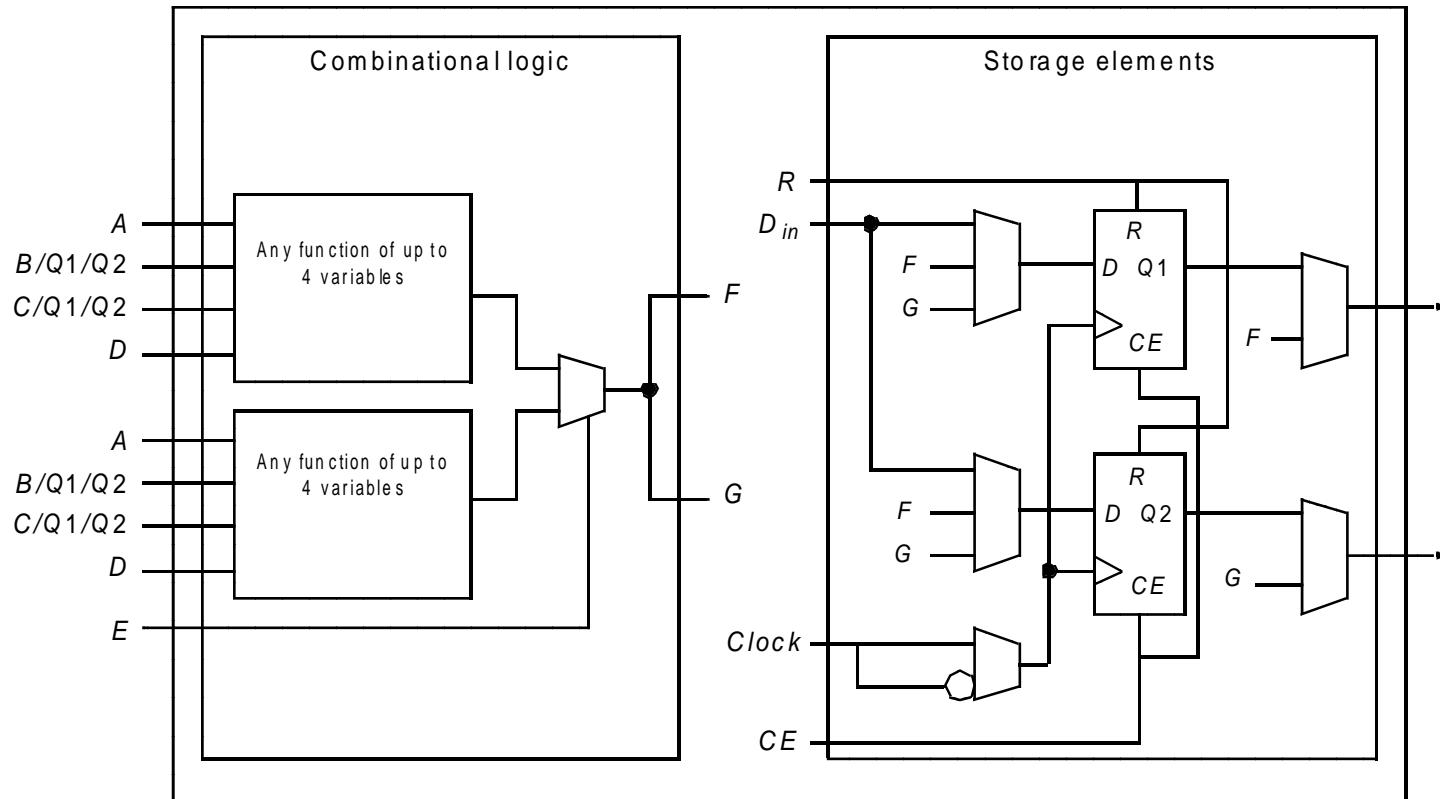


Field-Programmable Gate Arrays

RAM-based



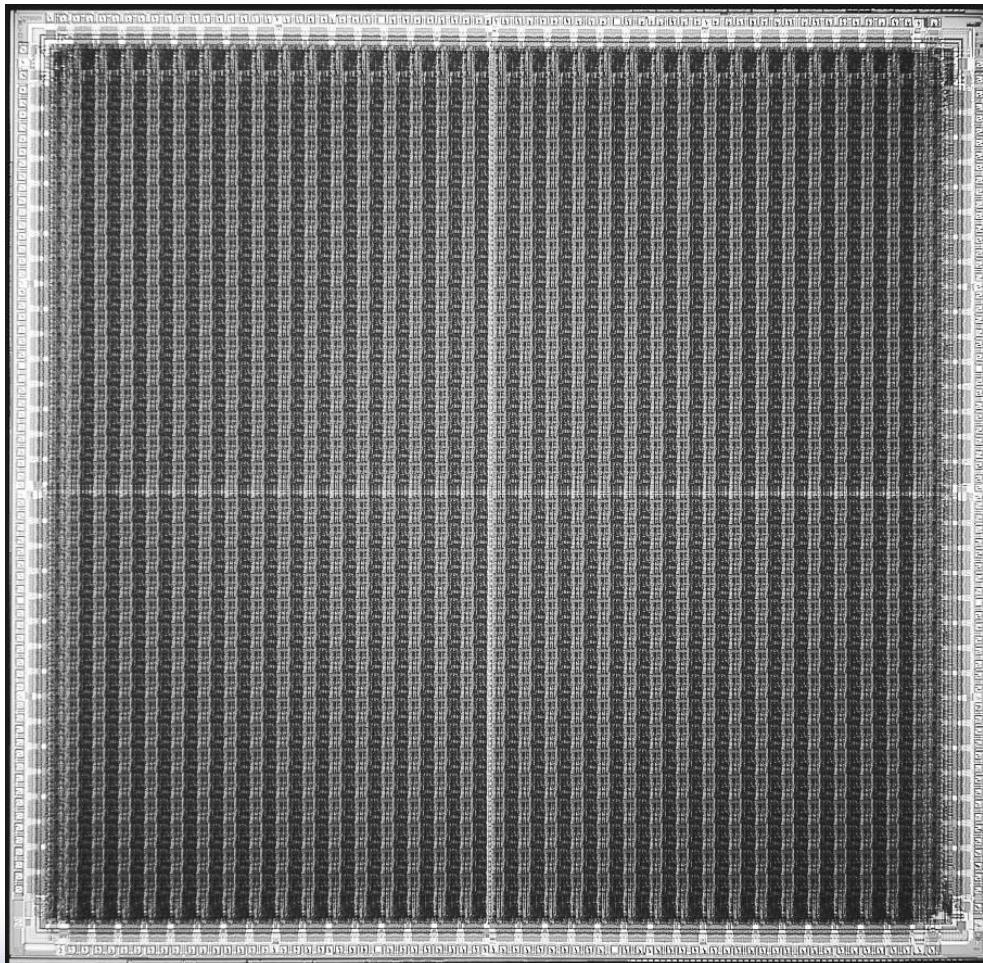
RAM-based FPGA Basic Cell (CLB)



Courtesy of Xilinx

Design Methodologies

RAM-based FPGA



Xilinx XC4025

Taxonomy of Synthesis Tasks

