# Digital Integrated Circuits
## A Design Perspective

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Anantha Chandrakasan
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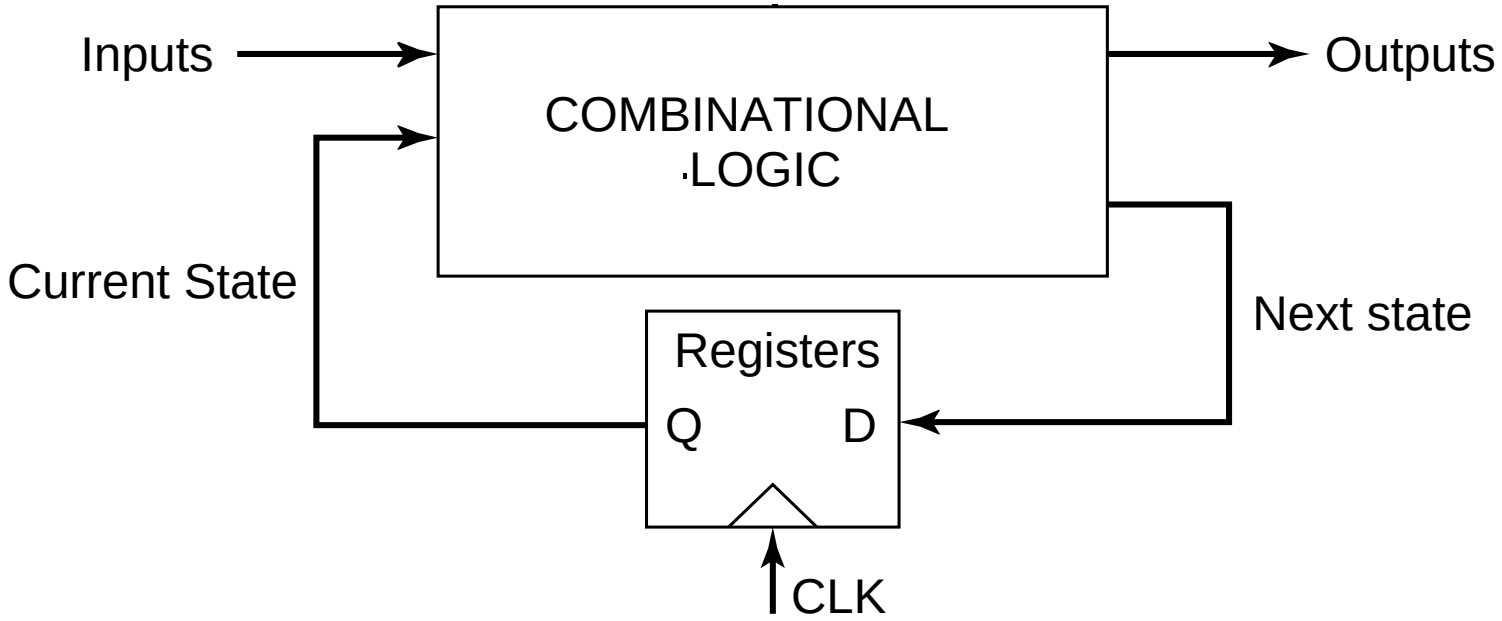
# Designing Sequential Logic Circuits

*November 2002*

# Sequential Logic




**2 storage mechanisms**

- **positive feedback**
- **charge-based**

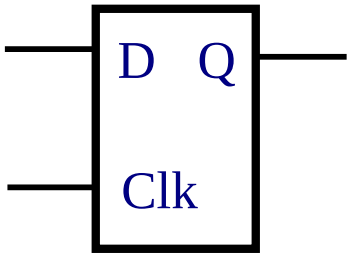
# Naming Conventions

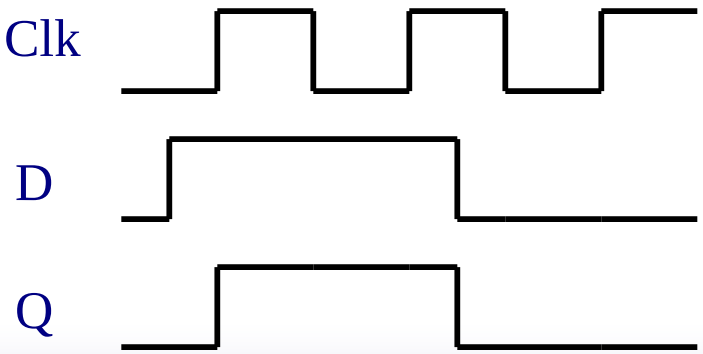
- In our text:
  - a latch is level sensitive
  - a register is edge-triggered
- There are many different naming conventions
  - For instance, many books call edge-triggered elements flip-flops
  - This leads to confusion however

# Latch versus Register

- Latch

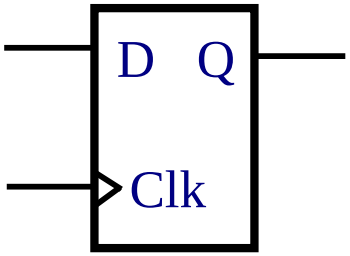
  stores data when clock is low

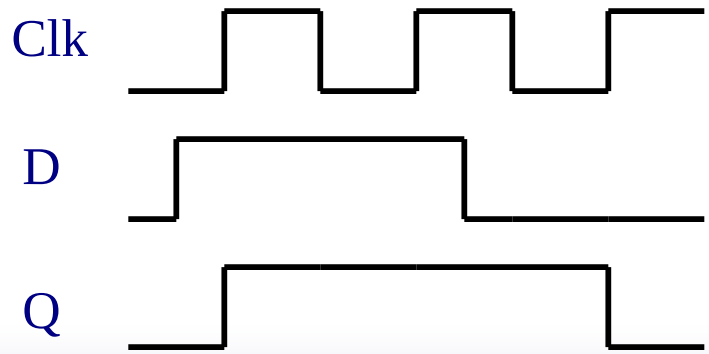


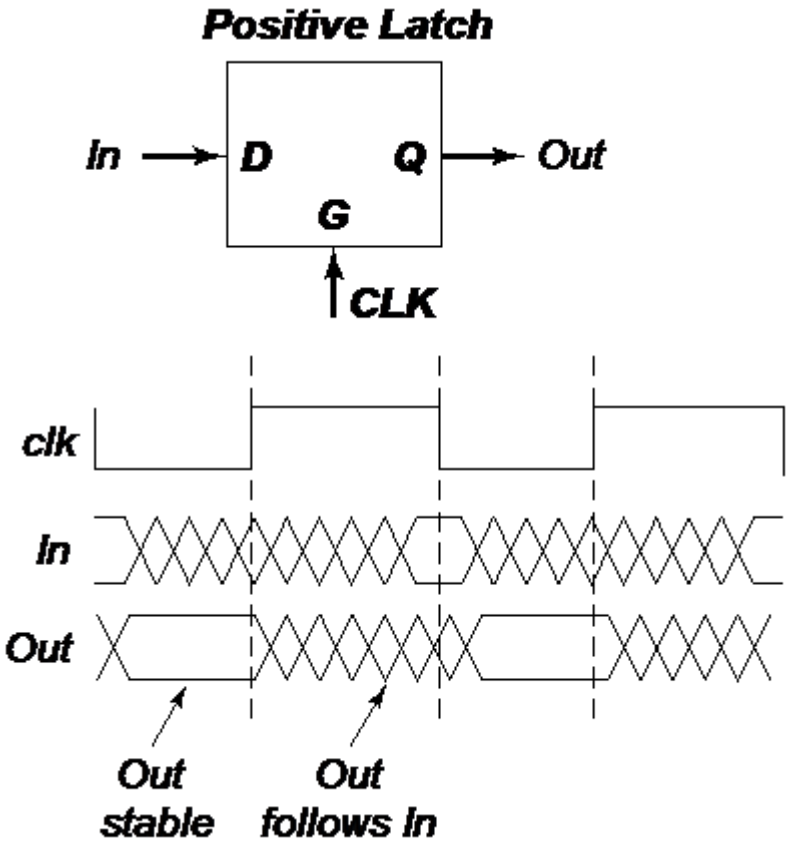

- Register

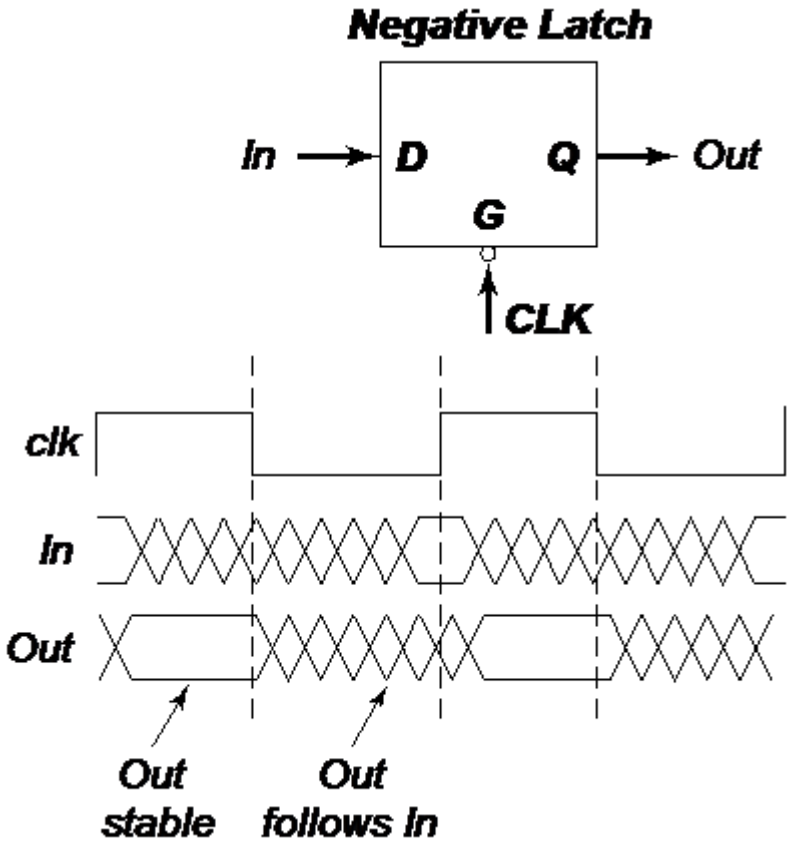
  stores data when clock rises



# Latches

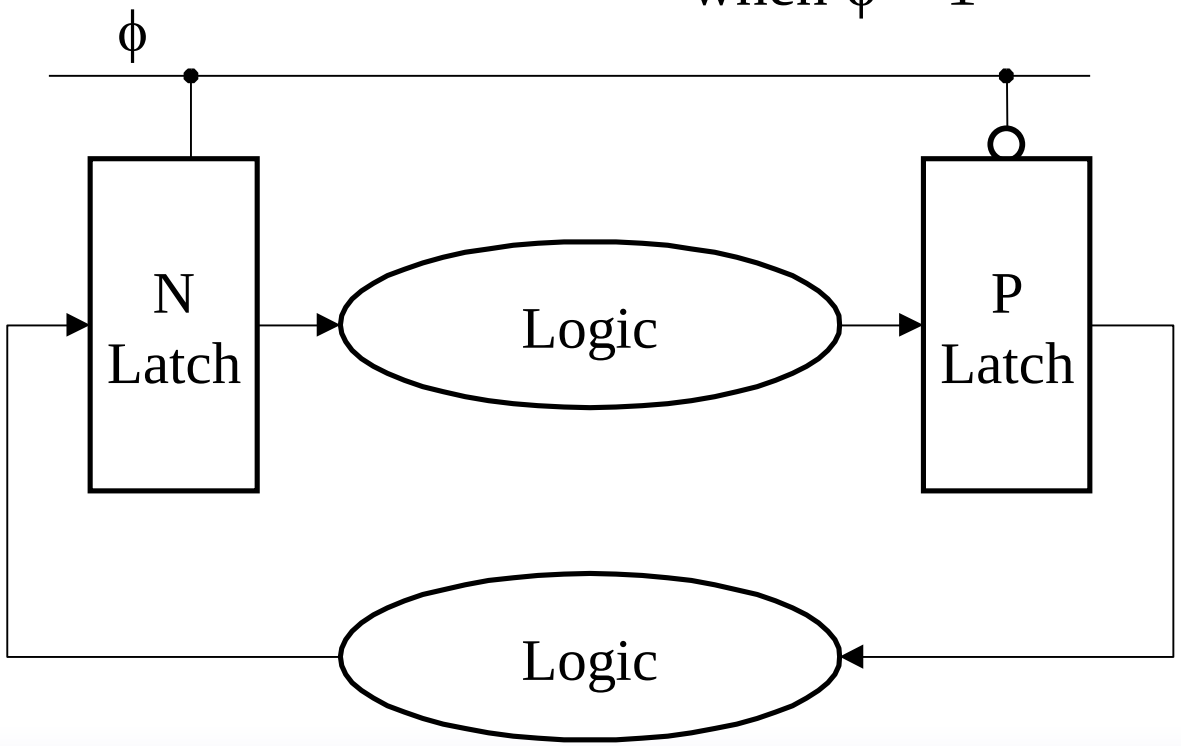

Positive Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out
stable
Out
follows In


Negative Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out
stable
Out
follows In

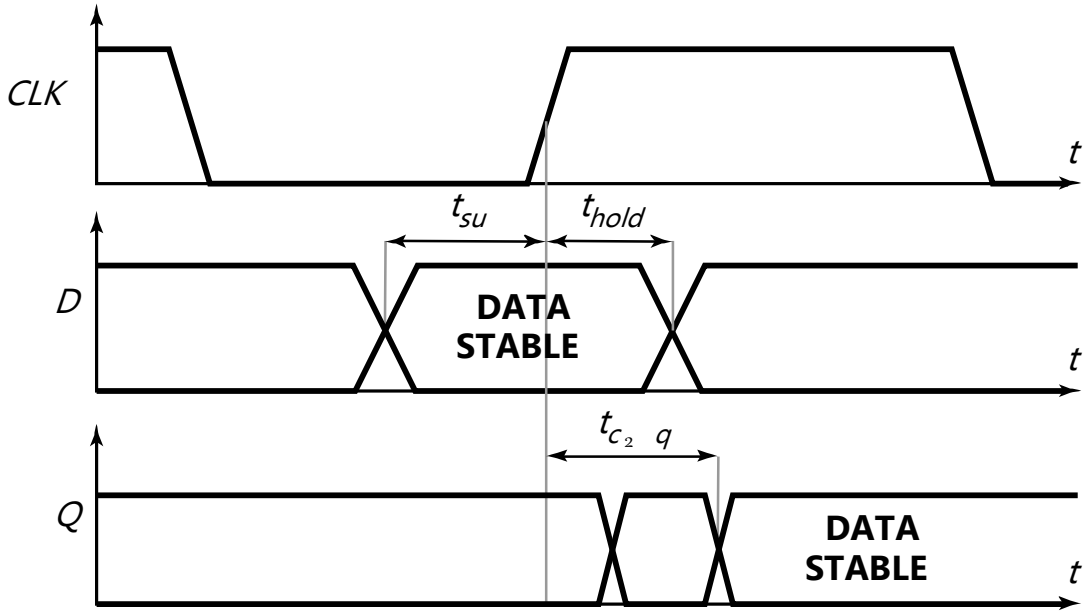
# Latch-Based Design

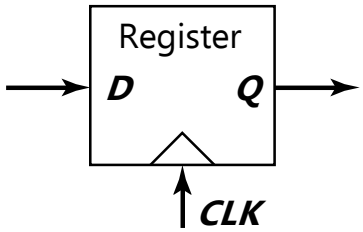
• N latch is transparent when $\phi = 0$

• P latch is transparent when $\phi = 1$

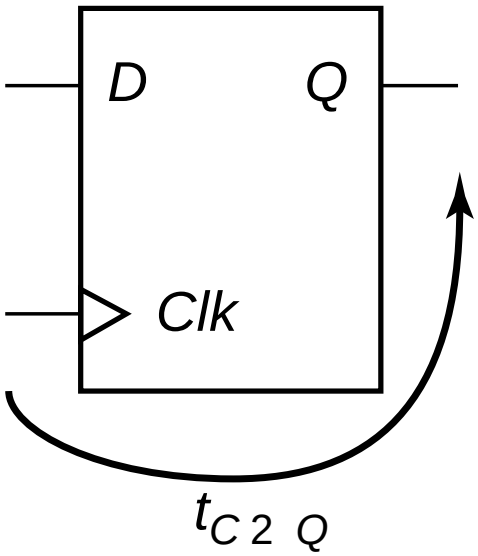


# Timing Definitions

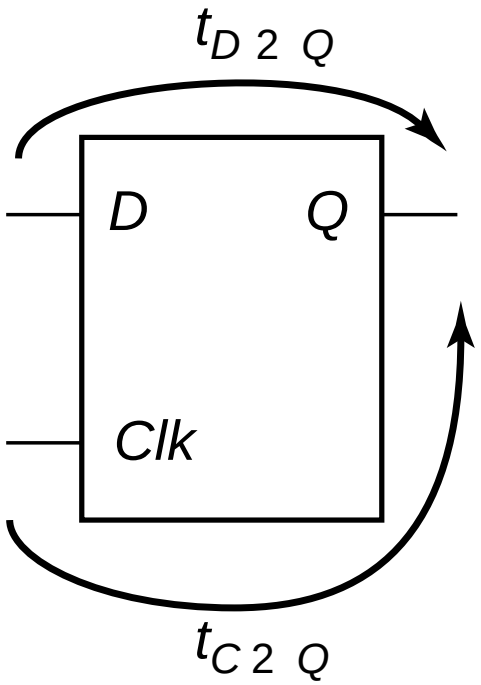


# Characterizing Timing

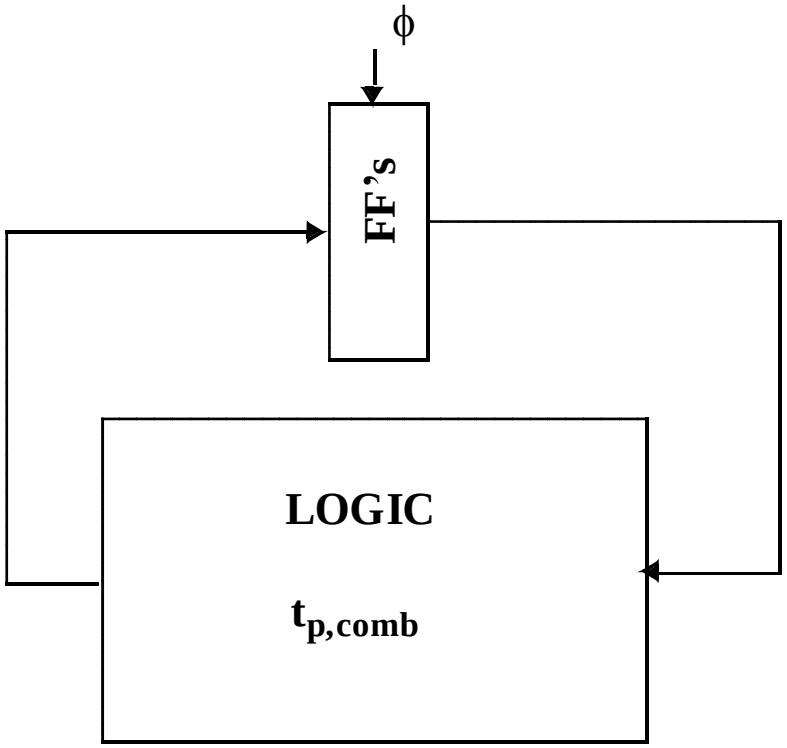



Register




Latch

# Maximum Clock Frequency



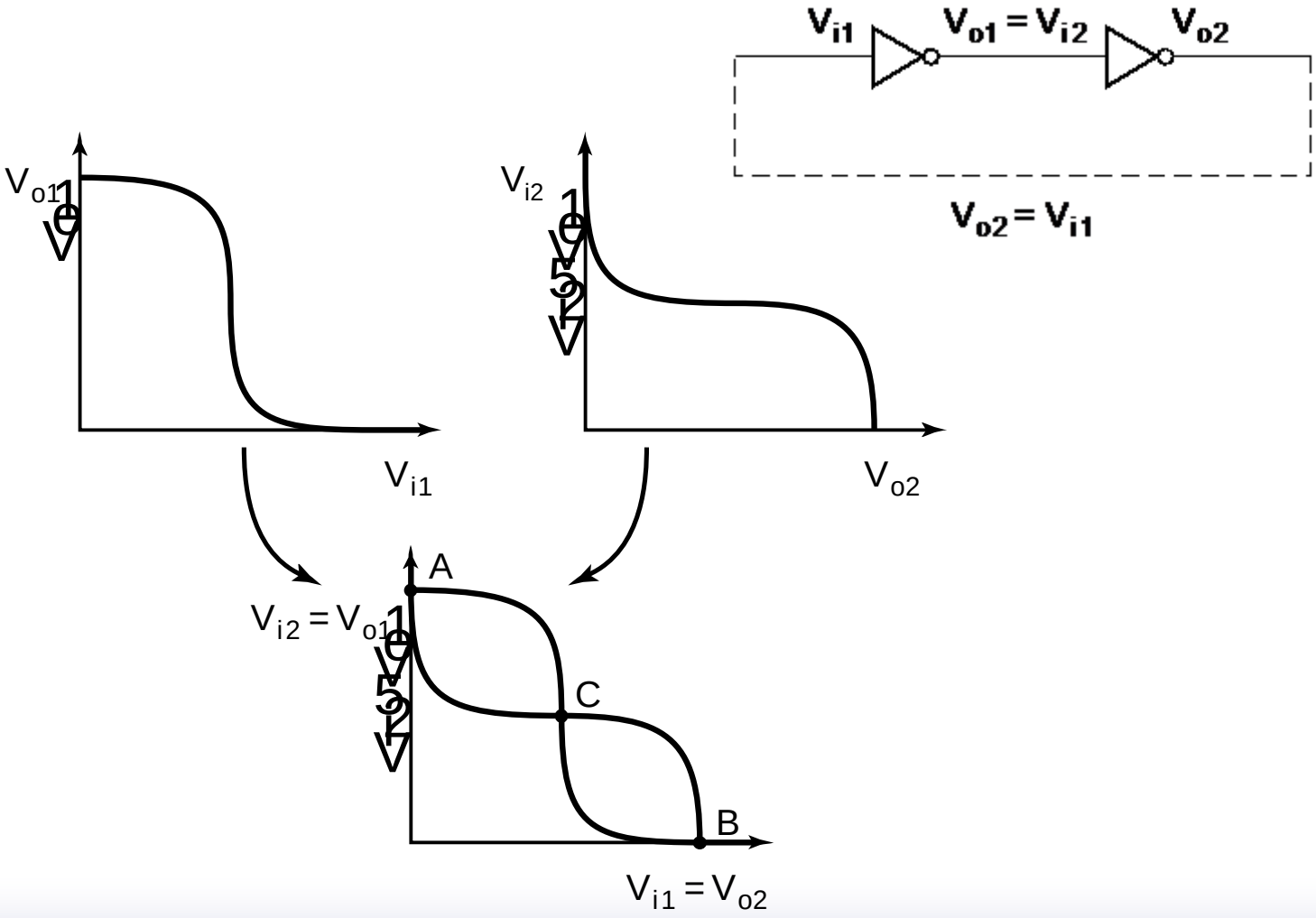

$t_{clk\text{-}Q} + t_{p,comb} + t_{setup} = T$

**Also:**

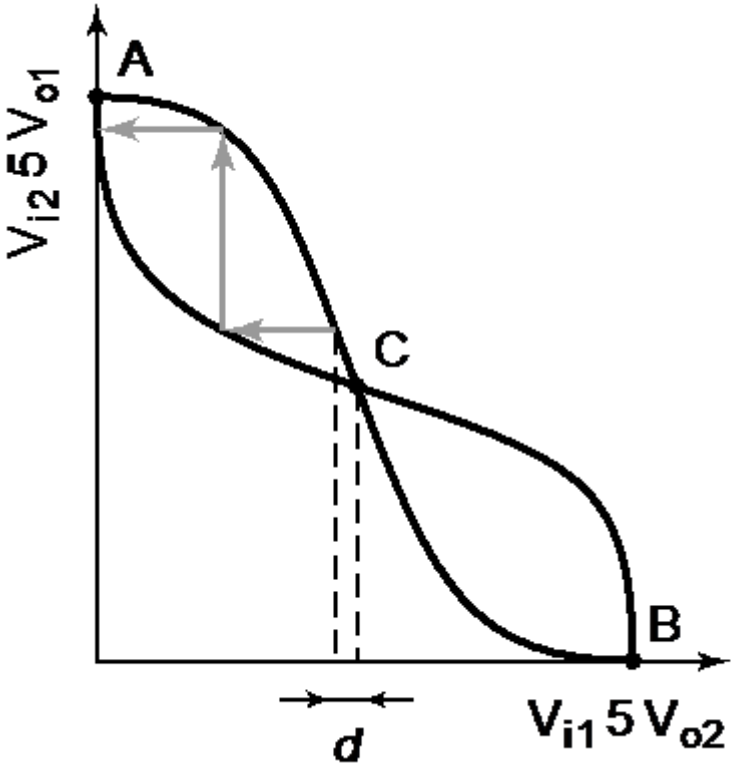
$t_{cdreg} + t_{cdlogic} > t_{hold}$

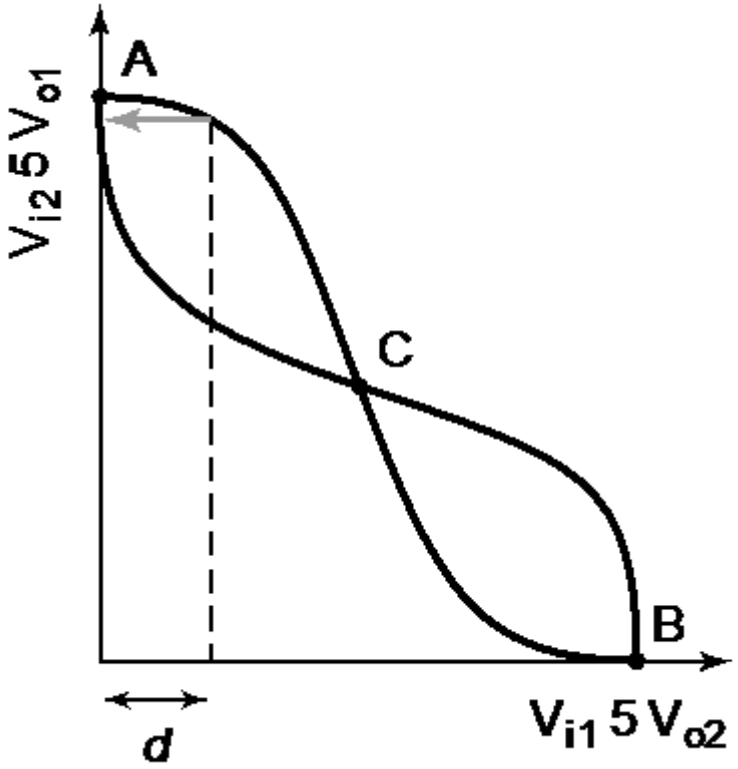
**$t_{cd}$: contamination delay = minimum delay**

# Positive Feedback: Bi-Stability



# Meta-Stability

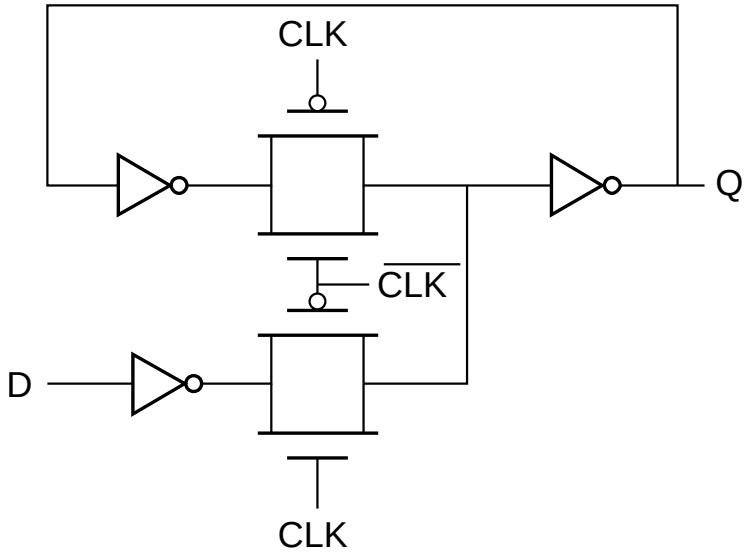


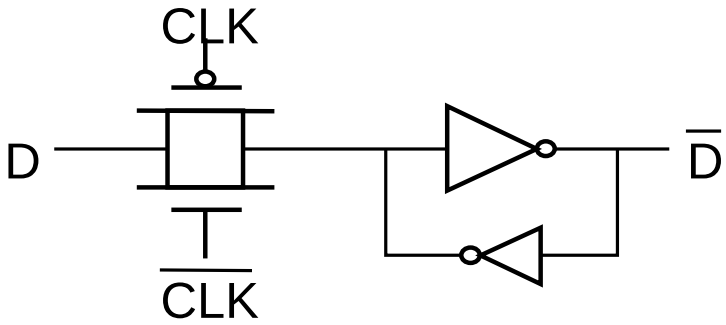

**Gain should be larger than 1 in the transition region**

# Writing into a Static Latch

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states



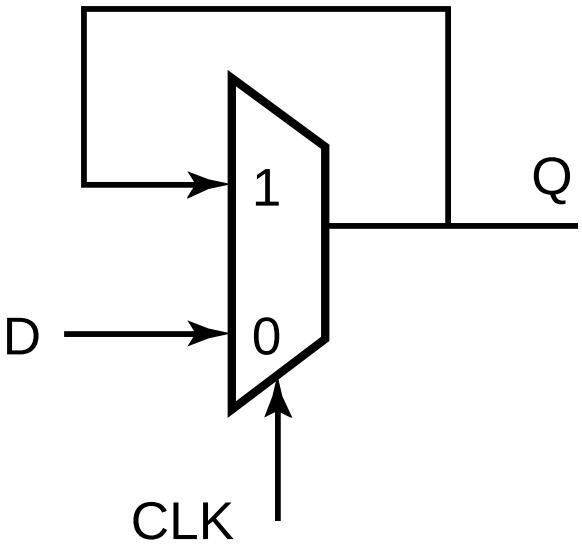

Converting into a MUX




Forcing the state
(can implement as NMOS-only)

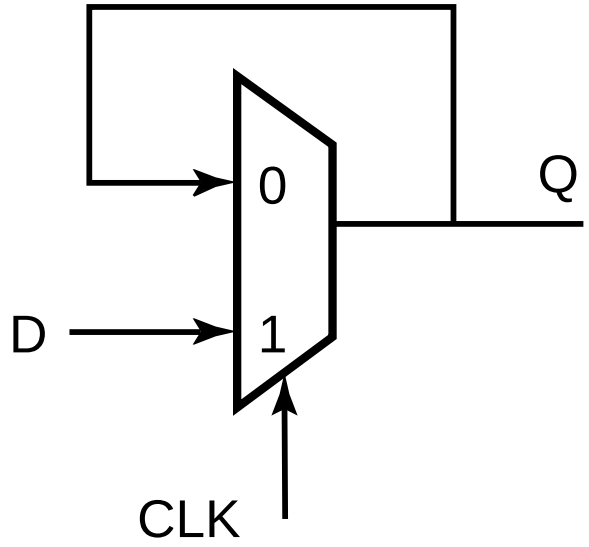
# Mux-Based Latches

**Negative latch**
**(transparent when CLK= 0)**



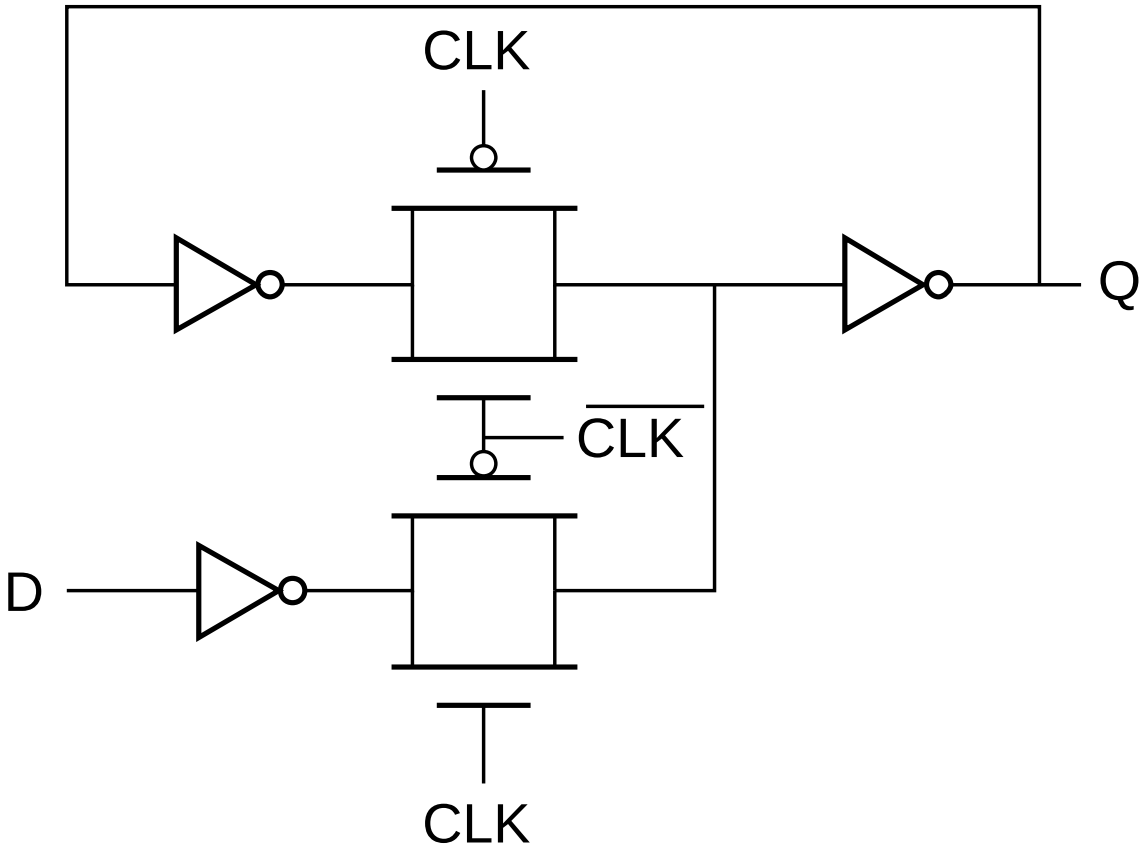

$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

**Positive latch**
**(transparent when CLK= 1)**

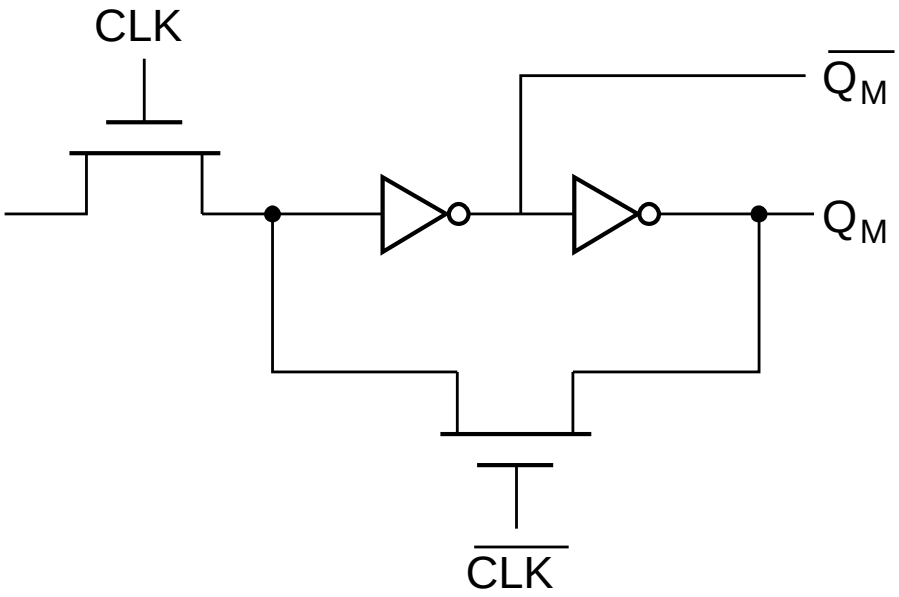



$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

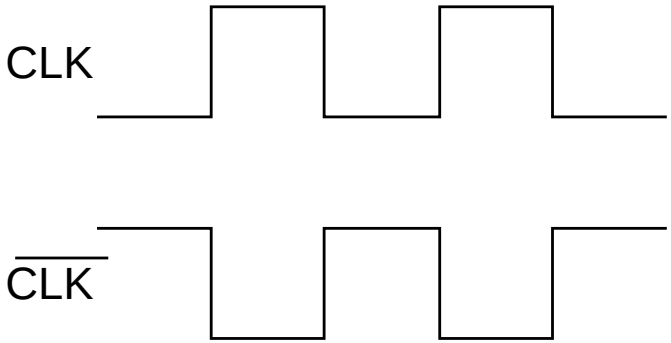
# Mux-Based Latch



# Mux-Based Latch

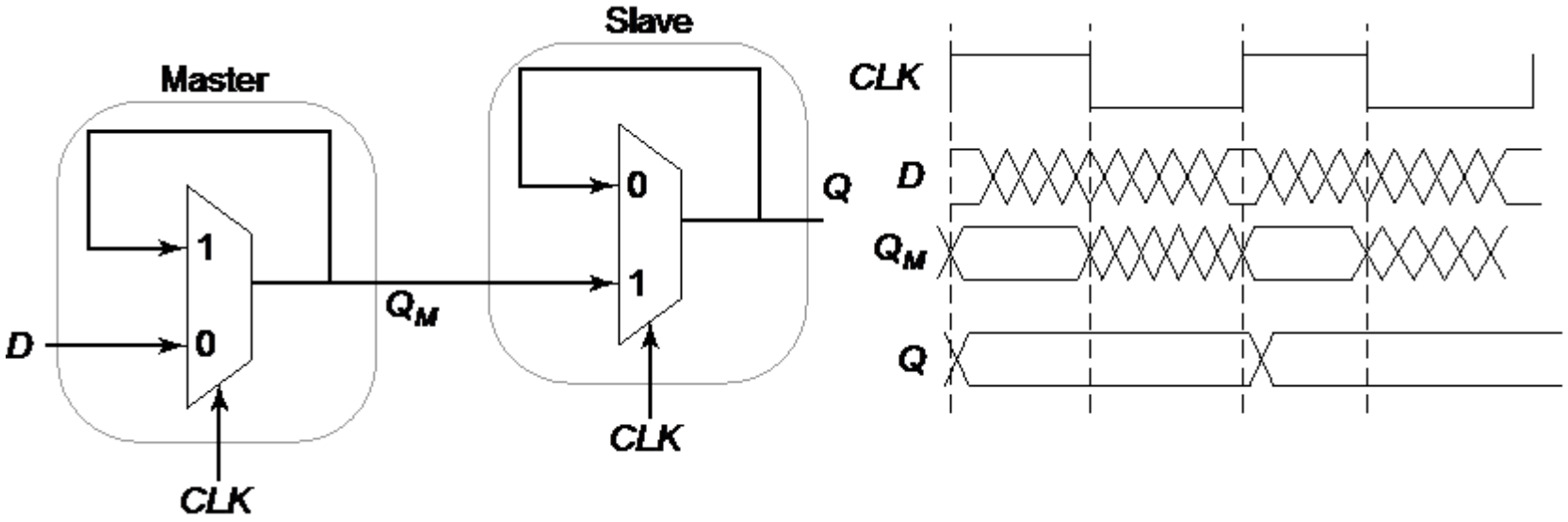



NMOS only




Non-overlapping clocks

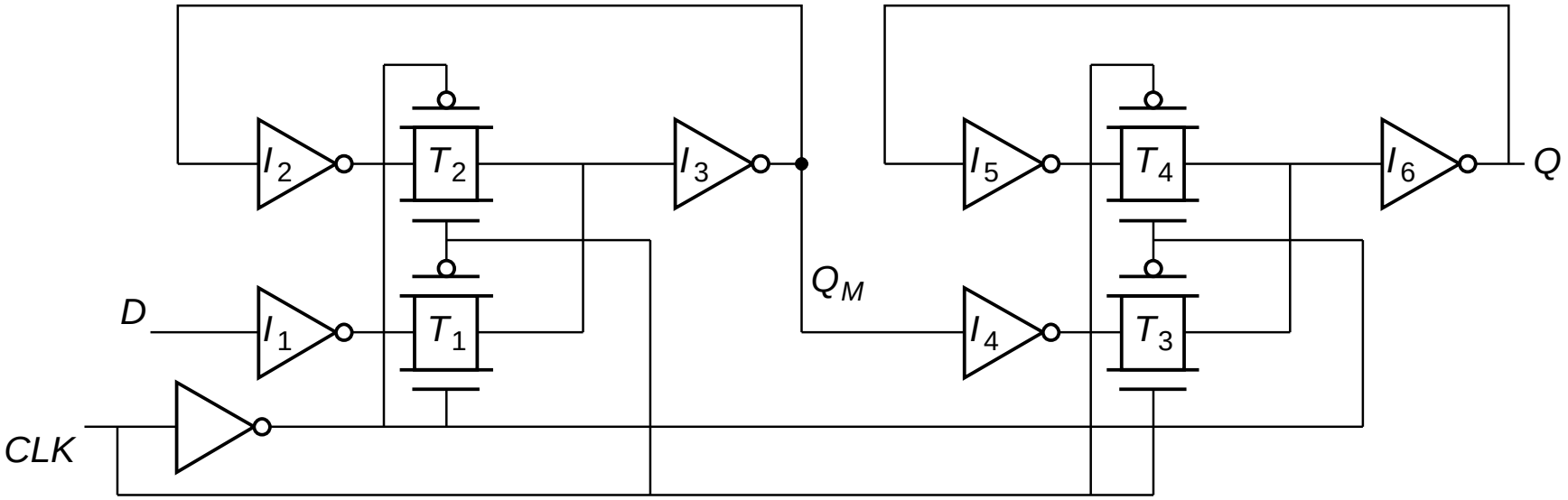
# Master-Slave (Edge-Triggered) Register



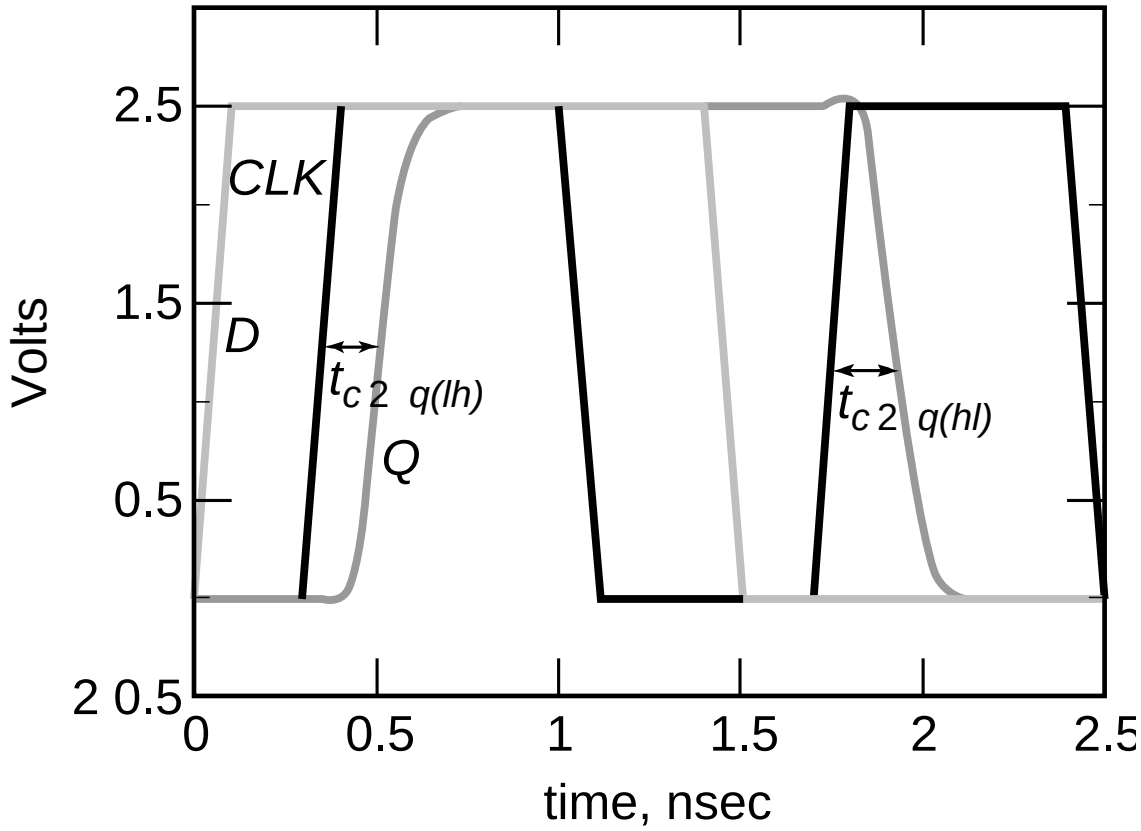

Two opposite latches trigger on edge
Also called master-slave latch pair

# Master-Slave Register

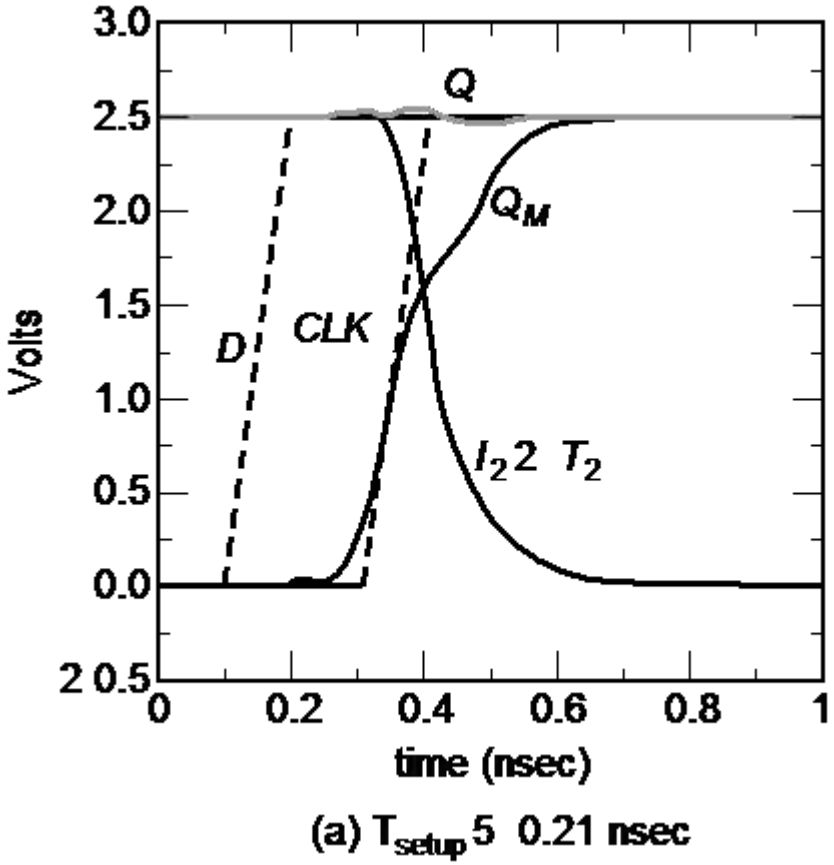
Multiplexer-based latch pair



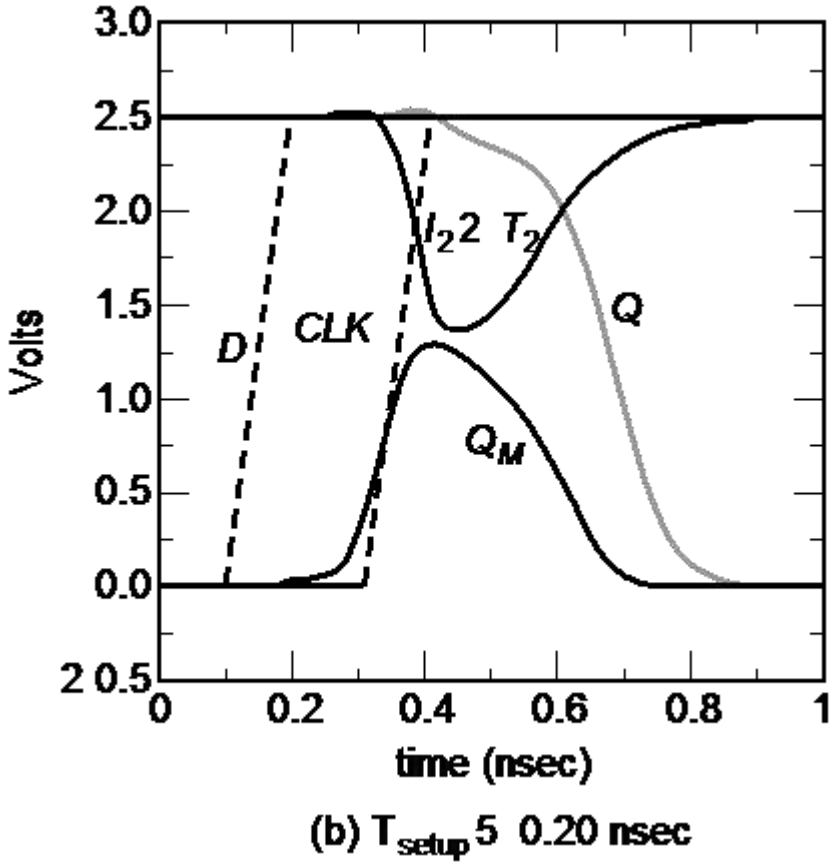
# Clk-Q Delay



# Setup Time

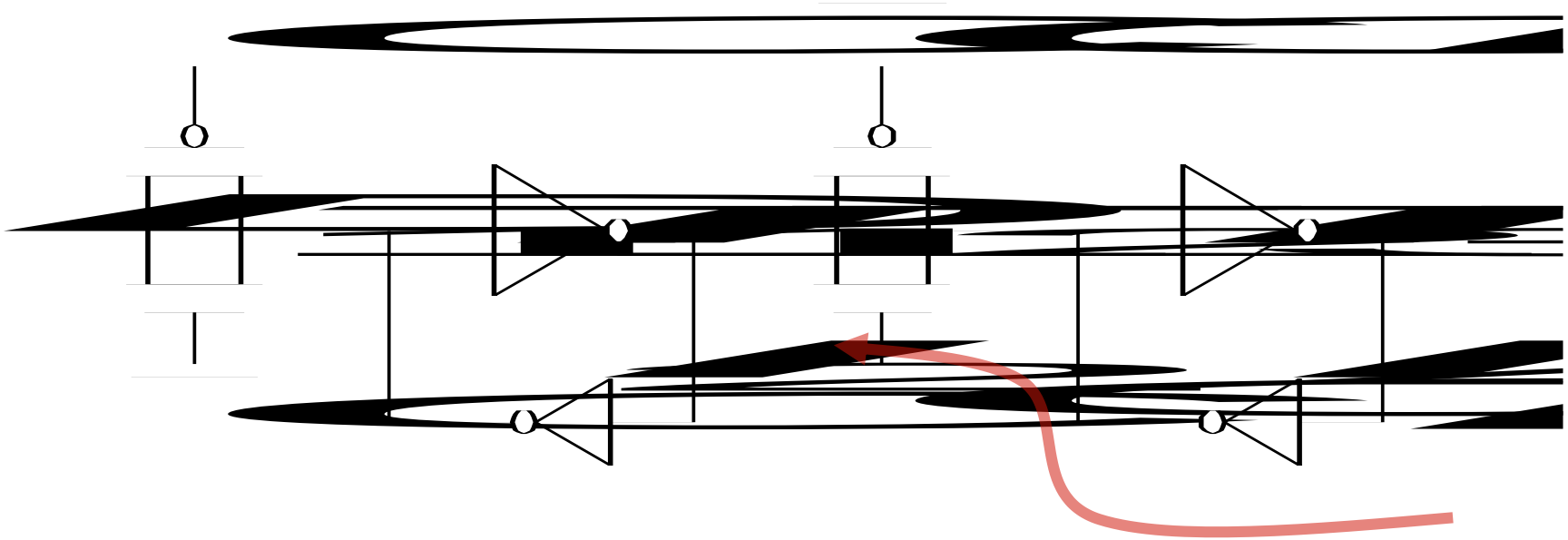



(a) $T_{setup}$ 5 0.21 nsec

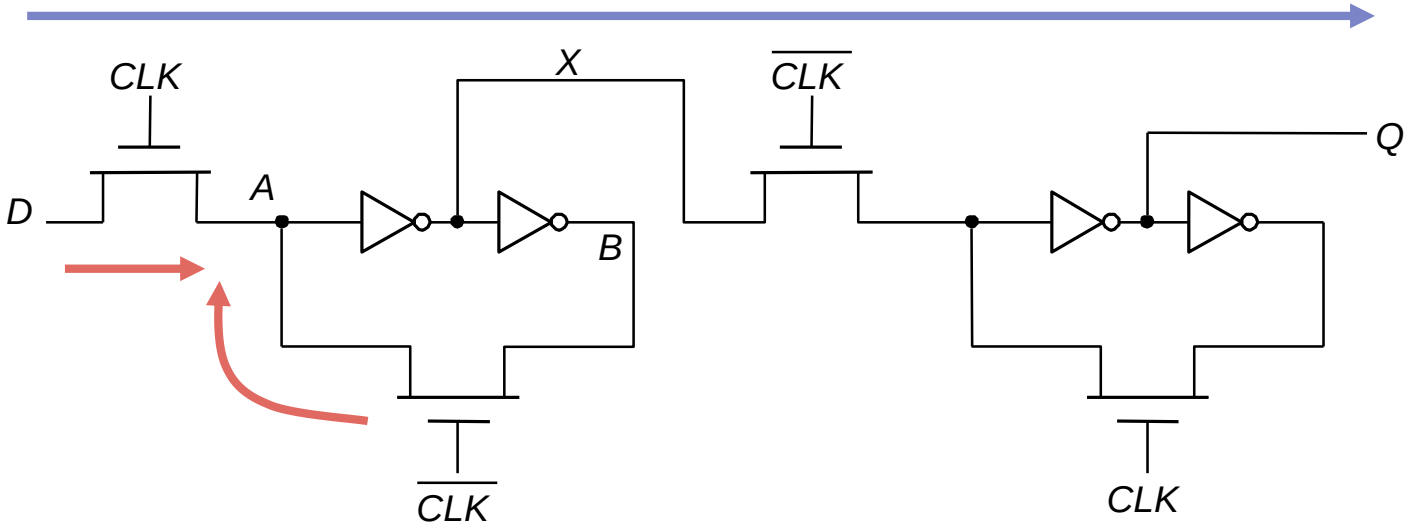



(b) $T_{setup}$ 5 0.20 nsec

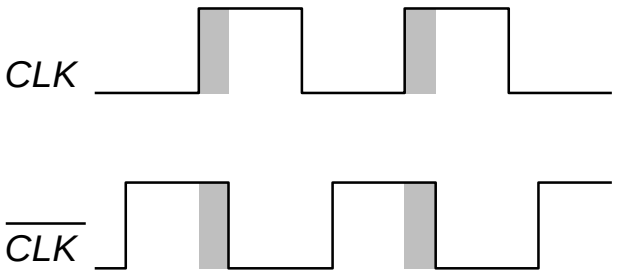
# Reduced Clock Load Master-Slave Register



# Avoiding Clock Overlap



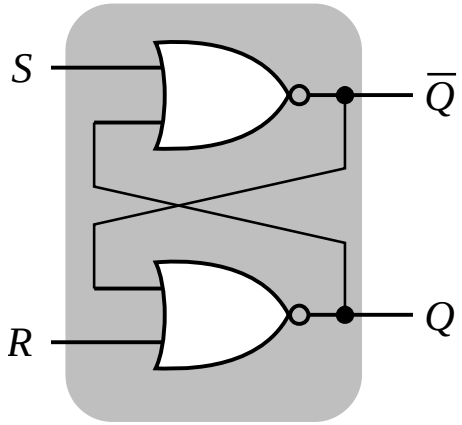

(a) Schematic diagram

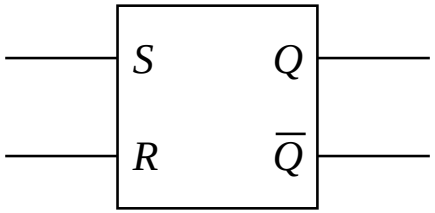



(b) Overlapping clock pairs

# Overpowering the Feedback Loop — Cross-Coupled Pairs

NOR-based set-reset



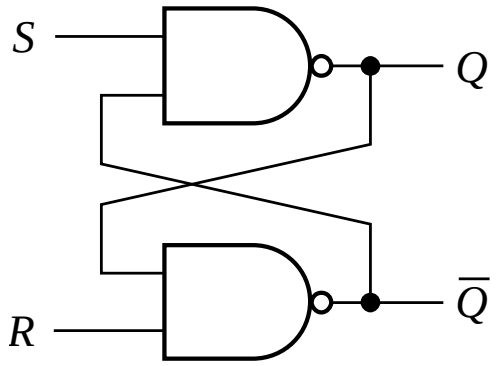




| S | R | Q | $\overline{Q}$ |
|---|---|---|---|
| 0 | 0 | Q | $\overline{Q}$ |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 |

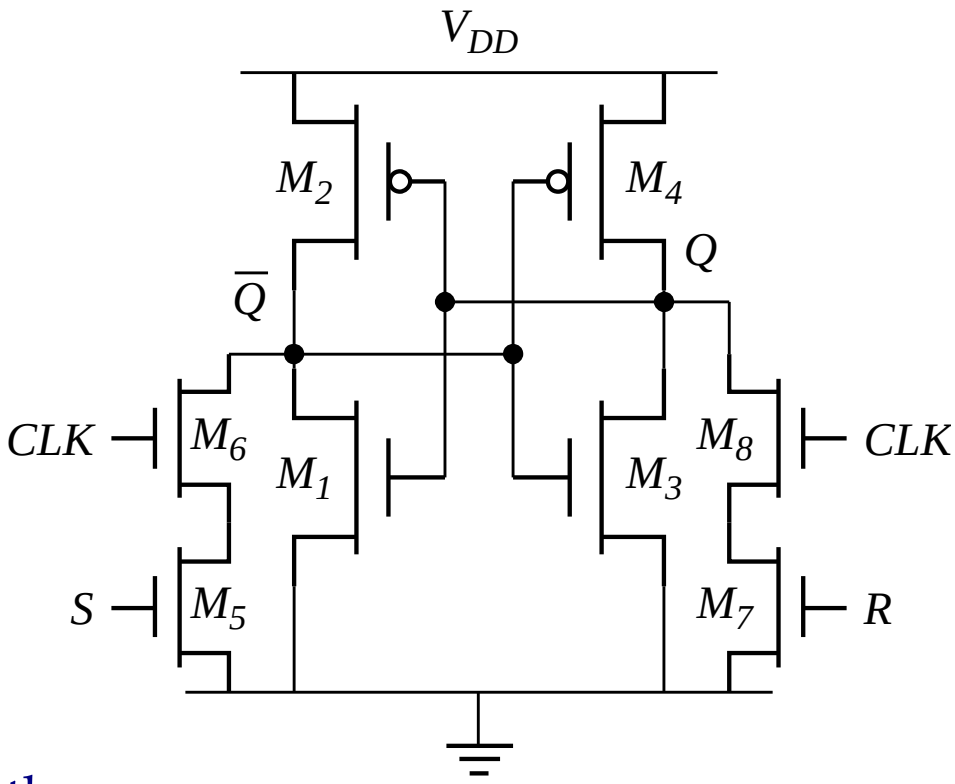
Forbidden State

# Cross-Coupled NAND

Cross-coupled NANDs

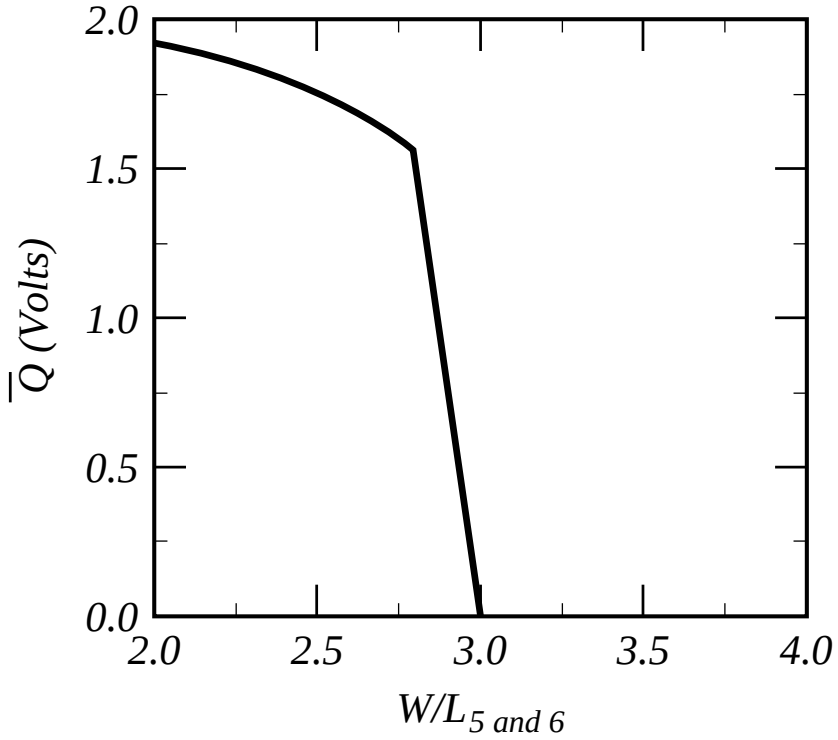



Added clock



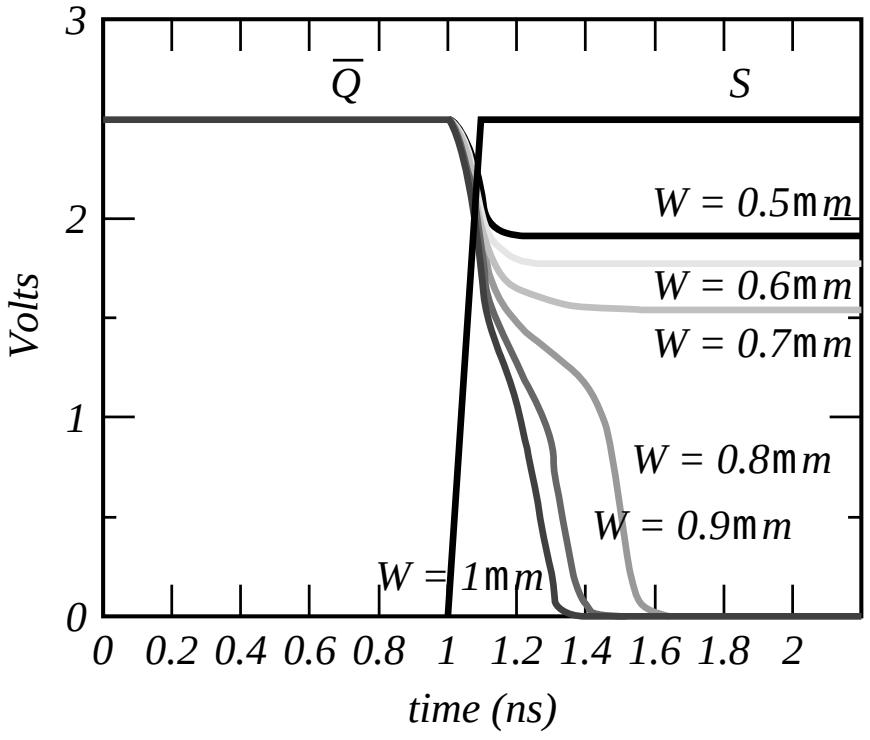

This is not used in datapaths any more, but is a basic building memory cell

# Sizing Issues




(a)

Output voltage dependence on transistor width

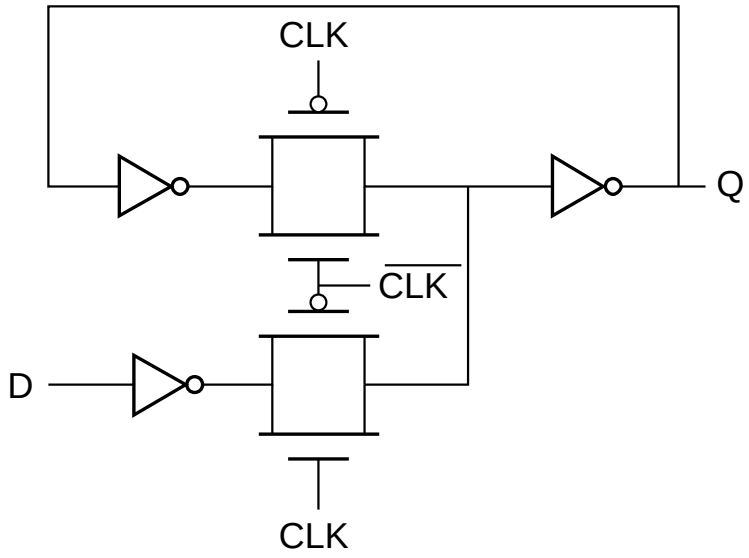



(b)

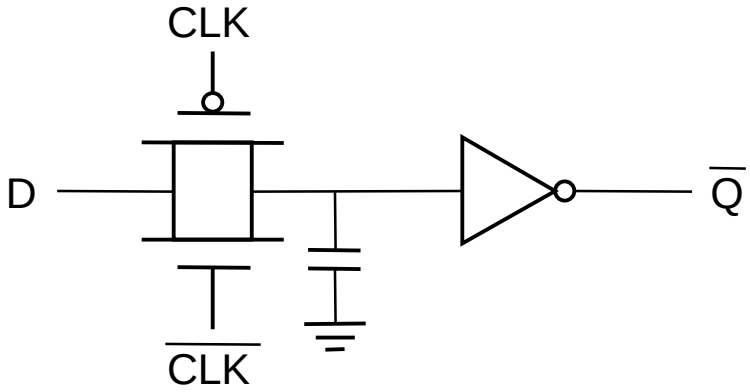
Transient response

# Storage Mechanisms

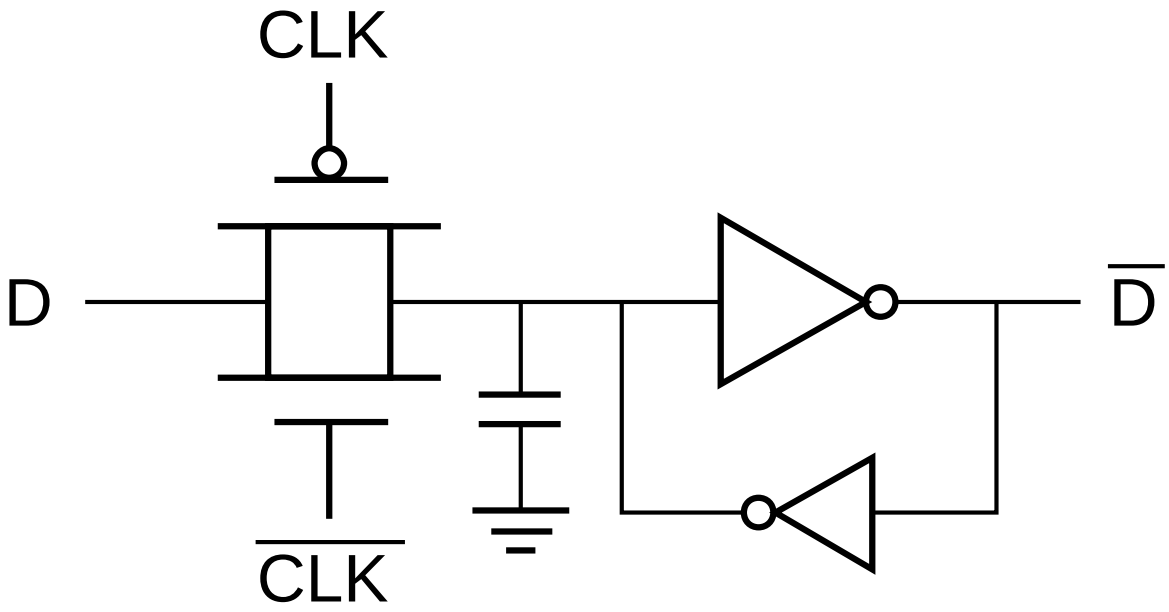
Static



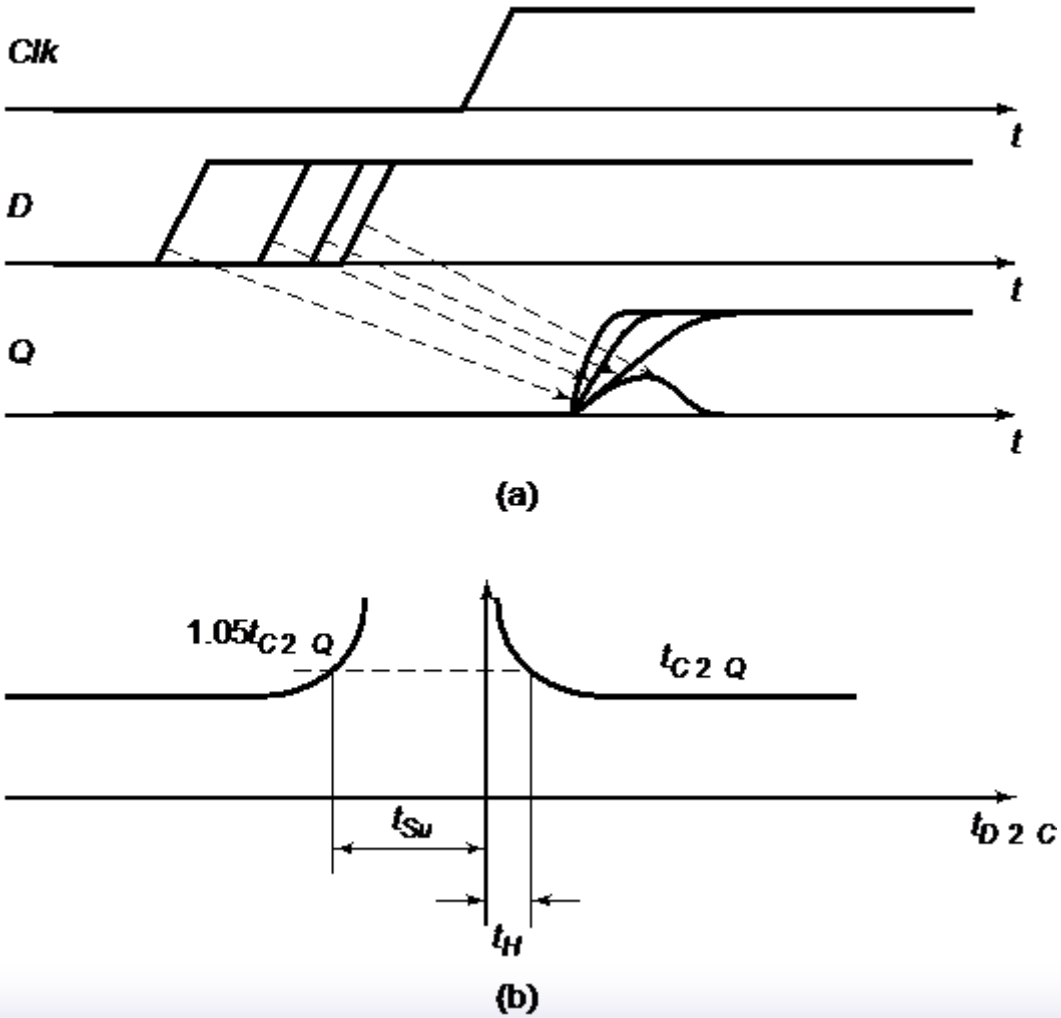

Dynamic (charge-based)



# Making a Dynamic Latch Pseudo-Static

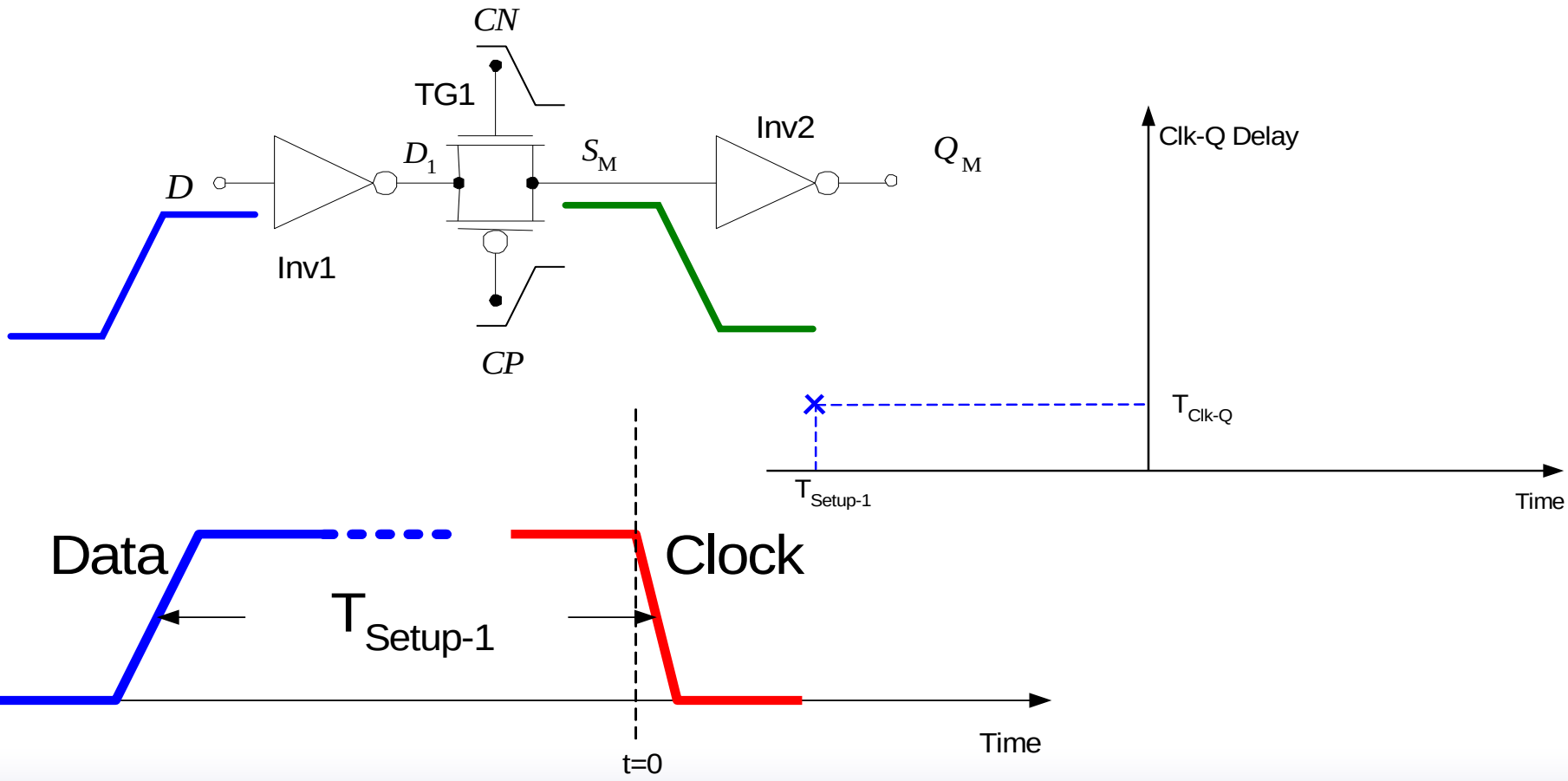


# More Precise Setup Time



# Setup/Hold Time Illustrations

## Circuit before clock arrival (Setup-1 case)



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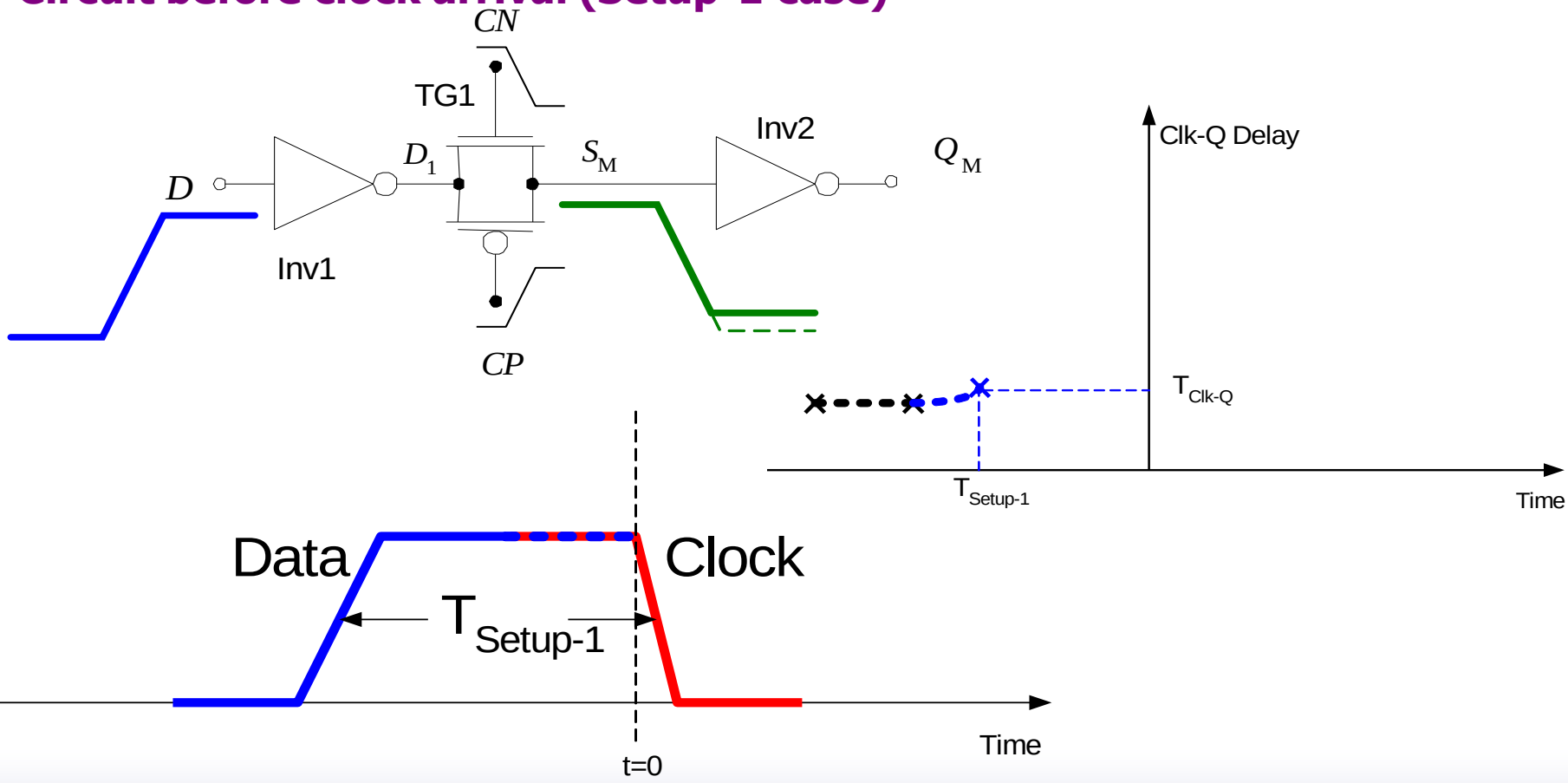

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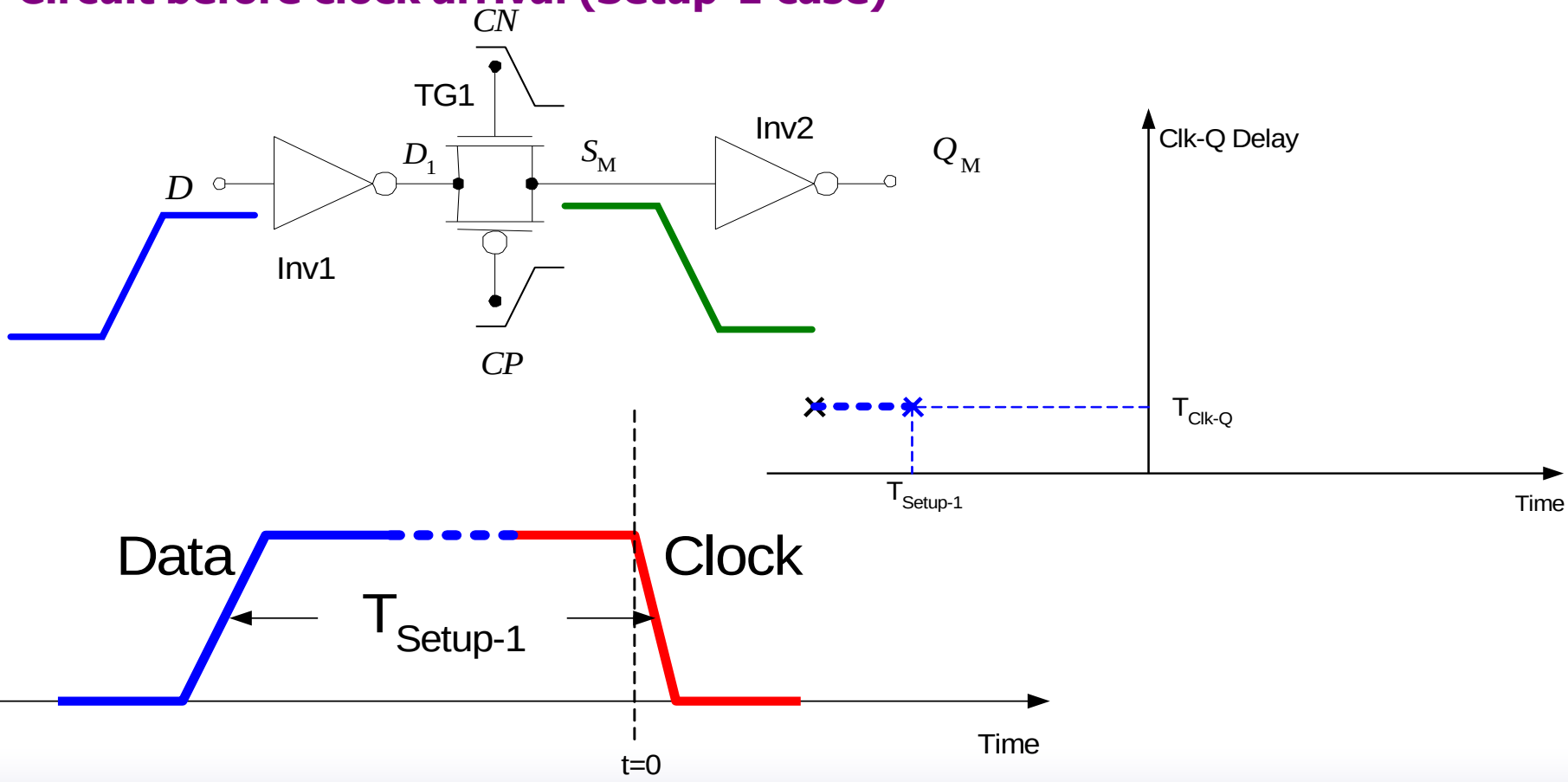

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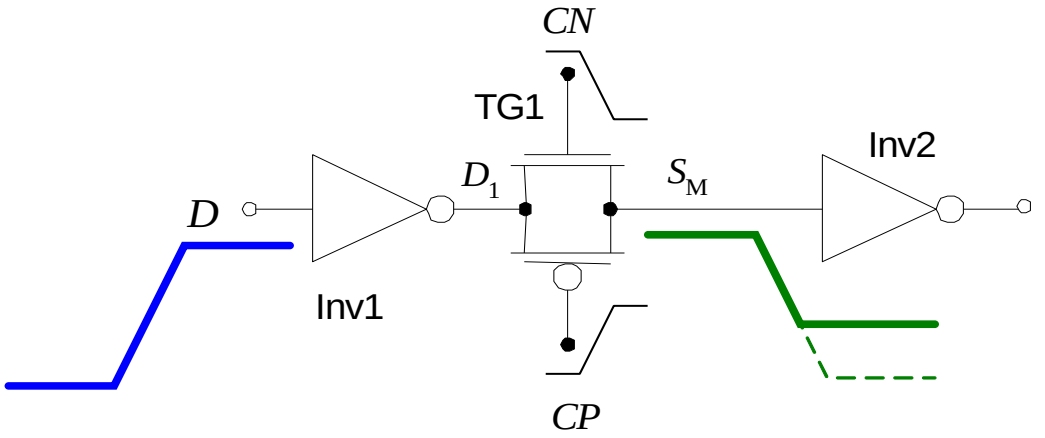


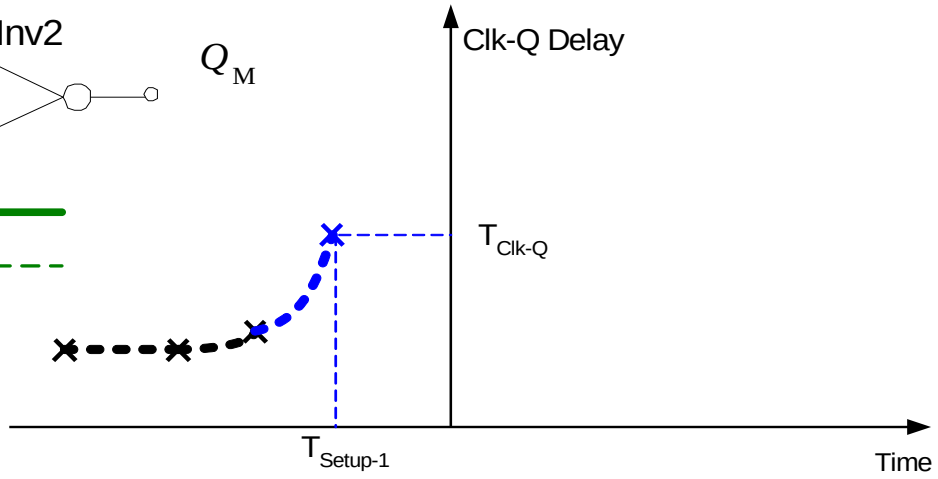


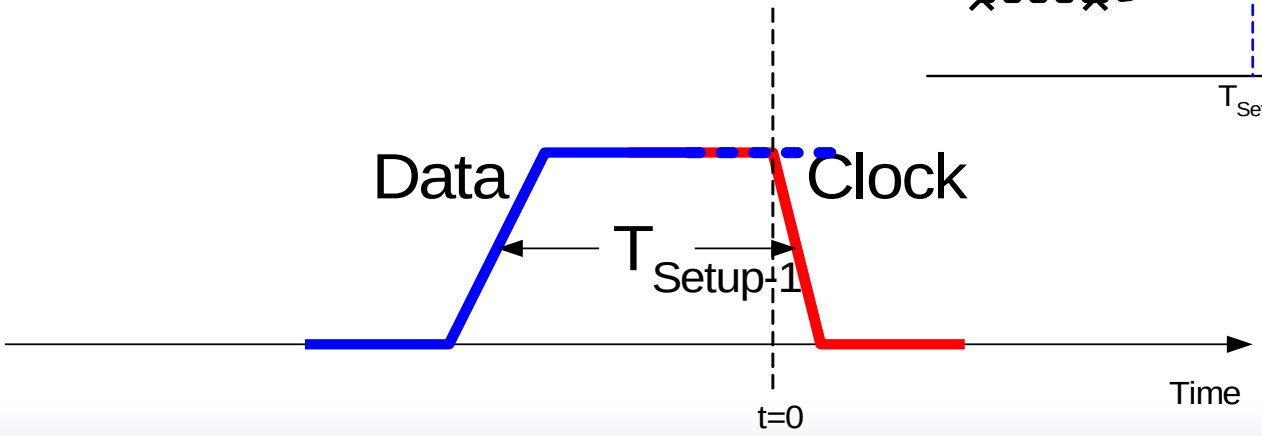

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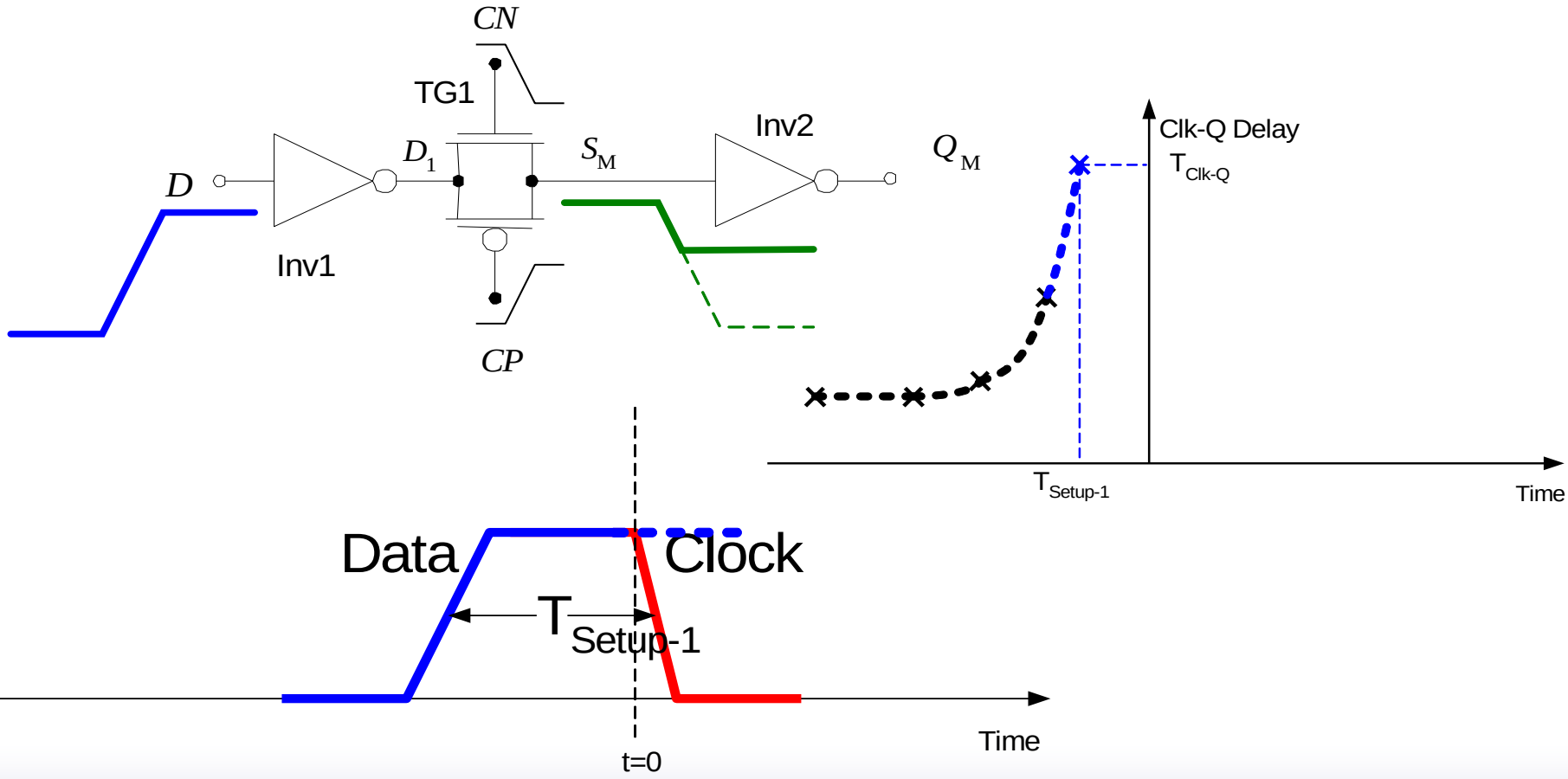

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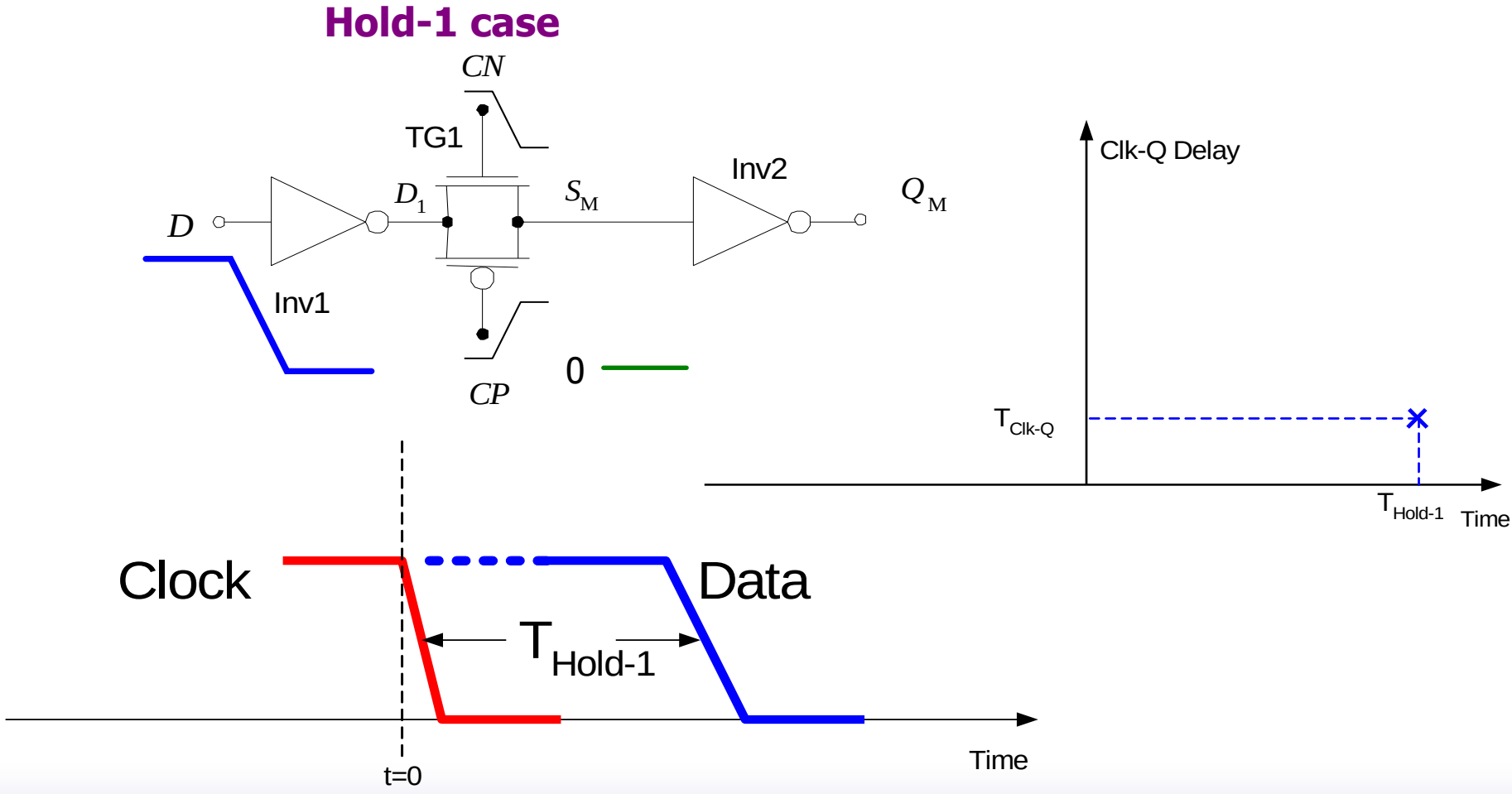

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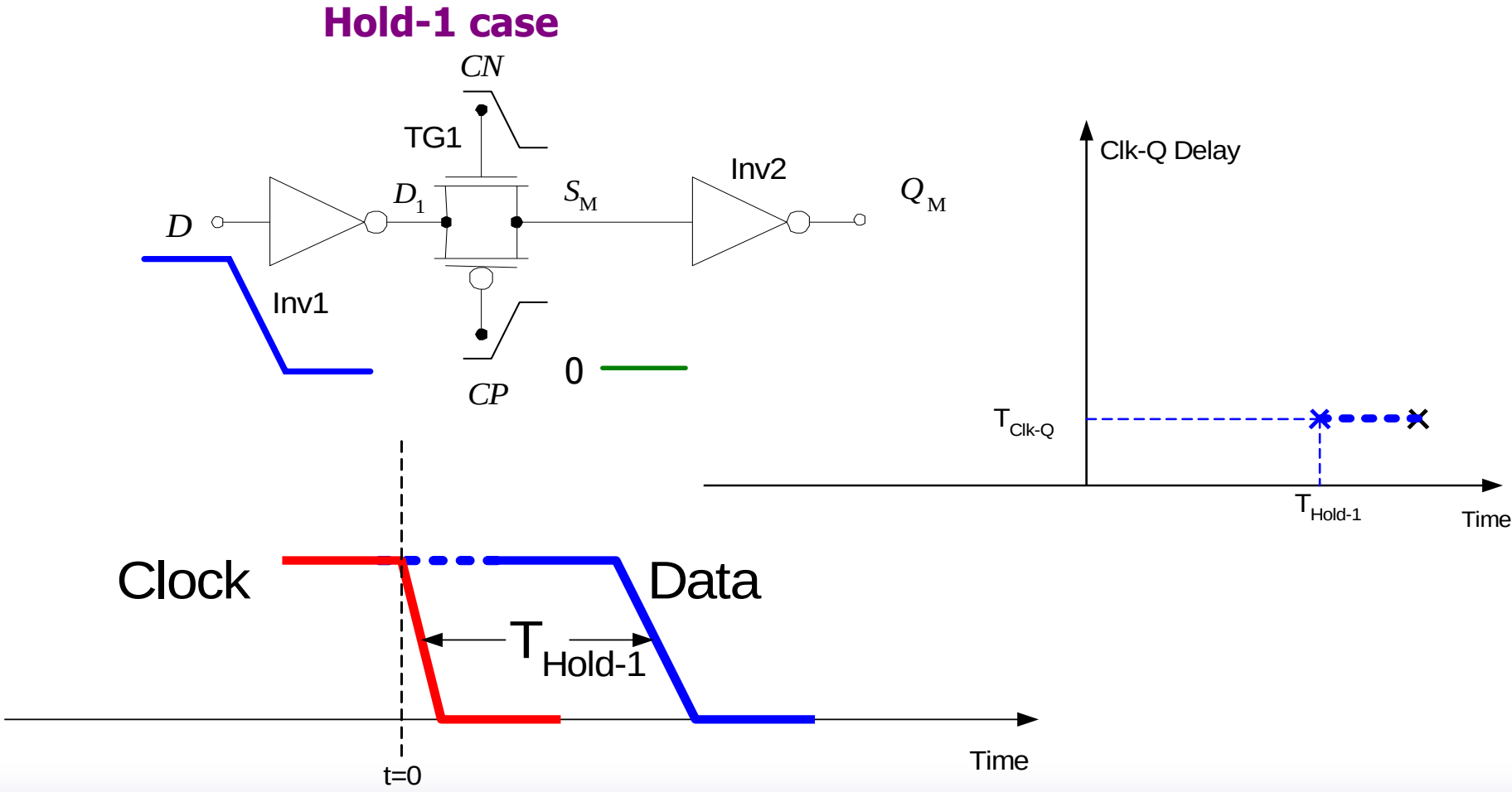

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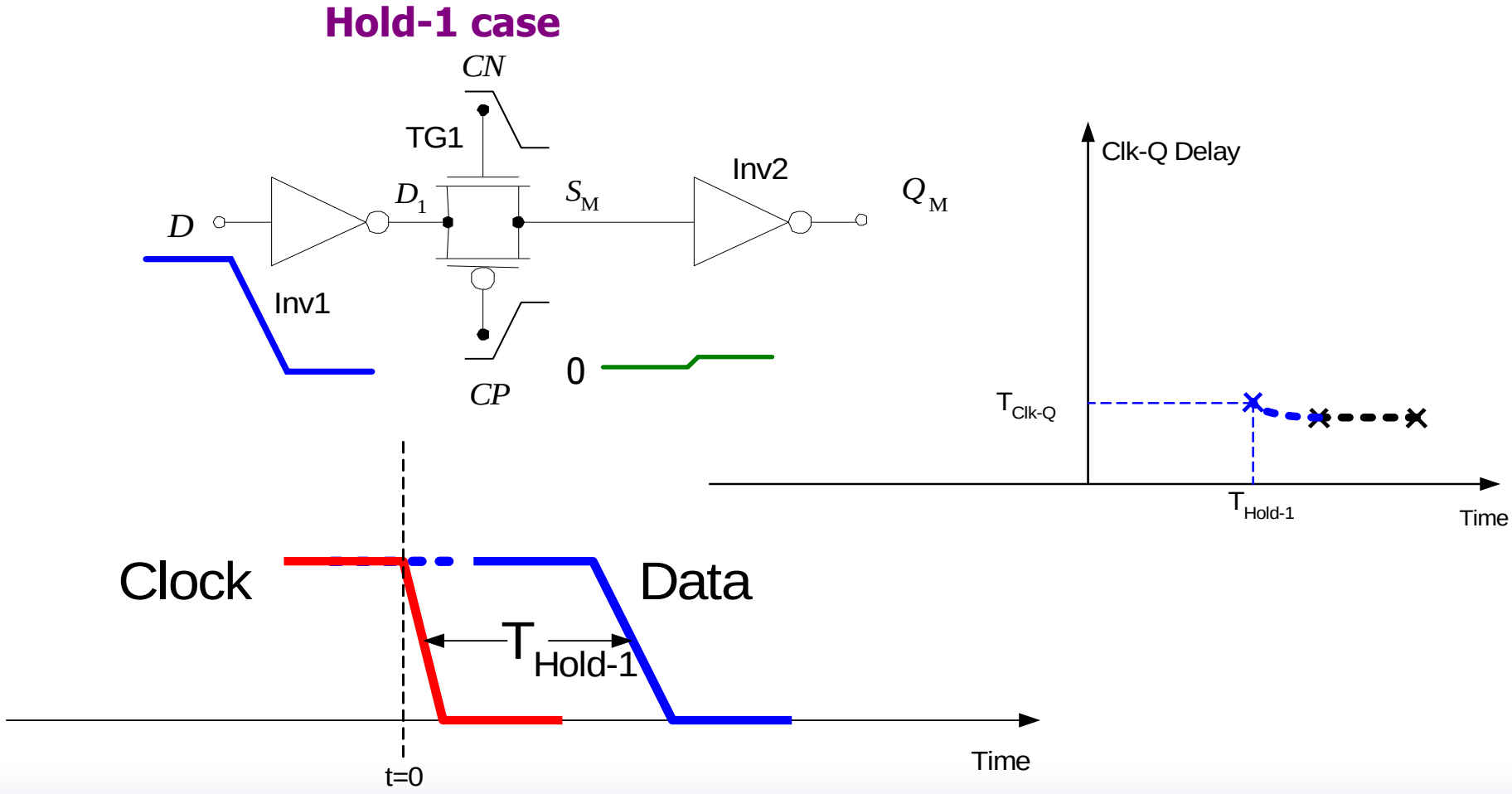

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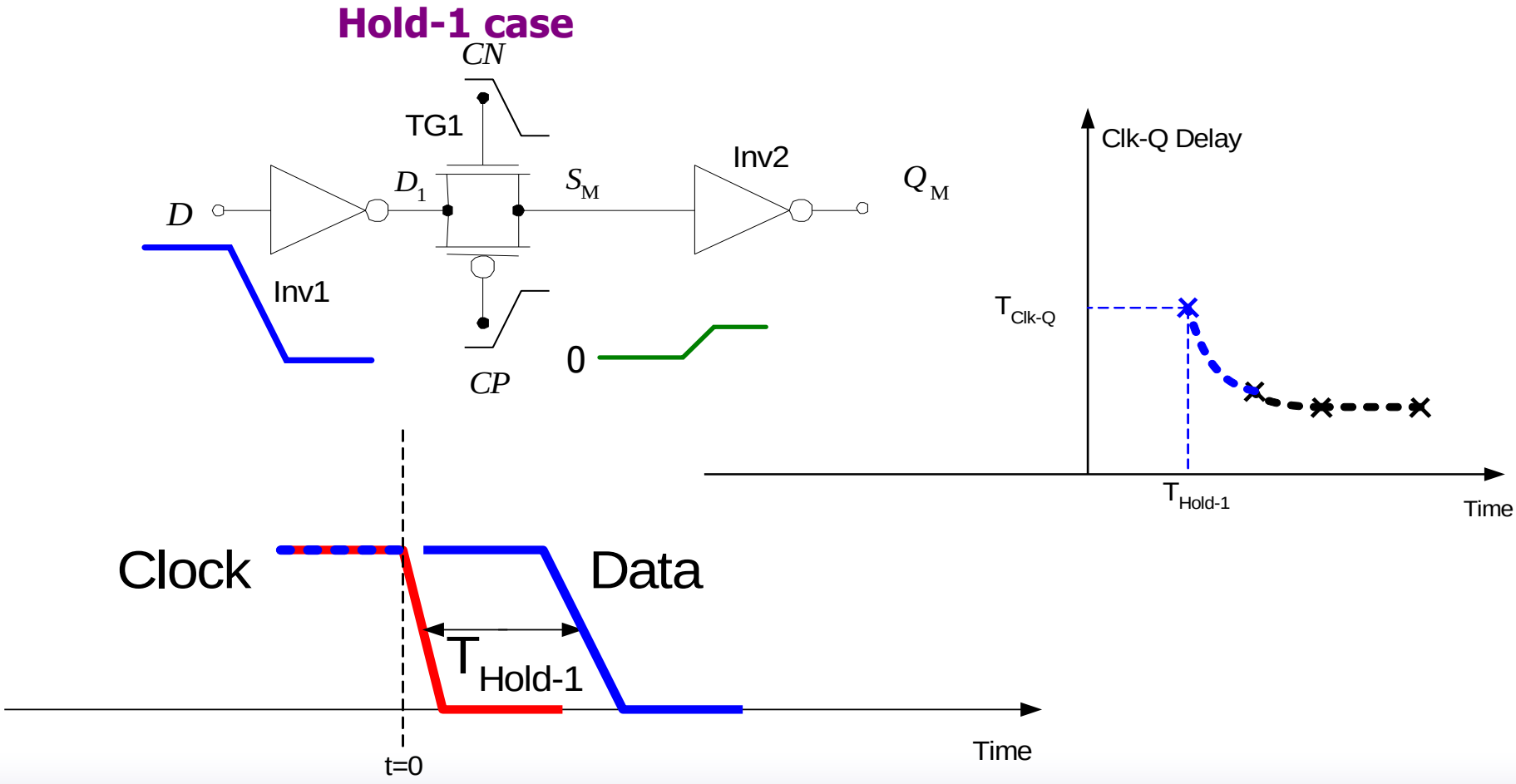
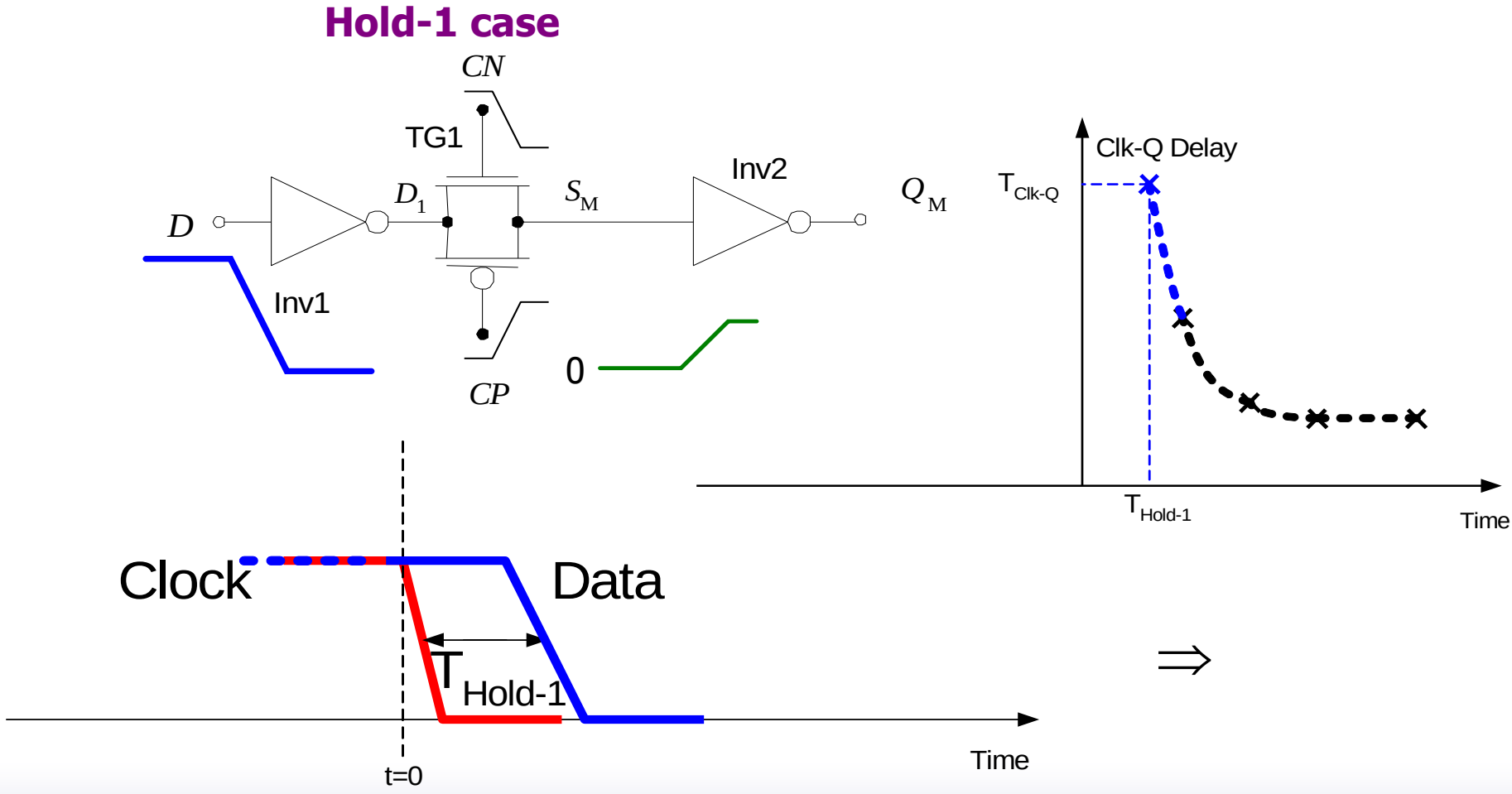
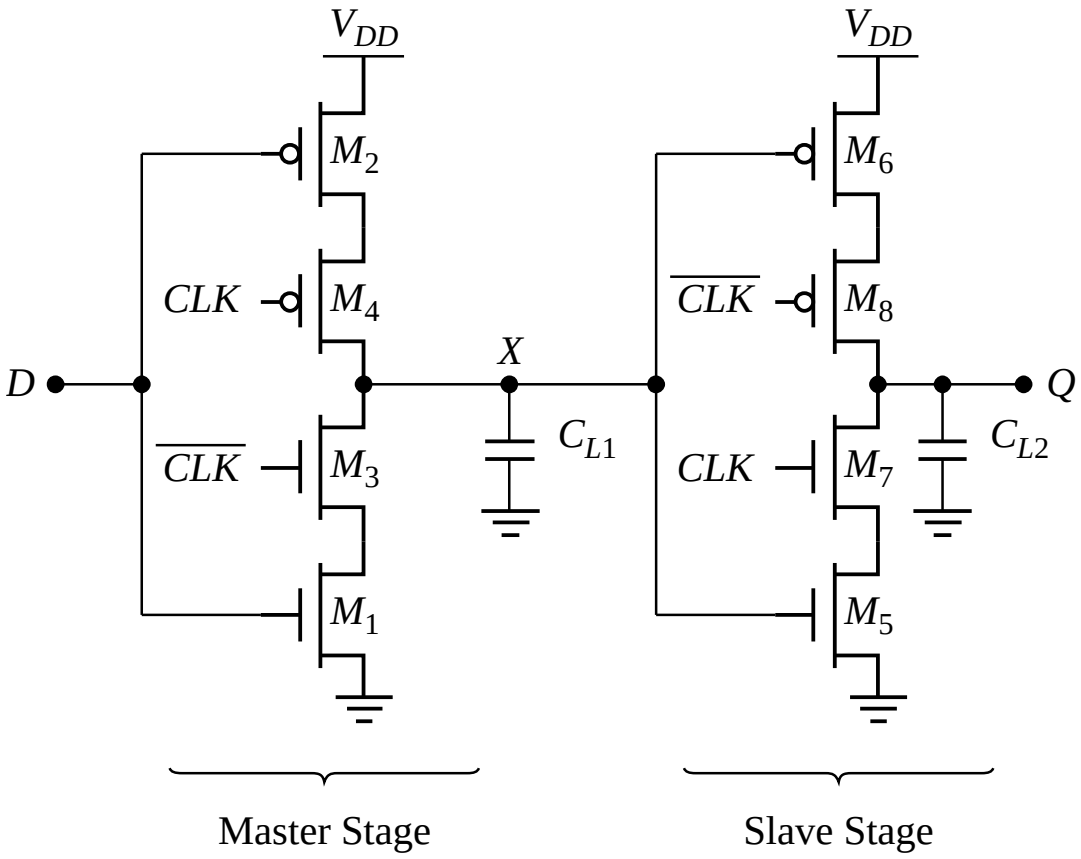


# Setup/Hold Time Illustrations

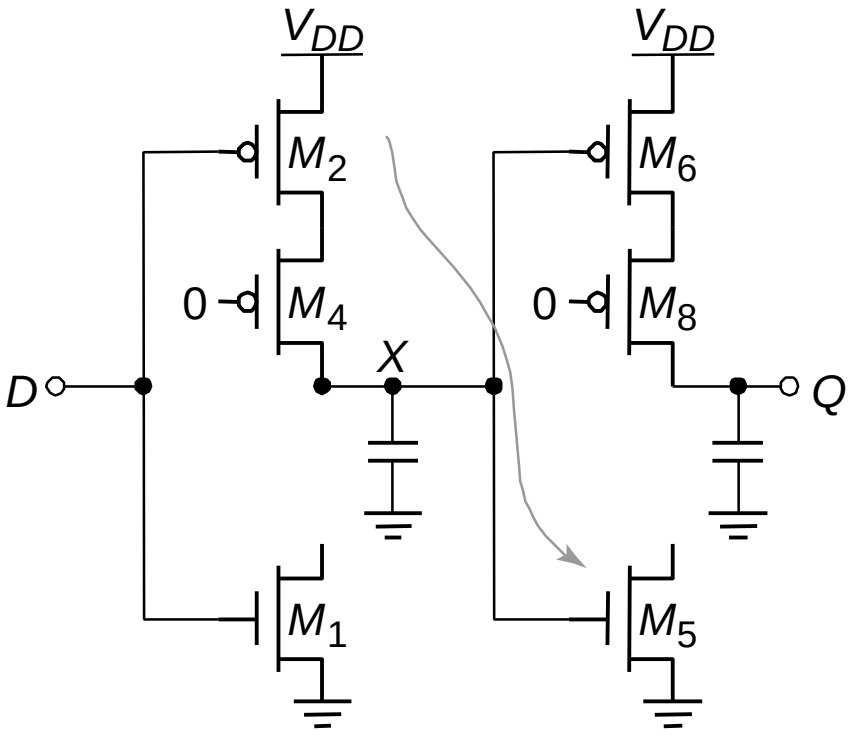


# Other Latches/Registers: C²MOS

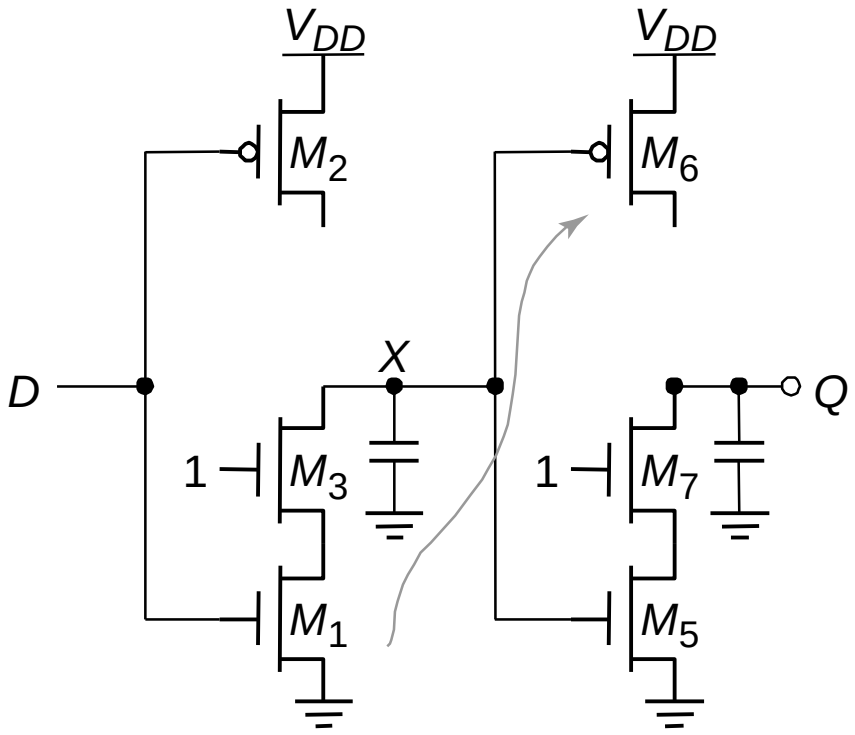



"Keepers" can be added to make circuit pseudo-static

# Insensitive to Clock-Overlap

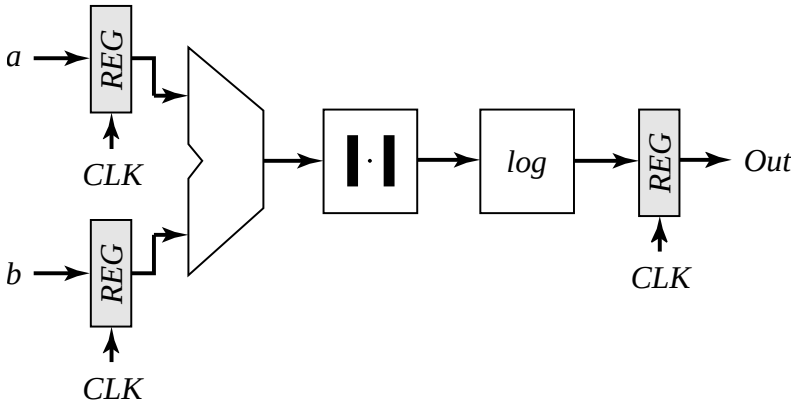



(a) (0-0) overlap



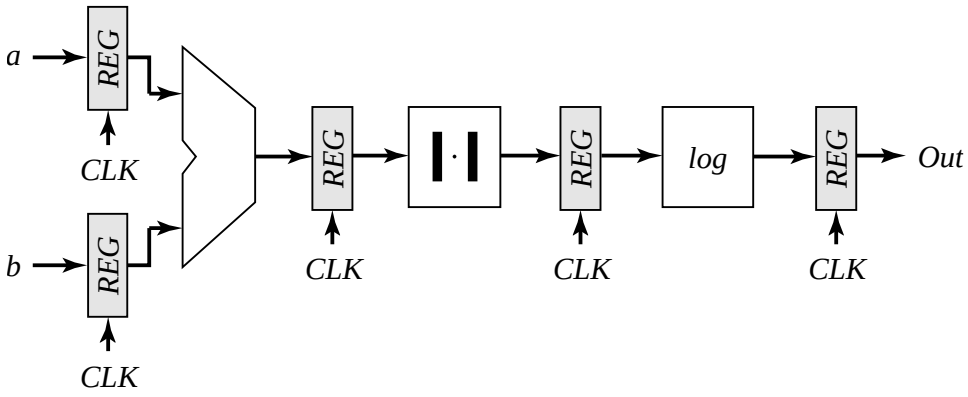

(b) (1-1) overlap

# Pipelining



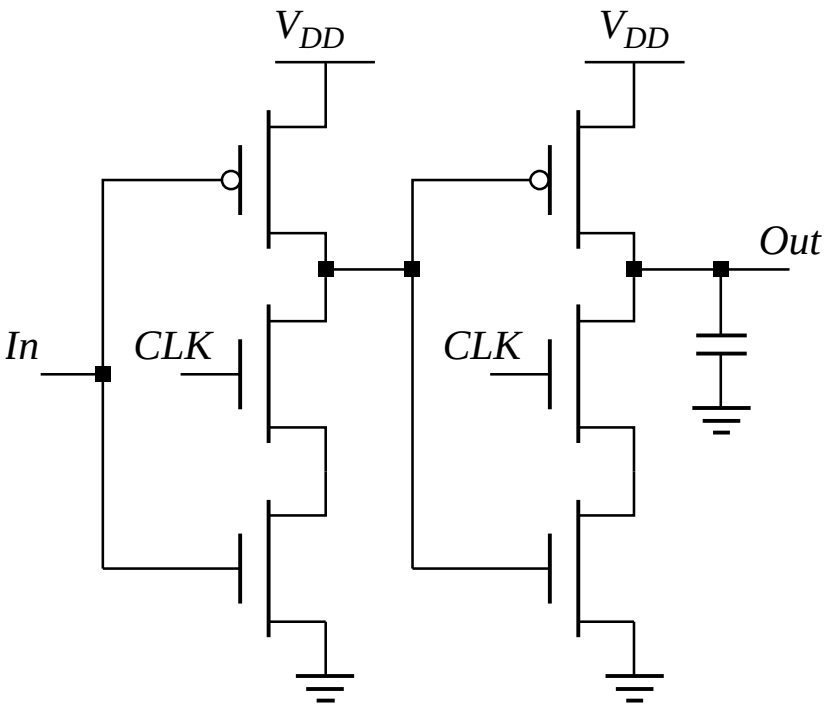

Reference

| Clock Period | Adder | Absolute Value | Logarithm |
|---|---|---|---|
| 1 | $a_1 + b_1$ | | |
| 2 | $a_2 + b_2$ | $\|a_1 + b_1\|$ | |
| 3 | $a_3 + b_3$ | $\|a_2 + b_2\|$ | $\log(\|a_1 + b_1\|)$ |
| 4 | $a_4 + b_4$ | $\|a_3 + b_3\|$ | $\log(\|a_2 + b_2\|)$ |
| 5 | $a_5 + b_5$ | $\|a_4 + b_4\|$ | $\log(\|a_3 + b_3\|)$ |

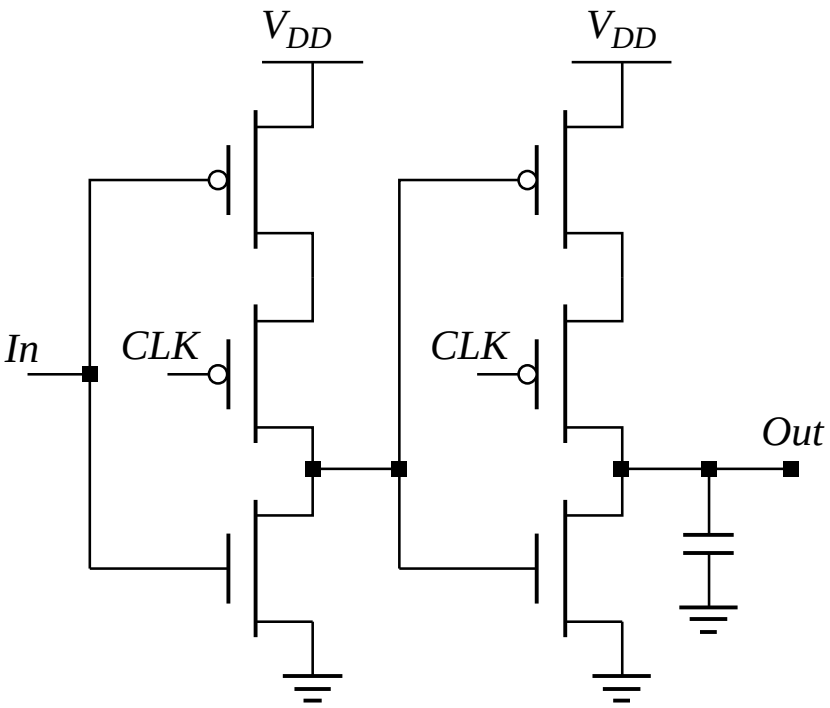



Pipelined

# Other Latches/Registers: TSPC

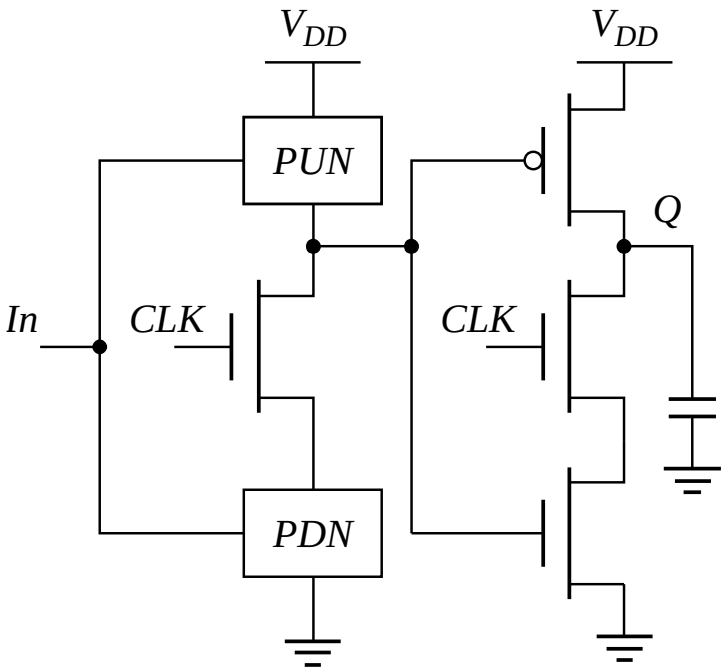



Positive latch
(transparent when CLK= 1)

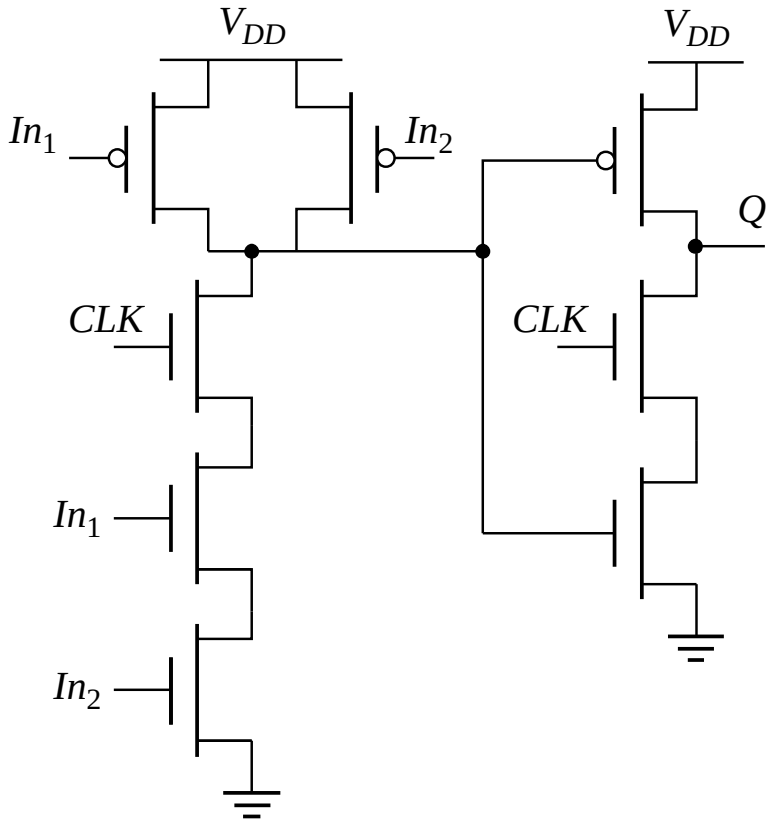



Negative latch
(transparent when CLK= 0)

# Including Logic in TSPC

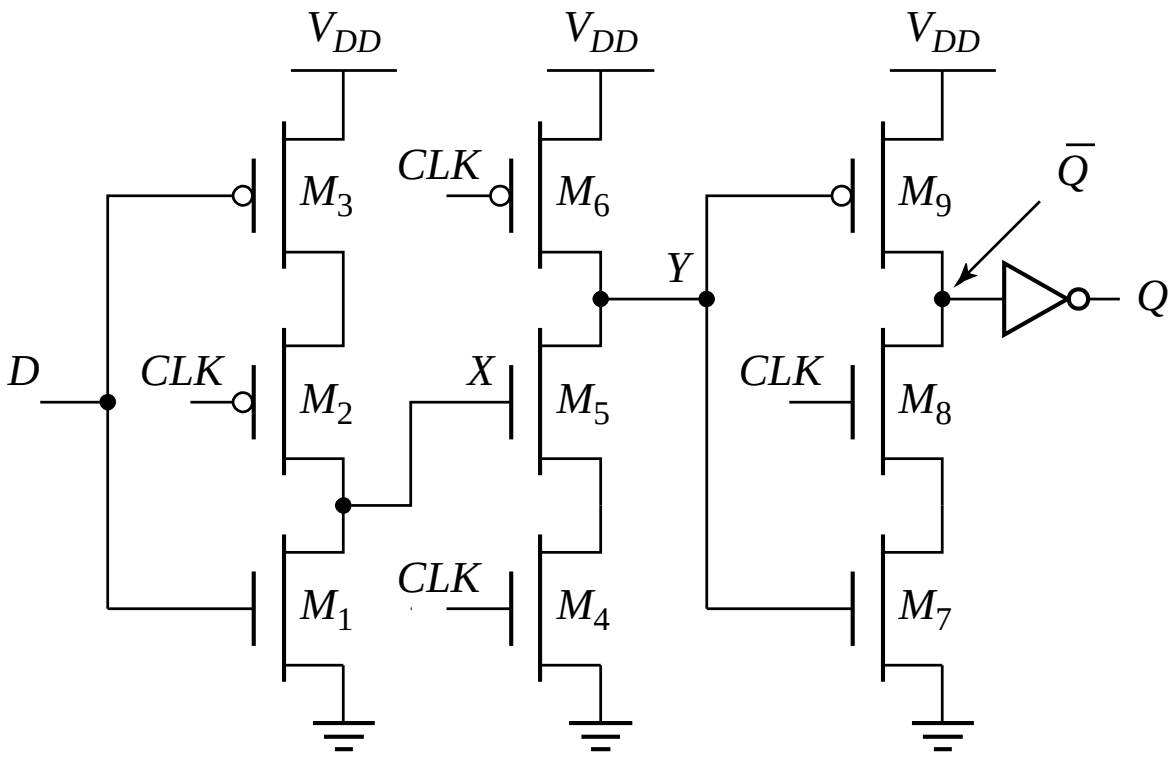



Example: logic inside the latch




AND latch

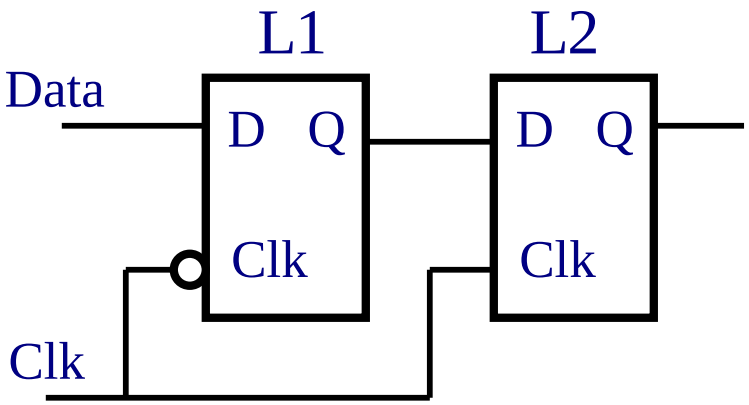
# TSPC Register



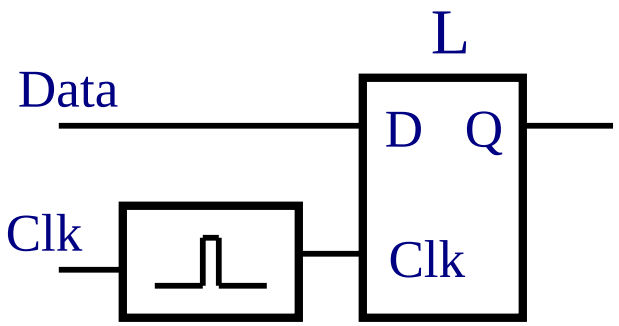
# Pulse-Triggered Latches
# An Alternative Approach

Ways to design an edge-triggered sequential cell:

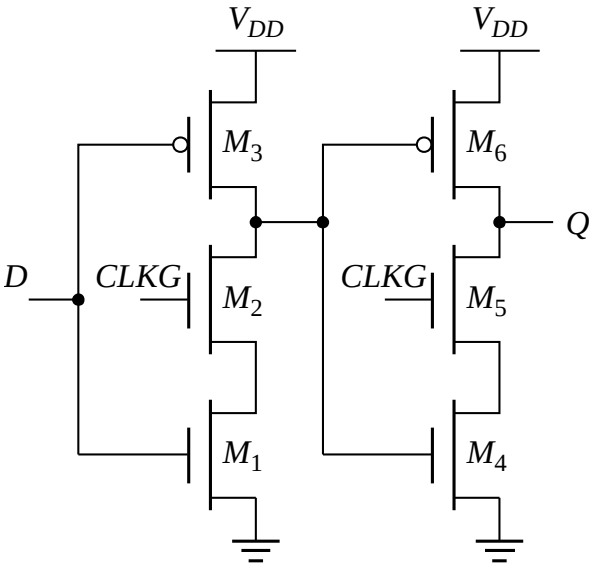
Master-Slave Latches



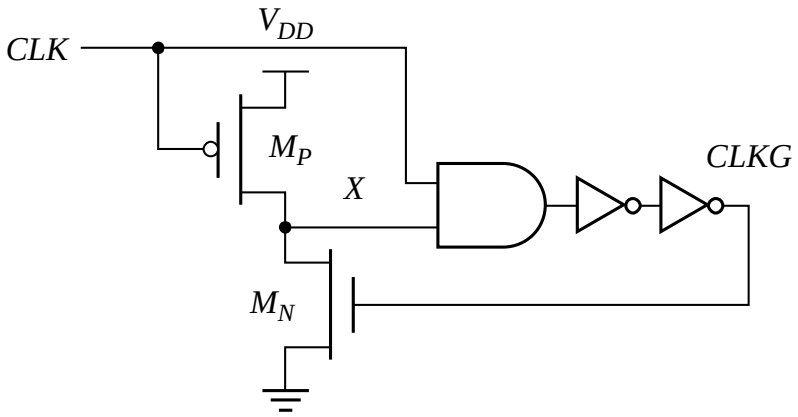

Pulse-Triggered Latch



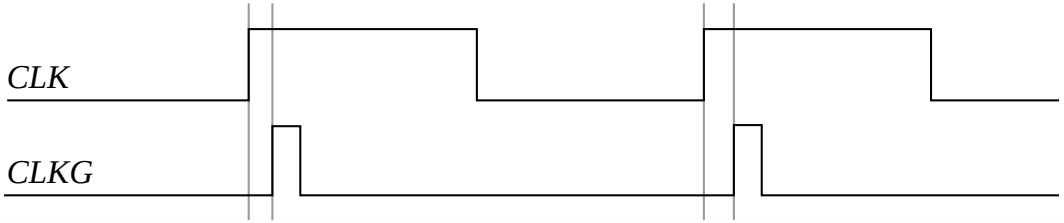
# Pulsed Latches




*(a) register*



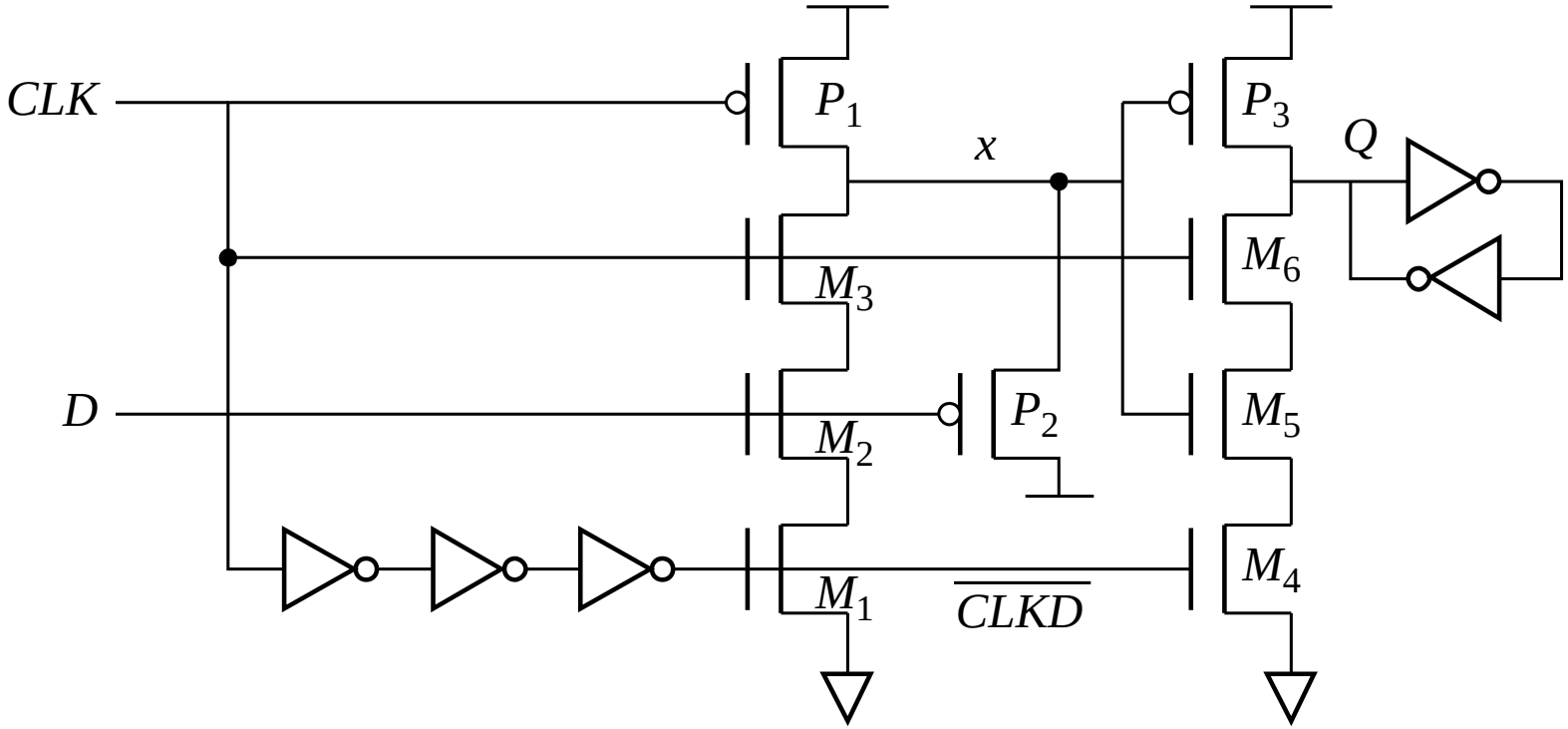

*(b) glitch generation*



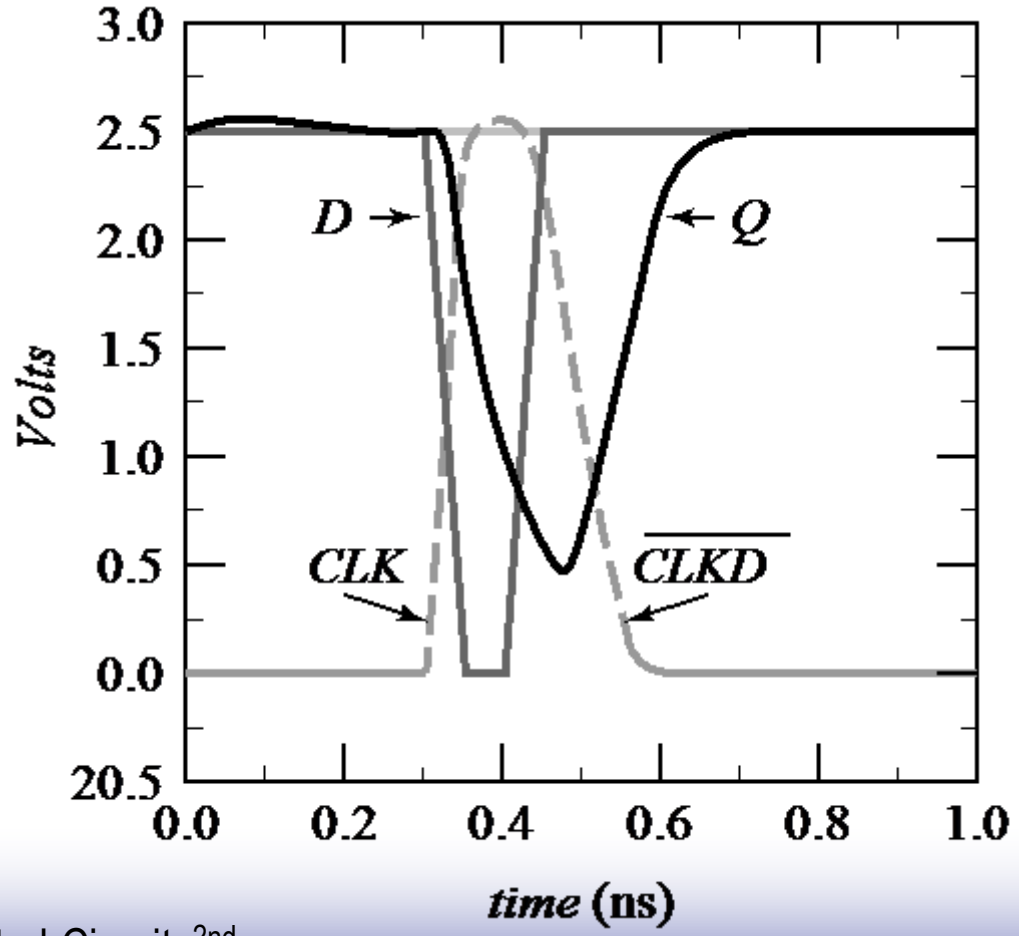

*(c) glitch clock*

# Pulsed Latches

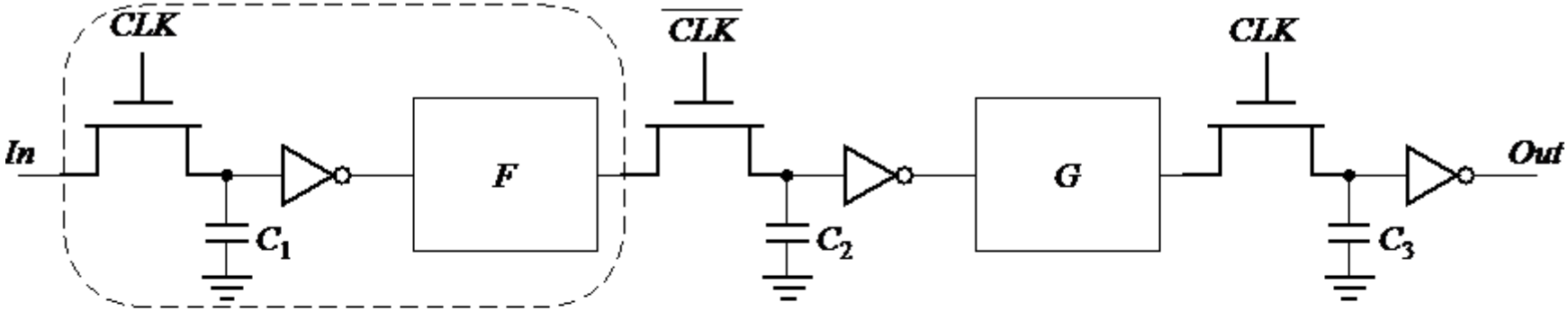
Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7 :

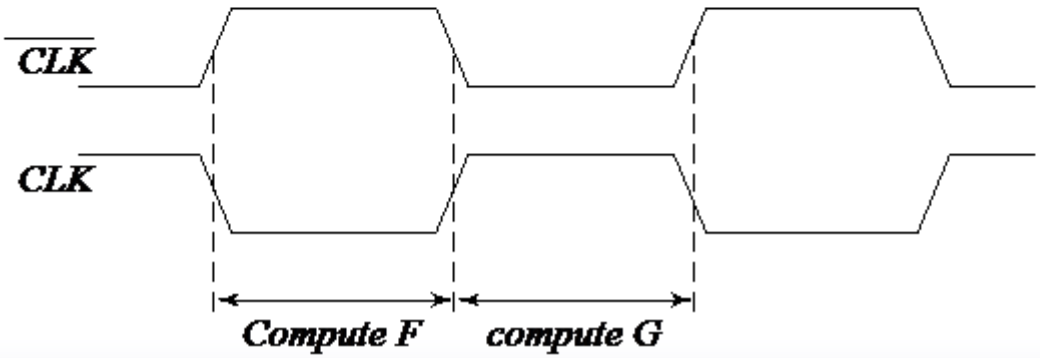


# Hybrid Latch-FF Timing

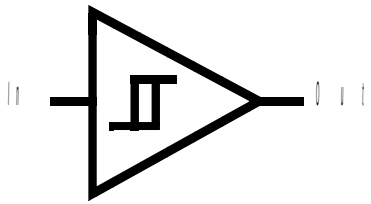


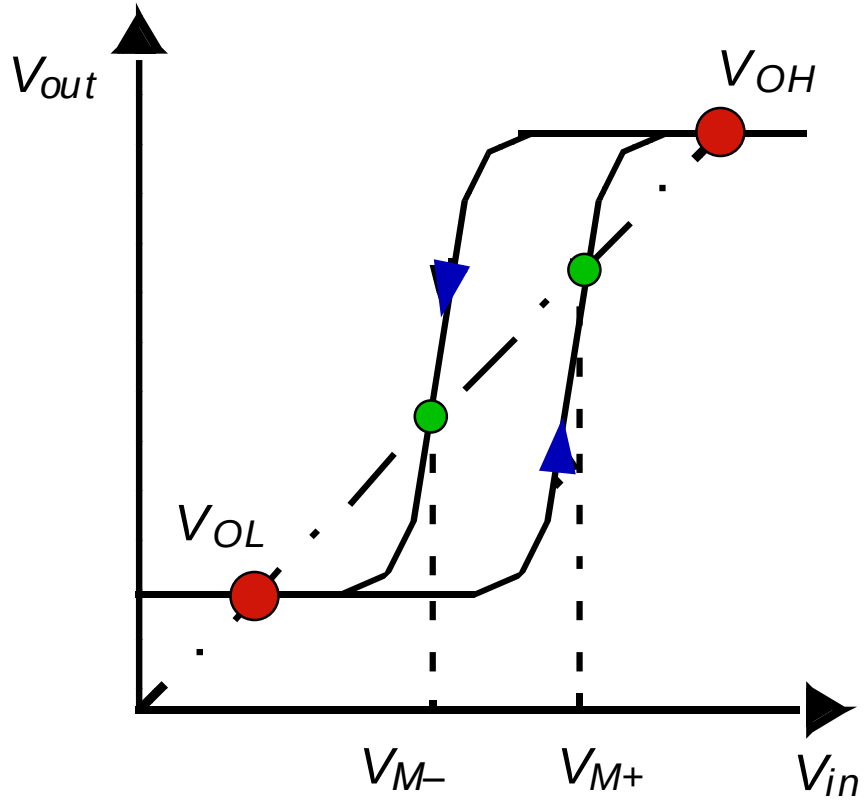
# Latch-Based Pipeline



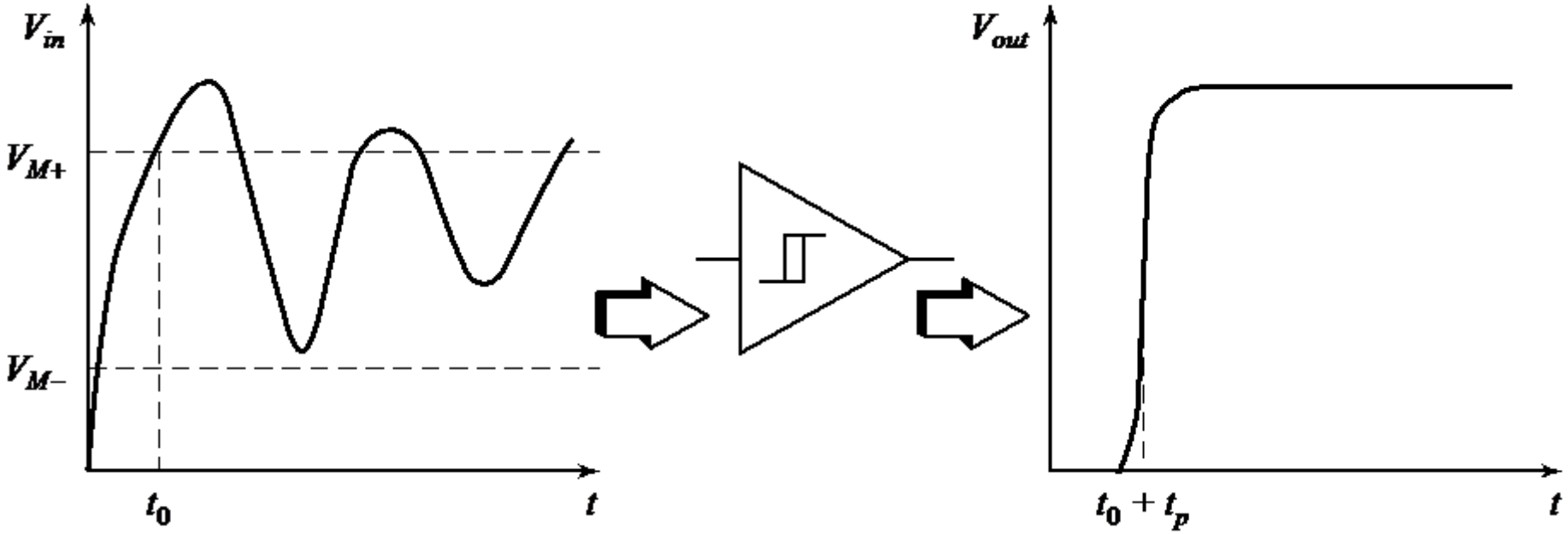
# Non-Bistable Sequential Circuits—Schmitt Trigger



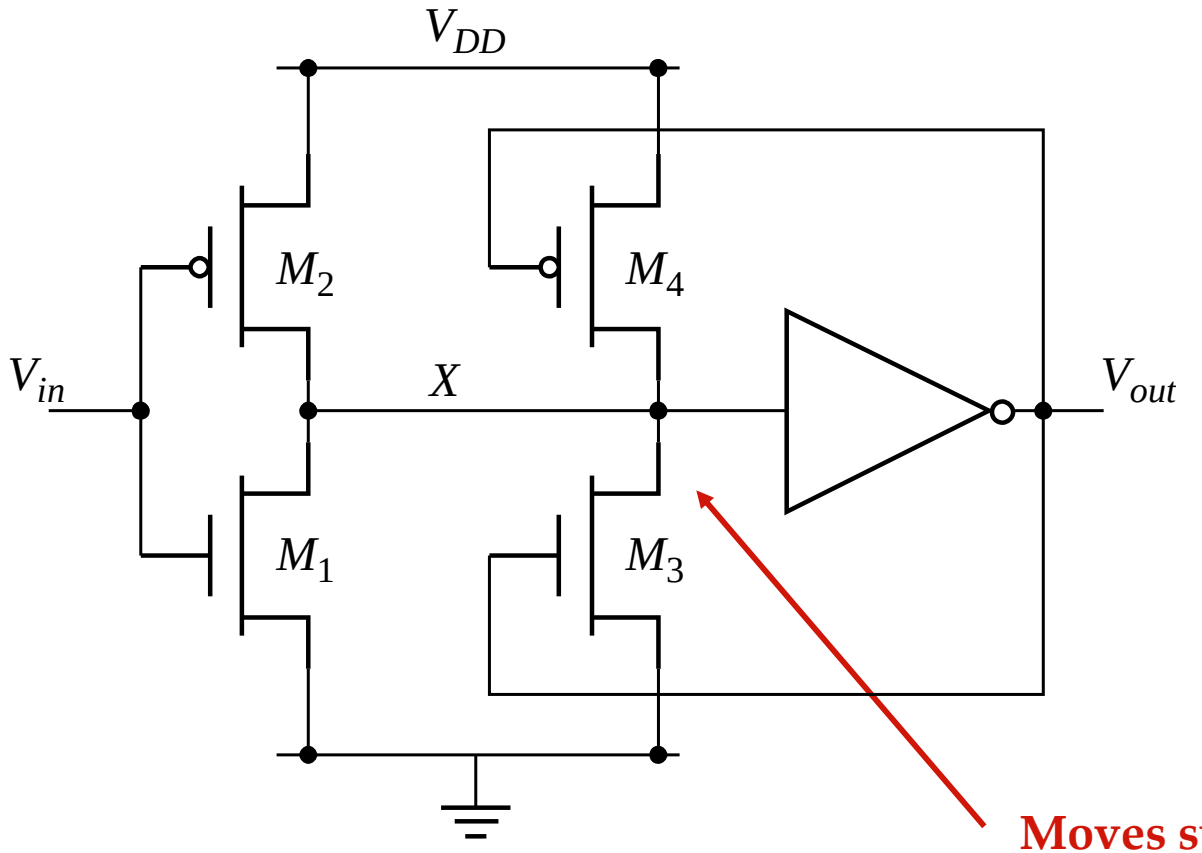



- VTC with hysteresis
- Restores signal slopes

# Noise Suppression using Schmitt Trigger

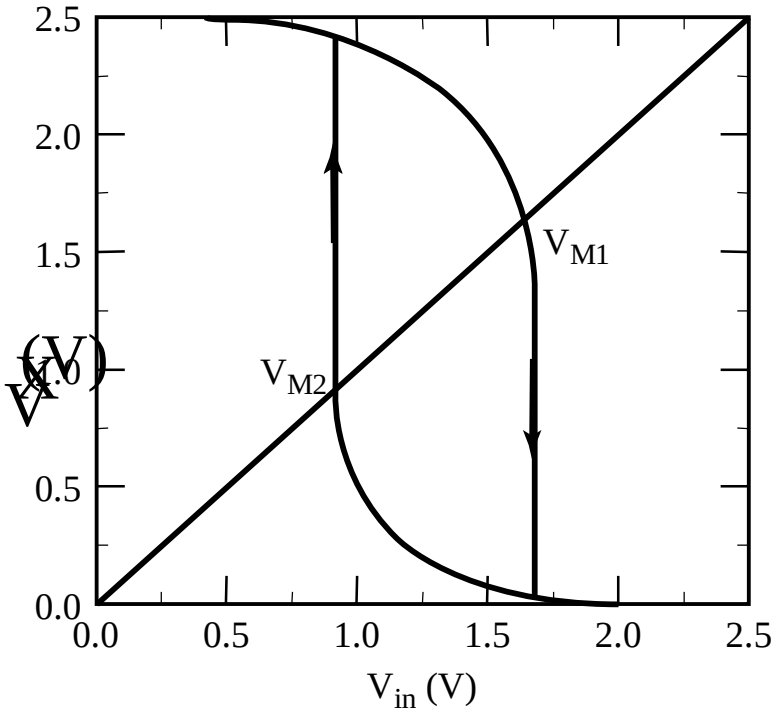


# CMOS Schmitt Trigger

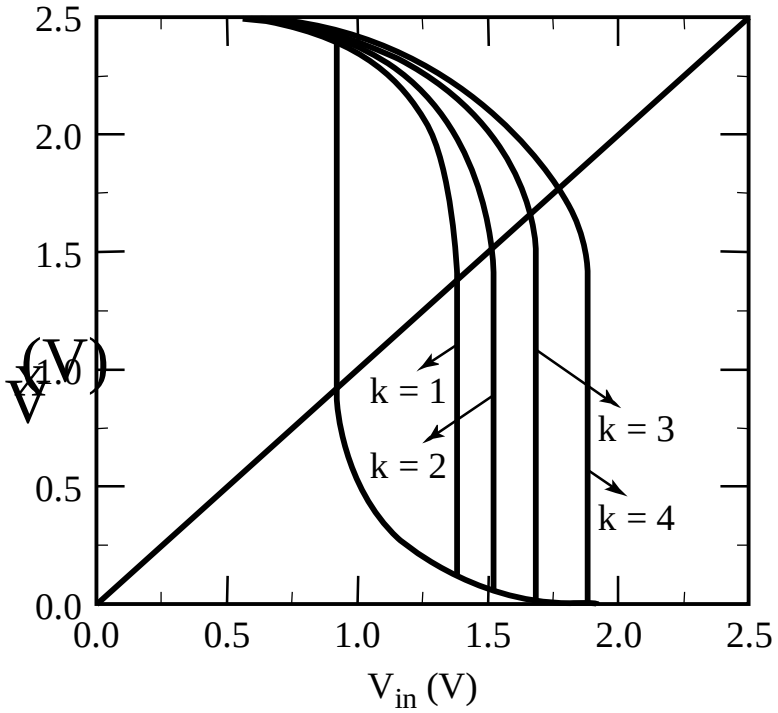



**Moves switching threshold of the first inverter**

# Schmitt Trigger Simulated VTC

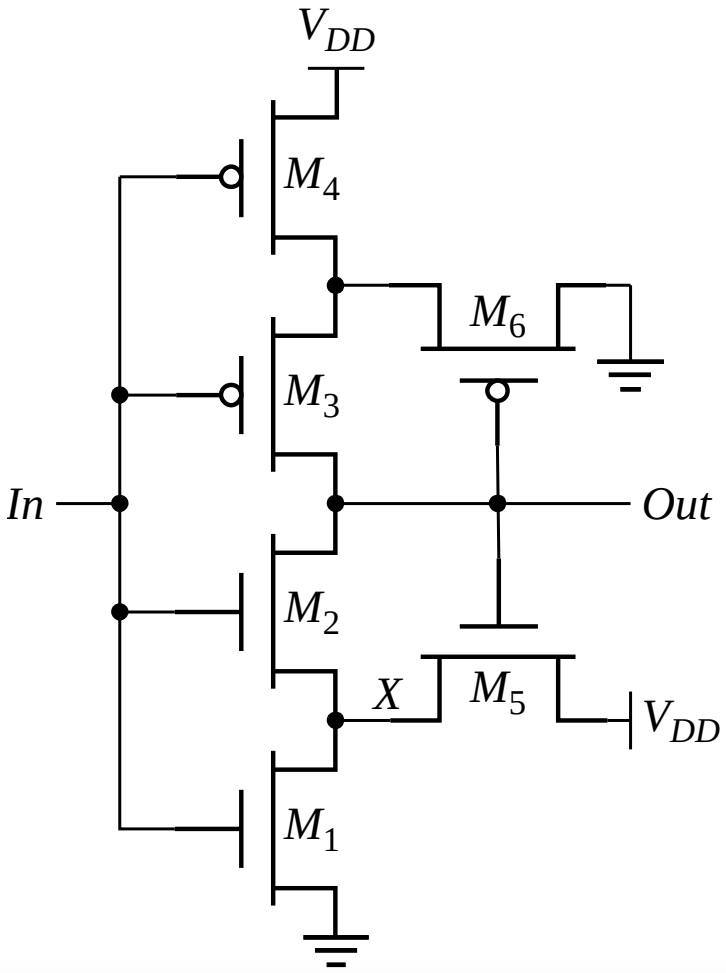



Voltage-transfer characteristics with hysteresis.

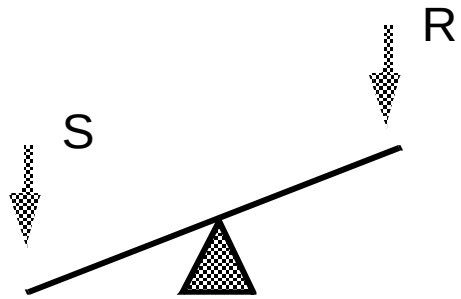



The effect of varying the ratio of the PMOS device $M_4$. The width is k* 0.5$_m$ m.

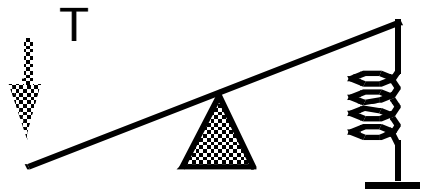
# CMOS Schmitt Trigger (2)



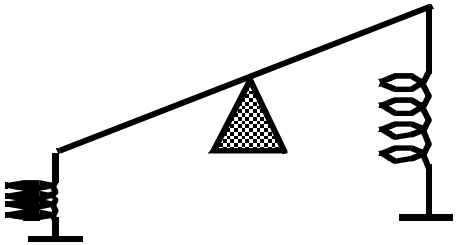
# Multivibrator Circuits




**Bistable Multivibrator**
flip-flop, Schmitt Trigger

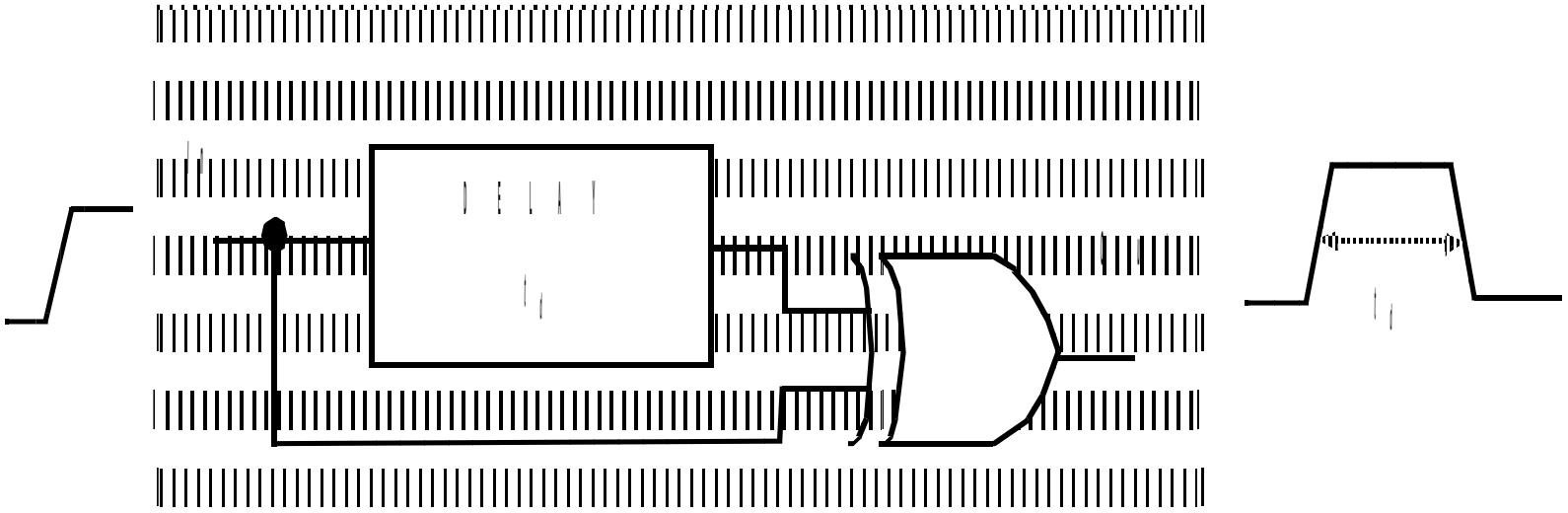



**Monostable Multivibrator**
one-shot

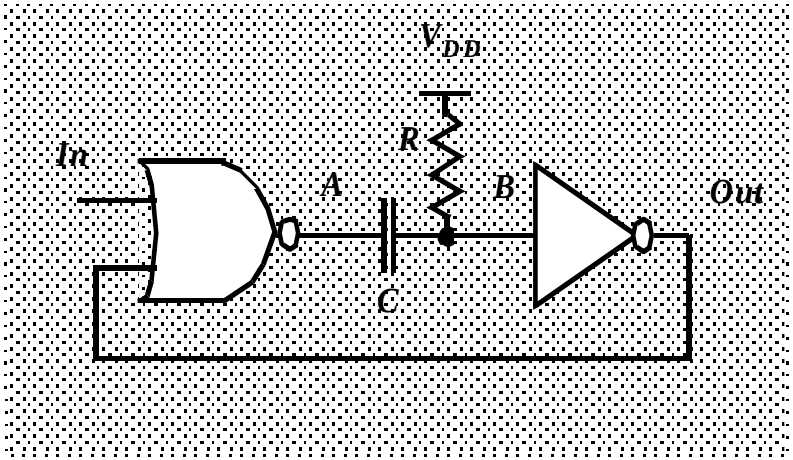


**Astable Multivibrator**
oscillator

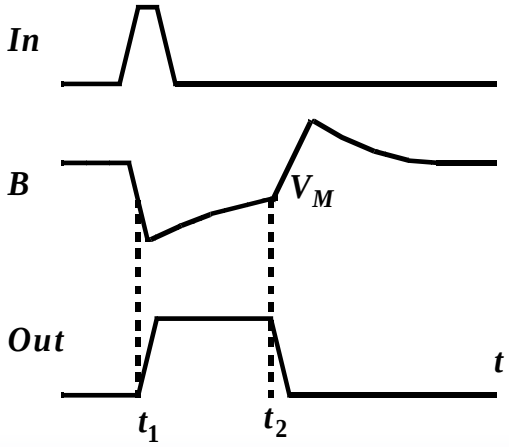
# Transition-Triggered Monostable



# Monostable Trigger (RC-based)

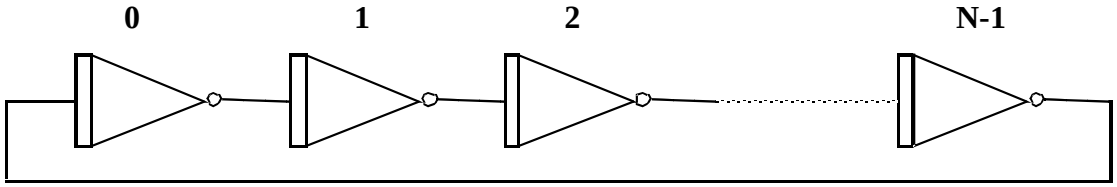



(a) Trigger circuit.

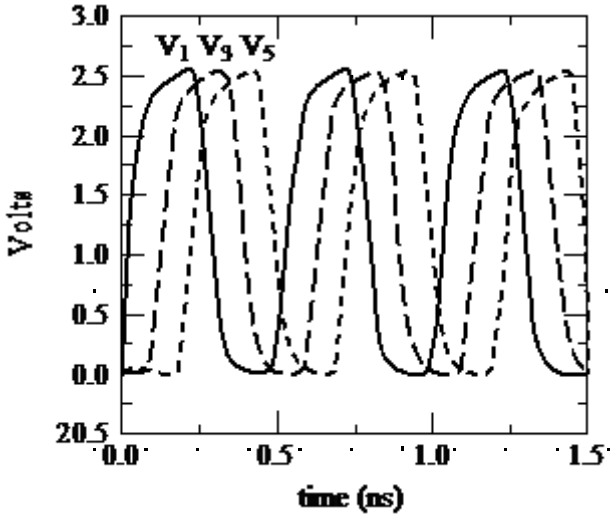



(b) Waveforms.

# Astable Multivibrators (Oscillators)

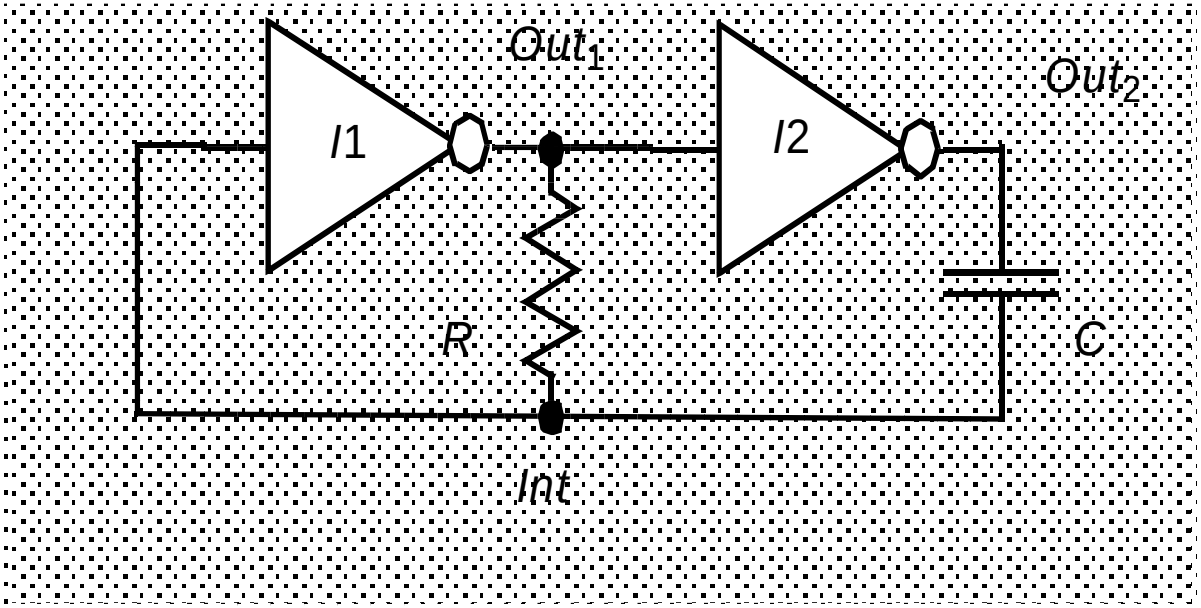



**Ring Oscillator**



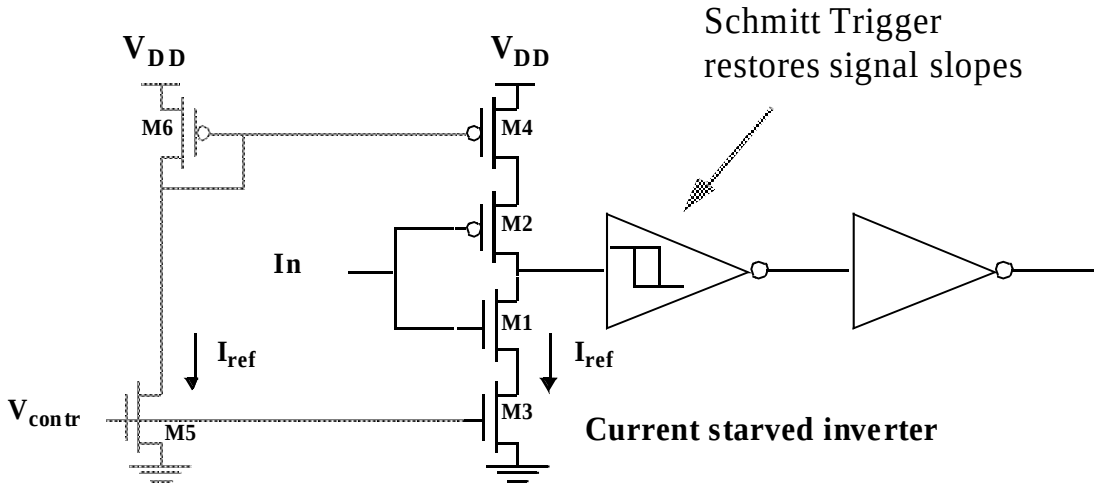

simulated response of 5-stage oscillator

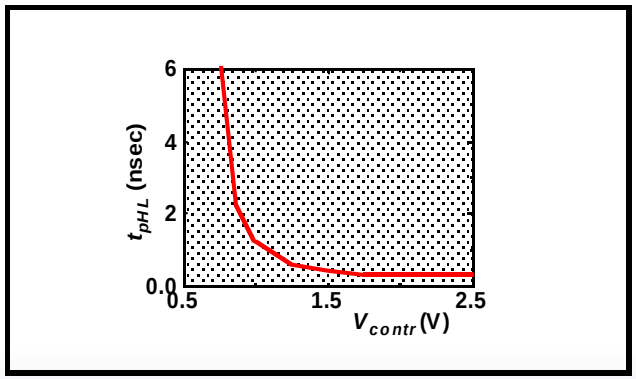
# Relaxation Oscillator




$$T = 2\ (\log 3)\ RC$$

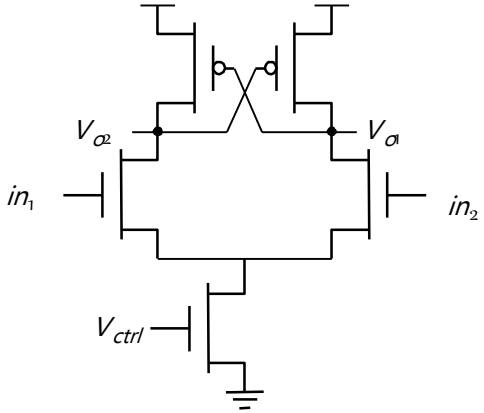
# Voltage Controller Oscillator (VCO)



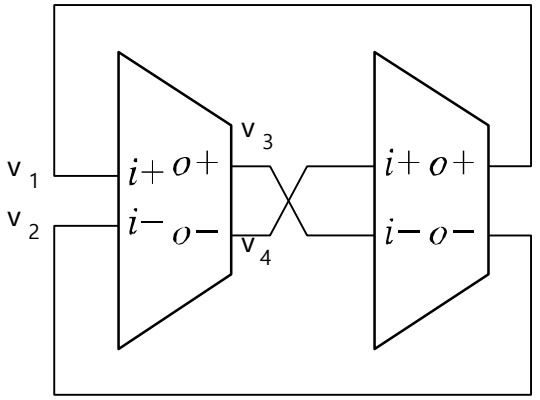




propagation delay as a function of control voltage

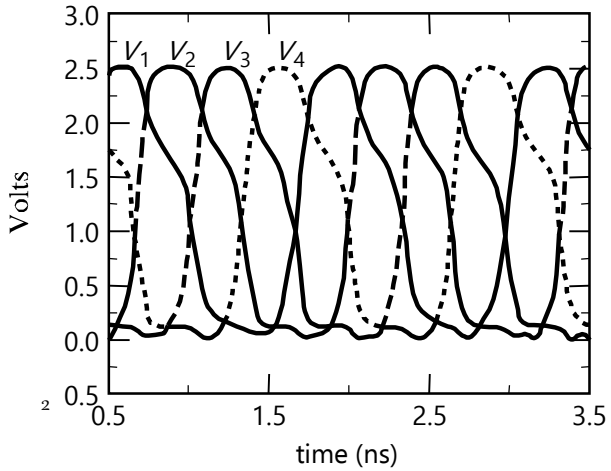
# Differential Delay Element and VCO




delay cell




two stage VCO




simulated waveforms of 2-stage VCO