Labs

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Group 1 - Section 1

Assignment 1

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TO

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Four-bit by Three-bit binary multiplier

Introduction

Multiplication of binary numbers is performed in the same way as multiplication of decimal numbers. The multiplicand is multiplied by each bit of the multiplier, starting from least significant bit. Each such multiplication forms a partial product. Successive partial products are shifted one position to the left. The final product is obtained from the sum of partial products.

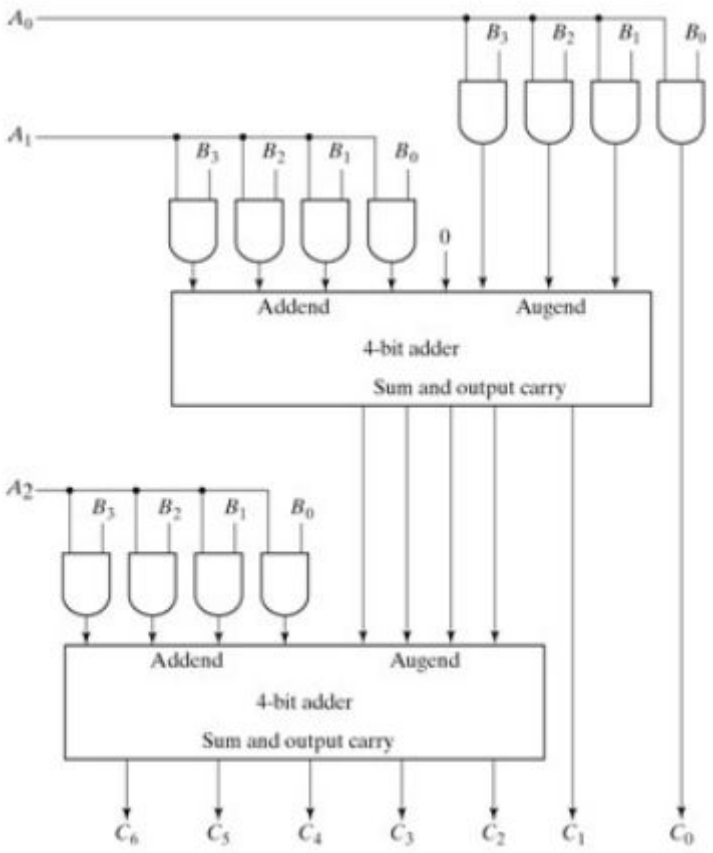
Design Main Idea

A combinational circuit binary multiplier can be constructed as follows, a bit of the multiplier is ANDed with each bit of the multiplicand in as many levels as there are bits in the multiplier. The binary output in each level of AND gates is added with the partial product of the previous level to form a new partial product. The last level produces the product. For J multiplier bits and K multiplicand bits, we need (J*K) AND gates, and (J-1) K-bit adders to produce a product of J+K bits.

Idea Application on 4-bit by 3-bit

Consider a multiplier circuit that multiplies a binary number represented by 4 bits by a number represented by 3 bits. Let the multiplicand be represented by B3B2B1B0 and the multiplier by A2A1A0. Since K = 4 and J = 3, we need 12 AND gates and 2 4-bit adders to produce a product of 7 bits.

Diagram



Logisim Simulation

You can find simulation file here:

https://drive.google.com/file/d/1jaEOktr6zFnbxDXdxvdX70rx2xNyfeK8/view?usp=sharing