A SEMINAR REPORT

on

"WORKING OF A TTL NAND GATE WITH OPEN COLLECTOR OUTPUT AND ALSO MENTION THE DISADVANTAGES OF THIS CONFIGURATION."

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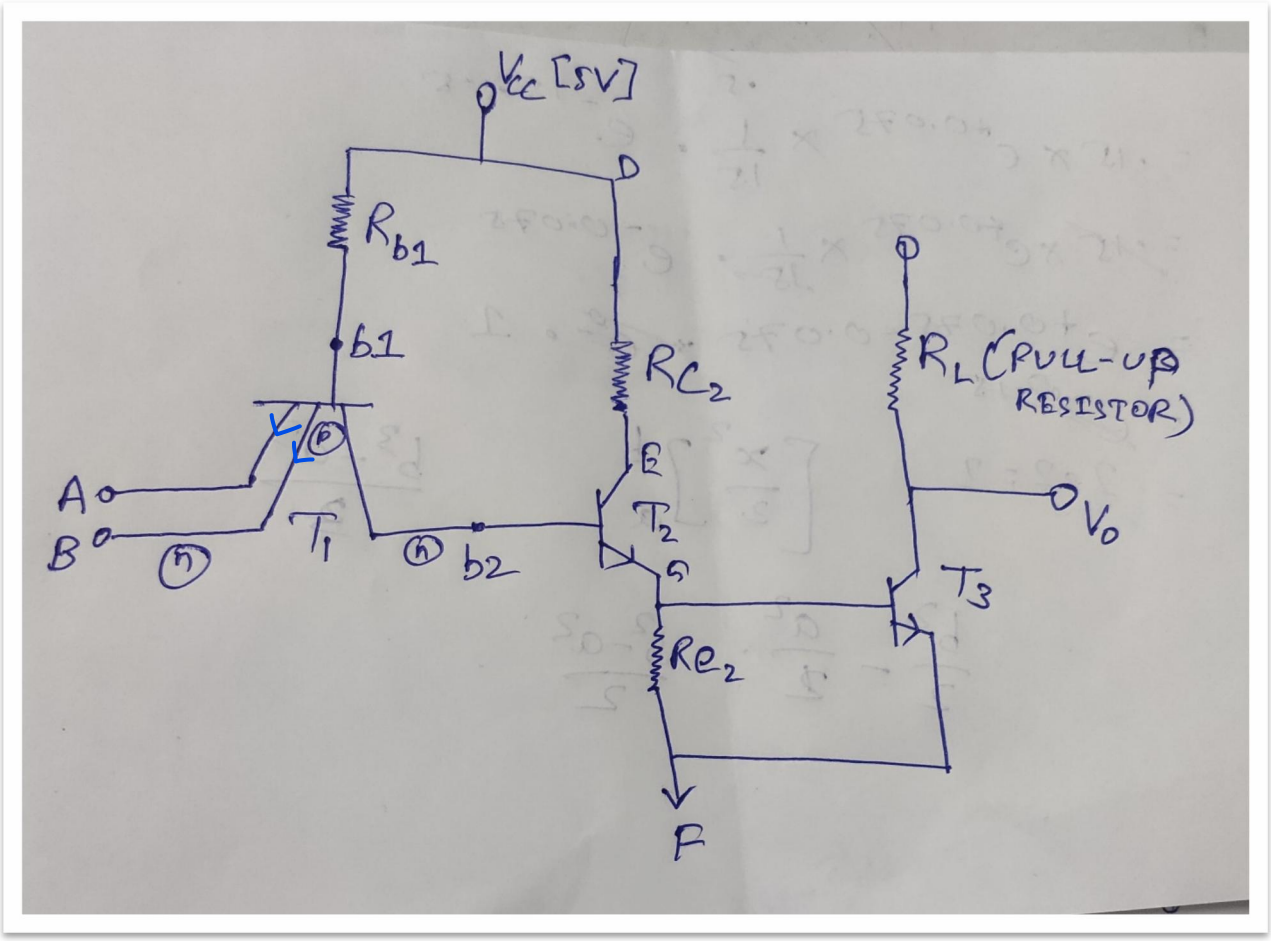
Introduction:-

- Transistor-Transistor Logic belongs to the digital logic family. It consists of transistors at both input and output side, diodes and few resistors.
- There are 3 Types of TTL family.
  TTL logic families are classified based on the types of output configurations. They are
  1. Open collector output
  2. Totem pole or standard output
  3. Three state (or tri state) output

Open-Collector TTL NAND Gate

Block Diagram of Open-Collector TTL NAND Gate:-



Construction of Open-Collector TTL NAND Gate:-

- Multiple-I/P's are given to Emitter Of Transistor T3.
- Transistor T2 is connected in Common Collector Configuration. This makes the Emitter follower as whatever will be the available in base terminal of Transistor T2 , the same will be available in the Emitter terminal of T2 Transistor.
  Ex: If voltage available at Base is 5V then voltage at Emitter will be 5V.
  Conversely, If Voltage at Base is 0V then Voltage at Emitter is 0V.
- Output of Emitter of Transistor T3 is connected to the next transistor T3 and T3 Transistor's Collector is Left Open. That is why it is called as Open Collector TTL NAND Gate
- Since Output/ Collector of Transistor T3 is Open, so there is no change to get the Output at collector side. In order to get the required Output, an External Resistor is Connected called as **Pull-UP Resistor**.
  Note: Pull-up resistor is not included in the IC itself, it is connected externally separately.
- Note: If External O/P Resistor is connected to the supply it is called as **Pull-UP** Resistor and if it is connected to ground then it is called as **Pull-DOWN** Resistor.

Operation of Open-Collector TTL NAND Gate:-

Note: Here Output is taken from Open Collector.

Case-1 (When Any I/P is of Logic 1)

- When anyone input A or B are low, Base Emitter-Junction will come in Forward Bias and Base-Collector Junction will come in Reversed Bias.
- Forward Bias->ON (Pass logic-1)
- Reverse Bias->OFF (Pass logic-0)
- T1 will come in active region. "**b2"** wont get base triggering and T2 will be turned OFF.
- Note: 1.4V is required to Switch ON T2.
- T3 Will be turned OFF since DE and GF will be Open Circuited, Hence no current will pass to T3.
- Now, Output Voltage will be driven by the external network with Vcc and Rl.
  - $\mathbf{V_O=V_{cc}-V_L}$
    $\mathbf{=V_{cc}-IR_L}$

Case-2 (When All the I/P's are set to Logic 0)

- In this Case, Base-Emitter Junction will Operate in Reversed Bias and Base Collector Junction of Transistor T1 will operate in Forward Bias.
- Now b2 will draw supply to T2 and from that Base of T3 logic is supplied and T3 will be turned ON.
- As T3 is ON, our Output Voltage V_o will be V_{CE} i.e 0.2V.
- $V_o=V_{CE}$(Saturation)=0.2 V= Logic 0.
- Note: If both of the Input are 1 then Output is Logic 0.

Output Truth Table of Open-Collector TTL NAND Gate:-

A	B	V_o
0	0	1
0	1	1
1	0	1
1	1	0

Disadvantage of TTL NAND gate with open collector output Configuration :-

1. High Power Consumption.
   Reason: This is because **Pull-UP** resistor in the circuit uses power when Output is pulled to low state. This shows for required functional and when the resistor value is low then the pull-up becomes stronger resulting in high power consumption. Hence Propagation delay of the Pull-UP Resistor is High.
