DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Supplementary Examination – Summer 2022

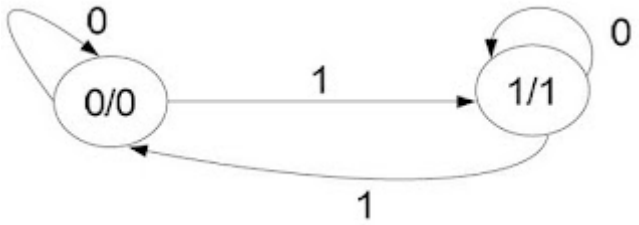
Course: B. Tech. **Branch: E&TC** **Semester: III**

Subject Code & Name: BTETC303 Digital Electronics

Max Marks: 60 **Date:** **Duration: 3 Hr.**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *Use of non-programmable scientific calculators is allowed.*
3. *Assume suitable data wherever necessary and mention it clearly.*

		(Level/CO)	Marks
Q. 1	**Solve Any Two of the following.**		**12**
A)	Simplify following expression using K-Map $f(A,B,C,D) = \Sigma m(1,4,7,12,13,14,15) + d(0,5,8)$	**(2)**	**6**
B)	Implement Binary to Gray code Converter.	**(3)**	**6**
C)	Draw and explain Binary Full Adder. Design the logic diagram for full adder.	**(1)**	**6**
Q.2	**Solve Any Two of the following.**		**12**
A)	Design 3-bit synchronous up counter using JK flip flop.	**(3)**	**6**
B)	Convert D Flip-flop to T flip-flop.	**(2)**	**6**
C)	Draw and explain Universal shift Register.	**(4)**	**6**
Q. 3	**Solve Any One of the following.**		**12**
A)	An FSM is given as in the below diagram. find out  1. What is the output sequence for the given input data sequence 001010110110110111? 2. What is the behaviour of the above Finite state machine? 3. Decide the Flip-flop which can be used by avoiding external logic gates.	**(3)**	**12**
B)	a. Explain Basic design steps with example- State diagram, State table, State reduction, State assignment. b. Explain briefly with the difference between the Mealy model and Moore model.	**(4)**	**12**

Q.4	**Solve Any Two of the following.**		**12**
A)	Compare Characteristics of TTL, CMOS, ECL, RTL, I2L and DCTL logic families.	**(3)**	**6**
B)	Define and explain: i)Fan in and Fan out ii) Noise immunity iii) Propagation Delay	**(1,2)**	**6**
C)	Explain in brief the operation of CMOS NAND Gate with schematic diagram.	**(3)**	**6**
Q. 5	**Solve Any Two of the following.**		**12**
A)	Implement given Boolean functions using PLA, PAL and PROM F1 (A,B,C)= $\Sigma m(0, 2,6,7)$ F2(A,B,C)= $\Sigma m(1, 3,4,5,7)$	**(4)**	**6**
B)	Write VHDL code for Mux 4:1 using dataflow and behavioural architecture style.	**(4)**	**6**
C)	Classify memories RAM and ROM.	**(3)**	**6**
	***** End *****		

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DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Winter End Semester Examination – March 2023

Course: B. Tech. **Semester: III**

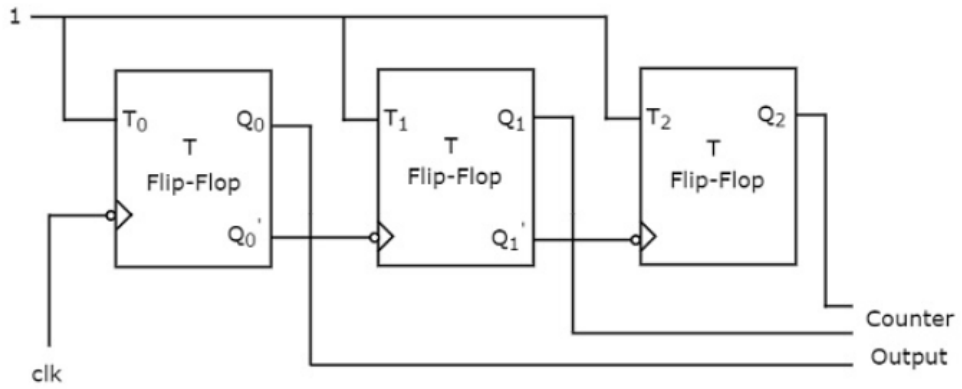
Subject Code & Name: BTETC303 & Digital Electronics

Max Marks: 60 **Date:13/03/2023** **Duration: 3 Hr.**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(Level/CO)	Marks
Q. 1	**Solve Any Two of the following.**		**12**
A)	Convert the following Boolean equation into standard SOP and POS form. F(A,B,C) = AB + AC' + BC	**L2**	**6**
B)	Write VHDL code for full adder using Structural architecture method.	**L3**	**6**
C)	Explain TTL logic in detail.	**L2**	**6**
Q.2	**Solve Any Two of the following.**		**12**
A)	Draw the counter output of the following sequential circuit using clock diagram.	**L2**	**6**

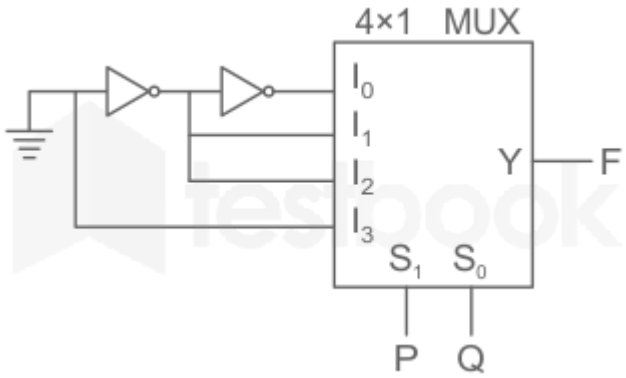


B)	What is the difference between TTL and CMOS and ECL?	**L2**	**6**
C)	Explain General Architecture of CPLD in detail.	**L2**	**6**
Q. 3	**Solve Any Two of the following.**		**12**
A)	Draw the Moore state diagram for One bit Serial adder.	**L2**	**6**
B)	Implement the following Boolean functions using PAL and PROM. $A(X,Y,Z)=\sum m(4,6,7)$, $B(X,Y,Z)=\sum m(2, 4, 5,6)$	**L3**	**6**

C)	Minimise the following function in SOP and POS form using K-Maps: F(A, B, C, D) = m(1, 2, 6, 7, 8, 13, 14, 15) + d(0, 3, 5, 12)	**L3**	**6**

Q.4 Solve Any Two of the following. **12**

A)	Explain the universal shift register operation with diagram.	**L3**	**6**
B)	The logic function is implemented by the multiplexer circuit is ("ground implies a logic 0") find the output of F?	**L3**	**6**



C)	Write VHDL code for 4-bit up counter.	**L3**	**6**

Q. 5 Solve Any Two of the following. **12**

A)	Implement the following function using i) multiplexer 8x1 ii) multiplexer 2x1 F(A,B,C,D) = m(0,1,3,5,7,10,11,14)	**L3**	**6**
B)	Design sequence detector to detect three or more consecutive 1's in string of bits coming through an input lines.	**L3**	**6**
C)	i) What is disadvantage in SR flipflop? ii) What is difference between T flipflop and D flipflop? iii) Write down the next state equation of T flipflop.	**L2**	**6**

***** End *****

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Regular & Supplementary Winter Examination – 2023

Course: B. Tech. Branch: Electronics/Electronics & telecom/Electronics & comm

Semester: III

Subject Code & Name: (BTEXC303/BTETC303) Digital Electronics

Max Marks: 60 **Date:06/01/2024** **Duration: 3 Hrs.**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		Level/(CO)	Marks
Q. 1	**Solve Any Two of the following.**		**12**
A)	Minimize the following Boolean function using K-map F (A, B, C, D) = Σm (0, 1, 2, 3, 8, 9, 11, 14) + d (5, 6,7, 13)	CO1	6
B)	Implement 5:32 decoder using 3:8 decoder	CO2	6
C)	Convert the following Boolean expression given below in both standard SOP and standard POS forms: F = (X +Y') (X+Z)	CO1	6
Q.2	**Solve Any Two of the following.**		**12**
A)	i) On the third clock pulse, a 4-bit Johnson sequence is $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 1$, and $Q_3 = 0$. On the fourth clock pulse, the sequence is _____. ii) Draw the 4-bit Johnson counter using D flip flop.	CO2	6
B)	Explain SR, JK, T, D flip flop in detail & write next state equation.	CO2	6
C)	Design 4 bit serial-in-parallel -out shift register is initially set to 1111. Data 1010 is applied as the input. What will be the output after 3 clock pulses?	CO1	6
Q. 3	**Solve Any Two of the following.**		**12**
A)	Draw the mealy state diagram for sequence detector 1010.	CO4	6
B)	Draw state diagram of JK flip flop?	CO2	6
C)	Design 8:1 MUX using a) 4:1 MUX. Tree b) Only one 2:1 MUX	CO2	6
Q.4	**Solve Any Two of the following.**		**12**
A)	Define the following term a) Propagation delay b) Fanout c) Power Dissipation d) Figure of Merit	CO2	6

B)	Draw the CMOS schematic and stick diagram for NAND gate.	CO3	6
C)	Explain CMOS inverter characteristics using cutoff, active and saturation regions of operations.	CO4	6

Q. 5 Solve Any Two of the following. **12**

A)	Explain General Architecture of FPGA in detail.	CO2	6
B)	Implement the following Boolean function using PAL, PLA F1= ∑ m (3,5,7) and F2 = ∑ m (4,5,7).	CO3	6
C)	Write VHDL code for full adder using structural style.	CO4	6

***** End *****

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Supplementary Examination Summer 2024

Course: B. Tech. Branch : E&TC / Electronics & Comm. / Electronics Engineering Semester : III

Subject Code & Name: BTETC303 / BTEXC303 Digital Electronics

Max Marks: 60 Date: 04/07/2024 Duration: 3 Hr.

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(Level)	Marks
Q. 1	**Solve Any Two of the following.**		**12**
A)	Design a full-adder circuit and provide the truth table, logic diagram, and simplified logic expressions for the sum and carry outputs.	*Level 2*	**6**
B)	Design a BCD-to-7 segment decoder and provide the truth table for each segment output (a, b, c, d, e, f, g).	*Level 1*	**6**
C)	Implement the following functions using Multiplexers. $F(A,B,C,D)= \sum m(0,1,3,4,8,9,15)$	*Level 4*	**6**
Q.2	**Solve Any Two of the following.**		**12**
A)	Simplify the following logic function using a K-map and express the simplified form in both SOP and POS: $F(A,B,C,D) = \sum m(0,2,5,7,8,10,13,15)$	*Level 4*	**6**
B)	What is a clocked SR flip-flop? Explain its operation with the help of a truth table and logic diagram.	*Level 4*	**6**
C)	Describe how a T flip-flop can be derived from a JK flip-flop.	*Level 3*	**6**
Q. 3	**Solve Any Two of the following.**		**12**
A)	What is shift register? Explain its working with the help of a diagram & truth table.	*Level 1*	**6**
B)	Distinguish between Mealy and Moore machines in terms of their design and applications.	*Level 5*	**6**
C)	Design a finite state machine to detect the sequence "1101" using D flip-flops.	*Level 4*	**6**
Q.4	**Solve Any Two of the following.**		**12**
A)	Briefly explain any six characteristics of Digital ICs.	*Level 1*	**6**
B)	Describe the construction and operation of CMOS NAND and NOR gates.	*Level 2*	**6**
C)	Discuss the advantages and disadvantages of using CMOS over TTL in modern digital circuits.	*Level 3*	**6**

Q. 5	**Solve Any Two of the following.**		**12**
A)	Describe the architecture and operation of a Programmable Logic Array (PLA). How does it differ from a PAL?	*Level 2*	**6**
B)	Distinguish between SRAM and DRAM	*Level 3*	**6**
C)	Write a VHDL code for a full adder using structural description.	*Level 2*	**6**

***** End *****