DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Regular & Supplementary Winter Examination-2023

Course: B. Tech. **Branch : AIDS** **Semester : III**

Subject Code & Name: BTAIES304 & Computer Architecture & Operating Systems

Max Marks: 60 **Date: 09/01/2024** **Duration: 3 Hr.**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(Level/CO)	Marks
Q. 1	**Solve Any Two of the following.**		**12**
A)	Explain about address sequencing in control memory with neat diagrams?	L1 CO1	6
B)	What are the basic operations performed by the processor?	L1 CO1	6
C)	Write briefly about computer fundamental system?	L1 CO1	6
Q.2	**Solve Any Two of the following.**		**12**
A)	Explain Contiguous Allocation.	L2 CO2	6
B)	Describe Implementation of Page Table.	L2 CO2	6
C)	Explain Second Chance Page Replacement Algorithm.	L2 CO2	6
Q. 3	**Solve Any Two of the following.**		**12**
A)	Explain role of interrupts in process state transitions.	L3 CO3	6
B)	Describe USB with it's Protocol.	L3/CO3	6
C)	Explain Parallel Processors.	L3/CO3	6
Q.4	**Solve Any Two of the following.**		**12**
A)	Explain operating system structure.	L4 CO4	6
B)	Describe Micro Kernel System Structure with it's modules.	L4 CO4	6
C)	Compare between Process and Thread.	L4/CO4	6
Q. 5	**Solve Any Two of the following.**		**12**
A)	Describe Dining-Philosophers Problem.	L5 CO5	6
B)	Explain Monitor Implementations using Semaphores.	L5 CO5	6
C)	Write a note on Banker's Algorithm.	L5 CO5	6

*** End ***

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE – RAIGAD -402 103

Winter Semester Examination – Dec - 2019

Branch: B.Tech. (Computer Engineering)	**Sem: III**
Subject with Subject Code: Computer Architecture & Organization[BTCOC304]	**Marks:60**
Date:- 17-12-2019	**Time: 3 Hrs**

Instructions to the Students:

1.Each question carries 12 marks.

2. Attempt **any five** questions of the following.

3. Illustrate your answers with neat sketches, diagram etc., wherever necessary.

4. If some part or parameter is noticed to be missing, you may appropriately assume it and should mention it clearly.

Q.1	**Solve any following questions.**	
(A)	What, in general terms, is the distinction between computer organization and computer architecture?	**06**
(B)	Explain the computer: the top level structure with structural component with neat sketch diagram.	**06**
Q. 2	**Attempt the following questions.**	
(A)	Enlist and explain any two addressing modes. Given the following memory values and a one-address machine with an accumulator, what values do the following instructions load into the accumulator? • Word 20 contains 40. • Word 30 contains 50. • Word 40 contains 60 • Word 50 contains 70. a. LOAD IMMEDIATE 20 b. LOAD DIRECT 20 c. LOAD INDIRECT 20 d. LOAD IMMEDIATE 30	**06**
(B)		
I.	Convert the following instruction into Accumulator based CPU, Register based CPU. Instruction:(A*B)-(R+Z)/T	**03**
II.	Is RISC better than CISC? Illustrate your answer with example of processor.	**03**
Q.3	**Attempt the following questions.**	
(A)	Given x = 1011 and y = 1001 in twos complement notation (i.e., x = -5, y = - 7), draw and compute the product p = x * y with Booth's algorithm flowchart.	**06**
(B)	Show how the following floating-point additions are performed (where significants are	**06**

	truncated to 4 decimal digits). Show the results in normalized form. a. $5.566 \times 10^{2} \times 7.777 \times 10^{3}$ b. $3.344 \times 10^{1} + 8.877 \times 10^{-2}$ c. $6.21 \times 10^{5} \div 8.877 \times 10^{1}$	
Q.4	**Attempt the following questions.**	
(A)	What are the differences among direct mapping, associative mapping, and set-associative mapping?A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.	**06**
(B)	Elaborate the concept of SRAM and DRAM memory with typical memory cell structure.	**06**
Q.5	**Attempt the following questions.**	
(A)	What is the overall function of a processor's control unit?A stack is implemented.show the sequence of micro-operations for a. popping b. pushing the stack PUSH 10 PUSH 70 PUSH 8 ADD PUSH 20 SUB MUL	**06**
(B)	What is the difference between a hardwired implementation and a microprogrammed implementation of a control unit?	**06**
Q.6	**Attempt any two questions.**	
(A)	In virtually all systems that include DMA modules, DMA access to main memory is given priority than CPU access to main memory. Why?	**06**
(B)	What is the meaning of each of the four states in the MESI protocol? Can you foresee any problem with the write-once cache approach on bus-based multiprocessors? If so, suggest a solution.	**06**
(c)	How does instruction pipelining enhance system performance? Elaborate your answer using RISC instruction stages.	**06**

**********End of Paper**********

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

End Semester Examination – Summer 2019

Course: B. Tech in Computer Engineering **Sem: III**

Subject Name: Computer Architecture and Organization

Subject Code: BTCOC304

Max Marks: 60 **Date: 31/05/19** **Duration: 3 Hr.**

Instructions to the Students:

1. *Solve **ANY FIVE** questions out of the following.*
2. *The level question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(Level/CO)	Marks
Q. 1	**Solve Any Four of the following.**		**12**
A)	Differentiate between Big and Little endian. Why are transfer of control instructions needed?	Informative/Easy	
B)	A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. (i) How many selection inputs are there in each multiplier? (ii) What sizes of multiplexers are needed? (iii) How many multiplexers are there in the bus?	Synthesis/Logical	
C)	Enlist the design issues of computer organisation with explanation. For move and add instructions, the format is load location1,location 2 and add R1, R0. Is it possible to use fewer instructions to accomplish the task? If yes, then elaborate your answer and give the proper sequence.	Application/ Average Level	
D)	Why a format that allows multiple words to be use for a single instruction would be needed to represent an instruction set? Why there is need of computer organization?	Understanding /Easy	
E)	Represent the decimal values 5,-2,14,-10 as signed seven bit numbers in the following binary formats. a) Signed and Magnitude b) 1's complement c) 2's complement.	Informative/ Average	
Q.2	**Solve Any Four of the following.**		**12**
A)	Why is RISC architecture better suited for pipeline processing than CISC? Which architecture is more common in mobile phones RISC or CISC?	Info/Average	
B)	What is the purpose of integer arithmetic and describe the role of overflow in addition and subtraction operations of integer arithmetic? Calculate (72530-48960) using tens complement arithmetic. Assume rules similar to those for twos complement arithmetic.	Understanding	
C)	A memory byte location contains the pattern 00101100. What does this pattern represents when interpreted as a binary number? What does it represent as ASCII code? How two's complement relates with subtraction	Understanding/	

	rule? Write proper reason and example.	Hard	
D)	Discuss the need of variable length instruction format. How many bits wide memory address have to be if the computer had 16 MB of memory?	Tough Level/ Synthesis	
E)	How do you improve the cache performance? How many check-bits are needed if the hamming error correction code is used to detect single bit errors in a 2048 bit data word?	Application	
Q. 3	**Solve the following.**		**12**
A)	Discuss difference between dynamic and static RAM in terms of characteristics such as speed,size and cost. What is the basic advantage of using interrupt initiated data transfer over transfer under program control without an interrupt?	Understanding	
B)	How is the syndrome for the Hamming code interpreted? Suppose that the processor has access to two levels of memory. Level 1 contains 1000 words and has an access time of 0.01 microseconds; level 2 contains 1,00,000 words and has an access time of 0.1 microseconds. Assume that if a word to be accessed in level 1, then the processor accesses it directly. If it is in level 2, then the word is first transferred to level 1 and then accessed by the processor. Suppose 95% of the memory accesses are found in the cache. Then, what should be the average time to access a word?	Info/Average	
Q.4	**Solve Any four of the following.**		**12**
A)	Differentiate virtual with main memory?	Info	
B)	Consider a cache with a line size of 32 bytes and a main memory that requires 30 ns to transfer a 4 byte word. For any line that is written at least ones before being swapped out of the cache, what is the average number of times that the line must be written before being swapped out for a write-back cache to be more efficient than a write-through cache?	Understanding	
C)	Give the difference between sequential, random and direct access.	Info	
D)	A set associative cache consists of 64 lines or slots divided into four line sets. Main memory contains 8K blocks of 64 words each. Show the format of main memory addresses.	Application	
E)	How the memory is organized?	Info	
Q. 5	Attempt any four of the following.		**12**
A)	When a DMA module takes control of a bus and while it retains control of the bus, what does the processor do?	Understanding	
B)	What is the difference between isolated I/O and memory mapped I/O? Why does DMA have priority over the CPU when both request a memory transfer?	Info	
C)	When a device interrupt occurs, how does the processor determine which device issued the interrupt?	Average/ Understanding	
D)	How three techniques have defined and differentiated for performing Input/Output?	Info	
E)	What is parity bit? How does SDRAM differ from ordinary DRAM?	Info/Synthesis	

Q. 6 Attempt the following. **12**

A) Explain the difference between hardwired control and micro-programmed control. What are different stages of a pipe?

Informative/ Logical/ Reasoning based

B) Why does an assembly line in a manufacturing plant refer to as pipe-lining?Discuss the need of instruction pipe-lining.

Reasoning/Info

C) Many pipelined processors use four to six stages. Others divide instruction execution into smaller steps and use more pipeline stages and a faster clock.
Considering the above scenario, for fast operations what would you suggest in terms of pipeline stages? How we relate instructions and micro-operations? What is the overall function of a processor's control unit?

Application/ Understanding

END

DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE – RAIGAD -402 103
Semester Examination – December - 2018

Branch: Computer Science and Engineering **Sem.:- I**
Subject with Subject Code:- Computer Architecture & Organization(BTCOC304) **Marks: 60**
Date:-7/12/2018 **Time:- 3 Hr.**

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Instructions to the Students

1. Each question carries 12 marks.
2. Attempt **any five** questions of the following.
3. Illustrate your answers with neat sketches, diagram etc., wherever necessary.
4. If some part or parameter is noticed to be missing, you may appropriately assume it and should mention it clearly

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(Marks)

Q.1. a) Describe the structural overview of computer. (5)
b) Define stored program concept and Explain Von Neumann's Architecture with diagram. (7)

Q.2. a) List assembler directives? Assuming any assembler, give the necessary directives required for any program. (5)
b) Explain in detail different types of addressing modes. (7)

Q.3. a) Convert $(100.125)_{10}$ in IEEE-754 single precision floating point representation. (5)
b) Sketch and explain flowchart for multiplication of floating point numbers. (7)

Q.4. a) Encode the data 1101 in even parity by using Hamming Code. (5)
b) Elaborate various types of ROM: Magnetic as well as optical (7)

Q.5. a) Discuss Micro operations to execute an instruction MOV R1,R2. (5)
b) Explain Wilki's design of Micro programmed Control Unit. (7)

Q.6. a) Explain Instruction Pipelining. (5)
b) Discuss Interrupt Driven I/O. Compare it with Programmed I/O and explain types of Interrupts (7)
