23EC202	DIGITAL SYSTEM DESIGN	3/0/0/3

Nature of Course	:G (Theory & Analytical)

Course Objectives:

1	To introduce the principles of Canonical forms to minimize the logic expression
2	To enable the students to understand the operation of various combinational and sequential logic circuits.
3	To allow students to analyze synchronous sequential circuits.
4	To enable the students to construct PLD's and their roles in digital systems
5	To enable the students to write verilog code for combinational logical circuits.

Course Outcomes:
Upon completion of the course, students shall have ability to

C202.1	Demonstrate knowledge on canonical forms and their realization using logic gates	[U]
C202.2	Applying K- Map and Tabulation method to minimize the Boolean functions.	[AP]
C202.3	Understand various combinational logic and sequential logic circuits and their implementation	[AP]
C202.4	Apply synchronous sequential logic for reducing state reduction.	[AP]
C202.5	Understanding Programmable logic devices and applying for logical function implementation.	[AP]
C202.6	Apply verilog code for realization of combinational logical circuits.	[AP]

Course Contents:

Canonical Forms and Minimization **15**

Minterms, Maxterms, Complements, Implementation using universal logic gates, Minimizing functions using Karnaugh maps – 2,3 & 4 Variables, Minimization using Quine McClusky method – 4 Variables.

Combinational and Sequential logic circuits: **15**

Adders and Subtractors, Multiplexer, Demultiplexer, Encoders, Decoders, Two Bit Magnitude comparator, Carry Look-ahead adder, Code converters, – Binary to Gray, BCD to Excess-3 Parity generator and Checker. **Sequential logic circuits:** Latches and flip flops, Realization of one flip flop using other flip flops, Asynchronous Up counter and Synchronous counters, Shift registers –SISO,SIPO,PISO,PIPO, Application of Shift registers. Case Study: DTMF Decoder.

Synchronous Sequential logic: **15**

Analysis of Synchronous Sequential Circuits, Sequence generator, State transition diagrams and state transition tables. PLD's - PLA, PAL, Modelling basic combinational circuits using Verilog**.**

Total Hours:	**45**

Text Books:

1	M. Morris Mano, Michael D.Ciletti., "Digital Design",6th Edition, Pearson education, 2018
2	Donald D. Givone, "Digital principles and Design", 2004, McGraw Hill Education India Private Ltd., 29th Reprint, 2018
3	Samir Palnitkar,"Verilog HDL: A Guide to Digital Design and Synthesis" Prentice Hall, Second Edition, 2018

Reference Books:

1	J. F. Wakerly, "Digital Design - principles and practices", 4th Edition, Pearson Education, 2008.
2	Thomas L. Floyd, Digital Fundamentals, 10th Edition, Pearson Education, New

	Delhi, 2017
3	John.M Yarbrough, “Digital Logic Applications and Design”, Thomson Learning, 2006.
Web References:	
1	https://www.tutorialspoint.com/digital_circuits/digital_circuits_useful_resources.htm
2	http://www.technologystudent.com/elec1/dig1.htm
3	*https://www.electronicsforu.com/technology-trends/learn-electronics/digital-electronics-basics*
4	*https://www.electrical4u.com/digital-electronics/*
Online Resources:	
1	https://nesoacademy.org/ec/05-digital-electronics
2	https://www.electronics-tutorials.com/basics/digital-basics.htm
3	https://www.geeksforgeeks.org/digital-electronics-logic-design-tutorials/
4	https://www.tutorialandexample.com/digital-electronics-tutorial

Continuous Assessment				End Semester Examination	Total
Formative Assessment	**Summative Assessment**	**Total**	**Total Continuous Assessment**		
80	**120**	**200**	**40**	**60**	**100**

Assessment Methods & Levels (based on Blooms’ Taxonomy)			
Formative Assessment based on Capstone Model			
Course Outcome	**Bloom’s Level**	**Assessment Component (Choose and map components from the list - Quiz, Assignment, Case Study, Seminar, Group Assignment)**	**FA (16%) [80 Marks]**
C202.1	Understand	Quiz	20
C202.2, C202.3	Apply	Assignment	20
C202.4, C202.5	Apply	Assignment	20
C202.6	Apply	Simulation using Logisim	20

Assessment based on Summative and End Semester Examination			
Bloom’s Level	**Summative Assessment [120 Marks]**		**End Semester Examination (60%) [100 Marks]**
	CIA1 : [60 Marks]	**CIA2 : [60 Marks]**	
Remember	20	10	10
Understand	40	40	40
Apply	40	40	30
Analyse		10	20
Evaluate			
Create			

Assessment based on Continuous and End Semester Examination						
Continuous Assessment (40%) [200 Marks]						End Semester Examination (60%) [100 Marks]
CA 1 : 100 Marks			CA 2 : 100 Marks			
SA 1 (60 Marks)	FA 1 (40 Marks)		SA 2 (60 Marks)	FA 2 (40 Marks)		
	Component - I (20 Marks)	Component - II (20 Marks)		Component - I (20 Marks)	Component - II (20 Marks)	

Course Articulation Matrix													
CO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PSO 1	PSO 2
1	3	2	1	1	-	-	-	1	-	-	-	2	-
2	3	2	1	1	-	-	-	-	-	-	-	2	-
3	3	2	1	1	-	-	-	-	-	-	-	2	-
4	3	2	2	1	-	-	-	-	-	-	-	2	-
5	3	2	2	1	-	-	-	-	-	-	-	2	-
6	3	2	2	1	-	-	-	-	-	-	-	2	-
1	Reasonably agreed				2	Moderately agreed			3	Strongly agreed			