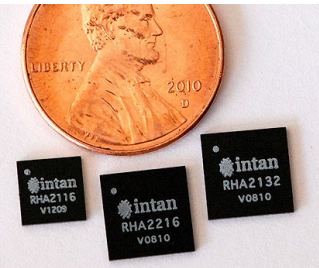
intan TECHNOLOGIES, LLC

RHA2116
RHA2216
RHA2132



Fully Integrated Multi-Channel Biopotential Amplifier Arrays

20 August 2010; updated 30 July 2012

Features

- Fully integrated 46 dB (200 V/V) amplifier array; no off-chip capacitors required for amplifiers
- Low input-referred noise: 2 μV_{rms}
- Low power operation: less than 500 µW per channel
- Low supply voltage requirements (2.9V-3.6V) permit operation from small batteries
- On-chip high-speed analog multiplexer allows all amplifiers to share one external analog-to-digital converter (over 30 kSamples/s/channel).
- Upper cutoff frequency of all amplifiers set by external resistors; adjustable from 10 Hz to 20 kHz
- Lower cutoff frequency of all amplifiers set by external resistor; adjustable from 0.02 Hz to 1.0 kHz
- True zero gain at DC rejects electrode offset voltages
- *In situ* electrode impedance measurement capability

Applications

- Miniaturized multi-channel headstages for neural or ECoG recording
- Low-power wireless headstages or backpacks for neurophysiology experiments
- Recording spikes and/or local field potentials (LFPs) from microelectrodes
- "Smart Petri dish" *in vitro* recording systems
- Portable multi-channel EEG or EMG recording systems
- Wearable EKG monitors

Description

The RHA2000-series microchips are integrated, low-power amplifier arrays from Intan Technologies. These devices contain 16 or 32 amplifiers with programmable bandwidths suitable for many bioinstrumentation monitoring and recording applications. Proprietary micropower circuit design allows for portable, battery-powered operation without sacrificing low input-referred noise levels needed for detection of microvolt level signals.

The upper bandwidth of the amplifiers may be programmed to any value between 10 Hz and 20 kHz, and the lower bandwidth from 0.02 Hz to 1.0 kHz, by means of three external resistors per chip. This flexibility allows the chips to be optimized for different types of signals (e.g., 0.1 – 100 Hz for EEG or EKG signals, 250 Hz – 7.5 kHz for neural action potentials). Each amplifier has a 3rd-order Butterworth low-pass filter to reject signals and noise beyond the desired bandwidth and to minimize aliasing. Internal capacitors completely reject any DC offset voltages at the input pins, eliminating problems with built-in potentials at electrode-tissue interfaces.

A low-distortion, high-speed analog multiplexer (MUX) routes a selected amplifier signal off the chip. The MUX allows many amplifiers to share a single analog-to-digital converter (ADC) and be sampled at high rates. Additional on-chip circuitry facilitates real time *in situ* electrode impedance measurements.

RHA2000-series chips are packaged in standard 6mm × 6mm or 8mm × 8mm QFN surface-mount packages, and are also available as unpackaged bare die. The small footprint and low power consumption of the multi-channel chips enable the miniaturization of front-end electronics for miniature headstages and other wearable or portable biopotential recording systems.

Simplified Chip Diagrams

RHA2000-SERIES FAMILY

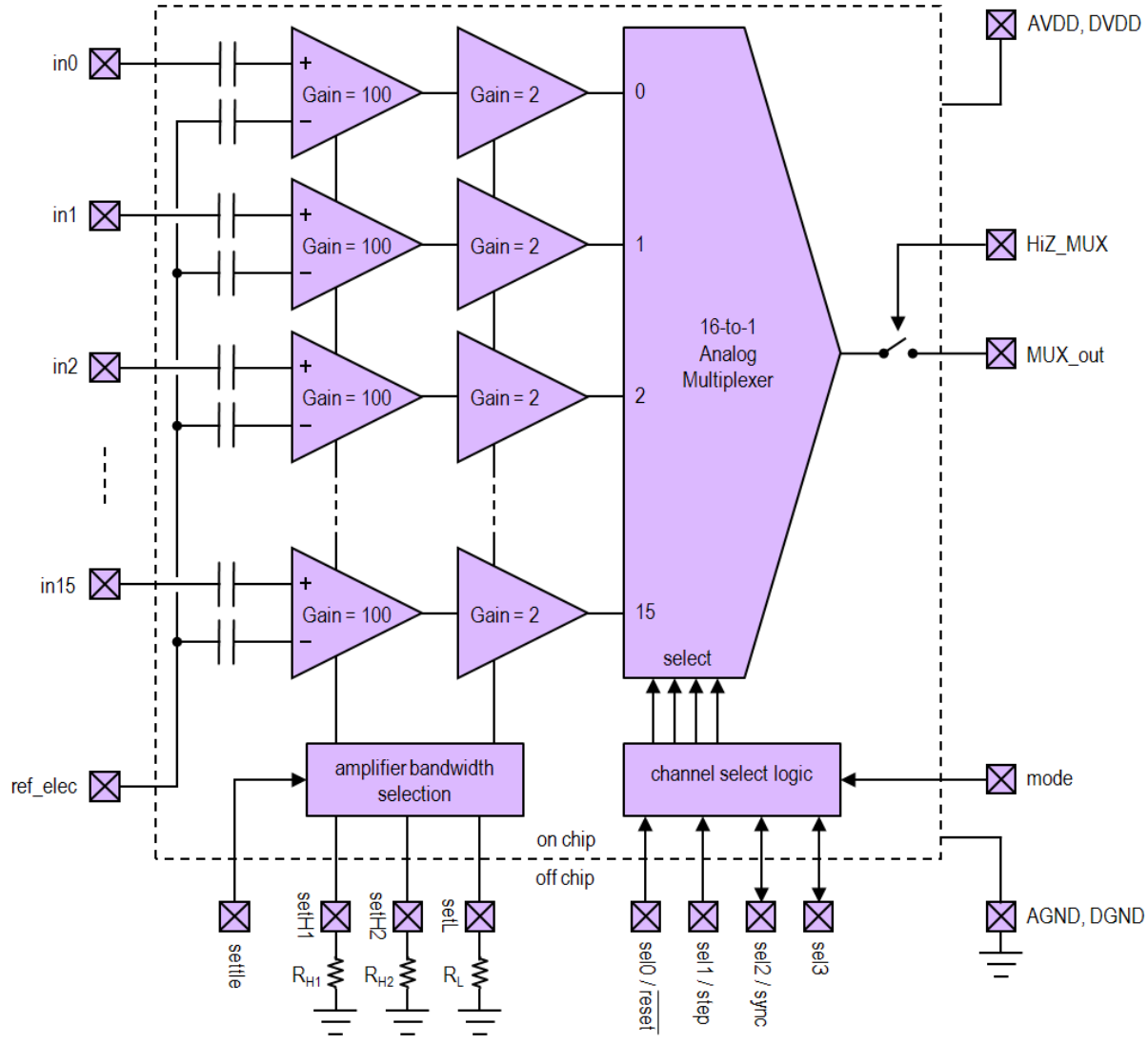
There are three devices in the RHA2000-series amplifier array family: the RHA2116, RHA2216, and RHA2132. The following table lists the features of these chips:

DEVICE	AMPLIFIERS PER CHIP	AMPLIFIER INPUT PINS	PACKAGE SIZE
RHA2116	16	16 unipolar amplifier inputs; 1 common reference input	6 mm × 6 mm 40-pin QFN
RHA2216	16	16 × 2 bipolar amplifier inputs	8 mm × 8 mm 56-pin QFN
RHA2132	32	32 unipolar amplifier inputs; 1 common reference input	8 mm × 8 mm 56-pin QFN

Simplified functional block diagrams of these chips (excluding impedance measurement circuitry) are shown on the next pages.

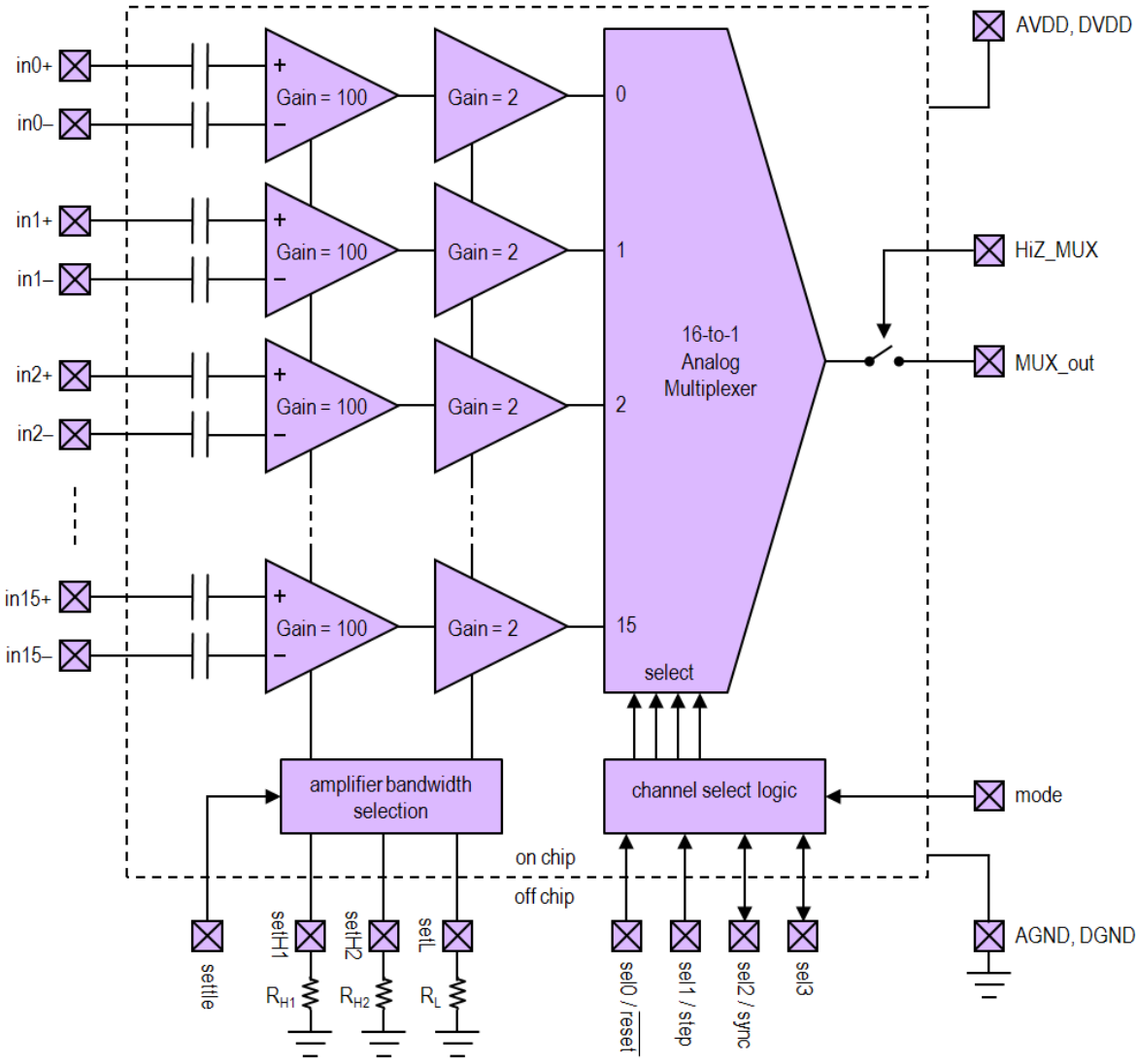
RHA2116 SIMPLIFIED DIAGRAM

The RHA2116 contains an array of 16 amplifiers having unipolar inputs (**in0**, **in1**,…) and a common, shared reference line (**ref_elec**).



RHA2216 SIMPLIFIED DIAGRAM

The RHA2216 contains an array of 16 amplifiers having independently accessible bipolar inputs (**in0+**, **in0–**, **in1+**, **in1–**,…).

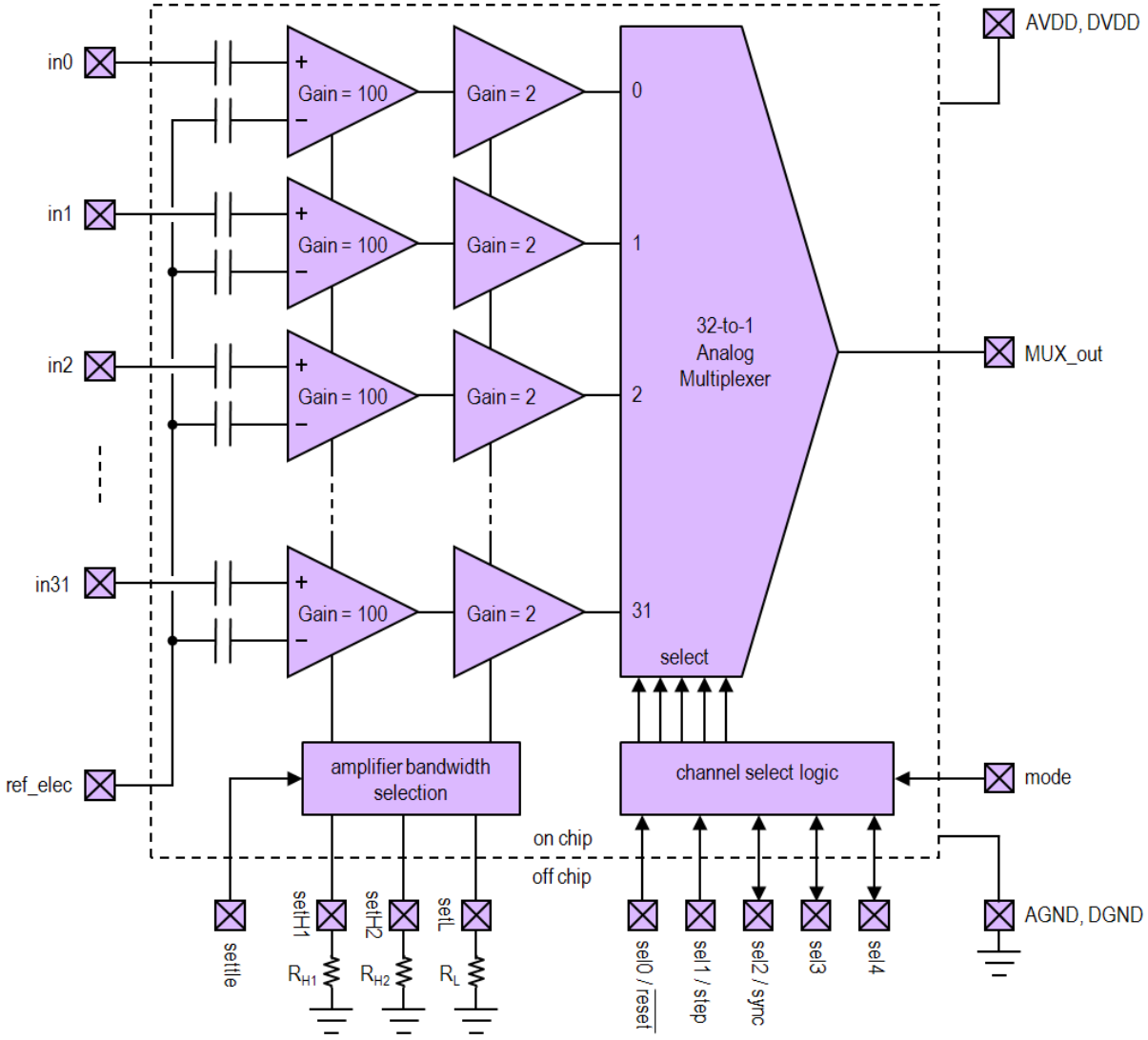


The RHA2216 is recommended for applications where signal (+) and reference (-) electrodes have similar impedances (e.g., surface EMG, EEG). The input impedances of each RHA2216 amplifier pin (**in0+**, **in0–**, **in1+**, **in1–**,…) are identical, so the voltage divider ratio formed by the electrode impedance and the amplifier input impedance will be identical for each electrode. This will improve the system's ability to reject large common-mode signals (e.g., 50/60 Hz) that can otherwise be converted into differential signals by a mismatch in the input impedance seen by the signal and reference electrodes.

The RHA2116 and RHA2132 are recommended for applications where the reference electrode has much lower impedance than the signal electrodes (e.g., recording from microelectrodes and using a platinum reference wire). On these chips, all negative amplifier inputs are tied to one **ref_elec** pin (see previous page and next page), so the input impedance of this pin is 16 or 32 times lower than the input impedance seen by a signal electrode (**in0**, **in1**,…). See page 9 for exact impedance specifications.

RHA2132 SIMPLIFIED DIAGRAM

The RHA2132 contains an array of 32 amplifiers having unipolar inputs (**in0**, **in1**,…) and a common, shared reference line (**ref_elec**).

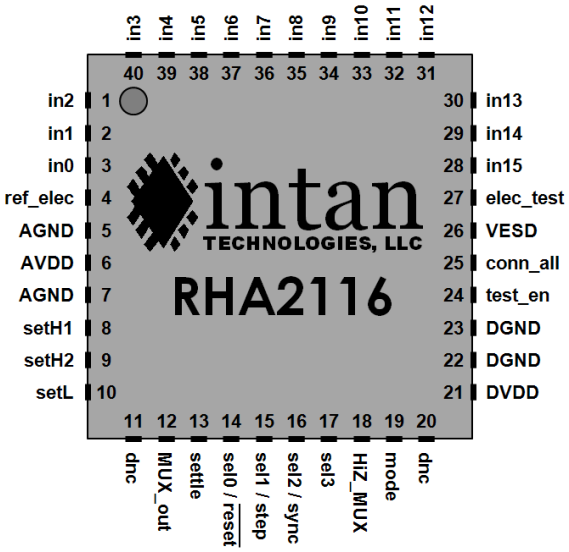


Pin Descriptions

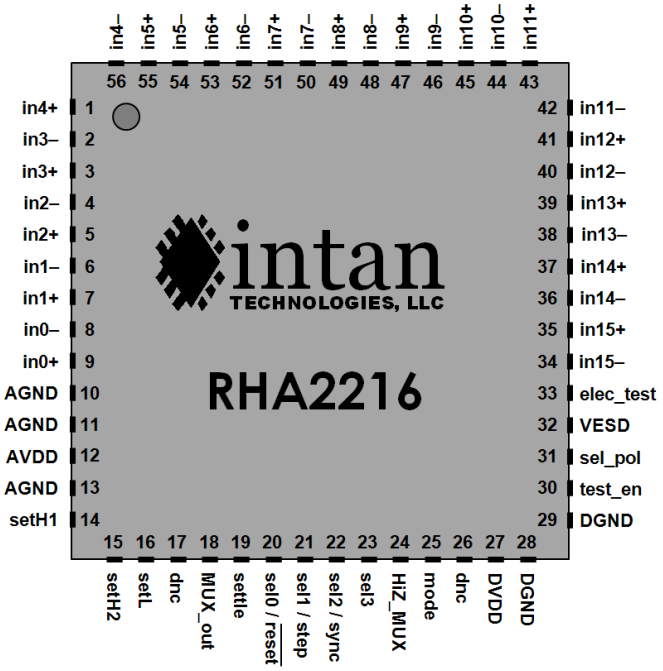
PIN	TYPE	FUNCTION
AVDD, **DVDD**, **AGND**, **DGND**	power	Power supply (2.9V – 3.6V). **AVDD** and **DVDD** must be at the same potential. **AGND** and **DGND** must be at the same potential.
in0, **in1**, **in2,**…	analog inputs	Unipolar amplifier inputs (RHA2116 and RHA2132 only).
ref_elec	analog input	Amplifier array common negative (reference) input (RHA2116 and RHA2132 only).
in0+, **in0–,**…	analog inputs	Bipolar (differential) amplifier inputs (RHA2216 only).
MUX_out	analog output	Amplifier array output after analog multiplexer (MUX).
HiZ_MUX	digital input	Setting this pin high puts **MUX_out** in a high impedance (Hi-Z) state, allowing multiple 16-channel chips to share a single A/D converter by connecting their **MUX_out** pins in parallel. External logic must then be used to ensure that only one chip has **HiZ_MUX** pulled low at any time. (RHA2116 and RHA2216 only.)
mode	digital input	Selects the addressing method for controlling the analog multiplixer. If this pin is pulled low, random access of amplifiers is enabled and pins **sel0**, **sel1**, etc. are used to select the amplifier channel. If this pin is pulled high, sequential access of amplifiers is enabled, and **reset** , **step**, and **sync** are used to advance an on-chip counter that selects successive amplifier channels.
sel0, **sel1**, **sel2,**…	digital inputs	When **mode** is pulled low, these pins serve as channel select for analog multiplexer. Selected amplifier signal appears on output. The **sel0** signal is least significant bit (LSB) in the 4-bit word (RHA2116 or RHA2216) or 5-bit word (RHA2132).
$\overline{\text{reset}}$	digital input	When **mode** is pulled high, pulling this pin low resets the on-chip counter to select channel 0 on **MUX_out**. The reset is asynchronous.
step	digital input	When **mode** is pulled high, a rising edge on **step** advances the on-chip counter to the next amplifier channel. Once reaching the last amplifier, the counter rolls over to 0.
sync	digital output	When **mode** is pulled high, this pin goes high when the on-chip counter is selecting channel 0.
settle	digital input	Fast settle. Pulsing this pin high resets all amplifiers to baseline levels. This pin can be used for quick recovery from large transient signals.
setH1, **setH2**	other	Connection pins for two off-chip resistors used to set the upper bandwidth (f_H) of amplifiers.
setL	other	Connection pin for off-chip resistor used to set the lower bandwidth (f_L) of amplifiers.
test_en	digital input	If **test_en** is pulled high, the **elec_test** pin is connected to the selected amplifier input pin, facilitating electrode impedance measurement or activation.
elec_test	analog input	Used to inject AC currents for electrode impedance measurement or DC voltage for electrode activation.
sel_pol	digital input	When **test_en** is pulled high, **sel_pol** connects **elec_test** to the positive input terminal (**inX+**) if pulled low or the negative input terminal (**inX–**) if pulled high (RHA2216 only).
conn_all	digital input	Ties all amplifier input pins to **elec_test** for parallel activation of electrodes (RHA2116 and RHA2132 only).
VESD	power	Electrostatic discharge protection power line for amplifier inputs. This line should be tied to ground whenever the amplifiers are used. It may be tied to a higher voltage *only* during electrode activation. (See below for more information.)
dnc	do not connect	These pins should be left unconnected. They should *not* be connected to ground or to each other.

Package Descriptions

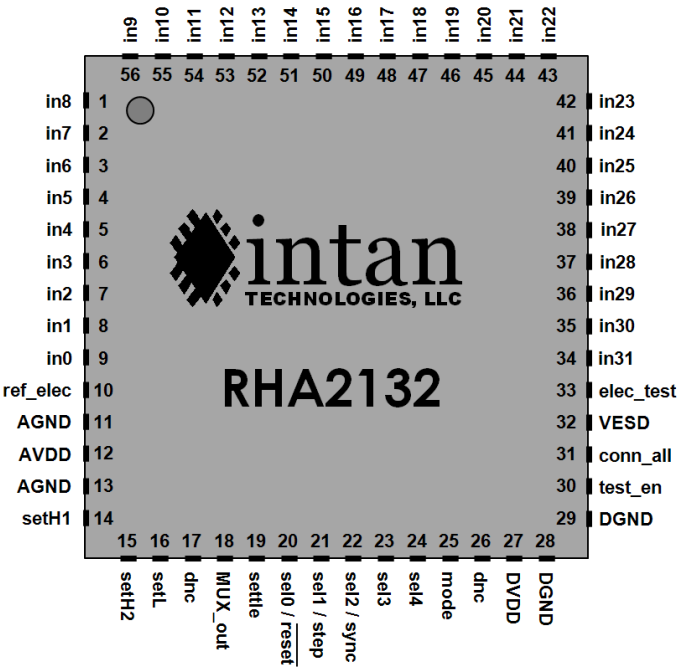
RHA2116: 40-Pin QFN Package



RHA2216: 56-Pin QFN Package



RHA2132: 56-Pin QFN Package



Electrical Characteristics

T_A = 25ºC, V_{DD} = 3.0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNITS	COMMENTS
V_{DD}	Supply Voltage		2.9 – 3.6	V	Recommended nominal supply voltage is 3.0 V – 3.3 V
V_{inLO}	Digital "Low" Input Voltage	For all digital inputs to chip	-0.4 – +0.7	V	Nominal "low" input voltage is GND (0 V)
V_{inHI}	Digital "High" Input Voltage	For all digital inputs to chip	2.4 – V_{DD} + 0.4	V	Nominal "high" input voltage is V_{DD}. *5V signals should not be applied directly to RHA2000-series chips.*
A_D	Differential Gain	In midband region between f_L and f_H	200 46	V/V dB	
A_0	DC Differential Gain		0	V/V	Complete DC rejection, unlike amplifiers that have A_0 = 1 V/V.
f_L	Low-Frequency 3-dB Cutoff Frequency (High-Pass Filter)	Set by off-chip resistor; tunable from 0.02 Hz to 1.0 kHz	0.02 – 1000	Hz	1-pole roll-off below f_L.
f_H	High-Frequency 3-dB Cutoff Frequency (Low-Pass Filter)	Set by two off-chip resistors; tunable from 10 Hz to 20 kHz	10 – 20000	Hz	3-pole 3rd-order Butterworth filter roll-off above f_H.
V_{OUT0}	Baseline Output Voltage	V_{in} = 0 V	1.235	V	
V_{OS}	Input-Referred Offset Voltage		< ±100	µV	Input referred; baseline output voltage varies by 200x this value (i.e., ±20 mV).
V_{OUT}	Output Voltage Swing		0.235 – 2.235	V	MUX output can swing ±1.0V around the baseline level
V_{IN-AC}	Differential Input Voltage AC Swing		±5.0	mV	
V_{IN-DC}	Allowable Input Voltage DC Offset		±0.4	V	
V_{CM}	Allowable Common Mode Input Voltage Range		±0.4	V	
CMRR	Common Mode Rejection Ratio	f = 50 or 60 Hz f = 1 kHz	82 82	dB dB	Typical
PSRR	Power Supply Rejection Ratio	f = 50 or 60 Hz f = 1 kHz	75 75	dB dB	Typical
	Crosstalk	f = 0.05 Hz to 10 kHz	–78	dB	Typical; measured between adjacent amplifiers on chip.
I_b	Amplifier Input Bias Current	–0.2 V <V_{IN} < +0.2 V –0.3 V <V_{IN} < +0.3 V –0.4 V <V_{IN} < +0.4 V	< 20 < 500 < 20	pA pA nA	Individual amplifier input (**inX**, **inX+**, or **inX–** pin) Voltage referenced to GND.
I_{bREF}	Amplifier Reference Input Bias Current	–0.2 V <V_{REF} < +0.2 V –0.3 V <V_{REF} < +0.3 V –0.4 V <V_{REF} < +0.4 V	< 120 < 3 < 120	pA nA nA	Common amplifier reference (**ref_elec** pin) Voltage referenced to GND.

Electrical Characteristics

T_A = 25ºC, V_{DD} = 3.0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNITS	COMMENTS
I_{S16}	16-Amplifier Chip Total Supply Current	f_L = 0.1 Hz			RHA2116 or RHA2216
		V_{DD} = 3.3V,f_H = 10 kHz	2.4	mA	
		V_{DD} = 3.0V,f_H = 10 kHz	2.3	mA	
		V_{DD} = 3.3V,f_H = 5 kHz	1.7	mA	
		V_{DD} = 3.0V,f_H = 5 kHz	1.7	mA	
		V_{DD} = 3.3V,f_H = 1 kHz	1.3	mA	
		V_{DD} = 3.0V,f_H = 1 kHz	1.3	mA	
		V_{DD} = 3.3V,f_H = 500 Hz	1.3	mA	
		V_{DD} = 3.0V,f_H = 500 Hz	1.2	mA	
P_{S16}	16-Amplifier Chip Total Power Dissipation	f_L = 0.1 Hz			RHA2116 or RHA2216
		V_{DD} = 3.3V,f_H = 10 kHz	7.8	mW	
		V_{DD} = 3.0V,f_H = 10 kHz	7.0	mW	
		V_{DD} = 3.3V,f_H = 5 kHz	5.6	mW	
		V_{DD} = 3.0V,f_H = 5 kHz	5.0	mW	
		V_{DD} = 3.3V,f_H = 1 kHz	4.3	mW	
		V_{DD} = 3.0V,f_H = 1 kHz	3.8	mW	
		V_{DD} = 3.3V,f_H = 500 Hz	4.1	mW	
		V_{DD} = 3.0V,f_H = 500 Hz	3.7	mW	
I_{S32}	32-Amplifier Chip Total Supply Current	f_L = 0.1 Hz			RHA2132
		V_{DD} = 3.3V,f_H = 10 kHz	4.7	mA	
		V_{DD} = 3.0V,f_H = 10 kHz	4.7	mA	
		V_{DD} = 3.3V,f_H = 5 kHz	3.5	mA	
		V_{DD} = 3.0V,f_H = 5 kHz	3.5	mA	
		V_{DD} = 3.3V,f_H = 1 kHz	2.8	mA	
		V_{DD} = 3.0V,f_H = 1 kHz	2.8	mA	
		V_{DD} = 3.3V,f_H = 500 Hz	2.7	mA	
		V_{DD} = 3.0V,f_H = 500 Hz	2.7	mA	
P_{S32}	32-Amplifier Chip Total Power Dissipation	f_L = 0.1 Hz			RHA2132
		V_{DD} = 3.3V,f_H = 10 kHz	15.4	mW	
		V_{DD} = 3.0V,f_H = 10 kHz	14.0	mW	
		V_{DD} = 3.3V,f_H = 5 kHz	11.4	mW	
		V_{DD} = 3.0V,f_H = 5 kHz	10.6	mW	
		V_{DD} = 3.3V,f_H = 1 kHz	9.1	mW	
		V_{DD} = 3.0V,f_H = 1 kHz	8.3	mW	
		V_{DD} = 3.3V,f_H = 500 Hz	8.8	mW	
		V_{DD} = 3.0V,f_H = 500 Hz	8.1	mW	

Electrical Characteristics

T_A = 25°C, V_{DD} = 3.0V unless otherwise noted.

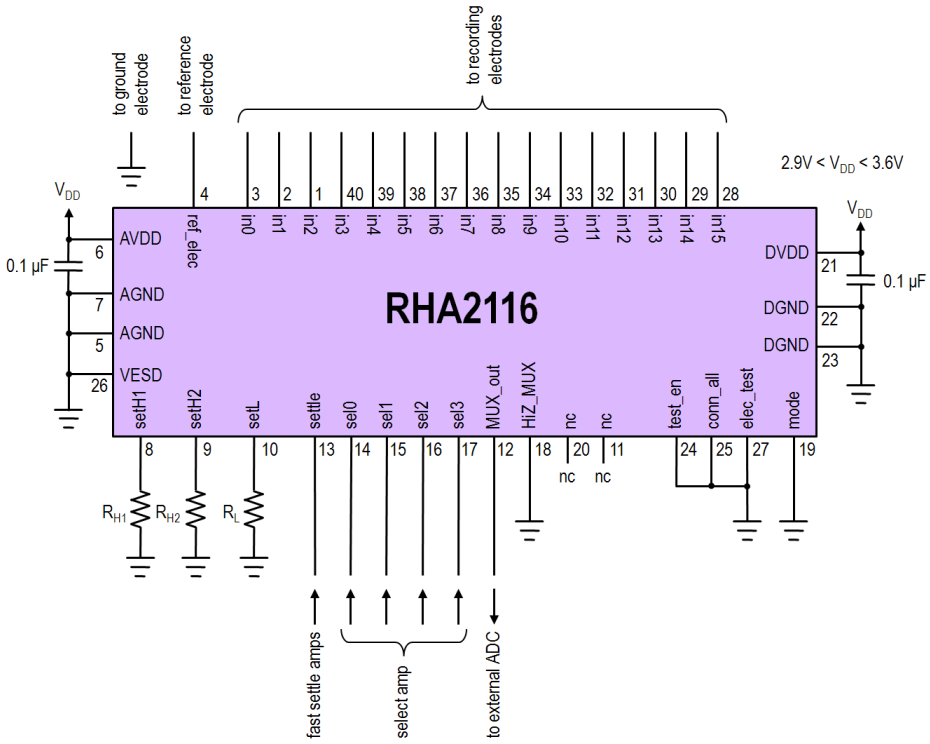
SYMBOL	PARAMETER	CONDITIONS	VALUE	UNITS	COMMENTS
C_{in}	Input Capacitance		12	pF	Individual amplifier input (**inX**, **inX+**, or **inX–** pin)
C_{inREF}	Reference Input Capacitance	RHA2116 RHA2132	164 325	pF pF	Common amplifier reference (**ref_elec** pin)
$\|Z_{in}\|$	Input Impedance	f = 10 Hz f = 1 kHz	1300 13	MΩ MΩ	Individual amplifier input (**inX**, **inX+**, or **inX–** pin)
$\|Z_{inREF}\|$	Reference Input Impedance	f = 10 Hz, RHA2116 f = 1 kHz, RHA2116 f = 10 Hz, RHA2132 f = 1 kHz, RHA2132	100 1 50 0.5	MΩ MΩ MΩ MΩ	Common amplifier reference (**ref_elec** pin)
v_{ni}	Input-Referred Noise		2	μV_{rms}	Typical. Varies slightly with amplifier bandwidth.
THD	Total Harmonic Distortion (with f_L = 0.1 Hz, f_H = 10 kHz)	f = 1 kHz V_{IN} = 4 mV_{P-P} V_{IN} = 10 mV_{P-P}	 0.1 < 0.8	 % %	Includes any nonlinearity in MUX. Distortion may increase near f_L and f_H.
f_{MUX}	Maximum MUX Switching Frequency		1.0	MHz	16 amplifiers can be sampled up to 62.5 kSamples/s each. 32 amplifiers can be sampled up to 31.25 kSamples/s each.
t_{settle}	MUX Settling Time	C_L = 20 pF || R_L > 1 MΩ C_L = 80 pF || R_L > 1 MΩ	500 800	ns ns	Capacitive load on **MUX_out** should be minimized for rapid multiplexing.
	Size and Mass of Packaged RHA2116		6.0 × 6.0 0.089	mm^2 g	40-pin plastic QFN package (0.85 mm thick).
	Size and Mass of Packaged RHA2216 or RHA2132		8.0 × 8.0 0.158	mm^2 g	56-pin plastic QFN package (0.85 mm thick).
	Size and Mass of RHA2116 Bare Die		2.8 × 3.1 0.005	mm^2 g	Silicon die with aluminum pads (0.25 mm thick)
	Size and Mass of RHA2216 or Bare Die		3.7 × 3.1 0.007	mm^2 g	Silicon die with aluminum pads (0.25 mm thick)
	Size and Mass of RHA2132 or Bare Die		4.8 × 3.1 0.009	mm^2 g	Silicon die with aluminum pads (0.25 mm thick)

ESD CAUTION

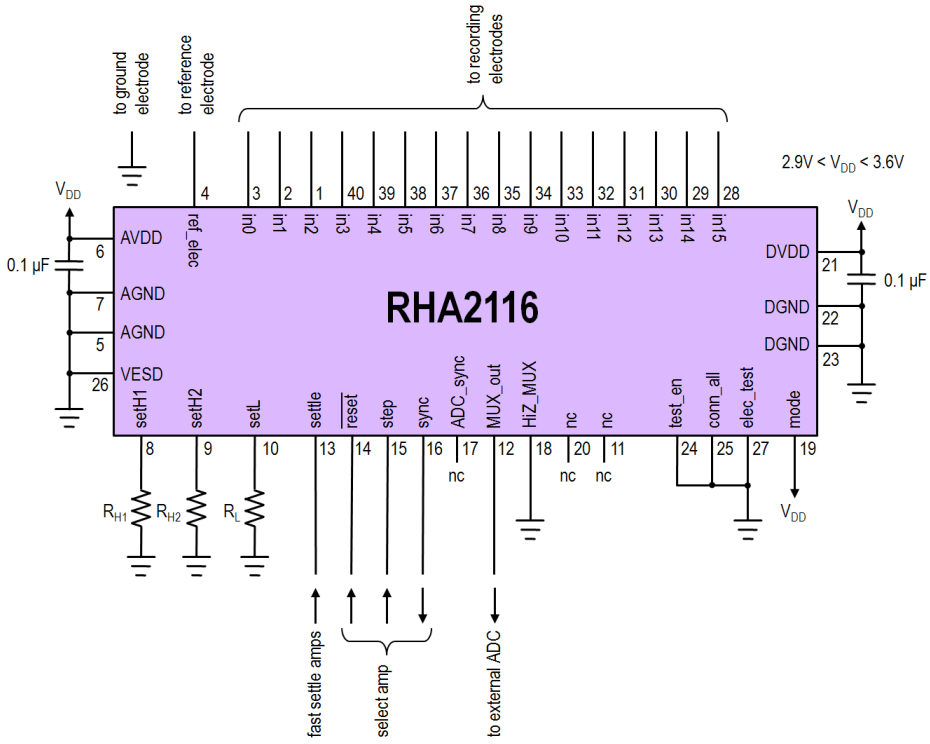
Like all CMOS integrated circuits, RHA2000-series chips are ESD (electrostatic discharge) sensitive devices. Electrostatic charges of greater than 1000 V can accumulate on the human body and test equipment and can discharge without detection. Although these products incorporate standard ESD protection circuitry to protect against mild ESD events, permanent damage may occur on devices subjected to high energy electrostatic discharges. Severe ESD damage can lead to amplifier input bias currents exceeding specified limits. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality. If strong ESD events are possible, external transient voltage suppressors manufactured by a variety of semiconductor companies (e.g., Vishay, Littelfuse, STMicroelectronics) should be used to provide additional protection.

Typical Connection Diagram

RANDOM AMPLIFIER ACCESS (MODE = 0)



SEQUENTIAL AMPLIFIER ACCESS (MODE = 1)



Measured Performance Characteristics

BIOPOTENTIALS MEASURED WITH RHA2000-SERIES AMPLIFIERS

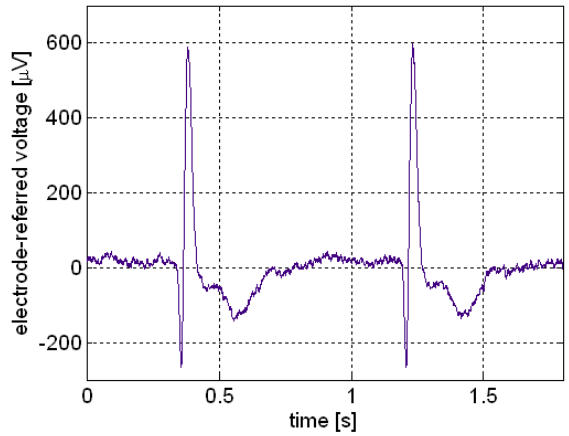


Figure 1. EKG signal recorded with three Ag/AgCl electrodes (amplifier input and reference on chest, 5 cm apart; ground on elbow) during two heartbeats. Amplifier was configured with **f_L = 0.1 Hz, f_H = 100 Hz**.

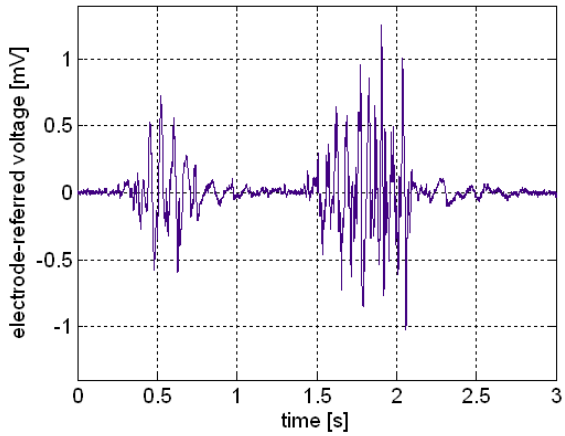


Figure 2. EMG signal recorded with three Ag/AgCl electrodes (amplifier input and reference on bicep, 5 cm apart; ground on elbow) during bicep contractions. Amplifier was configured with **f_L = 10 Hz, f_H = 1.0 kHz**.

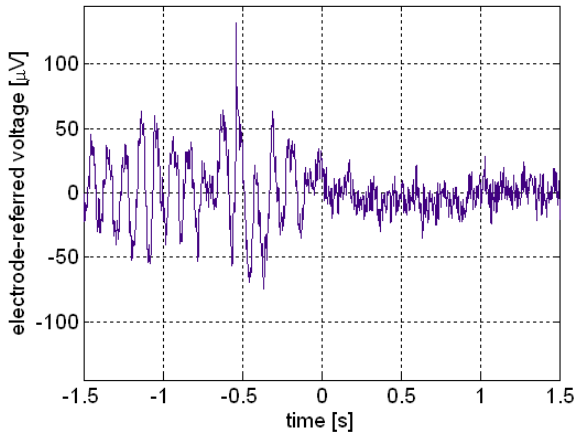


Figure 3. EEG signal recorded from electrode at occipital region O_2 with **f_L = 1.0 Hz, f_H = 100 Hz**. Reference was at location C_Z and ground was connected to left earlobe. Subject's eyes were closed initially then opened at t = 0, suppressing the 10 Hz alpha waves. Some residual 60 Hz interference is also present.

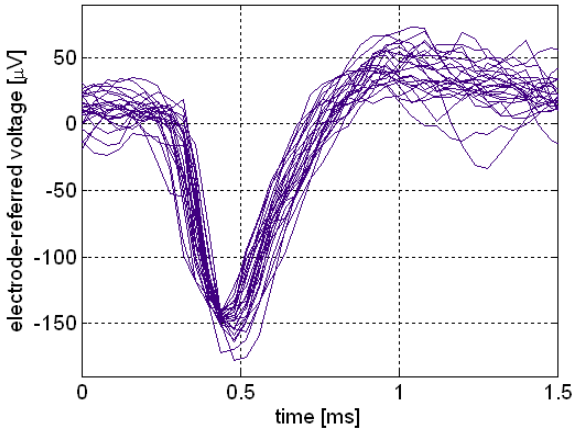


Figure 4. Superimposed time-aligned neural spikes recorded from mouse brain using 260 kΩ gold microelectrode with **f_L = 1.0 Hz, f_H = 10 kHz**. Additional software filtering was used to attenuate frequencies below 250 Hz after recording.

Measured Performance Characteristics

AMPLIFIER NOISE AND OUTPUT MUX SWITCHING

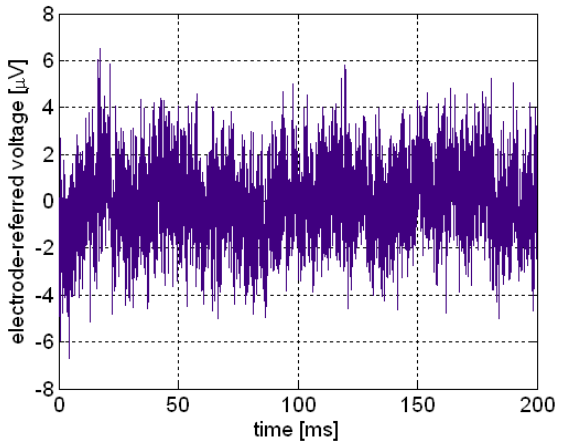


Figure 5. Typical electrode-referred noise for amplifier configured with **f_L = 0.1 Hz, f_H = 10 kHz**, measured for **200 ms**.

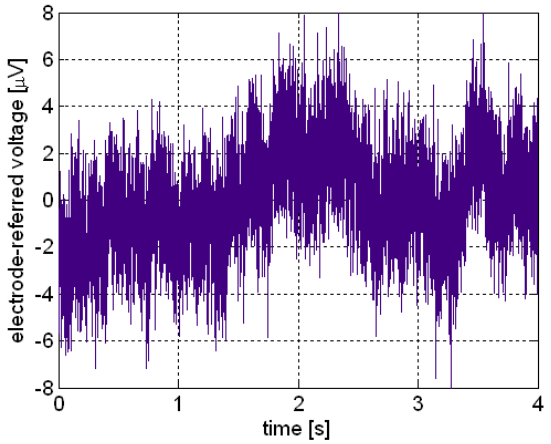


Figure 6. Typical electrode-referred noise for amplifier configured with **f_L = 0.1 Hz, f_H = 10 kHz**, measured for **4 s**.

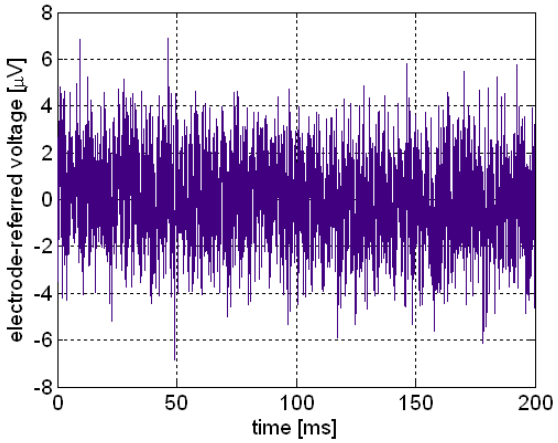


Figure 7. Typical electrode-referred noise for amplifier configured with **f_L = 250 Hz, f_H = 7.5 kHz**.

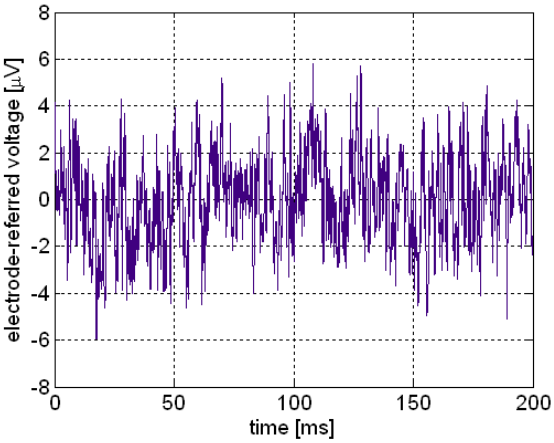


Figure 8. Typical electrode-referred noise for amplifier configured with **f_L = 20 Hz, f_H = 1.0 kHz**.

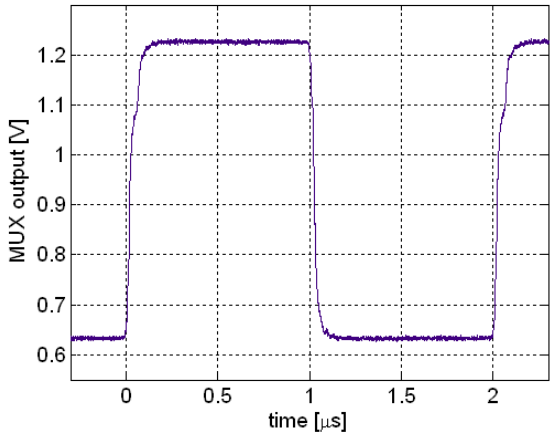


Figure 9. Output MUX switching channels every 1 µs with load of **20 pF || 10 MΩ** on the **MUX_out** pin.

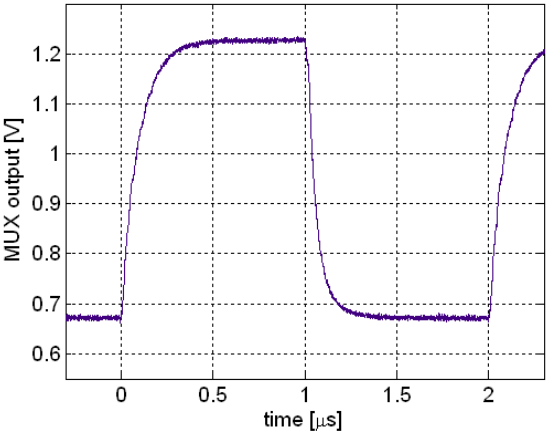


Figure 10. Output MUX switching channels every 1 µs with load of **80 pF || 10 MΩ** on the **MUX_out** pin.

Measured Performance Characteristics

SAMPLING AMPLIFIER ARRAY WITH EXTERNAL ADC

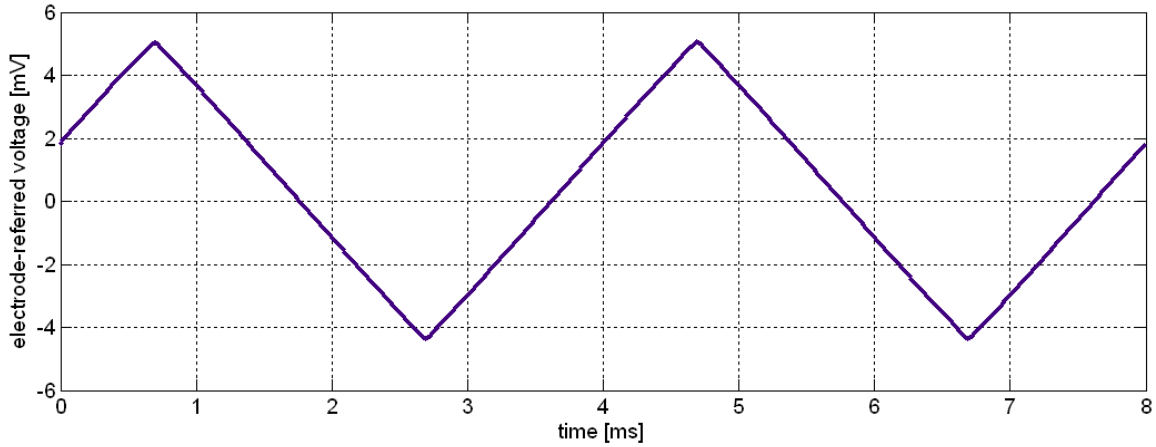


Figure 11. Measurement of **±5.0 mV**, 250 Hz triangle wave using off-chip 16-bit ADC running at **62.5 kSamples/s per channel** (total ADC sampling rate = 1.0 MSample/s), showing large-signal linearity.

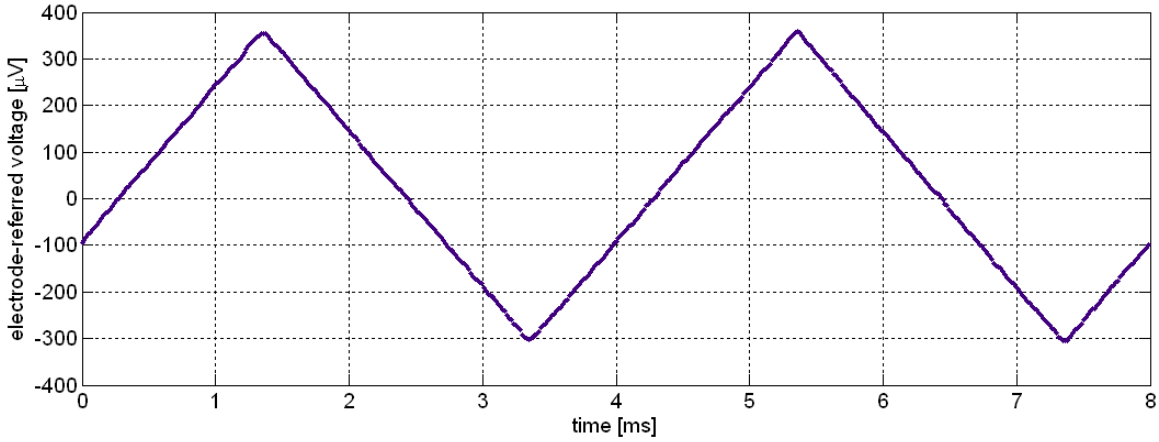


Figure 12. Measurement of **±350 µV**, 250 Hz triangle wave using off-chip 16-bit ADC running at **62.5 kSamples/s per channel** (total ADC sampling rate = 1.0 MSample/s).

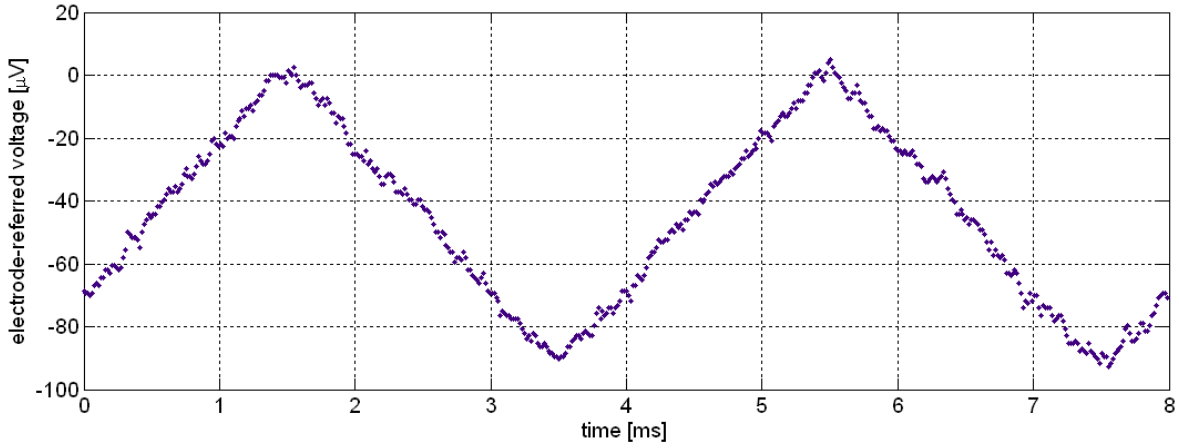


Figure 13. Measurement of **±50 µV**, 250 Hz triangle wave using off-chip 16-bit ADC running at **62.5 kSamples/s per channel** (total ADC sampling rate = 1.0 MSample/s), showing amplifier noise.

Measured Performance Characteristics

TYPICAL AMPLIFIER GAIN AND PHASE CHARACTERISTICS

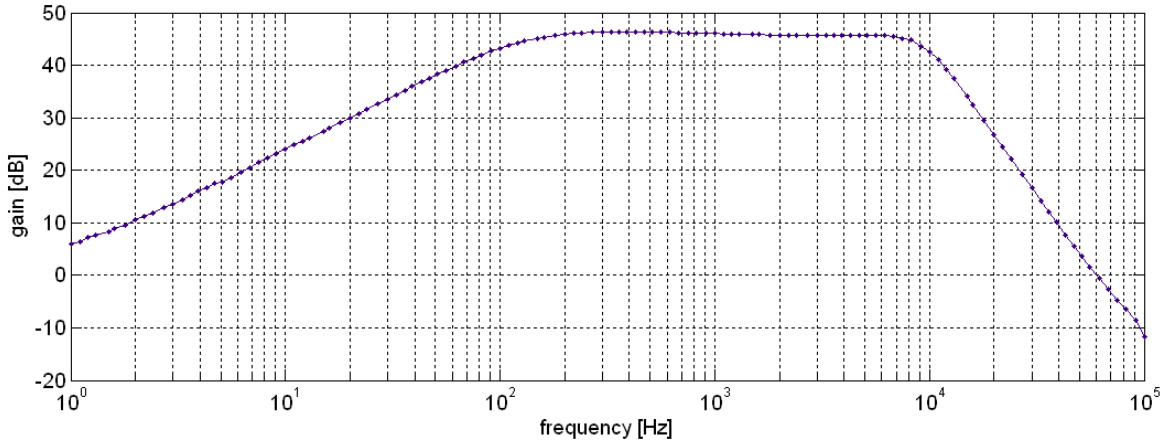


Figure 14. Measured amplifier gain from 1 Hz to 100 kHz. Amplifier was configured for **f_L = 100 Hz, f_H = 10 kHz**. Gain is measured in dB, where $Gain_{[dB]} = 20 \cdot \log_{10}(Gain_{[V/V]})$, so 20 dB = 10 V/V. At frequencies above f_H, gain decreases 60 dB/decade (18 dB/octave). At frequencies below f_L, gain decreases 20 dB/decade (6 dB/octave).

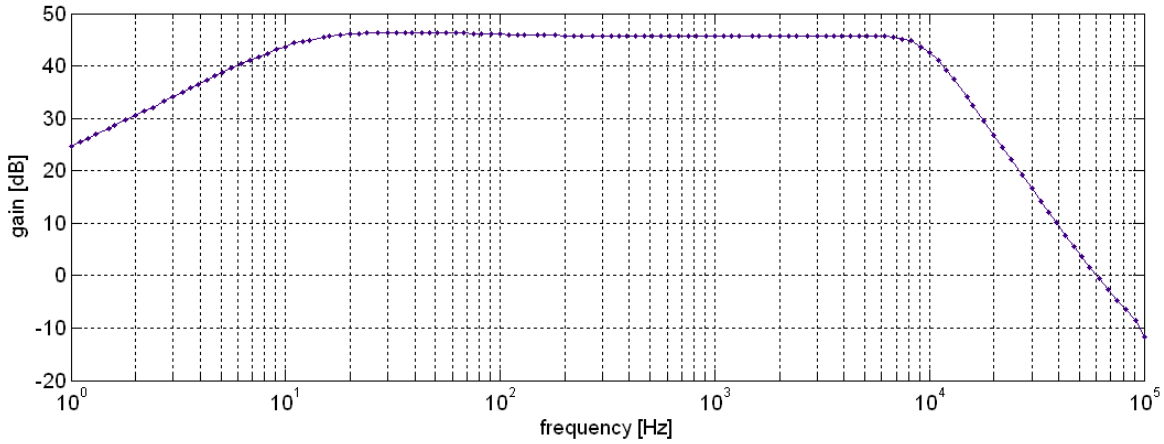


Figure 15. Measured amplifier gain from 1 Hz to 100 kHz. Amplifier was configured for **f_L = 10 Hz, f_H = 10 kHz**.

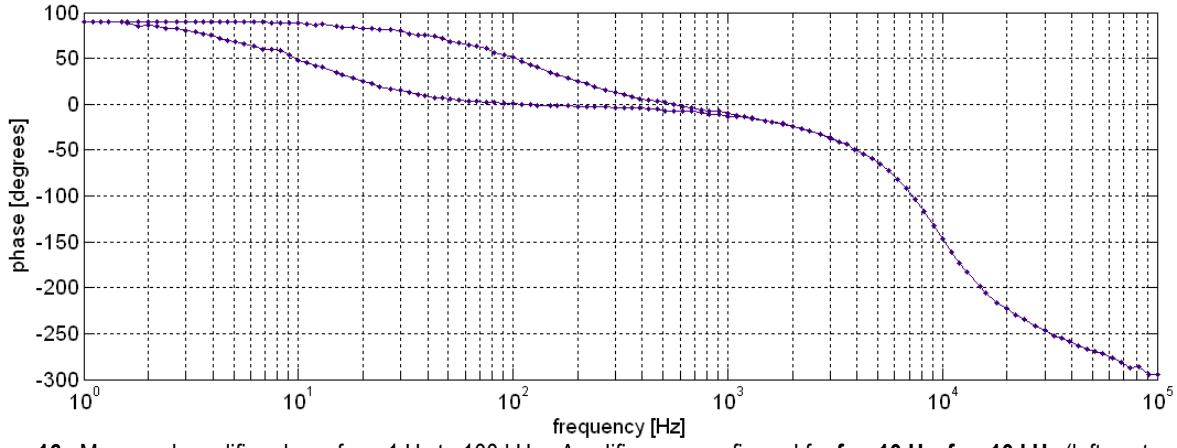


Figure 16. Measured amplifier phase from 1 Hz to 100 kHz. Amplifier was configured for **f_L = 10 Hz, f_H = 10 kHz** (leftmost curve), or **f_L = 100 Hz, f_H = 10 kHz** (rightmost curve). Negative phase denotes the output lagging the input. Phase response asymptotes to +90° for f << f_L and roughly -270° for f >> f_H.

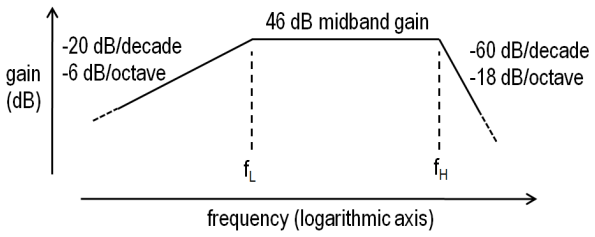
Amplifier Bandwidth

At the core of each RHA2000-series chip is an array of low-noise amplifiers with a midband gain of 46 dB (200 V/V) and built-in filtering to isolate frequencies of interest. The upper bandwidth has a 3rd-order Butterworth low-pass filter at the 3-dB frequency f_H. The lower bandwidth has a 1st-order high-pass filter characteristic at the 3-dB frequency f_L.

The 3rd-order Butterworth low-pass filter characteristic at f_H has a maximally flat pass-band region with -60 dB/decade (-18 dB/octave) of attenuation beyond f_H. The table below lists filter gains for several frequencies above and below f_H.

SIGNAL FREQUENCY	NORMALIZED GAIN	
	V/V	dB
0.5· f_H	0.99	-0.07 dB
0.8· f_H	0.89	-1.0 dB
f_H	0.707	-3.0 dB
1.2· f_H	0.50	-6.0 dB
2· f_H	0.12	-18 dB
10· f_H	0.001	-60 dB

The diagram below illustrates the frequency response of RHA2000-series amplifiers:



See the Measured Performance Characteristics section for a diagram of actual gain and phase response versus signal frequency.

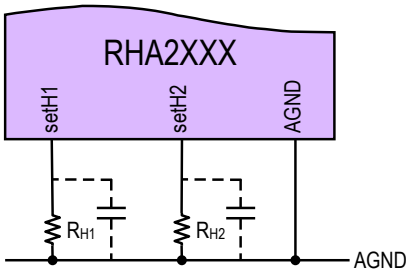
Setting Upper Bandwidth

Two off-chip resistors, R_{H1} and R_{H2}, are tied to the pins **setH1** and **setH2** to set the upper bandwidth (f_H) of the amplifiers. Standard 1% resistor values are given in the table to the right. Resistors with these precise values may be obtained from many electronic component distributors. Any resistor with a power rating of 0.01 W or greater may be used. For bandwidths not listed on this table, interpolate or contact Intan Technologies for recommended resistor values.

UPPER BANDWIDTH f_H	R_{H1}	R_{H2}
20 kHz	6.80 kΩ	11.5 kΩ
15 kHz	9.10 kΩ	15.0 kΩ
10 kHz	12.4 kΩ	21.0 kΩ
7.5 kHz	15.8 kΩ	26.7 kΩ
5.0 kHz	22.0 kΩ	37.4 kΩ
3.0 kHz	34.0 kΩ	57.6 kΩ
2.5 kHz	39.2 kΩ	66.5 kΩ
2.0 kHz	47.5 kΩ	80.6 kΩ
1.5 kHz	61.9 kΩ	102 kΩ
1.0 kHz	88.7 kΩ	147 kΩ
750 Hz	115 kΩ	191 kΩ
500 Hz	169 kΩ	274 kΩ
300 Hz	270 kΩ	432 kΩ
250 Hz	324 kΩ	511 kΩ
200 Hz	402 kΩ	634 kΩ
150 Hz	523 kΩ	820 kΩ
100 Hz	787 kΩ	1.20 MΩ
75 Hz	1.05 MΩ	1.58 MΩ
50 Hz	1.60 MΩ	2.32 MΩ
30 Hz	2.70 MΩ	3.83 MΩ
25 Hz	3.30 MΩ	4.64 MΩ
20 Hz	4.12 MΩ	5.76 MΩ
15 Hz	5.62 MΩ	7.68 MΩ
10 Hz	8.87 MΩ	12 MΩ

See the Application Notes section for circuits that can be used to make the amplifier bandwidth digitally programmable.

Both R_{H1} and R_{H2} should be tied to GND, as shown in the next figure. Care should be taken to minimize parasitic capacitance (such as stray capacitance resulting from long circuit board traces) at the **setH1** and **setH2** pins. Capacitance on each of these pins should be kept below 50 pF. (Do *not* add capacitors to these pins; the capacitors in the diagram below represent stray capacitance which should be minimized.) Resistors should be kept close to the RHA2000-series chip on the printed circuit board, particularly when resistor values exceed 1 MΩ.



Setting Lower Bandwidth

Each RHA2000-series chip has a programmable lower bandwidth that is set by an external resistor R_L tied to the pin **setL**. Standard 1% resistor values are given in the table to the right.

The resistor R_L should be tied to GND. As with R_{H1} and R_{H2}, care should be taken in minimize parasitic capacitance on pin 10. This resistor should be kept close to the RHA2000-series chip on the printed circuit board.

LOWER BANDWIDTH f_L	R_L
1.0 kHz	5.36 kΩ
750 Hz	5.49 kΩ
500 Hz	5.76 kΩ
300 Hz	6.20 kΩ
250 Hz	6.34 kΩ
200 Hz	6.65 kΩ
150 Hz	7.15 kΩ
100 Hz	7.87 kΩ
75 Hz	8.45 kΩ
50 Hz	9.53 kΩ
30 Hz	11.3 kΩ
25 Hz	12.0 kΩ
20 Hz	13.0 kΩ
15 Hz	14.3 kΩ
10 Hz	16.9 kΩ
7.5 Hz	19.1 kΩ
5.0 Hz	23.2 kΩ
3.0 Hz	32.4 kΩ
2.5 Hz	36.5 kΩ
2.0 Hz	43.0 kΩ
1.5 Hz	56.0 kΩ
1.0 Hz	86.6 kΩ
0.75 Hz	127 kΩ
0.50 Hz	226 kΩ
0.30 Hz	511 kΩ
0.25 Hz	698 kΩ
0.20 Hz	1.05 MΩ
0.15 Hz	1.74 MΩ
0.10 Hz	3.74 MΩ
0.075 Hz	6.65 MΩ
0.050 Hz	15 MΩ
0.030 Hz	33 MΩ
0.025 Hz	50 MΩ
0.020 Hz	100 MΩ

See the Application Notes section for circuits that can be used to make the amplifier bandwidth digitally programmable.

Supply Voltage Levels

RHA2000-series chips require a regulated voltage supply (V_{DD}) between 2.9V and 3.6V for operation. A nominal supply voltage between 3.0V and 3.3V is recommended for most applications. The **AVDD** and **DVDD** pins should be kept at identical potentials.

The following pins should all be connected to ground: **AGND**, **AGND**, **DGND**, and **VESD**. All of these pins must be kept at the same potential, and the DC level of signals going to the amplifiers and amplifier reference should be kept at this same ground potential.

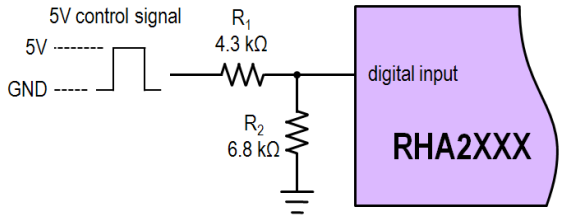
In all applications using these chips, it is necessary to tie the biological tissue under observation to chip ground. The DC electrode potentials always should be near chip ground, although small positive or negative electrode-tissue potentials can be present. At all times, electrode potentials should be held within ±400 mV of chip ground. In this input voltage range, DC currents into the input pins are less than ±20 nA.

A 0.1 µF power supply bypass capacitor should be connected between the **DVDD** and **DGND** pins, and should be located as close as possible to the chip on the printed circuit board. An additional 0.1 µF bypass capacitor should be connected between the **AVDD** and **AGND** pins on the opposite side of the chip. Standard ceramic capacitors are recommended. If long wires are used to supply power to the circuit board, an additional capacitor (1 µF to 10 µF tantalum or ceramic) should be used to bypass V_{DD} and ground where these lines first connect to the board.

Control Voltage Levels

The RHA2000-series chips have a number of digital input pins: **sel0**, **sel1**, etc. control which amplifier signal appears at the output pins, **mode** controls the manner in which amplifiers are addressed, **HiZ_MUX** can set the multiplexer output to a high impedance state, and **settle** performs a fast settle on the amplifiers. The logic threshold separating logic "low" from logic "high" is approximately half of V_{DD}.

Any device sending digital control signals to a RHA2000-series chip should provide logic levels between -0.4 V and +0.7 V for a logical "low", or between 2.4 V and V_{DD} + 0.4 V for a logical "high". *Note: 5V logic signals cannot be used directly with RHA2000-series chips.* Logic signals more than 400 mV above V_{DD} or more than 400 mV below ground can cause permanent damage to the chip. Logic signals between 0.7 V and 2.4 V will not damage the chip, but may cause excessive power dissipation. A simple resistor divider interface can allow 5V logic signals to control RHA2000-series digital inputs safely:



The digital inputs of an RHA2000-series chip should always be driven either high or low. An input pin left unconnected may drift or oscillate unpredictably. Note that the **sel2/sync** and **sel3** pins act as inputs when **mode** = 0 and outputs when **mode** = 1. Digital outputs should never be driven by external electronics.

Analog Multiplexer Control

The RHA2000-series chips have two modes for selecting which signal from the 16 amplifiers is passed through the analog multiplexer to the output pin **MUX_out**: random access and sequential access.

RANDOM ACCESS

If the **mode** pin is pulled low, the amplifiers may be accessed in any order by applying a digital word to pins **sel0** – **sel3** (RHA2116 or RHA2216) or **sel0** – **sel4** (RHA2132). The **sel0** signal is least significant bit (LSB) in the word. The output signal from the selected amplifier appears on **MUX_out** after the specified settling time.

SEQUENTIAL ACCESS

If the **mode** pin is pulled high, the amplifiers are accessed in a sequential manner using an on-chip counter. This counter is controlled by the **reset** and **step** pins. When **reset** is pulled low, the internal counter is reset to zero and the signal from amplifier channel 0 appears on **MUX_out**. On the rising edge of **step**, the counter advances to the next amplifier channel. If the last amplifier in the array is being addressed, the counter next rolls over to channel 0. (Note that **reset** is an asynchronous reset, and does not require a rising edge on **step** to take effect. Care should be taken to ensure that glitches are absent on this signal, as this could lead to spurious resetting of the on-chip counter.) The state of the on-chip counter is undetermined at power-up, so **reset** can be used to start the counter in a known state.

In sequential access mode, the **sync** pin acts as a digital output, and goes high when the on-chip counter is selecting channel 0. This signal can be used to verify the state of the on-chip counter.

In sequential access mode, the **sel3** pin acts as a digital output that always drives a digital low signal off the chip.

This pin should not be driven by external circuits or excess power dissipation will result.

Fast Settle Function

Due to the potentially long time constant associated with the low cutoff frequency f_L, it may be useful to reset the amplifiers if a large input signal causes the output signals to saturate. The fast settle pin (**settle**) is an active-high digital input that should be held low in normal operation. To settle the amplifiers, **settle** should be pulled high momentarily. It is recommended (though not required) to hold **settle** high momentarily after powering up the chip if low values of f_L are used.

The recommended duration of a fast settle pulse is $2.5/f_H$; as the upper bandwidth of the amplifiers is lowered, settling takes more time. Using this guideline, if f_H is set to 10 kHz then a 250 µs pulse is sufficient to settle the amplifiers to baseline.

Analog Multiplexer Output

The voltage on the analog multiplexer output pin **MUX_out** maintains a DC level of approximately 1.235 V, generated by an on-chip voltage reference. With the amplifier gain of 200, the output will swing ±1.0 V around this baseline level in response to input signals with amplitudes up to ±5 mV. Each amplifier channel has some small random DC offset in the range of ±100 µV, referred to the amplifier input. This leads to an offset of ±20 mV in the baseline level of different amplifier channels at the **MUX_out** pin. See the Application Notes section for a method to remove these offsets in software after A/D conversion.

In most applications, **MUX_out** will be connected to an analog-to-digital converter (ADC). The designer must ensure that the total capacitive loading C_L on each output pin does not exceed 80 pF and that any load resistance R_L is no smaller than 1 MΩ. Larger capacitive loads will impair the ability of the analog MUX to switch at rapid speeds.

It is important to remember that standard coaxial cable has a capacitance of approximately 100 pF/meter, so care must be taken to minimize the length of high-capacitance shielded cables connected to the output. In some applications, it may be desirable to convey the analog output signal of the RHA2000-series chip some distance over ribbon cable or a twisted pair of wires. Ribbon cable typically has an inter-wire capacitance of 30 – 50 pF/meter; twisted pair capacitance can range from 60 – 80 pF/meter.

When a new amplifier channel is selected, the output voltage will change to reflect the signal from the newly selected amplifier. The output voltage takes between 500 ns and 800 ns to settle to a new value, depending on the capacitance on the **MUX_out** pin. If an external ADC is used to sample the RHA2000-series chip output signal, a conversion should not be initiated until the proper settling time has elapsed after a new channel is selected.

If we budget 500 ns for the MUX to settle and another 500 ns to wait while the ADC samples the RHA2000-series chip output voltage and initiates a conversion, then we can sample at the rate of 1.0 MSamples/s. This would allow us to sample each of the 16 amplifiers on the RHA2116 or RHA2216 at a rate of 62.5 kSamples/s, or sample each of the 32 amplifiers on the RHA2132 at 31.25 kSamples/s each. See the Application Notes section for an example of interfacing an ADC to an RHA2000-series chip.

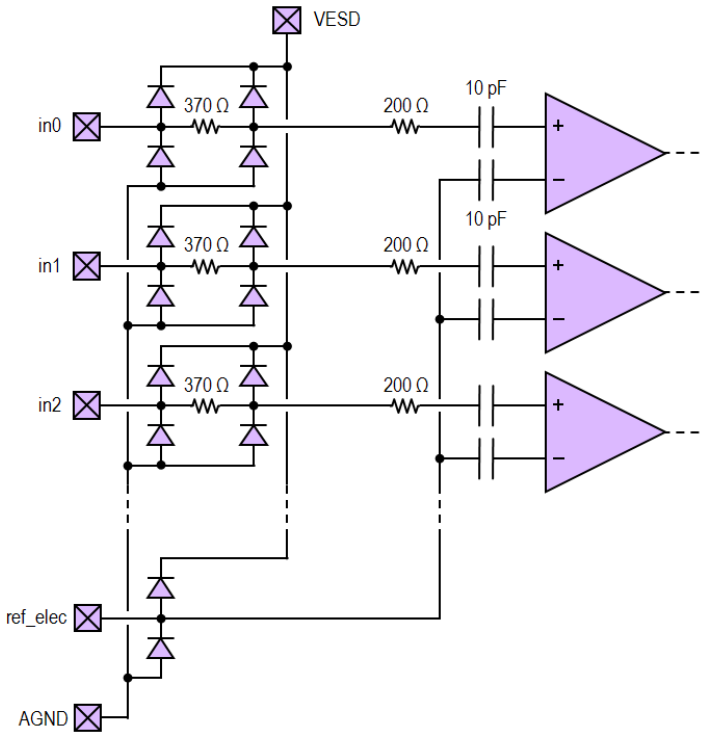
Under normal operation, the **HiZ_MUX** pin should be held low. If **HiZ_MUX** is held high, the output pins assume a high-impedance state. This allows multiple 16-channel chips to share a single ADC. See the Application Notes section for an example of this technique. Note that the RHA2132 does not have a **HiZ_MUX** pin.

Amplifier Input Protection

All CMOS integrated circuits are susceptible to damage by exposure to electrostatic discharge (ESD) from charged bodies. Electrostatic charges of greater than 1000 V can accumulate on the human body or test equipment and can discharge without detection. All RHA2000-series chips incorporate protection circuitry to guard against mild ESD events. However, permanent damage may occur on devices subjected to high energy electrostatic discharges. It is important for users to understand the nature of the ESD protection circuitry used on the chip.

The figure below illustrates the passive elements (diodes and resistors) used for ESD protection at the input to each amplifier. Diodes are connected to **AGND** and **VESD**, and are used to bleed off charge quickly to prevent the voltage on the series capacitors from exceeding damaging levels. Small series resistors (370 Ω and 200 Ω) create voltage drops in response to large ESD currents, further protecting the amplifiers.

The DC level of all amplifier input pins should be within ±400 mV of ground. This prevents the ESD diodes from becoming significantly forward biased and passing current. As long as the voltage across the diodes does not exceed 400 mV, the resulting current will be less than 20 nA. The reference electrode on the RHA2116 and RHA2132 has 6x more ESD diodes than the amplifier input pins, so input bias current due to excursions away from ground will be 6x larger on this pin.



*The **VESD** pin should normally be tied to ground for safety and noise reasons.* A high-energy ESD event could potentially short out any ESD diode. If **VESD** is tied to ground, then severe damage to any diode will only short the associated electrode to ground. Since any tissue contacted by electrodes should be grounded, no DC current will flow into the tissue. If, instead, **VESD** is tied to a voltage above ground, no significant current will flow under normal conditions since the corresponding diode will be reverse biased. However, if that diode is damaged in an ESD event, the voltage at **VESD** will be tied directly to the electrode, possibly resulting in high DC currents and tissue damage.

The voltage on **VESD** is capacitively coupled to the amplifier input through the capacitance of the reverse-biased ESD diode, so any voltage on this pin should be free of AC noise. Otherwise, noise will be injected directly into the amplifier input (and the electrode). For these reasons, it is strongly recommended to tie the **VESD** pin to ground (**AGND** and **DGND**).

The only time it may be useful to tie **VESD** to a higher potential is during electrode activation (see below). **VESD** should never be tied to voltages higher than V_{DD}.

Electrode Impedance Test

All RHA2000-series chips have built-in circuitry that gives selectable access directly to any of the amplifier input pins for the purpose of measuring the impedance of electrodes connected to the chip. Additional off-chip circuitry providing an AC current waveform is needed to measure electrode impedance (see Application Notes), but the RHA2000-series chips facilitate these measurements by providing a common input pin (**elec_test**) that can be connected to any selected amplifier input pin.

The figure below shows a detailed schematic of the amplifier array input circuitry on the RHA2116; input circuitry for the RHA2216 and RHA2132 are similar. Transistor switches S0 through S15 can be closed to connect one or all amplifiers to the auxiliary input pin **elec_test**. If the digital input **test_en** is held low, all switches remain open. This is the normal mode of operation for the chip.

If **test_en** is pulled high, then the switch corresponding to the amplifier that is currently selected for observation on the **MUX_out** pin (using either the random access or sequential access methods discussed above) is closed, and that amplifier's input is connected to the **elec_test** pin. This mode of operation should be used for measuring the impedance of individual electrodes. If an AC current waveform (with zero DC level) is applied to the **elec_test** pin, then the resulting voltage waveform (amplified by 200) may be observed on the **MUX_out** pin. The impedance of the electrode may then be calculated as the ratio of peak voltage to peak current.

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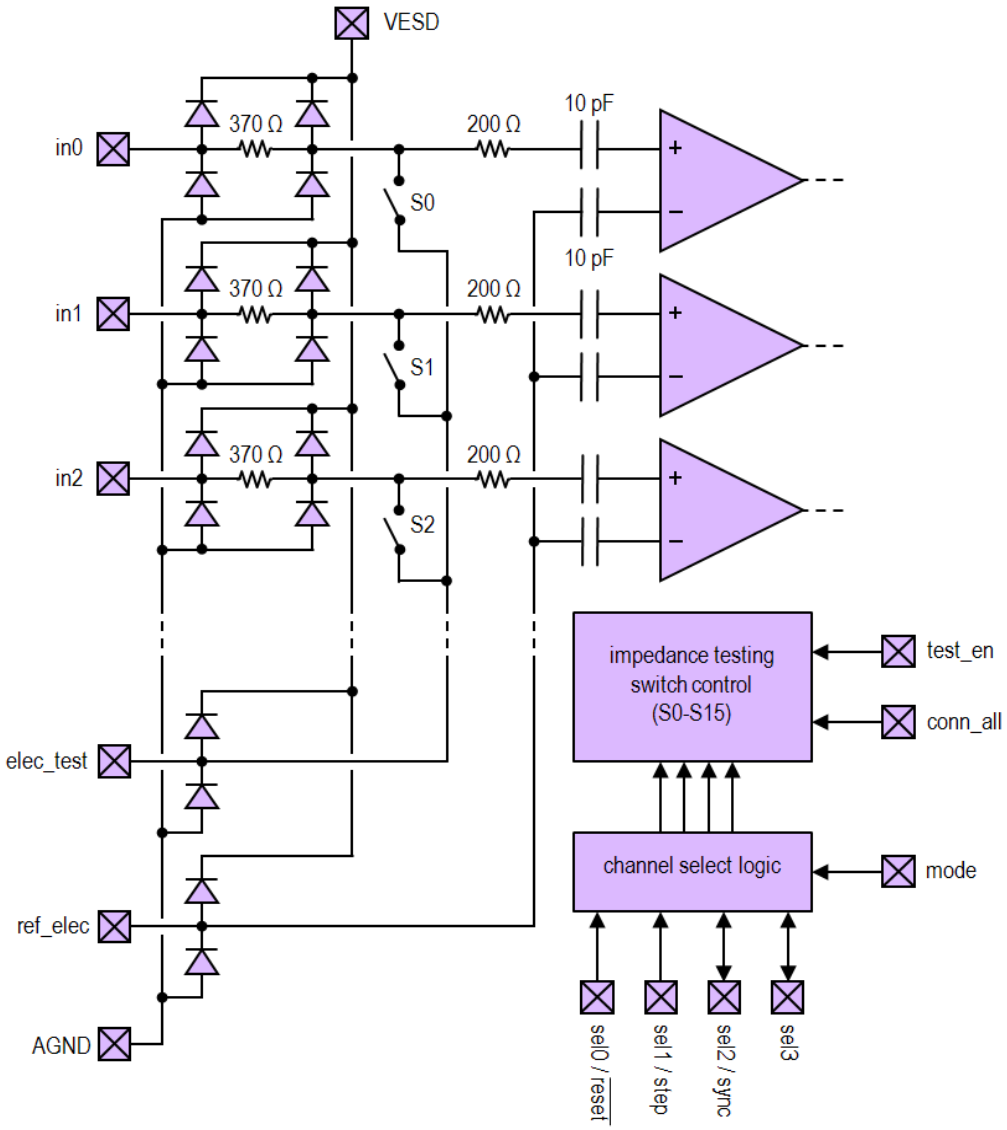


Note that this technique requires small currents, as the RHA2000-series amplifiers saturate for input voltages larger than ±5 mV. For example, a 1 nA peak current will elicit a 1 mV peak voltage with an electrode impedance of 1 MΩ.

See the Application Notes section below for an example circuit that generates a ±1 nA sine wave at 1 kHz for *in situ* electrode impedance testing.

Alternatively, the voltage on the **elec_test** pin may be measured by other means, even if the on-chip amplifiers have saturated. However, it is important to keep the voltage on this pin within ±400 mV of ground to prevent significant forward biasing of the ESD protection diodes at all input pins.

Note that any impedance measurement will include the capacitance of the on-chip amplifiers (10 pF), the ESD protection diodes (0.4 pF), and approximately 1.6 pF of parasitic capacitance associated with the bond pad and QFN package. This 12 pF of capacitance has an impedance magnitude of 13 MΩ at 1 kHz, and should only affect impedance measurements for relatively high-impedance electrodes. The ESD protection resistors have very small values, and are unlikely to significantly affect impedance measurements of typical electrodes.

The RHA2216 has two independent input pins for each amplifier, so an extra pin called **sel_pol** is provided to select between the positive and negative amplifier input pins during electrode impedance testing. When **test_en** is pulled high, **sel_pol** connects **elec_test** to the positive input terminal (**inX+**) of the selected amplifier if pulled low or the negative input terminal (**inX–**) if pulled high

Electrode Activation

The on-chip switches S0, S1, etc. may also be used to apply DC voltages to selected amplifier input pins in order to activate or electroplate various types of electrodes after they have been connected to the chip. DC voltages are applied through the **elec_test** pin. During this process, **VESD** will need to be connected *temporarily* to a higher voltage (such as V_{DD}) to prevent forward biasing of the ESD protection diodes. Note that the "on" resistance of each on-chip transistor switch (nominally around 400 Ω) increases significantly as the applied DC voltage rises above ground.

If negative voltages need to be applied to the electrodes (relative to some electrolyte) then the electrolyte must temporarily be held at a potential above chip ground. *The DC voltage applied to **elec_test** must remain between chip ground and **VESD** at all times.* Diagrams on the next page show example circuits for applying positive or negative DC voltages to electrodes.

To maintain a precise potential between the electrode to be activated (also called the working electrode) and the electrolyte solution, a three-electrode system should be used, as shown in Figs. A1 and A2. Here, an external operational amplifier is used in concert with a reference electrode (which has zero current passing through it) and a counter electrode (which provides DC current for activation) to maintain a precise electrolyte voltage despite potentials that form at any electrode/electrolyte interface in the presence of DC current. The external op amp should be powered from a dual-polarity power supply (e.g., ±5 V) since negative voltages may be needed on the counter electrode to maintain the desired electrolyte voltage.

The process of electroplating does not require an exact potential between the working electrode and the electroplating solution, so a simpler two-electrode system may be used (see Figs. A3 and A4).

If both the **test_en** and **conn_all** pins are pulled high, all switches are closed simultaneously. This connects all amplifier inputs to the **elec_test** pin in parallel. This mode of connectivity may be used to activate or electroplate all electrodes in an array concurrently. The **conn_all** pin *cannot* be used to test the impedance of all electrodes simultaneously; rather, it shorts all electrodes together, so any impedance measurements would return the impedance of all electrodes in parallel. Note that the **conn_all** pin is not available on the RHA2216 chip.

Example Circuits for Electrode Activation or Electroplating

Connecting the reference electrode to the **ref_elec** pin on the RHA2116 or RHA2132 during electrode activation or electroplating is optional, and will have no effect on the process. For clarity, these diagrams show only a single electrode tied to pin **inX** and assume that this channel has been selected either by random or sequential access, or by pulling **conn_all** high to activate all channels concurrently. (On the RHA2216, **sel_pol** must also be set correctly to select either the positive or negative input.) Once activation or electroplating is complete, **VESD** should be tied to ground before using the chip to observe biological signals.

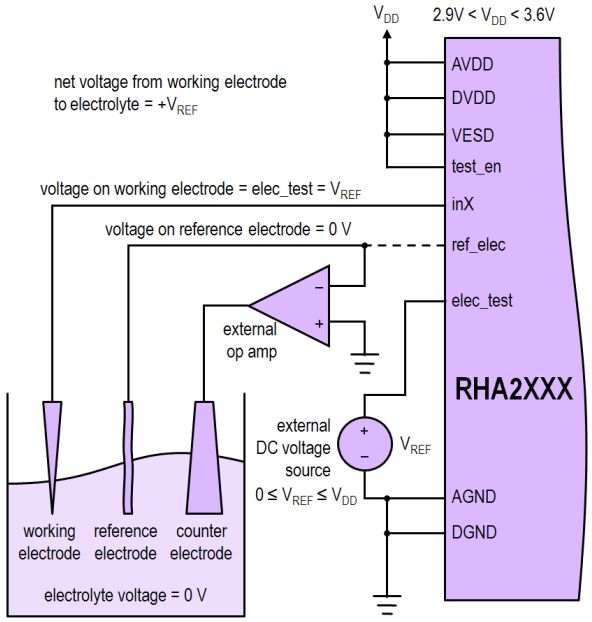


Figure A1. Electrode activation using a three-electrode setup to apply a positive voltage of $+V_{REF}$ (relative to the electrolyte solution) to an electrode connected to channel 0.

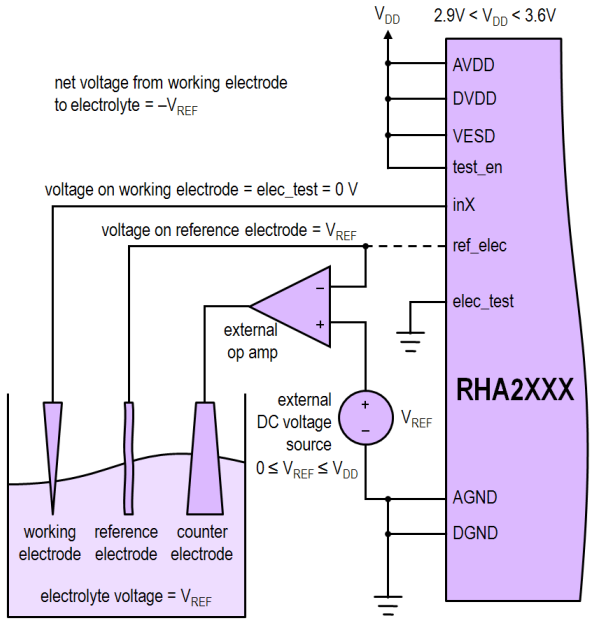


Figure A2. Electrode activation using a three-electrode setup to apply a negative voltage of $-V_{REF}$ (relative to the electrolyte solution) to an electrode connected to channel 0.

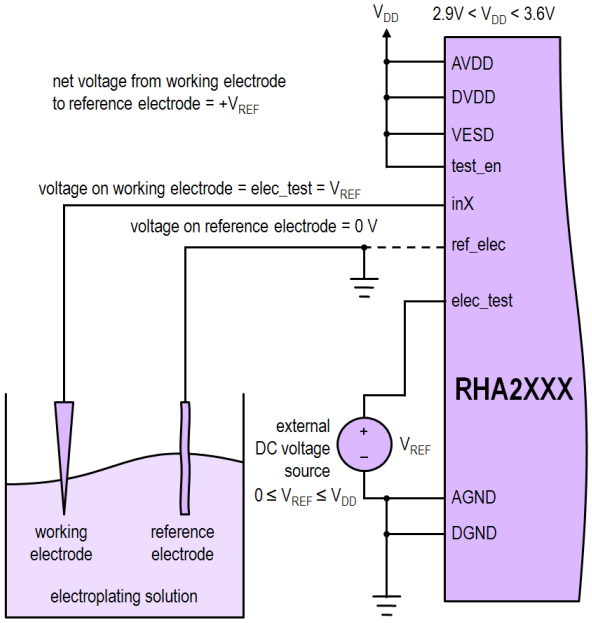


Figure A3. Electroplating using a two-electrode setup to apply a positive voltage of $+V_{REF}$ (relative to the reference electrode) to an electrode connected to channel 0.

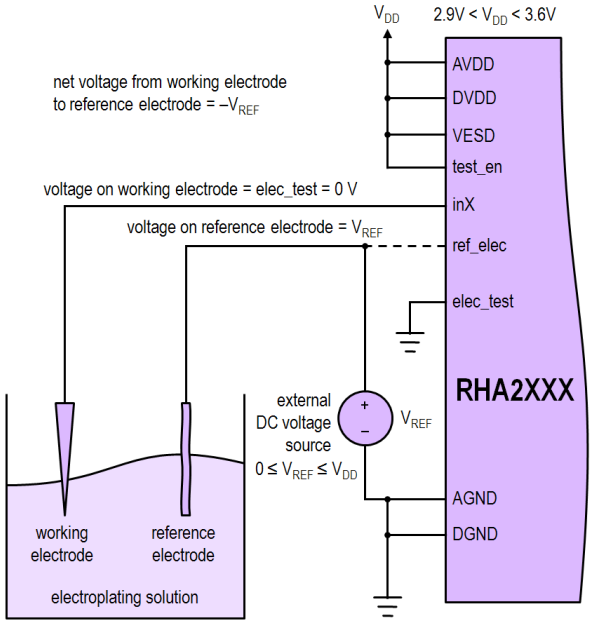
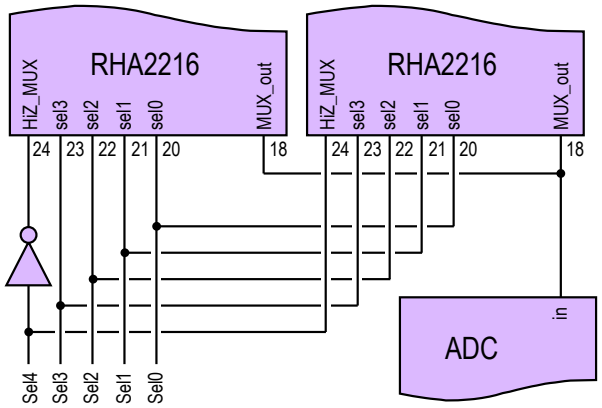


Figure A4. Electroplating using a two-electrode setup to apply a negative voltage of $-V_{REF}$ (relative to the reference electrode) to an electrode connected to channel 0.

Application Notes

MULTIPLE AMPLIFIER CHIPS SHARING ONE ADC

Multiple 16-channel chips (RHA2116 or RHA2216) can be connected in parallel to create recording systems with 32 or more channels that use only one analog-to-digital converter (ADC). The output pins of multiple chips can be connected in parallel (as shown below) as long as only one of the chips has its **HiZ_MUX** signal pulled low. The other chips should have **HiZ_MUX** driven high to keep their outputs in a high-impedance state so that only one chip drives the shared output pins at any time.



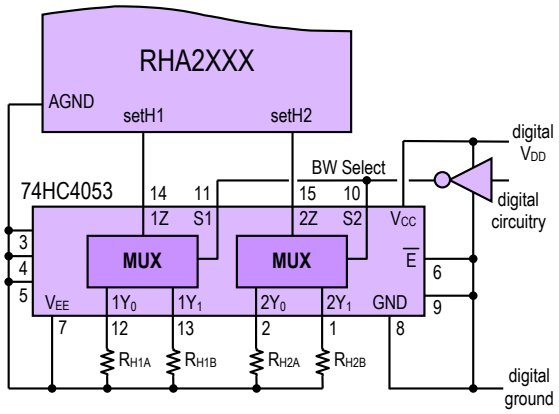
In the example shown above, an inverter (e.g., 74HC04) is added to create a 5-bit address bus to select between one of 32 amplifiers across two RHA2216 chips. Slightly more complex logic could be used to create a 4-chip, 64-channel recording system with a 6-bit address bus used to select amplifiers.

Ultimately, the finite MUX settling time will limit the number of amplifier chips that can be tied in parallel and sampled with a shared ADC. Note that the resistors R_{H1}, R_{H2}, and R_L *cannot* be shared between multiple RHA2116 or RHA2216 chips, and must be replicated for each chip.

The RHA2132 does not have a **HiZ_MUX** pin, so this technique cannot be used with this chip.

PROGRAMMABLE AMPLIFIER BANDWIDTH

The upper and lower bandwidths of RHA2000-series amplifiers may be made digitally controllable by using standard analog multiplexer (MUX) integrated circuits such as the 74HC4051 (an 8-to-1 analog MUX), the 74HC4052 (a dual 4-to-1 analog MUX), or the 74HC4053 (a triple 2-to-1 analog MUX). These ICs are compatible with 2.9V – 3.6V power and logic levels. An example using a 74HC4053 to select between two different amplifier upper bandwidths is shown below.



Two of the three 2-to-1 multiplexers in the 74HC4053 are used to select either resistors R_{H1A} and R_{H2A} (when the digital signal BW Select is low) or resistors R_{H1B} and R_{H2B} (when BW Select is high) to set the bandwidth of the RHA2000-series amplifiers. If more than two bandwidth settings are desired, a 74HC4052 can be used to select between four different resistor pairs, or two 74HC4051 chips can be used to select between eight different resistor pairs.

For finer bandwidth control, "digital potentiometer" ICs could be used for R_{H1}, R_{H2}, and R_L. However, care should be taken to ensure that the parasitic capacitance on pins 8-10 does not exceed 50 pF, or amplifier oscillations may occur. Consult the datasheets of potential digital potentiometer ICs for capacitance specifications.

BUILT-IN ELECTRODE IMPEDANCE TESTING

A simple circuit may be added to the **elec_test** pin of a RHA2000-series chip to facilitate *in situ* measurement of electrode impedances. As discussed in the Electrode Impedance Test section above, if the pin **test_en** is pulled high, an AC current applied to **elec_test** is routed directly to the input pin of the selected amplifier. The resulting voltage can be observed through the on-chip amplifiers as long as it stays within the specified ±5 mV range.

The circuit shown below creates a ±1 nA 1 kHz sine wave current through capacitor C_1. This AC current can be used to measure electrode impedances as high as 5 MΩ given the ±5 mV input voltage limit of the on-chip amplifiers. A digital 1 kHz square wave must be generated externally and supplied to the circuit composed of R_1-R_4 and C_1-C_3. The following table gives appropriate values of R_1 depending on the amplitude of the 1 kHz square wave:

1 kHz VOLTAGE	R_1
3.0 V	15.0 kΩ
3.3 V	16.9 kΩ
5.0 V	26.7 kΩ

The RC network formed by R_1-R_4 and C_2-C_3 attenuates and filters this square wave to produce a ±15.9 mV 1 kHz sine wave on the left side of C_1. At 1 kHz C_1 has an impedance of 15.9 MΩ, so a ±1 nA current flows into the **elec_test** pin. If **test_en** is high, this current is routed to the input pin of the selected amplifier. The optional circuit consisting of D_1, C_4, and R_5 can be used to activate **test_en** whenever a 1 kHz square wave is applied to the circuit. (This eliminates the need for a separate wire to supply the **test_en** signal.) When the square wave is removed and replaced by a steady logic low signal (i.e., GND), **test_en** goes low within approximately 10 ms. Any Schottky diode with a forward voltage (V_f) less than 400 mV and a maximum reverse voltage ($V_{r\text{-}max}$) greater than 4.0 V can be used for D_1.

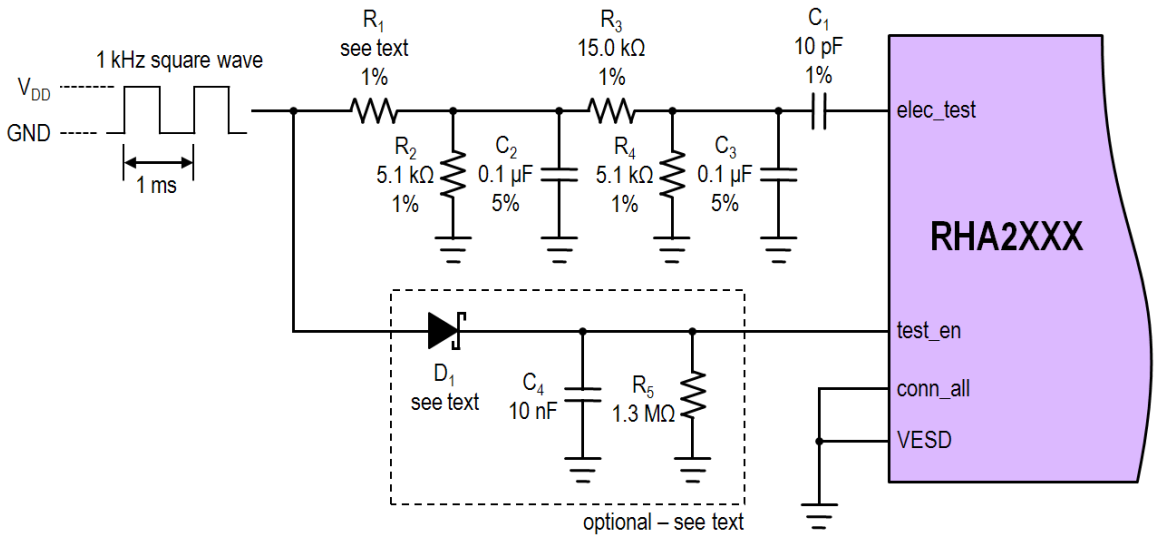
Note that the component values for R_1-R_4 and C_2-C_3 are only valid for 1 kHz operation, which is the most common frequency used for electrode impedance measurements. In applications where electrodes must be tested at a different frequency (e.g., when f_H < 1 kHz), contact Intan Technologies for recommended component values.

In PCB design, R_3, R_4, C_3, and C_1 should be placed as close to the RHA2000-series chip as possible.

When the ±1 nA current is applied to a selected electrode, a 1 kHz signal will appear on the corresponding amplifier output. The amplitude of this voltage signal (referred to the electrode) is equal to the electrode impedance multiplied by 1 nA. For example, a 100 kΩ electrode will produce a ±100 µV sine wave, referred to the amplifier input. After the 200x gain of the amplifier, a ±20 mV sine wave (40 mV peak-to-peak) will appear at **MUX_out**. This ±1 nA current can be used to measure electrode impedances down to roughly 20 kΩ (producing a voltage of ±20 µV at the amplifier input) while maintaining a reasonable signal-to-noise ratio. If other interfering frequencies (e.g., 50/60 Hz) are present, it may be necessary to use off-line filtering to isolate the amplitude of the 1 kHz signal.

If low-impedance electrodes (Z_E < 500 kΩ) are used exclusively, it is recommended to use a 100 pF capacitor for C_1. This increases the test current to ±10 nA, so a 100 kΩ electrode will produce a ±1 mV sine wave at the amplifier input. C_1 can further be increased to 1000 pF to measure electrode impedances below 50 kΩ with better resolution.

As discussed in the Electrode Impedance Test section above, any impedance measurement will also include the capacitance of the on-chip amplifiers (10 pF), the ESD protection diodes (0.4 pF), and approximately 1.6 pF of parasitic capacitance associated with the bond pad and QFN package. This 12 pF of parasitic capacitance has an impedance magnitude of Z_P = 13 MΩ at 1 kHz, and appears in parallel with the actual electrode impedance Z_E. From the total measured impedance Z_M, the true electrode impedance can be calculated by $Z_E = (Z_P Z_M) / (Z_P - Z_M)$.



SOFTWARE OFFSET REMOVAL

As discussed in the Analog Multiplexer Output section above, each amplifier channel has some small random DC offset in the range of ±100 µV, referred to the amplifier input. At the **MUX_out** signal, this leads to an offset of ±20 mV in the baseline level of different amplifier channels. These offsets may be removed in software after digitization by implementing a digital high-pass filter at some low frequency below the value of f_L used on the RHA2000-series amplifier.

A single-pole high-pass filter is easy to implement in software and requires little computational power. The pseudo-code to implement a single-pole high-pass filter is shown below:

```
double sample, state, waveform;

state = 0.0;
do {
  sample = read_one_sample_from_ADC();
  waveform = sample - state;
  state = B*sample + A*state;
}
```

Here, the variable `sample` is used to store the current ADC result, and `state` is the state variable of the filter. The output of the filter is `waveform`, which is updated to a new value with each pass through the infinite loop.

To design this high-pass filter for a particular cutoff frequency f_L', the constants `A` and `B` must be set using the following equations:

$$A = \exp(-2\pi f_L' / f_{sample})$$

$$B = 1 - A$$

where f_{sample} is the ADC sampling rate for each channel and exp(x) is the exponential function e^x. For example, if we sample each amplifier channel at 7.5 kSamples/s and we wish to implement a 0.1-Hz high-pass filter to remove residual baseline offsets, we should use A = exp(–2π × 0.1 / 7500) = 0.99991623 and B = 0.00008377. Double precision floating point variables are recommended for this algorithm.

NOTCH FILTER FOR LINE NOISE ATTENUATION

A notch filter to reduce 50/60 Hz line noise may be implemented as a second-order IIR filter. While the theory behind such filters is complicated, the implementation of a practical notch filter is quite straightforward.

Suppose the latest three samples of our waveform (the input to the notch filter) are called x[t], x[t-1], and x[t-2]. A notch filter can be implemented using the following equation at each point in time:

$$y[t] = b_2 \cdot x[t-2] + b_1 \cdot x[t-1] + b_0 \cdot x[t] - a_2 \cdot y[t-2] - a_1 \cdot y[t-1]$$

where y[t] is the output of the notch filter at time t. The constants a_1, a_2, b_0, b_1, and b_2 are calculated as follows:

$$a_1 = b_1 = -(1 + d^2) \cdot \cos(2\pi \cdot f_N / f_{sample})$$

$$a_2 = d^2$$

$$b_0 = b_2 = (1 + d^2) / 2$$

where

$$d = \exp(-\pi \cdot BW / f_{sample})$$

Here, f_N is the desired notch frequency (e.g., 60 Hz in America; 50 Hz in Europe), f_{sample} is the ADC sampling rate, and BW is the bandwidth of the notch or "bandstop" filter. Setting BW very low may sound like a good idea, but very small values here will lead to a long settling time for the filter. Selecting a bandwidth of 10 Hz (e.g., filtering out frequencies between 55 Hz and 65 Hz for the 60 Hz notch filter setting) implements a fast-settling filter.

As an example, if we select f_N = 60 Hz, f_{sample} = 25 kHz, and BW = 10 Hz, we get the following constants:

$$a_1 = b_1 = -1.9972627755$$

$$a_2 = 0.9974898815$$

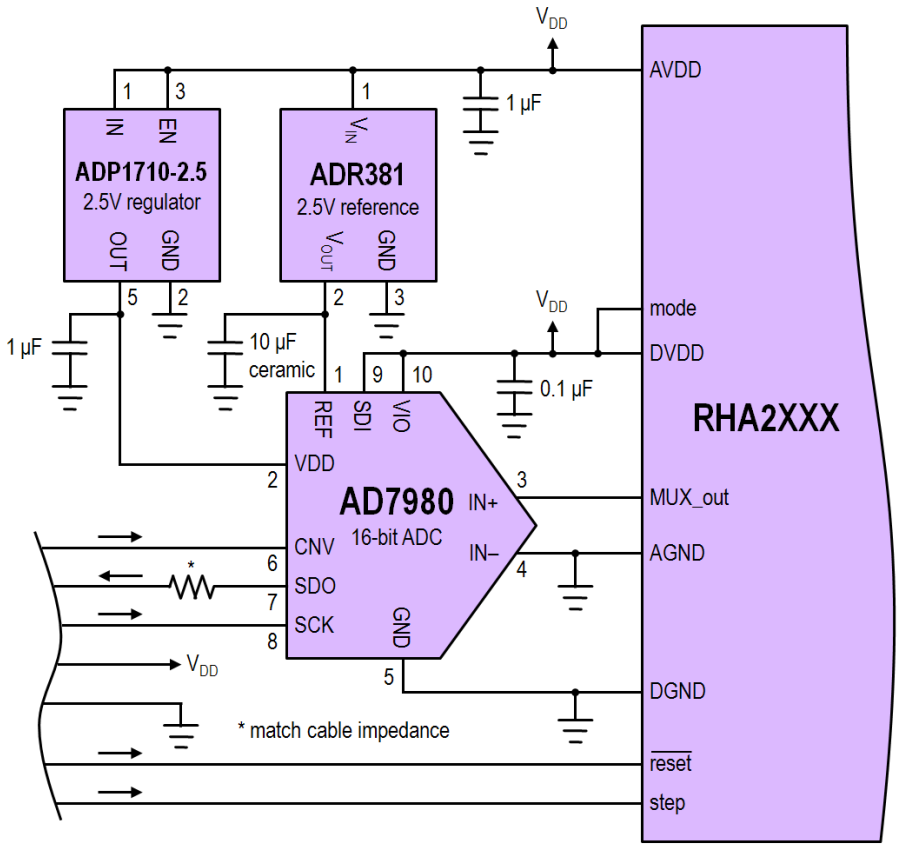
$$b_0 = b_2 = 0.9987449408$$

Here again, the use of high precision floating-point variables is good practice.

ADC INTERFACING EXAMPLE

The schematic below shows an example of using an Analog Devices AD7980 16-bit serial output ADC with an RHA2000-series chip. A 7-wire all-digital interface is shown, but users may wish to add additional wires to allow for a fast settle function and/or electrode impedance testing. Many companies offer 2.5V regulators and voltage references that may be used in place of those shown below.

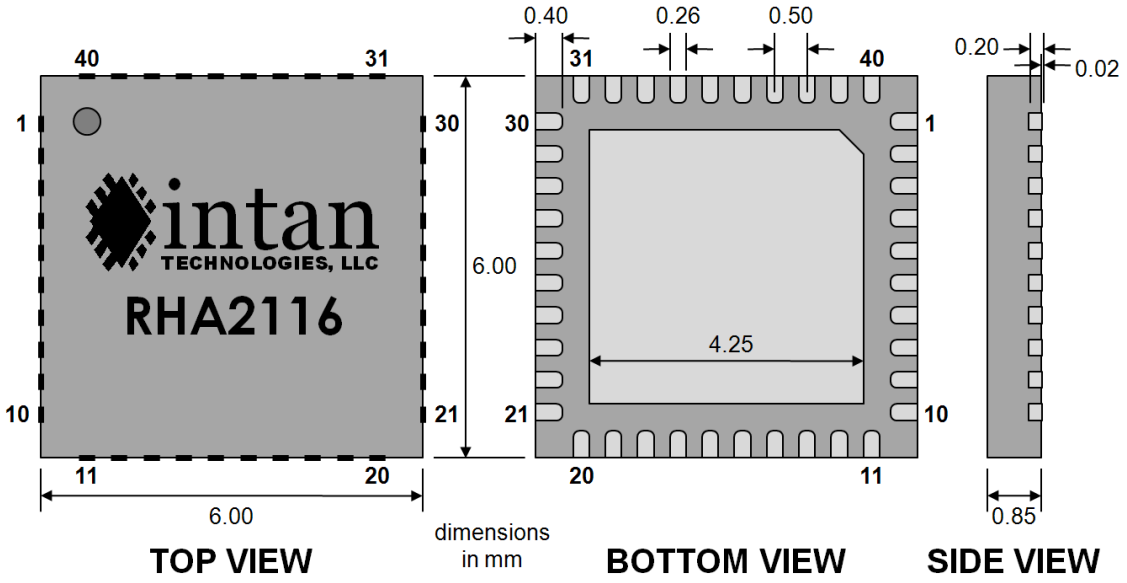
The RHA2000-series chip is configured for serial amplifier access here, so **step** and **reset** are used to cycle through channels. The AD7980 uses one signal to trigger conversion (CNV) and a clock signal (SCK) to clock data out of the serial digital output (SDO). See the AD7980 datasheet from Analog Devices for details on the operation of this high-quality ADC that is available in a small 3mm x 3mm QFN package.



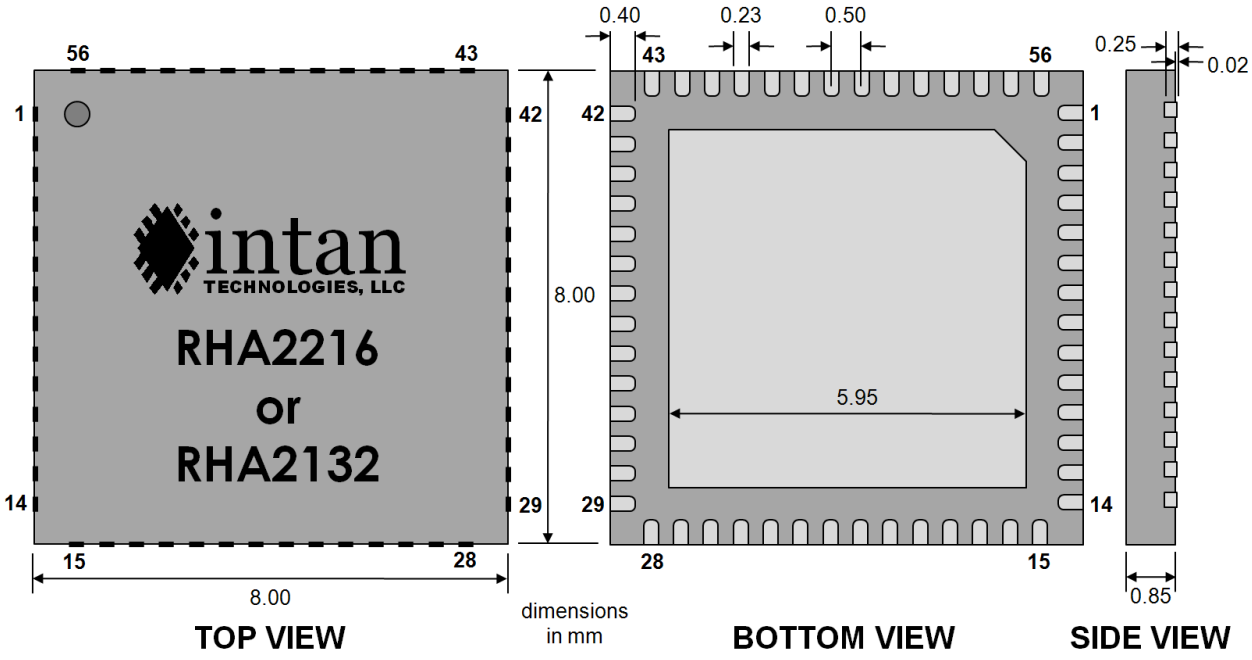
Package Dimensions

All dimensions are in millimeters.

40-Pin QFN Package

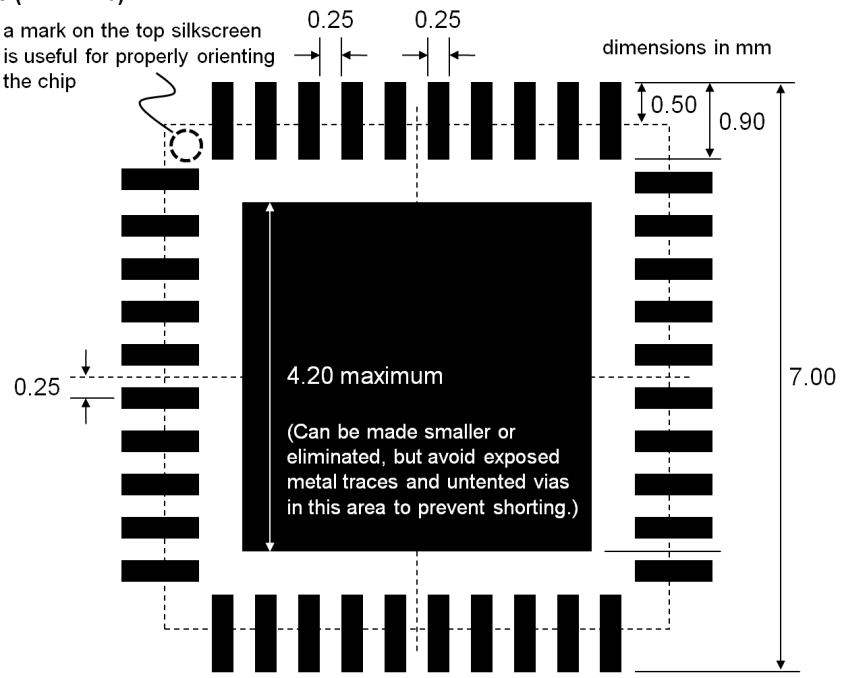


56-Pin QFN Package

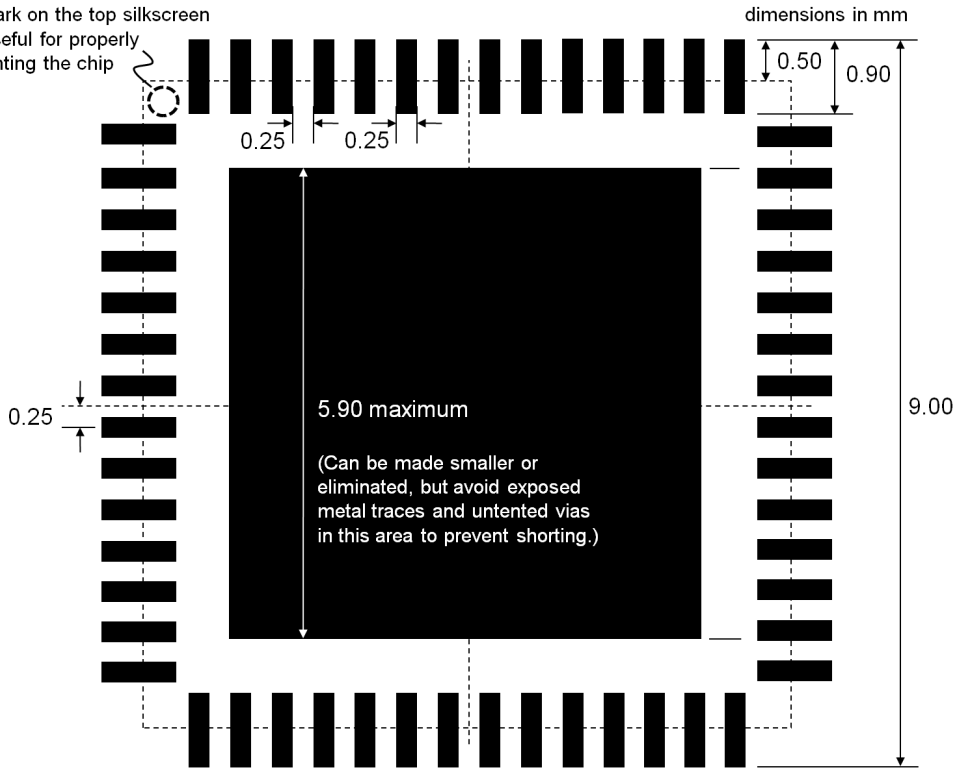


Printed Circuit Board Layout

40-Pin QFN Package (RHA2116)



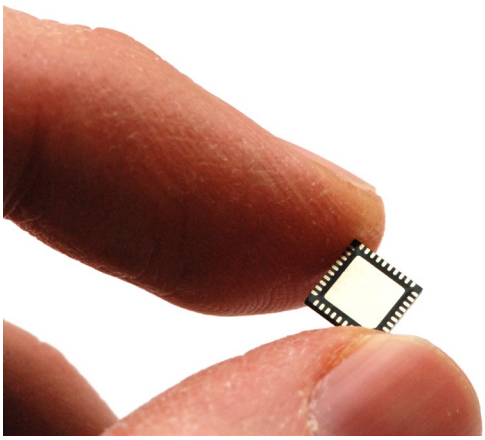
56-Pin QFN Package (RHA2216 and RHA2132)



Note: The center pad is not internally connected but may be soldered for mechanical integrity and tied to ground (GND) for electrical shielding

Pricing Information

See **www.intantech.com** for current pricing. All price information is subject to change without notice. Quantities may be limited. All orders are subject to current pricing at time of acceptance by Intan Technologies. Additional charges may apply for international purchases and shipping.



Contact Information

This datasheet is meant to acquaint engineers and scientists with the general characteristics of the RHA2000 series of integrated bioinstrumentation amplifier array developed at Intan Technologies. We value feedback from potential end users. We can discuss your specific needs and suggest a custom integrated solution tailored to your applications.

For more information, contact Intan Technologies at:

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