

AXI_DAQ_HiCCE128_v0

Register Structure

Read_intan (0x43C00000)

Set which block that need to read

												Read A	Read B	Read C	Read D
Bit 15												Bit 3			Bit 0

Ack_intan_DAQ (0x43C00000 + 4) – Read only

Provide FIFO status (1 – FIFO x full, 0 – FIFO x not full)

												FIFO A	FIFO B	FIFO C	FIFO D
Bit 15												Bit 3			Bit 0
00011000000100100															

Config_Res_intan_x (0x43C00000 + 4*n) (x(n) – A(2), B(3), C(4), or D(5))

Configure the intan block for data acquisition

			BW_SEL(1)	BW_SEL(0)	SETTLE	SEL4	SEL3	SEL2	SEL1	SEL0	TEST_ENB	CONN_ALL	DAQ_Start_Stop	READ_MODE	Virtual_Mode
Bit 15			Bit 12												Bit 0

Bit No.	Name	Value	Description
12-11	BW_SEL	11	Wider frequency bandwidth (0.75 – 20 kHz)
		01	narrower frequency bandwidth (1 kHz)
10	SETTLE	1	Resets all amplifiers to baseline levels
		0	For normal acquisition
9 - 5	SEL4 – SEL0	x	Channel selection bits when READ_MODE = 0 (manual reading)
		x	Ignore when READ_MODE = 1 (Auto reading)
4	TEST_ENB	1	The elec_test pin is connected to the selected amplifier input pin (for electrode impedance measurement)
		0	For normal acquisition
3	CONN_ALL	1	Ties all amplifier input pins to elec_test pin
		0	For normal acquisition
2	DAQ_Start_Stop	1	Start acquisition
		0	Stop acquisition
1	READ_MODE	1	Auto Sequential
		0	Manual
0	Virtual_Mode	1	Pre-defined test pattern or Virtual ADC (Should uncomment the code)

- A – 1010101010101010 (Hex: AAAA)
- B – 1100110011001100 (Hex: CCCC)
- C – 1110001110001110 (Hex: E38E)
- D – 1111000011110000 (Hex: F0F0)

0 Actual Data

SW_Res_DAQ (0x43C00000 + 24) – Read only

Read Board switches

								SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0
Bit - 15								Bit - 7							Bit - 0

LED_Res_DAQ (0x43C00000 + 28)

Set Board leds

								LD7	LD 6	LD 5	LD 4	LD 3	LD 2	LD 1	LD 0
Bit - 15								Bit - 7							Bit - 0

