DATA SHEET

OM6211
48 × 84 dot matrix LCD driver

Product specification
File under Integrated Circuits, IC12

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Philips
Semiconductors

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CONTENTS

1 FEATURES

- Single-chip LCD controller/driver
- 48 row, 84 column outputs
- Display data RAM 48 × 84 bits
- 3-line serial interface, maximum 4.0 Mbit/s
- On-chip:
  - Generation of LCD supply voltage V_{LCD}
  - Generation of intermediate LCD bias voltages
  - Oscillator (requires no external components).
- CMOS compatible inputs
- Mux rate 1 : 48
- Logic supply voltage range V_{DD1} to V_{SS}:
  - 1.7 to 2.3 V.
- Supply voltage range for high voltage part V_{DD2} to V_{SS}:
  - 2.5 to 4.5 V.
- LCD supply voltage range V_{LCD} to V_{SS}:
  - 4.5 to 9.0 V.
- Low power consumption (typical 90 μA), suitable for battery operated systems
- External reset
- Temperature compensation of V_{LCD}
- Temperature range: T_{amb} = –40 to +85 °C
- Manufactured in N-well silicon gate CMOS process.

2 APPLICATIONS

- Battery powered telecommunication systems.

3 GENERAL DESCRIPTION

The OM6211 is a low power CMOS LCD row/column driver, designed to drive a dot matrix graphic display of 48 rows and 84 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The OM6211 interfaces to microcontrollers via a 3-line serial interface.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM6211U/2/F1	tray	chip with bumps in tray	–

5 BLOCK DIAGRAM

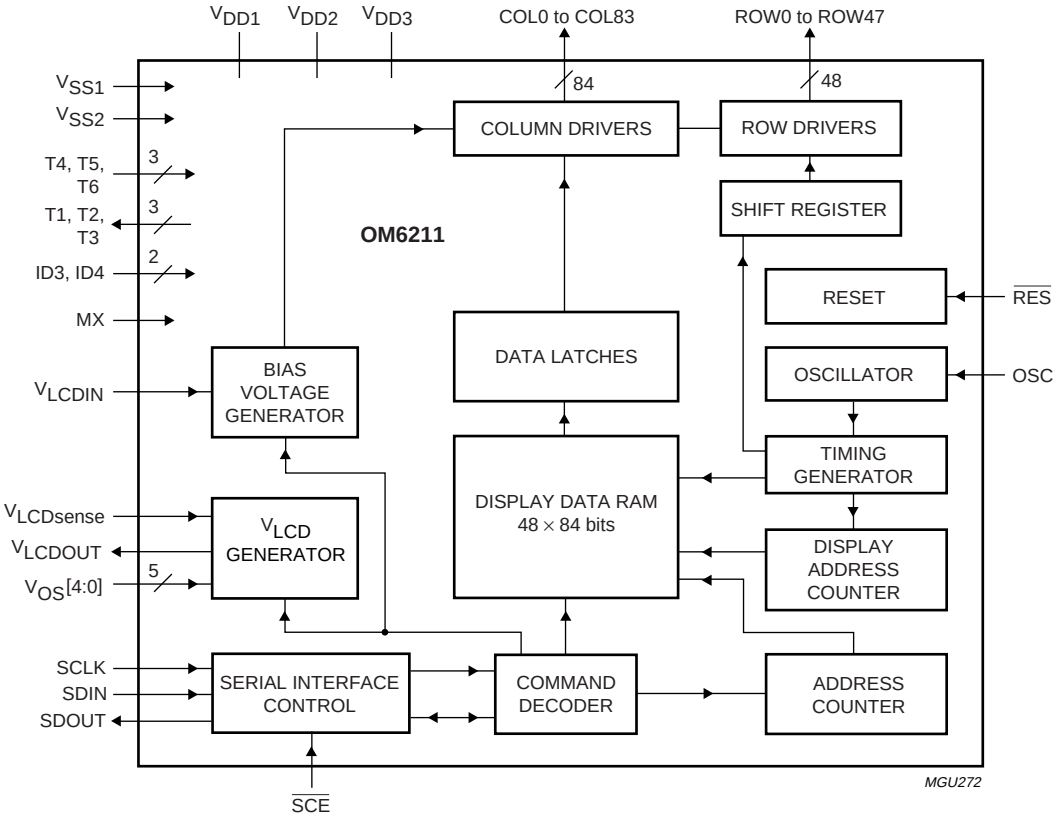


Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD	DESCRIPTION
V_{OS4}	3	input pin 4 for V_{LCD} calibration
V_{OS3}	4	input pin 3 for V_{LCD} calibration
V_{OS2}	5	input pin 2 for V_{LCD} calibration
V_{OS1}	6	input pin 1 for V_{LCD} calibration
V_{OS0}	7	input pin 0 for V_{LCD} calibration
T6	8 to 11	test input 6
$\overline{RES}$	16	external reset input (active LOW)
T5	17	test input 5
T4	18	test input 4
T3	19	test output 3
T2	20	test output 2
T1	21	test output 1
$\overline{SCE}$	22	chip enable input (active LOW)
V_{SS2}	23 to 30	ground
V_{SS1}	31 to 38	ground
OSC	40	oscillator input
SDOUT	41	serial data output
SDIN	42	serial data input
SCLK	43	serial clock input
ID4	44	module identification input
ID3	45	module identification input
MX	46	horizontal mirroring input
V_{DD1}	47 to 52	logic supply voltage
V_{DD2}	53 to 60	voltage multiplier supply voltage
V_{DD3}	61 to 64	voltage multiplier supply voltage
$V_{LCDSENSE}$	65	V_{LCD} generator regulation input
V_{LCDOUT}	66 to 72	V_{LCD} generator output
V_{LCDIN}	73 to 78	LCD supply voltage input
ROW 0 to ROW 23	89 to 112	LCD row driver outputs
COL 0 to COL 83	113 to 196	LCD column driver outputs
ROW 47 to ROW 24	197 to 220	LCD row driver outputs
	1, 12 to 15, 39, 79, 81 to 88 and 221 to 225	dummy pads

7 PIN FUNCTIONS

7.1 ROW 0 to ROW 47 row driver outputs

These pads output the display row signals.

7.2 COL 0 to COL 83 column driver outputs

These pads output the display column signals.

7.3 V_{SS1} and V_{SS2}: negative power supply rails

Negative power supply rails V_{SS1} and V_{SS2} must be connected together, hereafter referred to as V_{SS}. When a pin has to be connected externally to V_{SS}, then pin V_{SS1} should be used.

7.4 V_{DD1} to V_{DD3}: positive power supply rails

Positive power supply rails: V_{DD1} for logic supply, V_{DD2} and V_{DD3} for voltage multiplier. V_{DD2} and V_{DD3} must be connected together, hereafter referred to as V_{DD2}.

7.5 V_{LCDOUT}, V_{LCDIN} and $V_{LCDSENSE}$: LCD power supply

If the internal V_{LCD} generator is used, then all three pins must be connected together. If not (V_{LCD} generator is disabled and an external voltage is applied to V_{LCDIN}), then V_{LCDOUT} must be left open-circuit, $V_{LCDSENSE}$ must be connected to V_{LCDIN}, V_{DD2} and V_{DD3} should be applied according to the specified voltage range. The following settings are also required: HVE = 0, S_1 = 1 and S_0 = 0.

7.6 V_{OS4} to V_{OS0}: calibration inputs

Five pull-up input pins for on-glass V_{LCD} calibration. Each pin may be connected to V_{SS}, which corresponds to logic 0, or left open-circuit, which corresponds to logic 1. All five pins define a 5-bit two's complement number ranging from –16 to 15 decimal (from 10000 to 01111). The default value, with all pins connected to V_{SS}, is 0 decimal (00000).

In order to reduce current consumption related to the pull-up circuitry, the 5-bit number is stored in a register when exiting the Power-down mode. The pull-up circuitry is then disabled. Additionally, the register is refreshed by each HVE command.

7.7 SDIN: serial data input

Serial data input.

7.8 SDOUT: serial data output

Serial data output (3-state, push-pull). If bidirectional data transmission is required, SDOUT and SDIN should be connected externally. If the read mode is not used, SDOUT should be left open-circuit.

7.9 SCLK: serial clock input

Serial clock input.

7.10 $\overline{SCE}$: chip enable

Chip enable input, active LOW. If $\overline{SCE}$ is HIGH, the SCLK pulses are ignored.

7.11 OSC: oscillator

External clock input. The external clock is active only in a special test mode, so in the application it is not available. In normal mode (the internal on-chip oscillator used) this input must be connected to V_{SS}. If OSC is held HIGH, the internal oscillator is disabled.

7.12 MX: horizontal mirroring

Horizontal mirroring input. When MX = 1 the X address space is mirrored.

7.13 ID3 and ID4: identification inputs

LCD module identification inputs. Their state can be read out via the serial interface in order to identify the module version.

7.14 $\overline{RES}$: reset

External reset pin. When LOW the chip will be reset as defined in Section 9.1. The initialization by the $\overline{RES}$ pin is always required during power-on. Timing for the $\overline{RES}$ pin is illustrated in Fig.18.

7.15 T1, T2, T3, T4, T5 and T6: test pins

Test pins. In the application T4 and T5 must be connected to V_{SS}. T1, T2, T3 and T6 must be left open-circuit (T6 has a pull-down resistor).

8 BLOCK DIAGRAM FUNCTIONS

8.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. It has no external components.

8.2 Serial interface control

Detects the serial interface protocol, commands and display data bytes. The serial interface converts the data input (serial-to-parallel) as well as the output bits.

8.3 Command decoder

Decodes all commands.

8.4 Display Data RAM (DDRAM)

The OM6211 contains a 48 × 84 bit static RAM which stores the display data. The RAM is divided into six banks of 84 bytes (6 × 8 × 84 bits). During RAM access, data is transferred to the RAM via the serial interface. There is a direct correspondence between the X address and column output number.

8.5 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations of the serial interface.

8.6 Address Counter (AC)

The address counter assigns addresses to the display data RAM for writing. The X address (X_6 to X_0) and the Y address (Y_2 to Y_0) are set separately. After a write operation the address counter is automatically incremented by 1.

8.7 Display address counter

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The display status (all dots on/off, normal/inverse video) is set via the serial interface.

8.8 V_{LCD} generator

A voltage multiplier (charge pump) with a programmable number of stages. Internal capacitors are used for the voltage multiplier, therefore only decoupling capacitors for V_{LCD} and V_{DD2} are required.

8.9 Bias voltage generator

Generates 4 intermediate LCD bias voltages. The bias system is selectable; see Section 9.9.

8.10 LCD row and column drivers

The OM6211 contains 48 row and 84 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. Figure 3 shows typical waveforms.

8.11 Reset

A reset initializes the chip. It can be performed either by the $\overline{RES}$ pin being LOW or by a command.

9 FUNCTIONAL DESCRIPTION

The OM6211 is a low power LCD driver designed to interface with microprocessors/microcontrollers and a wide variety of LCDs.

The host microprocessor or microcontroller and the OM6211 are connected via a serial interface. The internal oscillator requires no external components. The appropriate intermediate bias voltages for the multiplexed LCD waveforms are generated on-chip. The only other connections required to complete the system are to the power supplies (V_{DD1}, V_{DD2}, V_{SS} and V_{LCD}) and suitable capacitors for decoupling V_{LCD} and V_{DD2}.

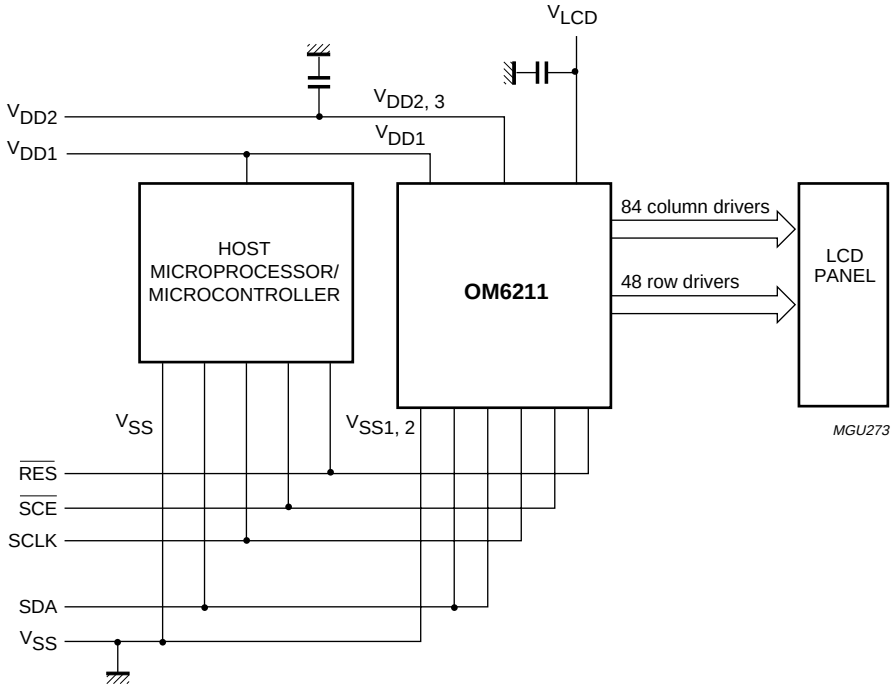


Fig.2 Typical system configuration.

9.1 Reset

The OM6211 has no internal Power-on reset, only external reset and reset by command. After power-on an external reset is required. A reset initiated either from the $\overline{RES}$ pin or by command will initialize the chip to the following starting conditions:

- Power-down mode (DON = 0 and DAL = 1):
  - Internal oscillator stopped
  - The V_{LCD} generator (HV generator) is switched off (HVE = 0) and V_{LCDOUT} is 3-state
  - Display is off and all LCD outputs are internally connected to V_{SS} (DON = 0)
  - Display all points is on (DAL = 1).
- Serial interface initialized; write mode
- Display normal video (E = 0)
- Address counter X_6 to X_0 = 0; Y_2 to Y_0 = 0; display start line Z_5 to Z_0 = 0; no Y mirroring (MY = 0)
- Bias system 1⁄7 (BS_2 to BS_0 = 100)
- V_{LCD} selection V_{PR7} to V_{PR0} = 0
- Voltage multiplication factor 4 (S_1 and S_0 = 10)
- Temperature control mode TC3 (TC_1 and TC_0 = 11)
- Frequency not calibrated and OC = 0
- RAM data is unchanged (after power-up undefined).

9.2 Power-down

The chip is in Power-down mode if the display is off (DON = 0) and display all points is on (DAL = 1), regardless of the order in which both bits are set. During the Power-down mode almost all static currents are switched off (no internal oscillator, no timing and no LCD segment drive system), and all LCD outputs are internally connected to V_{SS}. The V_{LCD} generator is switched off (but HVE is not affected). The serial interface function remains. RAM data is unchanged. When exiting the Power-down mode, the V_{OS} value is stored in a register.

9.3 LCD voltage selector

The practical value for V_{LCD} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast.

9.4 Oscillator

The internal logic operation and the multi-level drive signals of the OM6211 are clocked by the built-in RC oscillator. No external components are required. The oscillator is in operation as long as the chip is not in Power-down mode.

9.5 Timing

The timing of the OM6211 organizes the internal data flow of the device. The timing also generates the LCD frame frequency that is derived from the clock frequency generated by the internal clock generator.

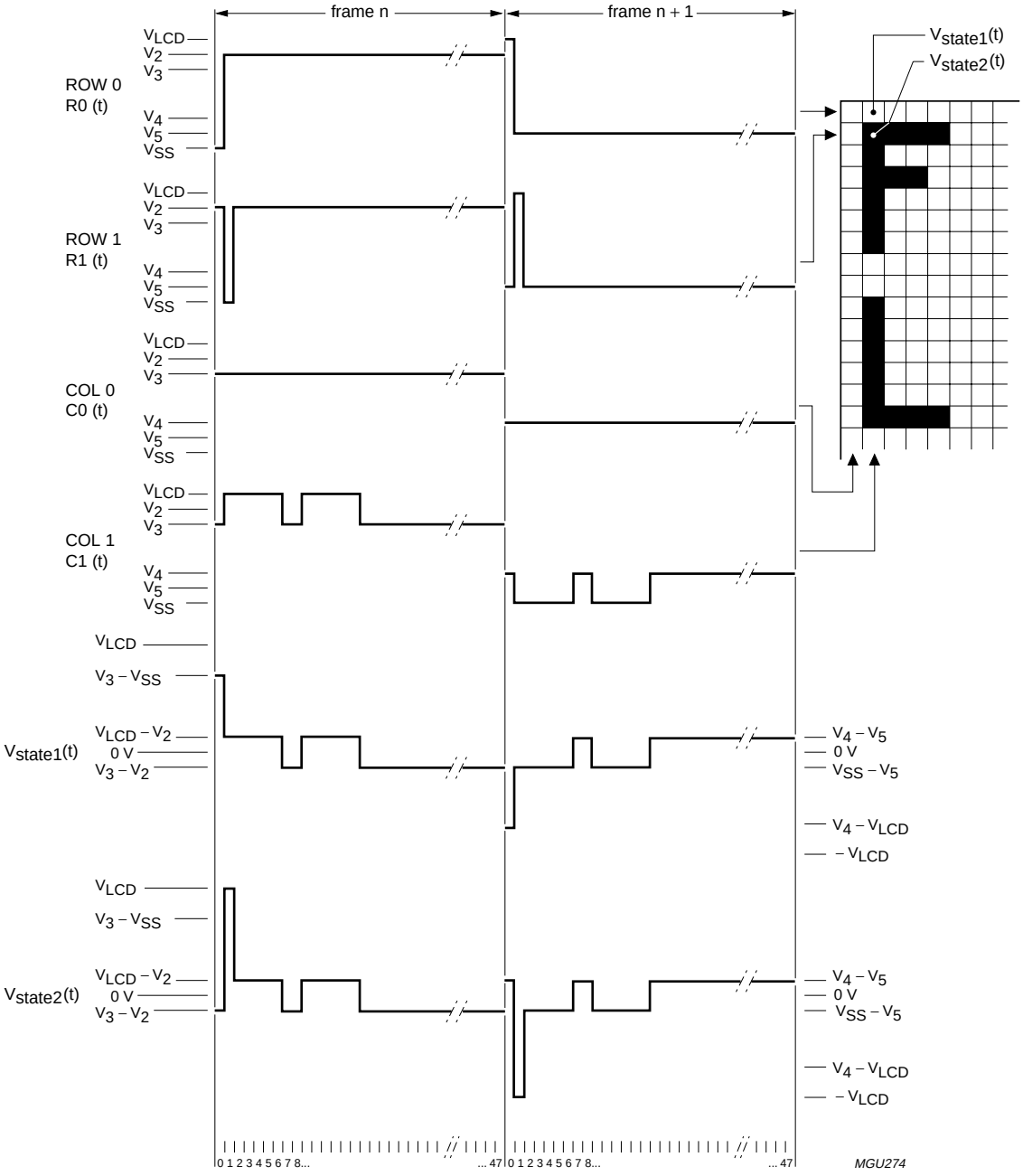
9.6 Column driver outputs

The LCD drive section includes 84 column outputs, which should be connected directly to the LCD. The column output signals are generated in accordance with the multiplexed row signals and with the data in the display latch. If less than 84 columns are required, the unused column outputs should be left open-circuit.

9.7 Row driver outputs

The LCD drive section includes 48 row outputs, which should be connected directly to the LCD. If less than 48 rows are required, the unused row outputs should be left open-circuit.

9.8 Drive waveforms



$V_{state1}(t) = C1(t) - R0(t)$.
$V_{state2}(t) = C1(t) - R1(t)$.

Fig.3 Typical LCD driver waveforms.

9.9 Bias system

The bias voltage levels are set in the ratio of R - R - nR - R - R. Different multiplex rates require different factors of n. This is programmed by BS_2 to BS_0. For optimum bias values, n can be calculated from the following equation:

$n = \sqrt{\text{Mux rate}} - 3$; where Mux rate is 48.

Changing the bias system from the optimum setting will have a consequence on the contrast and viewing angle.

One reason to depart from the optimum would be to reduce the required V_{LCD} voltage. A compromise between contrast and V_{LCD} must be found for any particular application.

In the OM6211 one of three possible values of the bias system can be selected. The value $1/7$ is default.

Table 1 Programming the required bias system

BS_2	BS_1	BS_0	n	BIAS MODE	TYPICAL MUX RATES
0	1	1	4	$1/8$	1 : 55 and 1 : 48
1	0	0	3	$1/7$	1 : 33
1	0	1	2	$1/6$	1 : 24

Table 2 LCD bias voltages for $1/6$ bias, $1/7$ bias and $1/8$ bias.

SYMBOL	BIAS VOLTAGE		
	FOR $1/6$ BIAS	FOR $1/7$ BIAS	FOR $1/8$ BIAS
V1	V_{LCD}	V_{LCD}	V_{LCD}
V2	$5/6V_{LCD}$	$6/7V_{LCD}$	$7/8V_{LCD}$
V3	$4/6V_{LCD}$	$5/7V_{LCD}$	$6/8V_{LCD}$
V4	$2/6V_{LCD}$	$2/7V_{LCD}$	$2/8V_{LCD}$
V5	$1/6V_{LCD}$	$1/7V_{LCD}$	$1/8V_{LCD}$
V6	V_{SS}	V_{SS}	V_{SS}

9.10 Voltage multiplier control

The OM6211 incorporates a software configurable voltage multiplier. After reset ($\overline{RES}$) the voltage multiplier is set to $4V_{DD2}$. Other voltage multiplier factors are set via the serial interface (S_1 and S_0).

Table 3 HV generator multiplication

S_1	S_0	MULTIPLICATION
0	0	$2V_{DD2}$
0	1	$3V_{DD2}$
1	0	$4V_{DD2}$
1	1	not available

9.11 Temperature compensation

Due to the temperature dependency of the liquid crystals viscosity, the LCD controlling voltage (V_{LCD}) must be increased at lower temperatures to maintain optimum contrast. Figure 4 shows V_{LCD} as a function of temperature for a typical high multiplex rate liquid.

In the OM6211 the temperature coefficient of V_{LCD} can be selected from 4 values by setting bits TC_1 and TC_0, see Tables 4 and 8.

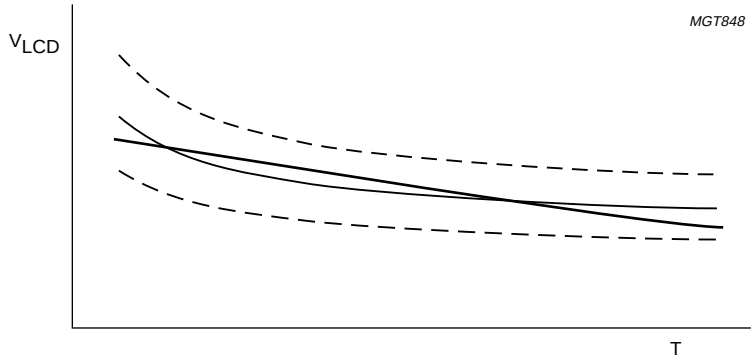


Fig.4 V_{LCD} as a function of liquid crystal temperature (typical values).

9.12 V_{LCD} generator

The binary number V_{OP} representing the operating voltage can be set by the serial interface command and can be adjusted (calibrated) by 5 input pins according to the following formula:

$$V_{OP} = V_{PR} + V_{OS} \quad (1)$$

where:

- V_{PR} is an 8-bit unsigned number set by the serial interface command
- V_{OS} is a 5-bit two's complement number set by the 5 input pins V_{OS4} to V_{OS0}, see Table 9
- V_{OP} is an 8-bit unsigned number used internally for generation of the LCD supply voltage V_{LCD}.

To avoid numerical overflow the allowed values of V_{PR} should be limited to the range 32 to 225 (decimal).

The corresponding voltage at the reference temperature, T_{nom}, can be calculated as follows:

$$V_{LCD(Tnom)} = (a + V_{OP} \times b) \quad (2)$$

The generated voltage at V_{LCD} is dependent on the temperature, programmed Temperature Coefficient (TC) and the programmed voltage at the reference temperature (T_{nom}).

$$V_{LCD} = (a + V_{OP} \times b) \times [1 + TC \times (T - T_{nom})] \quad (3)$$

T_{nom}, a and b for each temperature coefficient are given in Table 4. The maximum voltage that can be generated is dependent on the voltage of V_{DD2} and the display load current.

As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD}, the user has to ensure while setting the V_{PR} register and selecting the Temperature Compensation, that under all conditions and including all tolerances the V_{LCD} limit of maximum 9 V will never be exceeded.

For a particular liquid crystal, the optimum value of V_{LCD} can be calculated for a given multiplex rate. For a Mux rate of 1 : 48, the optimum operating voltage of the liquid crystal can be calculated as follows;

$$V_{LCD} = \frac{1 + \sqrt{48}}{\sqrt{2 \times \left(1 - \frac{1}{\sqrt{48}}\right)}} \times V_{th} = 6.06 \times V_{th} \quad (4)$$

where V_{th} is the threshold voltage of the liquid crystal used.

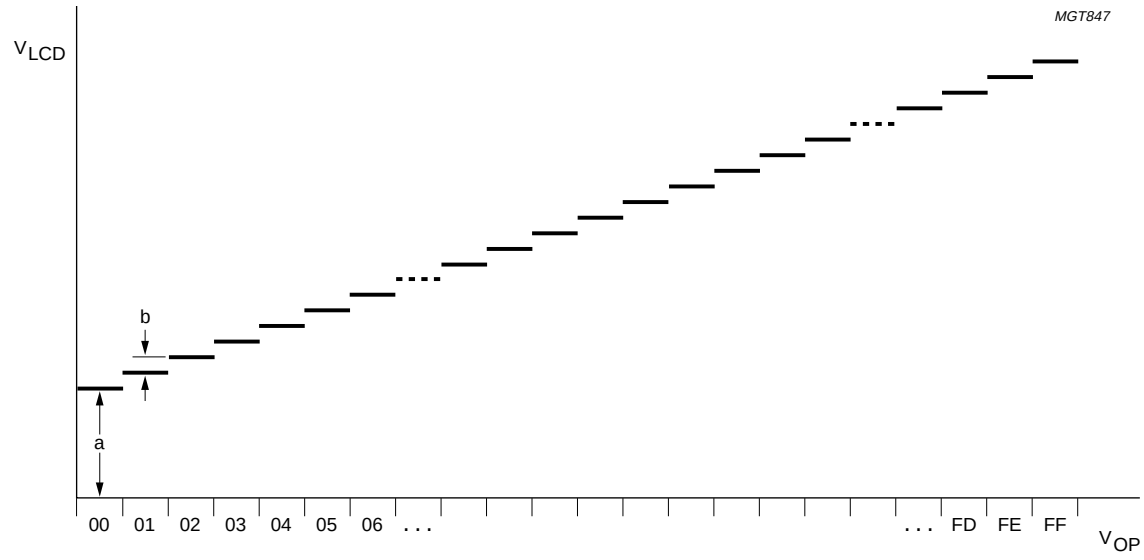
Table 4 Typical values for parameters of the HV generator programming

SYMBOL	TC0	TC1	TC2	TC3	UNIT
a	4.57	4.28	4.04	3.79	V
b	30.0	28.0	26.5	25.0	mV
T_{nom}	27	27	27	27	°C
TC	0	–0.25	–0.5	–0.75	10^{-3}/°C

Example: to achieve V_{LCD} = 8.3 V at temperature T_{nom} for TC3 it is necessary to set V_{PR} = 180 (decimal).

Example for calibration: Before calibration V_{PR} = 180 was applied, but the measured voltage was V_{LCD} = 8.4 V. To decrease V_{LCD} by 100 mV the best value for V_{OS} is –4 decimal (11100 binary in the two's complement notation). So after calibration with V_{OS} = –4 the proper V_{PR} value is still 180.

As V_{OS} is used for calibration and the default value is 0, for selecting the value of V_{PR} it can always be considered that V_{OS} = 0.



V_{OP7} to V_{OP0} programming, (00H to FFH).

Fig.5 V_{LCD} programming of OM6211.

10 INITIALIZATION

10.1 Initialization sequence

After reset ($\overline{RES}$) it is recommended to initialize the V_{LCD} generator using the following sequence; a starting state of HVE = 0, DON = 0 and DAL = 1 is assumed:

1. Set the required V_{OP} and, if required, the voltage multiplier S_1 and S_0
2. Set DAL = 0 to leave the Power-down state (in order to precharge the charge pump V_{LCD} is set to V_{DD2})
3. Wait for at least 1 ms and set HVE = 1 to switch-on the V_{LCD} generator
4. Set DON = 1 to switch the display on.

10.2 Frame frequency calibration (OC)

The OM6211 incorporates frame frequency calibration via software. The calibration is achieved by tuning the internal oscillator. After reset the frame frequency calibration is disabled (OC = 0). The calibration can only be performed if the driver is not in Power-down mode. The calibration is started by setting OC = 1 via the serial interface (start command) and will be stopped by setting OC = 0 (stop command). The time between start and stop of the calibration must be 200 ms to give a frame frequency of 80 Hz. Any variation in calibration time (deviation from 200 ms) results in a corresponding variation in frame frequency. During calibration all other commands are allowed.

The calibration may be repeated and is always performed with the previously calibrated frequency. Through repeated calibrations a better accuracy can be expected and, most especially, the temperature drift can be compensated for. A minimum time delay of 500 ms between consecutive calibration events is necessary (between stop and start).

The calibration will always be performed if the calibration time is between 190 and 210 ms. If, however, the calibration time is lower then 58 ms or higher than 690 ms (or the stop command does not occur at all), the calibration attempt is ignored and the previously selected frequency is maintained. For the remaining values of the calibration time (from 58 to 190 ms and from 210 to 690 ms) it cannot be determined if the calibration will be performed or ignored.

11 ADDRESSING

11.1 Addressing

Data is downloaded in bytes into the RAM matrix of OM6211 as illustrated in Figs 6 and 7. The display RAM has a matrix of 48 × 84 bits. The columns are addressed by the address pointer. The address ranges are X = 0 to 83 (1010011) and Y = 0 to 5 (101). Addresses outside of these ranges are not allowed. The X address increments after each byte (see Fig.7). After the last X address (X = 83) X wraps around to 0 and Y increments to address the next row. After the very last address (X = 83 and Y = 5) the address pointers wrap around to address X = 0 and Y = 0.

The selection of the MX input allows horizontal mirroring: when MX = 1, the X address space is mirrored (see Fig.6). When MX = 0 the mirroring is disabled. MX affects data only during writing to the RAM, so after a change of MX RAM data must be re-written.

The MY bit allows vertical mirroring: when MY = 1, then the Y address space is mirrored. MY does not affect the RAM content, but defines the way RAM data is written to the display. A change of MY has an immediate effect on the display.

Vertical scrolling of the display is controlled by the Z address with a range from 0 to 47 (101111). The Z address specifies which rows of the RAM are output to which row outputs. The value of the Z address defines which row of the RAM will be ROW 0 of the display (which is normally the top row of the display). For example, if the Z address is set to 31 (see Fig.8), then the data displayed on ROW 0 of the display will be the data from ROW 31 of the RAM and the data on ROW 1 will be from ROW 32 of the RAM. When the MY is active (MY = 1), then the Z address defines which row of the RAM is written to ROW 47 of the display. For example, when the Z address is set to 31, ROW 47 of the display would come from ROW 31 of the RAM and ROW 46 from ROW 32 of the RAM (see Fig.9).

The Z address does not affect the RAM content, but defines the way RAM data is written to the display. A change of Z address has an immediate effect on the display.

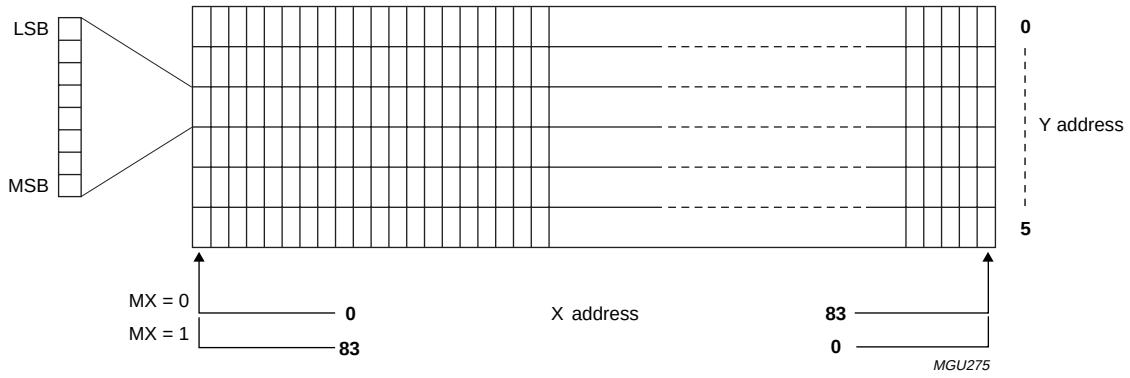


Fig.6 RAM format, addressing.

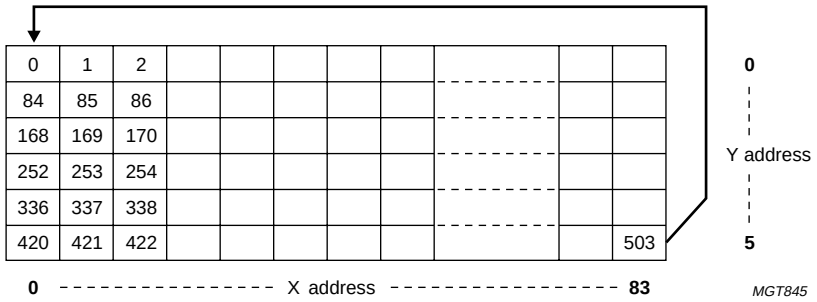


Fig.7 Sequence of writing data bytes into RAM.

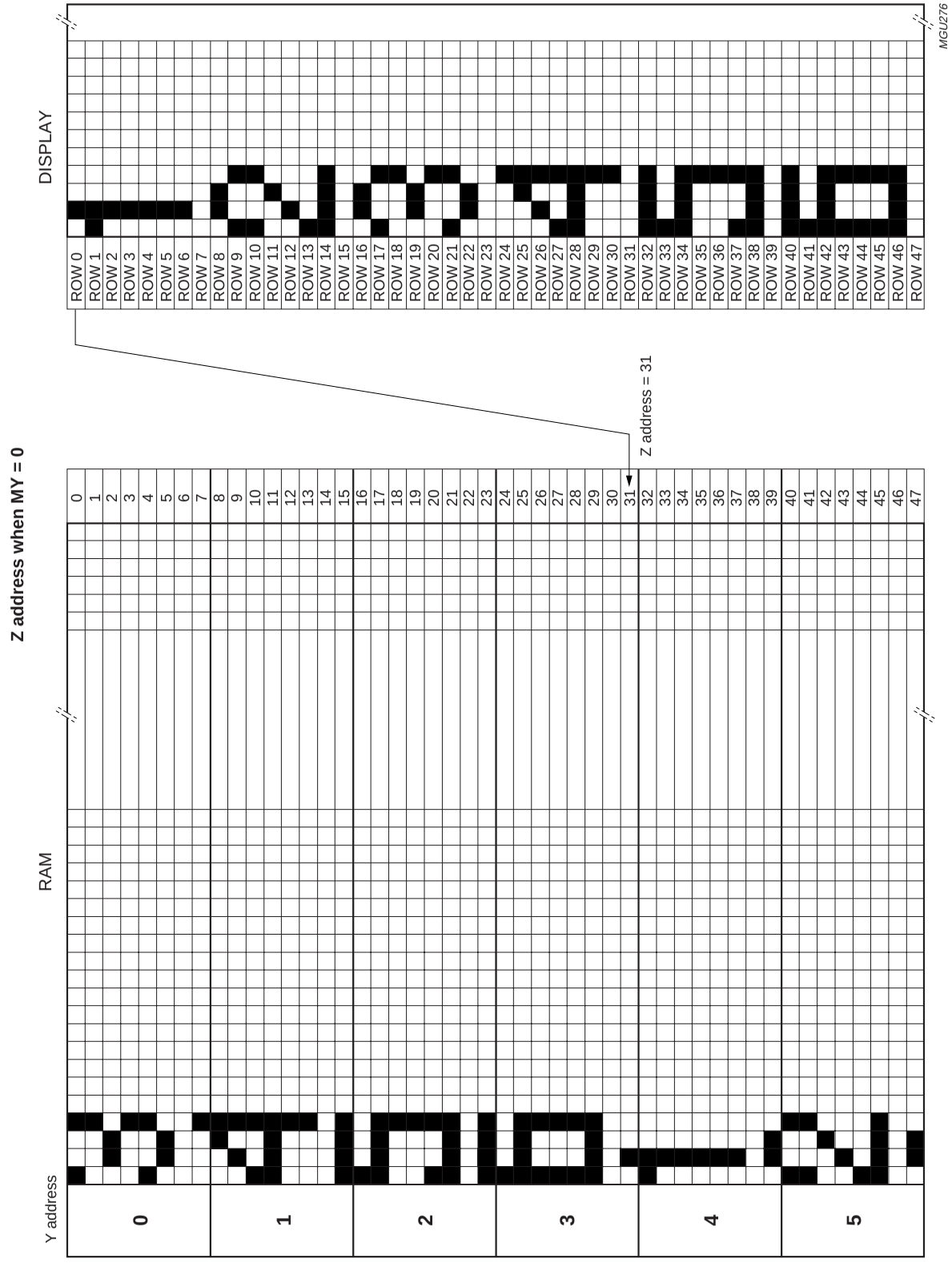


Fig.8 Programming the Z address when MY = 0.

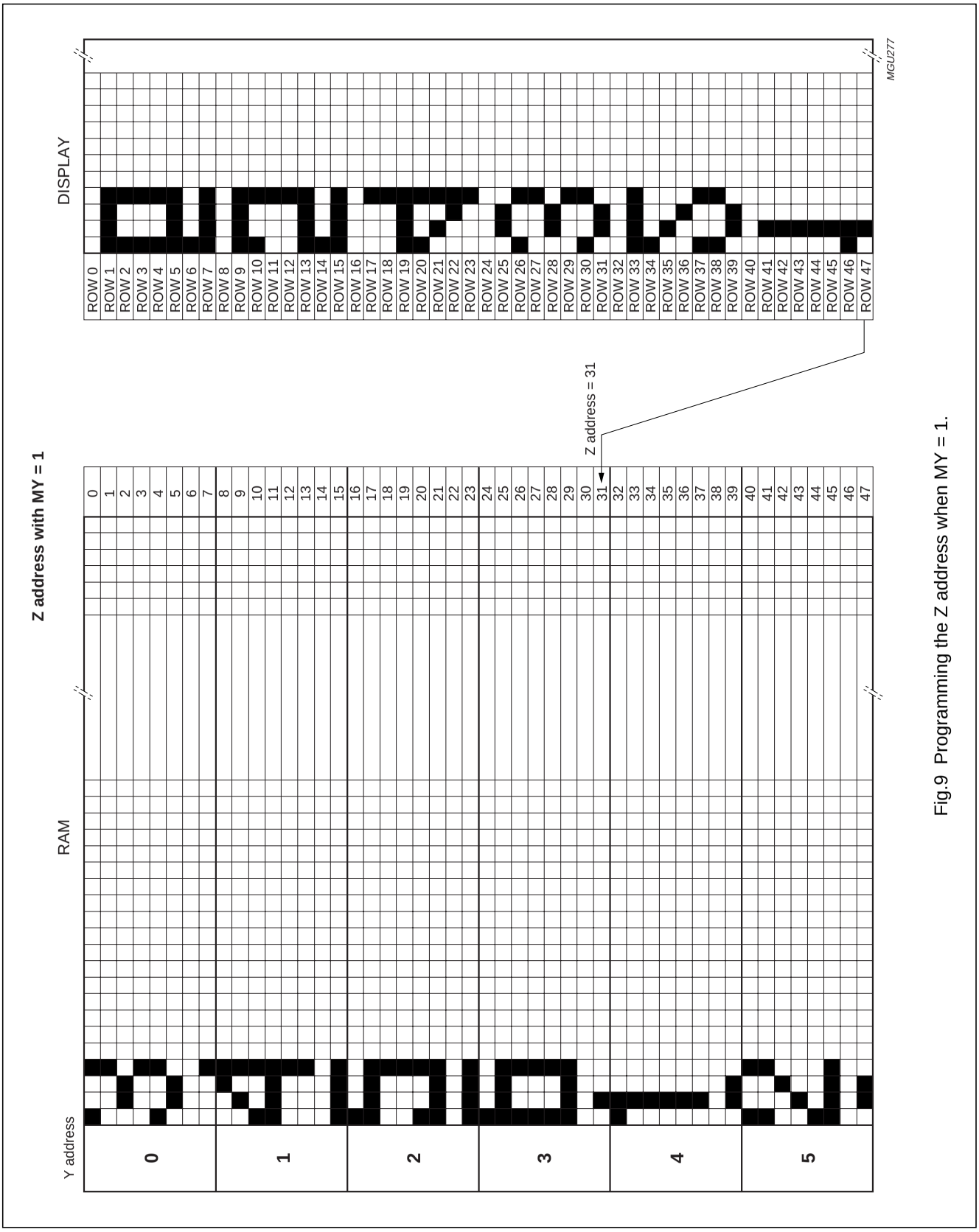


Fig.9 Programming the Z address when MY = 1.

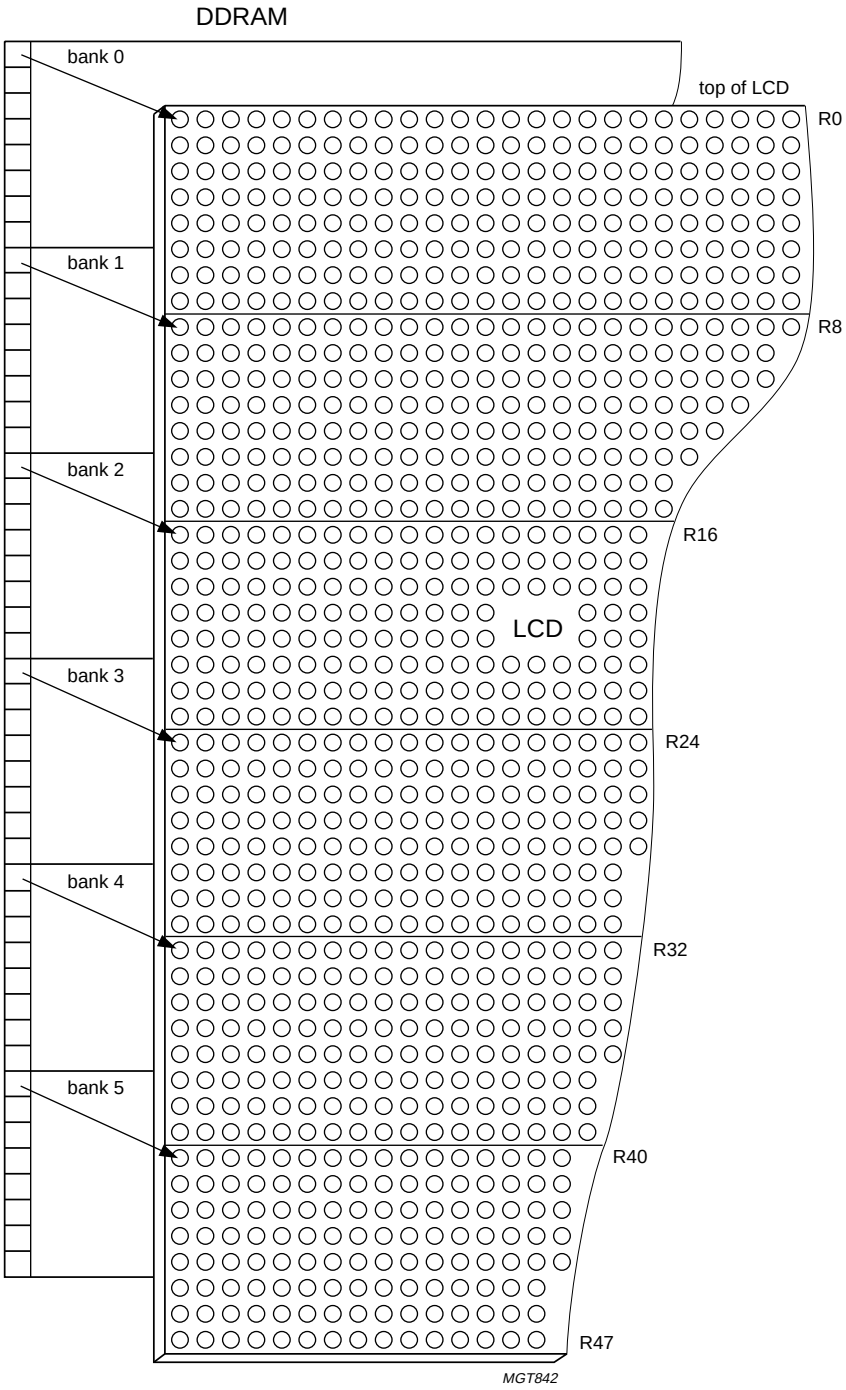


Fig.10 DDRAM to display mapping (Z = 0).

11.2 Serial interface

The serial interface is a 3-line bidirectional interface for communication between the microcontroller and the LCD driver chip. The 3 lines are: $\overline{SCE}$ (chip enable), SCLK (serial clock) and SDA (serial data). The OM6211 is connected to SDA by two pins: SDIN (data input) and SDOUT (data output) connected together.

11.2.1 WRITE MODE

The write mode of the interface means that the microcontroller writes commands and data to the OM6211. Each data packet contains a control bit D/$\overline{C}$ and a transmission byte. If D/$\overline{C}$ is LOW, the following byte is interpreted as a command byte (see Table 5). If D/$\overline{C}$ is HIGH, the following byte is stored in the display data RAM. After every data byte the address counter is incremented automatically. Figure 11 shows the general format of the write mode and the definition of the transmission byte. Every command can be sent in any order to the OM6211. The MSB of a byte is transmitted first. The serial interface is initialized when $\overline{SCE}$ is HIGH. In this state, SCLK clock pulses have no effect and no power is consumed by the serial interface. A falling edge on $\overline{SCE}$ enables the serial interface and indicates the start of a data transmission.

Figures 12, 13 and 14 show the protocol of the write mode:

- When $\overline{SCE}$ is HIGH, SCLK clocks are ignored: during the HIGH time of $\overline{SCE}$ the serial interface is initialized (see Fig.12)
- At the falling edge of $\overline{SCE}$ SCLK must be LOW (see Fig.16); for the transmission of each data bit a rising and then a falling edge of SCLK is necessary
- SDIN is sampled at the rising edge of SCLK
- D/$\overline{C}$ indicates whether the byte is a command (D/$\overline{C}$ = 0) or RAM data (D/$\overline{C}$ = 1); it is sampled with the first rising SCLK edge
- If $\overline{SCE}$ stays LOW after the last bit of a $\overline{command}$ or data byte, the serial interface expects the D/$\overline{C}$ bit of the next byte at the next rising edge of SCLK (see Fig.13)
- A reset pulse with $\overline{RES}$ interrupts the transmission. The data being written into the RAM may be corrupted. The registers are cleared. If $\overline{SCE}$ is LOW after the rising edge of $\overline{RES}$, the serial interface is ready to receive the D/$\overline{C}$ bit of a command or data byte (see Fig.14).

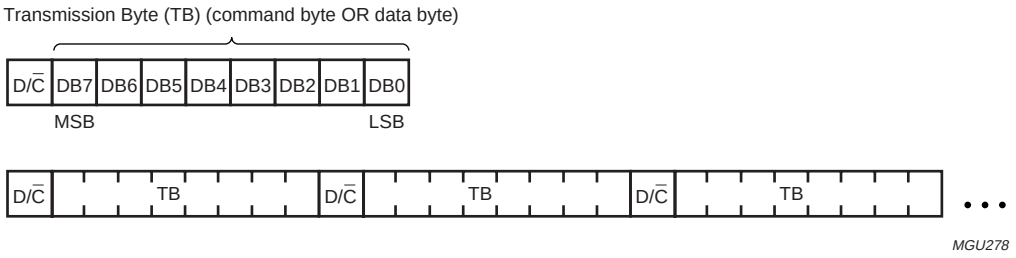


Fig.11 Serial data stream, write mode.

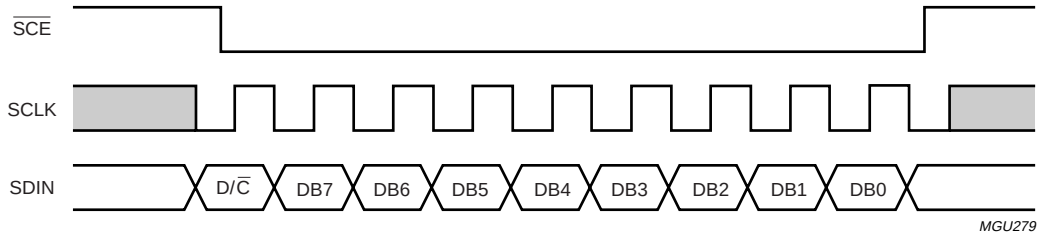


Fig.12 Write mode: a control bit followed by a transmission byte.

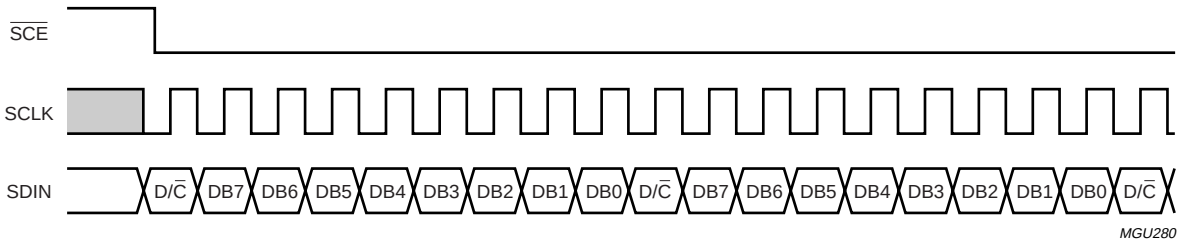


Fig.13 Write mode: transmission of several bytes.

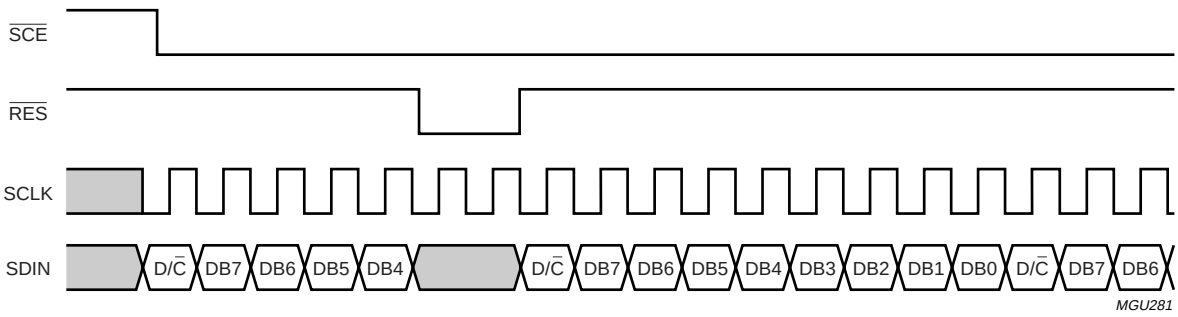


Fig.14 Write mode: interrupted by reset ($\overline{RES}$).

11.2.2 READ MODE

In the read mode of the interface the microcontroller reads data from the OM6211. To do so the microcontroller first has to send the read status command, and then the following byte is transmitted in the opposite direction (using SDOUT). After that $\overline{SCE}$ is required to go HIGH before a new command is sent (see Fig.15).

The OM6211 samples the SDIN data on the rising edges of SCLK, but shifts SDOUT data on the falling edges of SCLK. Thus the microcontroller is supposed to read SDOUT data on the rising edges of SCLK.

After the read status command has been sent, the SDIN line must be set to 3-state not later then the falling SCLK edge of the last bit (see Fig.15).

The 8th read bit is shorter than the others because it is terminated by the rising edge of SCLK (see Fig.15). The last rising edge of SCLK sets SDOUT to 3-state after the delay time t_3 (see Section 10.1 and Fig.17).

There are 5 bits of information only that can be read by the microcontroller (see Table 7). Two of them are chip identification bits and have fixed values. The next two bits are LCD module identification bits and can be set by connecting the ID3 and ID4 pins to V_{DD1} or V_{SS}. The fifth bit is the V_{LCD} voltage monitor bit VM.

It indicates that the charge pump is running and the voltage level of V_{LCD} is sufficient to provide enough contrast of the display (VM = 1). If the V_{LCD} generator cannot produce a voltage defined by V_{OP}, then VM = 0.

VM has a valid value 45 ms after a delay time of approximately 45 ms starting from the time the V_{LCD} generator has been switched on (by setting HVE = 1). This delay time is dependent on the external V_{LCD} decoupling capacitor (here 100 nF is assumed).

For more details concerning the VM bit see Chapter 22

The reading out of the chip identification bits and module identification bits can be used to implement different initialization schemes for different applications. The reading out of VM can be used to check the proper electrical contacts of the LCD module.

One read status command enables one status bit to be read, i.e. 5 commands are needed to read the status of all 5 bits. The first 4 bits of the read byte (DB7 to DB4) are always equal to the corresponding status bit and the next 4 bits (DB3 to DB0) are equal to the complement of this bit.

As stated before the SDOUT data is supposed to be read on the rising edge of SCLK. Care must be taken, however, when running the SCLK at maximum frequency. Because of the access time limit t_2 (see Section 10.1 and Fig.17) it might happen that the first bits of each group (DB7 to DB4 and DB3 to DB0) are not valid at the time of the corresponding SCLK edges. Thus it is recommended to read the bits DB4 and DB0 only.

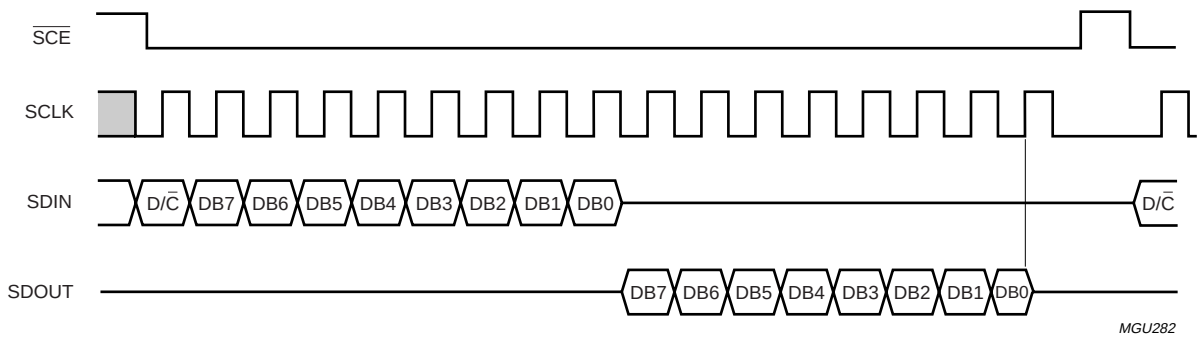


Fig.15 Read mode.

12 INSTRUCTIONS

12.1 Instruction set

Table 5 Instruction set; see notes 1 and 2 and Table 6

INSTRUCTION	D/$\overline{C}$	COMMAND BYTE								DESCRIPTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
NOP	0	1	1	1	0	0	0	1	1	no operation
Reset	0	1	1	1	0	0	0	1	0	software reset
Write data	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	write data to display RAM
Read status	0	1	1	0	1	1	SB2	SB1	SB0	read one of the status bits; Table 7
Display control	0	1	0	1	0	1	1	1	DON	display on/off; see Table 6
	0	1	0	1	0	0	1	1	E	normal, reverse mode; see Table 6
	0	1	0	1	0	0	1	0	DAL	all pixels on; see Table 6
	0	1	1	0	0	MY	X	X	X	mirror Y; see Table 6
Address commands	0	1	0	1	1	0	Y_2	Y_1	Y_0	set Y address; $0 \leq Y \leq 5$
	0	0	0	0	1	X	X_6	X_5	X_4	set X address; $0 \leq X \leq 83$
	0	0	0	0	0	X_3	X_2	X_1	X_0	set X address; $0 \leq X \leq 83$
Display start line	0	0	1	Z_5	Z_4	Z_3	Z_2	Z_1	Z_0	set start ROW, $0 \leq Z \leq 47$
Power control	0	0	0	1	0	1	HVE	HVE	HVE	switch HV-gen on/off; see Table 6
	0	1	0	0	V_{PR4}	V_{PR3}	V_{PR2}	V_{PR1}	V_{PR0}	lower part of V_{PR}; see Equation (1)
	0	0	0	1	0	0	V_{PR7}	V_{PR6}	V_{PR5}	higher part of V_{PR}
Frame calibration	0	1	0	1	0	1	1	0	OC	frame calibration start/stop; see Table 6
TC	0	0	0	1	1	1	0	TC1	TC0	set temperature coefficient; see Table 8
HV-gen stages	0	0	0	1	1	1	1	S_1	S_0	set multiplication factor; see Table 3
Bias system	0	0	0	1	1	0	BS2	BS1	BS0	set bias system; see Table 1
Test	0	1	0	1	0	1	0	0	X	reserved
	0	1	1	1	0	1	0	1	1	reserved
	0	1	1	1	0	1	1	0	0	reserved
	0	1	1	1	0	1	1	1	1	reserved

Notes

1. X = don’t care.
2. DB7 = MSB.

Table 6 Explanations for symbols in Table 5

BIT	LOGIC 0	LOGIC 1
DON	display off	display on
DAL	normal display (only if DON = 1)	all pixels on
E	normal display	inverse video mode (only if DAL = 0)
HVE	V_{LCD} generator (HV generator) is switched off	V_{LCD} generator is switched on
MY	no Y mirroring	Y mirroring
OC	stop frame frequency calibration	start frame frequency calibration

Table 7 Read status

SB[2:0]	READ STATUS BIT	DESCRIPTION
010	ID1	fixed value 0
011	ID2	fixed value 1
100	ID3	defined by input pin ID3
101	ID4	defined by input pin ID4
111	VM	VM

Table 8 Temperature coefficients

TC[1:0]	
00	TC0
01	TC1
10	TC2
11	TC3

Table 9 V_{OS} values in two's complement notation

DECIMAL	BINARY
+0	00000
+1	00001
+2	00010
+3	00011
+4	00100
+5	00101
+6	00110
+7	00111
+8	01000
+9	01001
+10	01010
+11	01011
+12	01100
+13	01101
+14	01110
+15	01111
–1	11111
–2	11110
–3	11101
–4	11100
–5	11011
–6	11010
–7	11001
–8	11000
–9	10111
–10	10110
–11	10101
–12	10100
–13	10011
–14	10010
–15	10001
–16	10000

13 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); notes 1 and 2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+6.5	V
V_{LCD}	LCD supply voltage		–0.5	+9.0	V
V_I, V_O	input/output voltage (any input/output)		–0.5	V_{DD1} + 0.5	V
I_I, I_O	DC input or output current		–10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	note 3	–50	+50	mA
P_{tot}	total power dissipation per package		–	100	mW
P_{out}	power dissipation per output		–	10	mW
T_{stg}	storage temperature		–65	+150	°C
$T_{j(max)}$	maximum junction temperature		–	150	°C

Notes

1. Stresses above those listed under limiting values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are referenced to V_{SS} unless otherwise specified.
3. V_{SS} = 0 V.

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

15 DC CHARACTERISTICS

V_{DD1} = 1.7 to 2.3 V; V_{DD2} = 2.5 to 4.5 V; V_{SS} = 0 V; V_{LCD} = 4.5 to 9.0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD1}	logic supply voltage		1.7	1.8	2.3	V
V_{DD2}, V_{DD3}	supply voltage for voltage multiplier	note 1	2.5	2.78	4.5	V
V_{LCDIN}	LCD supply voltage		4.5	–	9.0	V
V_{LCDOUT}	generated LCD supply voltage	note 2	6.8	–	–	V
$V_{LCD(tol)}$	tolerance of generated V_{LCD}	with calibration; note 3	–70	–	+70	mV
I_{DD1}	V_{DD1} supply current	Power-down mode; note 4	–	2	10	µA
		normal mode; note 4	–	12	–	µA
I_{DD2}, I_{DD3}	V_{DD2} and V_{DD3} supply current	Power-down mode; note 4	–	1	5	µA
		normal mode; note 4	–	78	–	µA
$I_{DD(tot)}$	total supply current (V_{DD1} and V_{DD2}, V_{DD3})	normal mode; note 4	–	90	–	µA
		normal mode; note 5	–	120	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	–	V_{DD1}	V
I_{OL}	LOW-level output current (SDOUT)	V_{OL} = 0.4 V; V_{DD1} = 1.8 V	0.5	–	–	mA
I_{OH}	HIGH-level output current (SDOUT)	V_{OH} = 1.4 V; V_{DD1} = 1.8 V	–	–	–0.5	mA
I_L	leakage current	$V_I = V_{DD1}$ or V_{SS}	–1	–	+1	μA
Column and row outputs						
$R_{o(col)}$	column output resistance (COL 0 to COL 83)	note 6	–	4	20	kΩ
$R_{o(row)}$	row output resistance (ROW 0 to ROW 47)	note 6	–	4	20	kΩ
$V_{bias(col)}$	bias tolerance (COL 0 to COL 83)		–100	0	+100	mV
$V_{bias(row)}$	bias tolerance (ROW 0 to ROW 47)		–100	0	+100	mV
Calibration inputs						
$R_{on(Vos)}$	external resistance between a V_{OS} pin and the V_{SS1} pin for logic 0		–	–	10	kΩ
$R_{off(Vos)}$	external resistance between a V_{OS} pin and the V_{SS1} pin for logic 1		5	–	–	MΩ

Notes

1. V_{DD2} is always equal V_{DD3}.
2. Conditions are: V_{DD2} = 2.5 V, voltage multiplier = $3V_{DD2}$, bias system 1/6, V_{LCD} output is loaded by 10 μA, T_{amb} = 25 °C.
3. Valid for values of temperature, V_{PR} and TC used at the calibration.
4. Conditions are: V_{DD1} = 1.8 V, V_{DD2} = 2.78 V, V_{LCD} = 6.8 V, voltage multiplier = $3V_{DD2}$, bias system 1/6, inputs at V_{DD1} or V_{SS}, serial interface inactive, internal V_{LCD} generation, V_{LCD} output is loaded by 10 μA; T_{amb} = 25 °C.
5. Conditions are: V_{DD1} = 1.8 V, V_{DD2} = 2.78 V, V_{LCD} = 8.3 V, voltage multiplier = $4V_{DD2}$, bias system 1/7, inputs at V_{DD1} or V_{SS}, serial interface inactive, internal V_{LCD} generation, V_{LCD} output is loaded by 10 μA; T_{amb} = 25 °C.
6. Load current 10 μA, outputs tested one at a time.

16 AC CHARACTERISTICS

V_{DD1} = 1.7 to 2.3 V; V_{DD2} = 2.5 to 4.5 V; V_{SS} = 0 V; V_{LCD} = 4.5 to 9.0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{osc(int)}$	internal oscillator frequency	note 1	–	251	–	kHz
f_{frame}	frame frequency	uncalibrated; note 2	46	80	142	Hz
		calibrated; notes 3 and 4	63	80	97	Hz
		calibrated; notes 3 and 5	75	80	85	Hz
t_{VHRL}	V_{DD1} to $\overline{RES}$ LOW	see Fig.18; note 6	0	–	30	ms
t_{RW}	reset LOW pulse width	see Fig.18	1000	–	–	ns
$t_{R(op)}$	end of reset pulse to interface being operational		–	–	1000	ns
Serial interface timing						
f_{SCLK}	clock frequency		0	–	4.00	MHz
t_{cyc}	clock cycle SCLK		250	–	–	ns
t_{PWH1}	SCLK pulse width HIGH		120	–	–	ns
t_{PWL1}	SCLK pulse width LOW		100	–	–	ns
t_{S2}	$\overline{SCE}$ set-up time		60	–	–	ns
t_{H2}	$\overline{SCE}$ hold time		100	–	–	ns
t_{PWH2}	$\overline{SCE}$ minimum HIGH time		100	–	–	ns
t_{H5}	$\overline{SCE}$ start hold time	note 7	100	–	–	ns
t_{S1}	SDIN set-up time		100	–	–	ns
t_{H1}	SDIN hold time		100	–	–	ns
t_2	SDOUT access time	note 8	0	–	450	ns
t_3	SDOUT disable time		25	–	450	ns
t_4	$\overline{SCE}$ hold time		100	–	–	ns
t_5	$\overline{SCE}$ hold time		20	–	–	ns

Notes

1. $f_{frame} = \frac{f_{osc}}{3136}$
2. Temperature range T_{amb} = –30 to +70 °C.
3. Calibrated at V_{DD1} = 1.8 V and T_{amb} = 25 °C, valid for both OTP calibration and software calibration, exact calibration time assumed.
4. Measured at V_{DD1} = 1.8 V, temperature range T_{amb} = –30 to +70 °C.
5. Measured at V_{DD1} = 1.8 V, T_{amb} = 25 °C.
6. It is recommended that $\overline{RES}$ is LOW before V_{DD1} goes HIGH
7. t_{H5} is the time from the previous SCLK rising edge (irrespective of the state of $\overline{SCE}$) to the falling edge of $\overline{SCE}$ (see Fig.16).
8. Capacitive load at pin SDOUT less than 50 pF.

16.1 Serial interface timing

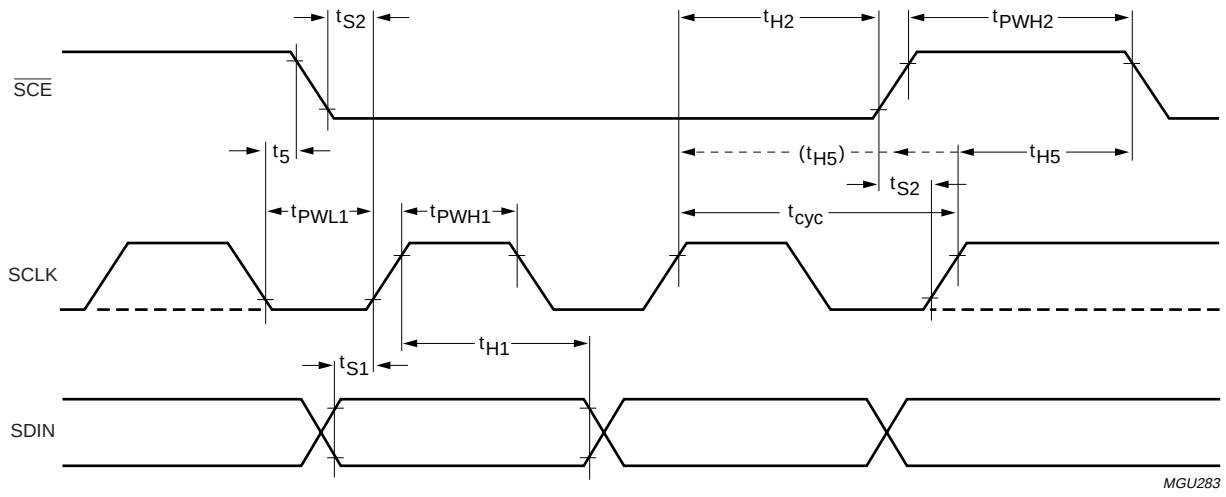


Fig.16 Serial interface timing: write mode.

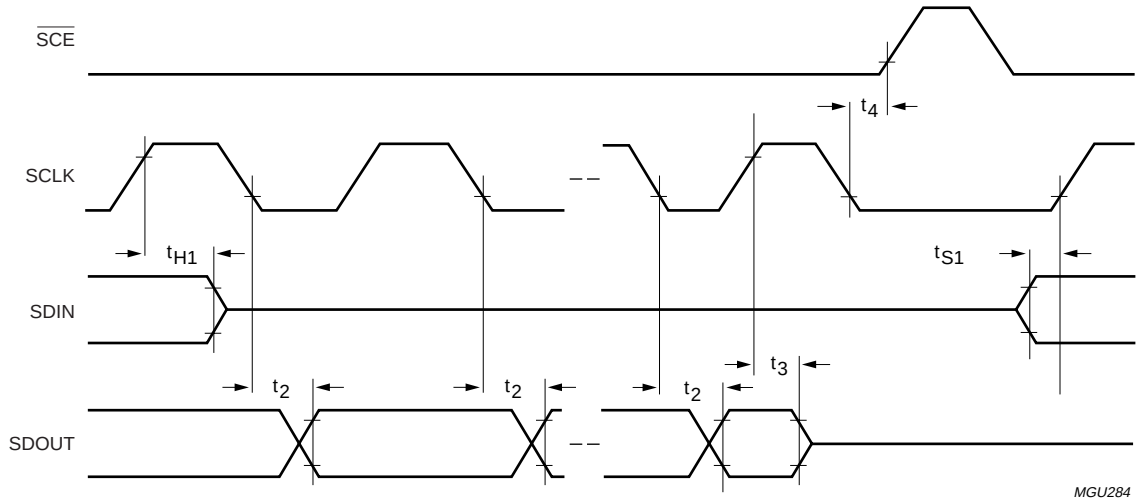


Fig.17 Serial interface timing: read mode.

16.2 Reset timing

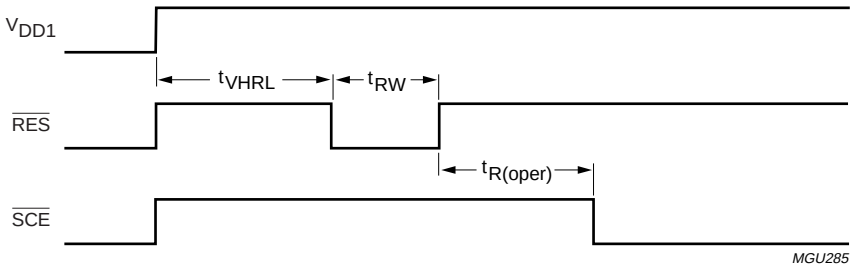


Fig.18 Reset timing.

17 APPLICATION INFORMATION

The pinning of the OM6211 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 48 × 84 pixels.

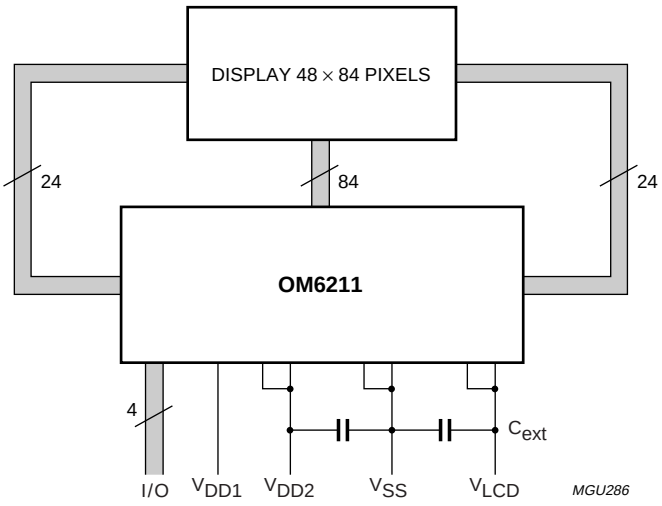


Fig.19 Application diagram.

The required minimum value for the two external capacitors (C_{ext}) in an application with the OM6211 is 100 nF (min.).

Higher capacitor values are recommended for ripple reduction.

18 MODULE MAKER PROGRAMMING

The One Time Programmable (OTP) technology has been implemented on the OM6211. It enables the module maker to program some extended features of the OM6211 after it has been assembled on an LCD module. Programming is made under the control of the serial interface and the use of one special pin. This pin must be made available on the module glass but needs not to be accessed by the set maker.

As the module maker programming is an extension of the normal functions of the OM6211 it will not be effective until specifically instructed with the 'Enable OTP' command.

The OM6211 features 3 module maker programmable parameters:

- V_{LCD} calibration
- V_{PR} default value
- Seal bit.

18.1 V_{LCD} calibration

The first feature included is the ability to tune the V_{LCD} voltage with a 5-bit code. This code is implemented in two's complement notation giving rise to a positive or negative offset to the V_{PR} register.

This is in the same manner as the on-glass calibration pins V_{OS} (laser trim pins). In theory, both may be used together but it is recommended that the laser trim pins are tied to V_{SS} when OTP calibration is being used. This will set them to a default offset of zero. If both are used then the addition of the two 5-bit numbers must not exceed a 5-bit result otherwise the resultant value will be undefined. The final adder in the circuit has underflow and overflow protection. In the event of an overflow, the output will be clamped to 255; and during an underflow the output will be clamped to 0.

The final control to the high voltage generator, V_{OP}, will be the sum of all the calibration registers and pins. The V_{OP} equation (1) given in Section 9.12 must be extended to include the OTP calibration.

$$V_{OP} = V_{PR} + V_{OS} + \text{MMVOPCAL} \quad (5)$$

The additional offset applied to V_{LCD} can be calculated from equation (2) and (5), where b is the step size as defined in Table 4.

$$V_{LCD}\text{OFFSET} = (V_{OS} + \text{MMVOPCAL}) \times b \quad (6)$$

The possible $MMVOPCAL_4$ to $MMVOPCAL_0$ values are the same as the V_{OS}[4:0] values, see Table 9.

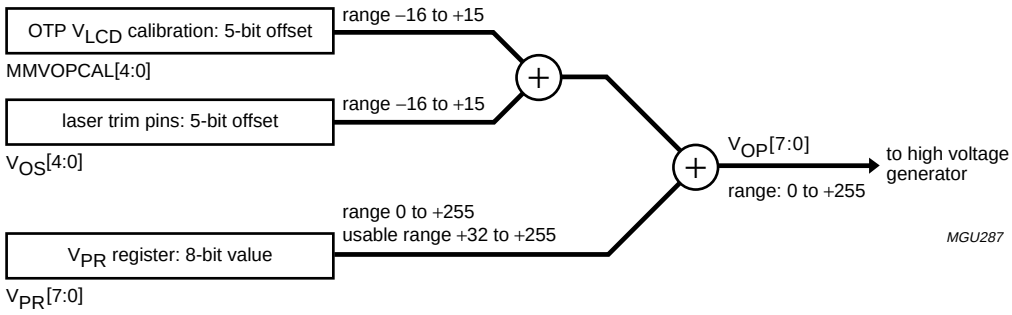


Fig.20 V_{LCD} calibration.

18.2 V_{PR} default value

The second feature is an OTP factory default setting for V_{PR}. This is an 8-bit value from which the V_{PR} register can be loaded using the 'Load factory default' command. The idea of this feature is to make it unnecessary for the set maker to specify the V_{PR} value. The factory default may be overridden by the set maker in the normal fashion using the 'Set V_{PR}' commands.

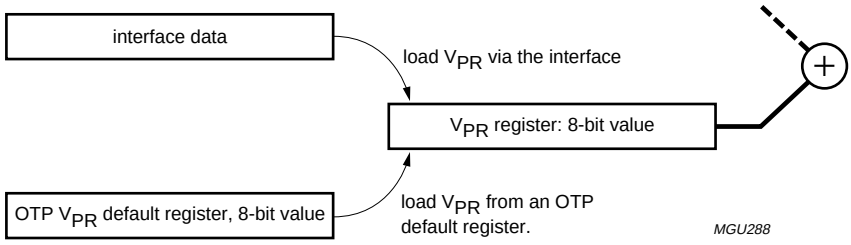


Fig.21 Load V_{PR} register: default or specified via interface.

18.3 Seal bit

The module maker programming is performed in a special mode: the calibration mode (CALMM). This mode is entered via a special interface command, CALMM.
To prevent wrongful programming, a seal bit has been implemented which prevents the device from entering the calibration mode. This seal bit, once programmed, cannot be reversed, thus further changes in programmed values are not possible. However, it is possible to disable all programmed values by not applying the 'Enable OTP' command.

Applying the programming voltages when not in CALMM mode will have no effect on the programmed values.

Table 10 Seal bit definition

SEAL BIT	ACTION
0	possible to enter calibration mode
1	calibration mode disabled

18.4 OTP architecture

The OTP circuitry in the OM6211 contains 14 bits of data: 5 for V_{LCD} calibration, 8 for V_{PR} default and 1 seal bit. The circuitry for 1-bit is called an OTP slice, thus there are 14 OTP slices.

Each OTP slice consists of 2 main parts: the OTP cell (a non-volatile memory cell) and the shift register cell (a flip-flop). The OTP cells are only accessible through their shift register cells: on the one hand both reading from and writing to the OTP cells is performed with the shift register cells, on the other hand only the shift register cells are visible to the rest of the circuit. The basic OTP architecture is shown in Fig.22.

This OTP architecture enables the following operations:

1. Reading data from the OTP cells. The content of the non-volatile OTP cells is transferred to the shift register where it may affect the OM6211 operation (provided it has been enabled by the 'Enable OTP' command).
2. Writing data to the OTP cells. Firstly, all 14 bits of data are shifted into the shift register via the serial interface. The content of the shift register is then transferred to the OTP cells (there are some limitations related to storing data in these cells, see Section 18.7).
3. Checking calibration without writing to the OTP cells. Shifting data into the shift register allows the effects on the V_{LCD} voltage to be observed.

All OTP circuitry of the OM6211 is disabled until the 'Enable OTP' command is given. Once enabled, the reading of data from the OTP cells is initiated by either:

- Exit from Power-down mode
- The 'Refresh' command.

It should be noted that in both cases the reading operation needs up to 5 ms to complete.

The shifting of data into the shift register is performed in a special mode called CALMM. In the OM6211 the CALMM mode is entered through the CALMM command. Once in the CALMM mode the data is shifted into the shift register via the serial interface at the rate of 1-bit per command. After transmitting the last (14th) bit and exiting the CALMM mode the serial interface returns to the normal mode and all other commands can be sent. Care should be taken that all 14 bits of data (or a multiple of 14) are transferred before exiting the CALMM mode, otherwise the bits will be in the wrong positions.

In the shift register the value of the seal bit is, like the others, always zero at reset. To ensure that the security feature works correctly, the CALMM command is disabled until a refresh has been performed. Once the refresh is completed, the seal bit value in the shift register is valid and permission to enter CALMM mode can thus be determined.

The 14 bits are shifted into the shift register in a predefined order: firstly the 8 bits of $MMOTPVOP_7$ to $MMOTPVOP_0$, then the 5 bits of $MMVOPCAL_4$ to $MMVOPCAL_0$ and lastly the seal bit. The MSB is always first, thus the first bit shifted is $MMOTPVOP_7$ and the two last bits are $MMVOPCAL_0$ and the seal bit.

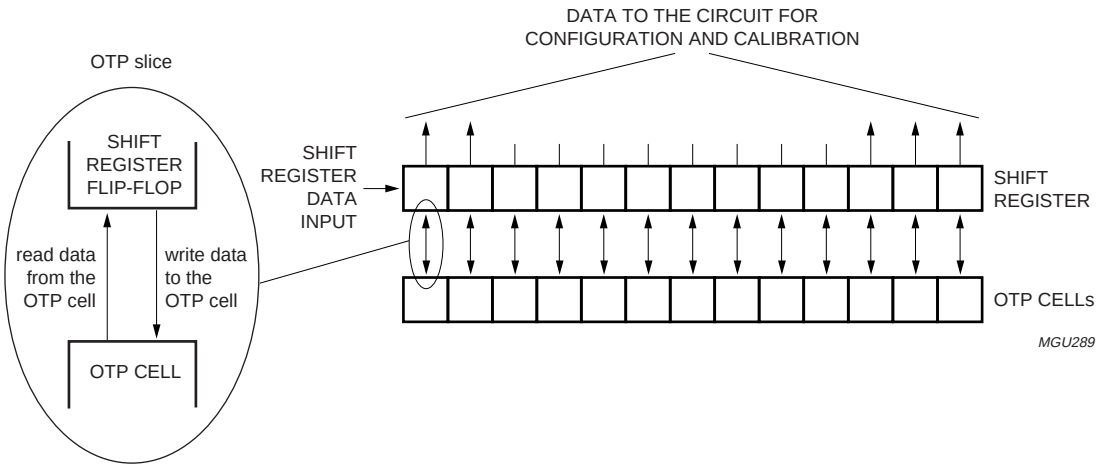


Fig.22 Basic OTP architecture.

18.5 Serial interface commands

These instructions are in addition to those indicated in Table 5.

Table 11 Additional instructions

INSTRUCTION	D/$\overline{C}$	COMMAND BYTE								ACTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Enable OTP	0	1	1	1	0	1	0	1	1	enable OTP circuitry
CALMM	0	1	1	1	0	1	1	1	1	enter CALMM mode
Load factory default	0	1	1	1	0	1	1	0	0	load $MMOTPVOP_7$ to $MMOTPVOP_0$ into V_{PR} register
Power control (refresh)	0	0	0	1	0	1	HVE	HVE	HVE	set HVE; force a refresh of the shift register

18.5.1 ENABLE OTP

This is a special instruction for the OM6211 which enables all included OTP circuitry. Once enabled the mode can only be disabled via a reset.

18.5.2 CALMM

This instruction puts the device into the calibration mode. This mode enables the shift register for loading and allows programming of the non-volatile OTP cells to take place. If the seal bit is set then this mode cannot be accessed and the instruction will be ignored. Once in calibration mode all commands are interpreted as shift register data. The mode can only be exited by sending data with bit DB7 set to logic 0. A reset will also clear this mode. Each shift register data byte is preceded by D/$\overline{C}$ = 0 and has only 2 significant bits, thus the remaining 6 bits are ignored. Bit DB7 is the continuation bit (DB7 = 1 remain in CALMM mode, DB7 = 0 exit CALMM mode). Bit DB0 is the data bit and its value is shifted into the OTP shift register (on the falling edge of SCLK).

18.5.3 LOAD FACTORY DEFAULT

The ‘Load factory default’ instruction is used to transfer the contents of the OTP shift register bits $MMOTPVOP_7$ to $MMOTPVOP_0$ into the normal working register of V_{PR}; see Fig.21. This is opposite to the calibration register $MMVOPCAL_4$ to $MMVOPCAL_0$ which is active immediately after a refresh.

18.5.4 REFRESH

The action of the ‘Refresh’ instruction is to force the OTP shift register to re-load from the non-volatile OTP cells. This instruction takes up to 5 ms to complete.

During this time all other instructions may be sent, however, instructions requiring the output of the shift register (‘Load factory default’) should be avoided as the register contents may not be valid.

In the OM6211 the ‘Refresh’ instruction is associated to the ‘Set HVE’ instruction so that the shift register is automatically refreshed every time the high voltage generator is enabled or disabled. It should be noted however, that if this instruction is sent while in Power-down mode, then the HVE bit is updated but the refreshing is ignored.

18.6 Example of filling the shift register

An example sequence of commands and data is shown in Table 12. In this example the shift register is filled with the following data: MMVOPCAL = −4 (11100B), MMOTPVOP = 19 (00010011B) and the seal bit is 0.

It is assumed that the OM6211 has just been reset. After transmitting the last bit the OM6211 can exit or remain in CALMM mode (see step 18). It should be noted that while in CALMM mode the interface does not recognize commands in the normal sense.

After this sequence has been applied it is possible to observe the impact of the data shifted in. This sequence is, however, not useful for OTP programming because the number of bits with the value ‘1’ is greater than that allowed for programming (see Section 18.7). Figure 23 shows the shift register after this action.

Table 12 Example sequence for filling the shift register; note 1

STEP	D/$\overline{C}$	COMMAND BYTE								ACTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	1	1	1	0	1	0	1	1	send enable OTP command
2	0	1	0	1	0	1	1	1	1	exit Power-down (e.g. DON = 1)
3										wait 5 ms for refresh to take effect.
4	0	1	1	1	0	1	1	1	1	enter CALMM mode
5	0	1	X	X	X	X	X	X	0	shift in data; $MMOTPVOP_7$ is first bit; note 2
6	0	1	X	X	X	X	X	X	0	$MMOTPVOP_6$
7	0	1	X	X	X	X	X	X	0	$MMOTPVOP_5$
8	0	1	X	X	X	X	X	X	1	$MMOTPVOP_4$
9	0	1	X	X	X	X	X	X	0	$MMOTPVOP_3$
10	0	1	X	X	X	X	X	X	0	$MMOTPVOP_2$
11	0	1	X	X	X	X	X	X	1	$MMOTPVOP_1$
12	0	1	X	X	X	X	X	X	1	$MMOTPVOP_0$
13	0	1	X	X	X	X	X	X	1	$MMVOPCAL_4$
14	0	1	X	X	X	X	X	X	1	$MMVOPCAL_3$
15	0	1	X	X	X	X	X	X	1	$MMVOPCAL_2$
16	0	1	X	X	X	X	X	X	0	$MMVOPCAL_1$
17	0	1	X	X	X	X	X	X	0	$MMVOPCAL_0$
18	0	0	X	X	X	X	X	X	0	seal bit; exit CALMM mode
An alternative ending could be to stay in CALMM mode										
18	0	1	X	X	X	X	X	X	0	seal bit; remain in CALMM mode

Notes

1. X = don’t care.
2. The data for the bits is not in the correct shift register position until all bits have been sent.

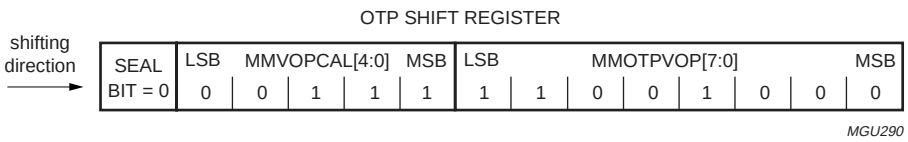


Fig.23 Shift register contents after example sequence of Table 12.

18.7 Programming flow

Programming is achieved whilst in CALMM mode and with the application of the programming voltages. As mentioned previously, the data for programming the OTP cell is contained in the corresponding shift register cell. The shift register cell must be loaded with a logic 1 in order to program the corresponding OTP cell. If the shift register cell contains a logic 0, then no action will take place when the programming voltages are applied.

Once programmed, an OTP cell can not be un-programmed. An already programmed cell, that is an OTP cell containing a logic 1, must not be re-programmed.

The order for programming cells is not significant. However, it is recommended that the seal bit is programmed last.

Once this bit has been programmed it will not be possible to re-enter the CALMM mode.

During programming a substantial current flows in the V_{LCDIN} pin. For this reason it is recommended to program only one OTP cell at a time. This is achieved by filling all but one shift register cells with logic 0. It should be noted that the programming specification refers to the voltages at the chip pins, contact resistance must therefore be considered by the user.

An example sequence of commands and data for OTP programming is shown in Table 13.

It is assumed that the OM6211 has just been reset.

Table 13 Example sequence for OTP programming; note 1

STEP	D/$\overline{C}$	COMMAND BYTE								ACTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1	0	1	1	1	0	1	0	1	1	send Enable OTP command
2	0	1	0	1	0	1	1	1	1	exit Power-down (e.g. DON = 1)
3										wait 5 ms for refresh to take effect
4	0	1	0	1	0	1	1	1	0	re-enter Power-down (DON = 0)
5	0	1	1	1	0	1	1	1	1	enter CALMM mode
6	0	1	X	X	X	X	X	X	0	shift in data. $MMOTPVOP_7$
7	0	1	X	X	X	X	X	X	0	$MMOTPVOP_6$
8	0	1	X	X	X	X	X	X	0	$MMOTPVOP_5$
9	0	1	X	X	X	X	X	X	1	$MMOTPVOP_4$ (the only bit with the value 1)
10	0	1	X	X	X	X	X	X	0	$MMOTPVOP_3$
11	0	1	X	X	X	X	X	X	0	$MMOTPVOP_2$
12	0	1	X	X	X	X	X	X	0	$MMOTPVOP_1$
13	0	1	X	X	X	X	X	X	0	$MMOTPVOP_0$
14	0	1	X	X	X	X	X	X	0	$MMVOPCAL_4$
15	0	1	X	X	X	X	X	X	0	$MMVOPCAL_3$
16	0	1	X	X	X	X	X	X	0	$MMVOPCAL_2$
17	0	1	X	X	X	X	X	X	0	$MMVOPCAL_1$
18	0	1	X	X	X	X	X	X	0	$MMVOPCAL_0$
19	0	1	X	X	X	X	X	X	0	seal bit; remain in CALMM mode
20										apply programming voltage at pins T6 and V_{LCDIN} according to Section 18.8
Repeat steps 6 to 20 for each bit that should be programmed to 1										
21										apply external reset

Note

1. X = don’t care.

18.8 Programming specification

Table 14 Programming specification; see Fig.24

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{T6}	voltage applied to T6 pin relative to V_{SS1}	programming active; notes 1 and 2	11	11.5	12	V
		programming inactive; notes 1 and 2	V_{SS} – 0.2	0	0.2	V
V_{LCDIN}	voltage applied to V_{LCDIN} pin relative to V_{SS1}	programming active; notes 1 and 3	9	9.5	10	V
		programming inactive; notes 1 and 3	–0.2	0	+4.5	V
I_{LCDIN}	current drawn by V_{LCDIN} during programming	when programming a single bit to logic 1	–	850	1000	µA
I_{T6}	current drawn by V_{T6} during programming		–	100	200	µA
$T_{amb(prog)}$	ambient temperature during programming		0	25	40	°C
$t_{su;SCLK}$	set-up of internal data after last clock		1	–	–	µs
$t_{h;SCLK}$	hold of internal data before next clock		1	–	–	µs
$t_{su;T6}$	set-up of V_{T6} prior to programming		1	–	10	ms
$t_{h;T6}$	hold of V_{T6} after programming		1	–	10	ms
t_W	pulse width of programming voltage		100	120	200	ms

Notes

1. The voltage drop across the I_{TO} track and zebra connector must be taken into account to guarantee sufficient voltage at the chip pins.
2. The maximum voltage must not be exceeded even for a short period of time. Therefore care must be taken when applying programming waveforms to avoid overshoot.
3. The Power-down mode (DON = 0 and DAL = 1) and CALMM mode must be active while the V_{LCDIN} pin is being driven.

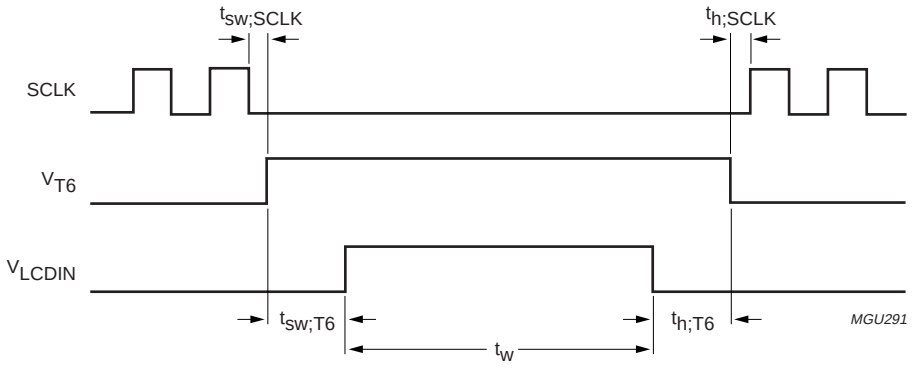


Fig.24 Programming waveforms.

19 BONDING PAD LOCATIONS

Table 15 Bonding pad information

PAD	ROWS AND COLS SIDE	INTERFACE SIDE	UNIT
Pad pitch	minimum 60	minimum 70	μm
Pad size (aluminium)	50 × 90	60 × 100	μm
CBB opening	26 × 66	36 × 76	μm
Bump dimensions	40 × 80 × 17.5 (±5)	50 × 90 × 17.5 (±5)	μm
Wafer thickness (excluding bumps)	381 (±25)		μm

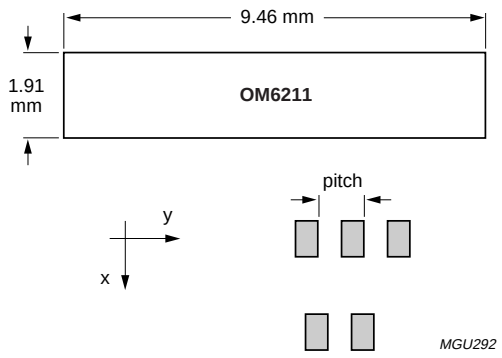


Fig.25 Chip size and pad pitch.

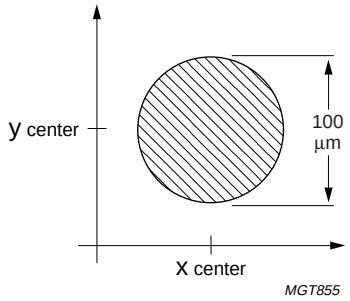


Fig.26 Shape of alignment mark.

Table 16 Bonding pad location
All x and y co-ordinates are referenced to the centre of the chip (dimensions in μm; see Fig.27).

SYMBOL	PAD	COORDINATES	
		x	y
Dummy	1	–835	+4630
Alignment mark	2	–825	+4527.5
V_{OS4}	3	–835	+4425
V_{OS3}	4	–835	+4215
V_{OS2}	5	–835	+4005
V_{OS1}	6	–835	+3795
V_{OS0}	7	–835	+3585
T6	8	–835	+3375
T6	9	–835	+3305
T6	10	–835	+3235
T6	11	–835	+3165
Dummy	12	–835	+3095
Dummy	13	–835	+3025
Dummy	14	–835	+2955
Dummy	15	–835	+2885
$\overline{RES}$	16	–835	+2395
T5	17	–835	+2185
T4	18	–835	+1975
T3	19	–835	+1765
T2	20	–835	+1555
T1	21	–835	+1345
$\overline{SCE}$	22	–835	+1135
V_{SS2}	23	–835	+1065
V_{SS2}	24	–835	+995
V_{SS2}	25	–835	+925
V_{SS2}	26	–835	+855
V_{SS2}	27	–835	+785
V_{SS2}	28	–835	+715
V_{SS2}	29	–835	+645
V_{SS2}	30	–835	+575
V_{SS1}	31	–835	+505
V_{SS1}	32	–835	+435
V_{SS1}	33	–835	+365
V_{SS1}	34	–835	+295
V_{SS1}	35	–835	+225
V_{SS1}	36	–835	+155
V_{SS1}	37	–835	+85
V_{SS1}	38	–835	+15
Dummy	39	–835	–405
OSC	40	–835	–825
SDOUT	41	–835	–1035
SDIN	42	–835	–1245
SCLK	43	–835	–1455
ID4	44	–835	–1665
ID3	45	–835	–1875
MX	46	–835	–2085
V_{DD1}	47	–835	–2155
V_{DD1}	48	–835	–2225
V_{DD1}	49	–835	–2295
V_{DD1}	50	–835	–2365
V_{DD1}	51	–835	–2435
V_{DD1}	52	–835	–2505
V_{DD2}	53	–835	–2575
V_{DD2}	54	–835	–2645
V_{DD2}	55	–835	–2715
V_{DD2}	56	–835	–2785
V_{DD2}	57	–835	–2855
V_{DD2}	58	–835	–2925
V_{DD2}	59	–835	–2995
V_{DD2}	60	–835	–3065
V_{DD3}	61	–835	–3135
V_{DD3}	62	–835	–3205
V_{DD3}	63	–835	–3275
V_{DD3}	64	–835	–3345
$V_{LCDSENSE}$	65	–835	–3415
V_{LCDOUT}	66	–835	–3485
V_{LCDOUT}	67	–835	–3555
V_{LCDOUT}	68	–835	–3625
V_{LCDOUT}	69	–835	–3695
V_{LCDOUT}	70	–835	–3765
V_{LCDOUT}	71	–835	–3835
V_{LCDOUT}	72	–835	–3905
V_{LCDIN}	73	–835	–3975
V_{LCDIN}	74	–835	–4045
V_{LCDIN}	75	–835	–4115
V_{LCDIN}	76	–835	–4185

SYMBOL	PAD	COORDINATES	
		x	y
V_{LCDIN}	77	–835	–4255
V_{LCDIN}	78	–835	–4325
Dummy	79	–835	–4395
Alignment mark	80	–825	–4500
Dummy	81	–835	–4605
Dummy	82	+840	–4590
Dummy	83	+840	–4530
Dummy	84	+840	–4470
Dummy	85	+840	–4410
Dummy	86	+840	–4350
Dummy	87	+840	–4290
Dummy	88	+840	–4230
ROW 0	89	+840	–4050
ROW 1	90	+840	–3990
ROW 2	91	+840	–3930
ROW 3	92	+840	–3870
ROW 4	93	+840	–3810
ROW 5	94	+840	–3750
ROW 6	95	+840	–3690
ROW 7	96	+840	–3630
ROW 8	97	+840	–3570
ROW 9	98	+840	–3510
ROW 10	99	+840	–3450
ROW 11	100	+840	–3390
ROW 12	101	+840	–3330
ROW 13	102	+840	–3270
ROW 14	103	+840	–3210
ROW 15	104	+840	–3150
ROW 16	105	+840	–3090
ROW 17	106	+840	–3030
ROW 18	107	+840	–2970
ROW 19	108	+840	–2910
ROW 20	109	+840	–2850
ROW 21	110	+840	–2790
ROW 22	111	+840	–2730
ROW 23	112	+840	–2670
COL 0	113	+840	–2490
COL 1	114	+840	–2430
COL 2	115	+840	–2370

SYMBOL	PAD	COORDINATES	
		x	y
COL 3	116	+840	–2310
COL 4	117	+840	–2250
COL 5	118	+840	–2190
COL 6	119	+840	–2130
COL 7	120	+840	–2070
COL 8	121	+840	–2010
COL 9	122	+840	–1950
COL 10	123	+840	–1890
COL 11	124	+840	–1830
COL 12	125	+840	–1770
COL 13	126	+840	–1710
COL 14	127	+840	–1650
COL 15	128	+840	–1590
COL 16	129	+840	–1530
COL 17	130	+840	–1470
COL 18	131	+840	–1410
COL 19	132	+840	–1350
COL 20	133	+840	–1290
COL 21	134	+840	–1230
COL 22	135	+840	–1170
COL 23	136	+840	–1110
COL 24	137	+840	–1050
COL 25	138	+840	–990
COL 26	139	+840	–930
COL 27	140	+840	–870
COL 28	141	+840	–690
COL 29	142	+840	–630
COL 30	143	+840	–570
COL 31	144	+840	–510
COL 32	145	+840	–450
COL 33	146	+840	–390
COL 34	147	+840	–330
COL 35	148	+840	–270
COL 36	149	+840	–210
COL 37	150	+840	–150
COL 38	151	+840	–90
COL 39	152	+840	–30
COL 40	153	+840	+30
COL 41	154	+840	+90

SYMBOL	PAD	COORDINATES	
		x	y
COL 42	155	+840	+150
COL 43	156	+840	+210
COL 44	157	+840	+270
COL 45	158	+840	+330
COL 46	159	+840	+390
COL 47	160	+840	+450
COL 48	161	+840	+510
COL 49	162	+840	+570
COL 50	163	+840	+630
COL 51	164	+840	+690
COL 52	165	+840	+750
COL 53	166	+840	+810
COL 54	167	+840	+870
COL 55	168	+840	+930
COL 56	169	+840	+1110
COL 57	170	+840	+1170
COL 58	171	+840	+1230
COL 59	172	+840	+1290
COL 60	173	+840	+1350
COL 61	174	+840	+1410
COL 62	175	+840	+1470
COL 63	176	+840	+1530
COL 64	177	+840	+1590
COL 65	178	+840	+1650
COL 66	179	+840	+1710
COL 67	180	+840	+1770
COL 68	181	+840	+1830
COL 69	182	+840	+1890
COL 70	183	+840	+1950
COL 71	184	+840	+2010
COL 72	185	+840	+2070
COL 73	186	+840	+2130
COL 74	187	+840	+2190
COL 75	188	+840	+2250
COL 76	189	+840	+2310
COL 77	190	+840	+2370
COL 78	191	+840	+2430
COL 79	192	+840	+2490
COL 80	193	+840	+2550

SYMBOL	PAD	COORDINATES	
		x	y
COL 81	194	+840	+2610
COL 82	195	+840	+2670
COL 83	196	+840	+2730
ROW 47	197	+840	+2910
ROW 46	198	+840	+2970
ROW 45	199	+840	+3030
ROW 44	200	+840	+3090
ROW 43	201	+840	+3150
ROW 42	202	+840	+3210
ROW 41	203	+840	+3270
ROW 40	204	+840	+3330
ROW 39	205	+840	+3390
ROW 38	206	+840	+3450
ROW 37	207	+840	+3510
ROW 36	208	+840	+3570
ROW 35	209	+840	+3630
ROW 34	210	+840	+3690
ROW 33	211	+840	+3750
ROW 32	212	+840	+3810
ROW 31	213	+840	+3870
ROW 30	214	+840	+3930
ROW 29	215	+840	+3990
ROW 28	216	+840	+4050
ROW 27	217	+840	+4110
ROW 26	218	+840	+4170
ROW 25	219	+840	+4230
ROW 24	220	+840	+4290
Dummy	221	+840	+4350
Dummy	222	+840	+4410
Dummy	223	+840	+4470
Dummy	224	+840	+4530
Dummy	225	+840	+4590

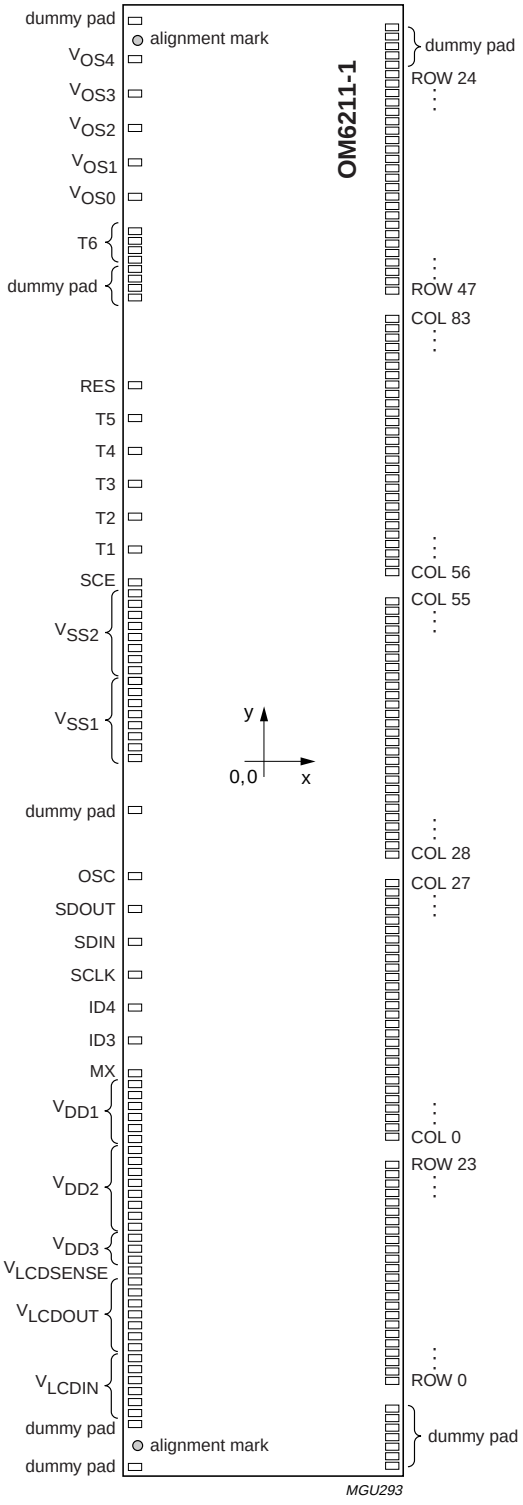
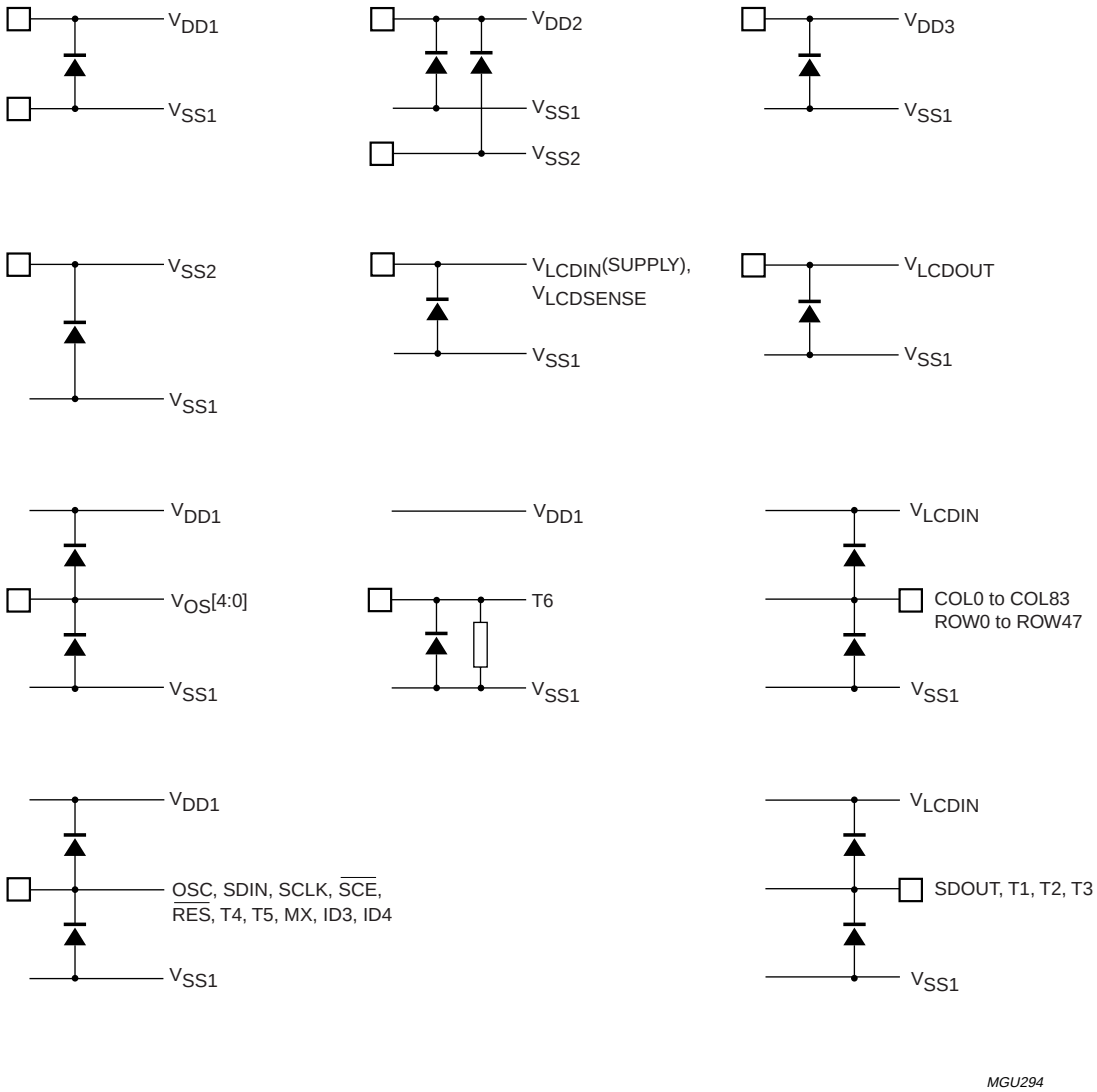


Fig.27 Pad locations.

20 DEVICE PROTECTION DIAGRAM



The conditions for continuity tests are as follows:
Maximum forward current = 5 mA; Maximum reverse voltage = 5 V.

Fig.28 Device protection diagram.

21 TRAY INFORMATION

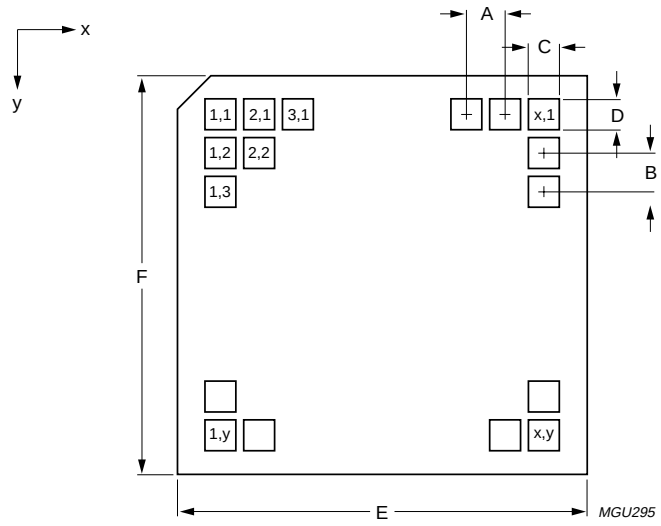
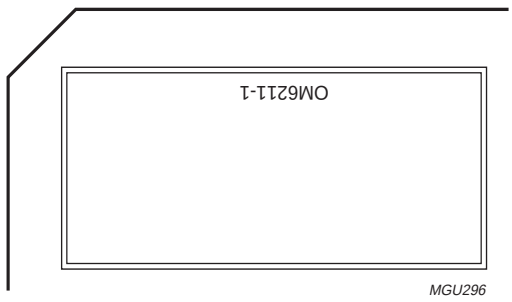


Fig.29 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientation and position of the type name on the surface.

Fig.30 Tray alignment.

Table 17 Tray dimensions

DIMENSION	DESCRIPTION	VALUE
A	pocket pitch x direction	13.76 mm
B	pocket pitch y direction	4.45 mm
C	pocket width x direction	9.56 mm
D	pocket width y direction	2.00 mm
E	tray width x direction	50.80 mm
F	tray width y direction	50.80 mm
x	number of pockets in x direction	3
y	number of pockets in y direction	10

22 APPLICATION NOTES

When reading the VM bit in the OM6211 two problems have been observed: corrupted format and VM bit toggling.

22.1 Corrupted format

The read-out of the VM bit has a special format, 11110000 for VM = 1 and 00001111 for VM = 0. However, sometimes a wrong format of the read-out byte can be observed; the first or the fifth or the eighth bit appears to be wrong. There are two reasons for this behaviour. When the first bit happens to be read out at the end of a frame then it is possible that the first bit belongs to the old VM value and the 7 following bits belong to the new VM value. Such behaviour is possible for the first bit only. The second reason is the violation of the OM6211 timing, if the timing parameters t_2 and t_3 (see Fig.17) are violated, then it results in reading a wrong value for the first, the fifth or the eighth bit. Thus, to prevent any problems with the wrong format of the read-out byte, these bits should always be ignored.

22.2 VM bit toggling

Under certain conditions it can happen that the result of reading VM is 0 even if the generated V_{LCD} voltage is correct (VM bit toggles). It is therefore recommended to repeat the VM read command several times according to the algorithm described below. This algorithm is based on the observation that a single reading of VM = 1 (after numerous readings of VM = 0) is enough to ensure that the charge pump operation is correct. One possible method which gives minimum measurement duration is shown in Fig.31 and described in detail below:

- Perform initialization with Enable OTP and set the operational parameters (V_{PR} = 159, S = 10, BS = 101, TC = 1, E = 0 and MY = 0) this results in a slightly higher V_{LCD} voltage than for normal operation (V_{LCD} = 8.732 V at T_{amb} = 27 °C)
- Select DAL = 1 and DON = 1 (for all pixels on)
- After setting HVE = 1 start a loop of a continuous VM reading (for example, every 1 ms), at first occurrence of reading VM = 1 interrupt the loop and accept VM = 1
- When the reading is always VM = 0, stop the loop after a certain time and accept VM = 0. This loop time limit should be chosen sufficiently long, e.g. 85 ms. Given that the uncertainty is much less then 0.1%, much less then 1 ppm is expected to be read out wrong.

For the loop time limit a value of not less than 85 ms is suggested. It should be noted that the value of 45 ms specified in Section 11.2.2 means that after at least 45 ms the VM measurement is possible. In practice it can be expected that VM is valid earlier than 45 ms. Therefore the proposed algorithm results in an optimization of the 45 ms wait time needed to charge the external V_{LCD} capacitor. So the selected loop time limit of 85 ms consists of 45 ms wait time and an additional 40 ms of measurement time. The loop time limit of 85 ms will ensure that even if the first VM = 1 value for any reason should be missed, there is always the possibility to hit the next VM = 1 value (note that the internal VM measurement is made once per 12.5 ms). However, the expectation is that **the average running time of the loop will be less than 45 ms**.

There is another possibility for optimization: during the wait time of the loop (1 ms) other tasks can be performed. Furthermore the first part of the 45 ms wait time, just after setting HVE = 1, may also be used for other tasks. For instance when the first 20 ms are reserved for those tasks, then the corresponding loop time limit would be 65 ms and the expected average loop time would be less than 25 ms.

After the VM test is completed the V_{PR} can be set to the desired value (e.g. V_{PR} = 137) without the charge pump being switched off.

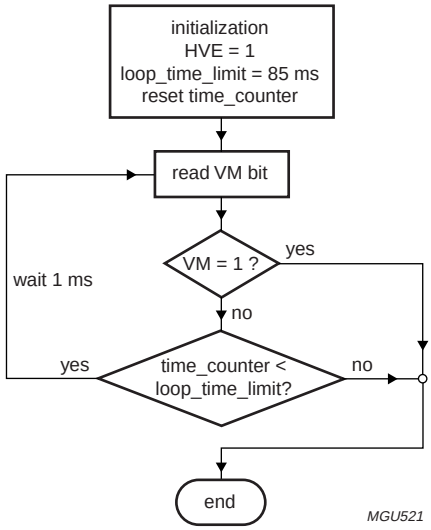


Fig.31 Algorithm of reliable and fast read-out of the VM bit.

23 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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