Multicore Resource Management for Embedded Real-Time Systems

Heechul Yun
University of Kansas



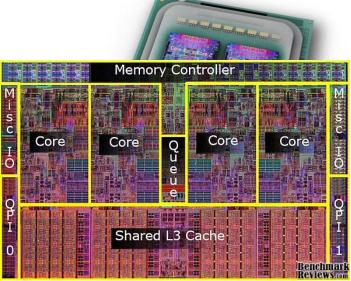
High-Performance **Multicores** for Embedded **Real-Time** Systems

Why?

- Intelligence → more performance
- Space, weight, power (SWaP), cost

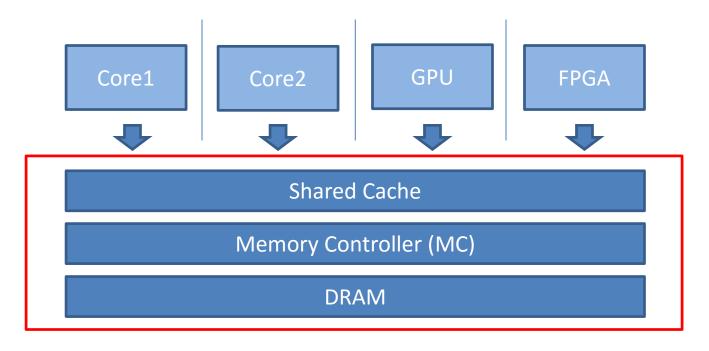








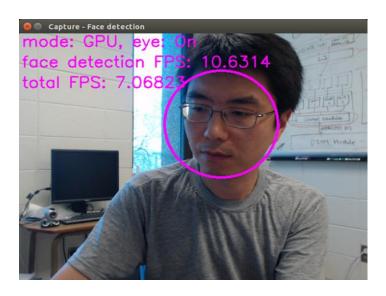
Time Predictability Challenge



- Hardware resources are shared among the cores
- Tasks can suffer significant interference delays
 - unpredictable, non-deterministic
 non-certifiable, unsafe



Example: Real-Time Obstacle Detection and Avoidance



mode: GPU, eye:
face detection FPS: 2.24625
total FPS: 1.4437

Run-alone

w/Co-runners

- Co-runners were launched on idle CPU cores
- 5X slowdown in detection speed (~10fps → 2fps)
 - can fail to avoid obstacle





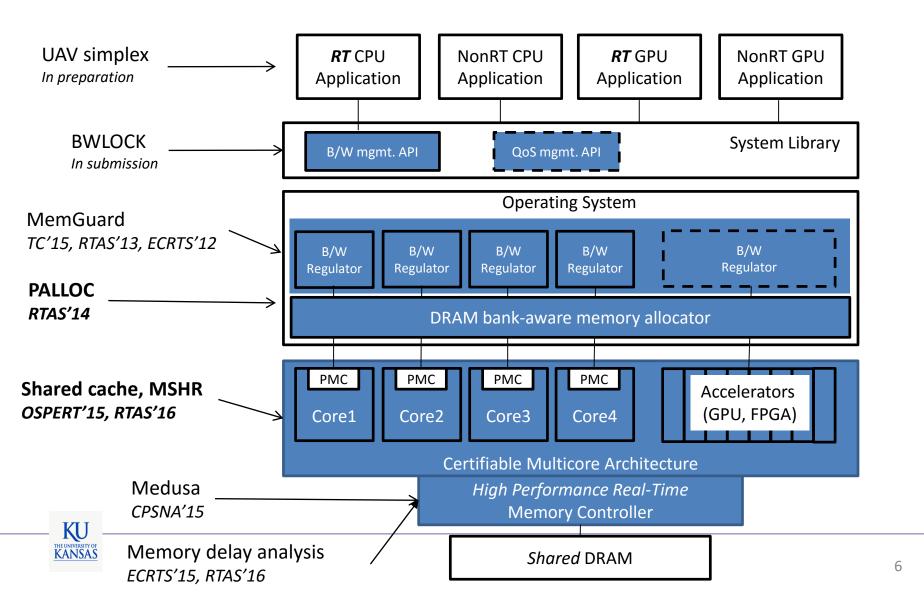
Research Mission

• Our research goal is to build **predictable**, **efficient**, and **safe** computing infrastructure for the next generation of intelligent embedded real-time systems, a.k.a., Cyber Physical Systems (CPS).

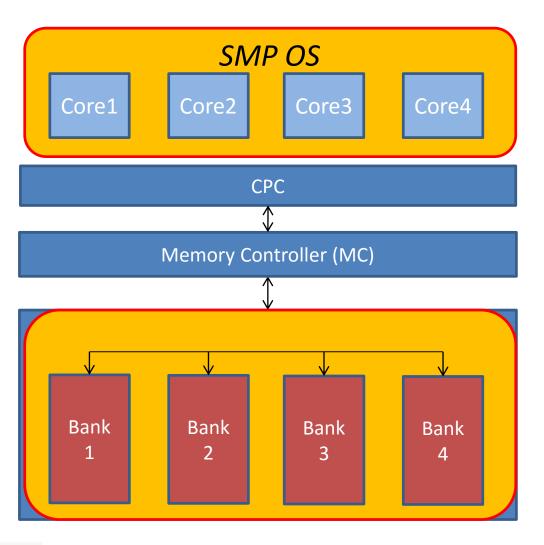
- Approach
 - Develop software/hardware mechanisms
 - Develop analysis framework



Research Results



PALLOC

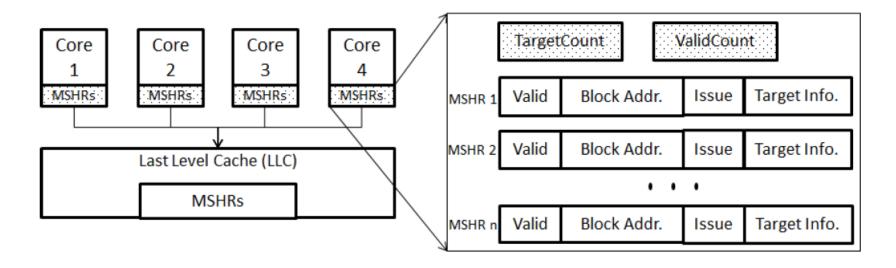


- DRAM bank-aware kernel memory allocator
- Can void bank conflict





OS Controlled MSHR Partitioning



- Experimentally showed cache partitioning doesn't provide cache performance isolation in non-blocking caches
- Proposed a OS/hardware collaborative solution that guarantees cache perf. isolation



References

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- [RTAS16-2] Rodolfo Pellizzoni, Heechul Yun. Memory Servers for Multicore Systems. IEEE Intl.
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- [TC15] **Heechul Yun**, Gang Yao, Rodolfo Pellizzoni, Marco Caccamo, and Lui Sha. Memory Bandwidth Management for Efficient Performance Isolation in Multi-core Platforms, *IEEE Transactions on Computers*, Vol 65, Issue 2, 2015, pp. 562 576 (Selected as **the Feature paper** by the editors)
- [CPSNA15] Prathap Kumar Valsan (*), Heechul Yun. MEDUSA: A Predictable and High-Performance DRAM Controller for Multicore based Embedded Systems IEEE Intl. Conference on Cyber-Physical Systems, Networks, and Applications (CPSNA), 2015, pp. 86 – 93
- [ECRTS15-1] Heechul Yun, Rodolfo Pellizzoni, Prathap Kumar Valsan (*). Parallelism-Aware Memory Interference Delay Analysis for COTS Multicore Systems. IEEE Euromicro Conference on Real-Time Systems (ECRTS), 2015.
- [ECRTS15-2] Renato Mancuso, Rodolfo Pellizzoni, Marco Caccamo, Lui Sha and Heechul Yun. WCET(m) Estimation in Multi-Core Systems using Single Core Equivalence. *Euromicro Conference on Real-Time Systems (ECRTS)*, 2015.
- [RTAS14] **Heechul Yun**, Renato Mancuso, Zheng Wu, Rodolfo Pellizzoni. PALLOC: DRAM Bank-Aware Memory Allocator for Performance Isolation on Multicore Real-Time Systems, *IEEE Intl. Conference on Real-Time and Embedded Technology and Applications Symposium (RTAS)*. 2014, pp. 155-166.



On-going Projects

- Multicore Resource Management
 - OS, architecture research for time predictability
 - Funding Agencies: NSF, ETRI

- UAV Software Platform
 - ROS (Robot Operating System) based autopilot and real-time sensor (radar and vision) processing
 - Funding Agencies: NASA



Autonomous Racing



Dr. Madhur Behl

University of Pennsylvania



Prospective Students

- Solid background in operating systems and computer architecture
- Good system programming skills
- Interests and experiences in building Intelligent cyber-physical systems
 - ROS, python, Linux, OpenCV, CUDA
 - PID control, real-time sensor fusion

Send me your CV and schedule a meeting

