# PIN DIAGRAM & ARCHITECTURE OF 8085



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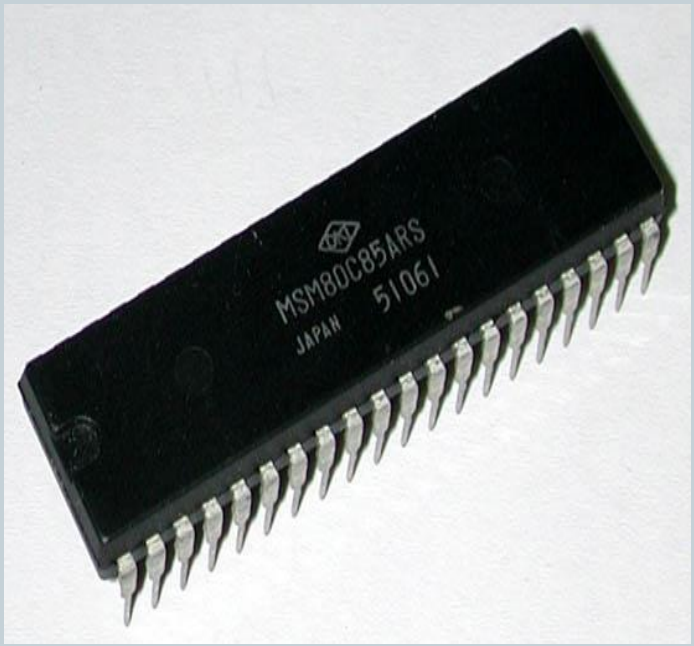
# Introduction to 8085

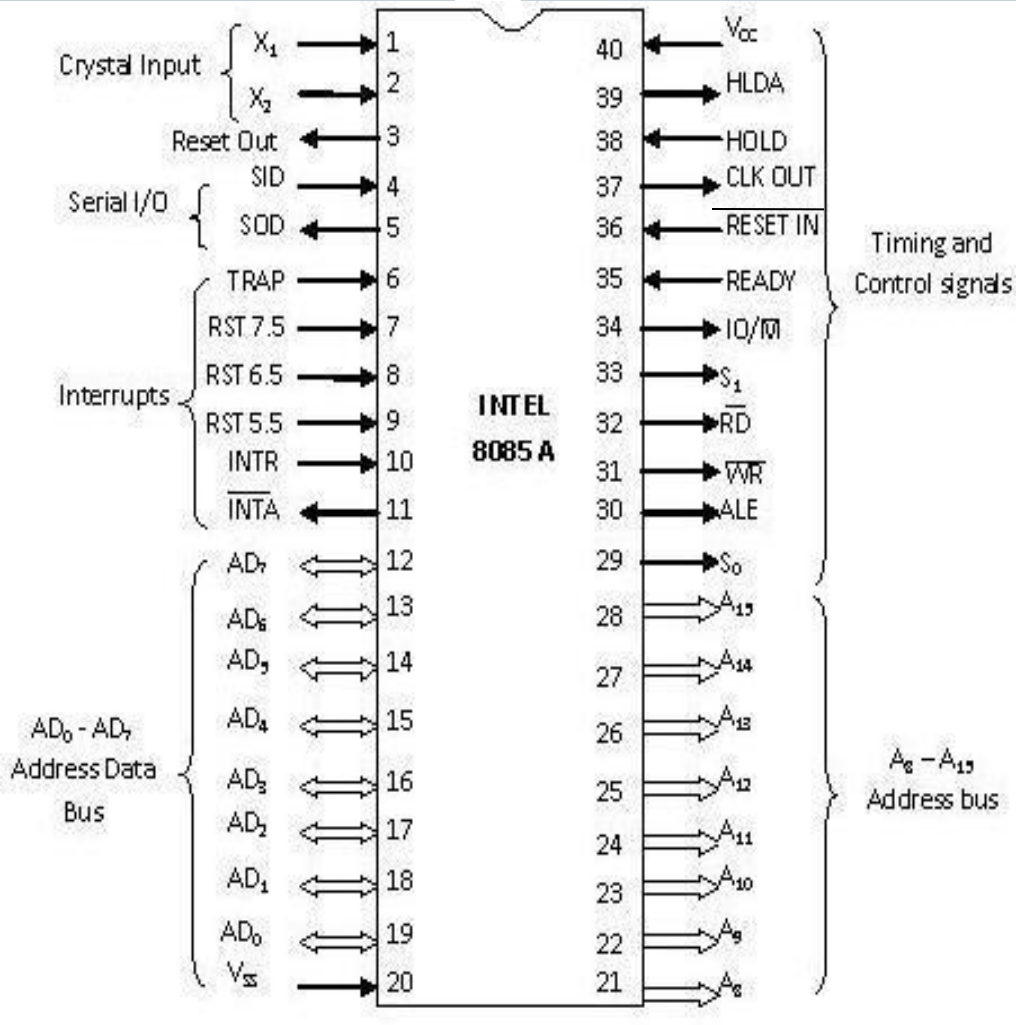





- It was introduced in 1977.
- It is 8-bit microprocessor.
- It is NMOS device.
- It is having 40 pins Dual-Inline-Package (DIP).
- The clock frequencies of 8085 are:
  - 8085 A 3 MHz
  - 8085 AH2 5 MHz
  - 8085 AH1 6 MHz

# Pin Diagram of 8085





# Various types of signals of 8085



1. Address bus and Data bus.
2. Control and Status signals
3. Power supply and frequency signals
4. Interrupts signals
5. Reset signals
6. DMA signals
7. Serial I/O ports

# Address bus and Data bus



- The address bus is a group of sixteen lines i.e A0-A15. The address bus is unidirectional, i.e bits flow in one direction from the MPU to peripheral devices.
- There is multiplexing of lower order address bus and data bus ie AD0 to AD7.

# Control and Status signals



- ALE: It is an Address Latch Enable signal. It goes high during first T state of a machine cycle. It enables the lower 8-bits of the address if its value is 1 otherwise data bus is activated from AD0-AD7.
- IO/M': It is a status signal which distinguishes whether the address is for memory or I/O. When it goes high the address on the address bus is for I/O devices. When it goes low the address on the address bus is for the memory.

# Control and Status signals



- S1, S0: These are status signals sent by the microprocessor to distinguish the various types of operations.
- RD': When it is 0 there is read operation.
- WR': When it is 0 there is write operation.
- READY : It is used by the microprocessor to sense whether a peripheral is ready to transfer data or not. If it is high the peripheral is ready. If it is low the microprocessor waits till it goes high.

# Control and Status signals



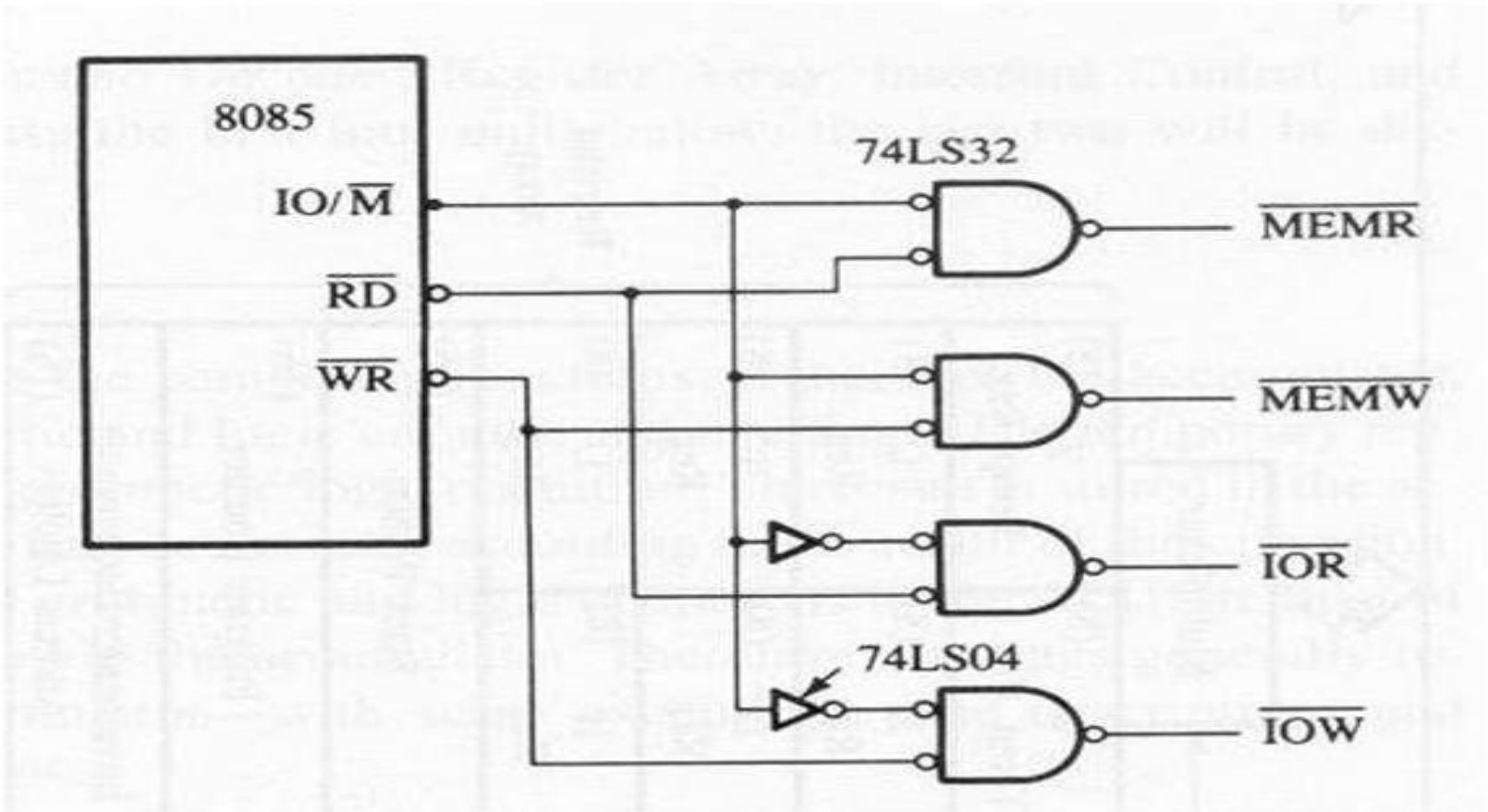
| IO/M' | S1 | So | Data Bus Status |
|---|---|---|---|
| 0 | 1 | 1 | Opcode fetch |
| 0 | 1 | 0 | Memory read |
| 0 | 0 | 1 | Memory write |
| 1 | 1 | 0 | I/O read |
| 1 | 0 | 1 | I/O write |
| 1 | 1 | 1 | Interrupt acknowledge |
| 0 | 0 | 0 | Halt |

If IO/M' = 0 and S1=0 & S0=1 then

Combining these two we get Memory Write Operation.

# Schematic to generate Control Signals





# Power supply and frequency signals



- Vcc - +5v power supply Vss - Ground Reference
- XI, X2 - A crystal is connected at these two pins. The frequency is internally divided by two, therefore, to operate a system at 3MHZ the crystal should have frequency of 6MHZ.
- CLK (OUT) - This signal can be used as the system clock for other devices.

# Interrupts signals



- The 8085 has five interrupts that can be used to interrupt a program execution.

i) INTR

ii) RST 7.5

iii) RST 6.5

iv) RST 5.5

v) TRAP

- The microprocessor acknowledges Interrupt Request by INTA' signal.

# Reset signals



- RESETIN’ : When the signal on this pin goes low, the program - counter is set to zero, the buses are tristated and the MPU is reset.
- RESET OUT : This signal indicates that the MPU is being reset. The signal can be used to reset other devices.

# DMA signals



- HOLD : It indicates that another device is requesting the use of the address and data bus. The processor regains the bus after the removal of the HOLD signal.
- HLDA : It is a signal which indicates that the hold request has been received and control of address and data bus is transferred to DMAC(8257).

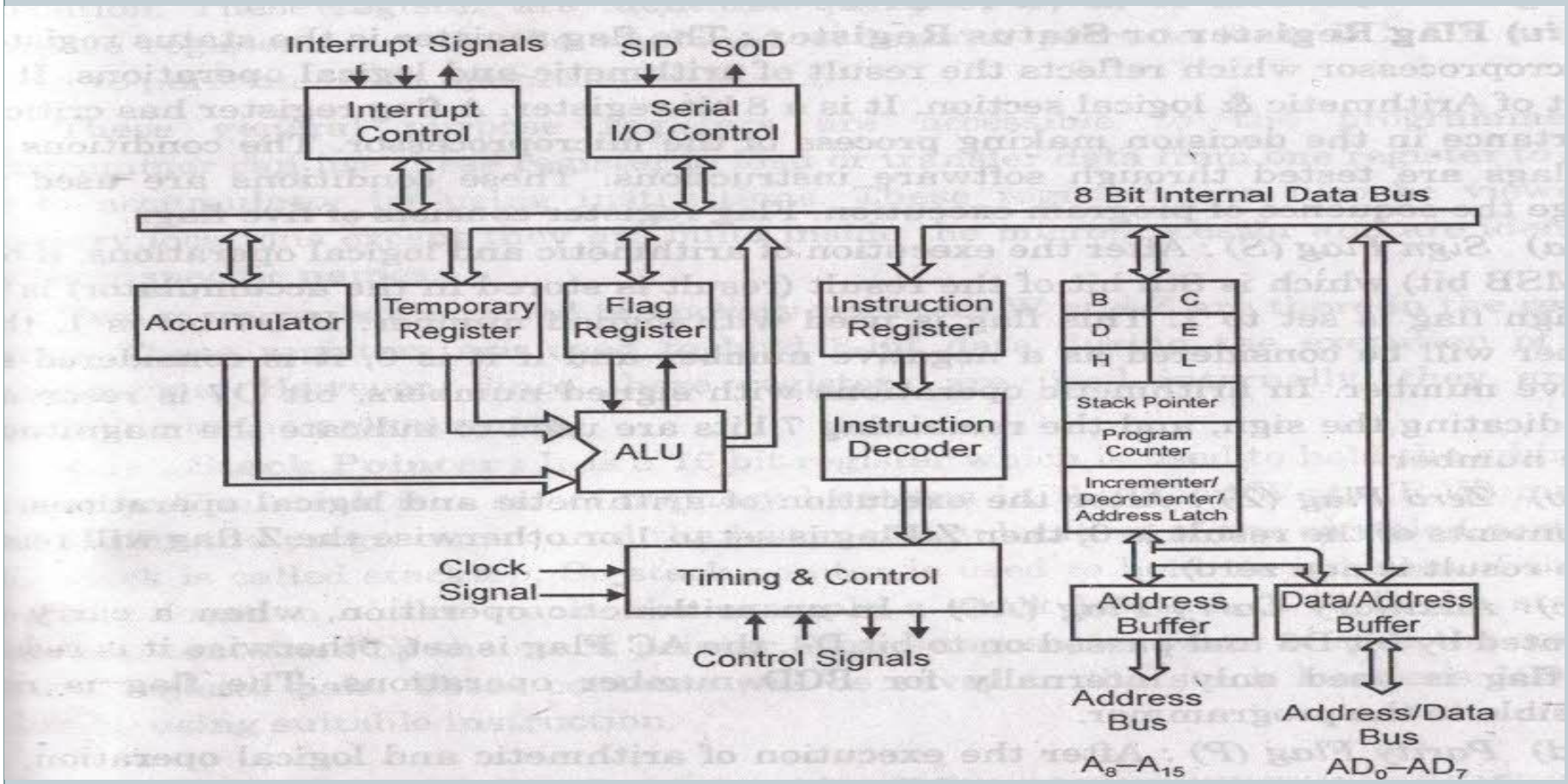
# Serial I/O ports



- The 8085 has two signals to implement the serial transmission.
- SID :SID is a data line for serial input
- SOD:SOD is a data line for serial output.
- Serial transfer of data is transmitted bit by bit on a single line.
- SID is used in RIM instruction and SOD is used in SIM instruction.

# 8085 Architecture





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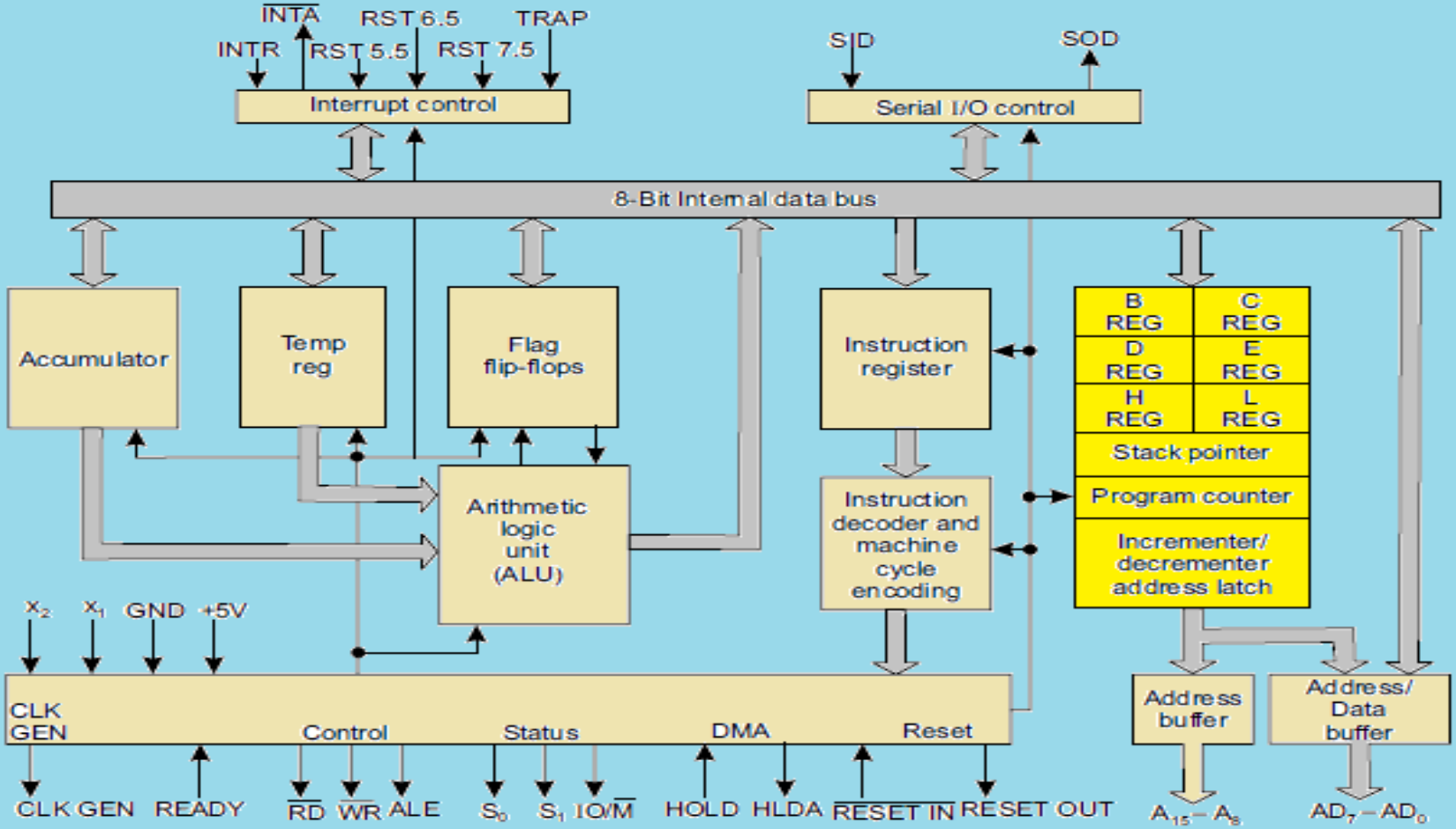


Architecture of 8085