Transistor Biasing

TRANSISTOR BIASING, DC LOAD LINE, QUIESCENT POINT

The proper flow of zero signal collector current and the maintenance of proper collector- emitter voltage during the passage of signal is known as **Transistor Biasing**. The circuit which provides transistor biasing is called as **Biasing Circuit**.

Need for DC biasing

If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

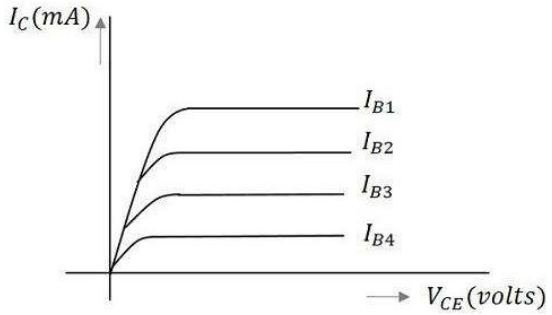
- The input voltage should exceed **cut-in voltage** for the transistor to be **ON**.
- The BJT should be in the **active region**, to be operated as an **amplifier**.

If appropriate DC voltages and currents are given through BJT by external sources, so that BJT operates in active region and superimpose the AC signals to be amplified, then this problem can be avoided. The given DC voltage and currents are so chosen that the transistor remains in active region for entire input AC cycle. Hence DC biasing is needed.

Output Characteristics

When the output characteristics of a transistor are considered, the curve looks as below for different input values.

In the above figure, the output characteristics are drawn between collector current **IC** and collector



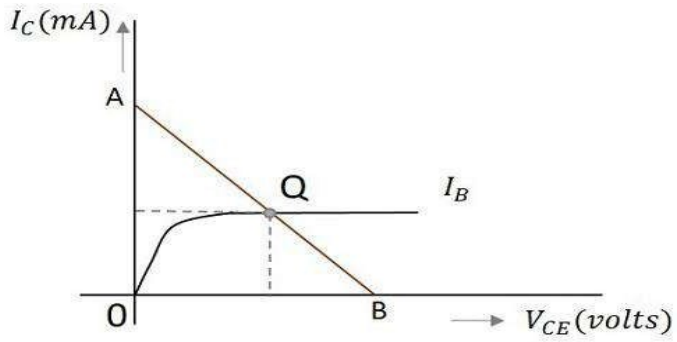
voltage **VCE** for different values of base current **IB**. These are considered here for different input values to obtain different output curves.

Operating point

When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the **saturation point**. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the **cutoff point**.

When a line is drawn joining these two points, such a line can be called as **Load line**. This is called so as it symbolizes the output at the load. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point**.

This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in active region. This can be better understood through the figure below.

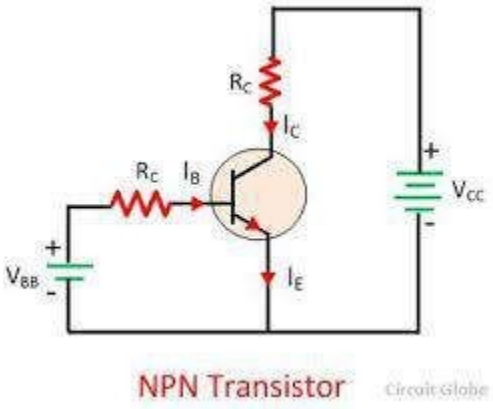


The load line has to be drawn in order to obtain the Q-point. A transistor acts as a good amplifier when it is in active region and when it is made to operate at Q-point, faithful amplification is achieved.

Faithful amplification is the process of obtaining complete portions of input signal by increasing the signal strength. This is done when AC signal is applied at its input.

DC Load line

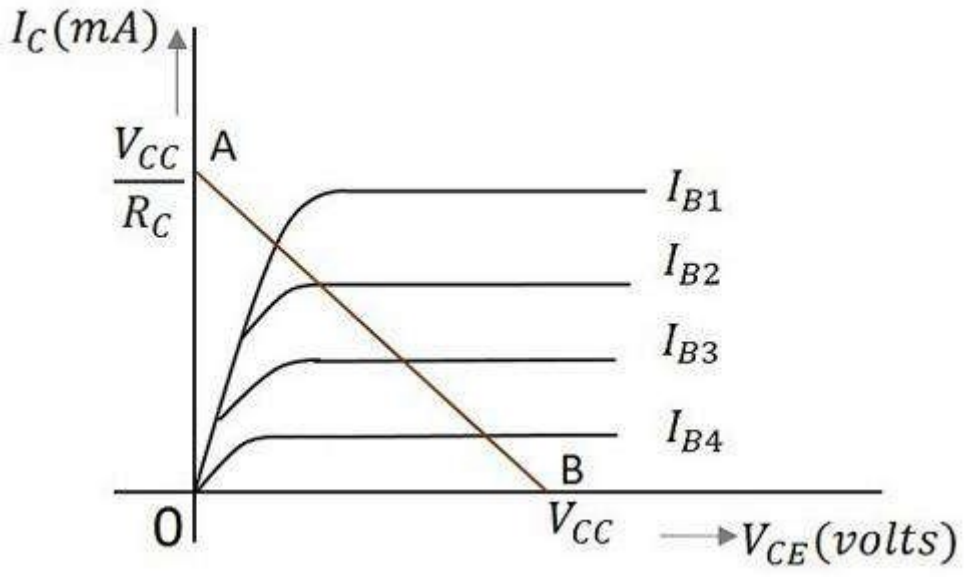
When the transistor is given the bias and no signal is applied at its input, the load line drawn at such condition, can be understood as **DC** condition. Here there will be no amplification as the AC signal is absent. The circuit will be as shown below.



The value of collector emitter voltage at any given time will be

$V_{CE}=V_{CC}-I_CR_C$

As V**CC** and R**C** are fixed values, the above one is a first degree equation and hence will be a straight line on the output characteristics. This line is called as **D.C. Load line**. The figure below shows the DC load line.



To obtain the load line, the two end points of the straight line are to be determined. Let those two points be A and B.

To obtain A

When collector emitter voltage VCE = 0, the collector current is maximum and is equal to VCC/RC. This gives the maximum value of VCE. This is shown as

VCE=VCC−ICRC 0=VCC−ICRC IC=VCC/RC

This gives the point A (OA = VCC/RC) on collector current axis, shown in the above figure.

To obtain B

When the collector current IC = 0, then collector emitter voltage is maximum and will be equal to the VCC. This is shown as

VCE=VCC−ICRC VCE =VCC

(As IC = 0)

This gives the point B, which means (OB = **VCC**) on the collector emitter voltage axis shown in the above figure.

Hence we got both the saturation and cutoff point determined and learnt that the load line is a straight line. So, a DC load line can be drawn.

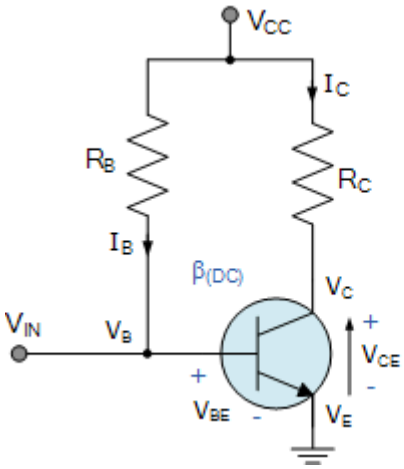
METHODS OF TRANSISTOR BIASING

The biasing in transistor circuits is done by using two DC sources **VBB** and **VCC**. It is economical to minimizethe DC source to one supply instead of two which also makes the circuit simple.

The commonly used methods of transistor biasing are

- Base Resistor method
- Emitter stabilised biasing
- Biasing with Collector feedback resistor
- Voltage-divider bias or Self bias

Base Resistor method or Fixed Base Biasing a Transistor



$V_C = V_{CC} - (I_C R_C)$
$V_{CE} = V_C - V_E$
$V_E = 0v$
$V_B = V_{BE}$
$I_B = \frac{V_{CC} - V_{BE}}{R_B}$
$I_C = \beta_{(DC)} I_B$
$I_E = (I_C + I_B) \cong I_C$

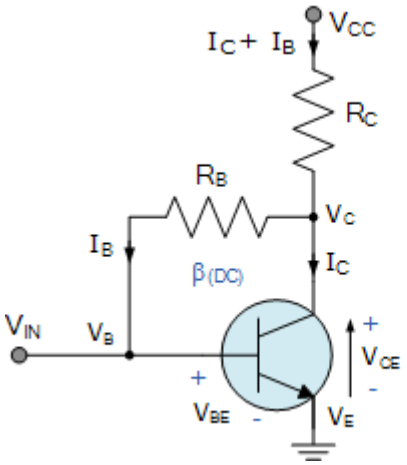
The circuit shown is called as a "fixed base bias circuit", because the transistors base current, I_B remains constant for given values of Vcc, and therefore the transistors operating point must also remain fixed. This two resistor biasing network is used to establish the initial operating region of the transistor using a fixed current bias.

This type of transistor biasing arrangement is also beta dependent biasing as the steady-state condition of operation is a function of the transistors beta β value, so the biasing point will vary over a wide range for transistors of the same type as the characteristics of the transistors will not be exactly the same.

The emitter diode of the transistor is forward biased by applying the required positive base bias voltage via the current limiting resistor R_B. Assuming a standard bipolar transistor, the forward base-emitter voltage drop would be 0.7V. Then the value of R_B is simply: $(V_{CC} – V_{BE})/I_B$ where I_B is defined as I_C/β.

With this single resistor type of biasing arrangement the biasing voltages and currents do not remain stable during transistor operation and can vary enormously. Also the operating temperature of the transistor can adversely effect the operating point.

Collector Feedback Biasing



$V_C = V_{CC} - R_C(I_C + I_B)$
$V_E = 0v$
$V_B = V_{BE}$
$I_B = \frac{V_C - V_B}{R_B}$
$I_C = \beta_{(DC)} I_B$
$I_E = (I_C + I_B) \cong I_C$

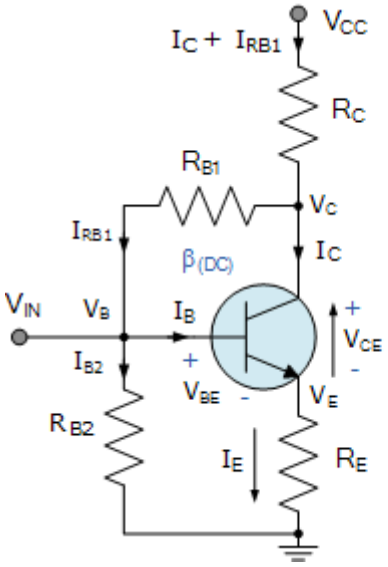
This self biasing collector feedback configuration is another beta dependent biasing method which requires two resistors to provide the necessary DC bias for the transistor. The collector to base feedback configuration ensures that the transistor is always biased in the active region regardless of the value of Beta (β). The DC base bias voltage is derived from the collector voltage V_C, thus providing good stability.

In this circuit, the base bias resistor, R_B is connected to the transistors collector C, instead of to the supply voltage rail, Vcc. Now if the collector current increases, the collector voltage drops, reducing the base drive and thereby automatically reducing the collector current to keep the transistors Q-point fixed. Therefore this method of collector feedback biasing produces negative feedback round the transistor as there is a direct feedback from the output terminal to the input terminal via resistor, R_B.

Since the biasing voltage is derived from the voltage drop across the load resistor, R_L, if the load current increases there will be a larger voltage drop across R_L, and a corresponding reduced collector voltage, V_C. This effect will cause a corresponding drop in the base current, I_B which in turn, brings I_C back to normal.

The opposite reaction will also occur when the transistors collector current reduces. Then this method of biasing is called self-biasing with the transistors stability using this type of feedback bias network being generally good for most amplifier designs.

Emitter Feedback Configuration



$$V_C = V_{CC} - R_C(I_C + I_{B1})$$
$$V_E = I_E R_E = V_B - V_{BE}$$
$$V_{CE} = V_C - V_E$$
$$V_B = V_{BE} + V_E$$
$$I_{RB2} = \frac{V_B}{R_{B2}}$$
$$I_{RB1} = I_B + I_{RB2} = \frac{V_C - V_B}{R_{B1}}$$
$$I_C = \beta_{(DC)} I_B$$
$$I_E = (I_C + I_B) \cong I_C$$

This type of transistor biasing configuration, often called self-emitter biasing, uses both emitter and base-collector feedback to stabilize the collector current even further. This is because resistors R_{B1} and R_E as well as the base-emitter junction of the transistor are all effectively connected in series with the supply voltage, V_{CC}.

The downside of this emitter feedback configuration is that it reduces the output gain due to the base resistor connection. The collector voltage determines the current flowing through the feedback resistor, R_{B1} producing what is called “degenerative feedback”.

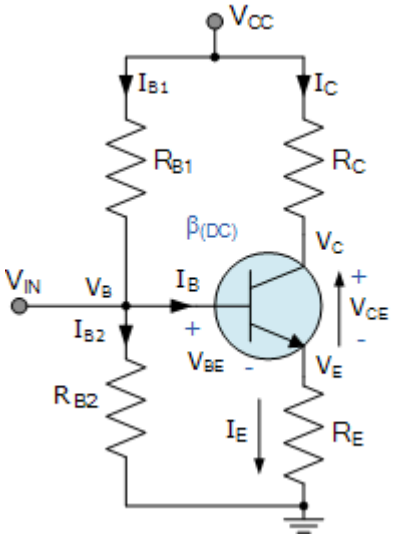
The current flowing from the emitter, I_E (which is a combination of $I_C + I_B$) causes a voltage drop to appear across R_E in such a direction, that it reverse biases the base-emitter junction.

So if the emitter current increases, due to an increase in collector current, voltage drop $I*R_E$ also increases. Since the polarity of this voltage reverse biases the base-emitter junction, I_B automatically decrease. Therefore the emitter current increase less than it would have done had there been no self biasing resistor.

Generally, resistor values are set so that the voltage dropped across the emitter resistor R_E is approximately 10% of V_{CC} and the current flowing through resistor R_{B1} is 10% of the collector current I_C.

Thus this type of transistor biasing configuration works best at relatively low power supply voltages.

Voltage Divider Transistor Biasing



$$V_C = V_{CC} - R_C I_C = (V_E + V_{CE})$$
$$V_E = I_E R_E = V_B - V_{BE}$$
$$V_{CE} = V_C - V_E = V_{CC} - (I_C R_C + I_E R_E)$$
$$V_B = V_{BE} + V_E = V_{RB2} = \left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right) V_{CC}$$
$$I_{B2} = \frac{V_B}{R_{B2}}$$
$$I_{B1} = I_B + I_{B2} = \frac{V_{CC} - V_B}{R_{B1}}$$
$$R_B = \frac{R_{B1} \times R_{B2}}{R_{B1}+R_{B2}} \qquad I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta)R_E}$$
$$I_C = \beta_{(DC)} I_B$$
$$I_E = I_C + I_B = \frac{V_E}{R_E}$$

Here the common emitter transistor configuration is biased using a voltage divider network to increase stability. The name of this biasing configuration comes from the fact that the two resistors R_{B1} and R_{B2} form a voltage or potential divider network across the supply with their center point junction connected the transistors base terminal as shown.

This voltage divider biasing configuration is the most widely used transistor biasing method. The emitter diode of the transistor is forward biased by the voltage value developed across resistor R_{B2}. Also, voltage divider network biasing makes the transistor circuit independent of changes in beta as the biasing voltages set at the transistors base, emitter, and collector terminals are not dependant on external circuit values.

To calculate the voltage developed across resistor R_{B2} and therefore the voltage applied to the base terminal we simply use the voltage divider formula for resistors in series.

Generally the voltage drop across resistor R_{B2} is much less than for resistor R_{B1}. Clearly the transistors base voltage V_B with respect to ground, will be equal to the voltage across R_{B2}.

The amount of biasing current flowing through resistor R_{B2} is generally set to 10 times the value of the required base current I_B so that it is sufficiently high enough to have no effect on the voltage divider current or changes in Beta.

The goal of **Transistor Biasing** is to establish a known quiescent operating point, or Q-point for the bipolar transistor to work efficiently and produce an undistorted output signal. Correct DC biasing of the transistor also establishes its initial AC operating region with practical biasing circuits using either a two or four-resistor bias network.

In bipolar transistor circuits, the Q-point is represented by (V_{CE}, I_C) for the NPN transistors or (V_{EC}, I_C) for PNP transistors. The stability of the base bias network and therefore the Q-point is generally assessed by considering the collector current as a function of both Beta (β) and temperature.