Interrupts in 8085

MICROPROCESSORS(TCS403)

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Interrupts

- When microprocessor receives any interrupt signal from peripheral(s) which are requesting its services, it stops its current execution and program control is transferred to a sub-routine by generating CALL signal and after executing sub-routine by generating RET signal again program control is transferred to main program from where it had stopped.
- When microprocessor receives interrupt signals, it sends an acknowledgement (INTA') to the peripheral which is requesting for its service.

Different Types of Interrupts

- Hardware and Software Interrupts –

When microprocessors receive interrupt signals through pins (hardware) of microprocessor, they are known as Hardware Interrupts.

There are 5 Hardware Interrupts and

these are INTR, RST 7.5, RST 6.5, RST 5.5, TRAP

Software Interrupts are those

which are inserted in between

the program which means these

are mnemonics of microprocessor.

There are 8 software interrupts. They are

RST 0, RST 1, RST 2, RST 3, RST 4,

RST 5, RST 6, RST 7.

Vector Addresses are calculated by the formula 8 * TYPE

INTERRUPT	VECTOR ADDRESS
RST 0	00 H
RST 1	08 H
RST 2	10 H
RST 3	18 H
RST 4	20 H
RST 5	28 H
RST 6	30 H
RST 7	38 H

Vectored and Non-Vectored Interrupts

Vectored Interrupts are those which have fixed vector address (starting address of sub-routine) and after executing these, program control is transferred to that address.

Non-Vectored Interrupts are those in which vector address is not predefined. The interrupting device gives the address of sub-routine for these interrupts. INTR is the only non-vectored interrupt in 8085 microprocessor.

INTERRUPT	VECTOR ADDRESS
TRAP (RST 4.5)	24 H
RST 5.5	2C H
RST 6.5	34 H
RST 7.5	3C H

Maskable and Non-Maskable Interrupts

- Maskable Interrupts are those which can be disabled or ignored by the microprocessor. These interrupts are either edge-triggered or level-triggered, so they can be disabled. INTR, RST 7.5, RST 6.5, RST 5.5 are maskable interrupts in 8085 microprocessor.
- Non-Maskable Interrupts are those which cannot be disabled or ignored by microprocessor. TRAP is a non-maskable interrupt. It consists of both level as well as edge triggering and is used in critical power failure conditions.

Priority of Interrupts

When microprocessor receives multiple interrupt requests simultaneously, it will execute the interrupt service request (ISR) according to the priority of the interrupts.

INTERRUPT	Priority
TRAP	Highest
RST 5.5	2nd highest
RST 6.5	2nd lowest
RST 7.5	lowest