Graphic Era Hill University
TCS-308, Logic Design and Computer Organization
Practice Problems/Assignment no. 3,4&5

1. Use QM Method to simplify F(A,B,C,D)= ∑m(0,2,5,6,7,8,10,12,13,14,15) for minimal POS.
2. Use QM Method to simplify F(A,B,C,D)= ∑m(0,2,5,6,7,8,10,12,13,14,15)
3. Minimize the following 5 variable SOP function using K map:
   F(A,B,C,D,E)= ∑m(0,5,6,8,9,10,11,16,20,24,25,26,27)
4. $\bar{A}\,B + B\,\bar{C} + \bar{A}\,\bar{C}$, Implement this logic expression using NAND-NAND logic gates and NOR-NOR logic gates only
5. Design 4-bit magnitude comparator and draw its logic diagram.
6. Construct a 16X1 mux with required number of 4X1 mux and 2X1 mux.
7. Implement the following Boolean expression
   i) F(A,B,C,D)= ∑m(0,1,3,4,8,9,15) using 8X1 mux
   ii) F(A,B,C,D)= ∑m(1,3,4,11,12,13,14,15) using 4X1 mux
8. Obtain the Simplified Boolean expression and draw the logic circuit diagram for the following Truth table

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	1	0	0
1	1	1	1

9. Minimize the following 5 variable POS function using K map:
   f(A,B,C,D,E)= πM (0,5,6,8,9,10,11,16,20,24,25,26,27)

10. Design 4 bit BCD/Decimal Adder.
11. Design code convertors i) BCD to Excess-3 Convertor ii) 4 bit Binary to Gray Code iii) Gray to Binary. (iv) BCD to 7-segment code for common cathode

12. An 8 x 1 multiplexer has inputs X,Y, Z connected to selection inputs of S_2, S_1 and S_0 respectively. The data inputs I_0 through I_7 are as follows
    $I_1=I_2=1$; $I_3=I_7=0$; $I_4=I_5=\bar{C}$; and ; $I_0=I_6$ =C .Determine the Boolean function that a multiplexer implements.

13. Explain priority encoder.
14. Implement full adder using 4x1 mux and using 3x8 decoder.
15. Design a combinational circuits with three input and one output
    i) The output is 1 when the binary value of the inputs is less than 3. Otherwise output is 0
    ii) The output is 1 when the binary value of the input is an even number.
16. Explain different addressing modes.
17. Differentiate between
    i) RISC and CISC machines.
    ii) Von Neuman and Harvard Architecture
18. What is floating point representation in computer architecture? Explain floating point arithmetic with a flowcharts.

19. Design a circuit with optimum utilization of PLA to implement the following functions
    i) F1= ∑m(0,2,5,8,9,11), F2=∑m(1,3,8,10,13,15), F3=∑m(0,1,5,7,9,12,14).
    ii) F1(A, B, C) = ∑ m(1, 3, 6, 7) and F2(A, B, C) = ∑ m(0, 2, 4, 5) using PLA.
20. Discuss Amdahl's Law.
21. Explain instruction cycle with timing diagram.
22. Discuss memory hierarchy design and its characteristics.
23. Design a 4-bit synchronous counter using D-flip flop.
24. Design mod-10 synchronous counter using JK-flip flop.
25. Draw the logic diagram of four bit binary ripple countdown counter using
    i) Flip flop that trigger on the positive-edge of the clock
    ii) Flip flop that trigger on the negative-edge of the clock
26. Explain universal shift register.
27. Explain the Johnson Counter with logic diagram
    Explain the following with flow chart approach
    i) Direct memory access
    ii) Interrupt driven I/O
    iii) Programmed I/O
28. Discuss Booth algorithm for multiplication with flowchart.
29. Answer the following questions on floating-point representation:
    i) Convert AD51001016 to an IEEE single-precision floating-point number.
    ii) Convert the following IEEE single-precision floating-point number to a decimal number: 10111111110100000000000000000000.