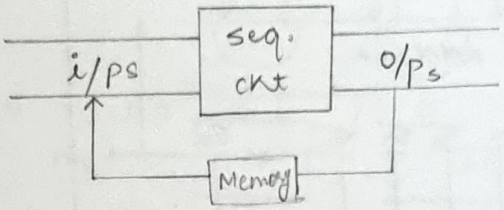
9th September, 23

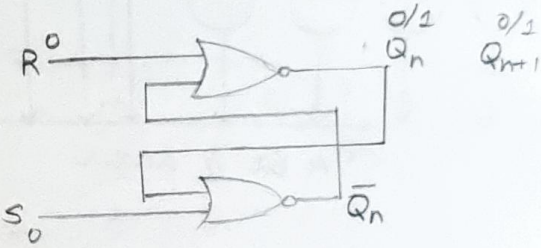
SEQUENTIAL CIRCUITS:

→ In sequential circuit, there is a feedback path b/w outputs and inputs. It means output depends upon present state as well as past outputs.



R-S latch

R (→Reset)	S (→Set)	Q_{n+1}	Comment
0	0	Q_n	No change (Memory is retained)
0	1	1	Set
1	0	0	Reset
1	1	X	Invalid / Forbidden / Indeterminate



* If Q_n and $\bar{Q}_n$ same, then it is invalid condition.

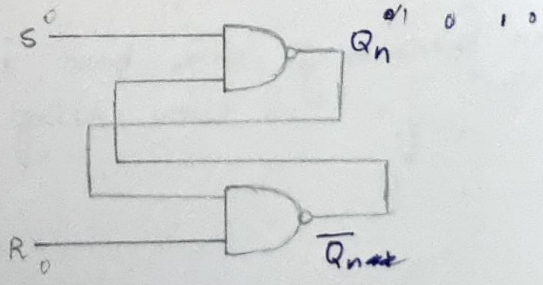
→ If any 1 input of NOR gate is high, then the output will be low irrespective of other inputs value.

→ Set condition $(Q_n = 1) \& (\bar{Q}_n = 0) \rightarrow S = 1$

→ Reset condition $(Q_n = 0) \& (\bar{Q}_n = 1) \rightarrow R = 1$

NAND Based S-R latch

S	R	Q_{n+1}	Comment
0	0	X	Invalid
0	1	1	Set
1	0	0	Reset
1	1	Q_n	No change



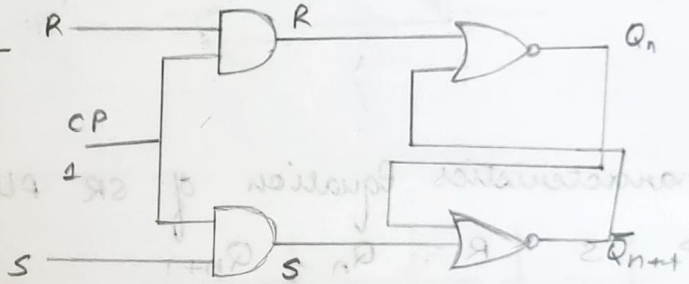
→ If we apply a clock pulse (CP) in latch, it becomes flip-flop.

Flip-flop

- It is the smallest unit of memory * it stores one bit at a time.
- It has two stable states that's why it is also called bi-stable multi-vibrator.
- It has two outputs and both are complement of each other. If both are same, then this condition is known as Invalid condition.
- If $Q_{n+1} = 1$ and $\overline{Q_{n+1}} = 0$, this is called Set condition.
- If $Q_{n+1} = 0$ and $\overline{Q_{n+1}} = 1$, this is called Reset / (unset) condition.

R-S Flip-Flop:

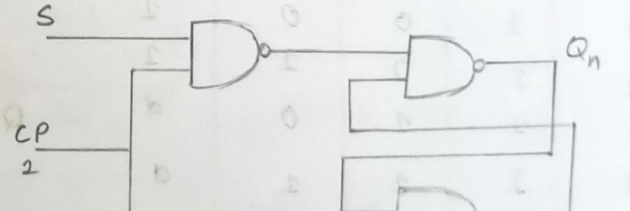
CP	R	S	Q_{n+1}	Comment
0	X	X	FF doesn't work	—
1	0	0	Q_n	No change
1	0	1	1	Set
1	1	0	0	Reset
1	1	1	X	Invalid



NOR Based R-S Flip-Flop

NAND Based SR FF :-

CP	R	S	Q_{n+1}	Comment
0	X	X	won't work	—
1	0	0	Q_n	No change
1	0	1	1	Set
1	1	0	0	Reset
1	1	1	X	Invalid

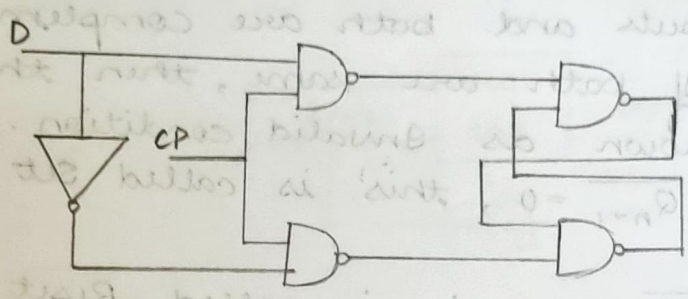


D flip flop (DFF):-

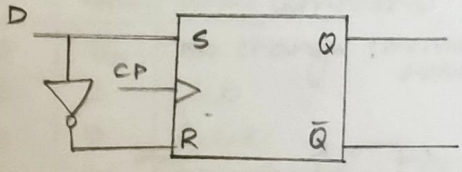
- We are getting stable output when both inputs are complement of each other in SR flip flop.

$S = D$

$R = \bar{D}$



Block diagram :



CP	D	Q_{n+1}
1	0	0
1	1	1

$\boxed{Q_{n+1} = D}$

Characteristics Equation of SR Flip Flop.

CP	S	R	Q_n	Q_{n+1}
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	d
1	1	1	1	d

S \ RQ_n	00	01	11	10
0		1		
1	1	1	d	d

$Q_{n+1} = S + \bar{R}Q_n$

C.Eq^n = $Q(n+1) = f(\text{F.F. I/P's}, Q_n)$

DFF :-

CP	D	Q_n	Q_{n+1}
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

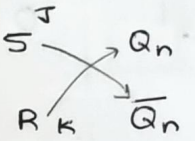
$Q_{n+1} = D$

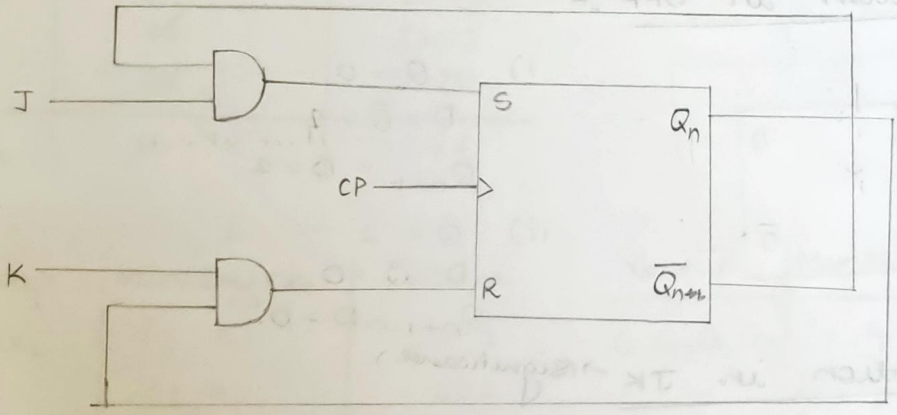
From Truth Table.

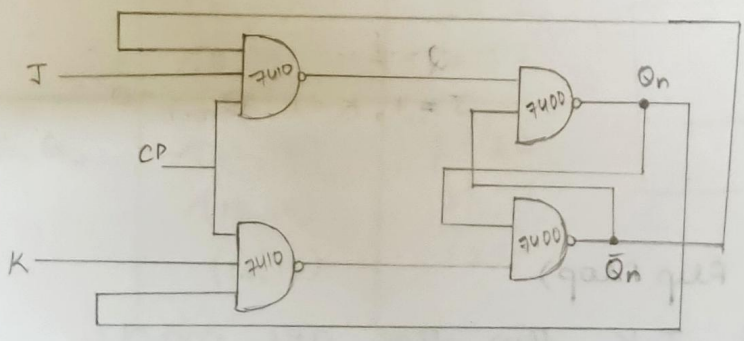
J K flip flop :-

$S = J\overline{Q_n}$

$R = KQ_n$







CP	J	K	Q_{n+1}	
0	X	X	Q_n	
1	0	0	Q_n	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q_n}$	Toggle.

$J = 0$, $K = 0$

If $Q_n = 0$, $Q_{n+1} = 0$

$Q_n = 1$, $Q_{n+1} = 1$

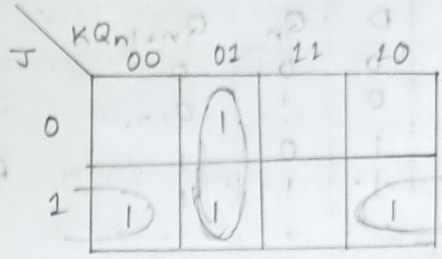
$J = 1$, $K = 1$

$Q_n = 0$, $Q_{n+1} = 1$

$Q_n = 1$, $Q_{n+1} = 0$

Characteristic Table :-

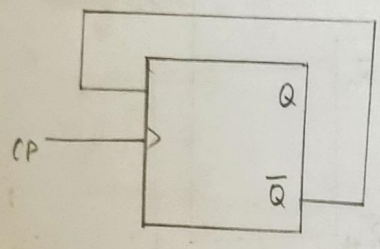
CP	J	K	Q_n	Q_{n+1}
	0	0	0	0
	0	0	1	1
	0	1	0	0
	0	1	1	0
	1	0	0	1
	1	0	1	1
	1	1	0	1
	1	1	1	0



Characteristic Eqn :-

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

Toggle condition in DFF :-



i) $Q = 0$

$D = \bar{Q} = 1$

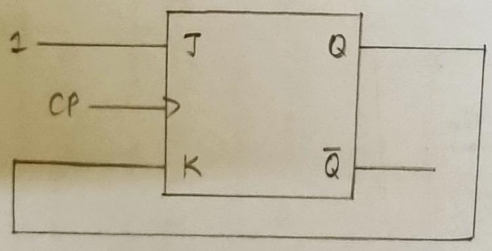
$Q_{n+1} = D = 1$

ii) $Q = 1$

$D = \bar{Q} = 0$

$Q_{n+1} = D = 0$

Toggle condition in JK → (significance)



$Q = 0$

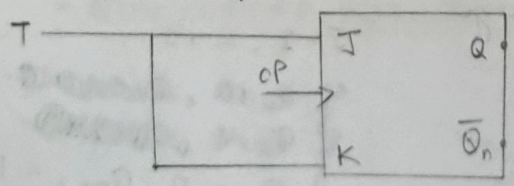
$J = 1, K = 0, Q_{n+1} = 1$

$Q = 1$

$J = 1, K = 1 \quad Q_{n+1} = 0$

T Flip-Flop (Toggle Flip Flop)

→ If both inputs of J-K flip flop are made common and connected to T input, it becomes T flip flop.



CP	T	Q_{n+1}	
ϕ	0	Q_n	No change
↓	1	$\bar{Q}_n$	Toggle

$$Q_{n+1} = T \oplus Q_n$$

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UNIT - 2

Characteristics Table (CT)

DFF

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

TFF

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Property of XOR :-

* If $a \oplus b = c$
  $c \oplus b = a$
  $a \oplus c = b$

SR FF

	S	R	Q_n	Q_{n+1}
→	0	0	0	0
	0	0	1	1
→	0	1	0	0
	0	1	1	0
	1	0	0	1
	1	0	1	1
	1	1	0	d
	1	1	1	d

Excitation Table (ET)

Q_n	Q_{n+1}	$D \rightarrow Q_{n+1}$
0	0	0
0	1	1
1	0	0
1	1	1

Q_n	Q_{n+1}	$T \rightarrow Q_n \oplus Q_{n+1}$
0	0	0
0	1	1
1	0	1
1	1	0

$Q_n + 1 = T \oplus Q_n$

$T = Q_n \oplus Q_n + 1$

Q_n	Q_{n+1}	S	R
0	0	0	d
0	1	1	0
1	0	0	1
1	1	d	0

↓ change 0 to d in middle

JK Flip Flop

Q_n	Q_{n+1}	J	K
0	0	0	d
0	1	1	d ←
1	0	d	1 ←
1	1	d	0

Flip Flop conversion :-

1. Convert D flip-flop into T flip flop.

D to T
↓ ↓
available required.

STEP 1 : Draw characteristics Table of required FF and excitation table of available FF and combine these two table.

STEP 2: Now with the help of Boolean Algebra or K-Map determine available flip flop inputs, which are function of present state (Q_n) and required flip flop inputs.

STEP 3: with the help of available FF and suitable logic gates, draw required FF.

CT (T) ET (D)

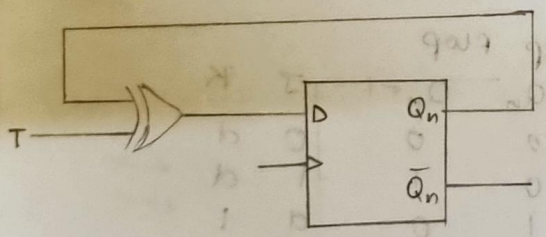
T	Q_n	Q_n+1	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

~~ET (D)~~

~~Q_n Q_{n+1} D~~

T \ Q_n	0	1
0		1
1	1	

$D = T \oplus Q_n$



2. Convert SR to JK flip flop.

CT (JK) ET (SR)

J	K	Q_n	Q_n+1	S	R
0	0	0	0	0	d
0	0	1	1	d	0
0	1	0	0	0	d
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	d	0
1	1	0	1	1	0
1	1	1	0	0	1

J \ KQ_n	00	01	11	10
0		X		
1	1	X		1

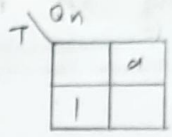
$S = J\bar{Q}_n$

J \ KQ_n				
	X		1	X
			1	

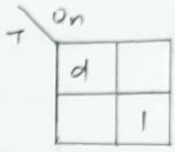
$R = KQ_n$

3° Convert SR to T.

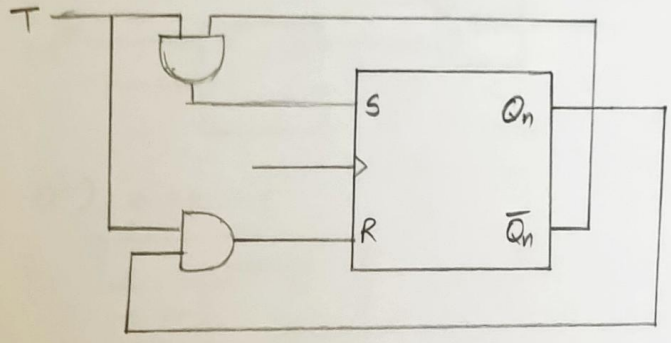
T	Q_n	Q_n+1	S	R
0	0	0	0	d
0	1	1	d	0
1	0	1	1	0
1	1	0	0	1



$S = T\bar{Q}_n$



$R = TQ_n$



4° Convert DFF into JK FF.

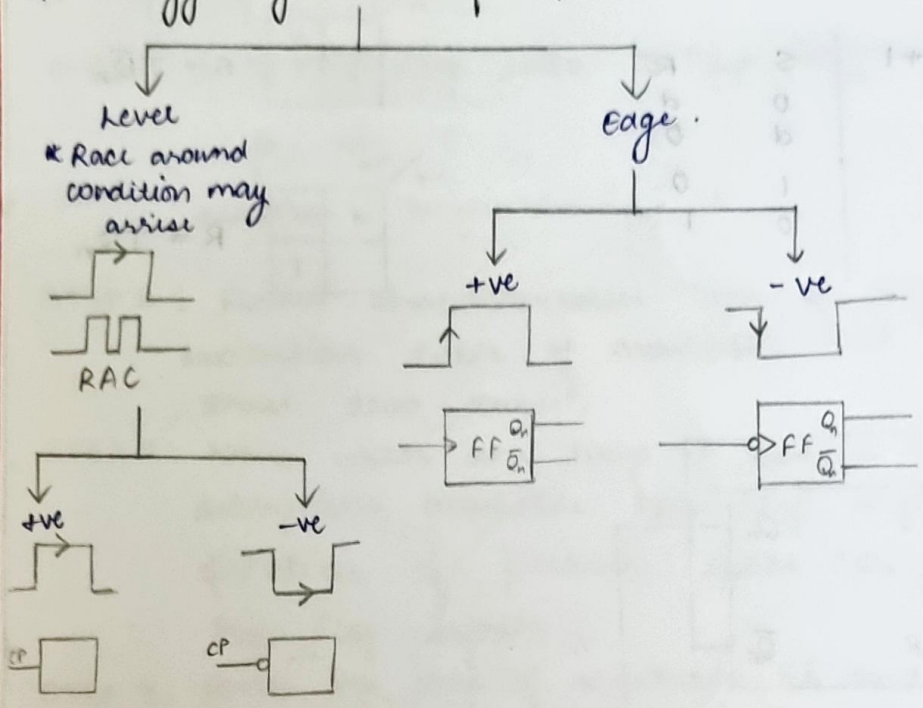
J	K	Q_n	Q_n+1	D (Q_{n+1})
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

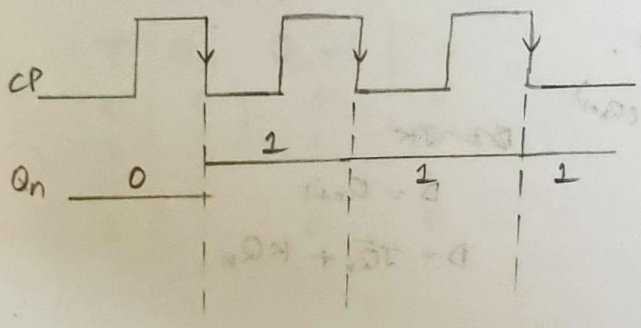
~~B = JK~~

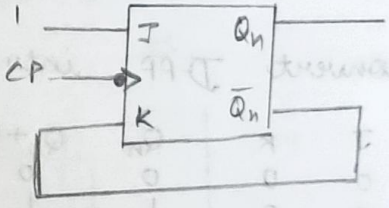
$D = Q_{n+1}$

$D = J\bar{Q}_n + KQ_n$

Triggering in Flip Flop.







$J = 1 \quad \overline{1}$

$K = \overline{Q}_n = \overline{0} = 1 \quad 0$

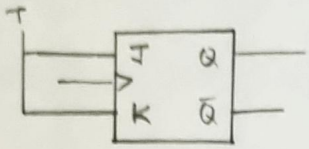
* When output changes many times in single clock pulse (CP), this condition is called race-around condition.
* RAC arises due to
  i) Level triggering either +ve or -ve.
  ii) when propogation delay of FF < ~~prop~~ pulse width of CP.

Total time req. to propogate any signal from I/p to O/p

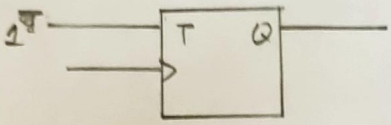
Q Draw FF circuits which ~~keeps~~ gives Toggle condition or output frequency is input frequency divided by?

i.e. $f_o = f_i/2$

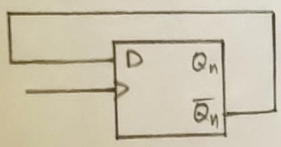
i) J = K = 1



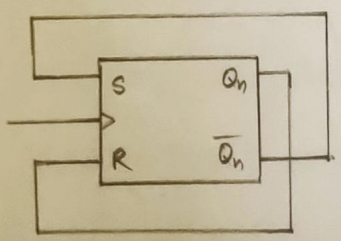
ii) T- FF



iii) D-FF (T)

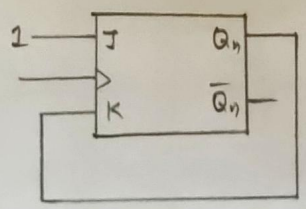


iv) SR.



$Q_n = 0$
$S = 1$
$R = Q_n = 0$
$Q_n + 1 = 1$

v)



vi)