Electrical and Computer Engineering
University of Thessaly (UTH)

ECE327 - VLSI

Fall Semester — Educational year 2022-2023

Lab01

CMOS Inverter Design & Simulation

Georgios Kapakos - AEM: 03165

Contents

Introduction

This assignment focuses on the design, extraction, and simulation of a CMOS inverter using SPICE. The tasks involve creating a schematic, extracting it into a SPICE netlist, verifying transistor connections, and performing transient analysis to measure key timing parameters such as propagation delays and rise/fall times. The goal is to understand the behavior of CMOS circuits and validate their functionality through simulation and graphical representation.

1 Exercise 1: CMOS Inverter Schematic

Initially, the `.spice` file is extracted as follows. After extraction, the resulting file cannot run directly in NGSPICE, so it requires modification.

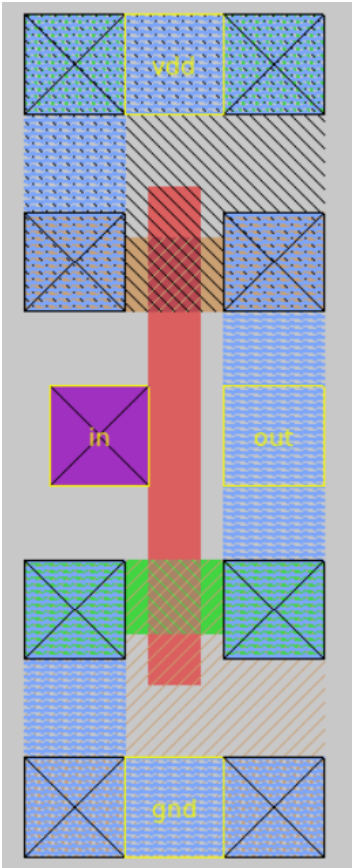

Figure 1: CMOS Inverter

From the code below, we conclude that the transistor terminals are correctly connected:

- **nMOS (M1000)**: Drain to output, gate to input, source and bulk to `vdd`.
- **pMOS (M1001)**: Drain to output, gate to input, source and bulk to ground.

exercise1.spice

```
gkapakos@LAPTOP-L3SKMRC7: /mnt/c/WINDOWS/system32
* SPICE3 file created from exercise1.ext - technology: scmos

.option scale=1u

M1000 out in vdd vdd pfet w=3 l=2
+  ad=19 pd=18 as=19 ps=18
M1001 out in gnd gnd nfet w=3 l=2
+  ad=19 pd=18 as=19 ps=18
C0 in 0 3.64fF
```

Figure 2: Spice code for the circuit

2 Exercise 2: Modified SPICE File and Timing Measurements

The modified `.spice` file is prepared for transient analysis. To measure propagation delays (`tphl`, `tplh`) and rise/fall times (`trise`, `tfall`), we adjust the models, add `.tran` commands, and use `.meas` to capture the required timing values.

exercise1.spice

```
gkapakos@LAPTOP-L3SKMRC7: /mnt/c/WINDOWS/system32/spice_excercises

Circuit: ****askisi 1****

Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Warning: vin: no DC value, transient time 0 value used

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vs                                         2.5
out                                        2.5
in                                           0
vin#branch                                   0
vdd#branch                          -5.27718e-12


No. of Data Rows : 620

  Measurements for Transient Analysis

t_phl               =  6.288096e-10 targ=  7.538096e-10 trig=  1.250000e-10
t_plh               =  7.607324e-10 targ=  1.885732e-09 trig=  1.125000e-09
t_rise              =  5.623999e-10 targ=  2.159177e-09 trig=  1.596777e-09
t_fall              =  3.037825e-10 targ=  9.487381e-10 trig=  6.449556e-10
```

Figure 3: Measurements for the transient analysis in spice.

Timing Measurements

Rise Time (`trise`)

To calculate `trise`, we determine the output rise time from 10% of `vdd` (0.25V) to 90% of `vdd` (2.25V) during the first rising edge (rise = 1). Using the points:

- $x_2 = 300$, $x_1 = 100$, $y_2 = 2.25$, $y_1 = 0.25$

Slope:

$$\lambda_1 = \frac{y_2 - y_1}{x_2 - x_1} = \frac{2}{200} = 0.01$$

Equation:

$$y = 0.01x - 0.75$$

- For $y = 0$: $x = 75$ ps (10% of `vdd`)
- For $y = 2.5$: $x = 325$ ps (90% of `vdd`)

Fall Time (`tfall`)

To calculate `tfall`, we determine the output fall time from 90% of `vdd` (2.25V) to 10% of `vdd` (0.25V) during the first falling edge (fall = 1). Using the points:

- $x_2 = 1150$, $x_1 = 950$, $y_2 = 0.25$, $y_1 = 2.25$

Slope:

$$\lambda_1 = \frac{y_2 - y_1}{x_2 - x_1} = \frac{-2}{200} = -0.01$$

Equation:

$$y = -0.01x + 11.75$$

- For $y = 0$: $x = 1175$ ps (10% of `vdd`)
- For $y = 2.5$: $x = 925$ ps (90% of `vdd`)

Propagation Delays (`tphl` and `tplh`)

- **`tplh`**: Time between 50% of `vdd` (1.25V) at the input (first fall, fall = 1) and 50% of `vdd` (1.25V) at the output (first rise, rise = 1).
- **`tphl`**: Time between 50% of `vdd` (1.25V) at the input (first rise, rise = 1) and 50% of `vdd` (1.25V) at the output (first fall, fall = 1).

Graphical Representation of CMOS Inverter

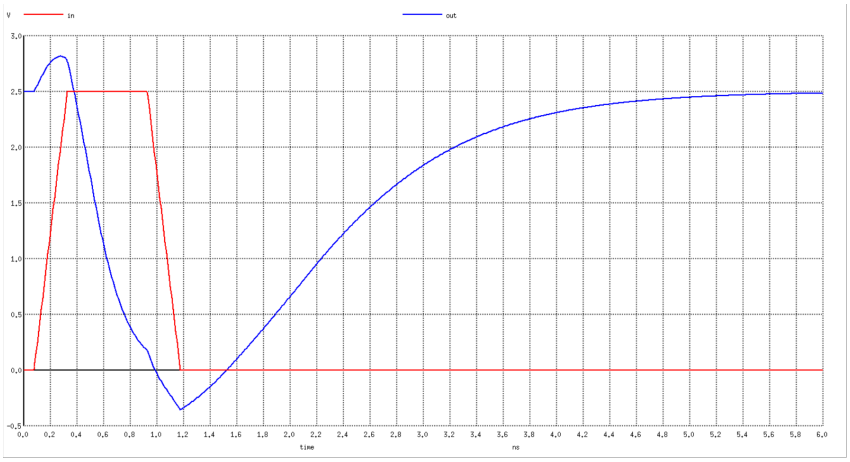

Figure 4: CMOS Inverter plot

Conclusion

This assignment successfully demonstrates the design and simulation of a CMOS inverter. The extraction process verified correct transistor connections, while the transient analysis provided accurate measurements of rise/fall times and propagation delays. The calculated values and waveforms confirm the inverter's functionality, offering insights into CMOS circuit performance and timing characteristics critical for VLSI design.