



Electrical and Computer Engineering  
University of Thessaly (UTH)

## **ECE327 - VLSI**

Fall Semester — Educational year 2022-2023

### **Lab03**

## **CMOS Logic Gate Design and Analysis**

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# Introduction

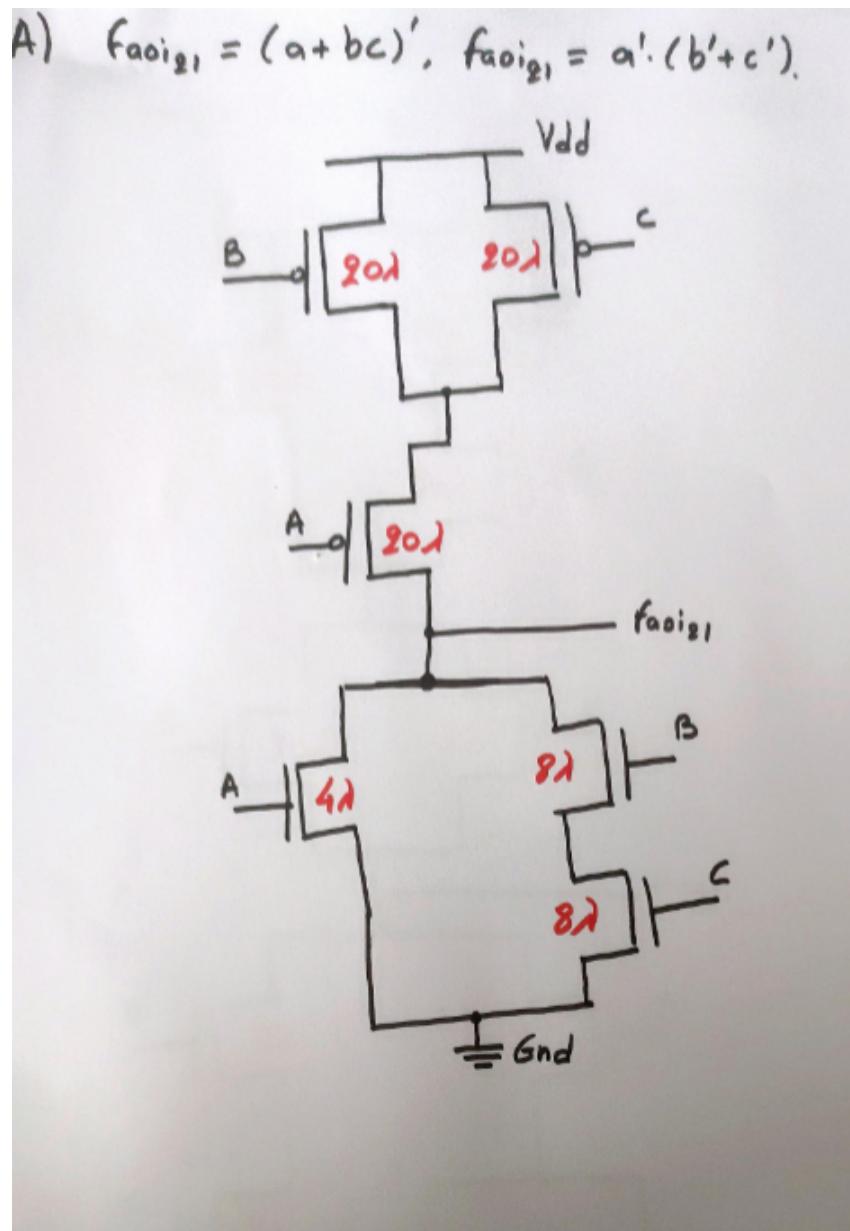
This assignment focuses on designing and analyzing combinational CMOS logic gates based on given Boolean functions. The tasks include schematic design with transistor sizing, stick diagram creation, layout implementation in Magic, capacitance calculations, and delay analysis using the Elmore model. The goal is to implement efficient CMOS circuits and verify their functionality and performance.

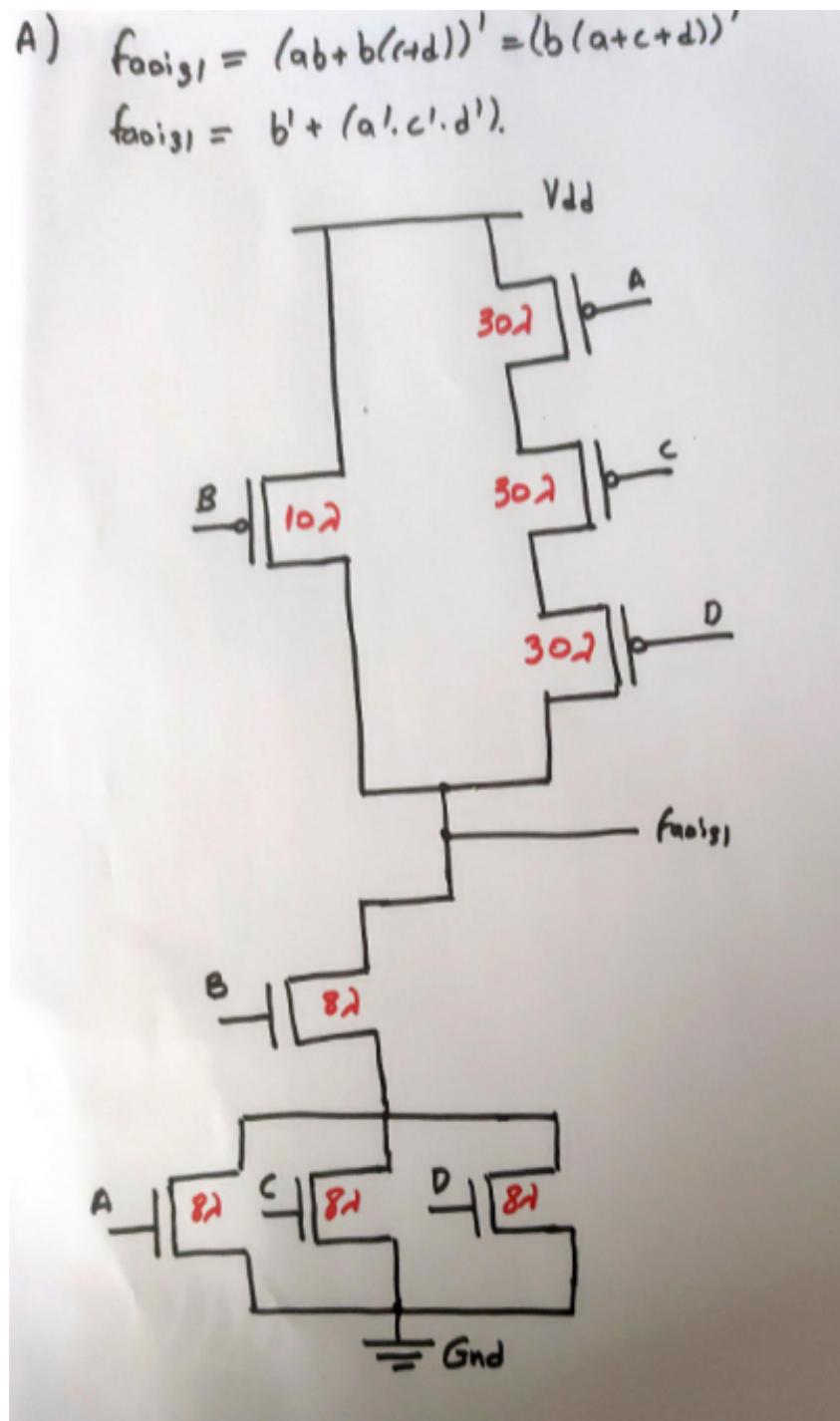
## 1 Exercise 1

### 1.1 (a) Schematic Design and Transistor Sizing

The following Boolean functions are implemented as static CMOS gates:

- $f_{aoi21} = (a + bc)'$
- $f_{aoi31} = (ab + b(c + d))'$
- $f_{maj} = (ab + bc + ac)'$
- $f_{aoi22} = (ac + bd)'$

1.1.1 faoi<sub>21</sub>Figure 1: faoi<sub>21</sub>

1.1.2 faoi<sub>31</sub>Figure 2: faoi<sub>31</sub>

## 1.1.3 fmag

A)  $f_{maj} = (ab + bc + ac)' = (a(b+c) + bc)'$   
 $f_{maj} = (a' + b') \cdot (b' + c') \cdot (a' + c') = (a' + (b' \cdot c')) \cdot (b' + c')$ .

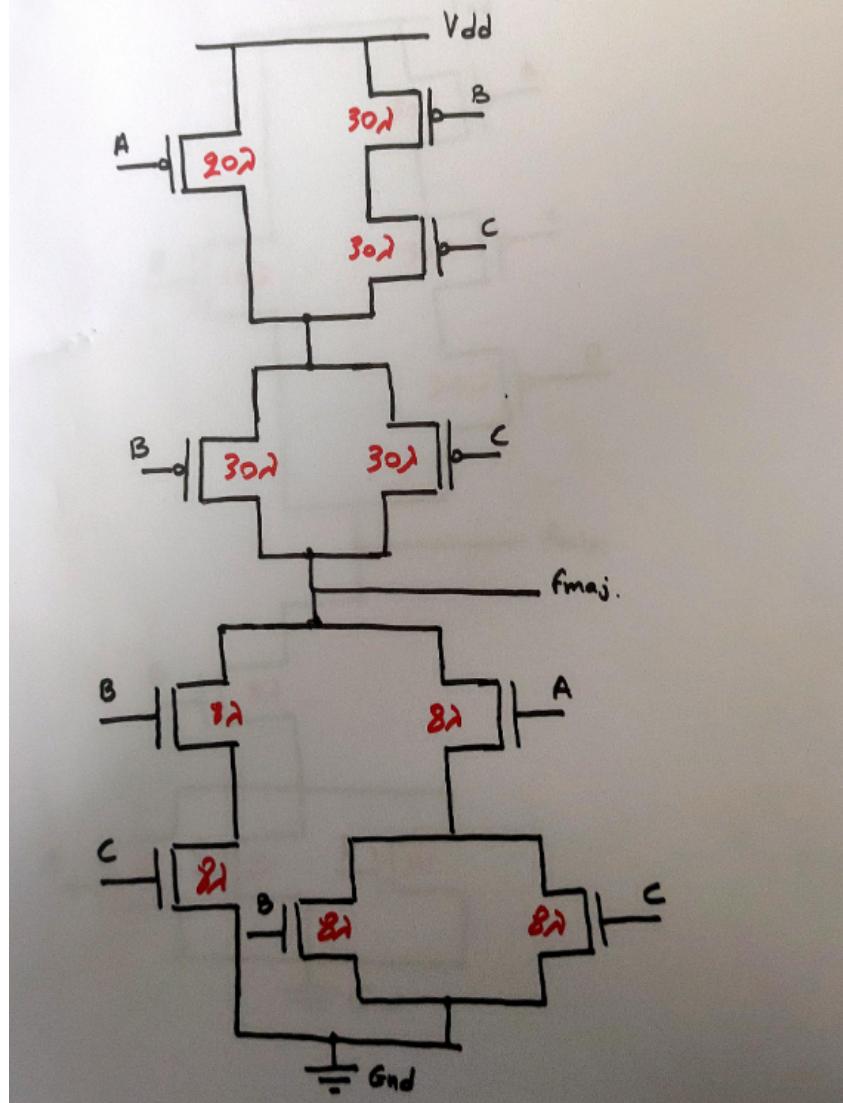
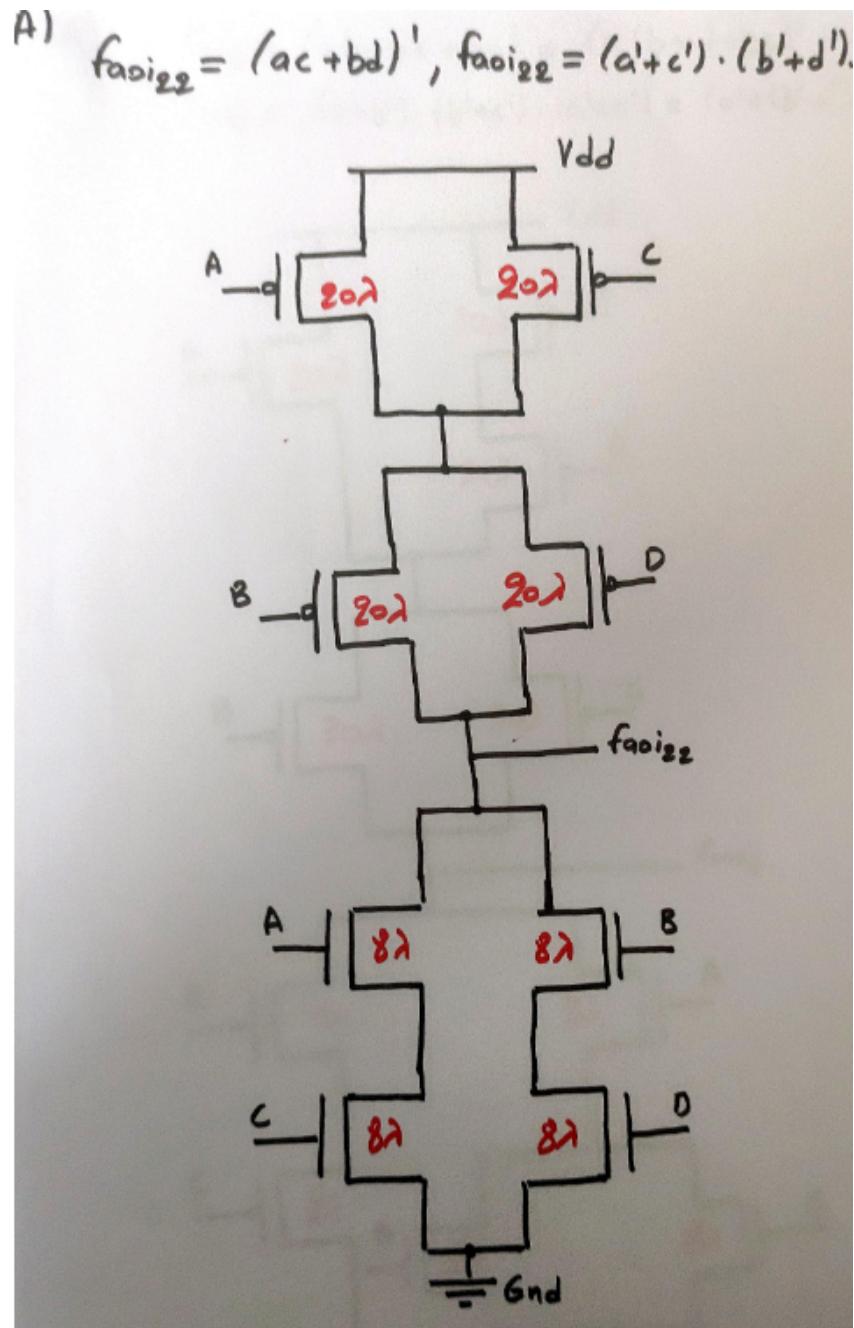


Figure 3: fmag

1.1.4 faoi<sub>22</sub>Figure 4: faoi<sub>22</sub>

**Transistor Sizing:** Transistor width is inversely proportional to resistance. Given:

- NMOS:  $R_n = 13 \text{ k}\Omega$ , minimum width  $W_n = 2\lambda \cdot 2 = 4\lambda$  (since pull-down resistance target is  $6.5 \text{ k}\Omega$ ,  $13/6.5 = 2$ ).
- PMOS:  $R_p = 31 \text{ k}\Omega$ , minimum width  $W_p = 2\lambda \cdot 5 = 10\lambda$  (since pull-up resistance target is  $6.5 \text{ k}\Omega$ ,  $31/6.5 \approx 5$ ).

Thus,  $W_n = 4\lambda$ ,  $W_p = 10\lambda$ . For series transistors, widths are multiplied by the number of transistors in the path; parallel transistors retain their widths.

## 1.2 (b) Stick Diagrams

Stick diagrams for the functions are created using Euler paths to avoid breaks in n-diffusion and p-diffusion regions.

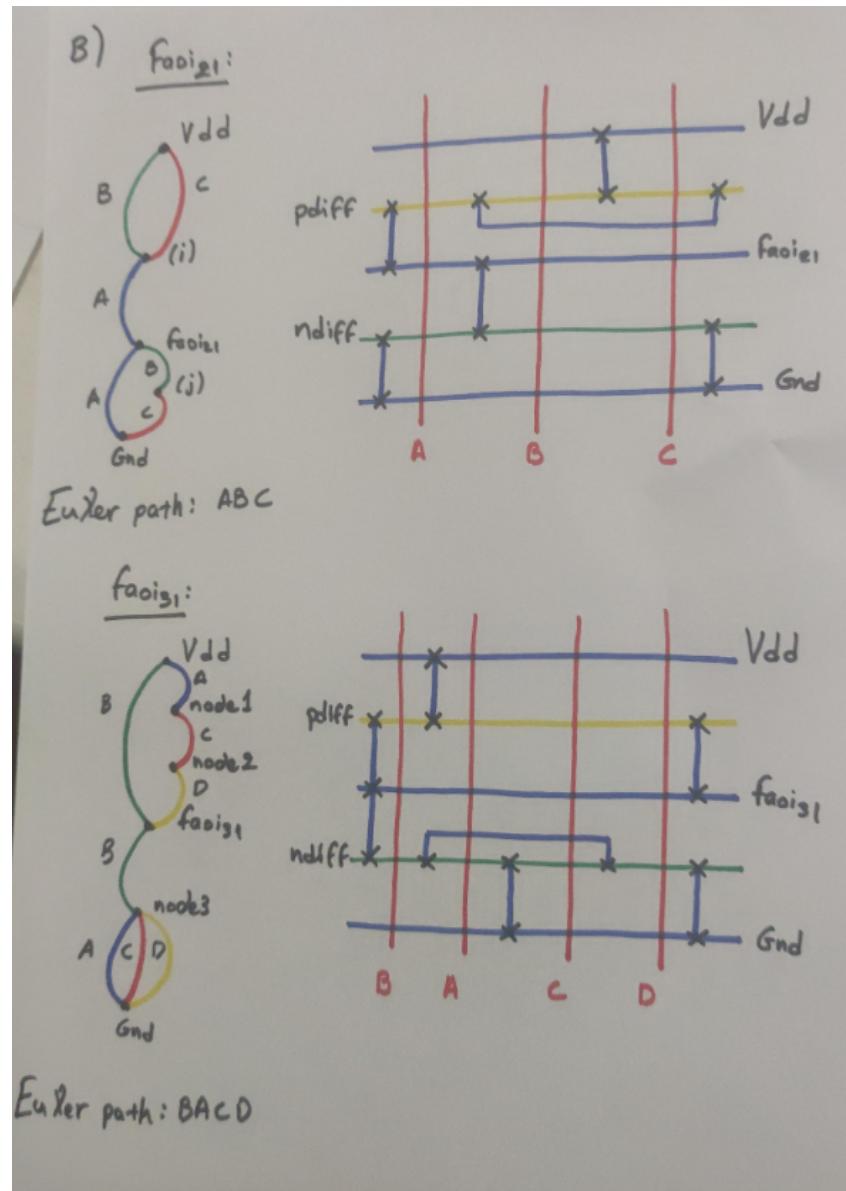
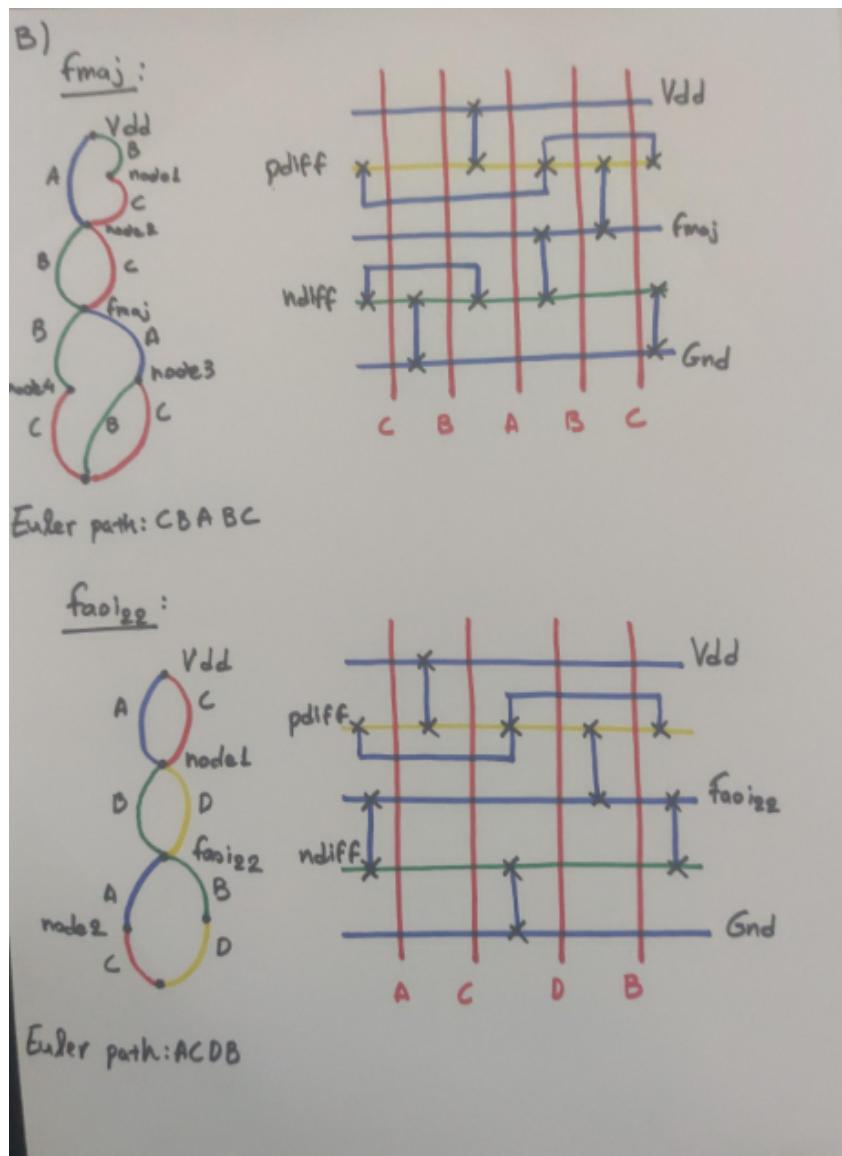


Figure 5:  $faoi_{21}$  &  $faoi_{31}$  stick diagrams

Figure 6: fmaj & faoi<sub>22</sub> stick diagrams

### 1.3 (c) Layout Design and Verification

Using Magic (SCMOS technology), layouts are derived from stick diagrams. Truth tables and NGSPICE waveforms verify functionality:

### 1.3.1 faoi<sub>21</sub>

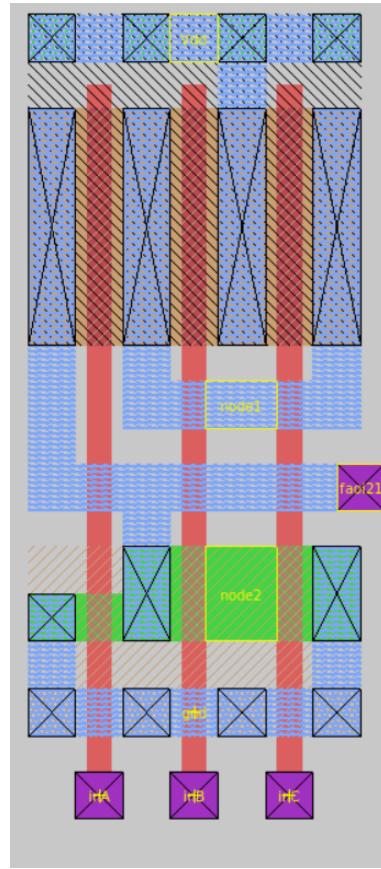


Figure 7: faoi<sub>21</sub> Magic

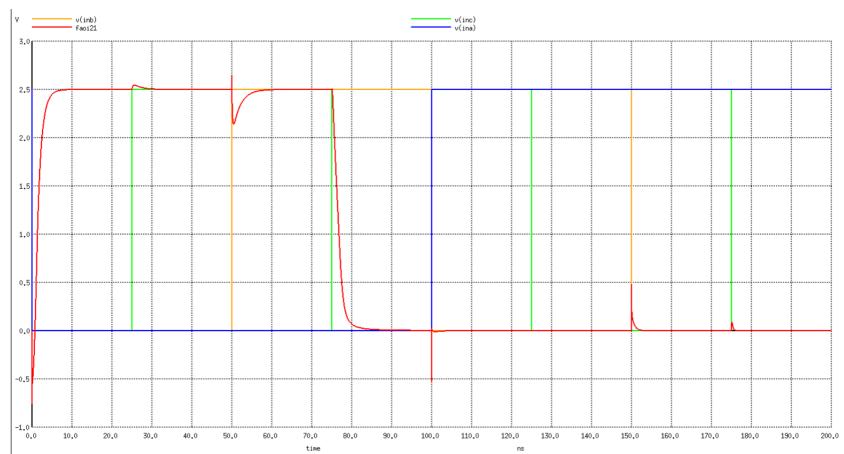


Figure 8: plot of faoi<sub>21</sub>

### 1.3.2 faoi<sub>31</sub>

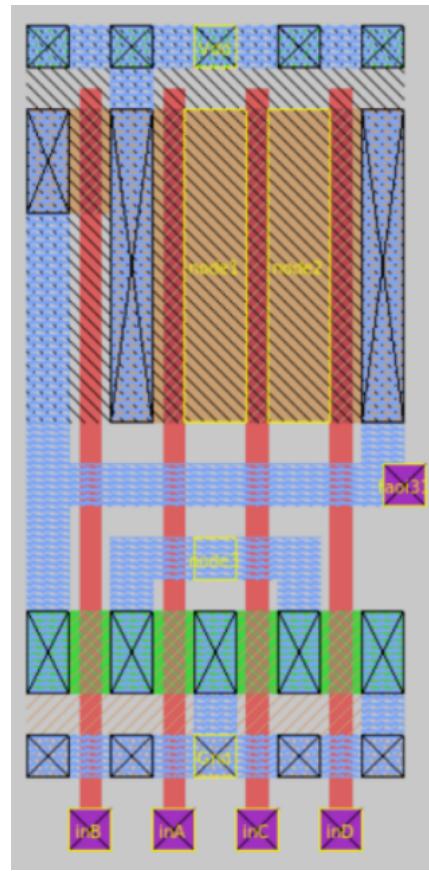


Figure 9: faoi<sub>31</sub> Magic

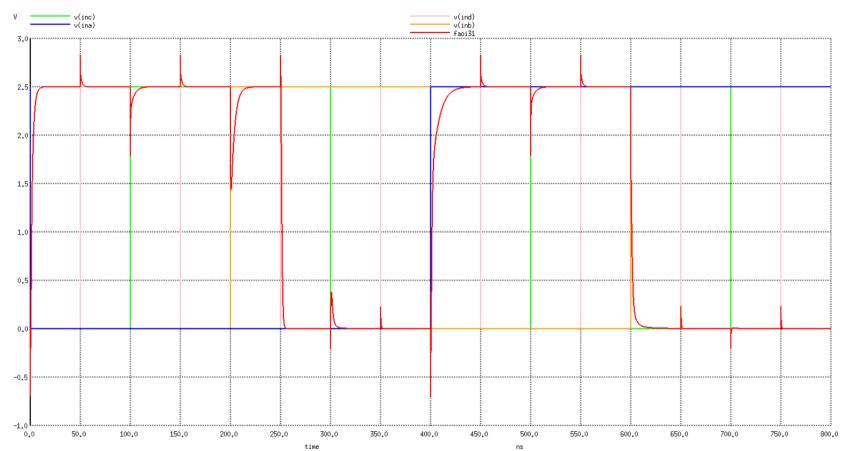


Figure 10: plot of faoi<sub>31</sub>

### 1.3.3 fmaj

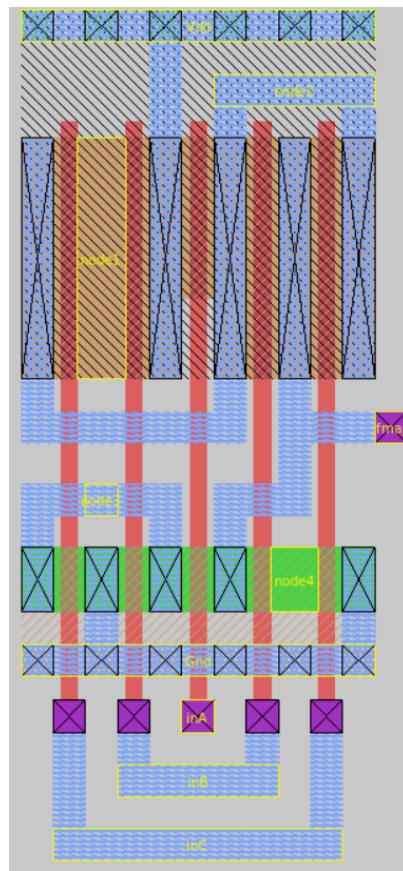


Figure 11: fmaj Magic

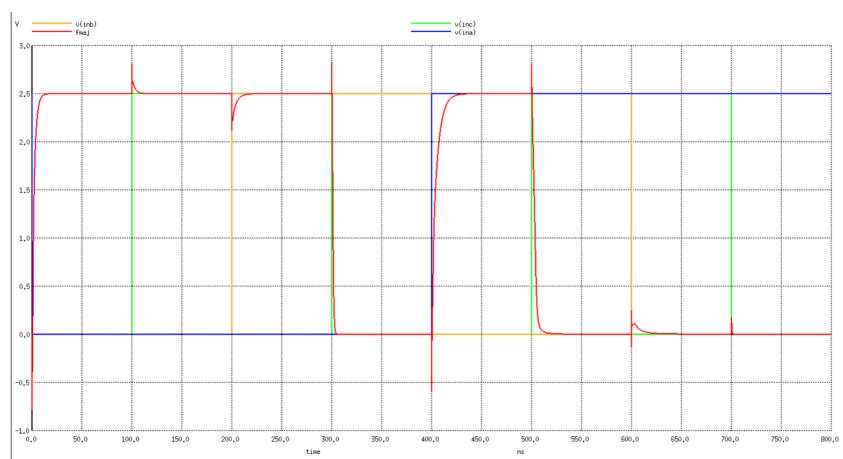


Figure 12: plot of fmaj

### 1.3.4 faoi<sub>22</sub>

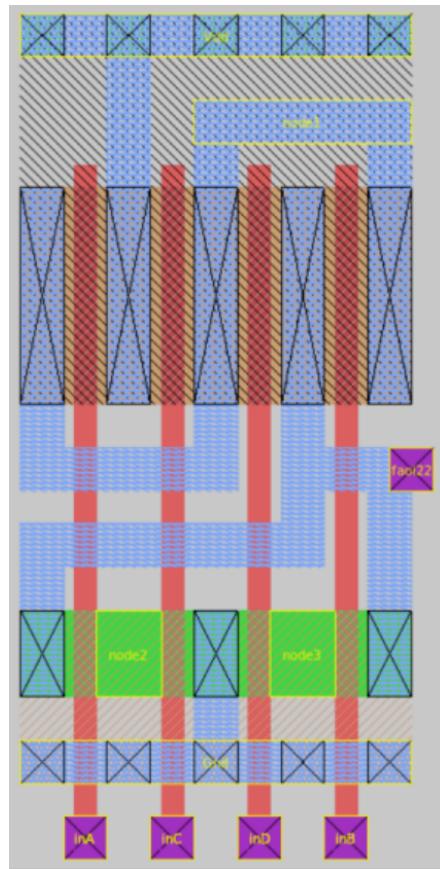


Figure 13: faoi<sub>22</sub>*Magic*

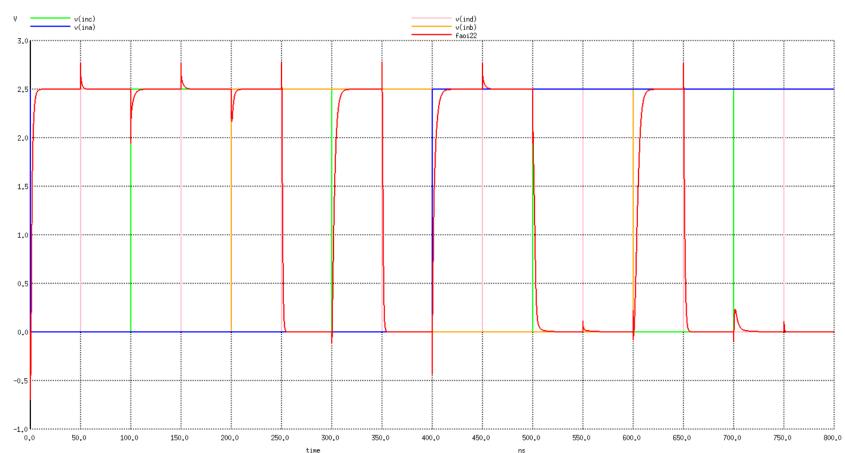


Figure 14: plot of faoi<sub>22</sub>

A	B	C	$f_{aoi21}$
0	0	0	1
0	0	1	1
0	1	0	1
• $f_{aoi21}$ :	0	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

A	B	C	D	$f_{aoi31}$
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
• $f_{aoi31}$ :	0	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

A	B	C	$f_{maj}$
0	0	0	1
0	0	1	1
0	1	0	1
• $f_{maj}$ :	0	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

- $f_{aoi22}$ :

A	B	C	D	$f_{aoi22}$
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

#### 1.4 (d) Capacitance Analysis for $f_{aoi21}$

Dimensions of transistors in  $f_{aoi21}$  are calculated by counting grid squares in Magic ( $\lambda = 0.125 \mu\text{m}$ ):

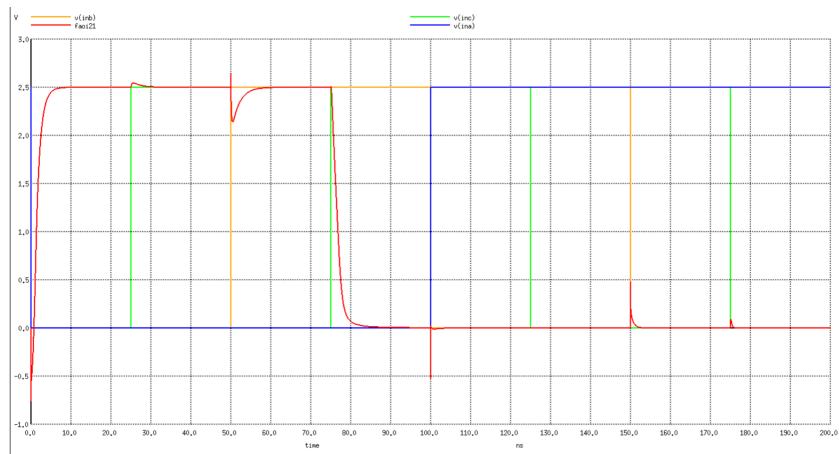


Figure 15: plot of faoi<sub>21</sub>

- Initial (in  $\lambda$ ):

Transistor	$W(\lambda)$	$AS(\lambda^2)$	$AD(\lambda^2)$	$PS(\lambda)$	$PD(\lambda)$
MNA	4	20	20	14	10
MNB	8	24	24	6	6
MNC	8	40	24	18	6
MPA	20	60	100	6	30
MPB	20	60	60	6	6
MPC	20	60	100	6	30

• Converted (in  $\mu\text{m}$ ):

Transistor	$W(\mu\text{m})$	$AS(\mu\text{m}^2)$	$AD(\mu\text{m}^2)$	$PS(\mu\text{m})$	$PD(\mu\text{m})$
MNA	0.5	0.3125	0.3125	1.75	1.25
MNB	1	0.375	0.375	0.75	0.75
MNC	1	0.625	0.375	2.25	0.75
MPA	2.5	0.9375	1.5625	0.75	3.75
MPB	2.5	0.9375	0.9375	0.75	0.75
MPC	2.5	0.9375	1.5625	0.75	3.75

### Diffusion Capacitances (1→0 Transition):

- PMOS:

$$C_{dbpA} = K_{pj} \cdot AD_p \cdot C_j + K_{pjsw} \cdot PD_p \cdot C_{jsw} = 0.79 \cdot 1.5625 \cdot 1.9 + 0.86 \cdot 3.75 \cdot 0.22 = 3.0548125 \text{ fF}$$

$$C_{sbpA} = 0.79 \cdot 0.9375 \cdot 1.9 + 0.86 \cdot 0.75 \cdot 0.22 = 1.5490875 \text{ fF}$$

$$C_{dbpB} = 0.79 \cdot 0.9375 \cdot 1.9 + 0.86 \cdot 0.75 \cdot 0.22 = 1.5490875 \text{ fF}$$

$$C_{dbpC} = 0.79 \cdot 1.5625 \cdot 1.9 + 0.86 \cdot 3.75 \cdot 0.22 = 3.0548125 \text{ fF}$$

- NMOS:

$$C_{dbnA} = K_{nj} \cdot AD_n \cdot C_j + K_{njsw} \cdot PD_n \cdot C_{jsw} = 0.57 \cdot 0.3125 \cdot 2 + 0.61 \cdot 1.25 \cdot 0.28 = 0.56975 \text{ fF}$$

$$C_{dbnB} = 0.57 \cdot 0.375 \cdot 2 + 0.61 \cdot 0.75 \cdot 0.28 = 0.5556 \text{ fF}$$

$$C_{sbnB} = 0.57 \cdot 0.375 \cdot 2 + 0.61 \cdot 0.75 \cdot 0.28 = 0.5556 \text{ fF}$$

$$C_{dbnC} = 0.57 \cdot 0.375 \cdot 2 + 0.61 \cdot 0.75 \cdot 0.28 = 0.5556 \text{ fF}$$

Source-to-bulk capacitances connected to  $V_{dd}$  or ground are omitted.

## 1.5 (e) Elmore Delay Analysis

For the  $f_{aoi21}$  pull-down network (worst-case), the path with two series NMOS transistors (B and C) is chosen, avoiding a single NMOS path to prevent a short circuit. Capacitances include  $C_{bc}$  (between B and C) and  $C_L$  (load, four identical gates = 25.8156 fF).

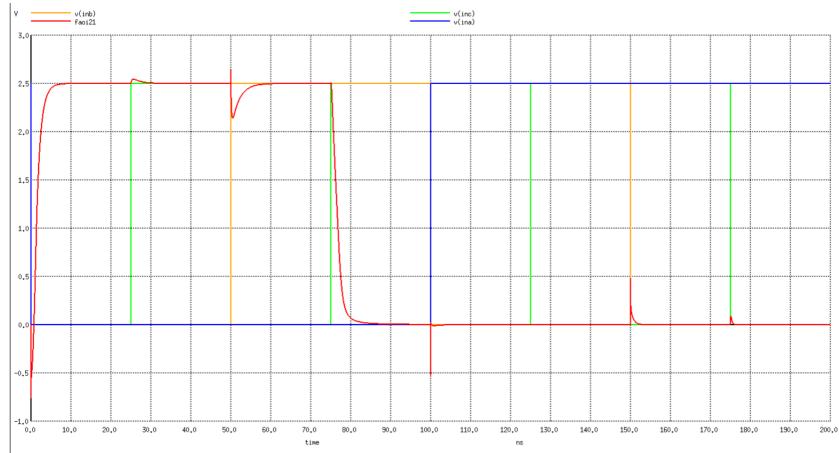


Figure 16: plot of  $f_{aoi21}$  connected

### Elmore Delay:

$$\tau = R_n \cdot (C_{bc} + C_L) + R_n \cdot C_L$$

Where  $R_n = 13 \text{ k}\Omega$ ,  $C_{bc} = C_{dbnB} + C_{sbnC} = 0.5556 + 1.7956 = 2.3512 \text{ fF}$ ,  $C_L = 25.8156 \text{ fF}$ :

$$\tau = 13 \cdot (2.3512 + 25.8156) + 13 \cdot 25.8156 = 707.7712 \text{ ps}$$

## Conclusion

This assignment successfully implemented CMOS logic gates for given Boolean functions, from schematic design to layout and performance analysis. Transistor sizing ensured target resistances, stick diagrams optimized diffusion continuity, and Magic layouts were verified with NGSPICE. Capacitance and delay calculations for  $f_{aoi21}$  provided insights into timing performance, reinforcing CMOS design principles.