



Electrical and Computer Engineering
University of Thessaly (UTH)

ECE327 - VLSI

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Lab02

Functional Verification and Timing Analysis

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Introduction

This assignment set explores the characteristics and behavior of CMOS transistors and inverters through SPICE simulations. It involves analyzing NMOS and PMOS transistor characteristics, calculating equivalent resistances, determining threshold voltages in series configurations, and evaluating the DC transfer characteristics and voltage scaling effects of a CMOS inverter. The objective is to deepen understanding of VLSI circuit design and performance metrics.

1 Exercise 1

1.1 (a) DC Analysis of NMOS and PMOS

After performing a .dc analysis in NGSPICE, the following plots of I_{ds} versus V_{ds} and V_{gs} are obtained for NMOS and PMOS transistors:

- NMOS: I_{ds}/V_{ds} , I_{ds}/V_{gs}
- PMOS: I_{ds}/V_{ds} , I_{ds}/V_{gs}

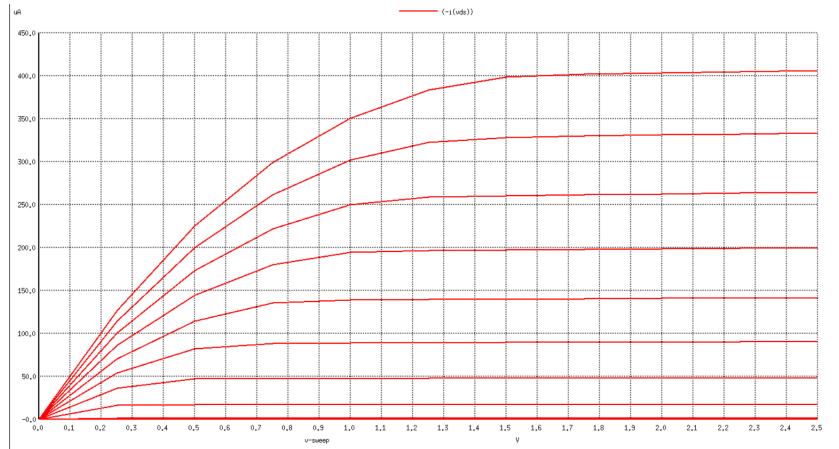


Figure 1: nMOS I_{ds}/V_{ds}

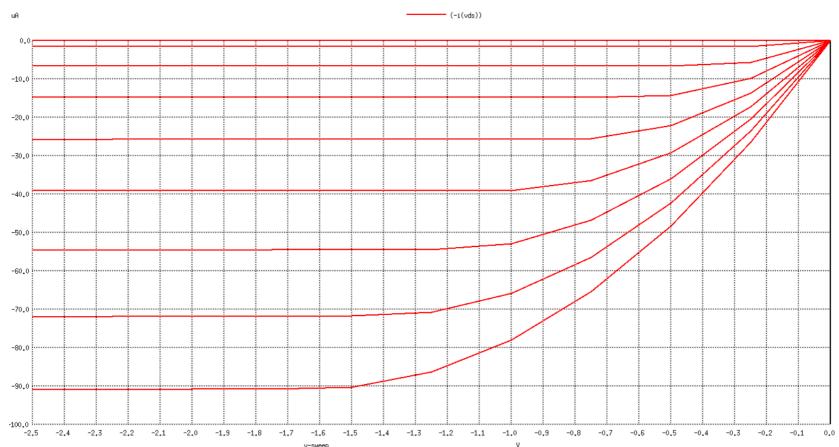
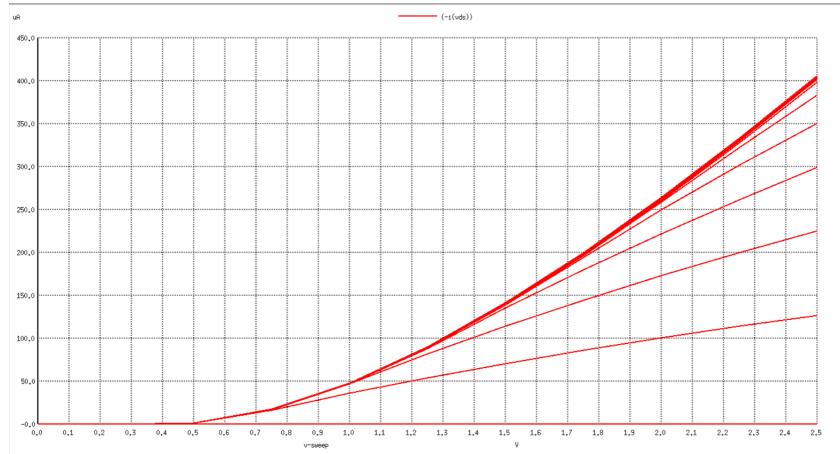
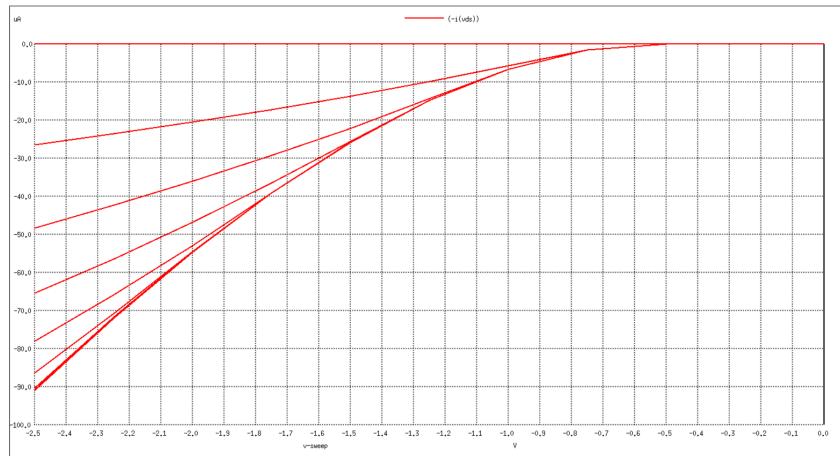


Figure 2: pMOS I_{ds}/V_{ds}

Figure 3: nMOS I_{ds}/V_{gs} Figure 4: pMOS I_{ds}/V_{gs}

Regions of Operation:

- **Linear Region:** $V_{ds} < V_{gs} - V_t$. The channel extends to the drain, and I_{ds} is proportional to V_{ds} , with conductivity dependent on channel depth.
- **Cutoff Region:** $V_{gs} < V_t$. No conductive channel exists, and $I_{ds} = 0 \text{ A}$.
- **Saturation Region:** $V_{ds} \geq V_{gs} - V_t$. The channel pinches off, and I_{ds} reaches a maximum (saturated) value dependent on $V_{gs} - V_t$, remaining nearly constant with V_{ds} . I_{ds} exhibits a quadratic relationship with V_{gs} .

Observations:

- As V_{dd} increases, the saturation region shrinks, and the linear region expands for both NMOS and PMOS due to $V_{ds} \geq V_{gs} - V_{tn}$ (NMOS) and $|V_{ds}| \geq |V_{gs}| - |V_{tp}|$ (PMOS).
- Vertical spacing between V_{gs} curves increases quadratically, not linearly.

Calculations of $V_{ds} = V_{gs} - V_t$:

V_{gs}	$V_{ds} = V_{gs} - V_t$
0 V	OFF ($V_{gs} < V_t$)
0.25 V	OFF ($V_{gs} < V_t$)
0.5 V	0.08 V
0.75 V	0.33 V
1 V	0.58 V
1.25 V	0.83 V
1.5 V	1.08 V
1.75 V	1.33 V
2 V	1.58 V
2.25 V	1.83 V
2.5 V	2.08 V

- NMOS ($V_{tn} = 0.42$ V):

V_{gs}	$V_{ds} = V_{gs} - V_t$
-2.5 V	-1.95 V
-2.25 V	-1.7 V
-2 V	-1.45 V
-1.75 V	-1.2 V
-1.5 V	-0.95 V
-1.25 V	-0.7 V
-1 V	-0.45 V
-0.75 V	-0.2 V
-0.5 V	OFF ($V_{gs} > V_t$)
-0.25 V	OFF ($V_{gs} > V_t$)
0 V	OFF ($V_{gs} > V_t$)

- PMOS ($V_{tp} = -0.55$ V):

Vertical Distances (V_{gs}):

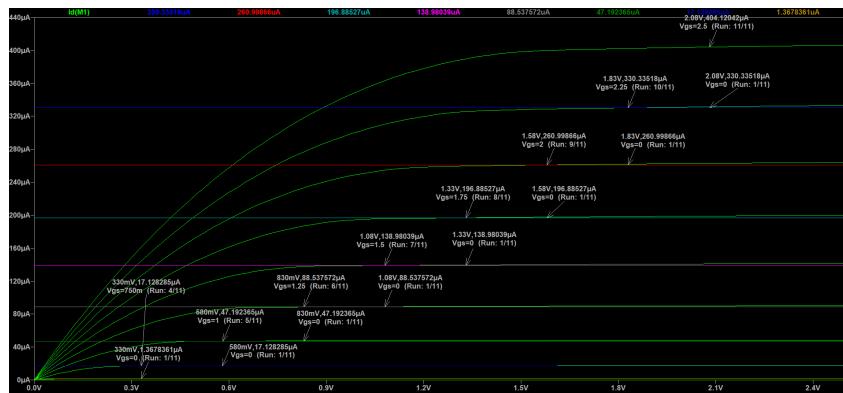
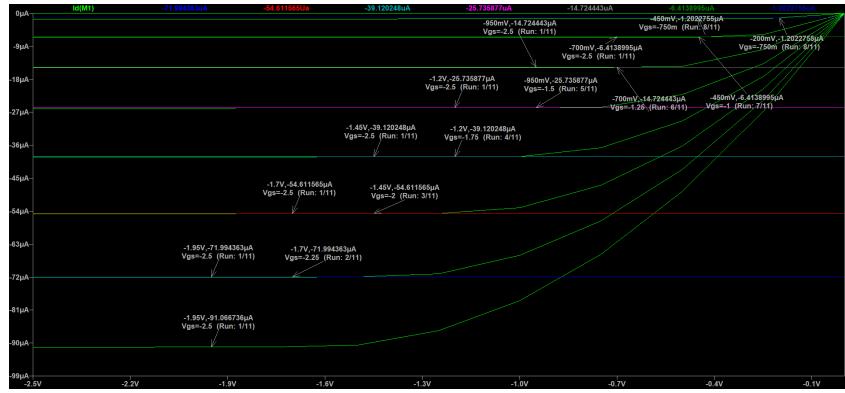


Figure 5: nMOS vertical distances V_{gs}

Figure 6: pMOS vertical distances V_{gs}

$V_{ds1} - V_{ds2}$	$I (\mu\text{A})$
2.08 V - 1.83 V	73.78524
1.83 V - 1.58 V	69.33652
1.58 V - 1.33 V	64.11339
1.33 V - 1.08 V	57.90488
1.08 V - 0.83 V	50.442818
0.83 V - 0.58 V	41.345207
0.58 V - 0.33 V	30.06408
0.33 V - 0.08 V	15.7604489

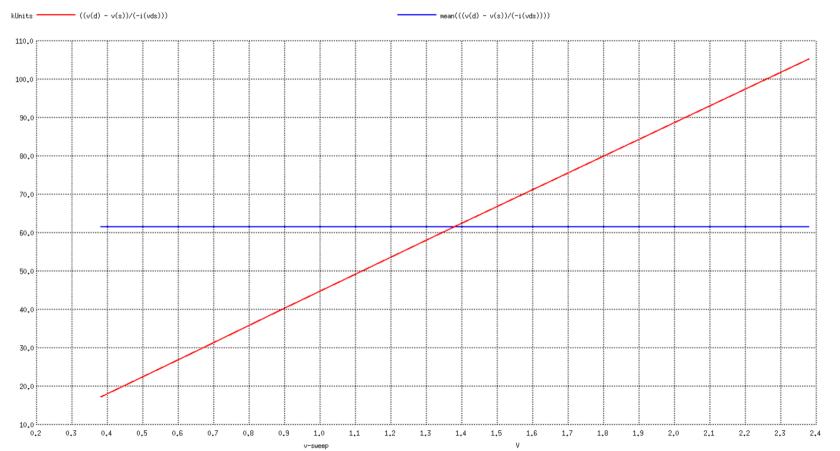
- NMOS:

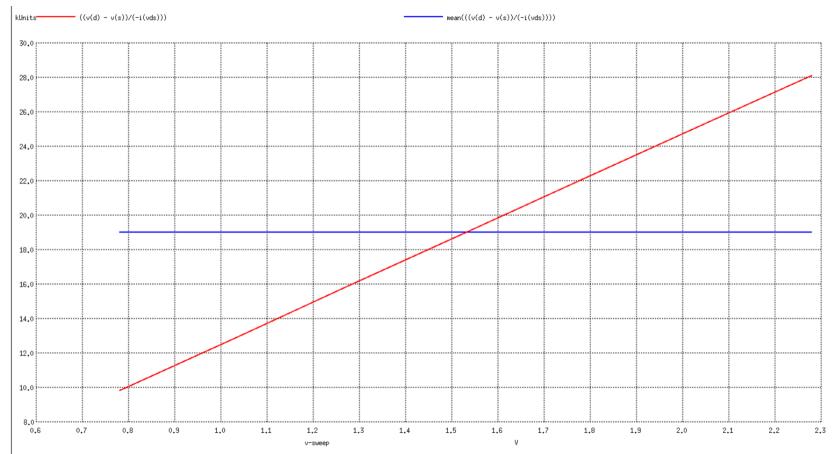
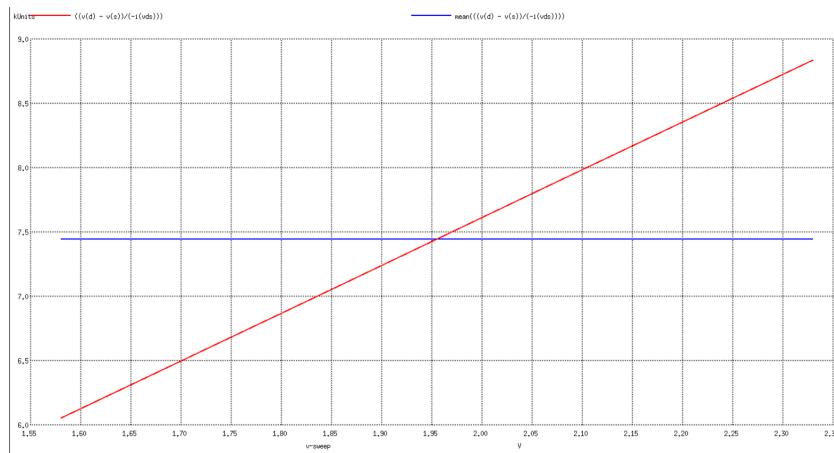
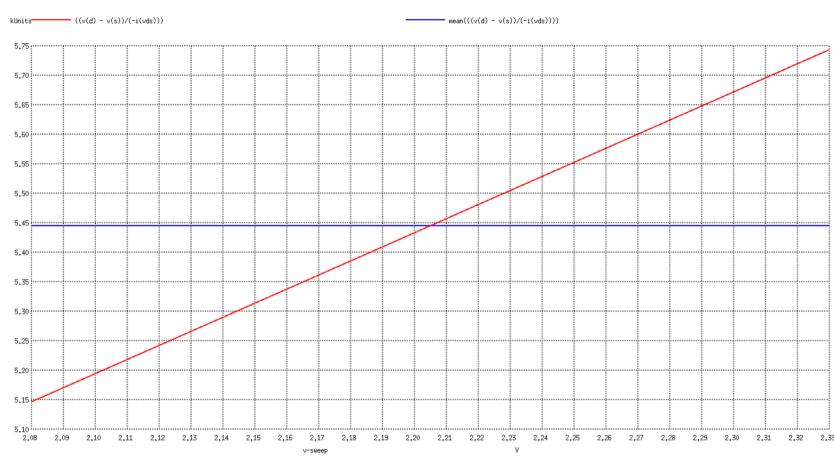
$V_{ds1} - V_{ds2}$	$I (\mu\text{A})$
-1.95 V, -1.7 V	-19.072373
-1.7 V, -1.45 V	-17.382798
-1.45 V, -1.2 V	-15.491317
-1.2 V, -0.95 V	-13.384371
-0.95 V, -0.7 V	-11.011434
-0.7 V, -0.45 V	-8.3105435
-0.45 V, -0.2 V	-5.211624

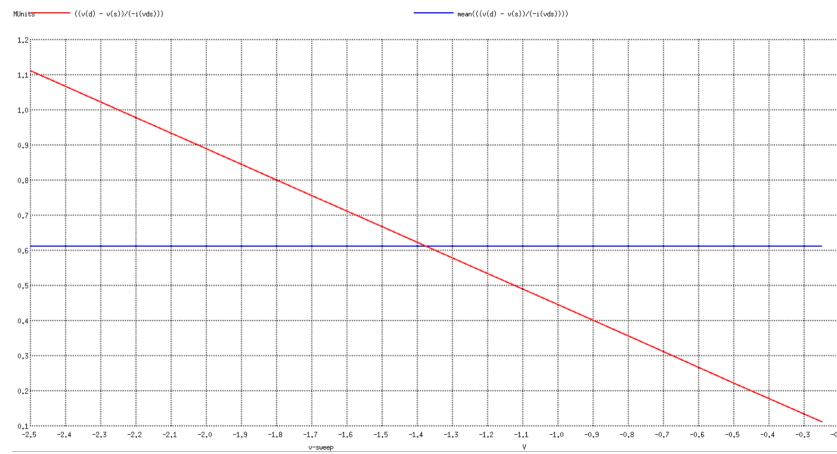
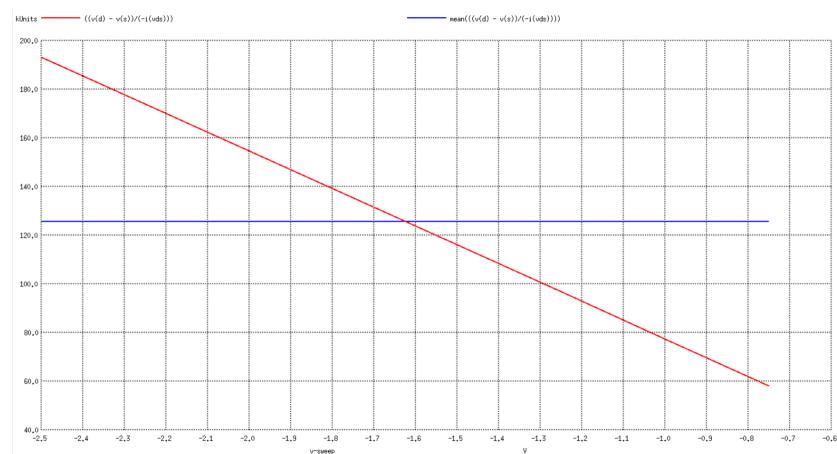
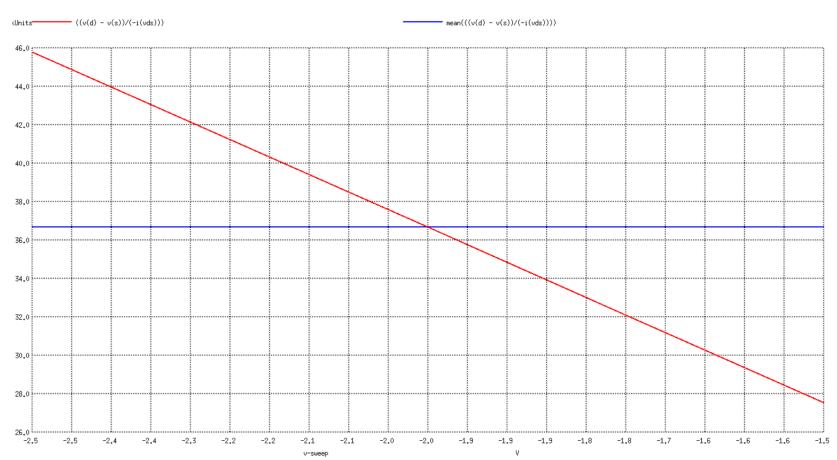
- PMOS:

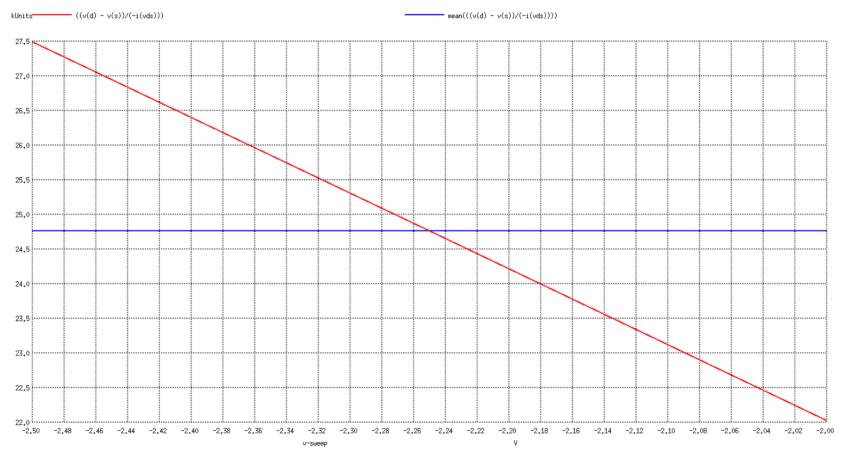
The vertical distances decrease as the curves converge to zero, with PMOS showing a slower reduction rate than NMOS.

Instantaneous and Average Resistance (R_{eq}): Instantaneous $R_{eq} = V/I$ is plotted in SPICE in the saturation region, and the average R_{eq} is computed:

Figure 7: nMOS with $V_{gs} = 0.8V$

Figure 8: nMOS with $V_{gs} = 1.2V$ Figure 9: nMOS with $V_{gs} = 2V$ Figure 10: nMOS with $V_{gs} = 2.5V$

Figure 11: pMOS with $V_{gs} = 0.8V$ Figure 12: pMOS with $V_{gs} = 1.2V$ Figure 13: pMOS with $V_{gs} = 2V$

Figure 14: pMOS with $V_{gs} = 2.5V$

Voltage	R_{eq} (average)
0.8 V	61.5 kΩ
1.2 V	19 kΩ
2 V	7.44 kΩ
2.5 V	5.445 kΩ

• NMOS:

Voltage	R_{eq} (average)
-0.8 V	612 kΩ
-1.2 V	125.6 kΩ
-2 V	36.65 kΩ
-2.5 V	24.75 kΩ

• PMOS:

As V_{gs} increases, R_{eq} decreases due to a shrinking saturation region. PMOS exhibits steeper slopes than NMOS due to a larger saturation region.

1.2 (b) RC Equivalent Resistance

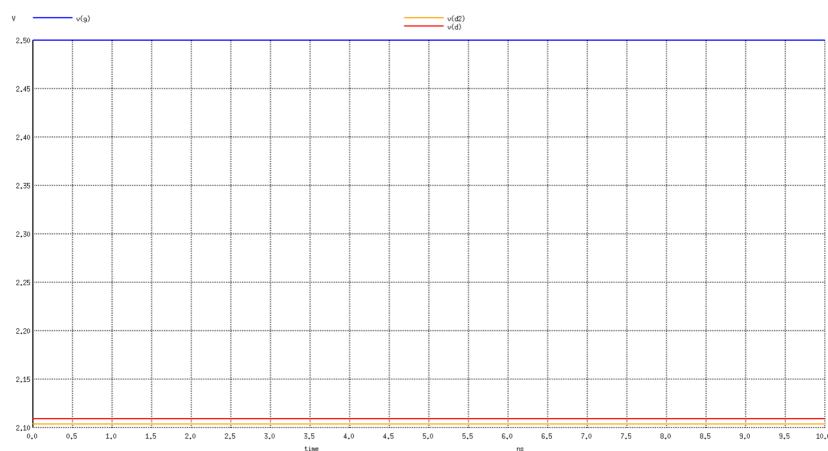
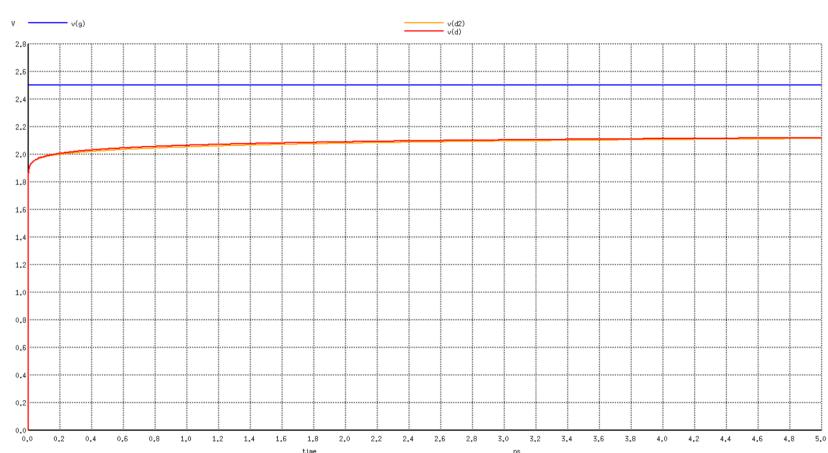
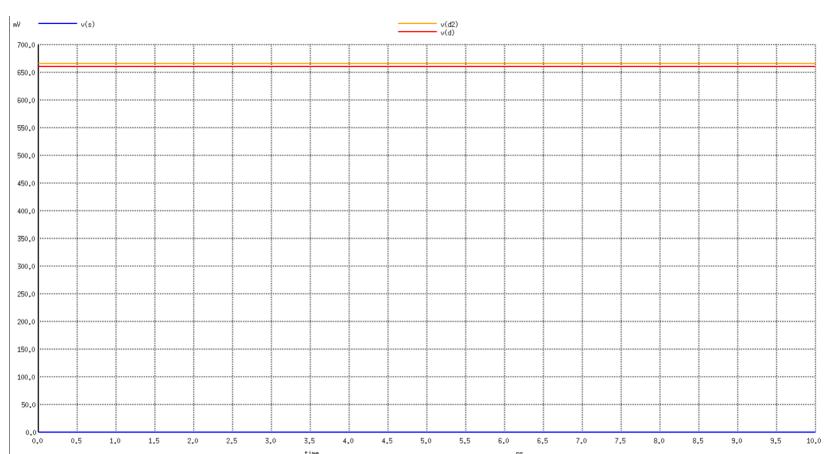
The equivalent resistance (R_{eq}) is calculated in SPICE using the delay time t_p :

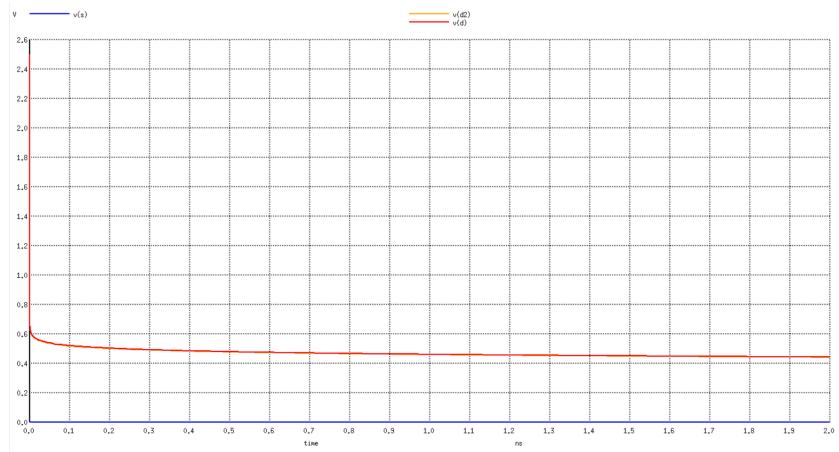
- NMOS: $t_p = 3.2 \times 10^{-10}$ s, $t_{pHL} = \ln(2)R_{eq}C_L$, $R_{eq} = 4.717$ kΩ.
- PMOS: $t_p = 1.42 \times 10^{-9}$ s, $t_{pHL} = \ln(2)R_{eq}C_L$, $R_{eq} = 20.486$ kΩ.

Compared to (a), R_{eq} decreases due to parasitic capacitance, with PMOS showing a larger reduction due to its higher resistance and shorter discharge time.

2 Exercise 2: Threshold Voltage in Series

Two NMOS (or PMOS) transistors are connected in series in SPICE. Outputs are at the drain of the first (V_d) and second (V_{d2}) transistors.

Figure 15: nMOS V_d Figure 16: nMOS V_{d2} Figure 17: pMOS V_d

Figure 18: pMOS V_{d2} **NMOS:**

- $V_d = 2.1089 \text{ V}$, $V_{d2} = 2.1037 \text{ V}$.
- First transistor: $V_{tn} = V_{dd} - V_{out} = 2.5 - 2.1089 = 0.3911 \text{ V}$ (close to $V_{tn} = 0.42 \text{ V}$).
- Second transistor: $V_{tn} = 0.3963 \text{ V}$.

PMOS:

- $V_d = 0.66089 \text{ V}$, $V_{d2} = 0.66612 \text{ V}$.
- First transistor: $V_{tp} = V_{out} = 0.66089 \text{ V}$ (close to $|V_{tp}| = 0.55 \text{ V}$).
- Second transistor: $V_{tp} = 0.66612 \text{ V}$.

Observations:

- NMOS transmits a weak logic 1, PMOS a weak logic 0, due to connections to V_{dd} and ground, respectively.
- PMOS cannot fully discharge V_{dd} , and NMOS cannot exceed $V_{dd} - V_{tn}$.

3 Exercise 3

3.1 (a) Inverter Transfer Curve

A CMOS inverter is simulated in SPICE, and the transfer curve is plotted. V_M (where $V_{in} = V_{out}$) is found to be 0.885821 V.

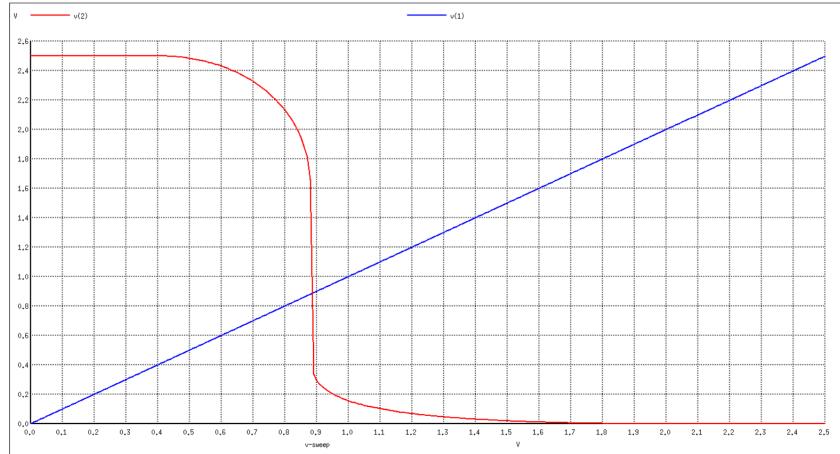
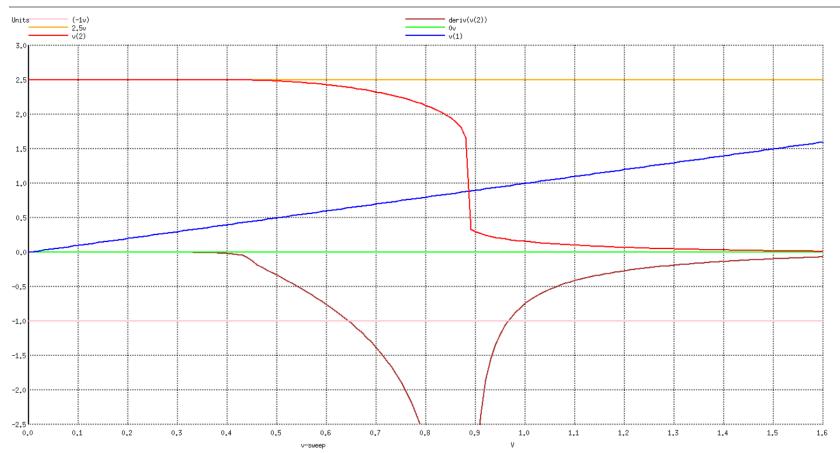


Figure 19: CMOS Inverter

V_{IL} and V_{IH} : Calculated where the derivative of the output is -1:

Figure 20: CMOS Inverter with V_{IL} & V_{IH}

- $V_{IL} = 0.643929 \text{ V}$
- $V_{IH} = 0.965465 \text{ V}$

V_{OH} and V_{OL} : Assumed as $V_{dd} = 2.5 \text{ V}$ and 0 V .

Noise Margins:

- $NM_H = V_{OH} - V_{IH} = 1.534535 \text{ V}$
- $NM_L = V_{IL} - V_{OL} = 0.643929 \text{ V}$

Symmetry Adjustment: The ratio $k_n/k_p = 4.81512193$. For symmetry ($k_n/k_p = 1$), W_n is divided by 4.81512193, yielding $V_M = 1.20706 \text{ V}$, $V_{IL} = 1.05168 \text{ V}$, $V_{IH} = 1.3748 \text{ V}$, $NM_H = 1.1252 \text{ V}$, $NM_L = 1.05168 \text{ V}$. For $V_M = V_{dd}/2 = 1.25 \text{ V}$, $k_n/k_p = 1.3$, $W_p/W_n = 5.79150579$, with $NM_H = 1.07279 \text{ V}$, $NM_L = 1.10564 \text{ V}$.

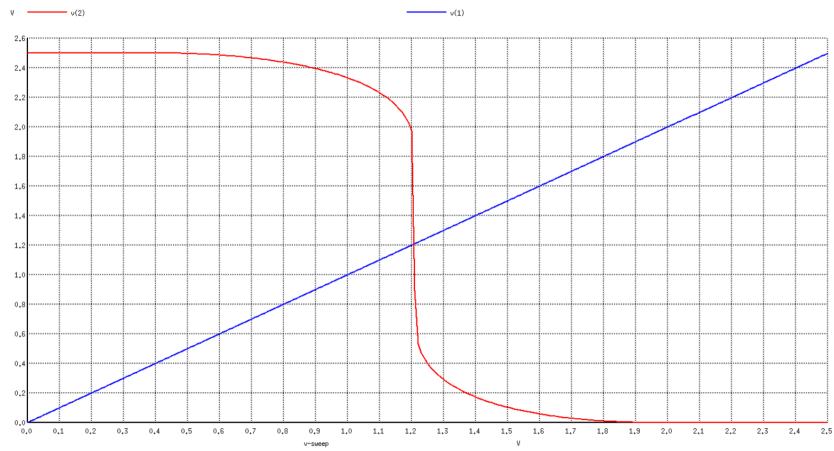


Figure 21: CMOS Symmetrical Inverter

3.2 (b) Voltage Scaling

Transfer curves are generated for $V_{dd} = \{2.5, 1.8, 1.2, 0.7\}$ V:

3.2.1 V=2.5V

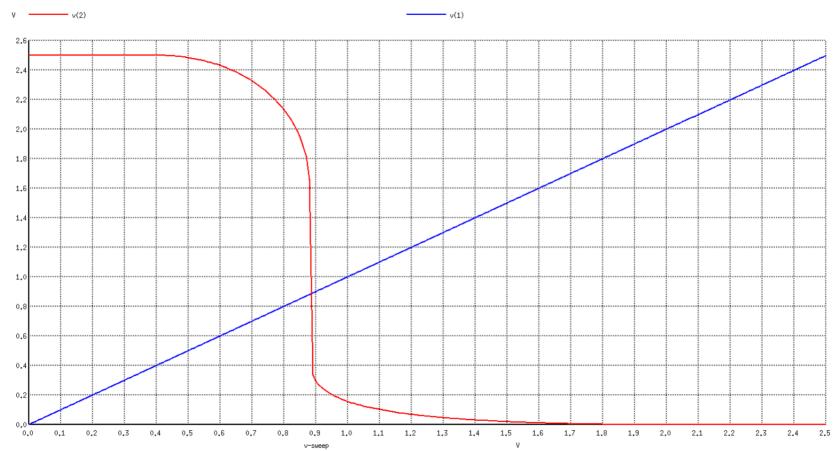


Figure 22: CMOS Inverter Output

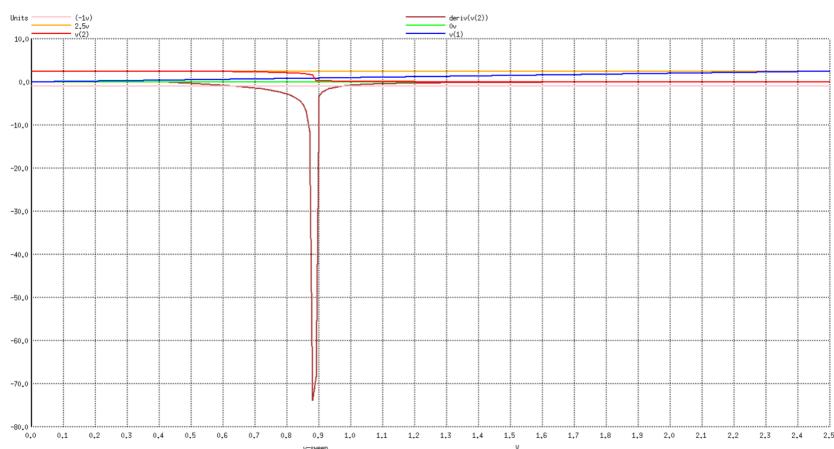


Figure 23: CMOS derivative Inverter Output

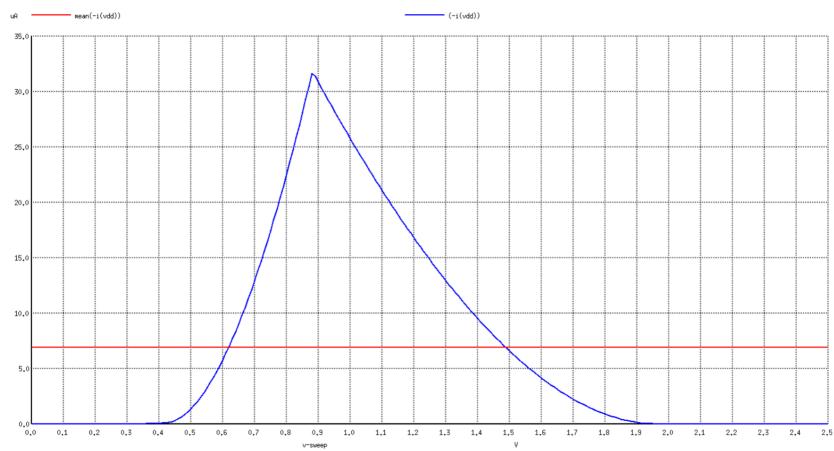


Figure 24: CMOS Inverter current

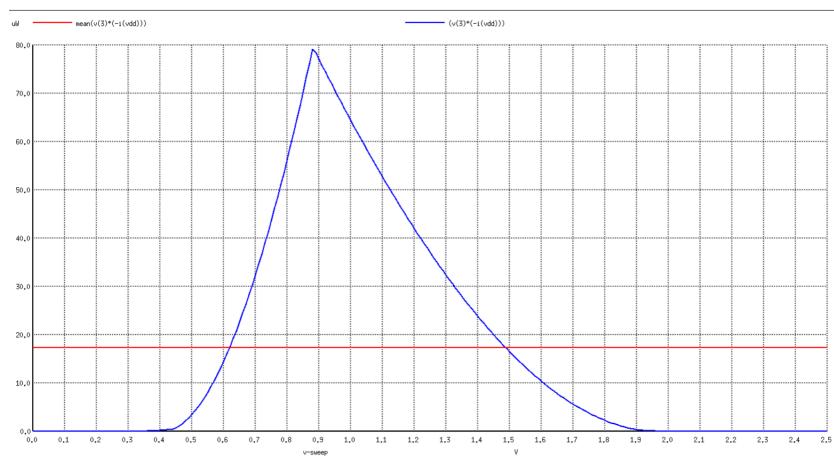


Figure 25: CMOS Inverter power

3.2.2 $V=1.8\text{V}$

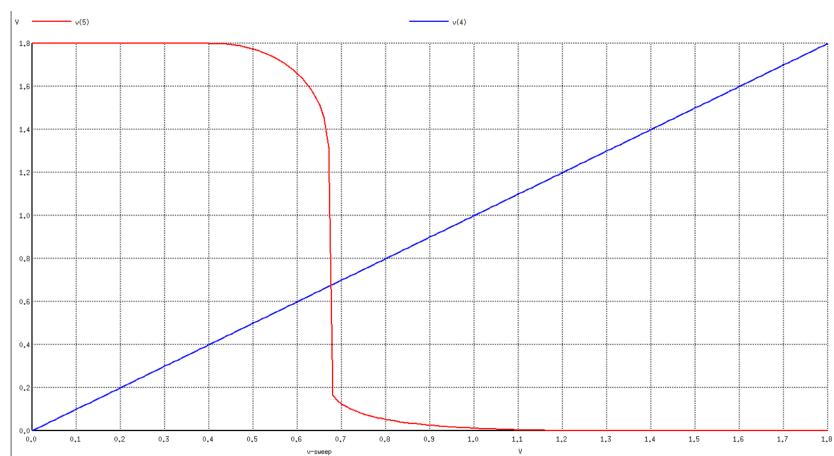


Figure 26: CMOS Inverter Output

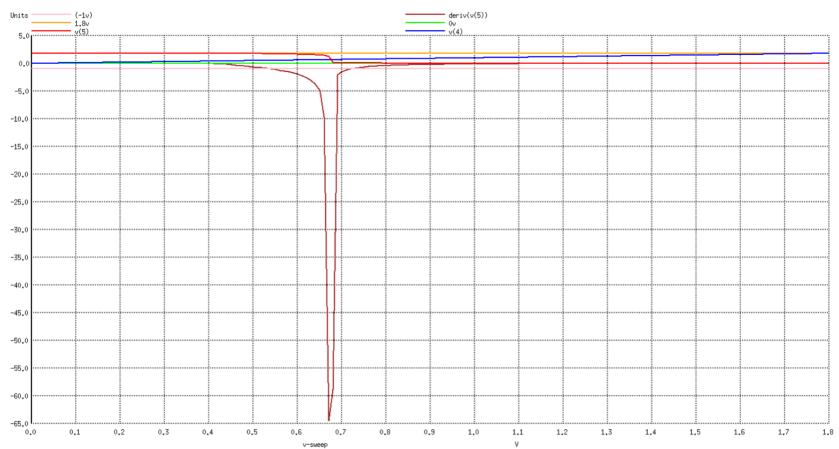


Figure 27: CMOS derivative Inverter Output

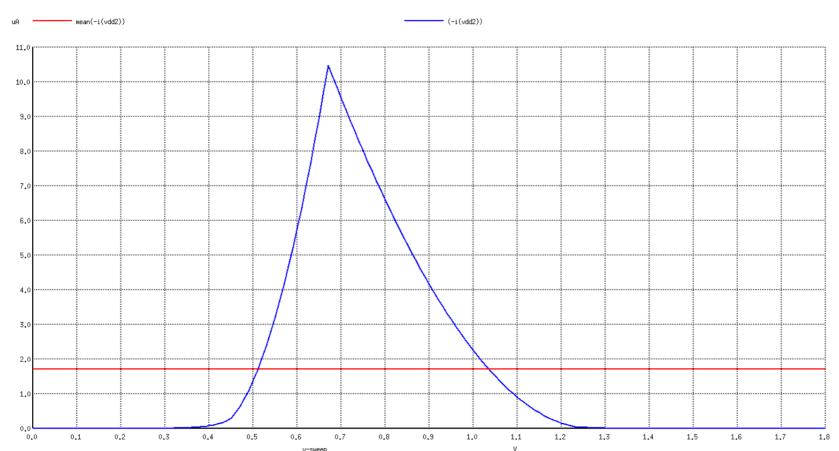


Figure 28: CMOS Inverter current

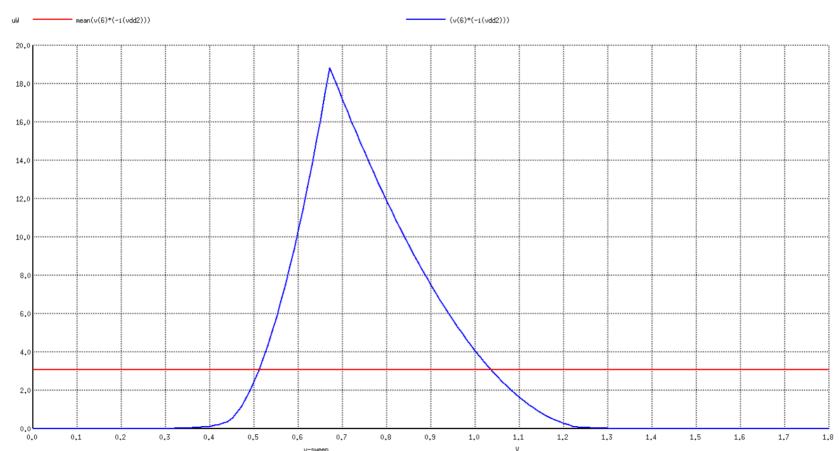


Figure 29: CMOS Inverter power

3.2.3 V=1.2V

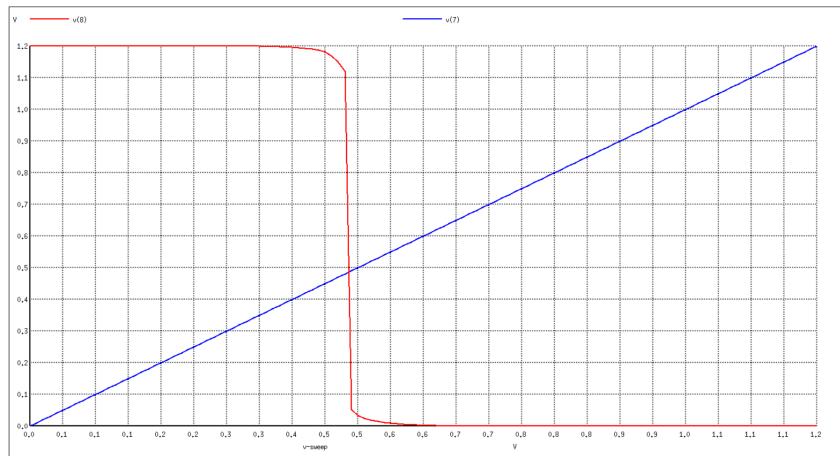


Figure 30: CMOS Inverter Output

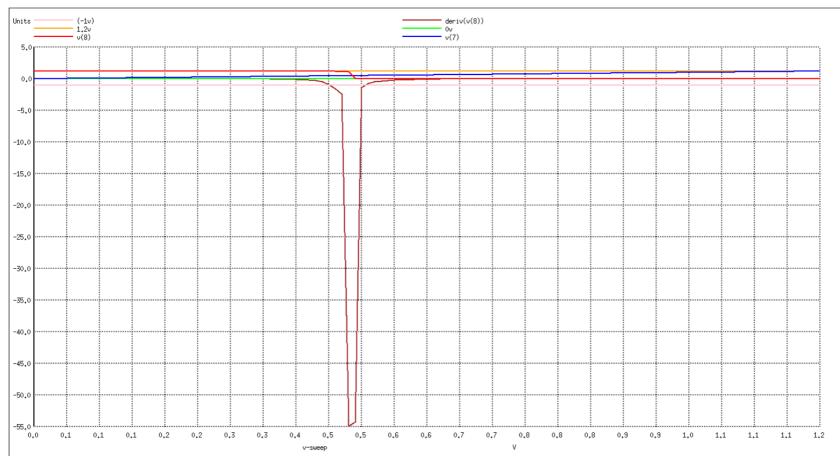


Figure 31: CMOS derivative Inverter Output

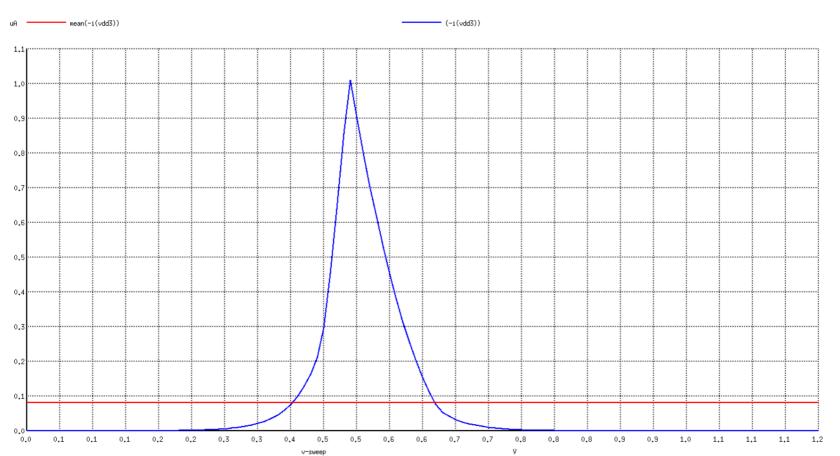


Figure 32: CMOS Inverter current

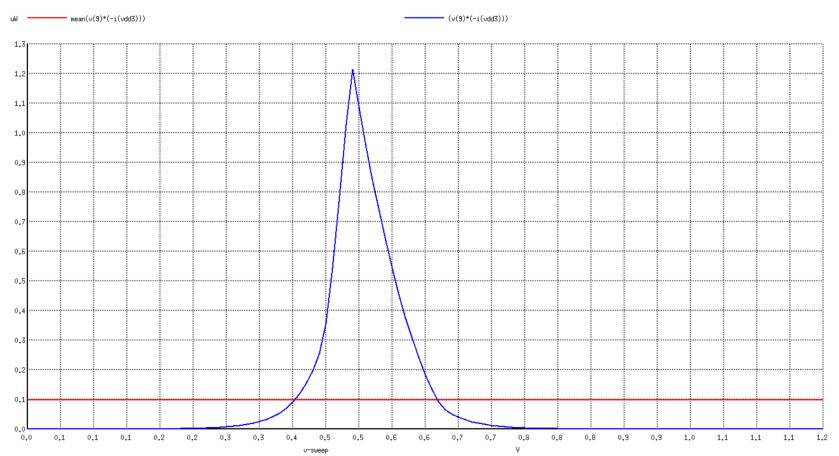


Figure 33: CMOS Inverter power

3.2.4 V=0.7V

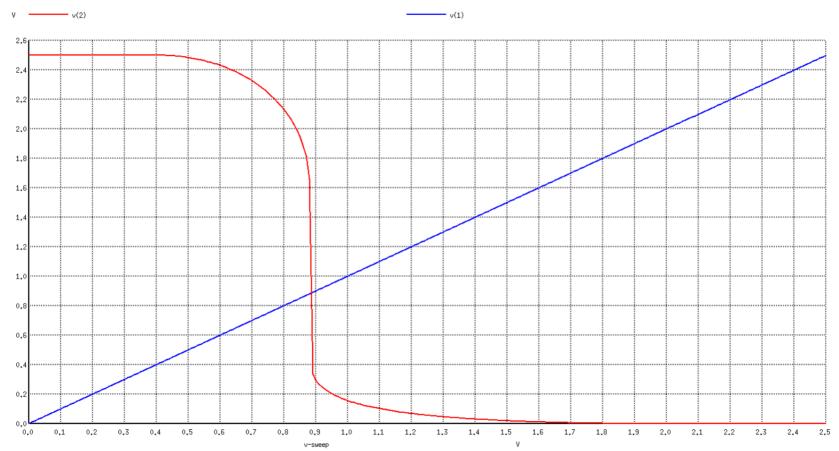


Figure 34: CMOS Inverter Output

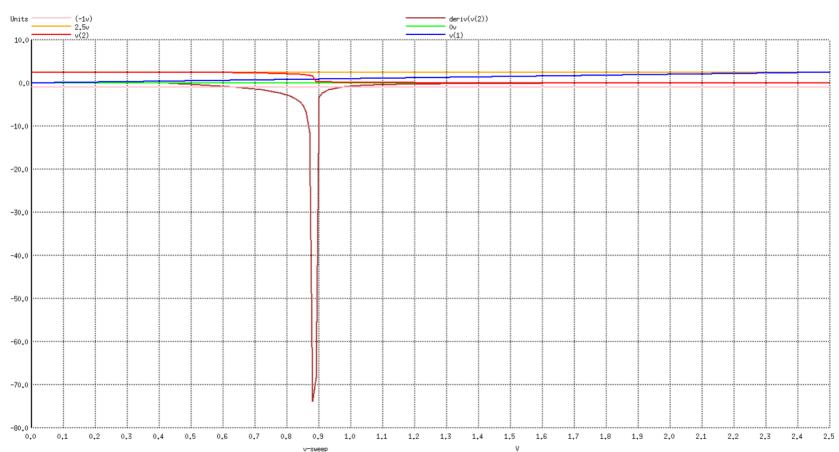


Figure 35: CMOS derivative Inverter Output

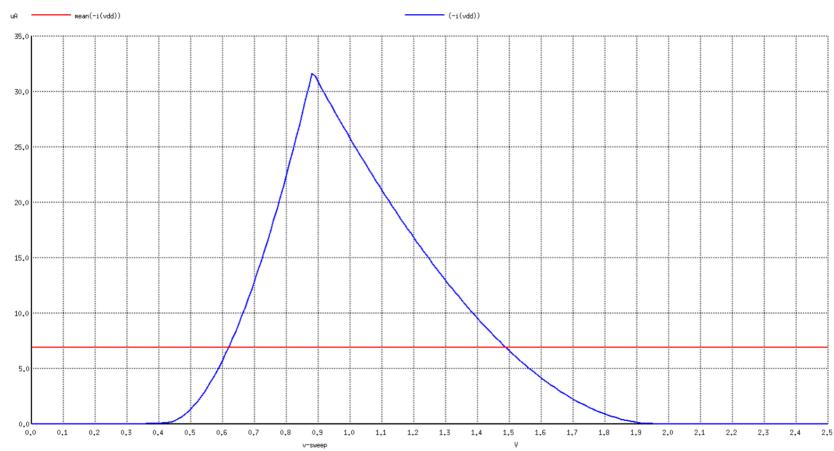


Figure 36: CMOS Inverter current

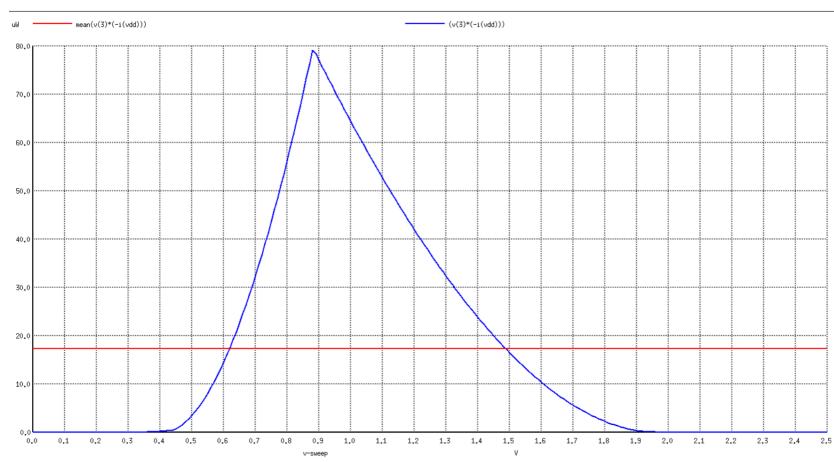


Figure 37: CMOS Inverter power

- $V_{dd} = 2.5 \text{ V}$: $V_{IL} = 0.643929 \text{ V}$, $V_{IH} = 0.965465 \text{ V}$, $NM_L = 0.643929 \text{ V}$, $NM_H = 1.534535 \text{ V}$
- $V_{dd} = 1.8 \text{ V}$: $V_{IL} = 0.541114 \text{ V}$, $V_{IH} = 0.718488 \text{ V}$, $NM_L = 0.541114 \text{ V}$, $NM_H = 1.081512 \text{ V}$
- $V_{dd} = 1.2 \text{ V}$: $V_{IL} = 0.450897 \text{ V}$, $V_{IH} = 0.505828 \text{ V}$, $NM_L = 0.450897 \text{ V}$, $NM_H = 0.694172 \text{ V}$
- $V_{dd} = 0.7 \text{ V}$: $V_{IL} = 0.250071 \text{ V}$, $V_{IH} = 0.279893 \text{ V}$, $NM_L = 0.250071 \text{ V}$, $NM_H = 0.420107 \text{ V}$

	V_{dd}	I_{av}	$P_{av} = V \cdot I$
Power and Current:	2.5 V	6.9 μA	17.2 μW
	1.8 V	1.71 μA	3.07 μW
	1.2 V	81.6 pA	98 nW
	0.7 V	260 pA	182 pW

Observations:

- Lower V_{dd} sharpens the transition region, improving gain and noise margins by reducing the undefined input range.
- Power and current decrease with V_{dd} , maintaining inverter functionality.

Conclusion

This assignment provided a comprehensive analysis of CMOS transistor and inverter characteristics. The DC analysis elucidated operational regions and resistance variations, while series configurations validated threshold voltages. The inverter study highlighted the impact of sizing on symmetry and the benefits of voltage scaling on noise margins and power efficiency, reinforcing key VLSI design principles.