Electrical and Computer Engineering
University of Thessaly (UTH)

ECE327 - VLSI

Fall Semester — Educational year 2022-2023

Lab04

4th Assignment: CMOS Latch and Flip-Flop Design

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Contents

Introduction

This assignment involves the design and simulation of sequential CMOS circuits, specifically a negative D latch and a negative edge-triggered master-slave D flip-flop. Using SPICE, the functionality is verified through truth tables and waveforms, and key timing parameters are measured. The objective is to understand the operation of these fundamental memory elements in VLSI systems and analyze their performance characteristics.

1 Exercise 1: Negative D Latch

The circuit is a negative D latch composed of a pass transistor and NOT gates. The pass transistor acts as a switch: when the clock (`Clk`) is 1, the gate is off, retaining the previous state; when `Clk` is 0, the input D is transferred to the output Q.

Truth Table:

Clock	D	Q_{n+1}
1	X	Q_n
0	0	0
0	1	1

NGSPICE waveforms confirm the truth table, showing correct state retention and input transfer.

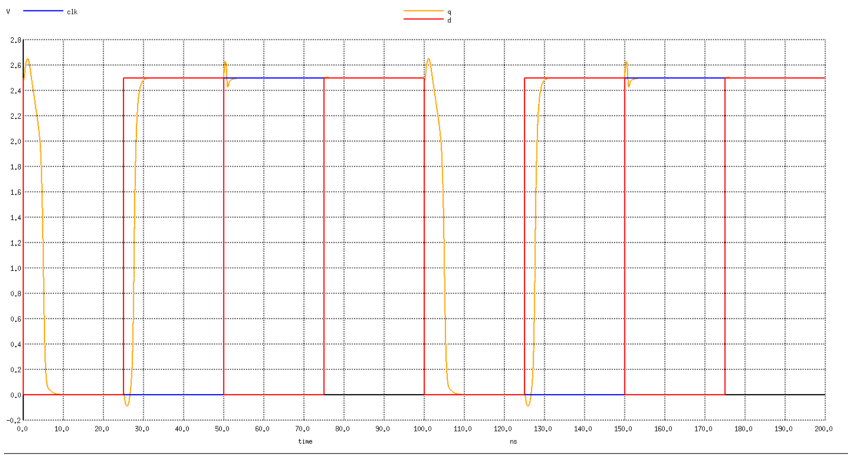

Figure 1: Spice waveforms

2 Exercise 2: Negative Edge-Triggered Master-Slave D Flip-Flop

2.1 (a) Schematic and Functionality

The circuit is a negative edge-triggered master-slave D flip-flop implemented with multiplexers using pass transistors.

Clk = 0:

- **Master**: T1 transistor is off, T2 conducts, transferring the inverted D to Q_m.
- **Slave**: T3 conducts, T4 is off, passing Q_m through an inverter to Q.

Clk = 1:

- **Master**: T1 conducts, T2 is off, transferring inverted D to Q_m.
- **Slave**: T3 is off, T4 conducts, retaining the previous Q via coupled inverters; Q_m is isolated.

Truth Table:

Clk	D	Q_{n+1}
1	X	Q_n
0	0	0
0	1	1

NGSPICE waveforms verify the truth table, showing correct state transitions on the negative clock edge.

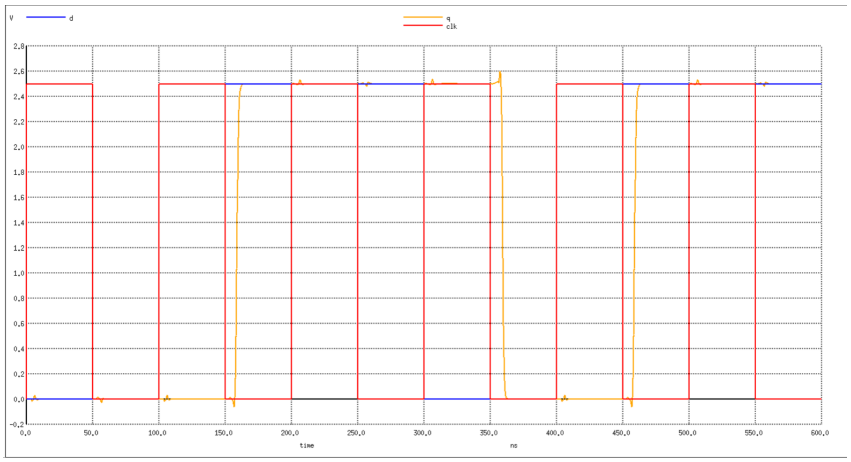

Figure 2: Spice waveforms

2.2 (b) Timing Measurements

The following figure represents the flip-flop schematic:

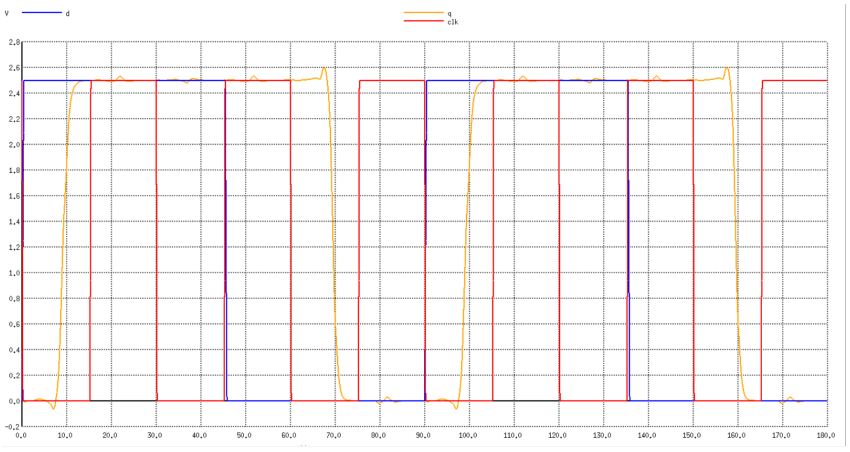

Figure 3: Spice waveforms

```
 Measurements for Transient Analysis

t_phl              =  5.422184e-08 targ=  6.952184e-08 trig=  1.530000e-08
t_plh              =  9.069881e-09 targ=  9.169881e-09 trig=  1.000000e-10
t_rise_qm          =  3.757343e-09 targ=  6.513244e-09 trig=  2.755901e-09
t_fall_qm          =  3.026329e-09 targ=  5.653681e-08 trig=  5.351049e-08
t_rise_q           =  2.390766e-09 targ=  1.063370e-08 trig=  8.242930e-09
t_fall_q           =  1.923559e-09 targ=  7.065606e-08 trig=  6.873250e-08
t_setup            =  2.990000e-08 targ=  3.010000e-08 trig=  2.000000e-10
t_hold             =  1.550000e-08 targ=  4.560000e-08 trig=  3.010000e-08
```

Figure 4: Measurements

Measurements:

Parameter	Time
Clk $\rightarrow Q$	31.5 ns
t_{rise} (Qm)	3.75 ns
t_{fall} (Qm)	3.02 ns
t_{rise} (Q)	2.39 ns
t_{fall} (Q)	1.92 ns
t_{setup}	29.9 ns
t_{hold}	15.5 ns

Total Propagation Delay:

$$t_f = \frac{t_{phl} + t_{plh}}{2} = 31.5\,\text{ns}$$

Measurement Definitions:

- t_{phl}: From 50% V_{dd} of `Clk` (rising) to 50% V_{dd} of Q (falling).
- t_{plh}: From 50% V_{dd} of `Clk` (falling) to 50% V_{dd} of Q (rising).
- t_{rise}: From 10% to 90% of the rising pulse.
- t_{fall}: From 90% to 10% of the falling pulse.
- t_{setup}: From 50% of the first rising edge of D to 50% of the second falling edge of `Clk`.
- t_{hold}: From 50% of the second falling edge of `Clk` to 50% of the first falling edge of D.

Conclusion

This assignment successfully demonstrated the design and simulation of a negative D latch and a master-slave D flip-flop. The truth tables and waveforms validated their functionality, while timing measurements provided insights into propagation delays, rise/fall times, and setup/hold constraints. These results highlight the critical timing considerations in sequential CMOS circuits, essential for reliable VLSI design.