COMP 1047 Lab Week 07

Pipelined CPU

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(1) A pipelined MIPS CPU is running the following program:

```
sub $s0, $t0, $t2
add $s1, $t2, $t3
beq $s3, $t4, 7
lw  $s2, 4($s5)
slt $s4, $s2, $s3
```

Which registers are being written, and which registers are being read in the fifth cycle? Assume the 1st instruction starts at cycle 1. No data or control hazard is considered. Also assume that each instruction is extended into 5 stages to avoid structural hazard.

(2) A pipelined MIPS CPU is running the following program:

```
add $t0, $s0, $s1
sub $t0, $t0, $s2
lw  $t1, 60($t0)
and $t2, $t1, $t0
```

Show all the data hazard possible in this piece of code.

(3) A pipelined MIPS CPU is running the following program:

```
add $t0, $s0, $s1
sub $t0, $t0, $s2
lw  $t1, 60($t0)
and $t2, $t1, $t0
```

Show the forwarding and stalls needed to execute the program in a pipelined processor.

(4) Calculate the total execution cycles of the following assembly code

```
addi $s0, $0, 0
addi $t0, $0, 2
for:
beq $s0, $t0, done
addi $s0, $s0, 1
j for
done:
```

(a) Using single-cycle MIPS CPU.

(b) Using 5-stage pipelined MIPS CPU. Assume no hazards considered.

(5) For the benchmark applications in SPECINT2000, the statistics of the compiled instructions are as follows:

- 25% memory loads
- 10% memory stores
- 11% branches
- 2% jumps
- 52% R-types

Suppose that (1) 40% of the loaded register values are used by the next instruction; and (2) 25% of the branches are not taken (not branched). Question: What is the average CPI of this set of instructions?