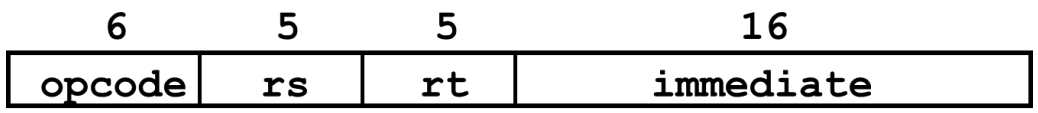

- New branched address = PC + 4 + immediate<<2

Label1 ->	0x0000 010C	Inst. H
	0x0000 0108	Inst. G
	0x0000 0104	Inst. F
	0x0000 0100	Inst. E = beq $t1, $t2, label1
	0x0000 00FC	Inst. D
	0x0000 00F8	Inst. C
	0x0000 00F4	Inst. B
	0x0000 00F0	Inst. A

What machine code will be instruction E translated to?
Note: the PC value when executing E is 0x0000 0100

Note2: the 'PC value' here is defined as the address of currently executing instruction.
In the lectures on CPU design, you will get a better understanding why we always use PC + 4.
For now, just take it (PC + 4 + immediate<<2) as is. (Verify it from the MIPS_ref_card)

Note3: the branch series instructions jump based on the current PC value. The word range of jump is determined by the 'immd' field, which is a 2's C number in $[-2^{15}, 2^{15}-1]$

Note 4: to work out the immediate value for beq $t1, $t2, label1, firstly note the distance between The 'beq' instruction and the branch target: 0x010C-0x0100 = 0xC = 12. So, 4 + immd << 2 = 12. Then we have 'immd' = 2. Thus, the machine code for beq $t1, $t2, label1 is 0x1149 0002