University of Nottingham Ningbo China

School of Computer Science

A Level 1 Module, Spring Semester 2020–2021

Systems and Architecture (AE1SYS)

Time Allowed: TWO Hours

Candidates may complete the front cover of their answer book and sign their desk card but must NOT write anything else until the start of the examination period is announced

Answer ALL questions

Total Marks: 100

No calculators are permitted in this examination

Dictionaries are not allowed with one exception. Those whose first language is not English may use a standard translation dictionary to translate between that language and English provided that neither language is the subject of this examination. Subject-specific translation dictionaries are not permitted.

No electronic devices capable of storing and retrieving text, including electronic dictionaries, may be used.

DO NOT turn examination paper over until instructed to do so.

APPENDIX: MIPS Reference Card

INFORMATION FOR INVIGILATORS:
Collect both the exam papers and the answer booklets at the end of the exam.

Question 1: MIPS Fundamentals (30 marks)

Questions (1)-(5) are Multiple Choice Questions. Identify all correct answers.

(1) What are the typical features of the von Neumann architecture? (3)

(a) Programs cannot be modified while the processor is running.
(b) Data and programs share the same address space.
(c) Programs have to be written in assembly language.
(d) Each machine instruction contains the address of the next instruction.
(e) The processor has a special register called the program counter (PC).

(2) Which of the following instruction(s) is/are not a MIPS32 I-type instruction(s)? (3)

(a) `sll $t1, $t0, 3`
(b) `slti $t1, $t0, 3`
(c) `j label`
(d) `bne $t1, $t0, label`
(e) `addi $t1, $t0, 3`

(3) In the pipelined MIPS32 processor, which stage is the value of the next PC determined for *lw* and *sw* instructions? (3)

(a) IF
(b) ID
(c) EX
(d) MEM
(e) WB

(4) Consider the following program fragment in MIPS32 assembly code:

```
li $s0, -1
srl $v0, $s0, 1
addiu $a0, $v0, 1
```

Which of the following statement(s) is/are correct? (3)

(a) Register $a0 will contain the largest positive representable signed number after executing the code fragment.

(b) Register $a0 will contain the least negative representable signed number after executing the code fragment.

(c) The code fragment will occupy 128 bits in memory.

(d) The code fragment will raise an overflow exception.

(e) Register $v0 will contain -1 after executing the code fragment.

(5) Which of the following statement(s) about 8-bit two's complement is/are correct? (3)

(a) The representable range is -128 to +127.

(b) The representable range is -127 to +128.

(c) To calculate x from -x, we flip all the bits and subtract 1.

(d) To calculate -x from x, we flip all the bits and add 1.

(e) The most significant bit has a weight of -2^6.

Questions (6)-(8) are Short Answer Questions. Provide solutions with necessary brief explanations.

(6) For $a = 115_{10}$, $b = 80_{10}$, $c = -73_{10}$, calculate using signed 8-bit two's complement format the following results:

(i) $a + b$

(ii) $b + c$

(iii) $a - c$

In which case(s) does/do the overflow occur? (7)

(7) Describe the calling conventions of a procedure for MIPS32:

(i) How are arguments passed?

(ii) How are results returned?

(iii) Which of the user registers have to be saved by the caller? (ignore $at, $k0 and $k1, and assume the caller needs them preserved.)

(iv) Which registers are always saved by the callee?

(v) Where are local variables stored? (6)

(8) Does pipelining reduce the execution time for individual instructions? Why? (2)

Question 2: MIPS Programming (20 marks)

(a) Convert the following high-level code into MIPS assembly. Use $t0 and $t1 to store variables 'pow' and 'x', respectively. The instructions that you can choose are: `add, sub, sll, sra, addi, lw, sw, j, beq, bne, slt`. Using instructions not specified in the list leads to no marks rewarded.

```
int pow = 1;
int x = 0;

while ((pow - x) < 128) {
    pow = pow * 6;
    x = x + 1;
}
```

Question 3: CPU design (30 marks)

(a) Refer to the following MIPS assembly code and answer the questions below: (10)

```
      addi $s0, $0, 0
      addi $t0, $0, 4
for:
      beq  $s0, $t0, done
      lw   $s1, 4($s3)
      add  $t3, $s1, $s0
      addi $s0, $s0, 1
      j    for
done:
```

(i) Assume the code is running on a 5-stage MIPS pipelined CPU, calculate the total execution cycles, assuming no data/control hazards. (4)

(ii) Indicate the RAW data hazard available in the above code. Calculate the total execution cycles considering both data and control hazards. Given: (a) Base CPI = 1; (b) Branching costs 1 penalty cycle if taken, no penalty if not taken; (c) Load CPI = 1 if there is no stall, and 2 if there are stalls; (d) Unconditional jump takes 1 penalty cycle. (6)

(b) Design a single-cycled CPU for an instruction set that contains only the following four instructions: lw, sw, add, and nand. Assume that the instruction formats are the same as in the MIPS architecture. Draw the CPU design, by showing all the hardware functional blocks, and all the data links. No control path needs to be shown. Specifically, show a 1-bit ALU design that supports the abovementioned instructions, including the block diagram and the table that indicates all the control signals and their corresponding operations. You must show only the minimal hardware required to implement the CPU and the ALU. (20)

Question 4: Computer Networks (20 marks)

Single Choice Questions. Identify exactly one correct answer. (8)

(1) In the OSI 7 layers model, which layer is the concept of subnet mask defined in?

(a) Presentation Layer.
(b) Network Layer.
(c) Transportation Layer.
(d) Session Layer.

(2) The key purpose of ISO proposing the OSI 7 layers model is

(a) To promote system interconnection.
(b) To increase the transmission rate.
(c) To set the standard for computer architectures.
(d) Economic benefit.

(3) What is the layer, where data are converted into segments?

(a) Application Layer.
(b) Presentation Layer.
(c) Transport Layer.
(d) Physical Layer.

(4) A client transfers a data frame of 1,000 bits to the server located 2 kilometers away measured in the circuit length. The signal propagation speed is 200 m/μs. The data transmission rate is 10Mbps. How long does it take to complete the transmission of this data frame?

(a) 100μs.
(b) 109μs.
(c) 110μs.
(d) None of above.

Multiple Choice Questions. Identify all correct answers. (12)

(5) Which of the following statement(s) is/are correct?

(a) The link layer is responsible for checking network topology and conducting message routing.

(b) During data transmission, if the receiver has less capacity compared to the sender, then congestion control is needed.

(c) Flow control aims at matching the sender and receiver's speed via buffer management.

(d) The RIP protocol is suitably applied to continental-wide networks.

(e) The RIP protocol broadcasts routing information to neighbour routers.

(6) For the IP address 192.168.19.255/20, which of the following statement(s) is/are correct?

(a) This is a broadcasting address.

(b) This is a subnet address.

(c) This is a private address.

(d) This is a public address.

(e) This address belongs to subnet 192.168.31.0.

(f) This address belongs to subnet 192.168.16.0.

(7) A new university is planning to construct its networking infrastructure. It needs about 280 subnets, each of which contains at most 40 host addresses. Assume the university obtains a class B address. Which of the following subnet masks will support an appropriate addressing scheme?

(a) 255.255.255.0.

(b) 255.255.255.128.

(c) 255.255.252.0.

(d) 255.255.255.224.

(e) 255.255.255.192.

(f) 255.255.248.0.

(8) Suppose in the network, a Router B contains the following routing table:

Dest. network	Vector Distance	Next Hop Router
N_1	7	A
N_2	2	C
N_6	8	F
N_8	4	E
N_9	4	F

Now it receives the routing table from Router C, as follows:

N_2	4	?
N_3	8	?
N_6	4	?
N_8	3	?
N_9	5	?

Which item(s) below is/are there in Router B's updated routing table after applying the Router Information Protocol?

(a) N_1 — 7 — C
(b) N_3 — 8 — C
(c) N_2 — 5 — C
(d) N_6 — 5 — F
(e) N_9 — 4 — F
(f) N_8 — 4 — E