Mask Set Errata for Mask 1M35Y

Introduction

This report applies to mask 1M35Y for these products:

- MPC563XM

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e3378: EQADC: Pull devices on differential pins may be enabled for a short period of time during and just after POR

Errata type: Errata

Description: The programmable pull devices (up and down) on the analog differential inputs of the eQADC may randomly be enabled during the internal Power On Reset (POR) and until the 1st clock edge propagates through the device. After the first clock edge, the pull resistors will be disabled until software enables them.

Workaround: Protect any external devices connected to the differential analog inputs. The worst case condition is with a 1.4K ohm resistor to VDDA (5K pull-up enabled) or VSSA (5K pull-down enabled). This may also cause temporary additional current requirements on the VDDA supply of each eQADC module, up to 15 mA on each eQADC if both the pull up and pull down resistors are enabled simultaneously on all of the differential analog pins.

e2740: ETPU2: Watchdog Status Register (WDSR) may fail to update on channel timeout

Errata type: Errata

Description: The Watchdog Status Register (WDSR) contains a single watchdog status bit for each of the 32 eTPU channels per engine. When this bit is set, it indicates that the corresponding channel encountered a watchdog timeout and was aborted. Under certain conditions the corresponding bit is not set due to a watchdog timeout, and therefore no indication is available as to which channel timed out. However, the global exception is indicated correctly on a per engine basis, and the correct exception is issued to the interrupt controller and may be serviced.

Workaround: The application software should treat any watchdog event as a global eTPU exception and handle it in the eTPU global exception handler. Additionally, during the global exception handler the application should check the WDSR and clear any bits that may be set by writing '1' to that bit.

e3114: FLASH: Erroneous update of the ADR register in case of multiple ECC errors

Errata type: n/a

Description: An erroneous update of the Address register (ADR) occurs whenever there is a sequence of 3 or more events affecting the ADR (ECC single or double bit errors or RWW error) and both the following conditions apply:

- The priorities are ordered in such a way that only the first event should update ADR.

- The last event although it does not update ADR sets the Read While Write Event Error (RWE) or the ECC Data Correction (EDC) in the Module Configuration Register (MCR).

For this case the ADR is wrongly updated with the address related to one of the intervening events.

Example - If a sequence of two double-bit ECC errors is followed by a single-bit correction without clearing the ECC Event Error flag (EER) in the MCR, then the value found in ADR after the single-bit correction event is the one related to the second double-bit error (instead of the first one, as specified)

Workaround: Always process Flash ECC errors as soon as they are detected.

Clear MCR[RWE] at the end of each flash operation (Program, Erase, Array Integrity Check, etc...).

e3196: FLASH: PFCR3 is not directly writable

Errata type: n/a

Description: The Flash Configuration Register 3 (PFCR3) that can control the prefetching settings (Data Prefetch Enable [DPFEN], Instruction Prefetch Enable [IPFEN], Prefetch Limit [PFLIM], and Buffer Enable [BFEN]) of the Bank 1 (array 1 and array 2) flash modules is not directly writable. These settings are enabled by setting the Global Configuration Enable bit in the Flash Bus Interface Unit Control register (BIUCR).

Workaround: Set the GCE bit (BIUCR[GCE=1) to allow the Bank 0, Array 0 prefetch settings to also control bank 1 (Array 1 and Array 2); or program a default value for the PFCR3 register that gets loaded into the register at reset into the Flash Shadow block at address 0x00FF_FE08.

e2379: FMPLL: Loss-of-clock detection may cause unexpected reset

Errata type: Errata

Description: An unexpected Loss-Of-Clock (LOC) event may occur in the following scenario:

1. The FMPLL is initially powered down in bypass mode.

2. The FMPLL is then powered on (still in bypass mode).

3. The LOCK bit of the SYNSR register is polled to determine when the FMPLL is ready.

4. After the LOCK flag becomes set, the FMPLL is switched to normal mode.

5. Loss-of-clock detection is enabled by setting the LOCEN bit of the Enhanced Synthesizer Control Register 2 (ESYNCR2), either before or immediately after switching to normal mode.

The unexpected LOC event will activate the backup clock switching feature, causing the reference clock to be selected as the system clock. If LOC reset was also enabled by setting the LOCRE bit in the ESYNCR2 register, a system reset will occur.

The reason for the unexpected LOC event is that the time it takes for the Clock Quality Monitor (CQM) to detect a valid FMPLL clock is typically larger than the time it takes for the FMPLL to lock. Polling the LOC flag does not help because (the way it is defined) it does not flag LOC in bypass mode.

This issue only occurs when the FMPLL is turned off and then on again without going through a reset cycle. Immediately following reset, the issue can not occur because the CQM keeps the part in reset until it detects a valid crystal clock with plenty of time to detect a valid FMPLL clock.

Workaround: Any time the FMPLL is powered down, wait for 600us before activating the loss-of-clock function.

If the intent is just to re-program the FMPLL, it is not required to turn it off. FMPLL settings can be changed on the fly, and then the CQM will never indicate loss-of-clock.

e3407: FlexCAN: CAN Transmitter Stall in case of no Remote Frame in response to Tx packet with RTR=1

Errata type: Errata

Description: FlexCAN does not transmit an expected message when the same node detects an incoming Remote Request message asking for any remote answer.

The issue happens when two specific conditions occur:

1) The Message Buffer (MB) configured for remote answer (with code "a") is the last MB. The last MB is specified by Maximum MB field in the Module Configuration Register (MCR[MAXMB]).

2) The incoming Remote Request message does not match its ID against the last MB ID.

While an incoming Remote Request message is being received, the FlexCAN also scans the transmit (Tx) MBs to select the one with the higher priority for the next bus arbitration. It is expected that by the Intermission field it ends up with a selected candidate (winner). The coincidence of conditions (1) and (2) above creates an internal corner case that cancels the Tx winner and therefore no message will be selected for transmission in the next frame. This gives the appearance that the FlexCAN transmitter is stalled or "stops transmitting".

The problem can be detectable only if the message traffic ceases and the CAN bus enters into Idle state after the described sequence of events.

There is NO ISSUE if any of the conditions below holds:

a) The incoming message matches the remote answer MB with code "a".

b) The MB configured as remote answer with code "a" is not the last one.

c) Any MB (despite of being Tx or Rx) is reconfigured (by writing its CS field) just after the Intermission field.

d) A new incoming message sent by any external node starts just after the Intermission field.

Workaround: Do not configure the last MB as a Remote Answer (with code "a").

e3159: MPC563xM/SPC563M: MIDR MASKNUM field is set to 0x21

Errata type: Errata

Description: The mask revision field (MASKNUM[Major, Minor]) of the MCU Identification Register is 0b0010_0001 (0x21).

Workaround: Expect that the MASKNUM fields of the MIDR register will change in the future.

e3205: NEXUS: EVTI not functional on QFP176 and BGA208 packages

Errata type: n/a

Description: Event In (EVTI) is an input that is read on the negation of TRST (or JCOMP) to enable (if asserted) or disable (if deasserted) the Nexus Debug port.

After reset, EVTI is an input which, when asserted, will initiate one of two events based on the EIC (EVTI Control) bits in the DC1 (Development Control 1) Register (if the Nexus Class 2+ module is enabled at reset):

1) Program Trace and Data Trace synchronization messages (provided Program Trace and EIC = 0b00).

2) Debug request to e200z335 Nexus Class 1 module (provided EIC = 0b01 and this feature is implemented).

Workaround: 1) Do not expect Program Trace Sync messages after EVTI assertion. Other condition for the sync messaging are not impacted.

2) Do not use EVTI to request the CPU to enter the debug state. Other requests are functional.

In case EVTI functionality is needed, CSP496 package can also be used to emulate the 176QFP or the BGA208 packages.

e3425: PMC: 5V VDDREG POR De-assertion Max Level 4.2V

Errata type: Errata

Description: 5V Voltage regulator input (VDDREG) power on reset (POR) de-assertion maximum specification level is now 4.2V. Previously, the maximum specification level was 4.005V.

Workaround: Expect that 4.2V is required on the VDDREG input before the device will exit from a power on reset. The POR levels for VDDSYN and VDD in the data sheet are unchanged.

e3221: PMC: SRAM standby power low voltage detect circuit is not accurate

Errata type: n/a

Description: The power management controller (PMC) SRAM standby voltage low power detect circuit cannot reliably detect the brown-out condition if the standby supply is below 1.0 volts. The Status Register Brown Out Flag (PMC.SR[LVFSTBY]) bit may not be set during a brownout condition of the SRAM standby voltage or may be set even though no data has been lost.

Workaround: The application software should not rely on the PMC.SR[LVFSTBY] bit to detect corrupted SRAM values.

e2338: Pad Ring: Leakage if VDDE is greater than VDD33

Errata type: Errata

Description: If the VDDEx supplies (provided by an external supply) are greater than the VDD33 supplies (provided by the internal regulator), leakage current can occur through all pins powered by VDDEx from the VDDEx supply on the pad output driver through the pad towards ground. The highest leakage current occurs at high temperatures and is exponentially proportional to the VDDEx-VDD33 differential. Worst case leakage, per grounded pad at 150C is 29uA with a 200mV differential, and 590uA with a 400mV differential in the VDDEx-VDD33.

Any I/O configured as an input with the weak pull down enabled will rise towards VDDE level as the VDDE-VDD33 voltage differential increases (as the leakage current exceeds the weak pull-down capability). The reset state of most Nexus pads is pull-down, so this would not be guaranteed. EVTI is pulled up internally during and after RESET. EVTO must be pulled low externally for Auto-baud rate detection. I/O pads configured as outputs driving LOW will remain below VOL level but will consume the leakage current through the pad driver. External logic driving pads configured as inputs will have to sink this leakage current when driving LOW.

Workaround: Maintain a VDDE-VDD33 voltage difference below 200mV. If VDDE is greater than 3.45V, the PMC_TRIMR[VDD33TRIM] for the internal regulator can be increased to 4 steps above typical (0b1011) to increase VDD33 default voltage by a nominal value of 120mV.

e3377: Pad Ring:Nexus pins may drive an unknown value immediately after power up but before the 1st clock edge

Errata type: Errata

Description: The Nexus Output pins (Message Data outputs 0:15 [MDO] and Message Start/End outputs 0:1 [MSEO]) may drive an unknown value (high or low) immediately after power up but before the 1st clock edge propagates through the device (instead of being weakly pulled low). This may cause high currents if the pins are tied directly to a supply/ground or any low resistance driver (when used as a general purpose input [GPI] in the application).

Workaround: 1. Do not tie the Nexus output pins directly to ground or a power supply.

2. If these pins are used as GPI, limit the current to the ability of the regulator supply to guarantee correct start up of the power supply. Each pin may draw upwards of 150mA.

If not used, the pins may be left unconnected.

e1421: SWT: switching SWT to system clock has very small chance of causing the SWT to enter an indeterminate state

Errata type: Errata

Description: The reset value for the clock source of the Software Watchdog Timer module (SWT) is the oscillator clock. If the clock source is switched to the system clock by clearing Clock Selection bit in the SWT Module Control Register (SWT_MCR[CSL]=0), then the SWT has a very small chance of entering an indeterminate state.

Workaround: Only use the oscillator clock as the SWT clock source.

e1297: eSCI : reads of the SCI Data Register, which clears the RDRF flag, may cause loss of frame if read occurs during reception of the STOP bit

Errata type: Errata

Description: A received SCI frame is not written into the SCI Data Registers and the Overrun (OR) flag is not set in the SCI Status Register 1 (SCISR1), if:

1.) The eSCI has received the last data bit of an SCI frame n

2.) and the Receive Data Register Full (RDRF) flag is still set in the SCISR1 after the reception of SCI frame n-1

3.) and during the reception of the STOP bit of frame n the host reads the SCI Data Registers, and clears the RDRF flag

In this case the RDRF flag is erroneously set again by the controller instead of the OR flag. Thus, the host reads the data of frame n-1 a second time, and the data of frame n is lost.

Workaround: The application should ensure that the data of the foregoing frame is read out from the SCI Data Registers before the last data bit of the actual frame is received.

e1381: eSCI: LIN Wakeup flag set after aborted LIN frame transmission

Errata type: Errata

Description: If the eSCI module is transmitting a LIN frame and the application sets and clears the LIN Finite State Machine Resync bit in the LIN Control Register 1 (eSCI_LCR1[LRES]) to abort the transmission, the LIN Wakeup Receive Flag in the LIN Status Register may be set (LWAKE=1).

Workaround: If the application has triggered LIN Protocol Engine Reset via the eSCI_LCR1[LRES], it should wait for the duration of a frame and clear the eSCI_IFSR2[LWAKE] flag before waiting for a wakeup.

e1221: eSCI: LIN bit error indicated at start of transmission after LIN reset

Errata type: Errata

Description: If the eSCI module is in LIN mode and is transmitting a LIN frame, and the application sets and subsequently clears the LIN reset bit (LRES) in the LIN Control register 1 (ESCI_LCR1), the next LIN frame transmission might incorrectly signal the occurrence of bit errors (ESCI_IFSR1[BERR]) and frame error (ESCI_IFSR1[FE]), and the transmitted frame might be incorrect.

Workaround: There is no generic work around. The implementation of a suitable workaround is highly dependent on the application and a workaround may not be possible for all applications.

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