

MSIS LAB

Introduction To MSIS Lab

Research of Touch Screen Chips

2018. 05



Prof. HyungWon Kim

MSIS LAB

Department of Electronics Engineering

Chungbuk National University

MSIS LAB'S RESEARCH (CIRCUIT AREAS)

Low Power Voltage Converters & Mixed Signal Circuits

- ◇ Ultra Low Power Switched Capacitor Voltage Converter & Digital Controller circuit (0.13um Magnachip)
- ◇ Split Charging and Energy Recycling and Voltage Converter Chip (0.13um Magnachip)
- ◇ Swapping Switched Capacitor Array and Self Charing Voltage Scaler Chip (0.13um Magnachip)
- ◇ DC-DC Converter Chip with On-Chip Inductor and Capacitor (0.13um Magnachip)
- ◇ Energy Harvesting Circuit (Based on RF wireless power, Piezo, solar cell)
- ◇ Low Power 12bit SAR ADC, 16bit Sigma-Delta ADC & Decimation Digital Filter, 12bit DAC 및 Digital Controller Circuit (Verilog) Design

High Sensitivity Sensor & Sensing SoC Chip Design

- ◇ High Sensitivity Differential Fingerprint Sensor Chip (0.13um Magnachip)
- ◇ Differential Fingerprint Sensor Mismatch Calibration Circuit
- ◇ RF Signal Based 3D depth Fingerprint Sensor and chip design
- ◇ High Speed Differential Touch Screen Sensor Read-out IC & Digital Controller SoC Chip design (65nm Samsung, 0.13um Magnachip)
- ◇ FDCS (Frequency Division Concurrent Sensing) Based Large Touch Screen Sensing circuit & SoC Chip design (65nm Samsung, 0.13um Magnachip)

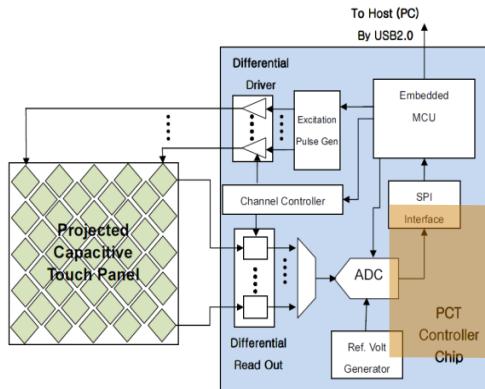
Part 01



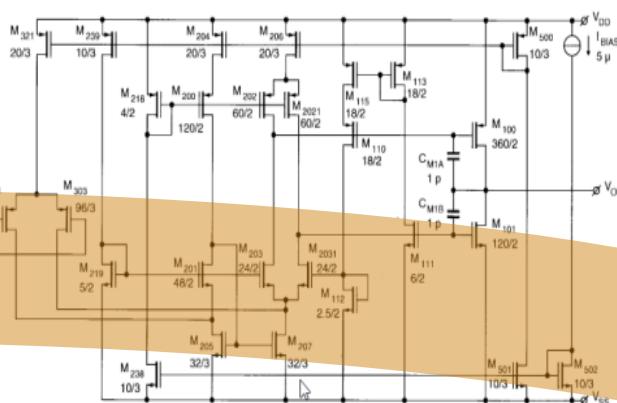
Mixed Signal SoC /
Touch Screen SoC

Mixed Signal SoC Design Methodology

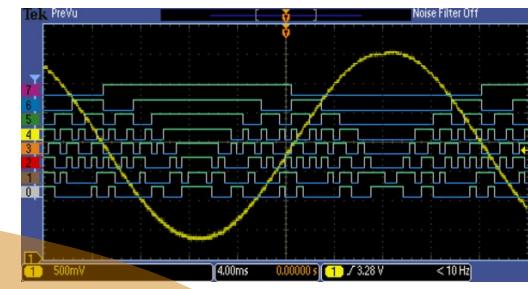
◆ Architecture Design



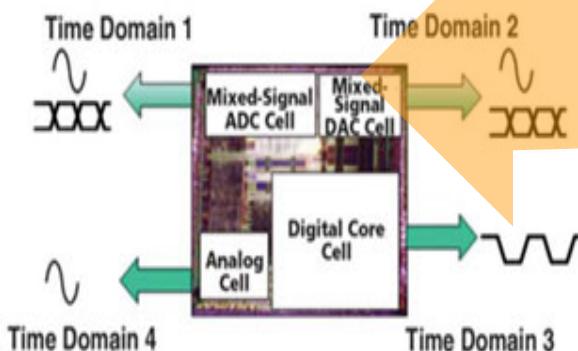
◆ Circuit Design



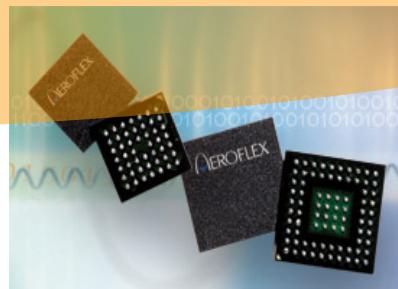
◆ Simulation and Verification



◆ Chip Test



◆ Chip Fabrication



◆ FPGA Design and Test

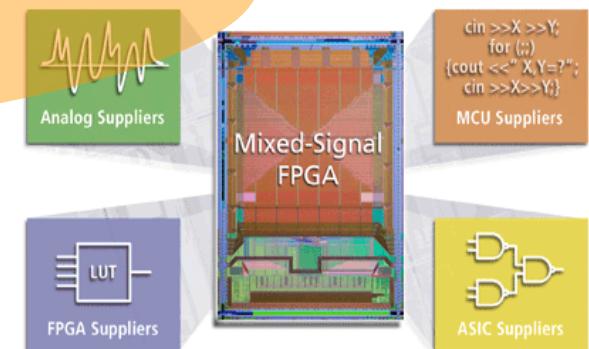


Figure 1. Design challenges require a mixed-signal FPGA

Target Applications for Mixed Signal SoC

❖ Large Multi-Touch Screen



❖ Large Touch / Digital Signage



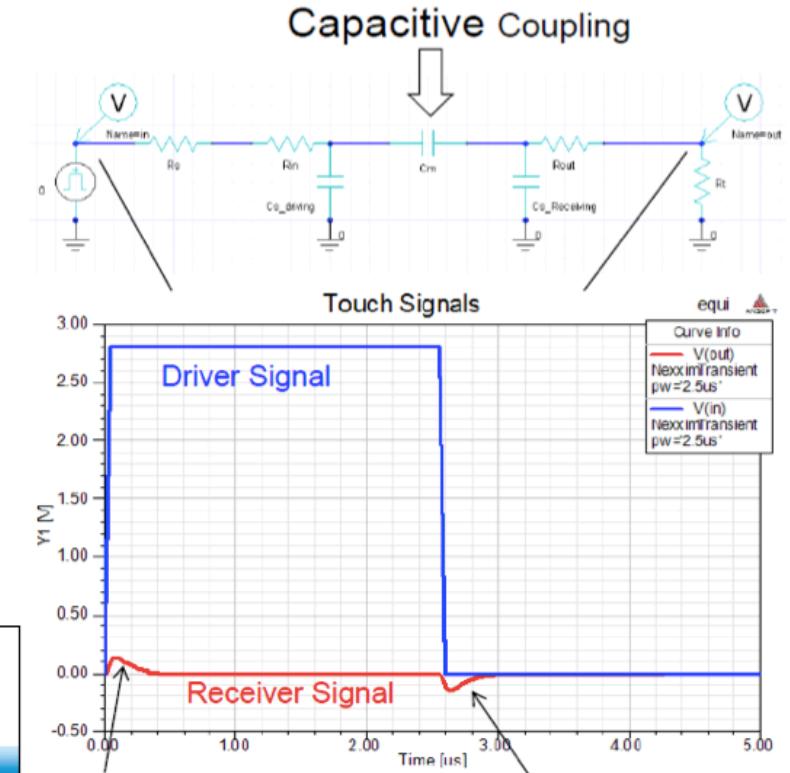
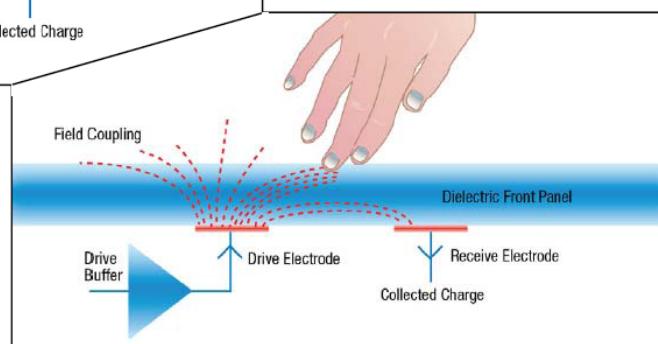
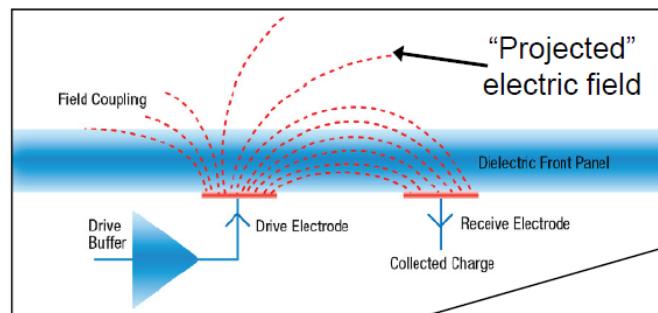
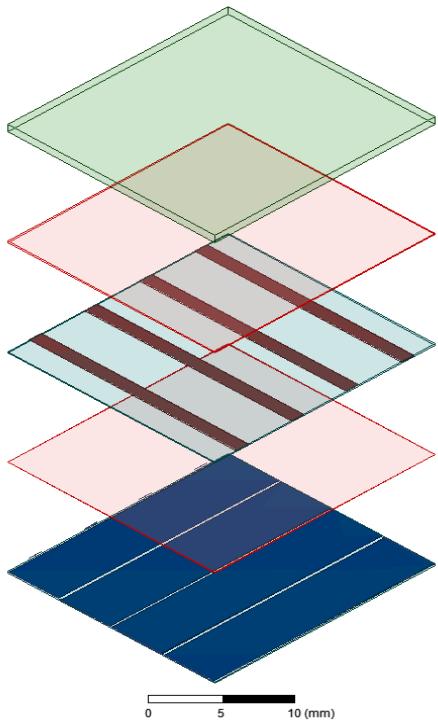
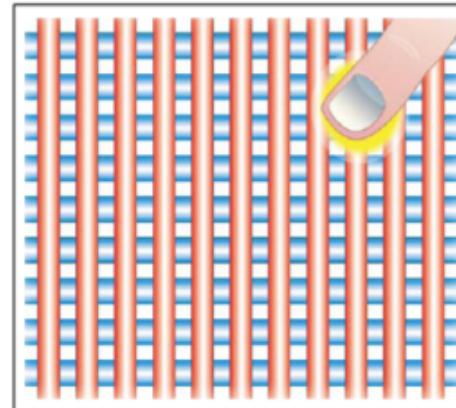
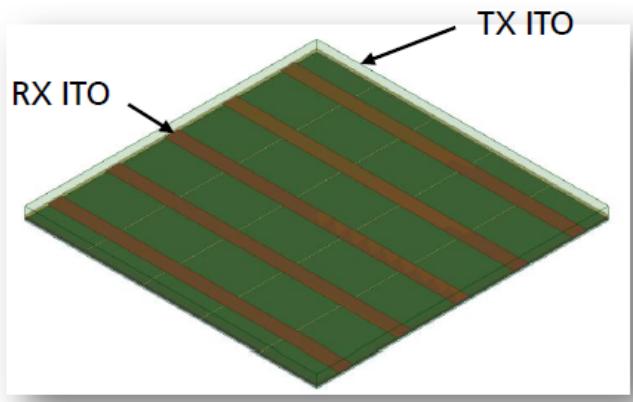
❖ Medical Sensors



❖ Bio Sensors



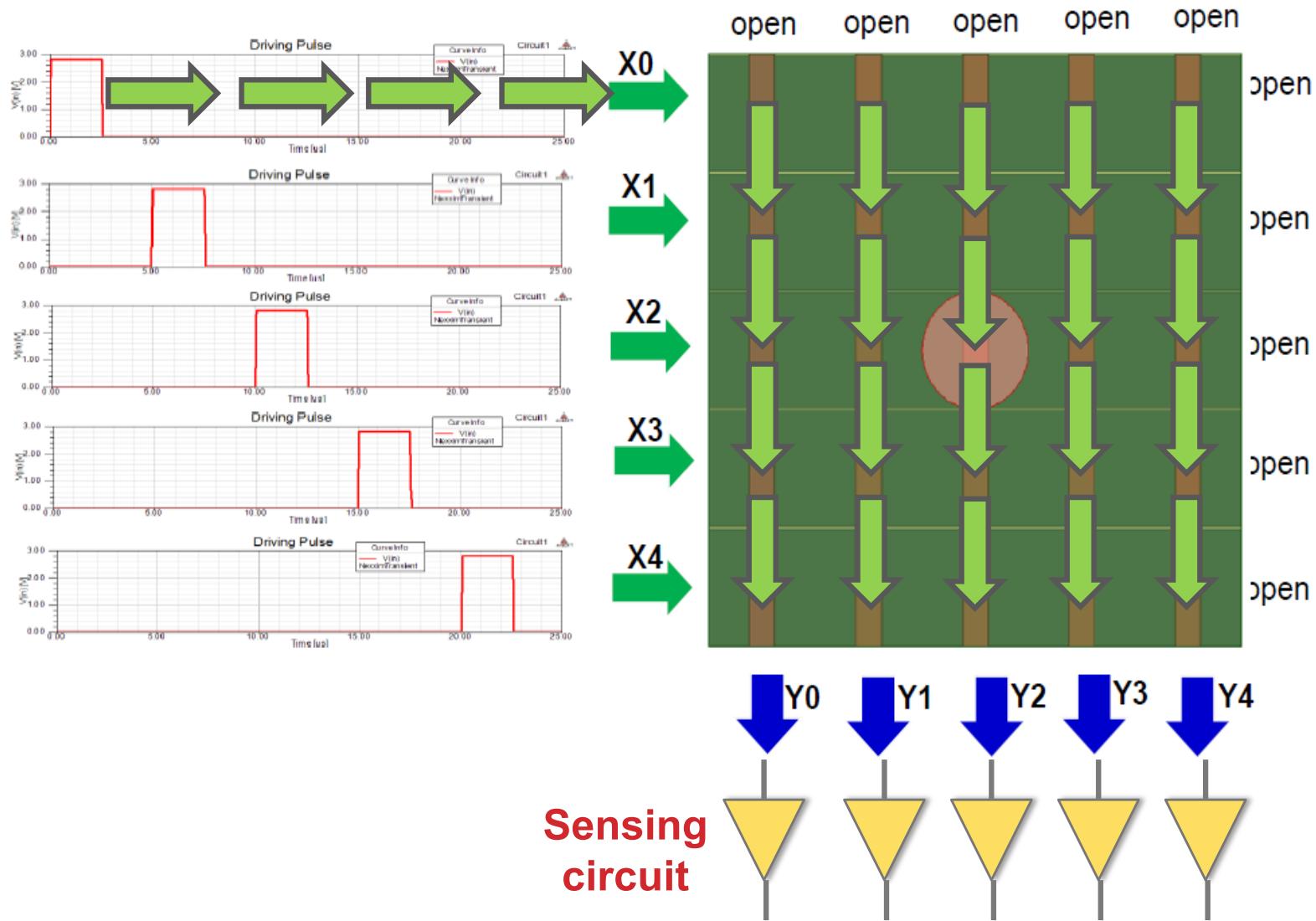
Target Touch Screen Type: Projected Capacitive / Mutual Capacitance



- Touch

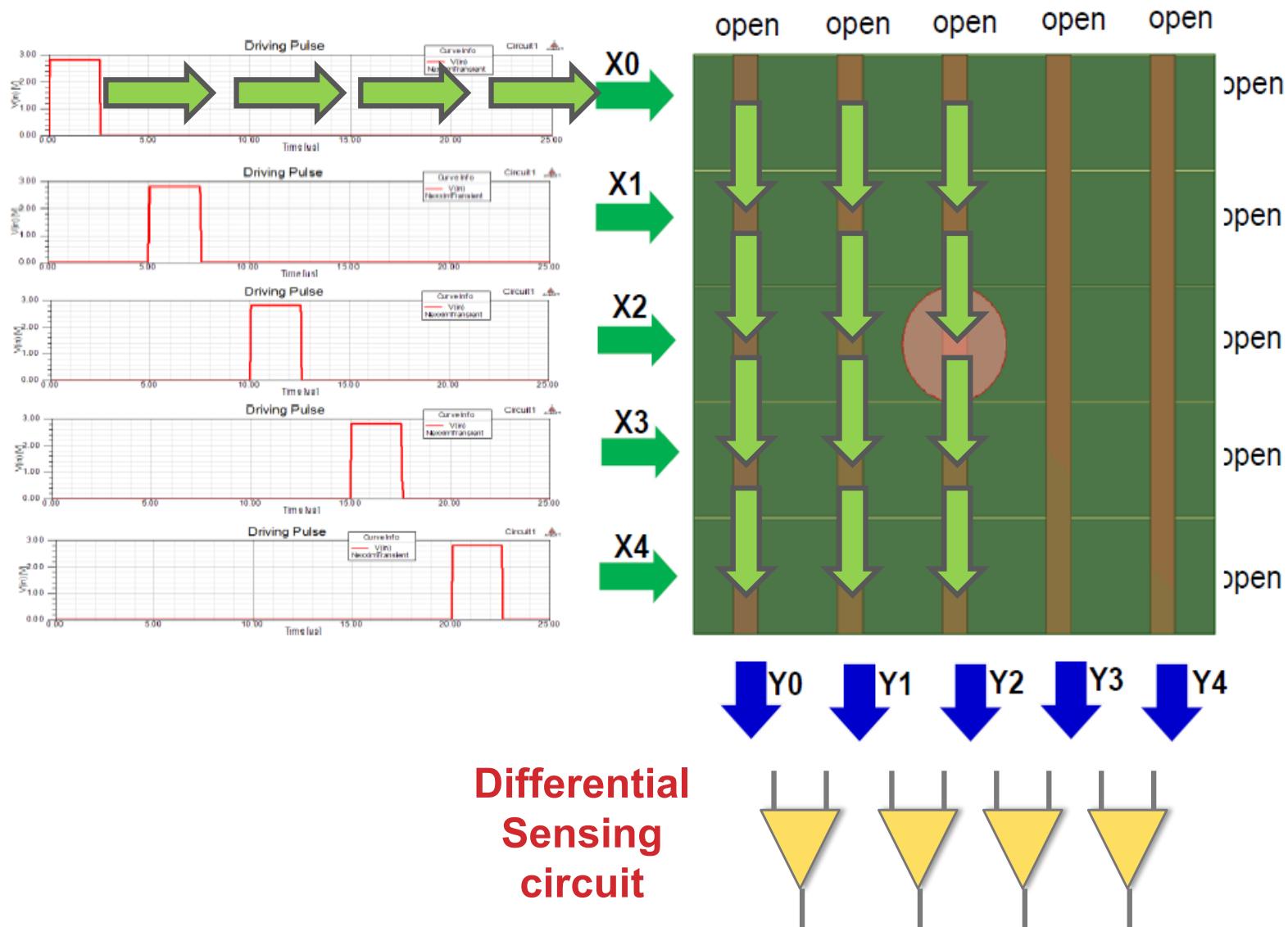
Single Line Sensing Method

❖ Single Line Sensing TSP Operations



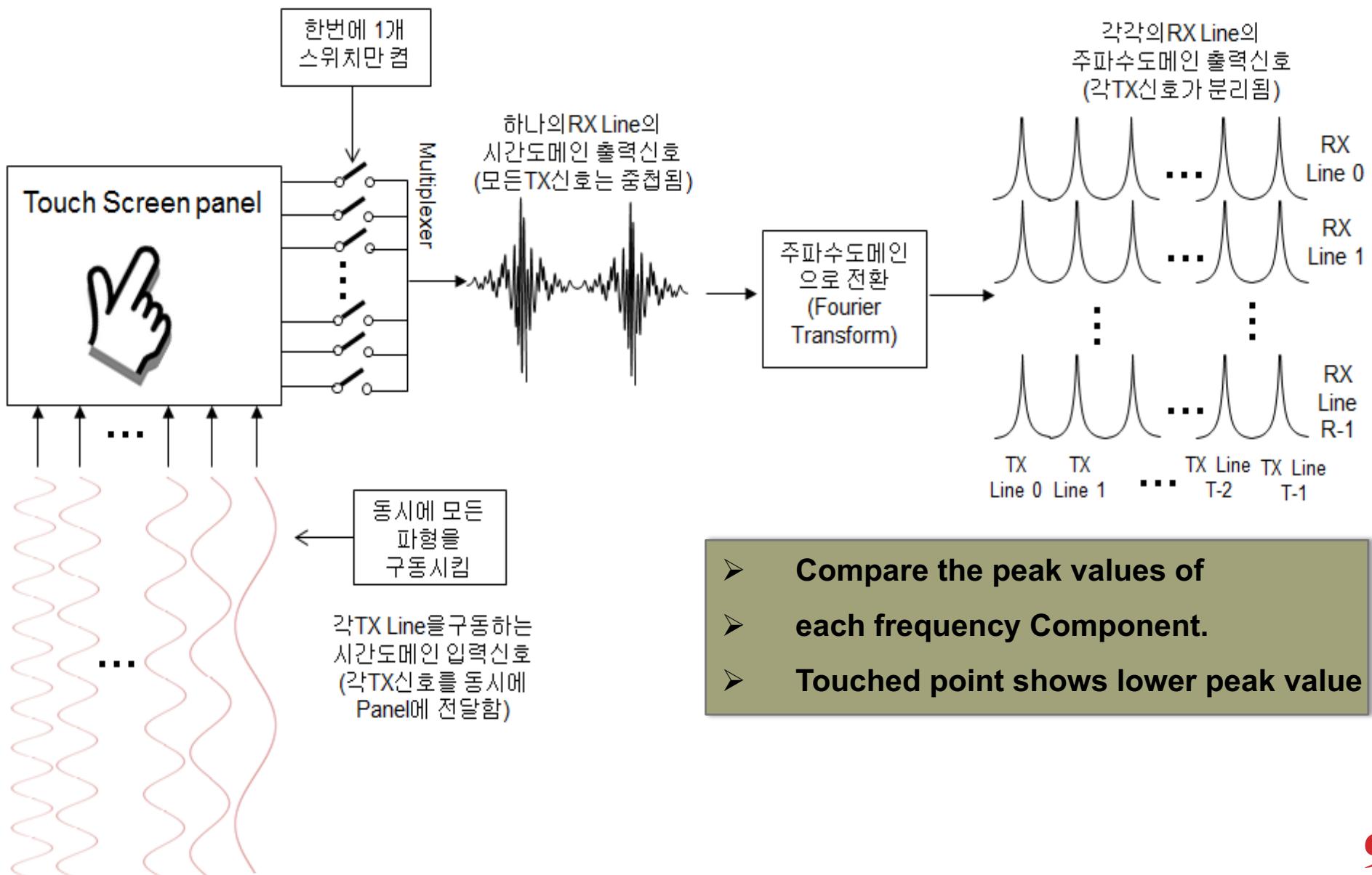
Differential Sensing Method

❖ Differential Sensing TSP Operations



FDCS (Freq. Division Concurrent Sensing) Method

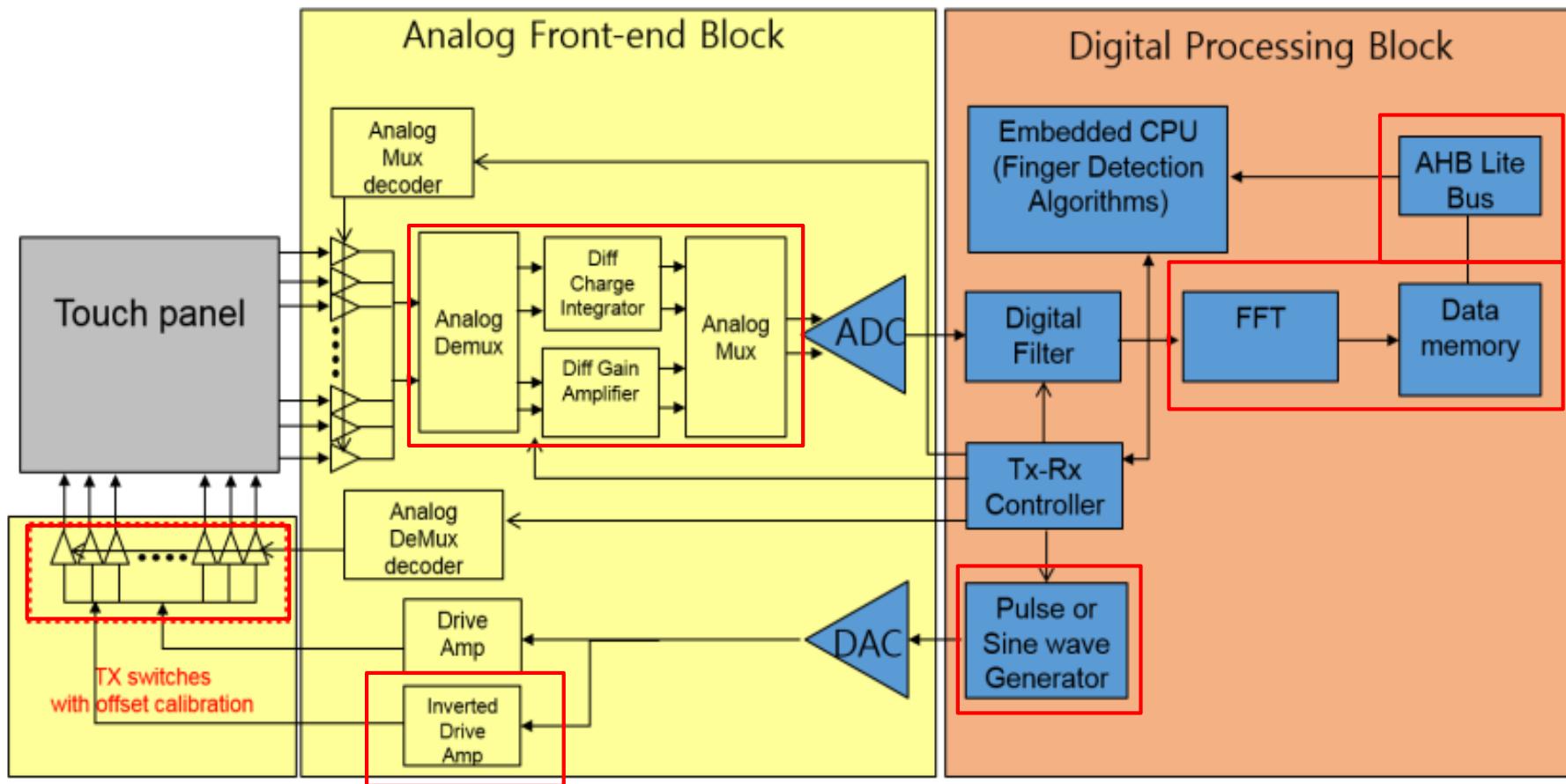
❖ FDCS System Architecture



FDCS Touch Screen Controller Architecture

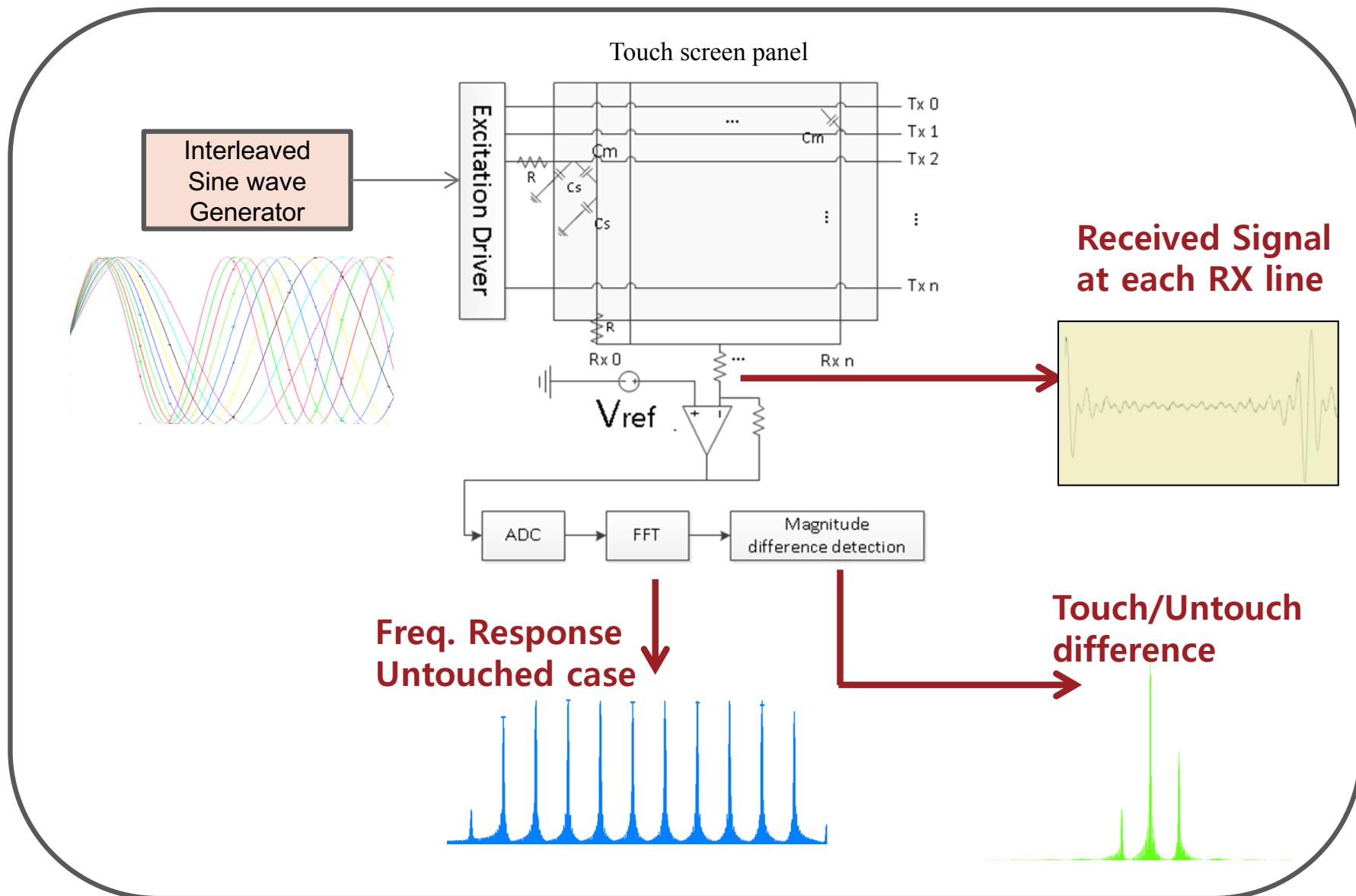
❖ Frequency division concurrent sensing method (FDCS)

- Single or differential line driving (pulse mode)
- Differential Gain amplifier, Differential charge integrator
- Sine wave mode concurrent driving and RX sensing with FFT



FDCS (Freq. Division Concurrent Sensing)

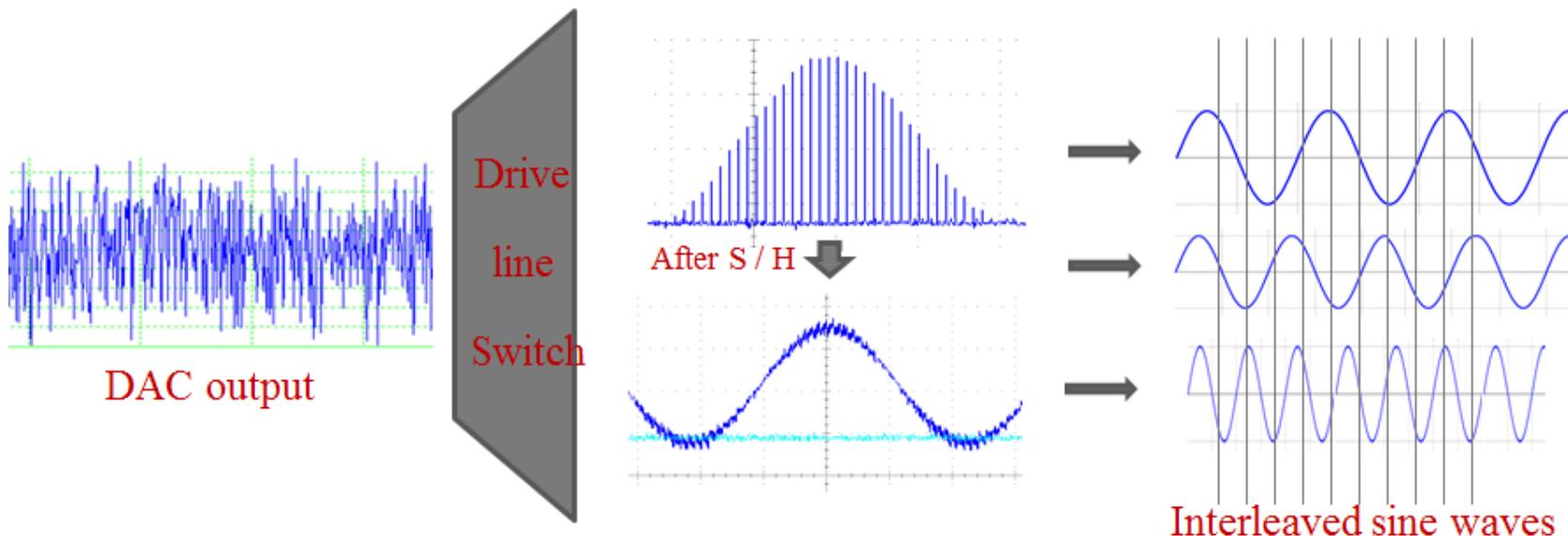
❖ Basic Operations



Concurrent Sine Wave Generator

❖ Interleaved Sine Waves with a Single Sample & Hold DAC

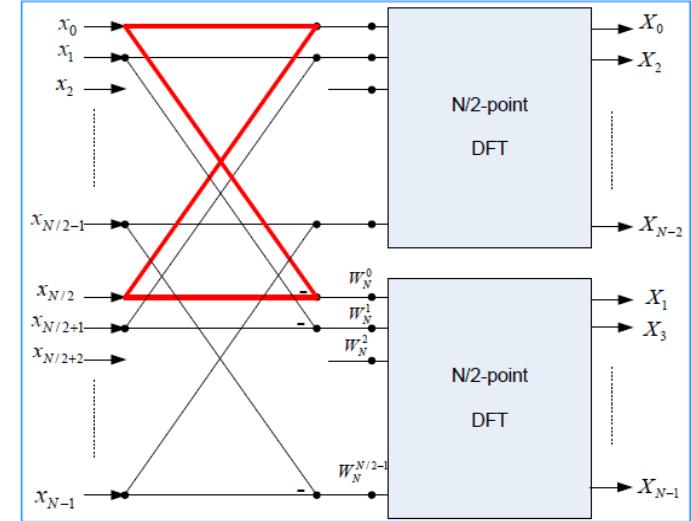
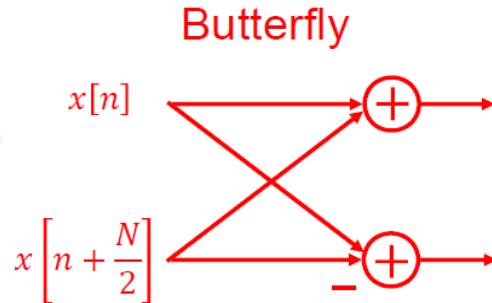
- Pre-calculated Sine Wave Samples Stored in Memory
- Digital block reads out N sine waves and interleave them
- Send each sample of the interleaved sine waves to 1 DAC
- Analog Demux sends each sine wave value (DAC output) to each TX line
- Analog Sine waves of different frequencies are simultaneously applied to all TX lines



FFT (Fast Fourier Transform) Design

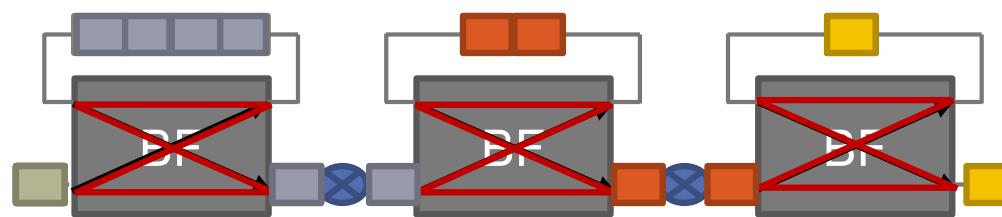
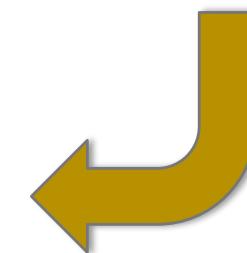
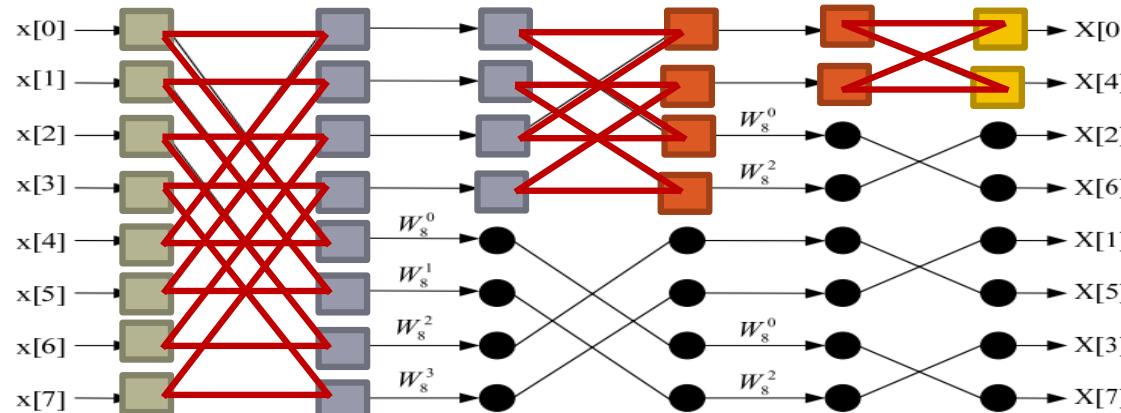
- ❖ FFT to convert RX signals from Touch Screen to Frequency domain

$$X_k = \sum_{n=0}^{N-1} e^{-2\pi i k \cdot (n/N)} x_n$$



❖ Pipelined FFT Design

- Decimation in Frequency (DIF)
- Single-Path Delay Feedback(SDF)
- 8 point Example below (256 point used in the chip)

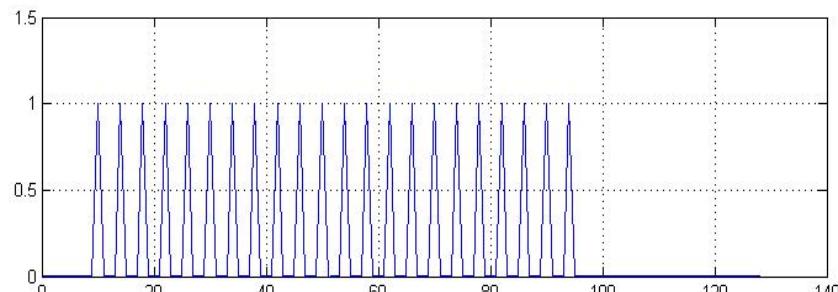


FDCS Simulation Results

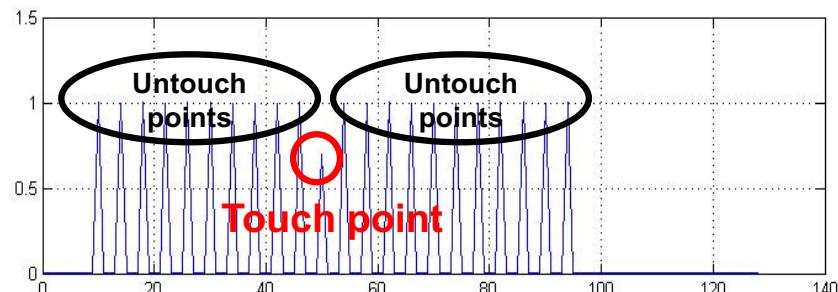
❖ Simulation comparison of MATLAB & Cadence Spectre (SPICE)

- MATLAB Simulation with Simplified model

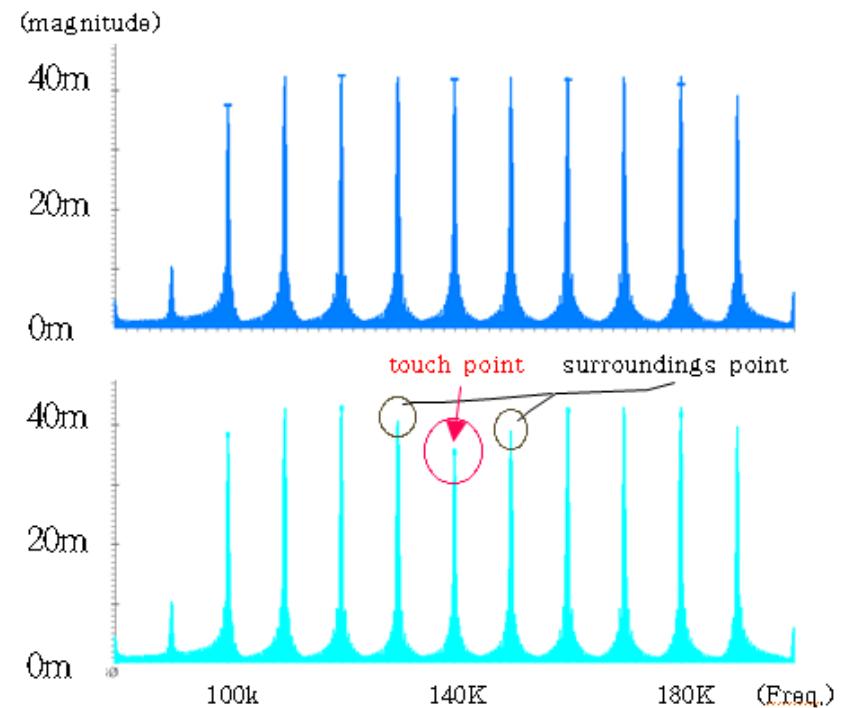
- Untouched case



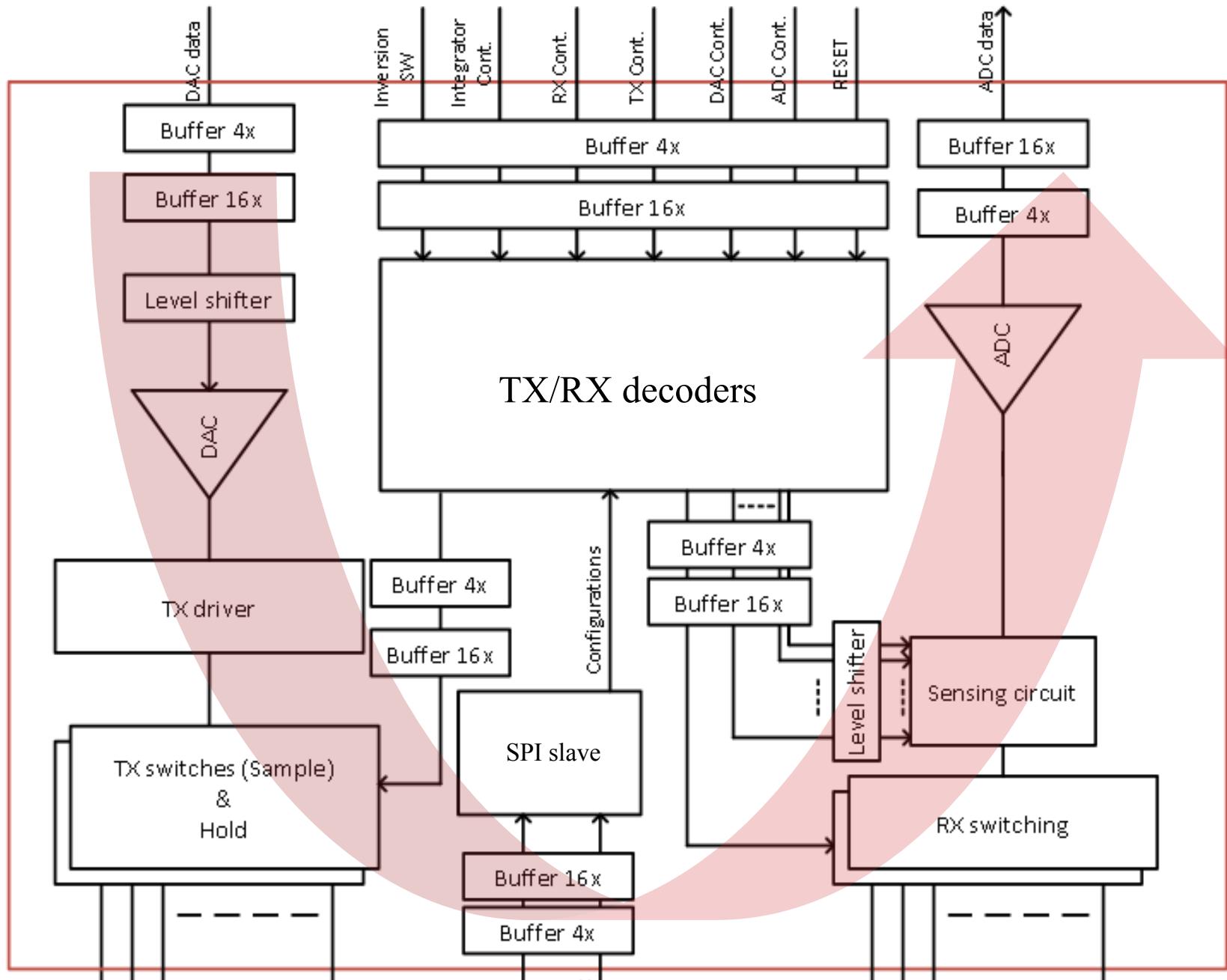
- Touched case



- Cadence Spectre (SPICE) Simulation with Touch Screen Model



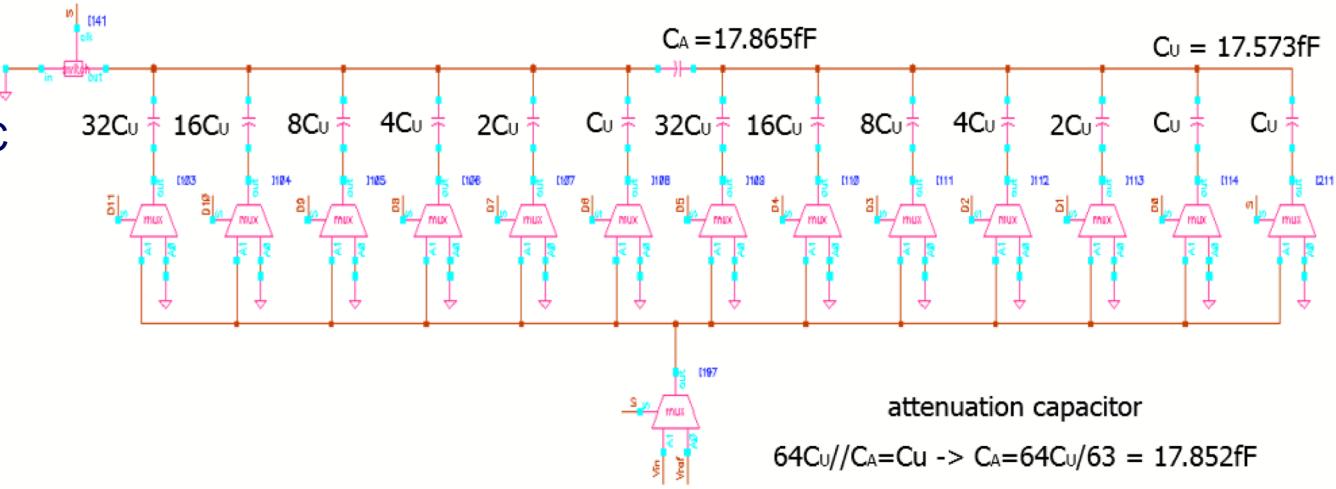
FDCS Analog Chip Architecture



DAC & ADC DESIGN

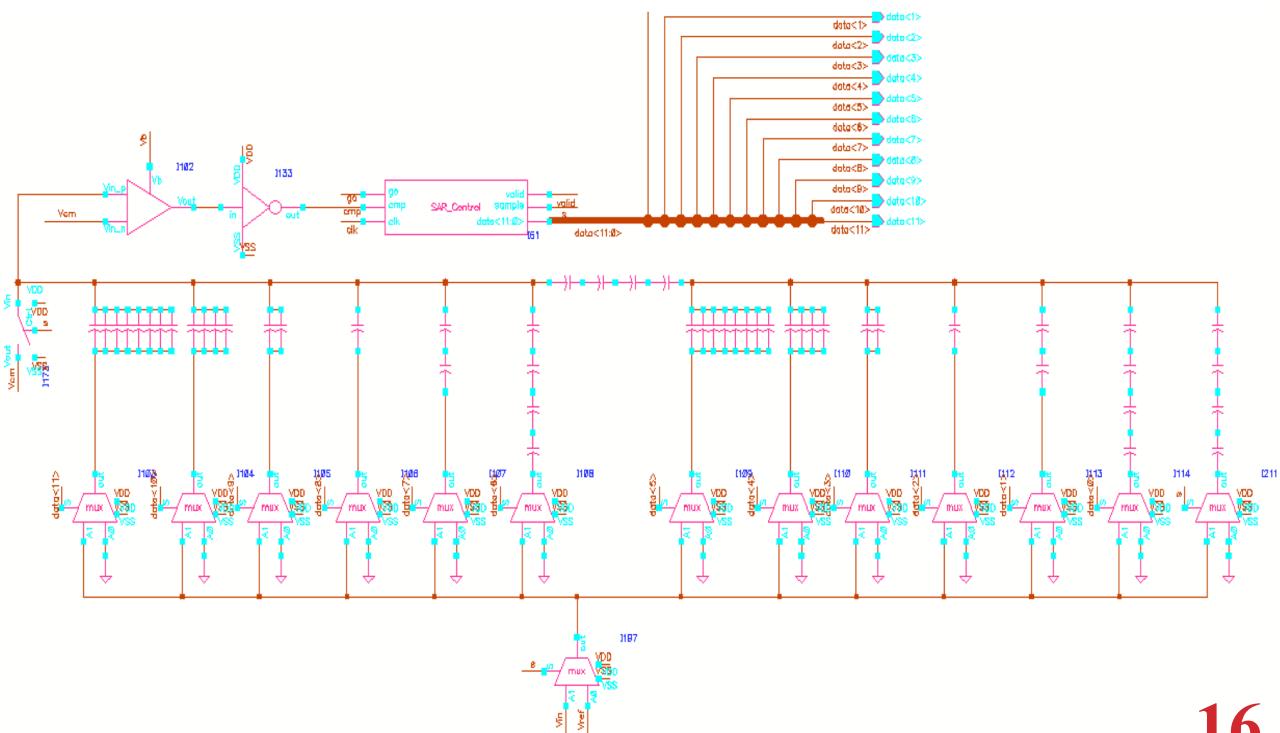
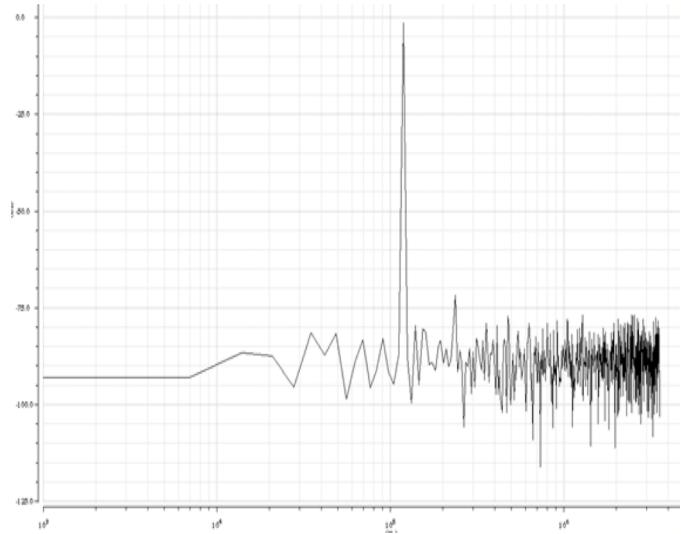
❖ 12bit DAC

- Parallel Charge Scaling DAC
- Used split capacitor to reduce the overall cap size
- Sampling Freq: 100MHz



❖ 12bit SAR ADC

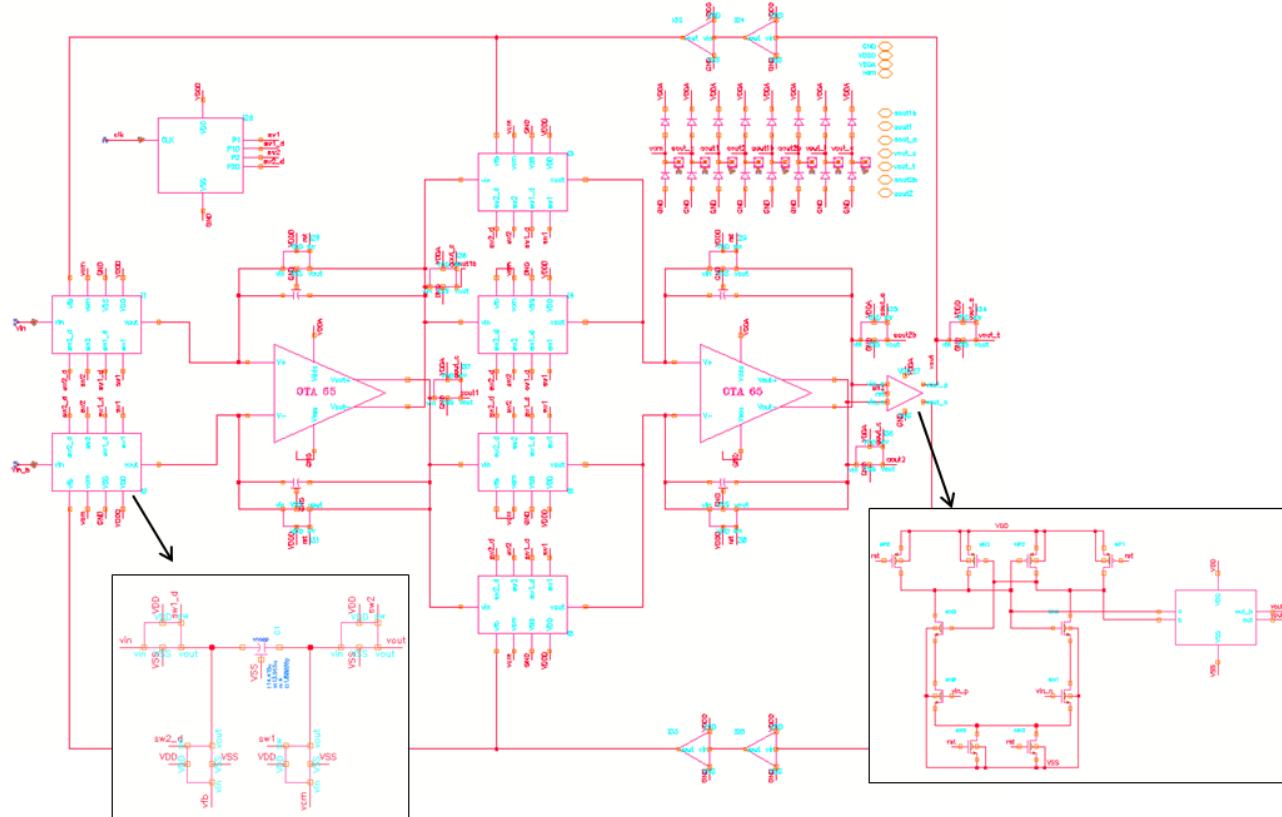
- ENOB : 8.5 bits
- Sampling freq: 5.1Mhz



DAC & ADC DESIGN

❖ 12bit Sigma-Delta ADC

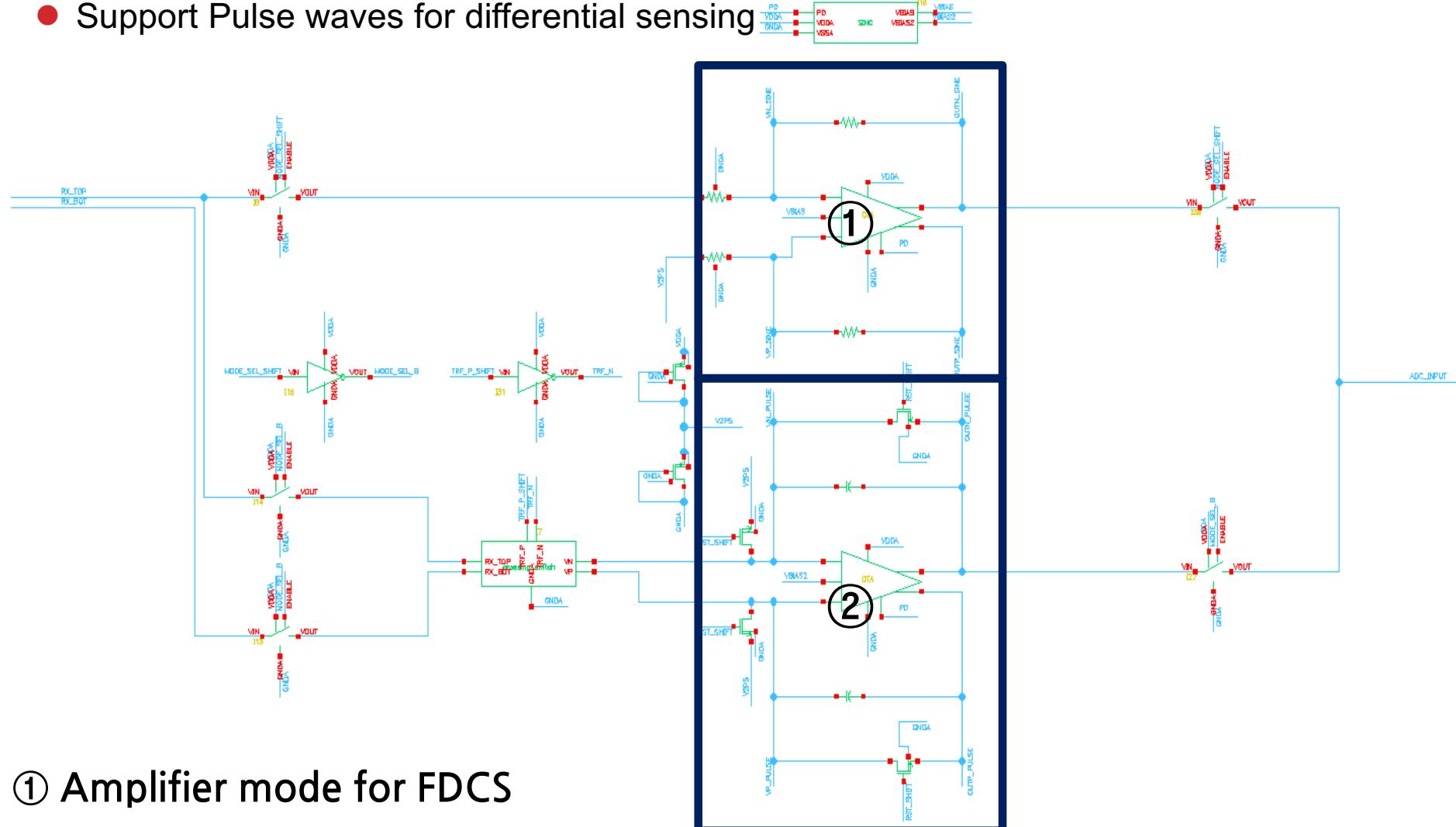
- Parallel Charge Scaling DAC
- Used split capacitor to reduce the overall cap size
- Sampling Freq: 100MHz



RX Sensing Circuit

❖ Integrated sensing circuit with 2-modes:

- Support Sine Waves for FDCS
- Support Pulse waves for differential sensing



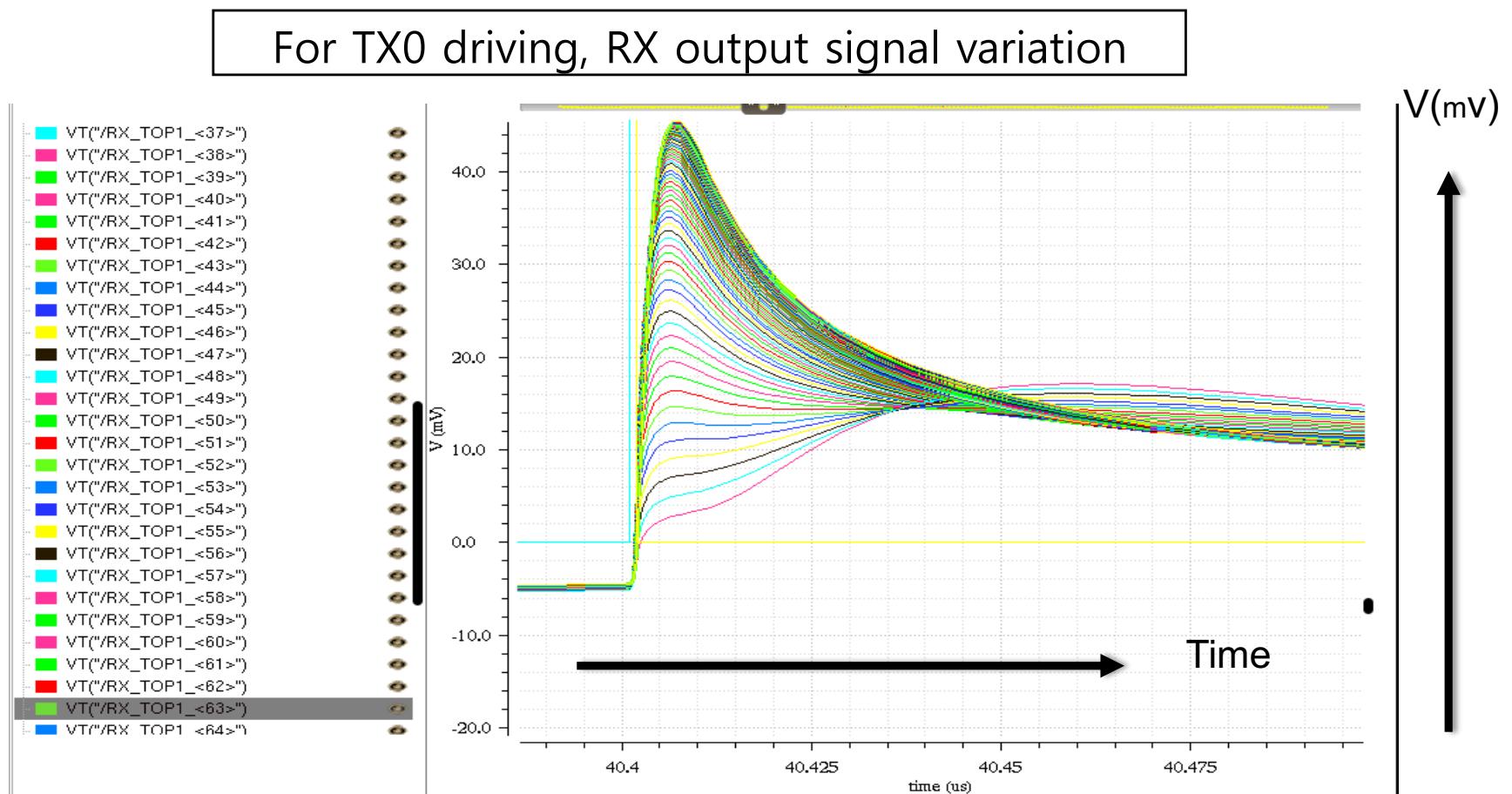
① Amplifier mode for FDCS

② Integrator mode for differential sensing

RX Sensing Circuit (Integrator)

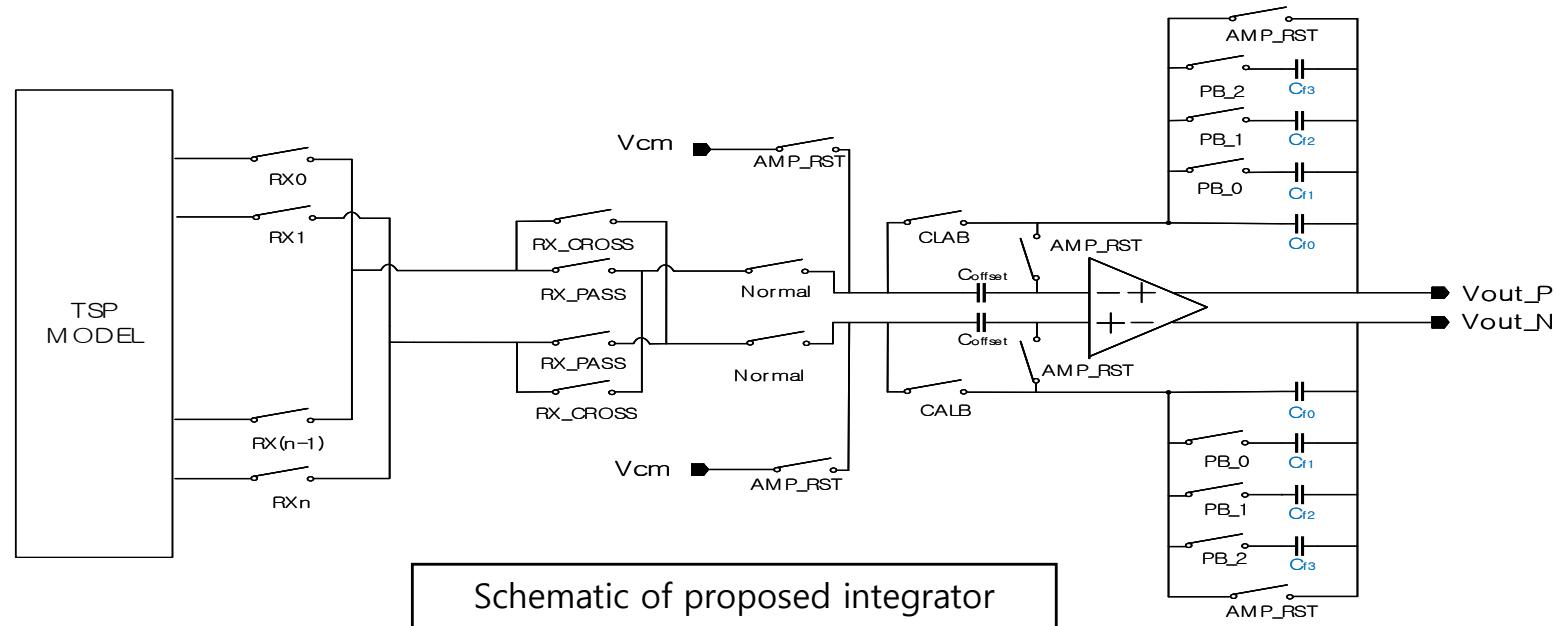
❖ Integrator Gain Compensation with Path balancing

- RX signals of touch screen vary in a wide range depending on the path length
- The path length is determined by the TX line and RX line

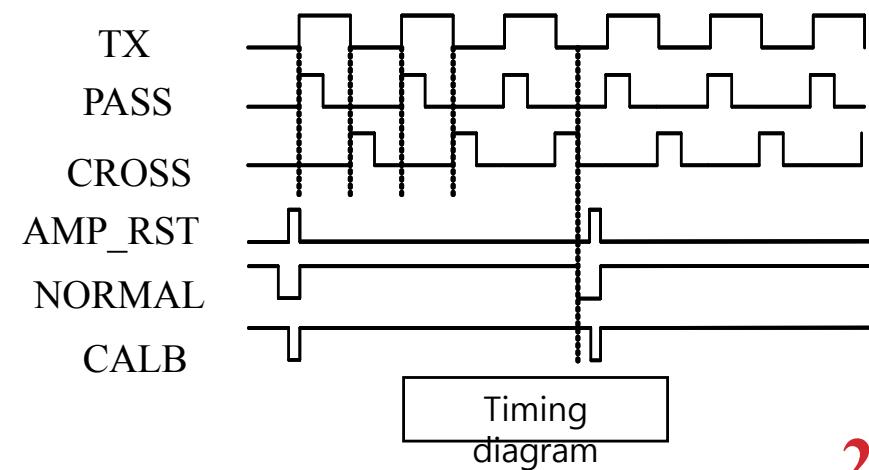


RX Integrator With Path Balancing

❖ Offset Calibration Integrator with Path balancing

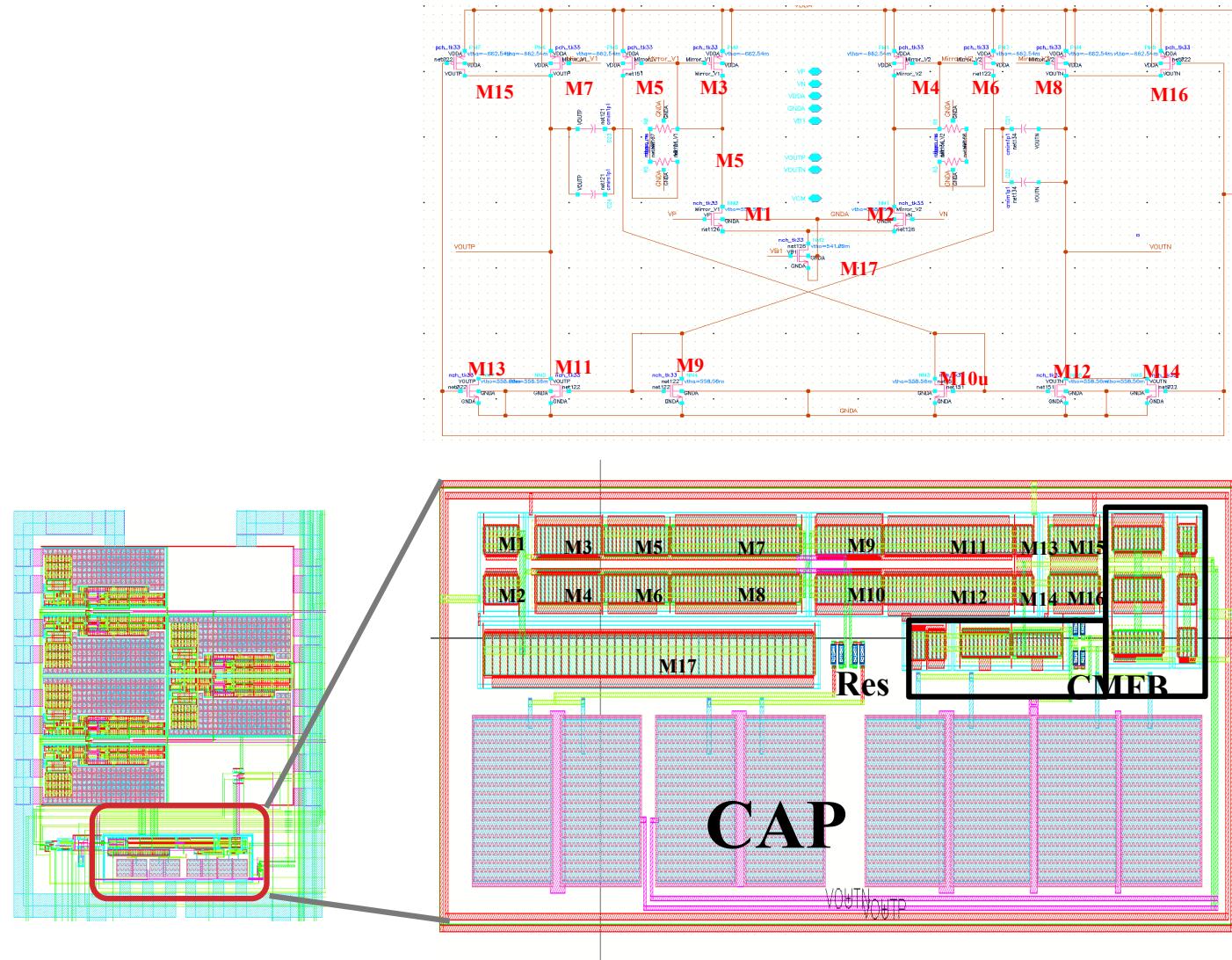


PASS : pass signal
CROSS : cross signal
AMP_RST : Integrator_rst & Calibration
NORMAL : work Integrator
CALB : AMP_RST signal inversion
PB_Signal : Integrator gain control



RX Sensing Circuit Layout

❖ Layout of RX Sensing Circuit



SNR Performance Measurement

❖ SNR for Touch Detection

$$SNR(dB) = 20 \log(TouchStrength / Noise Touched_{\gamma ms100})$$

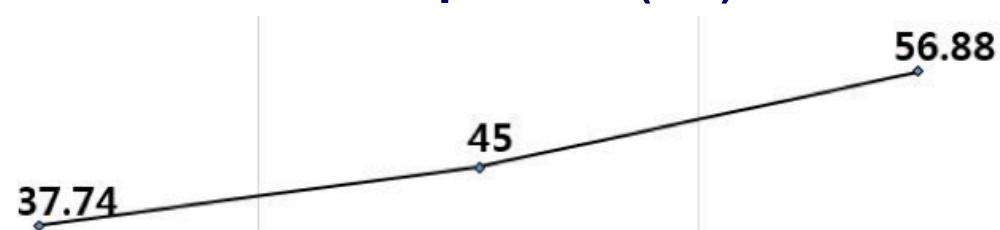
$$TouchStrength = Signal Touched_{AVG100} - Signal Untouched_{AVG100}$$

$$Noise Touched_{\gamma ms100} = \sqrt{\frac{\sum_{n=0}^{n=99} (Signal[n] - Signal Touched_{AVG100})^2}{100}}$$

❖ Voltage-Shifting Integrator SNR Comparison

	Conventional Integrator	Voltage-Shifting Integrator
TSP size	TX:44, RX:78	TX:44, RX:78
SNR at Sensing Circuit	0.34 dB	15.52 dB
SNR Gain	28.0 dB	43.39 dB

❖ Rotating Auto-Zeroing SNR Comparison (dB)

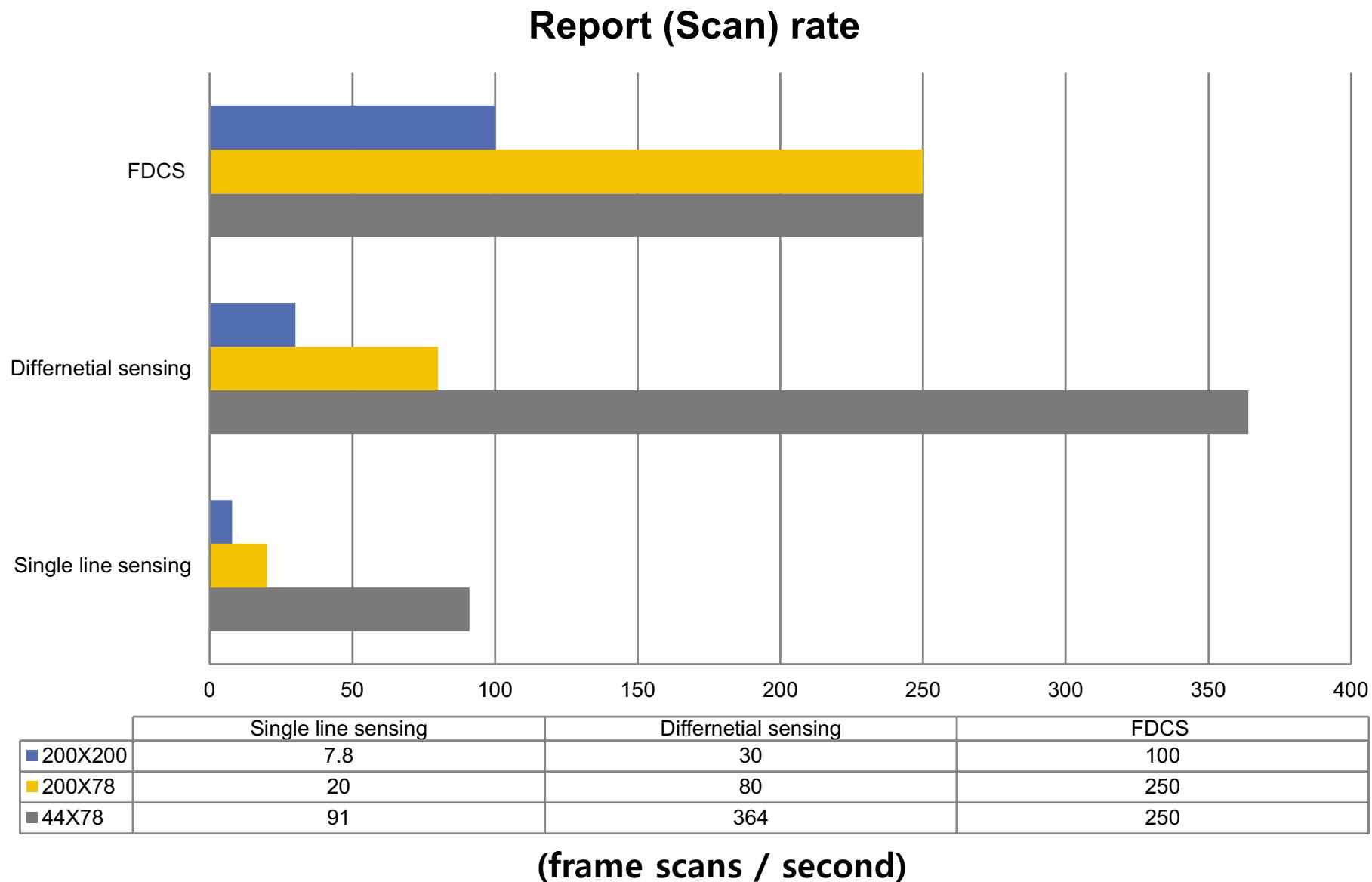


Conventional Method :
Differential Sensing without Auto-Zeroing

Differential Line Sensing using Conventional Auto-Zeroing Amplifier

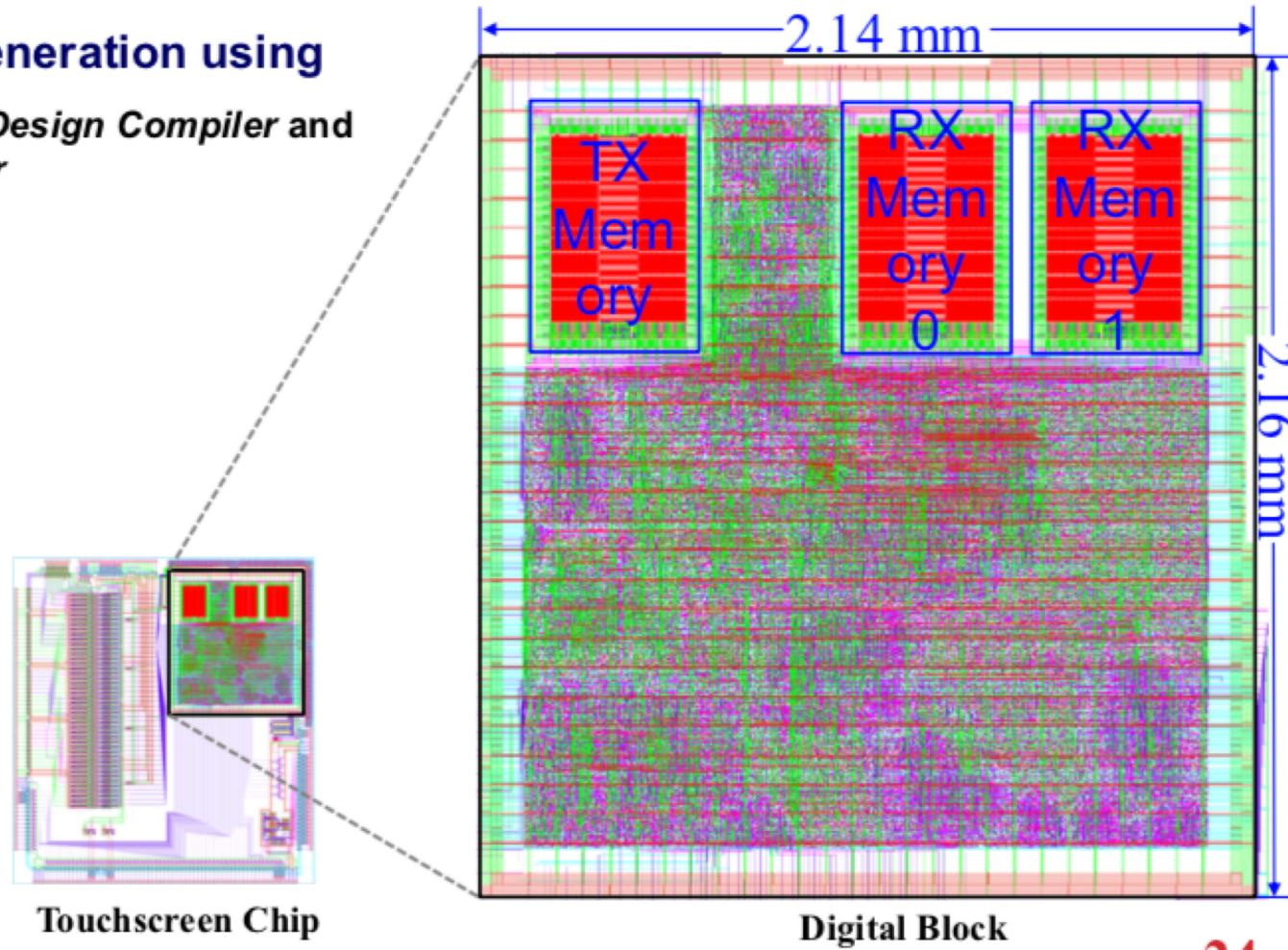
Differential Line Sensing using RAZA with Offset cancellation

Speed Performance Comparison



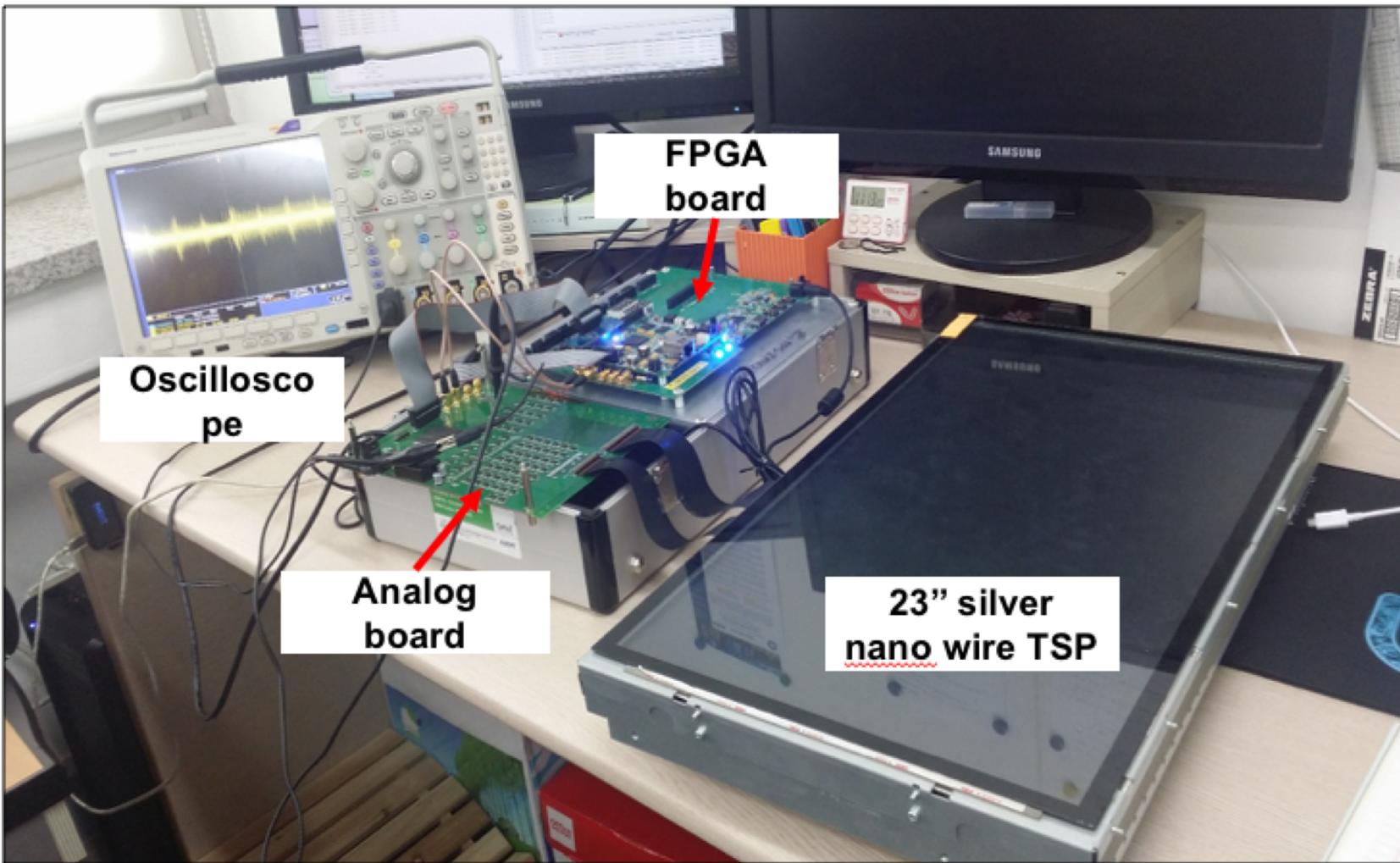
Digital Controller Layout Design

- ❖ Implemented in Verilog
- ❖ Layout generation using
 - Synopsys *Design Compiler* and *IC Compiler*



Testing Environment Set Up

- ❖ Touch screen controller Test Platform



Touch Screen Controller Soc MPWs

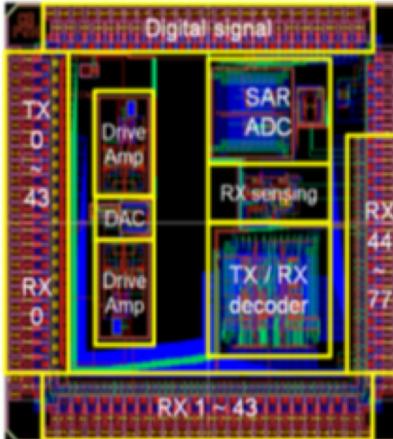
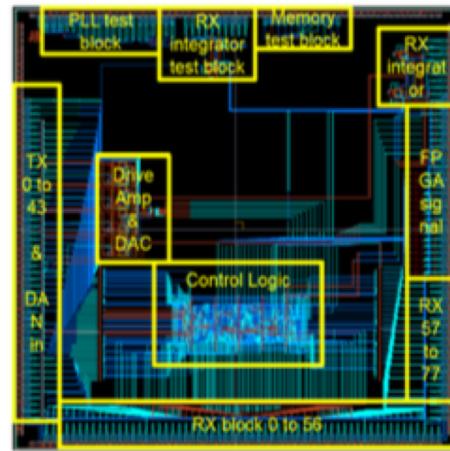
❖ Previous MPWs

Towerjazz 0.18um

Target Large Touch screen Controller Chip (Analog)

Chip Size 5mm x 5mm

Gate Count 1,222



DONGBU 0.18um

Target Frequency Division Concurrent Sensing Circuit (Analog)

Chip Size 2.35mm x 2.35mm

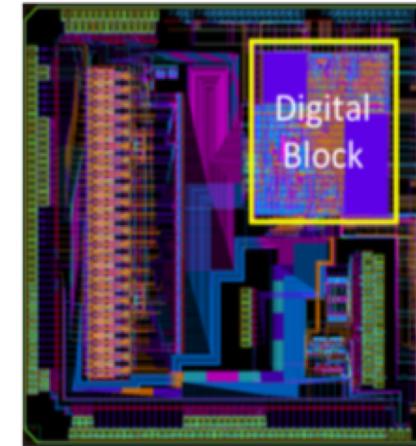
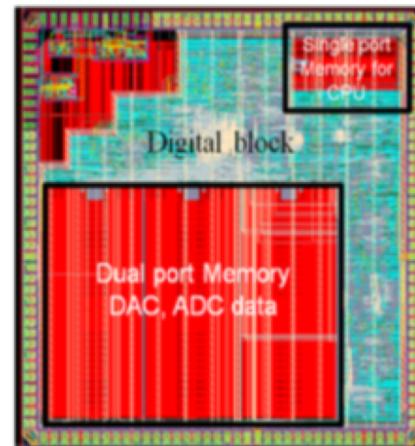
Gate Count 1,591

TSMC 0.18um

Target Frequency Division Concurrent Sensing SoC (Digital)

Chip Size 3mm x 3mm

Gate Count 647,649



SAMSUNG 65nm

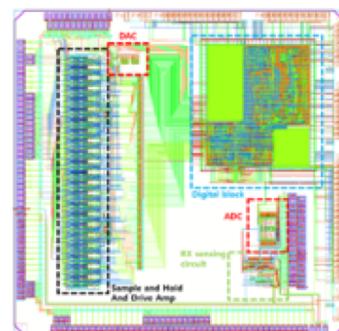
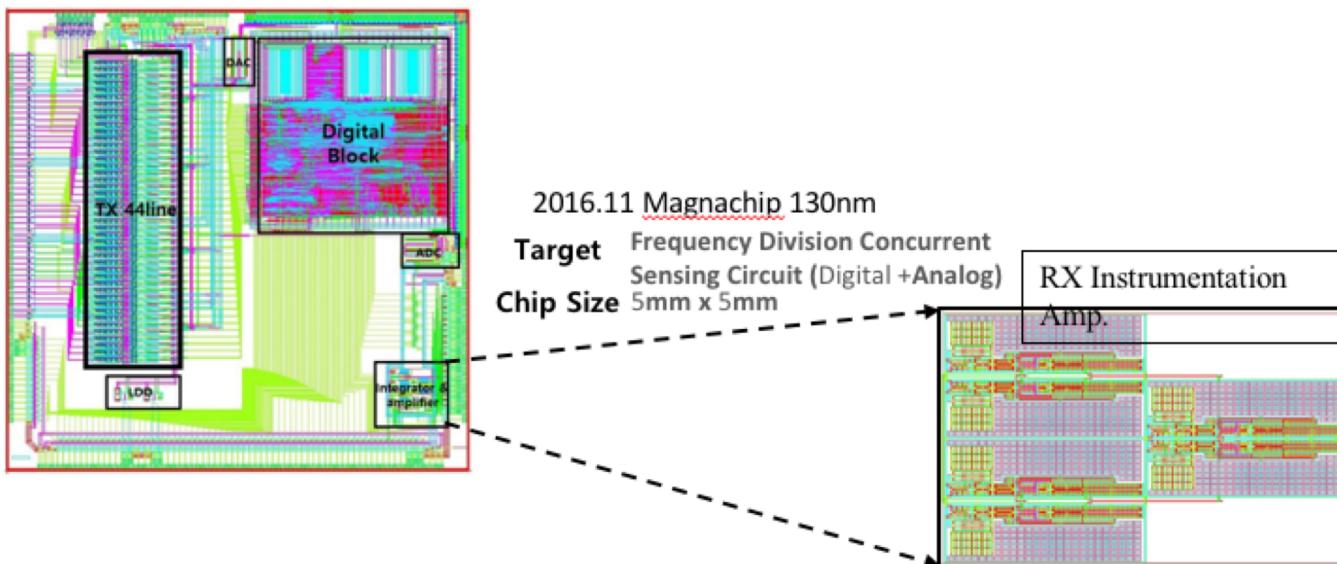
Target Large Touch screen Controller Chip

Chip Size 4mm x 4mm

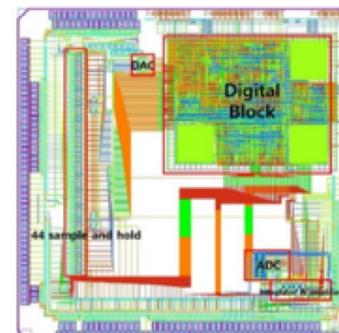
Gate Count 412,996

Touch Screen Controller Soc MPWs

❖ Latest MPWs



IDEC 2015.06 Samsung 65nm
Target Frequency Division Concurrent Sensing Circuit (Digital +Analog)
Chip Size 4mm x 4mm



IDEC 2016.02 Samsung 65nm
Target Frequency Division Concurrent Sensing Circuit (Digital +Analog)
Chip Size 4mm x 4mm