Outline

- Motivation and Prior Arts
- Proposed Receiver Architecture
- Circuit Implementation
- Measurement Results
- Conclusion

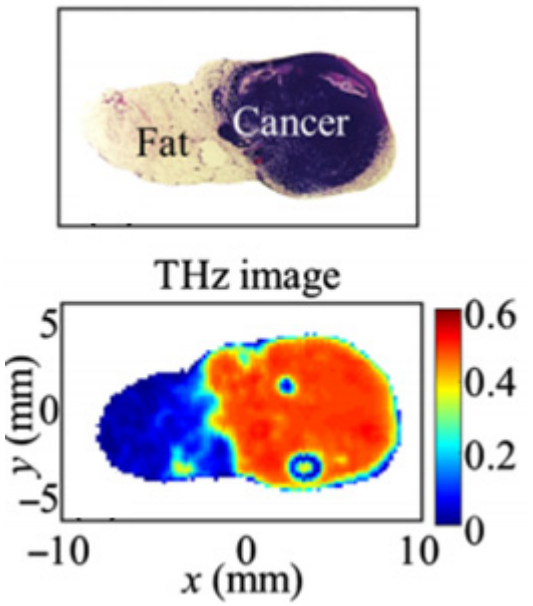
Outline

- Motivation and Prior Arts
- Proposed Receiver Architecture
- Circuit Implementation
- Measurement Results
- Conclusion

Motivation – 1

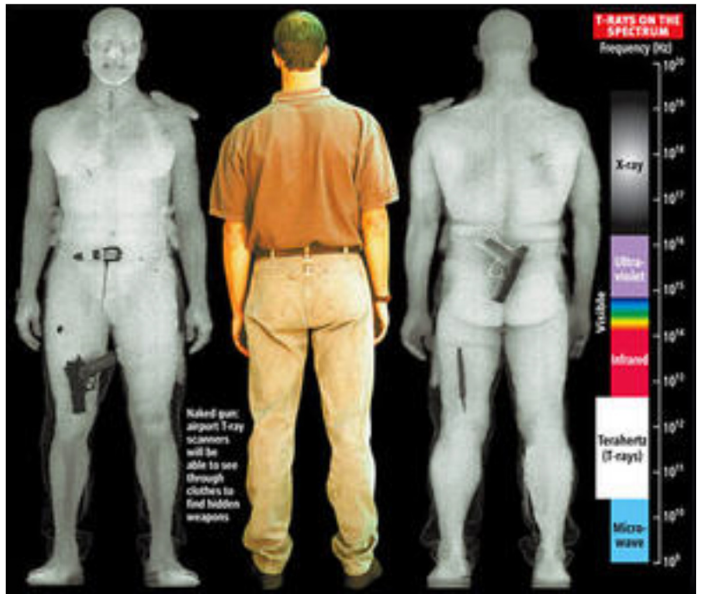
- Applications of THz imaging

Biomedical Diagnosis



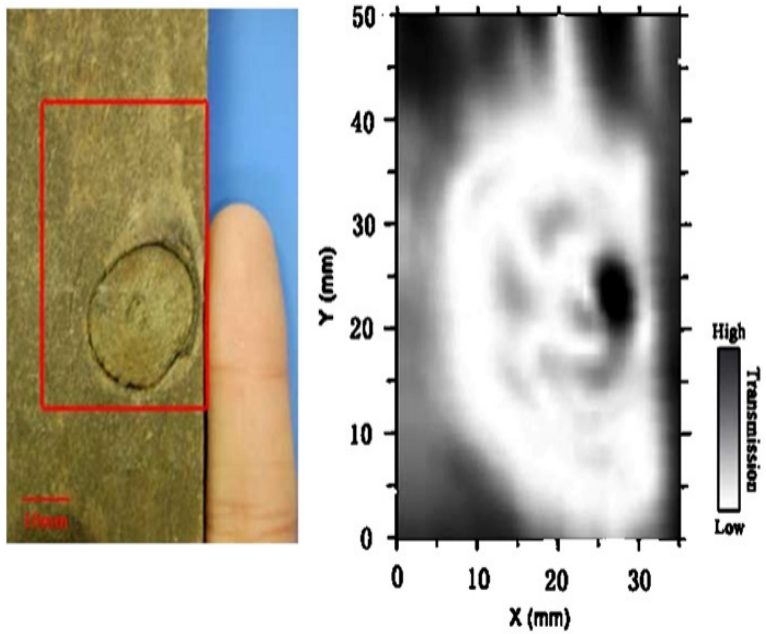
[T. Bowman, J. of Biomedical Optics., 2018]

Security



[K. Eaton, Fast Company., 2009]

Defect Inspection

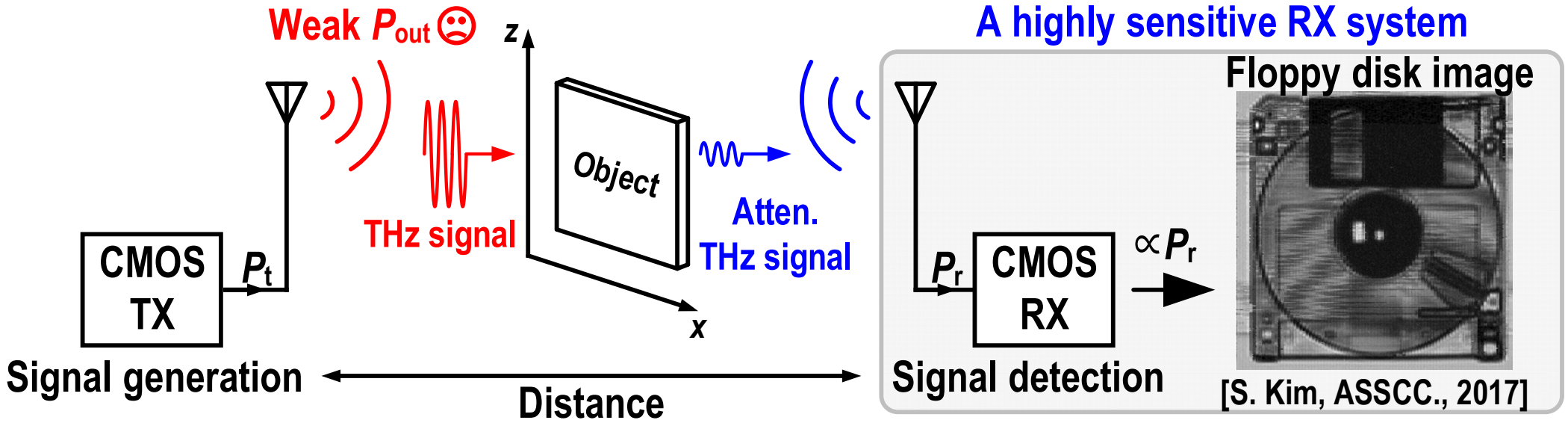


[Y. Oyama, NDT&E Int., 2009]

- CMOS THz imaging system
  - Solutions for **low-cost, high yield, and higher integration density**

Motivation – 2

- Typical imaging system

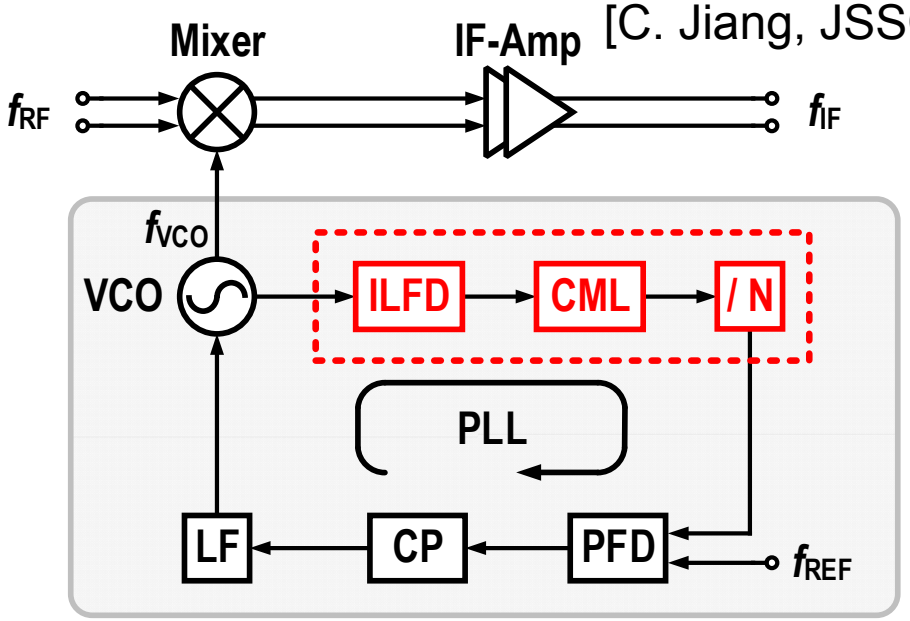


- Requirements for CMOS THz receiver
  - **High sensitivity** for high quality image (∝ SNR) and/or long distance
  - **Low-power implementation** for portable applications
  - **High integration level** for low-cost and small form factors

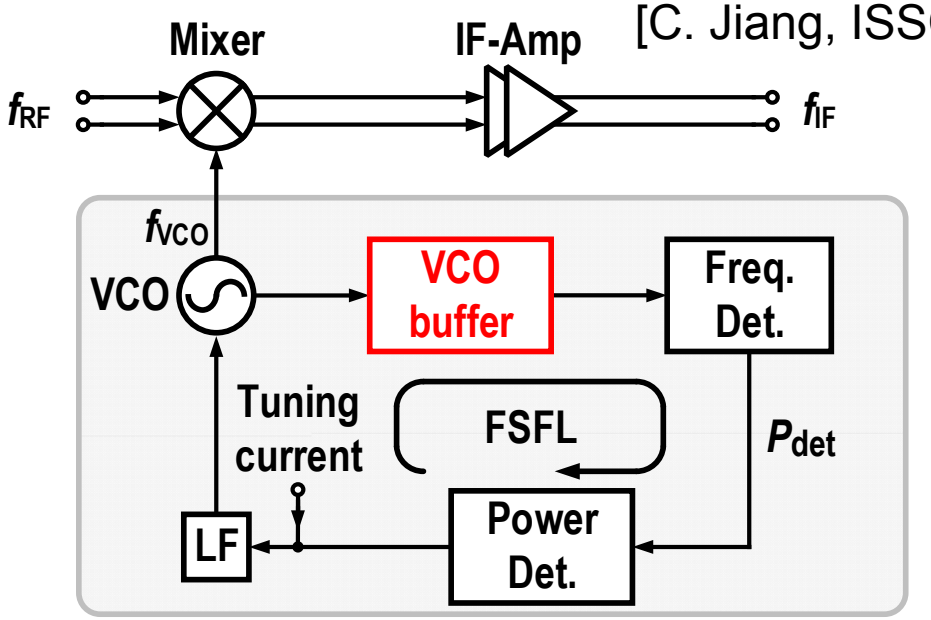
Prior Arts

- **Heterodyne RX** architecture
  - ☺ High Sensitivity
  - ☹ High power consumption for LO stabilization

Heterodyne RX with
Conventional PLL [C. Jiang, JSSC., 2016]



Heterodyne RX with
Frequency Stabilization Feedback Loop [C. Jiang, ISSCC., 2018]



Operating **divider chain** or **VCO buffer** @ f_{VCO}.

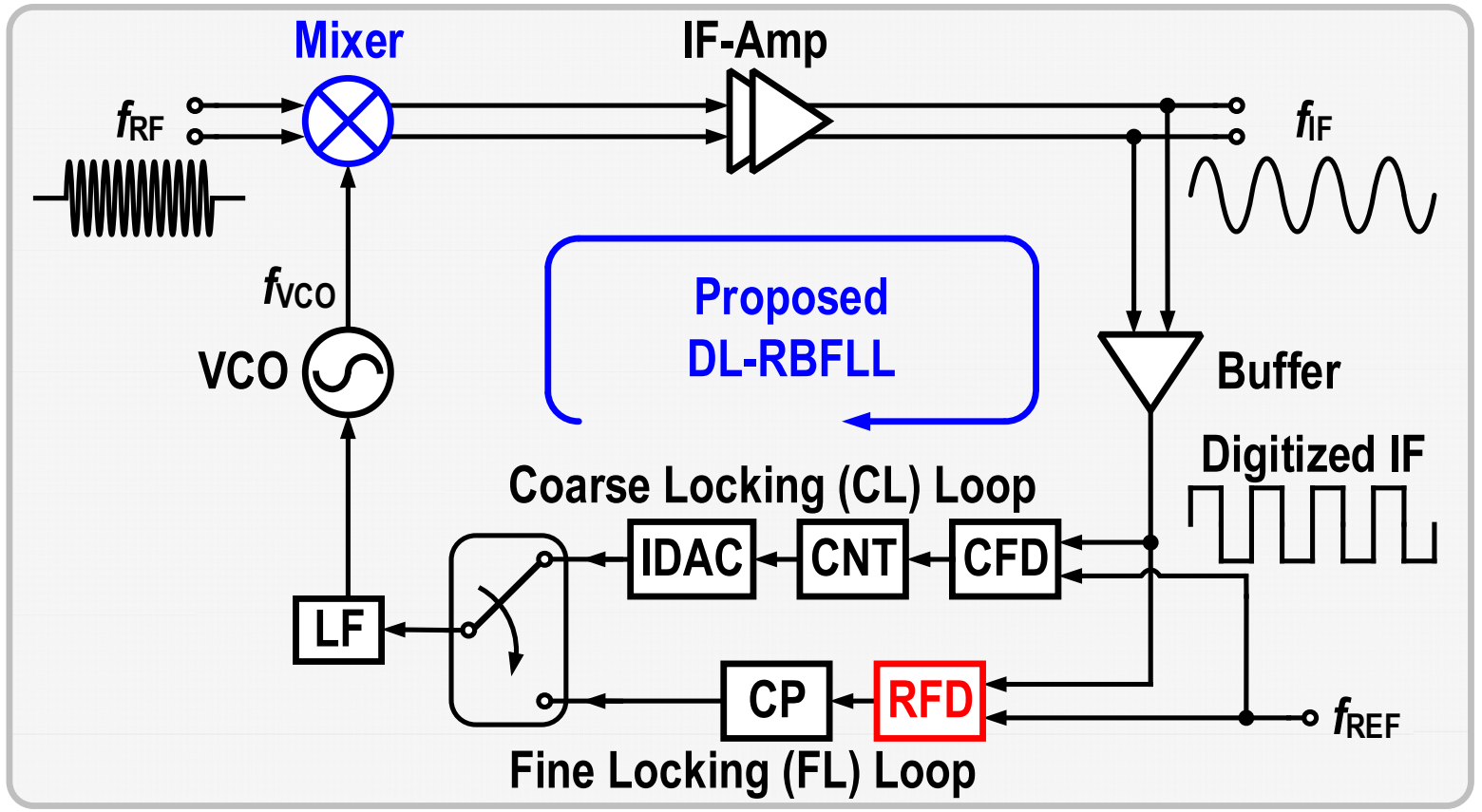
☹ High power/area consumption ☹ High design difficulty

Outline

- Motivation and Prior Arts
- Proposed Receiver Architecture
- Circuit Implementation
- Measurement Results
- Conclusion

Proposed Receiver Architecture

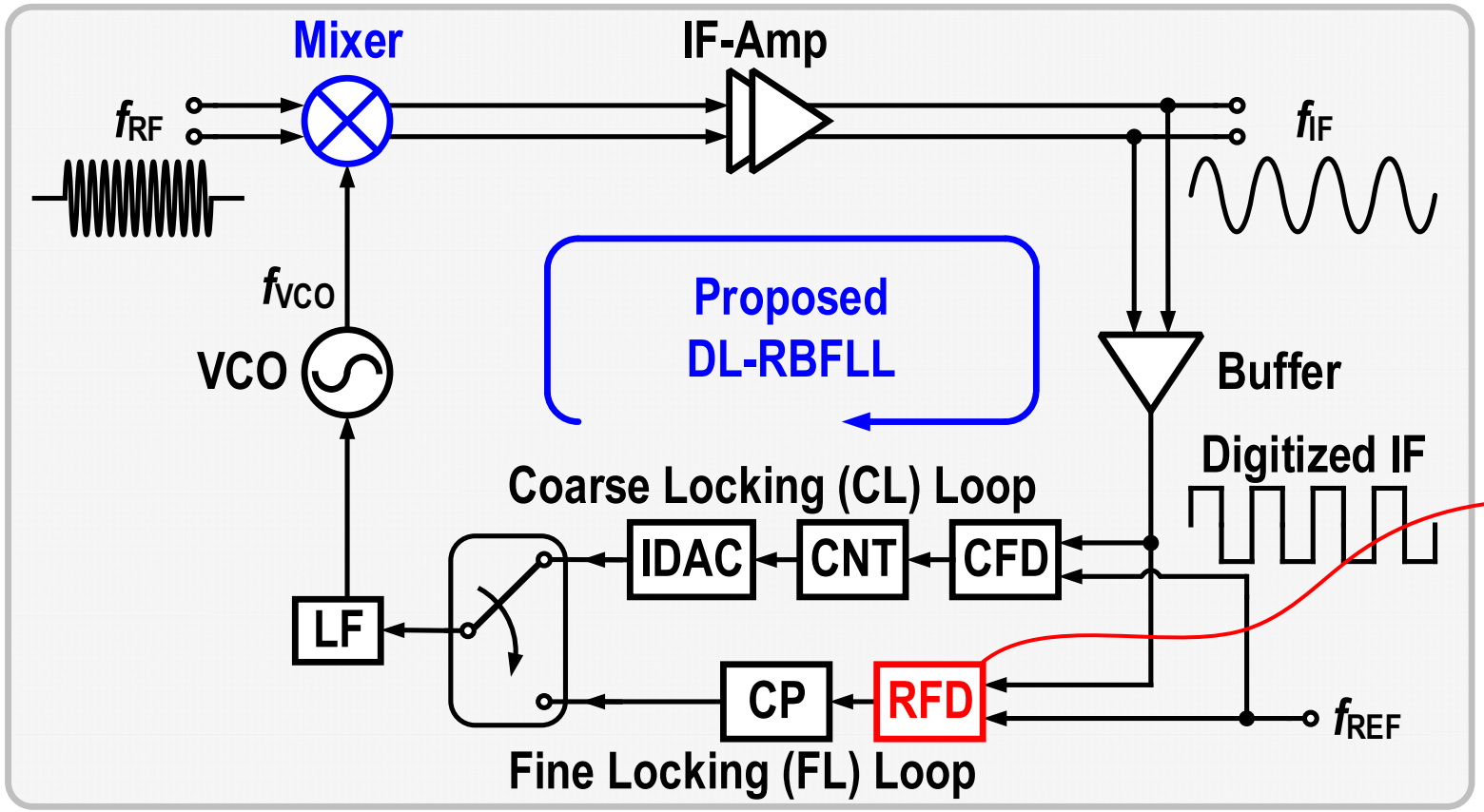
Proposed Dual-Locking Receiver-based FLL (DL-RBFLL)

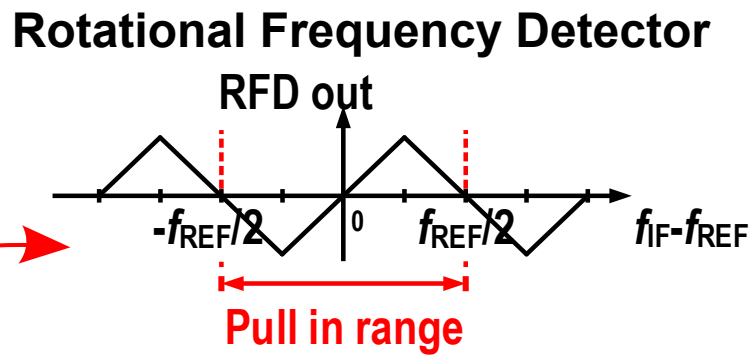


- **Eliminating divider chain & VCO buffer**
  - Low power/area consumption ☺
  - Low design difficulty ☺
- **Dual-locking loop implementation**
  - Widening acquisition range without increasing f_{REF} ☺

Proposed Receiver Architecture

Proposed Dual-Locking Receiver-based FLL (DL-RBFLL)



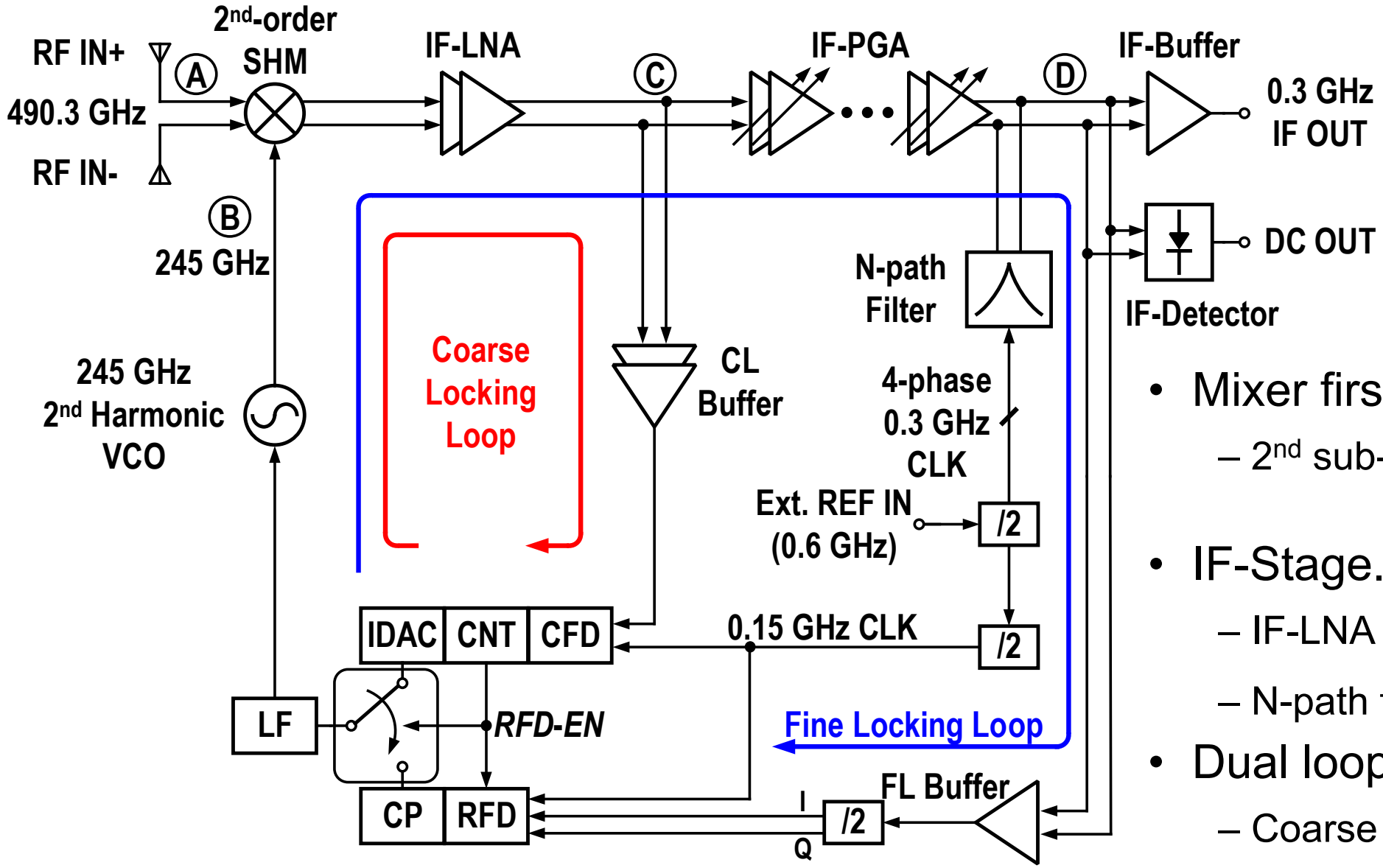


☹ **Limited pull in range**
($-0.5f_{REF} < f_{IF} < 0.5f_{REF}$)
[L. Jae-Seung, ISSCC., 2015]

- **Eliminating divider chain & VCO buffer**
  - Low power/area consumption ☺
  - Low design difficulty ☺

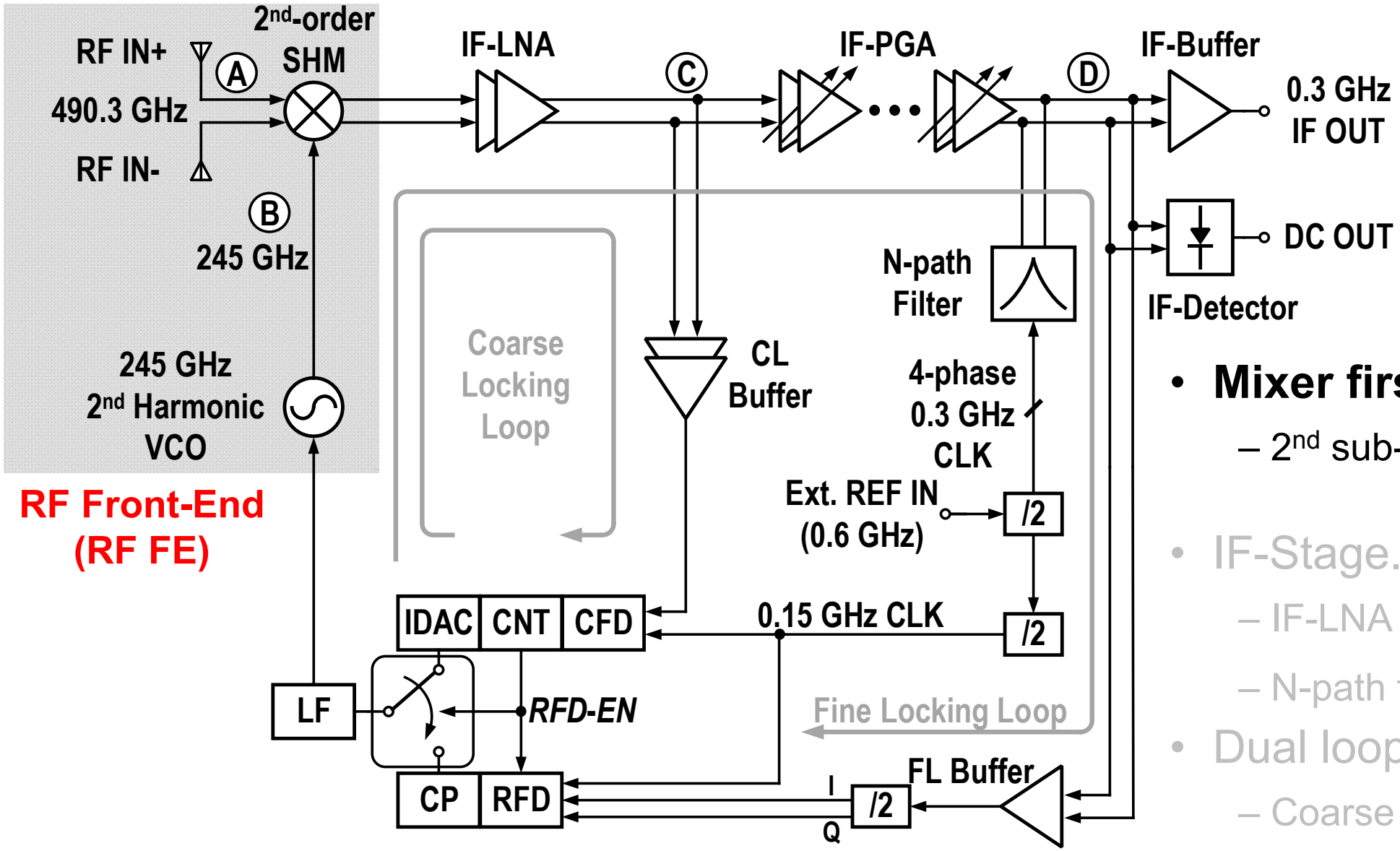
- **Dual-locking loop implementation**
  - Widening acquisition range without increasing f_{REF} ☺

Block Diagram of Proposed Receiver



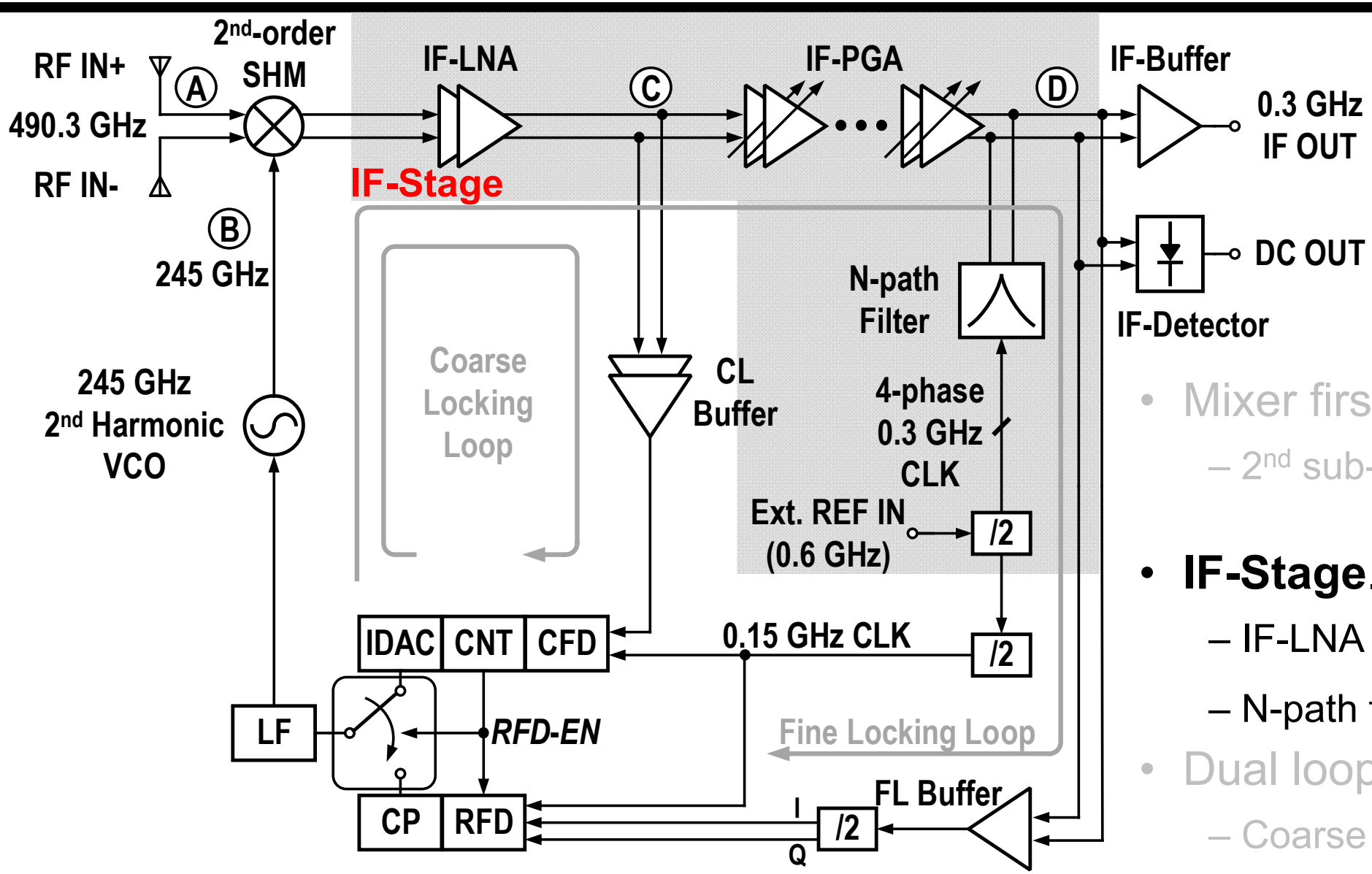
- Mixer first architecture.
  - 2nd sub-harmonic mixing ($f_{IF}=f_{RF}-2*f_{LO}$)
- IF-Stage.
  - IF-LNA / 10-stage IF-PGA
  - N-path filter
- Dual loop implementation.
  - Coarse / fine locking loop

Block Diagram of Proposed Receiver



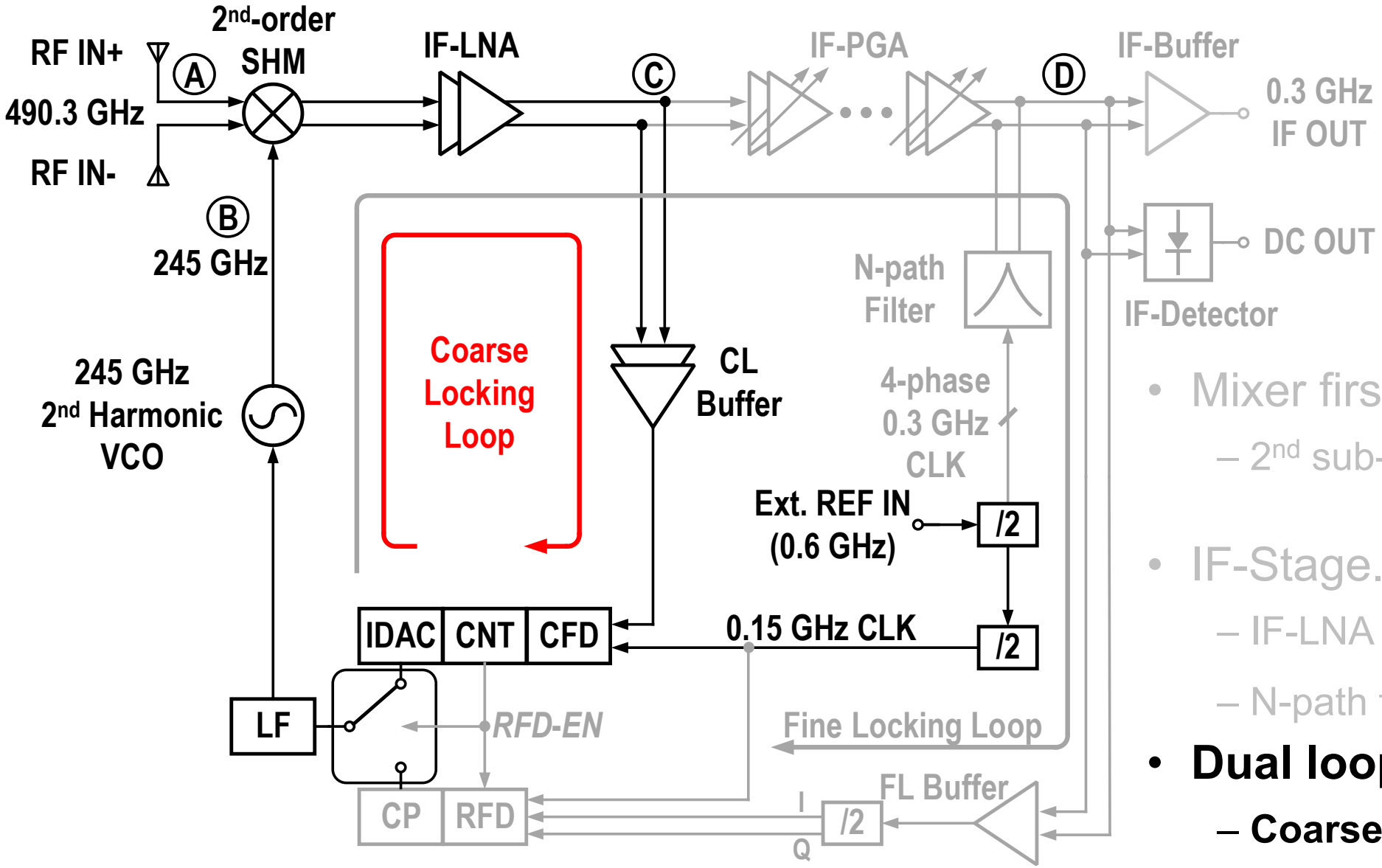
- **Mixer first** architecture.
  - 2nd sub-harmonic mixing ($f_{IF}=f_{RF}-2*f_{LO}$)
- IF-Stage.
  - IF-LNA / 10-stage IF-PGA
  - N-path filter
- Dual loop implementation.
  - Coarse / fine locking loop

Block Diagram of Proposed Receiver



- Mixer first architecture.
  - 2nd sub-harmonic mixing ($f_{IF}=f_{RF}-2*f_{LO}$)
- **IF-Stage**.
  - IF-LNA / 10-stage IF-PGA
  - N-path filter
- Dual loop implementation.
  - Coarse / fine locking loop

Block Diagram of Proposed Receiver – CL

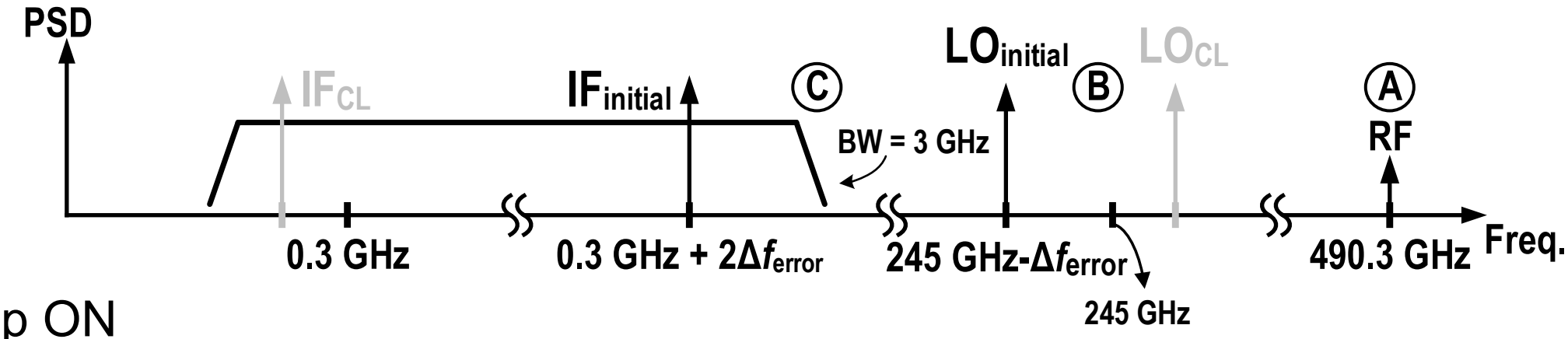


- Mixer first architecture.
  - 2nd sub-harmonic mixing ($f_{IF}=f_{RF}-2*f_{LO}$)
- IF-Stage.
  - IF-LNA / 10-stage IF-PGA
  - N-path filter
- **Dual loop** implementation.
  - **Coarse** / fine **locking loop**

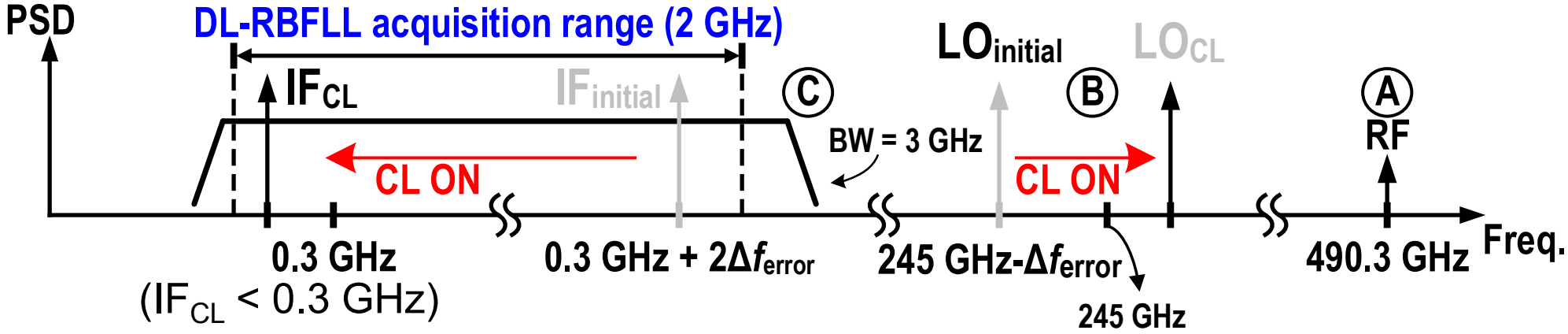
Frequency Plan – CL

f_{RF} = 490.3 GHz, Desired f_{LO} = 245 GHz, f_{IF} = f_{RF}-2*f_{LO} = 0.3 GHz

Initial

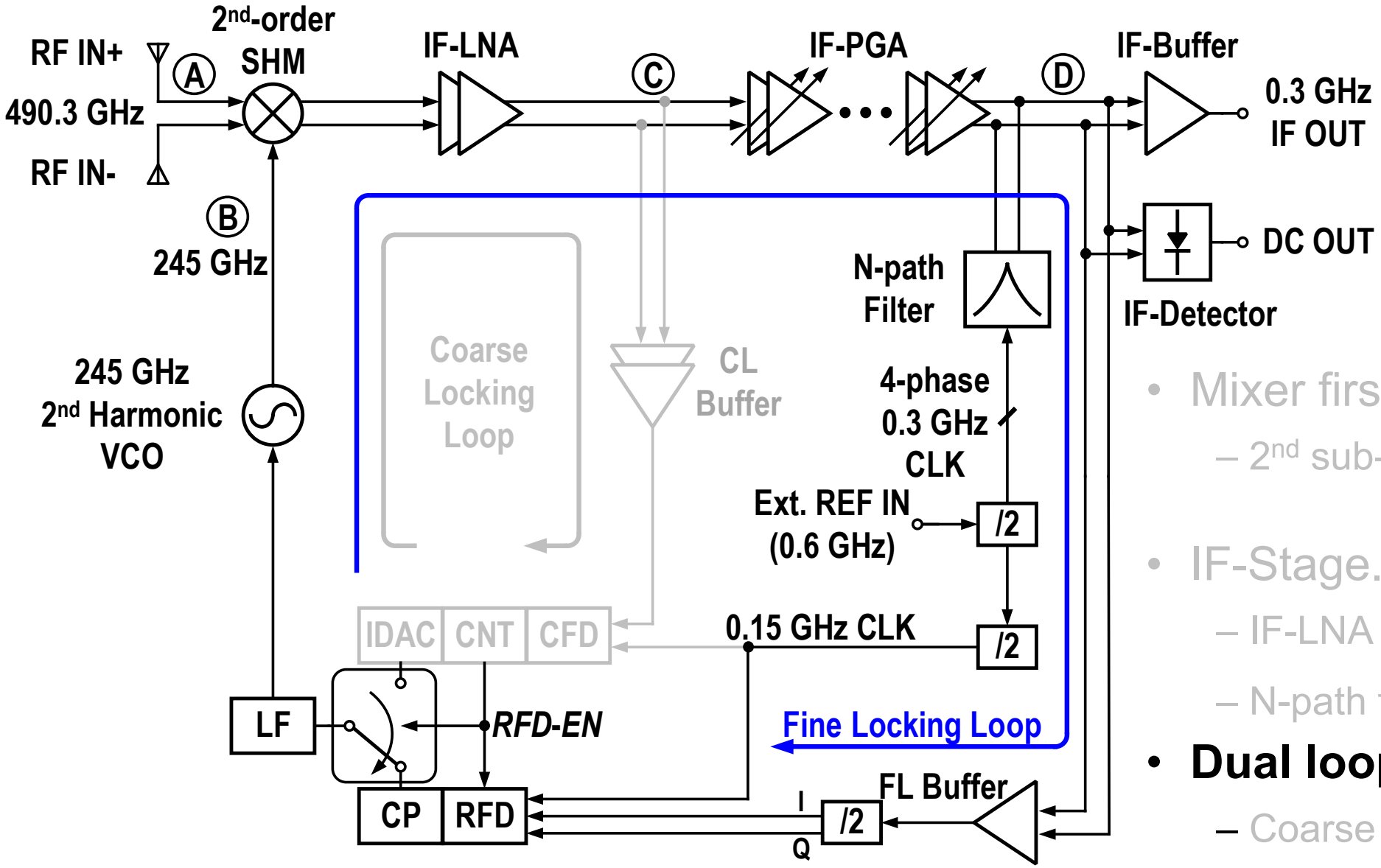


CL loop ON



Ⓐ RF IN Ⓑ VCO OUT Ⓒ IF-LNA OUT Ⓓ IF-PGA OUT

Block Diagram of Proposed Receiver – FL

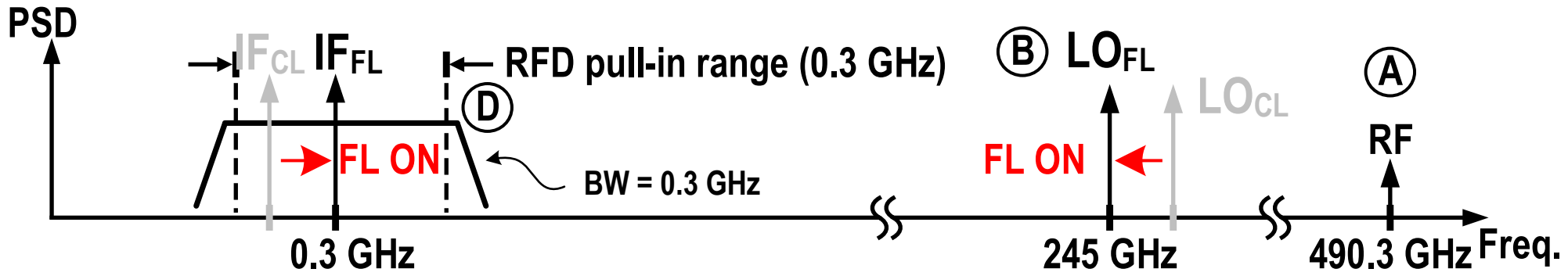


- Mixer first architecture.
  - 2nd sub-harmonic mixing ($f_{IF}=f_{RF}-2*f_{LO}$)
- IF-Stage.
  - IF-LNA / 10-stage IF-PGA
  - N-path filter
- **Dual loop** implementation.
  - Coarse / **fine locking loop**

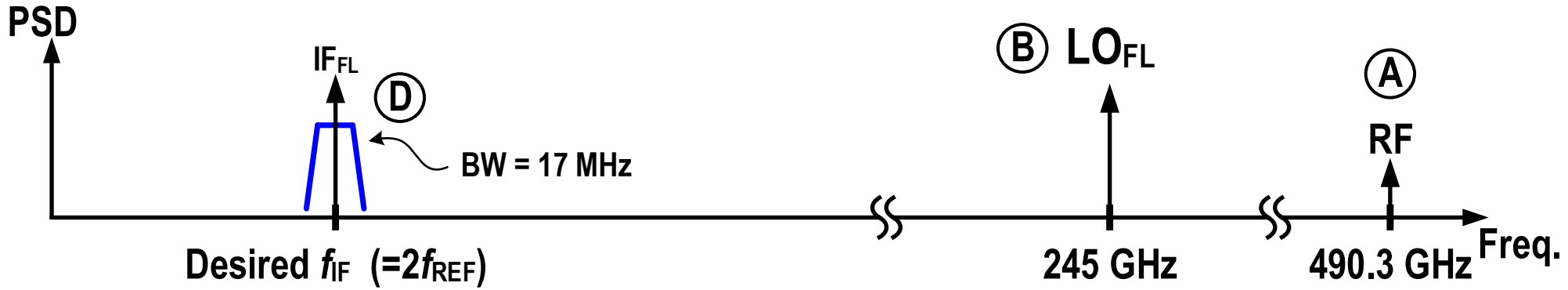
Frequency Plan – FL

f_{RF} = 490.3 GHz, Desired f_{LO} = 245 GHz, f_{IF} = f_{RF}-2*f_{LO} = 0.3 GHz

FL loop ON



N-path filter ON



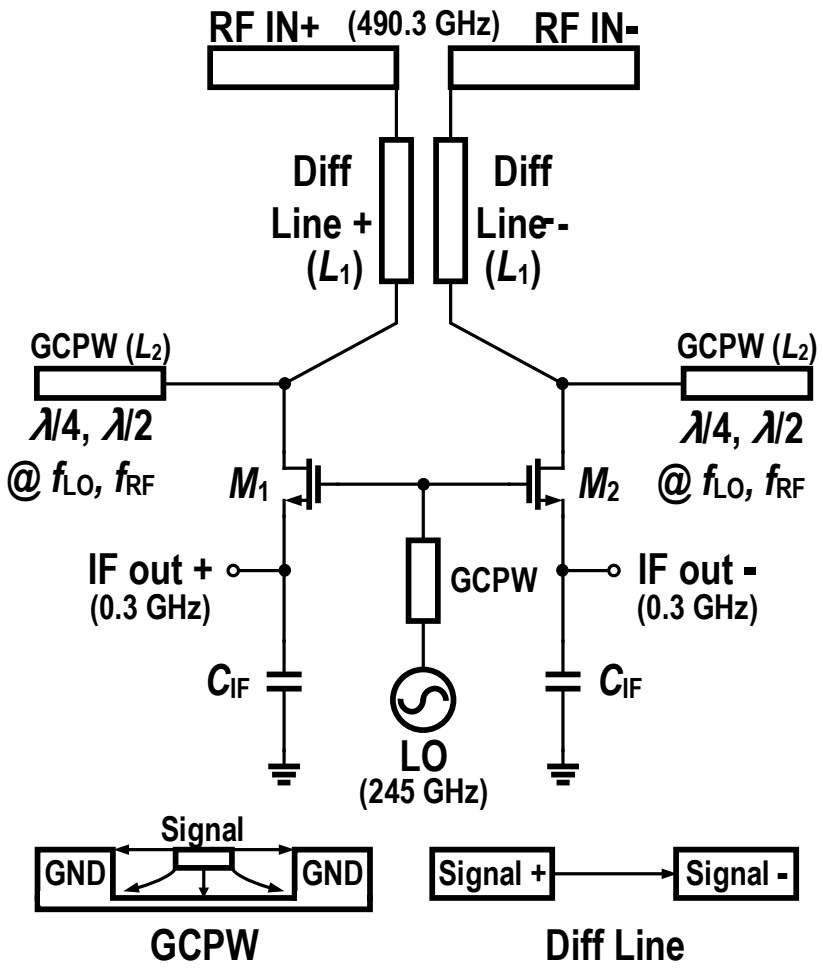
Ⓐ RF IN Ⓑ VCO OUT Ⓒ IF-LNA OUT Ⓓ IF-PGA OUT

Outline

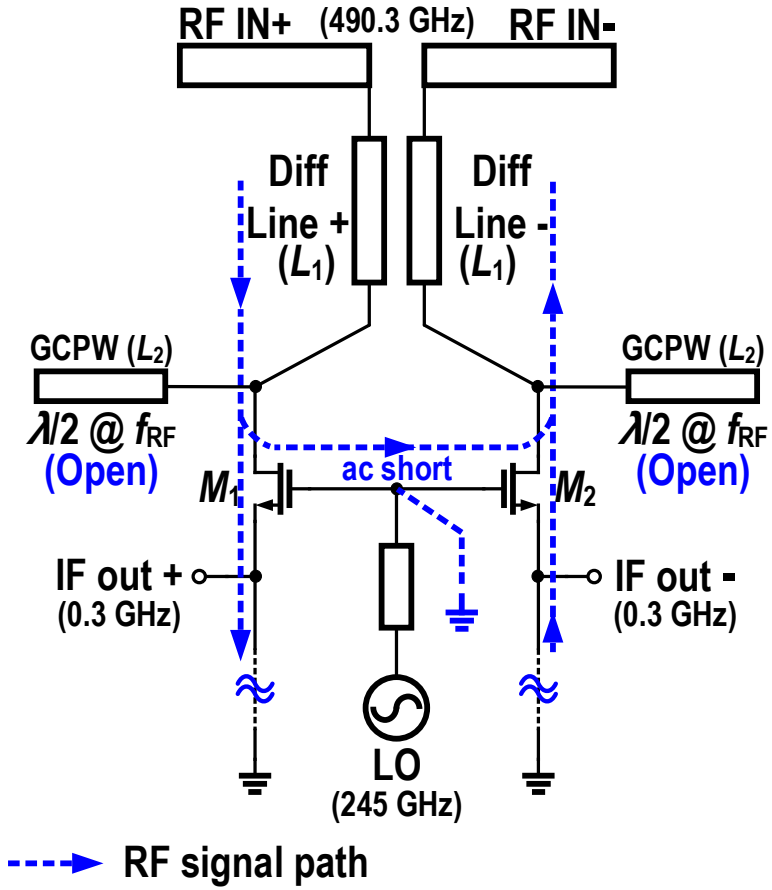
- Motivation and Prior Arts
- Proposed Receiver Architecture
- Circuit Implementation
- Measurement Results
- Conclusion

THz Receiver Front-End – Mixer

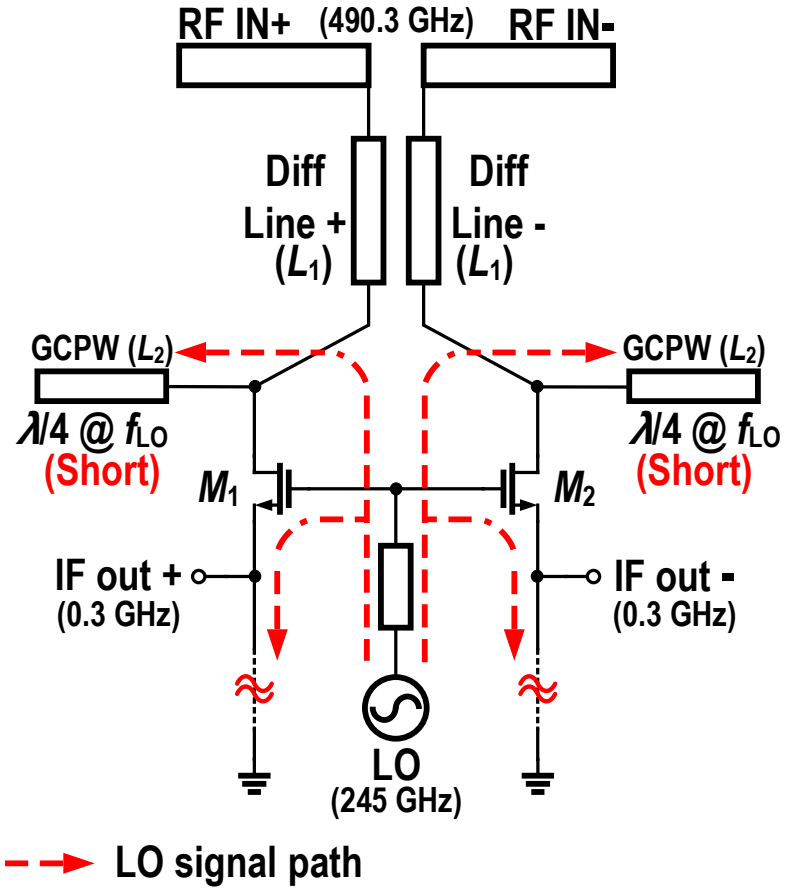
2nd-order sub-harmonic mixer (**SHM**) structure



Equivalent circuit for **RF**



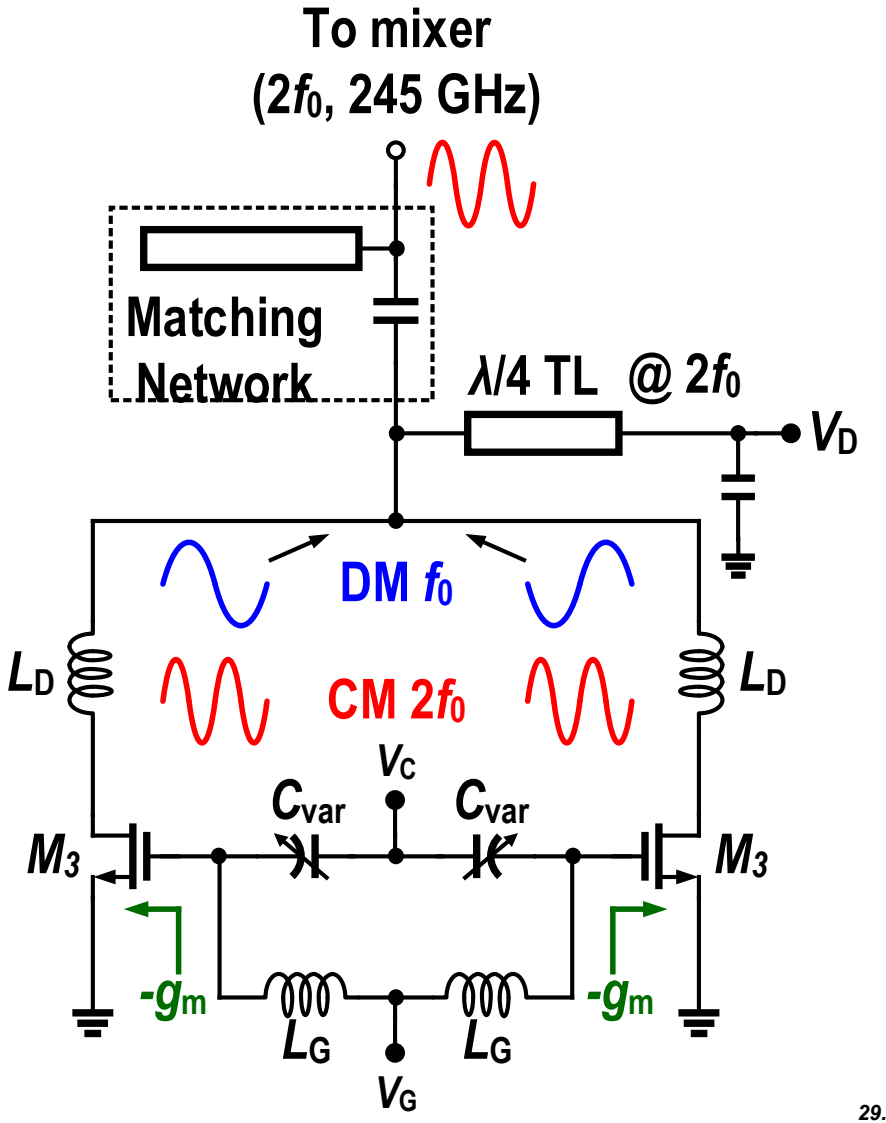
Equivalent circuit for **LO**



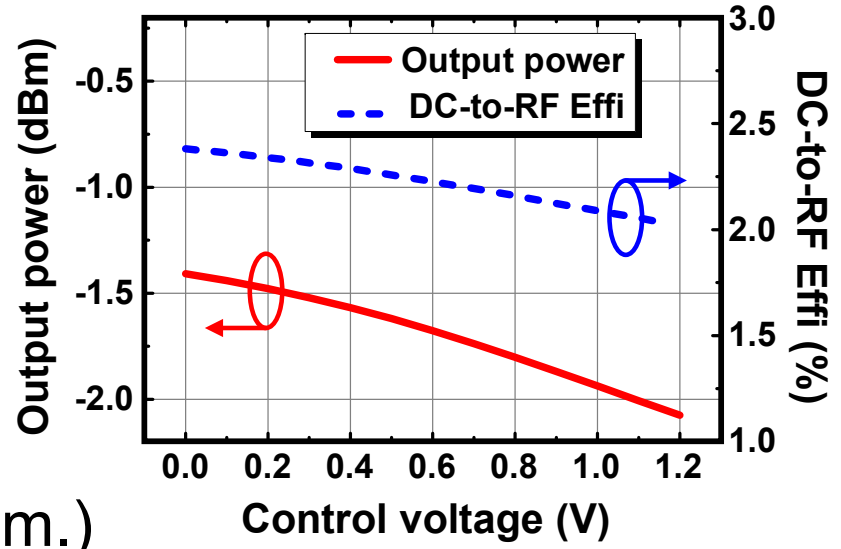
[K. Choi, IEEE MWCL., 2019]

THz Receiver Front-End – VCO

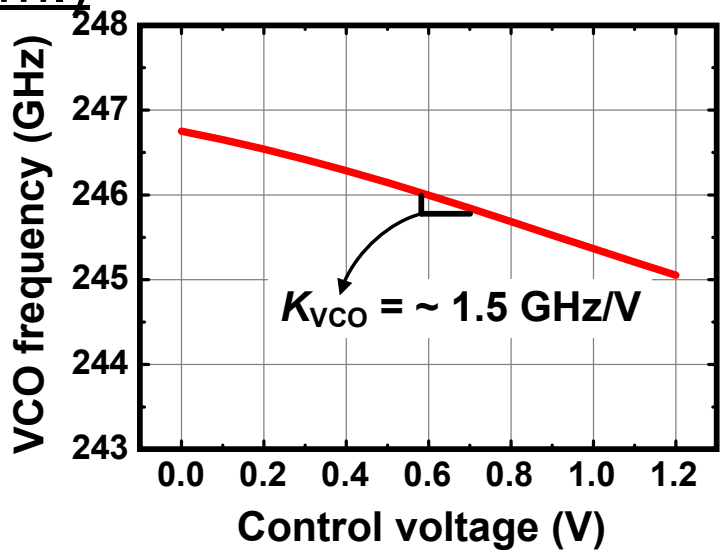
2nd-harmonic push-push VCO



Output power and DC-to-RF efficiency (Sim.)

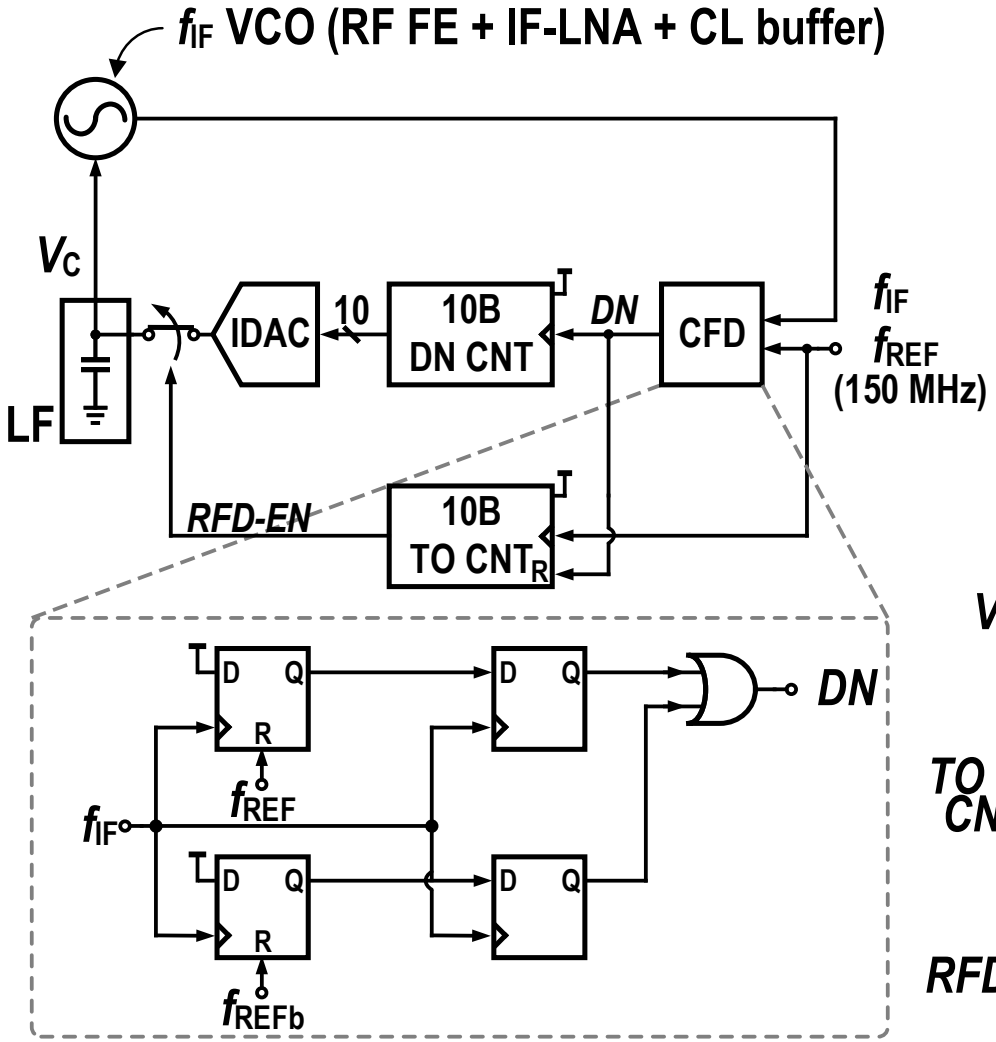


Kvco (Sim.)



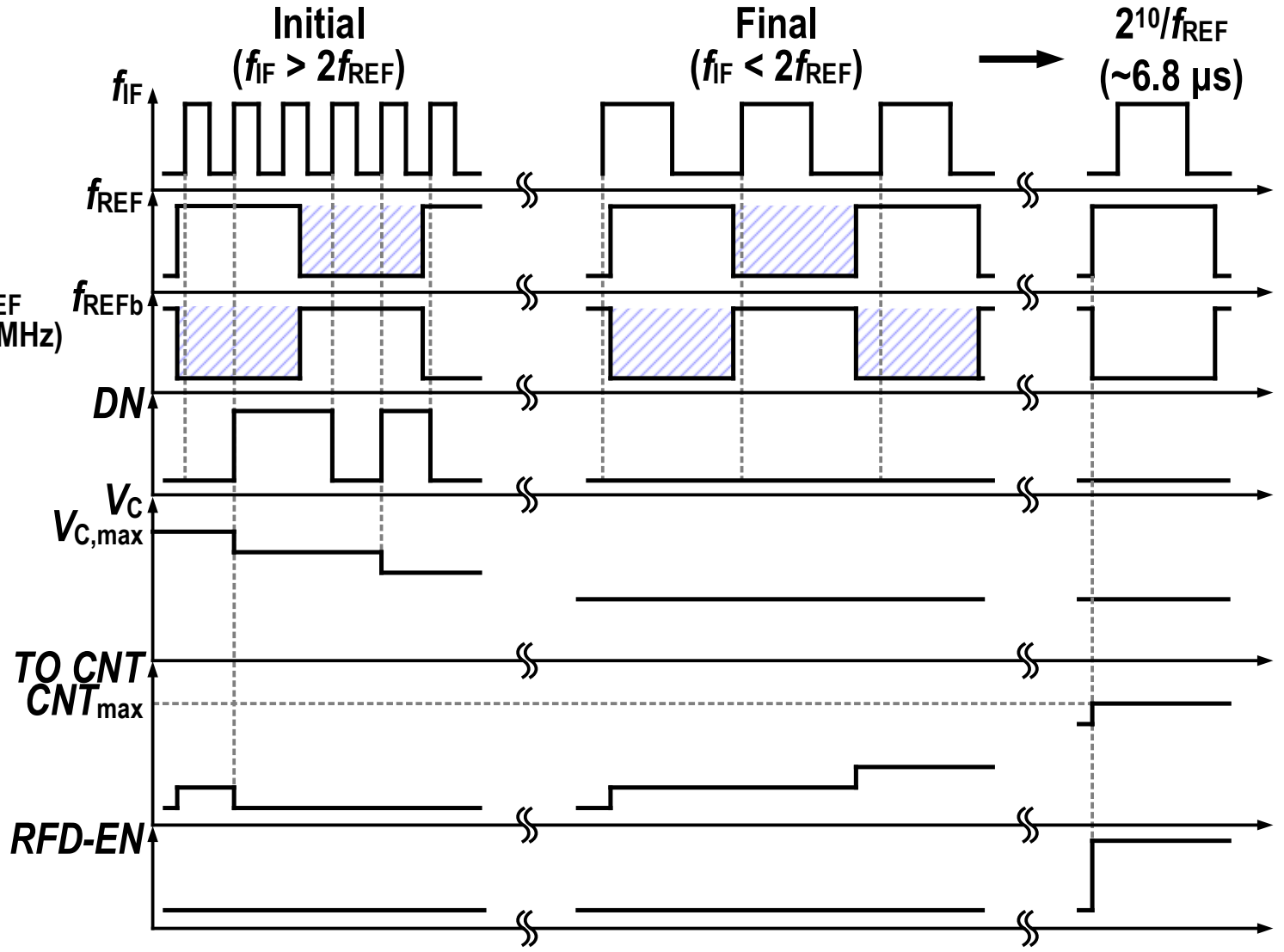
Coarse-Locking Loop

Block diagram of CL loop



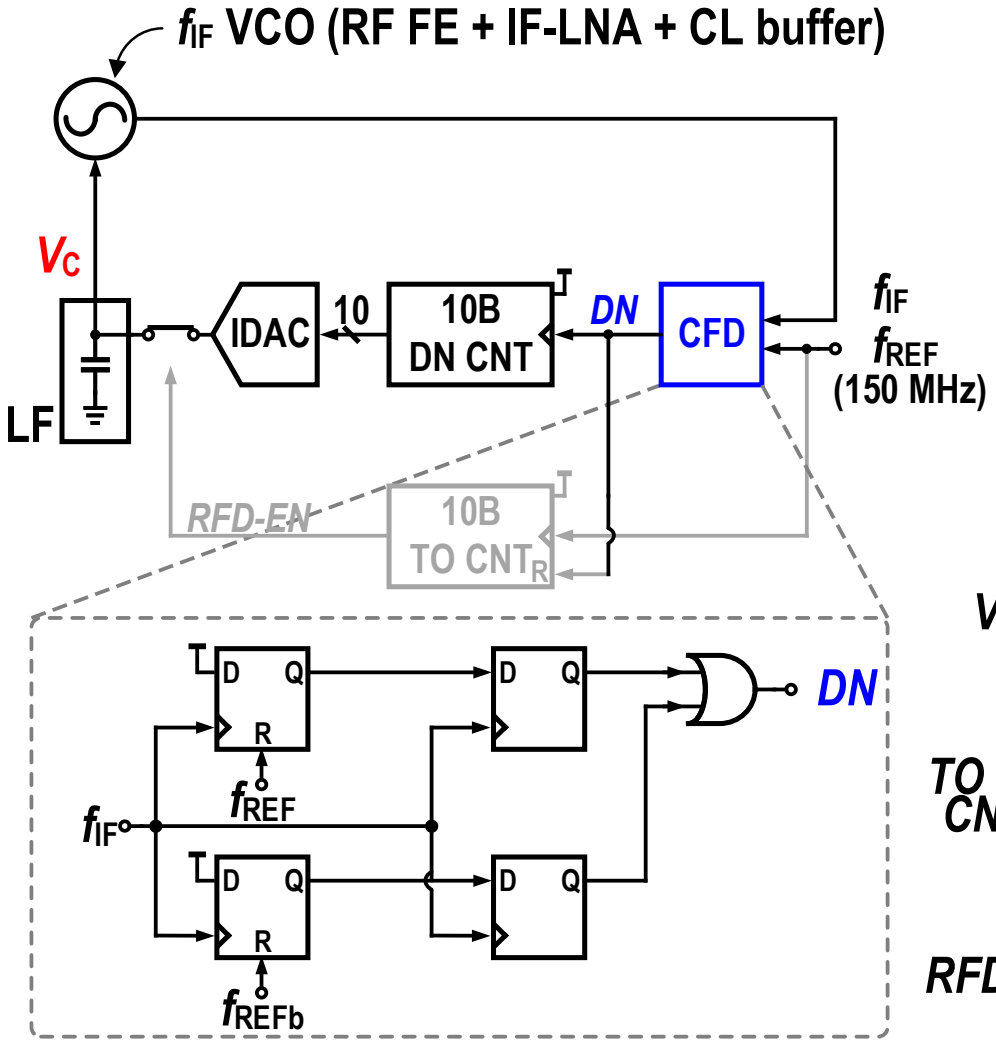
- $f_{IF} = f_{RF} - 2*f_{LO}$

Timing diagram of CL loop



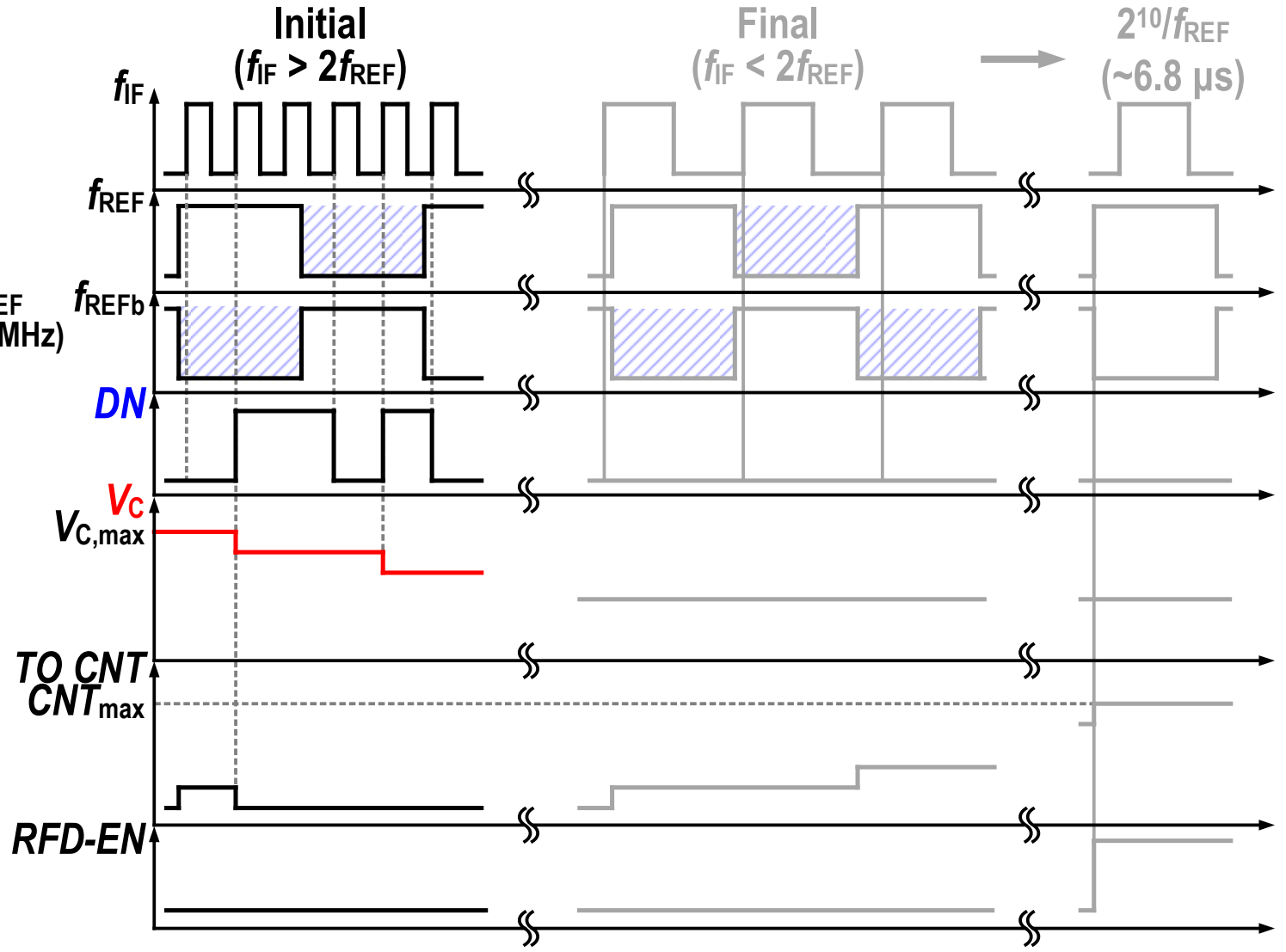
Coarse-Locking Loop

Block diagram of CL loop



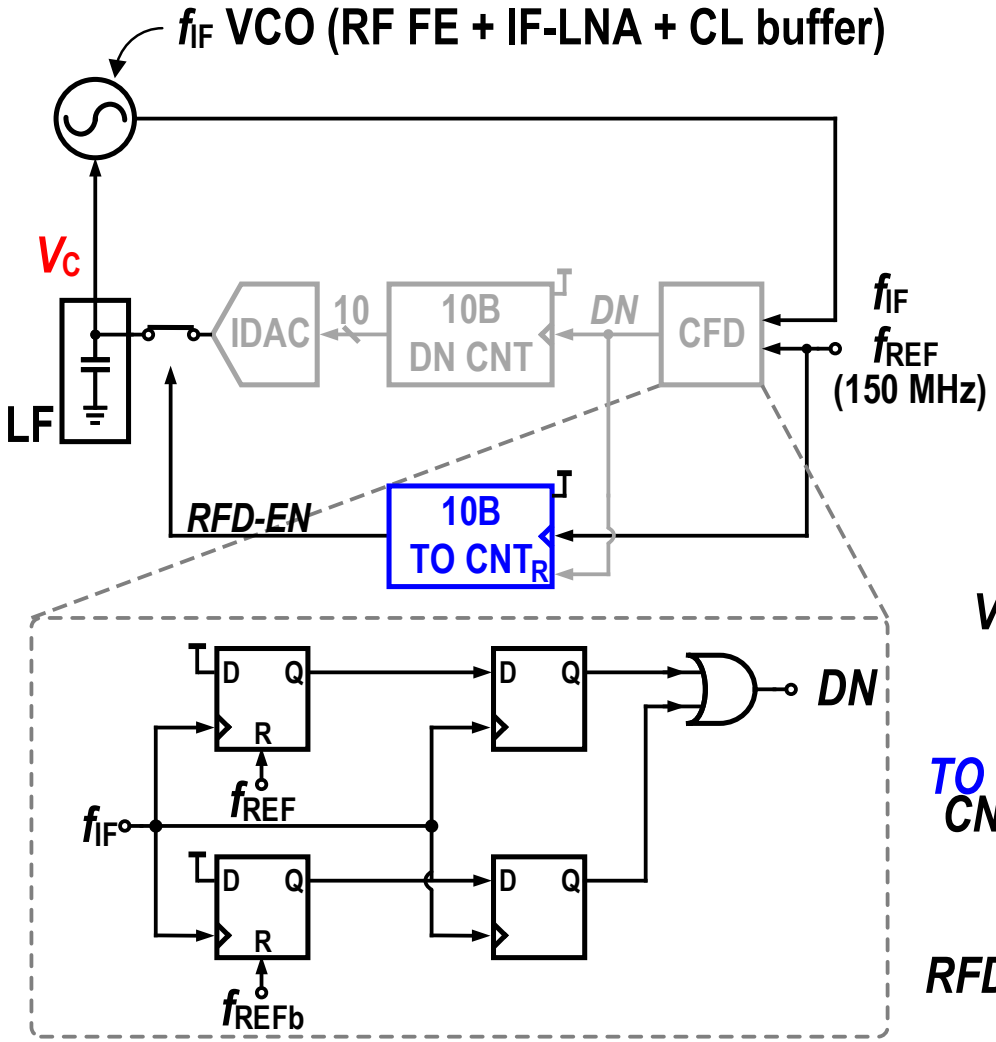
- $f_{IF} = f_{RF} - 2*f_{LO}$

Timing diagram of CL loop



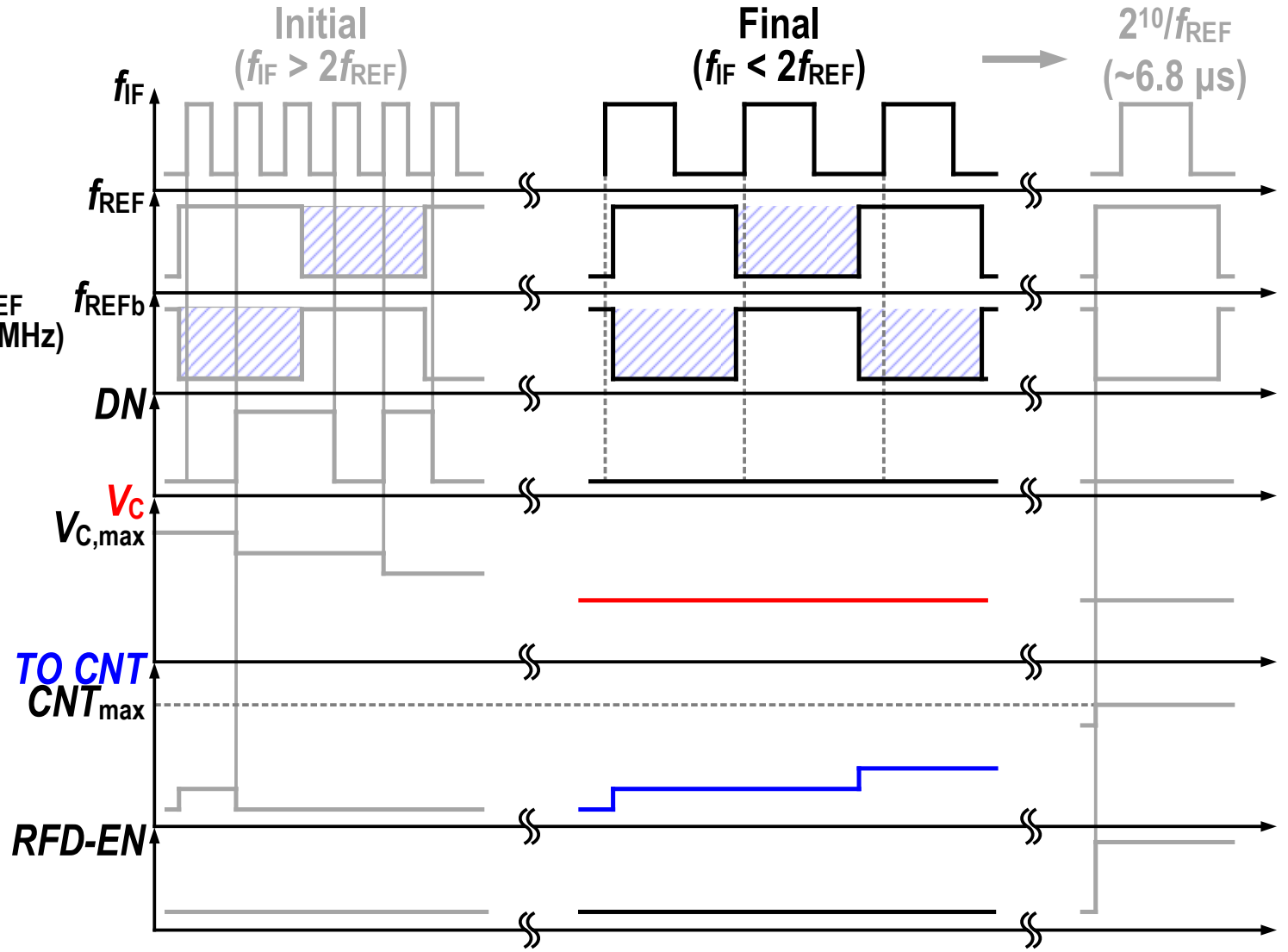
Coarse-Locking Loop

Block diagram of CL loop



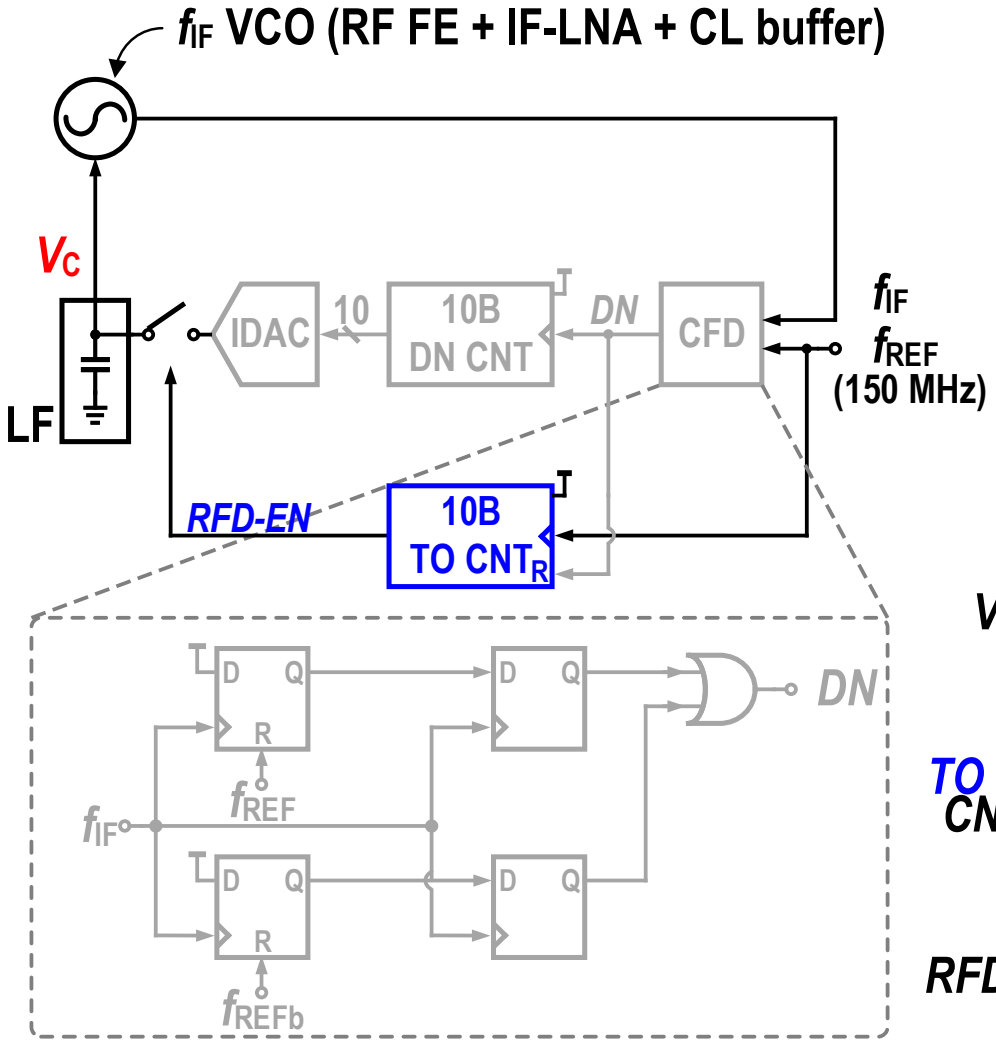
- $f_{IF} = f_{RF} - 2*f_{LO}$

Timing diagram of CL loop



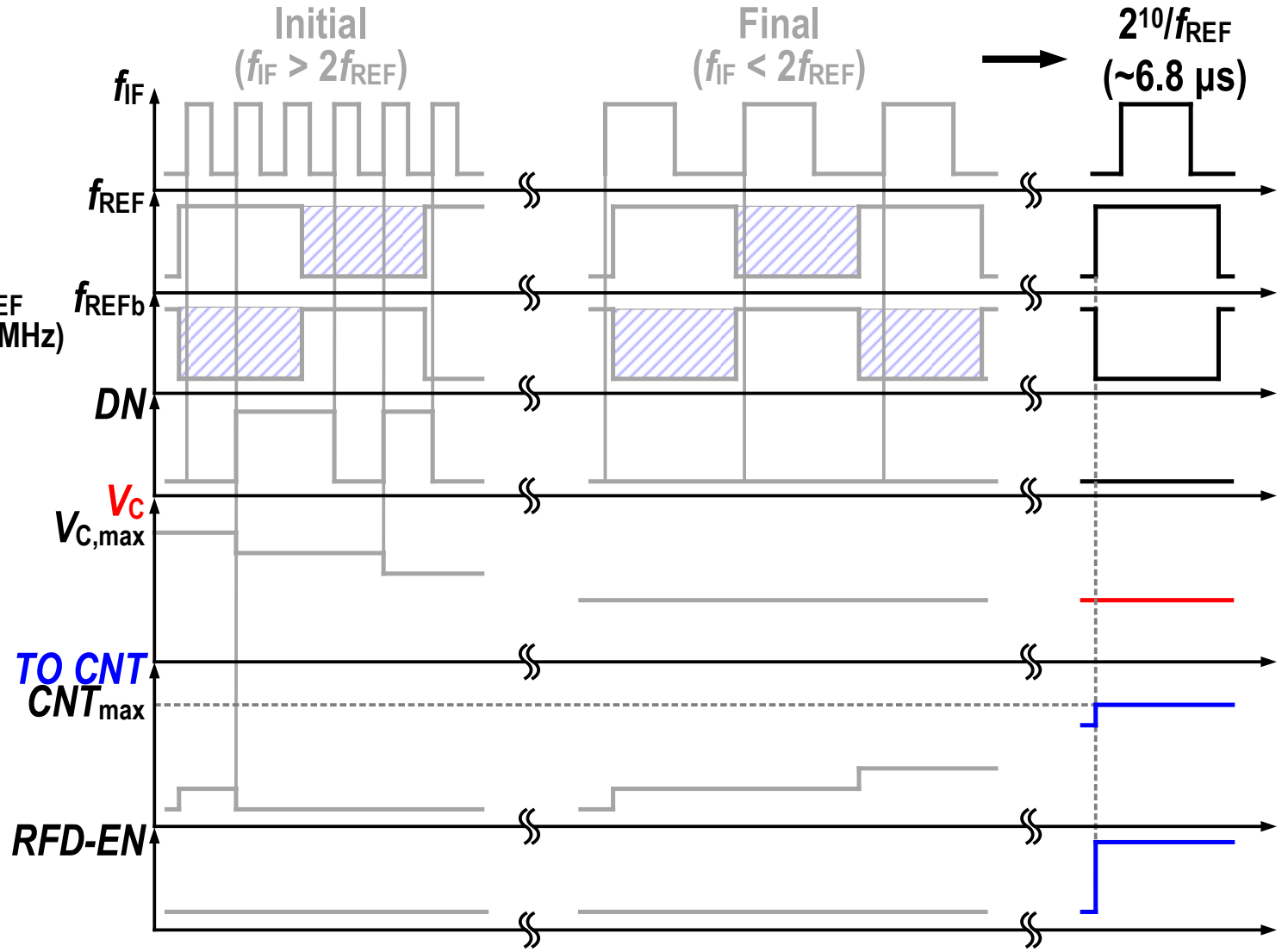
Coarse-Locking Loop

Block diagram of CL loop



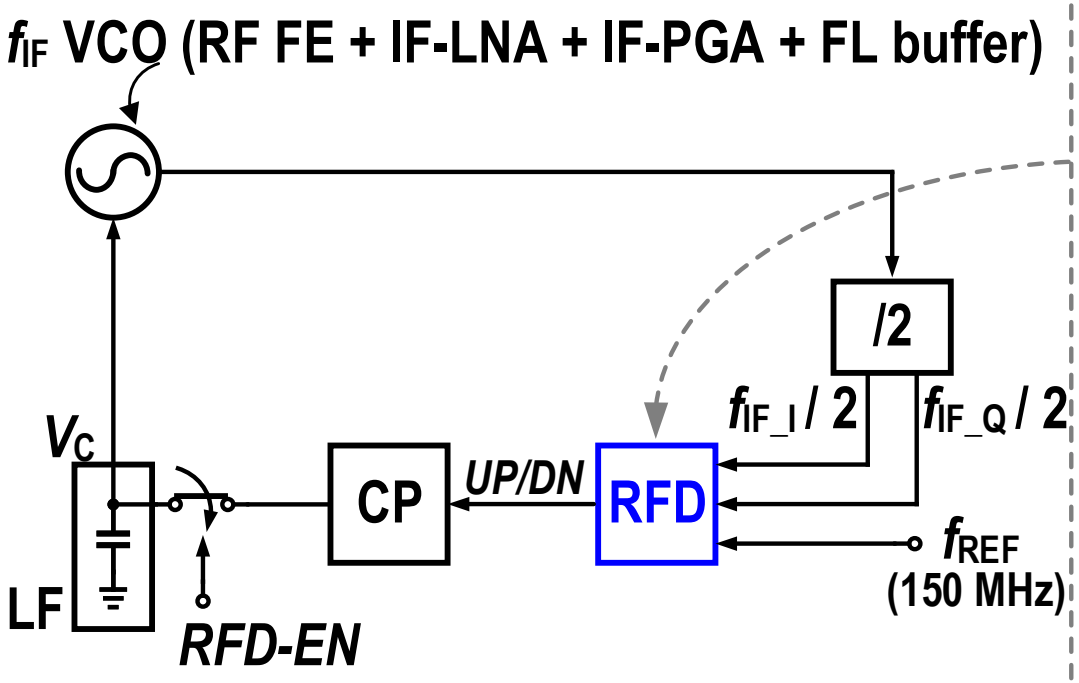
- $f_{IF} = f_{RF} - 2*f_{LO}$

Timing diagram of CL loop



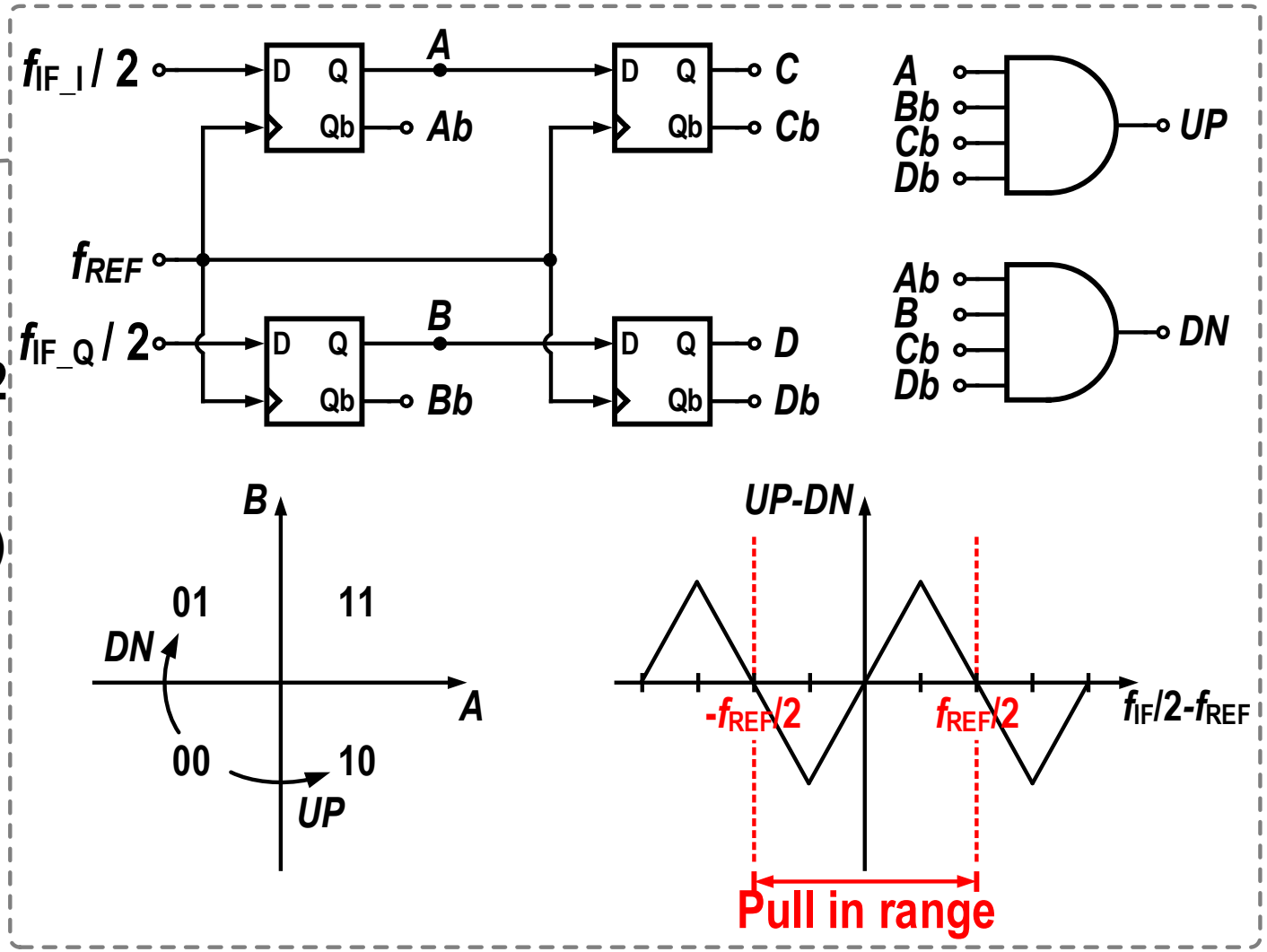
Fine-Locking Loop

Block diagram of FL loop [7]



- RFD operation
  - $f_{REF} < f_{IF}/2$: *UP*
  - $f_{REF} > f_{IF}/2$: *DN*
  - **Pull in range = ± 50%**
- $f_{IF} = f_{RF} - 2*f_{LO}$

Rotational frequency detector (RFD)

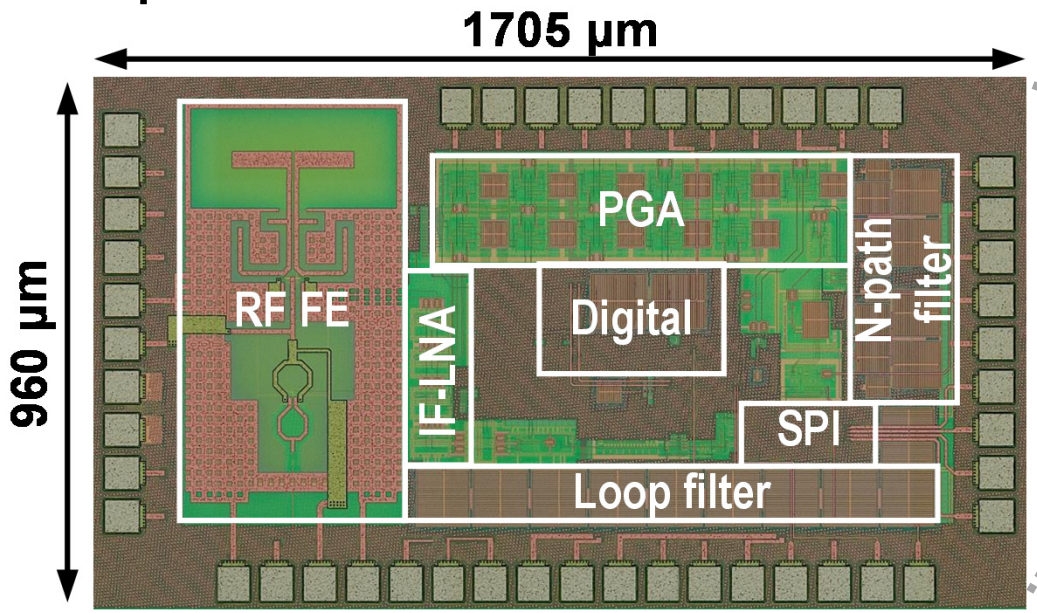


Outline

- Motivation and Prior Arts
- Proposed Receiver Architecture
- Circuit Implementation
- Measurement Results
- Conclusion

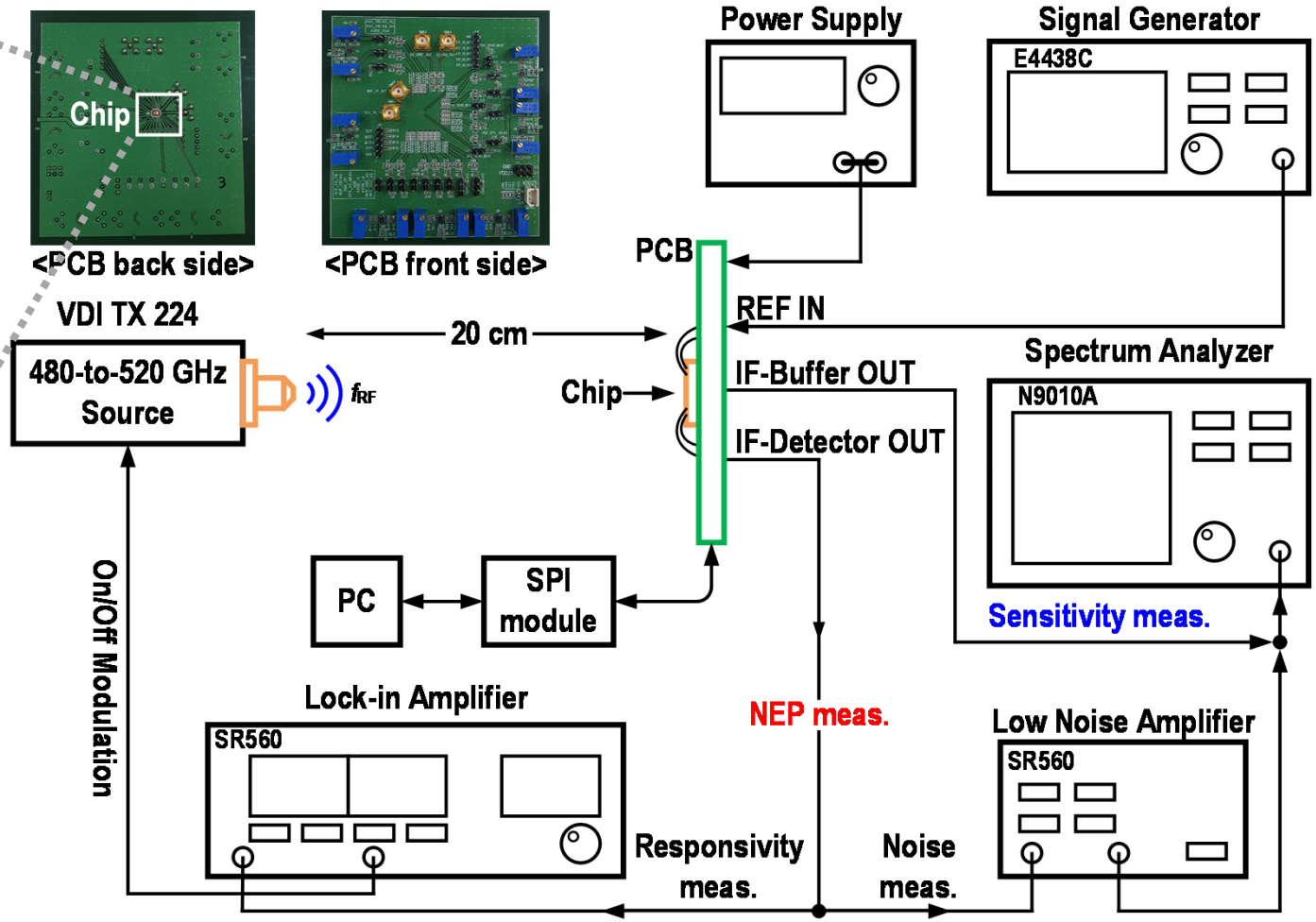
Chip Photo & Measurement Setup

Chip Photo



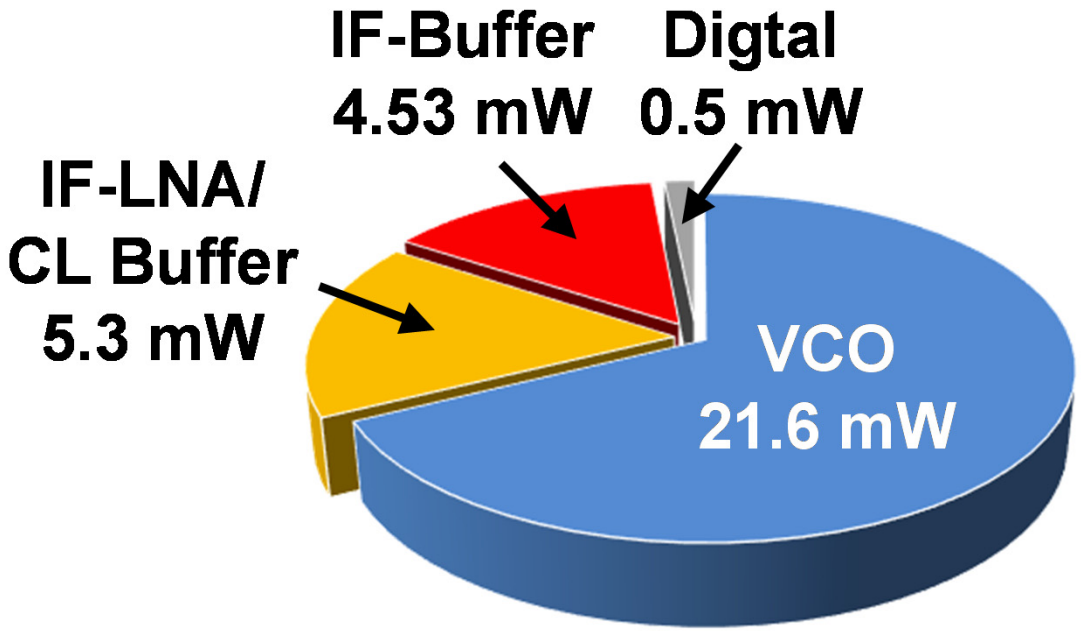
- TSMC 65nm CMOS process
- 1.2 V supply
- Chip size : 1705 × 960 µm²

Measurement setup



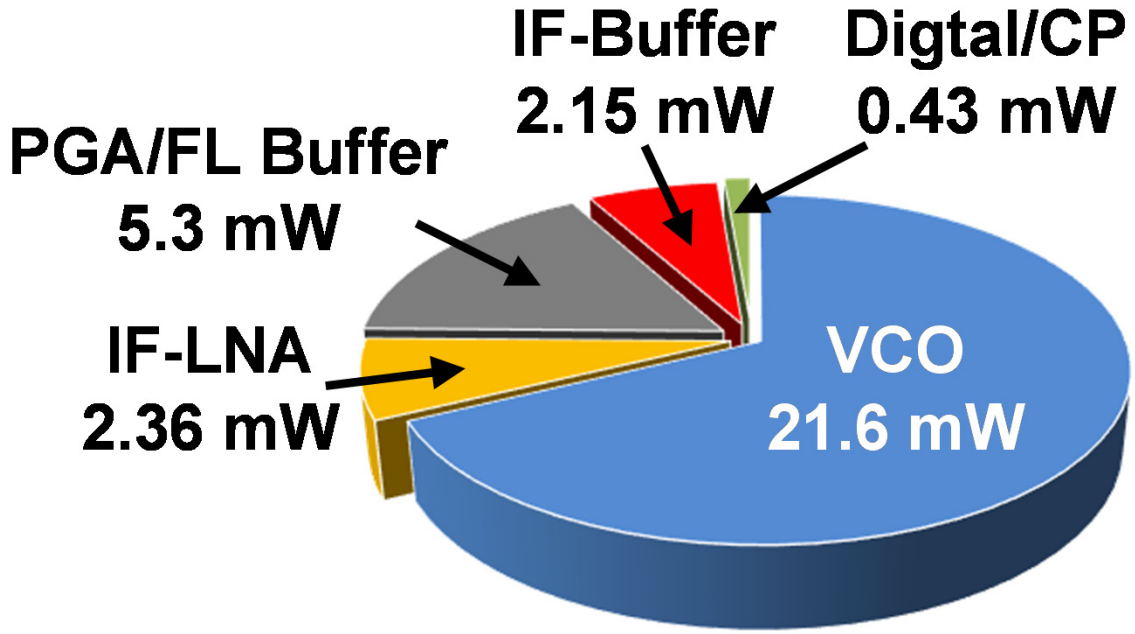
Power Breakdown

Coarse Locking Loop



Total P_{DC} = 31.9 mW

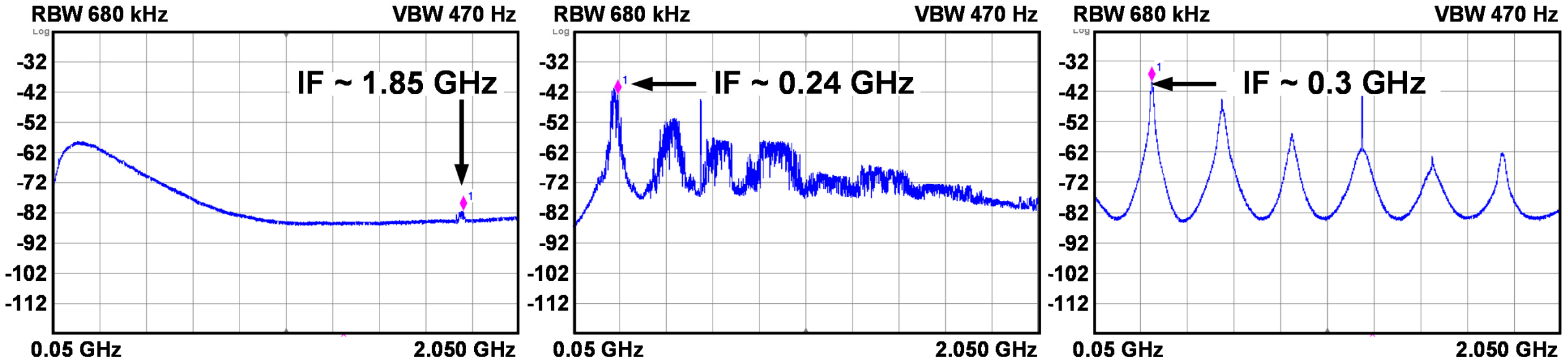
Fine Locking Loop



Total P_{DC} = 31.9 mW

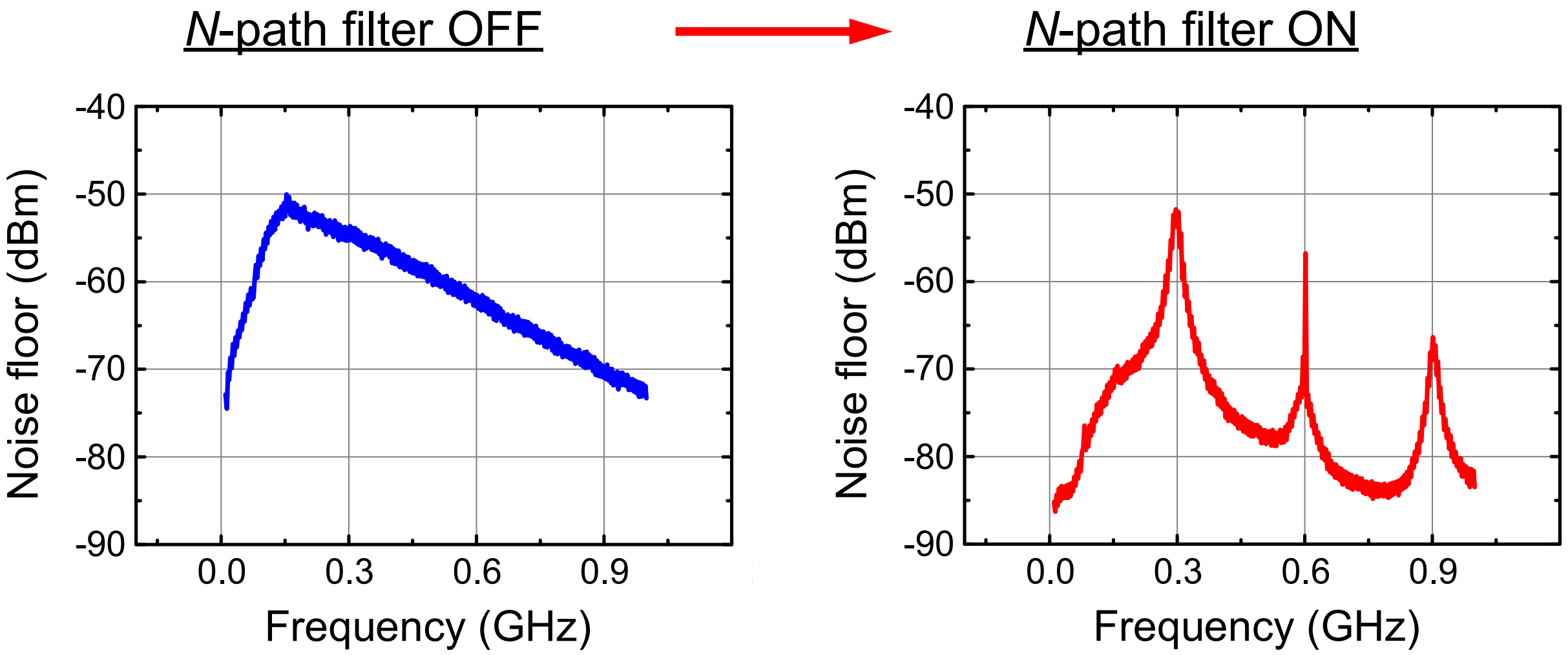
Measured Output Spectrum

Free-running LO → Coarse Locking ON → Fine Locking ON



- The spectrums are measured at the IF-Buffer output.
  - **Coarse** locking loop ON: **The IF frequency changes 1.85 → 0.24 GHz**
  - **Fine** locking loop ON: **The IF frequency changes 0.24 → 0.3 GHz**

Measured Noise Floor



- Noise bandwidth is reduced to 17 MHz when ***N*-path filter is ON**.

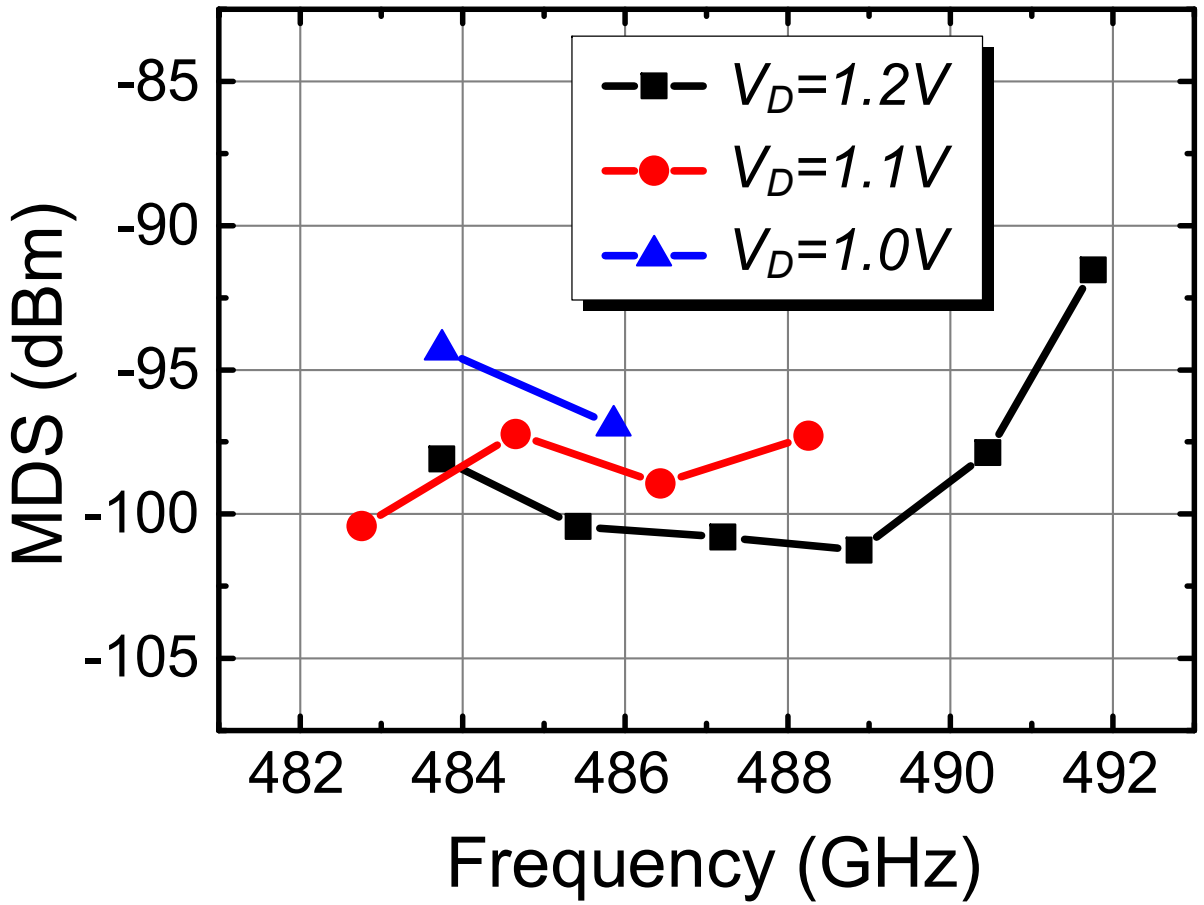
MDS/NEP Measurement Methods

- Minimum discernible (detectable) signal (MDS) for a 1 kHz noise BW.
  - **MDS [dBm] = – 174 [dBm/Hz] + NF [dB] + 10log(1 kHz).**
  - NF [dB] = 174 [dBm/Hz] – Conversion Gain [dB] – Output noise floor [dBm/Hz].
  - Conversion gain [dB] = **Output 300 MHz IF power [dBm]** – Input power [dBm]

- Noise equivalent power (NEP) for a 1 MHz on/off modulation.
  - **NEP [W/Hz$^{0.5}$]= (Output noise voltage [V^2/Hz])$^{0.5}$ / Responsivity [V/W].**
  - Responsivity [V/W] = **Output DC voltage [V]** / Input power [W].

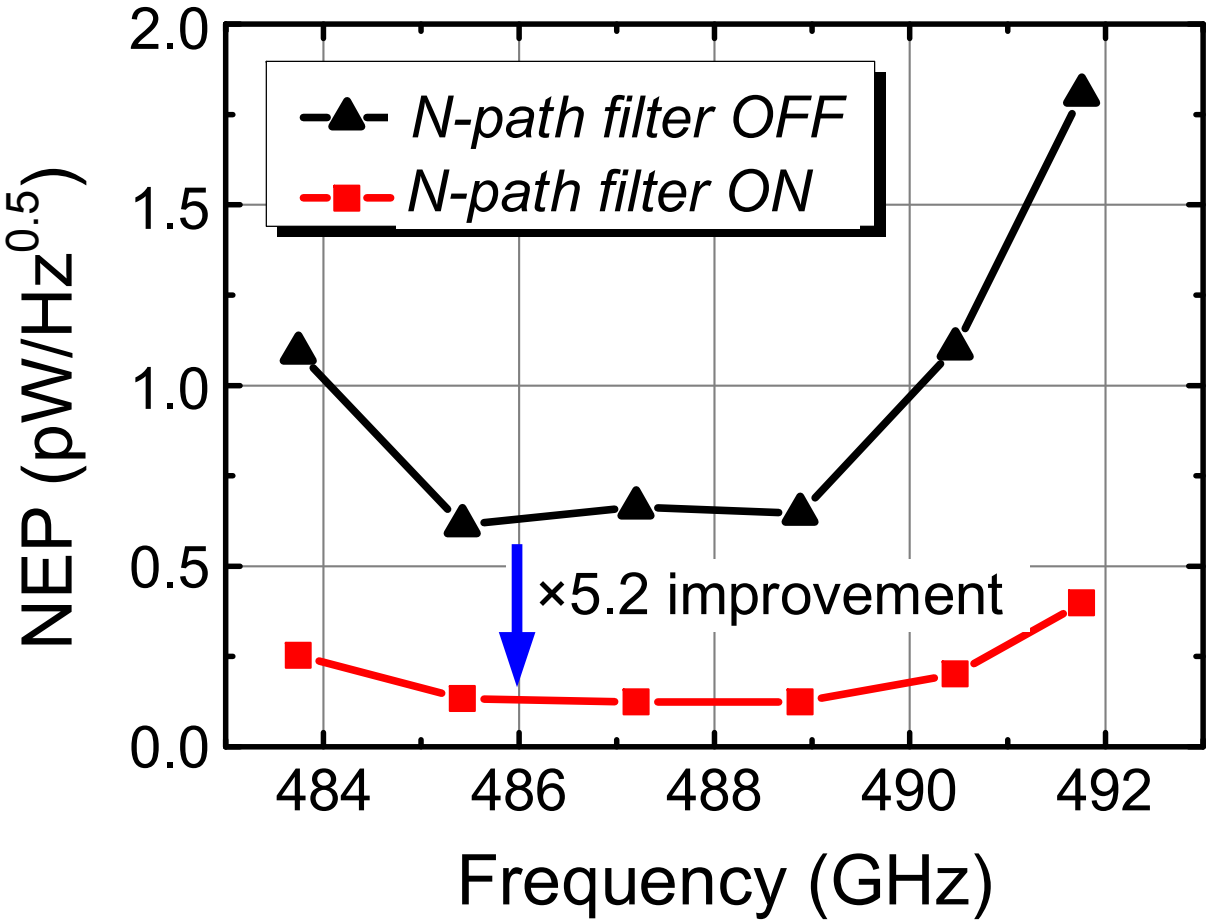
- Input power is estimated based on the Friis transmission equation.

Measured MDS



- Changing LO frequency by controlling V_D and V_G of the VCO
- **Minimum MDS = -101.3 dBm**

Measured NEP



- **Minimum NEP** is improved from 0.63 to **0.12 pW/Hz$^{0.5}$** due to the adoption of *N*-path filter.

Performance Comparison Table

References	JSSC'16 [4]	TTST'17 [1]	JSSC'19 [5]	VSLI'19 [2]	**This work**
Process	130 nm SiGe	130 nm SiGe	65 nm CMOS	65 nm CMOS	**65 nm CMOS**
RF freq. (GHz)	320	300	240	426	**490**
Mixer topology	2nd SHM	Fund.	Fund.	Fund.	**2nd SHM**
LO freq. (GHz)	160	300	240	426	**245**
LO type	PLL	Free-running	PLL	Injection-locking (@ 142 GHz)	**FLL**
MDS (dBm)	-71.5	N/A	-102.4	-86.6*	**-101.3**
NEP ($pW/Hz^{0.5}$)	N/A	3.9	N/A	N/A	**0.12**
Integration level	Fully-integrated	Fully-integrated	No IF-stage	No IF-stage, External 142 GHz source	**Fully-integrated**
Power (mW)	5.2 (Mixer) 75.5 (PLL)	21 (Mixer+VCO+ IF-stage)	21.6 (Mixer+VCO) 288 (PLL)	52 (Mixer+VCO)	**32 (Mixer+FLL+ IF-stage)**

* Estimated SSB NF from measured DSB NF + 3 dB

Conclusion

- A fully-integrated 490 GHz CMOS receiver adopting a DL-RBFLL is presented.
- The proposed **DL-RBFLL** allows to eliminate the power-hungry divider and buffer, thus the low-power implementation is achieved.
- The **DL** implementation extends acquisition range **six times** without increasing f_{REF}.
- The proposed receiver achieves;
  - power consumption of **32 mW from a 1.2 V supply.**
  - **MDS of -101.3 dBm** for a 1 kHz noise bandwidth.
  - **NEP of 0.12 pW/Hz$^{0.5}$** for a 1 MHz lock-in amplifier on/off modulation.