

# **Sub-THz CMOS Molecular Clock with 43ppt Long-Term Stability Using High- Order Rotational Transition Probing and Slot-Array Couplers**

**Cheng Wang, Xiang Yi, Mina Kim, Ruonan Han**

**Massachusetts Institute of Technology, Cambridge, MA**



**Massachusetts  
Institute of  
Technology**

# Outline

---

- **Background**
- **High-order locking for long-term stabilization**
- **Architecture and circuit design**
- **Measurement results**
- **Conclusions**

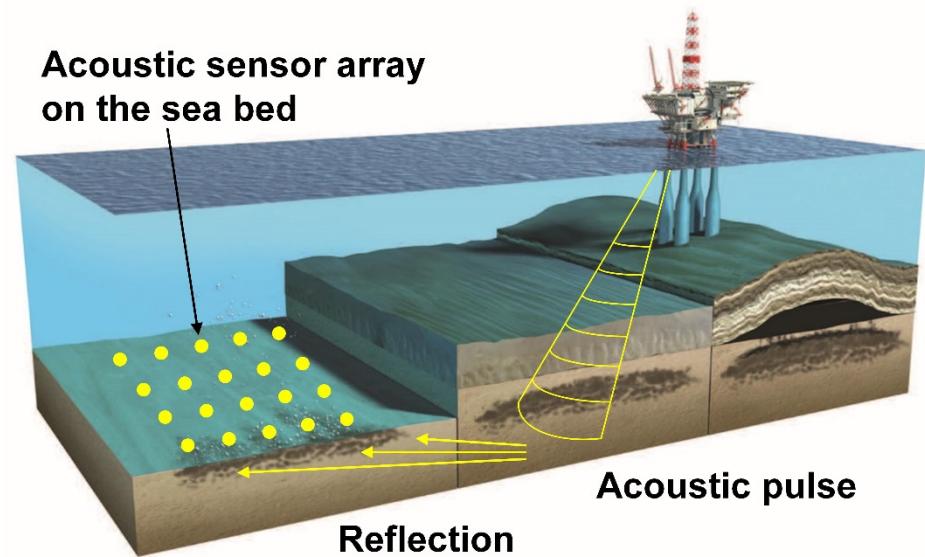
# Ultra-Stable, Miniaturized Clocks



[researchsnipers.com]

Synchronization of high-speed  
radio access networks

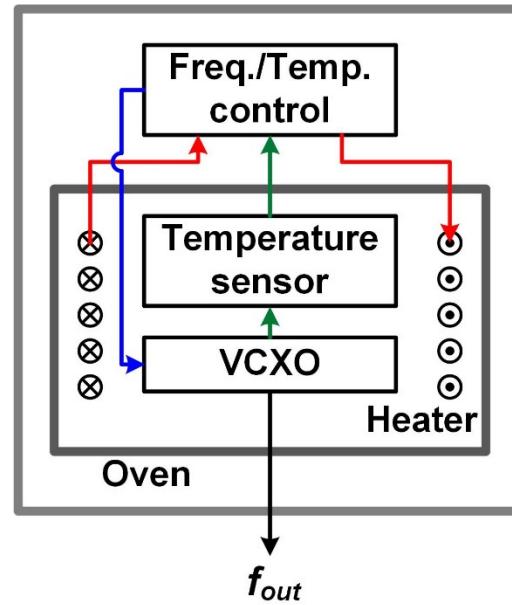
- 5G massive MIMO →  $\sigma_t < 65\text{ns}$
- Precise positioning →  $\sigma_t < 10\text{ns}$
- 1-min holdover →  $\Delta f < 10^{-10}$



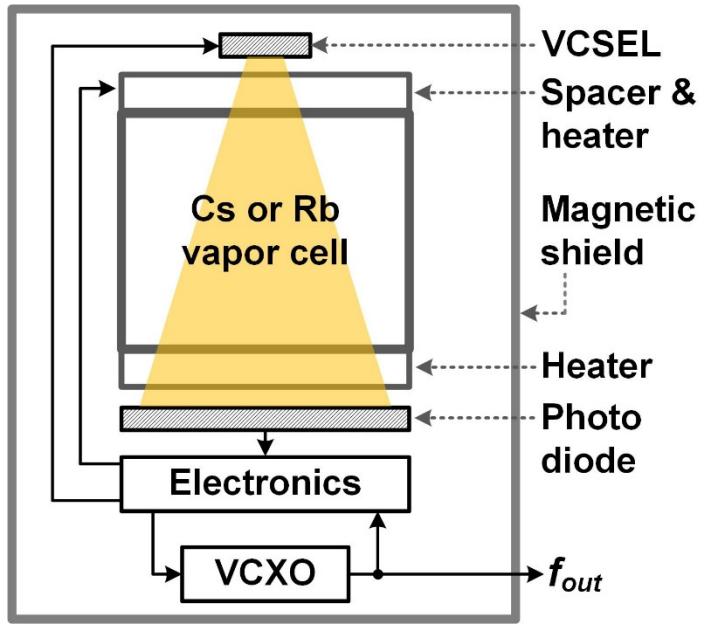
Precise timing for  
underwater oil exploration

- Temp. variation →  $\Delta f < 10^{-9}$
- Deployment time → Weeks
- DC Power →  $\sim 100\text{mW}$

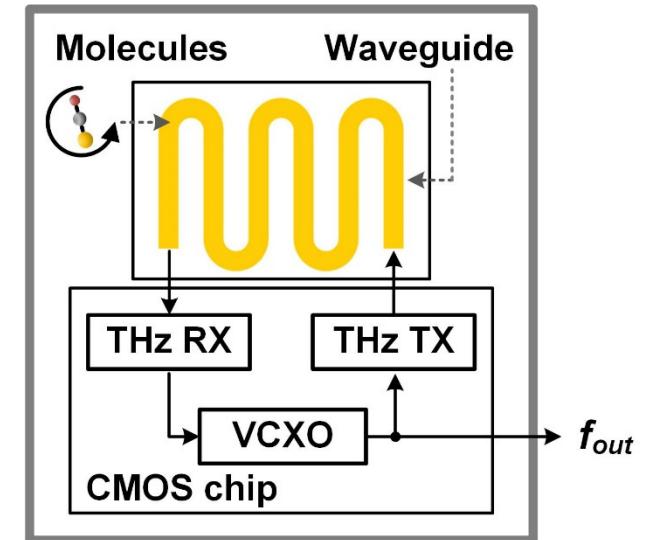
# Comparison of Portable Clocks



**Oven compensated crystal oscillator (OCXO)**



**Chip-scale atomic clock (CSAC)**



**Chip-scale molecular clock (CSMC) (This work)**

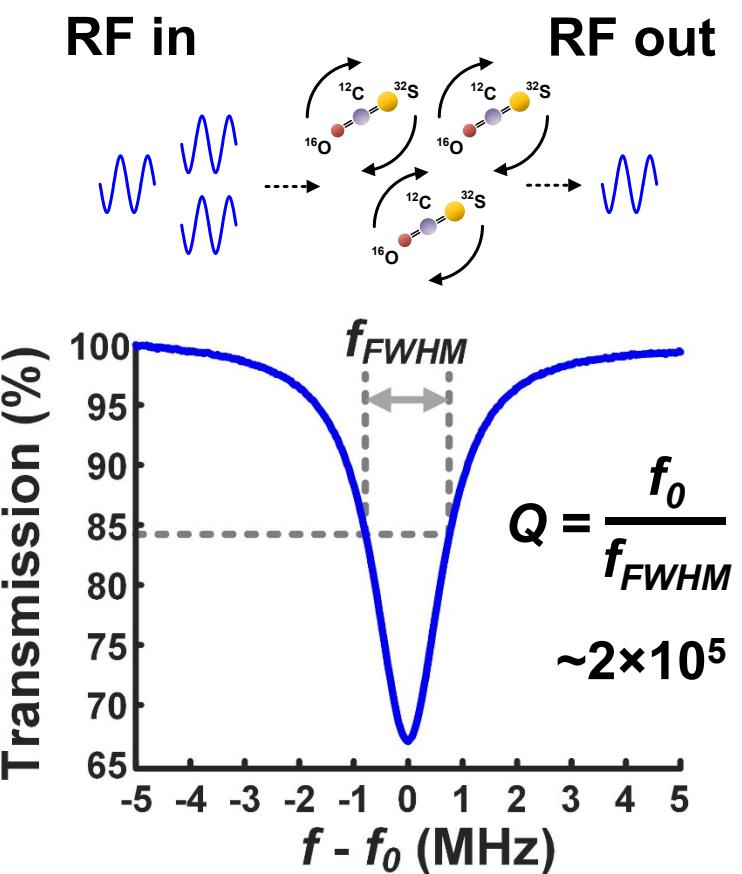
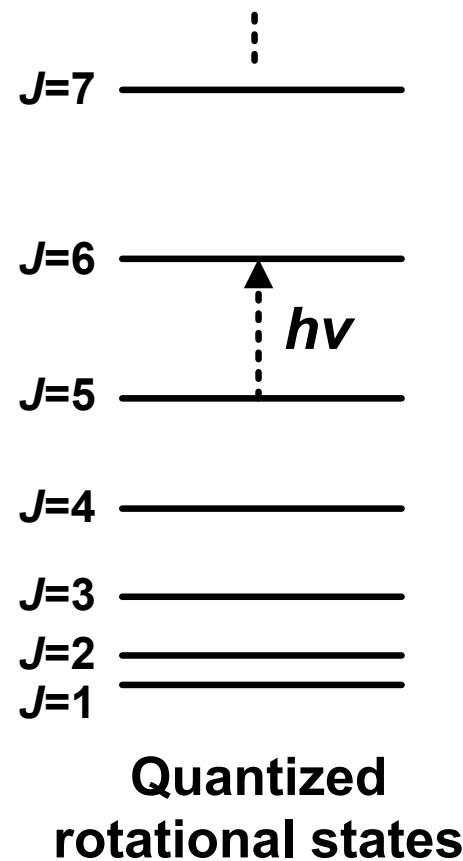
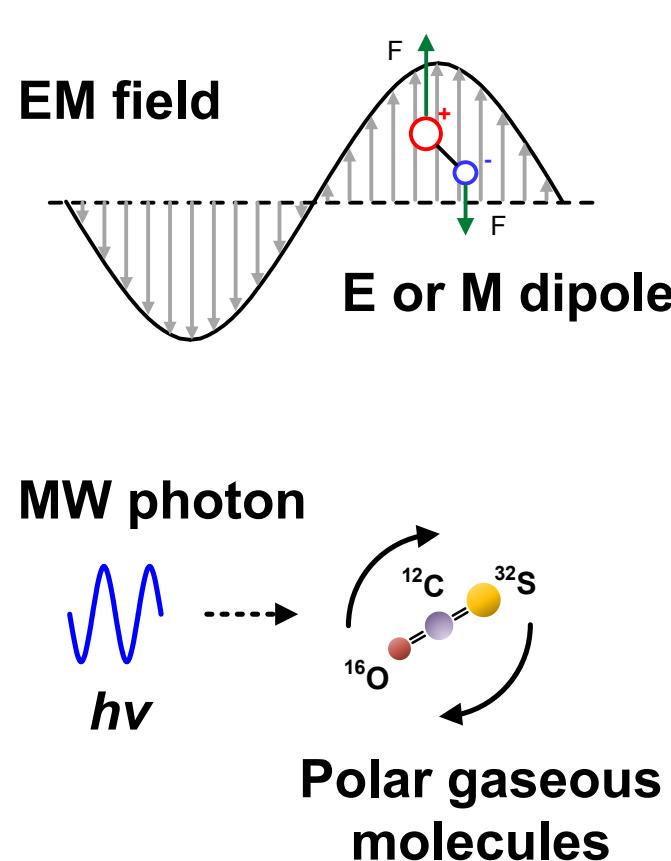
<b>Stability</b>	$\sim 10^{-10} @ 10^3 s$		$\sim 10^{-11} @ 10^3 s$		$\sim 10^{-11} @ 10^3 s$	
<b>Power</b>	$\sim 1W$		$\sim 100mW$		$\sim 100mW$	
<b>Cost</b>	$\sim \$100$		$\sim \$1000$		$\sim \$10$	

# Outline

---

- Background
- **High-order locking for long-term stabilization**
- Architecture and circuit design
- Measurement results
- Conclusions

# Rotational Spectra of Polar Gaseous Molecules

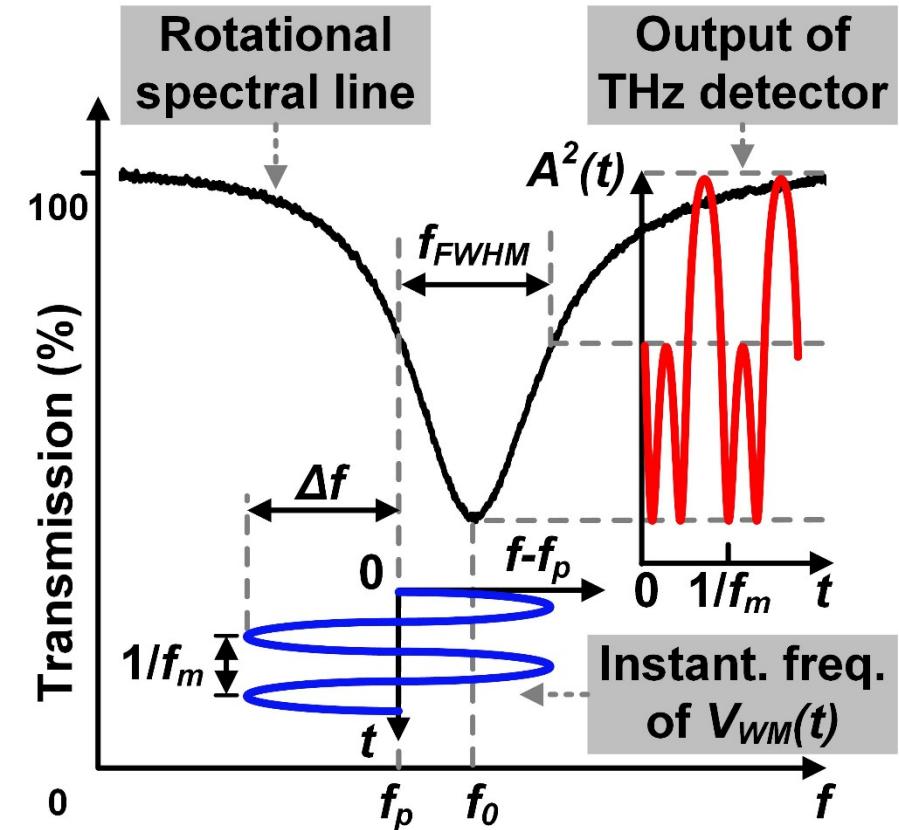
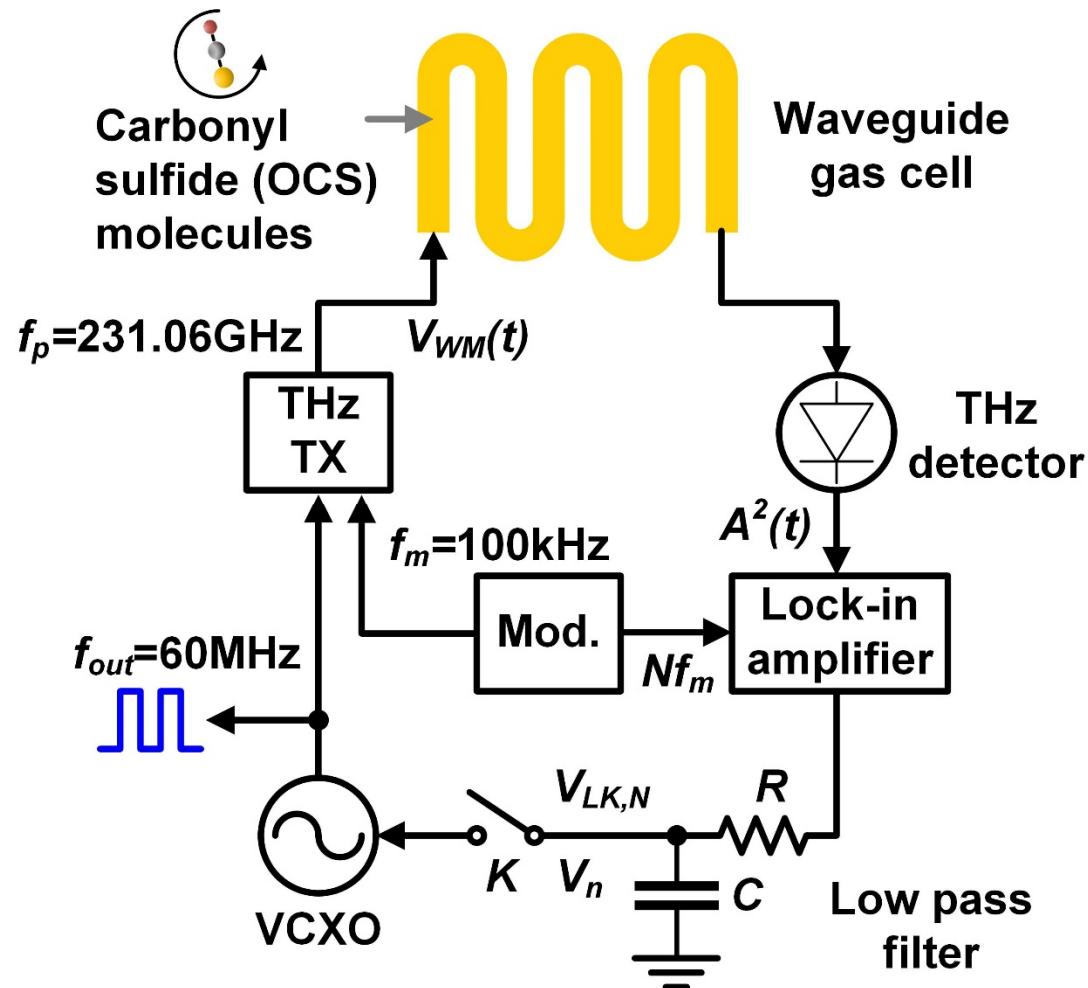


E/M torque  $\rightarrow$   
molecular rotation

Photon absorption  $\rightarrow$   
state transition ( $J \rightarrow J+1$ )

Rotational spectra  
observed in WG gas cell

# Wavelength Modulation Spectroscopy (WMS)

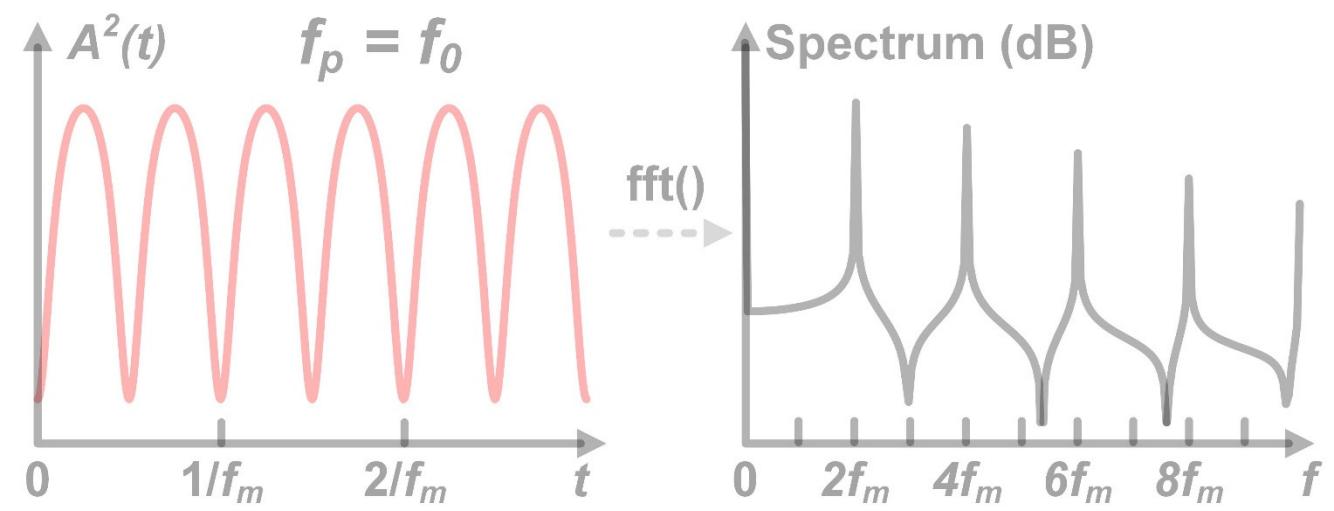
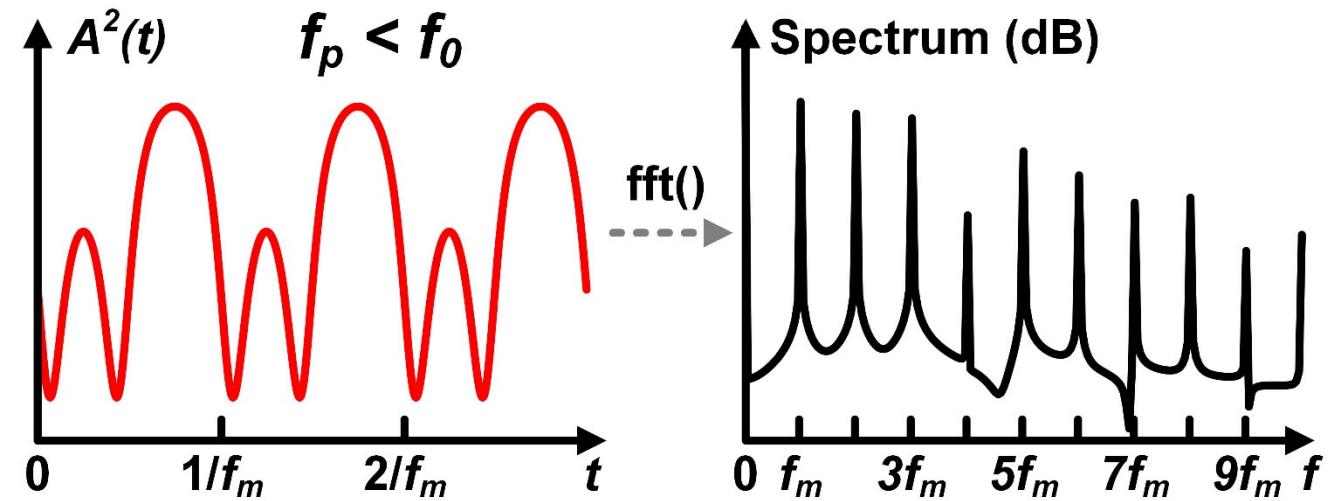
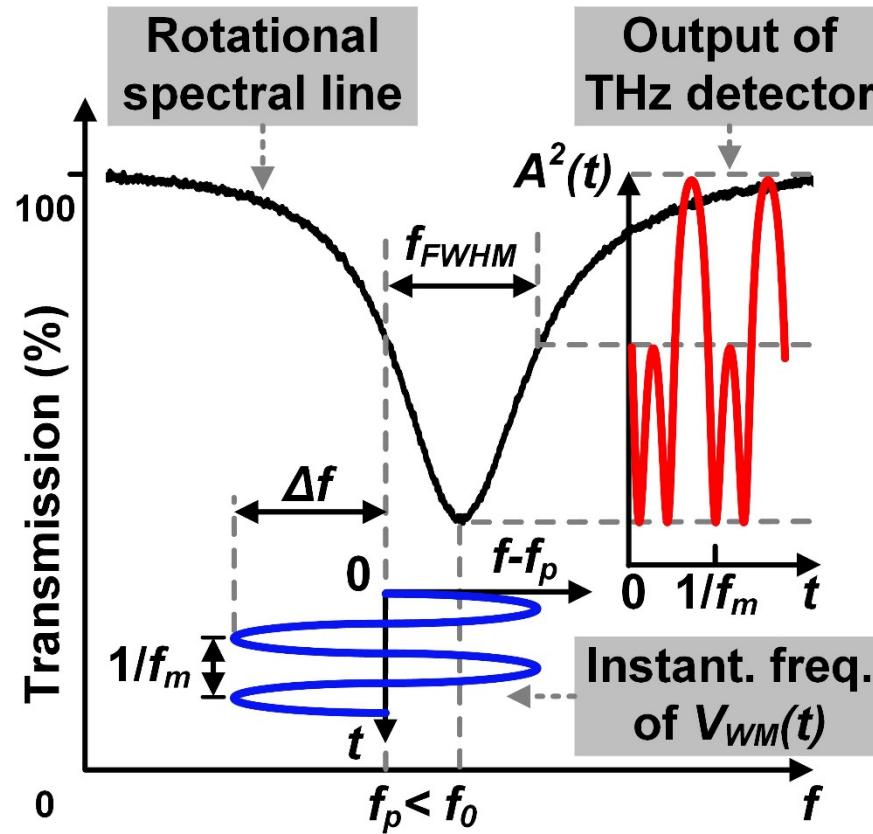


$$V_{WM}(t) = A(t) \cdot \sin[2\pi f_p t + \Delta f \cdot \sin(2\pi f_m t + \theta_0)]$$

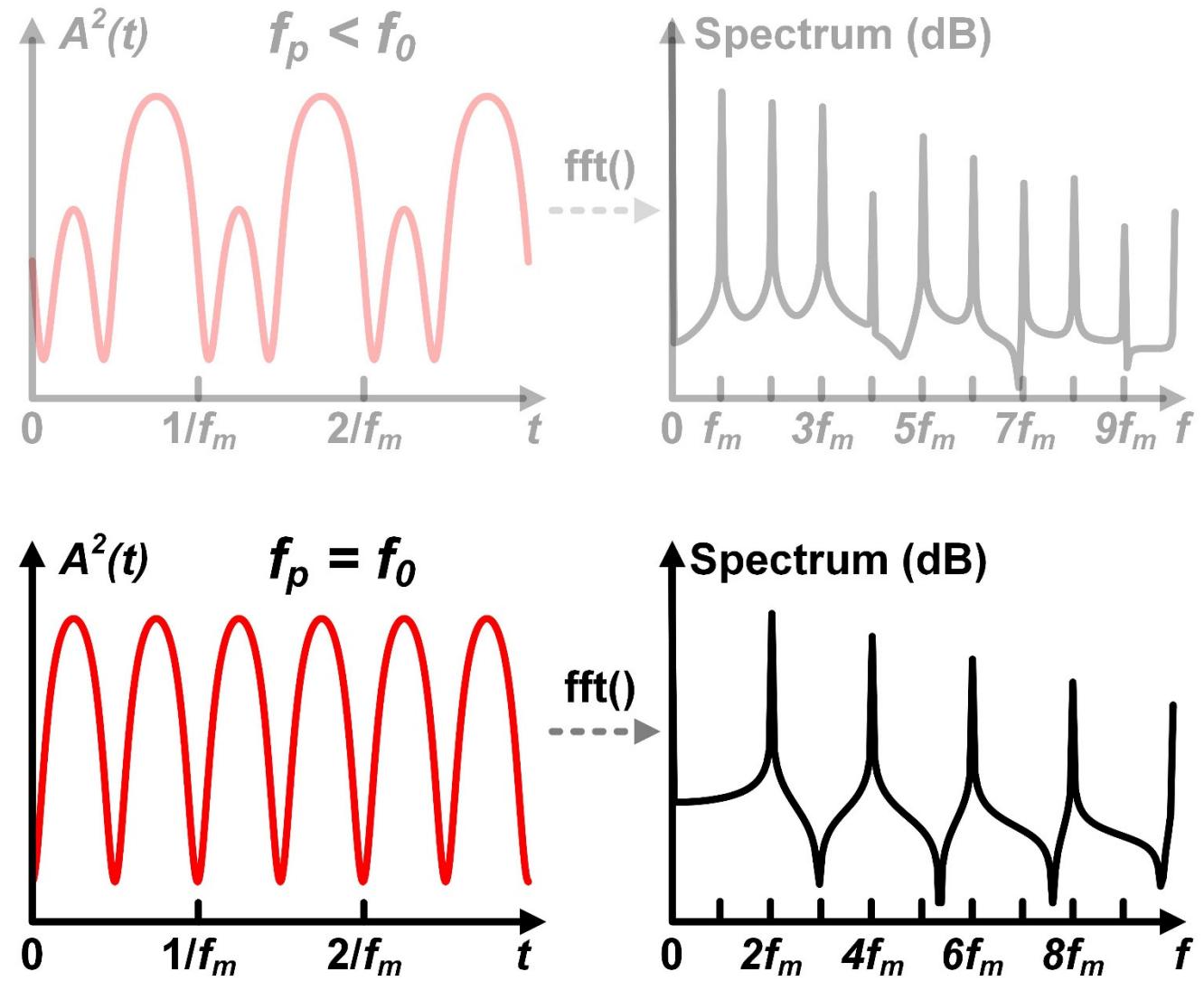
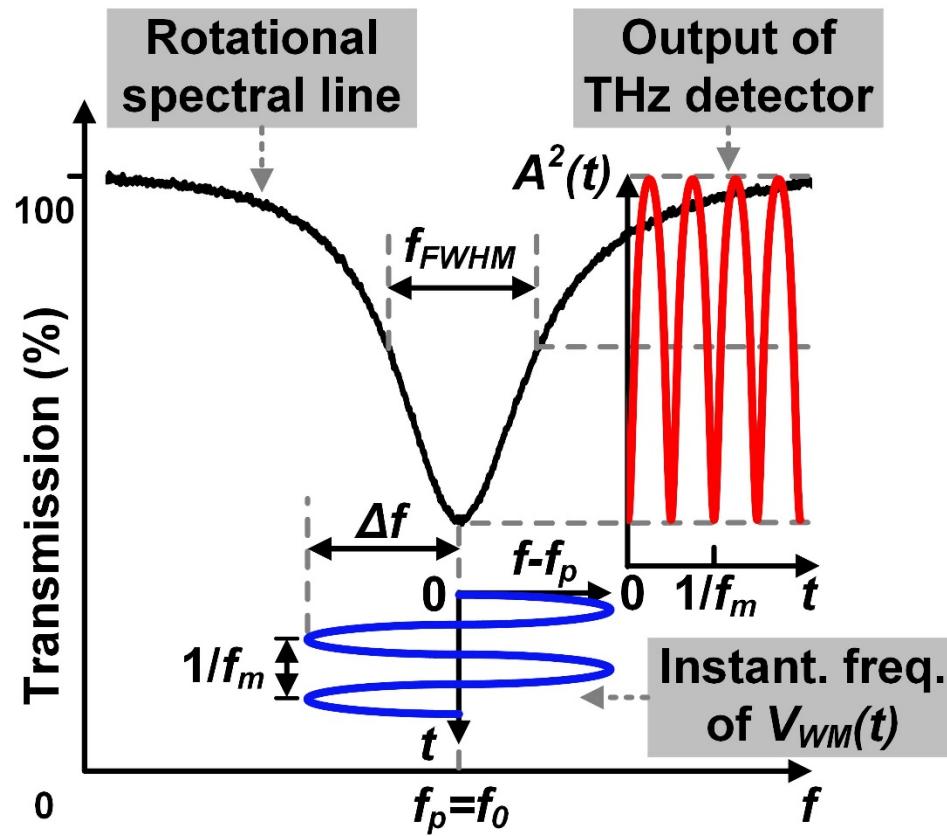
$f_m$  - Modulation freq.    $\Delta f$  - Freq. deviation

- $K$ : “open” → rotational spectrometer

# High Order Harmonics of $f_m$

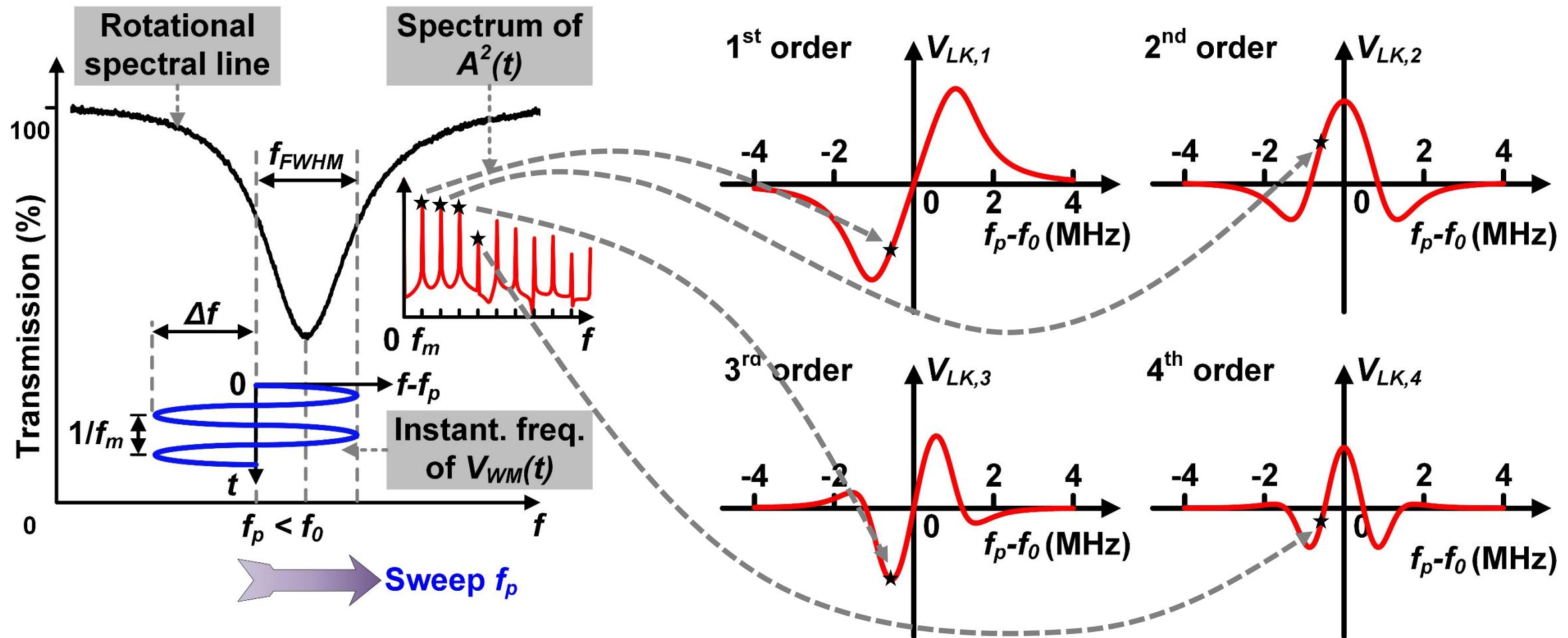


# High Order Harmonics of $f_m$



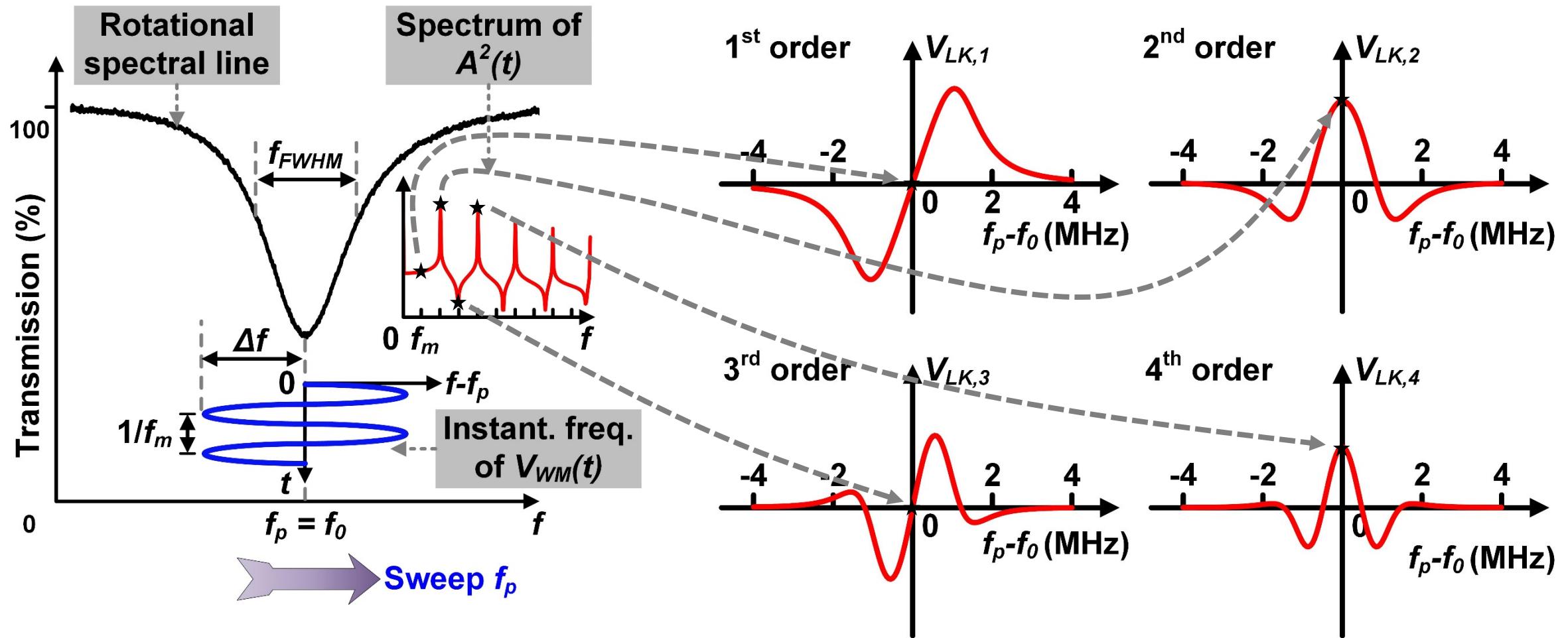
# Multi-Order Dispersion Curves

$N^{\text{th}}$  order dispersion curve  $\approx N^{\text{th}}$  order derivative

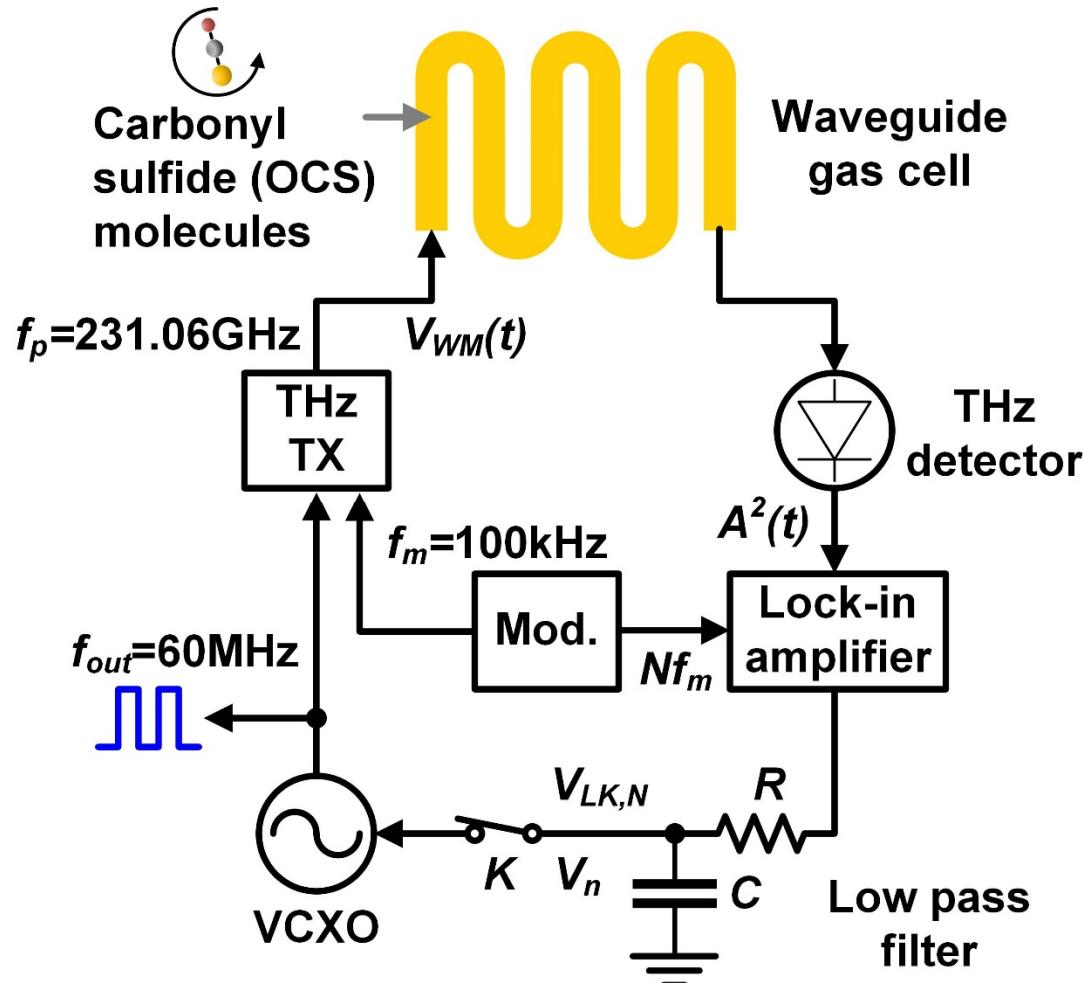


# Multi-Order Dispersion Curves

Odd order curves → zero-crossing point



# Molecular Clock Locking to Spectral Line Center

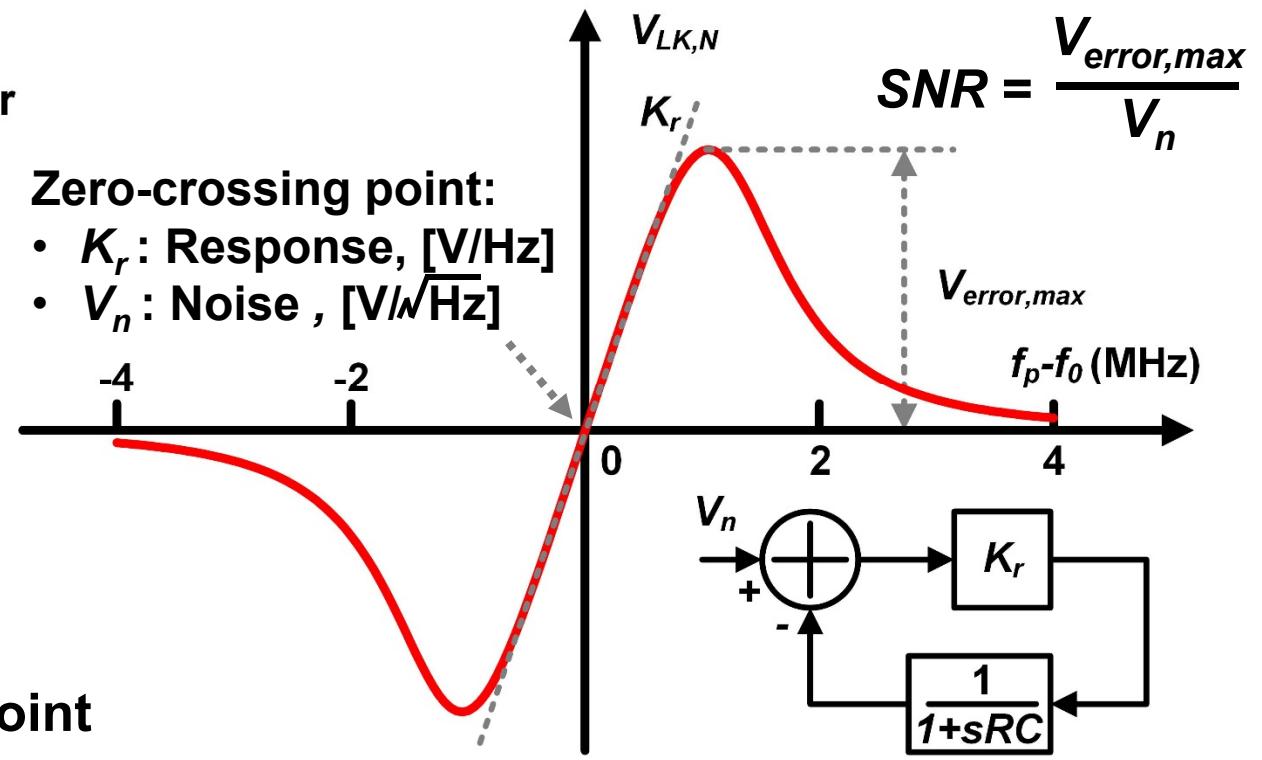


- $K$ : “closed”  $\rightarrow$  Lock to zero-crossing point

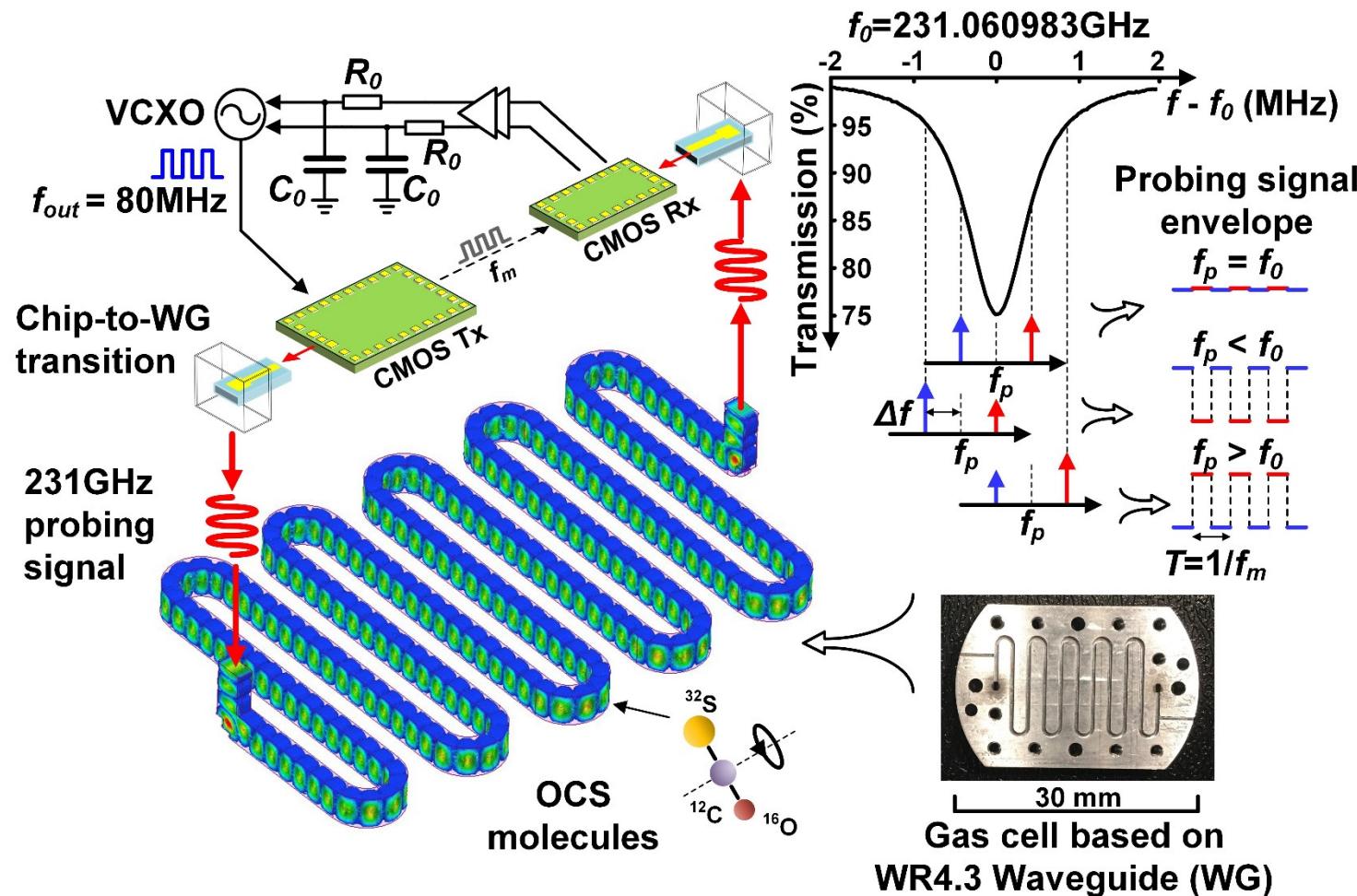
Allan deviation:

$$\sigma_y = \frac{V_n}{\sqrt{2T} \cdot K_r \cdot f_0} \approx \frac{N_0}{\sqrt{T} \cdot Q \cdot SNR}$$

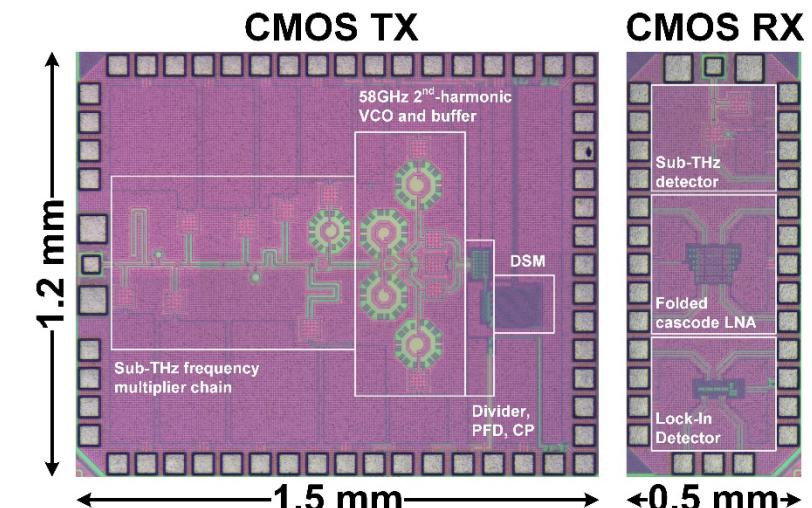
$T$  - Avg. time



# Proof-of-Concept: The 1<sup>st</sup> CSMC Prototype

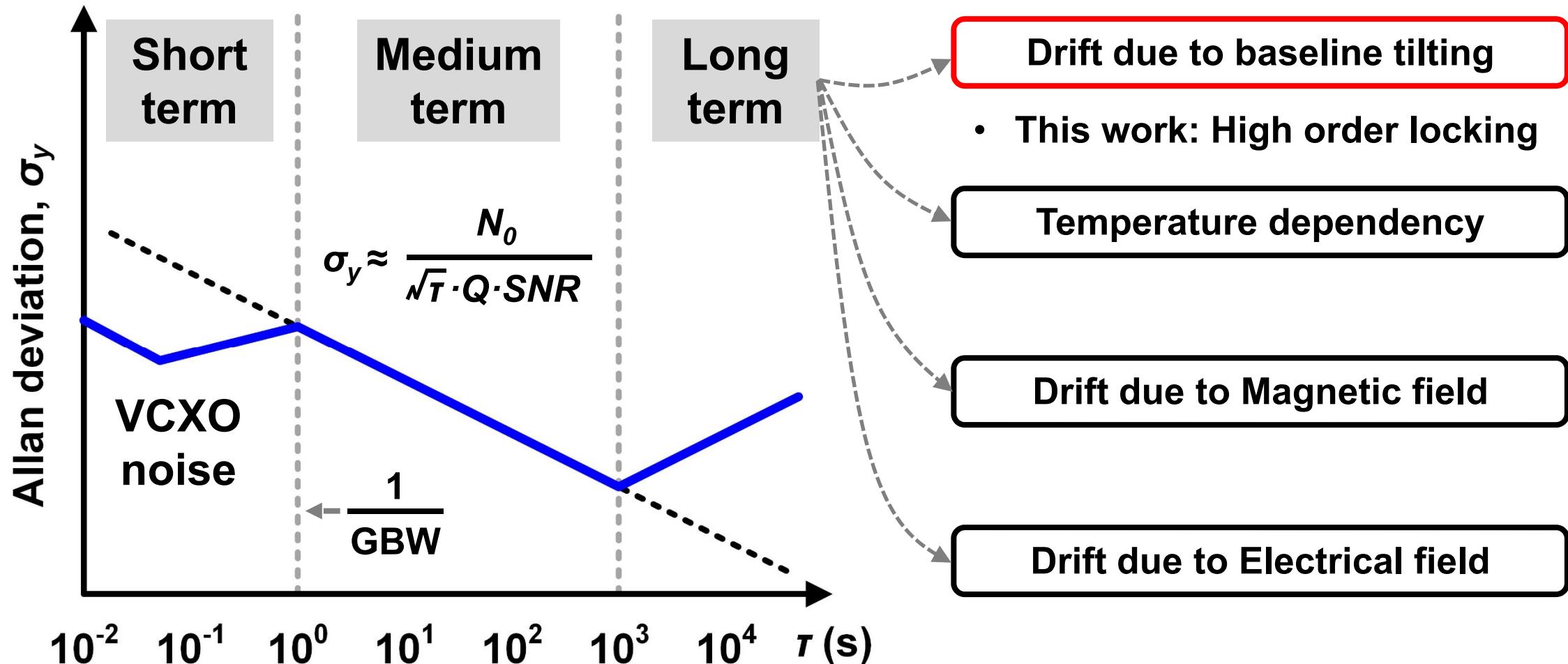


[C. Wang, et al., *Nature Electronics*, 2018]

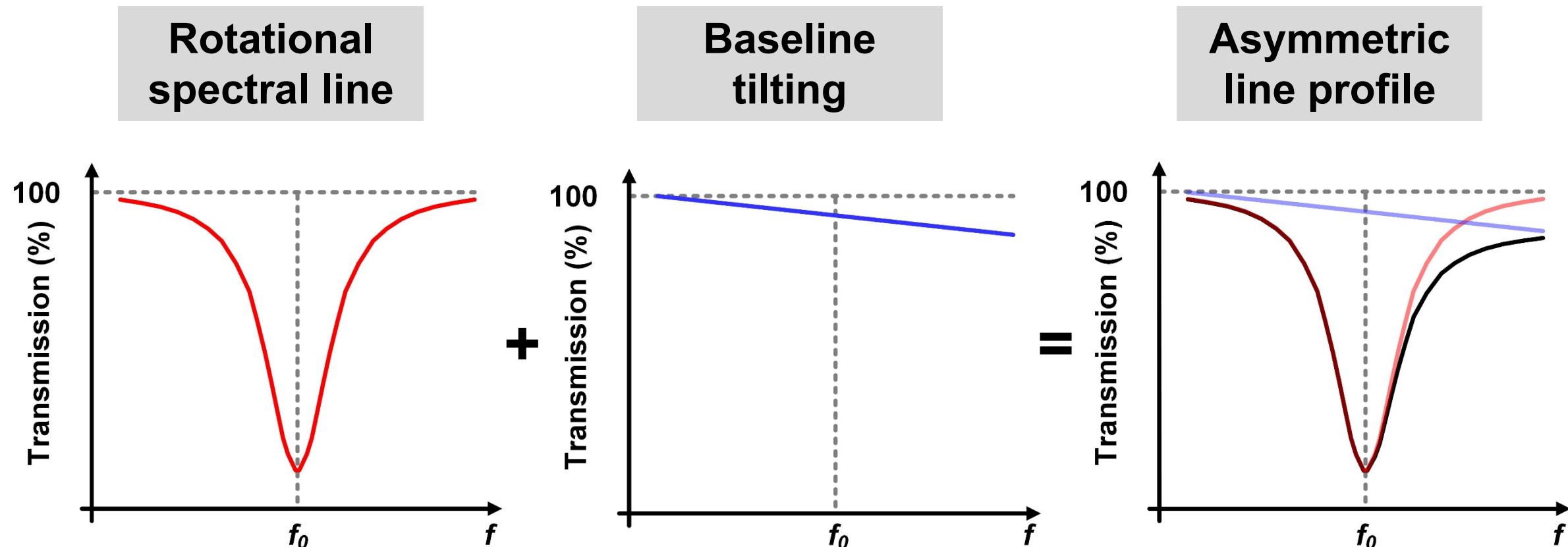


- 231.061GHz line of OCS
- 1<sup>st</sup> order dispersion curve
- Frequency stability:  
 $\sigma_y = 3.8 \times 10^{-10} @ \tau = 10^3 \text{s}$
- 66mW DC power.

# Frequency Stability of Molecular Clock



# Asymmetric Line Profile due to Baseline Tilting

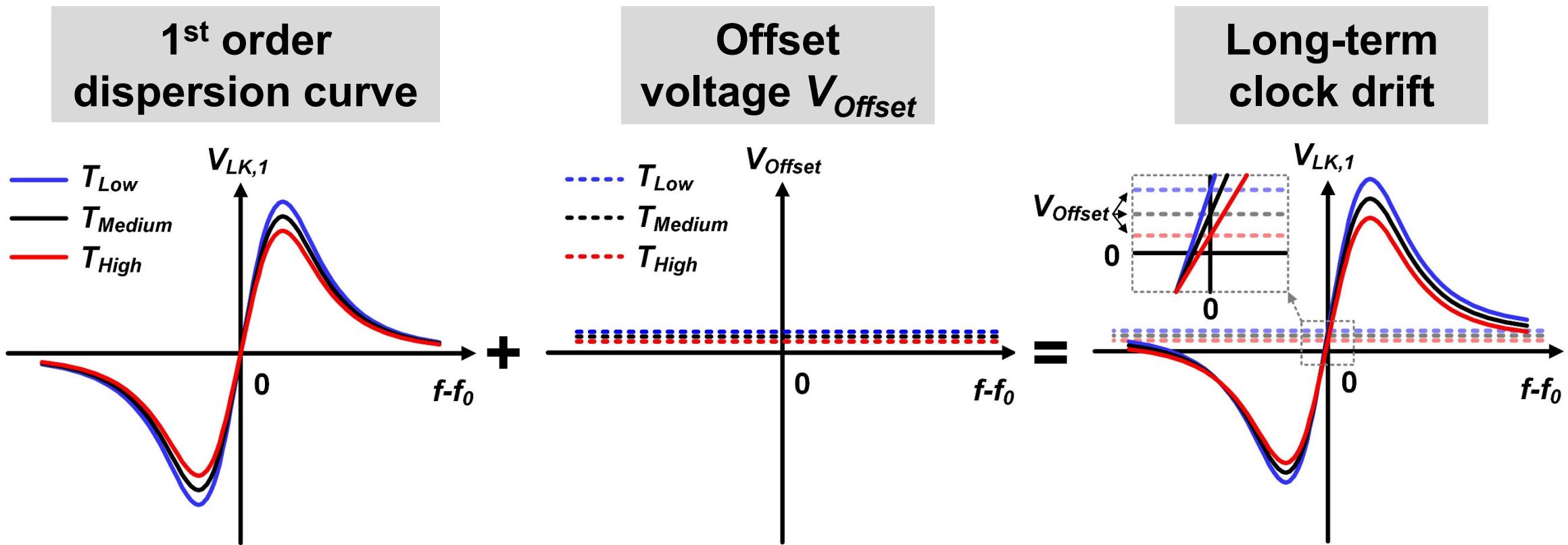


- Symmetric in theory

- THz transceiver response
- Gas cell response

- Measured in reality

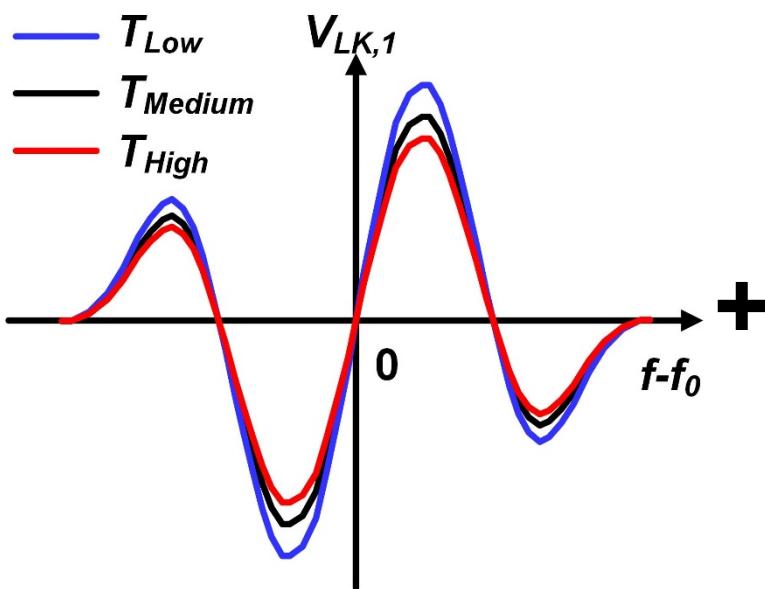
# 1<sup>st</sup> Order Dispersion Curve w/ Baseline Tilting



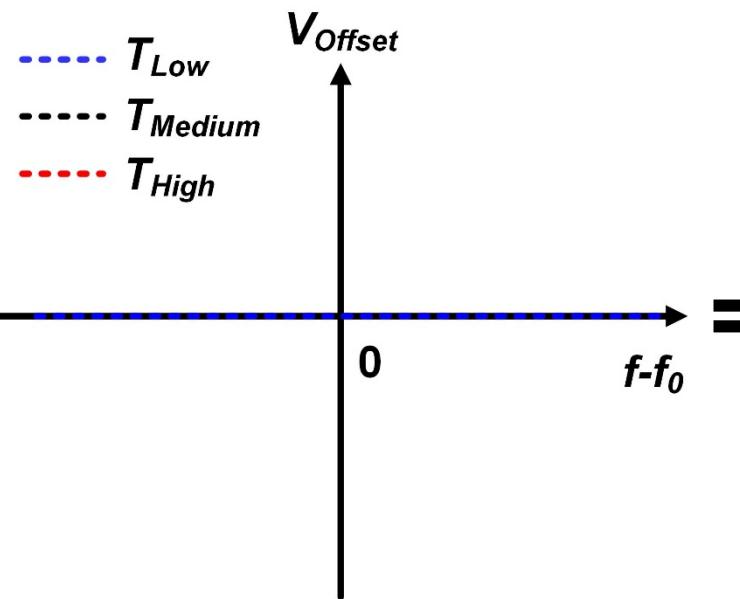
- Invariant zero-crossing point under PVT
- $V_{offset}$  is PVT dependent
- How to deal with varying zero-crossing point?

# High Order Dispersion Curve w/ Baseline Tilting

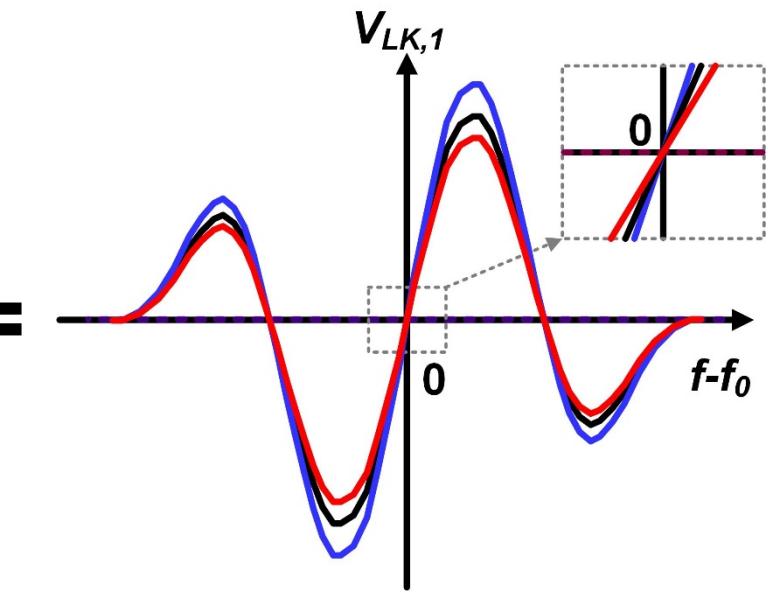
High order dispersion curve



Offset voltage  $V_{Offset}$



Stability enhanced

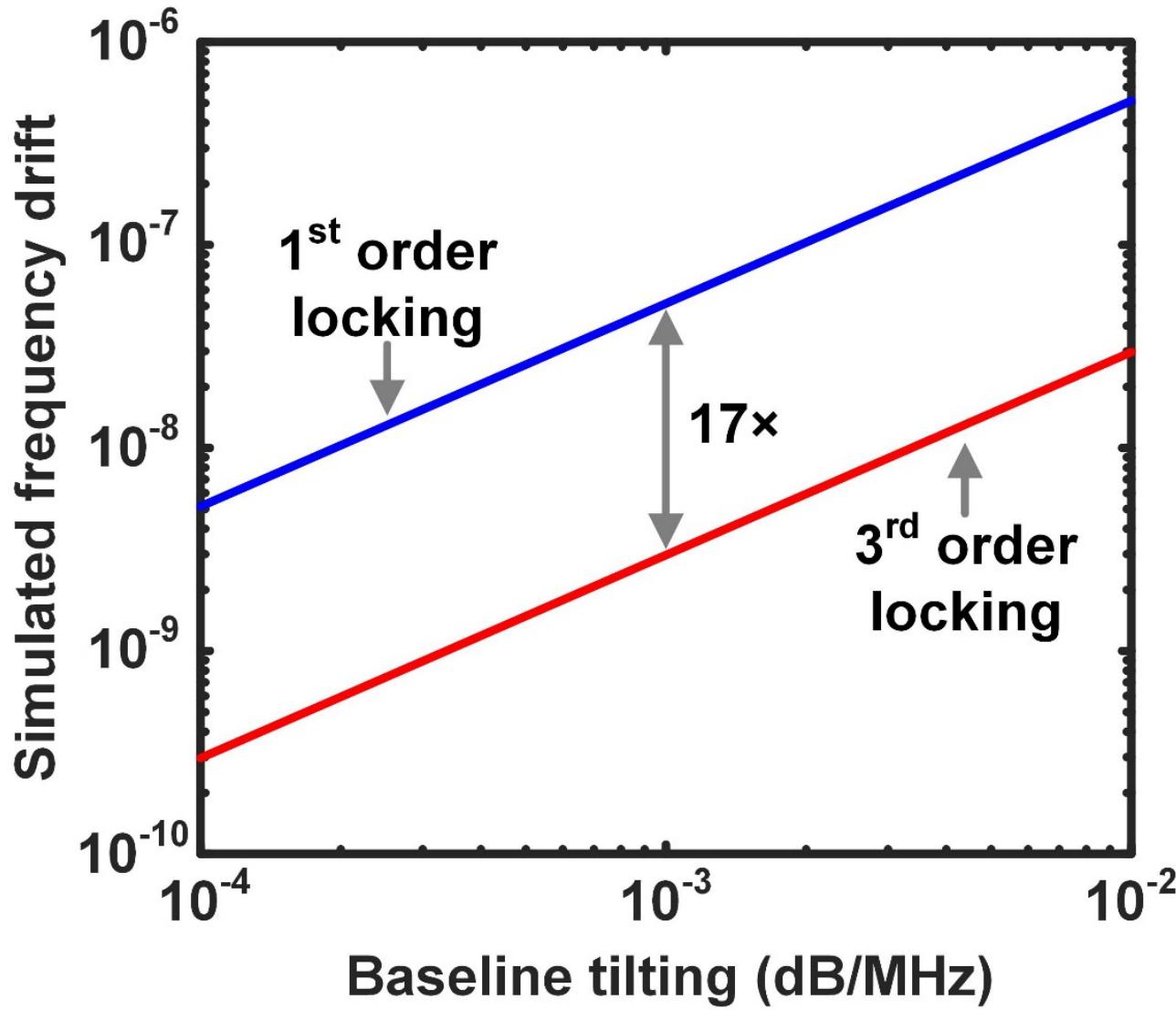


- Invariant zero-crossing point under PVT

- Eliminated by high order derivative,  $V_{offset} \approx 0$

- Invariant zero-crossing point under PVT

# Idea: CSMC with High-Order Locking



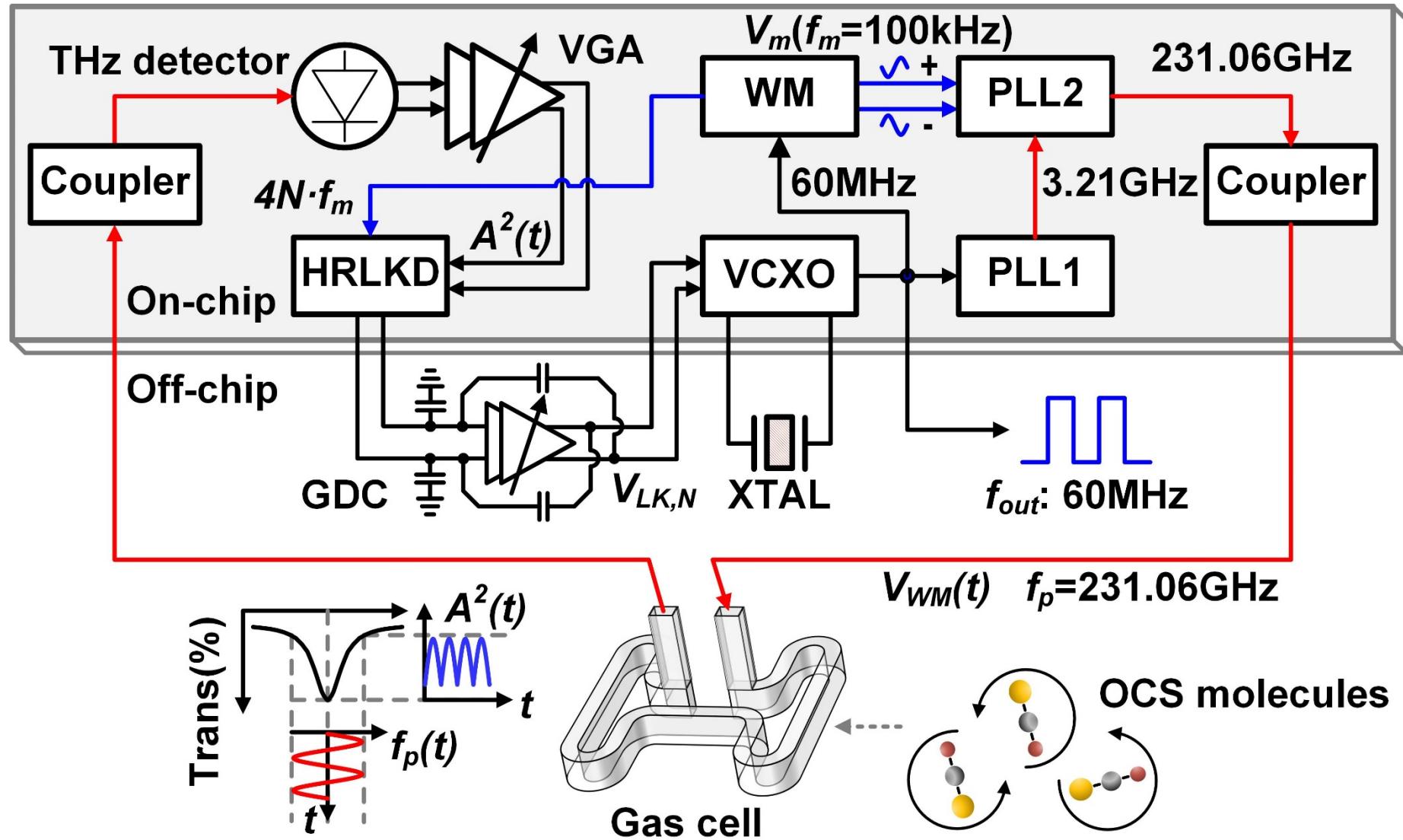
- Simulation: **0.1dB/GHz** baseline tilting → a frequency drift of:
  - $5 \times 10^{-9}$  for 1<sup>st</sup> order locking
  - $3 \times 10^{-10}$  for 3<sup>rd</sup> order locking
- This work: a chip-scale molecular clock (CSMC) locking to high order dispersion curve

# Outline

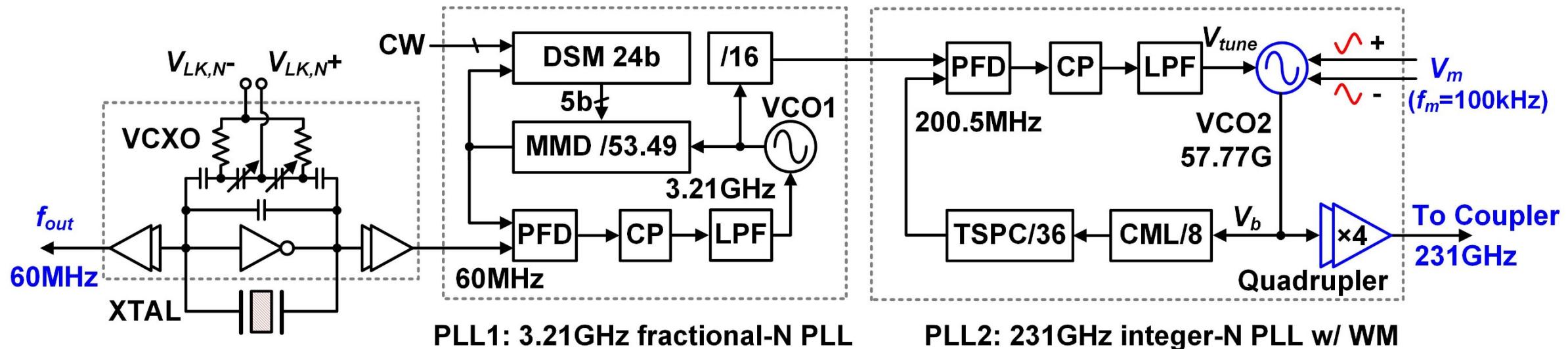
---

- Background
- High-order locking for long-term stabilization
- **Architecture and circuit design**
- Measurement results
- Conclusions

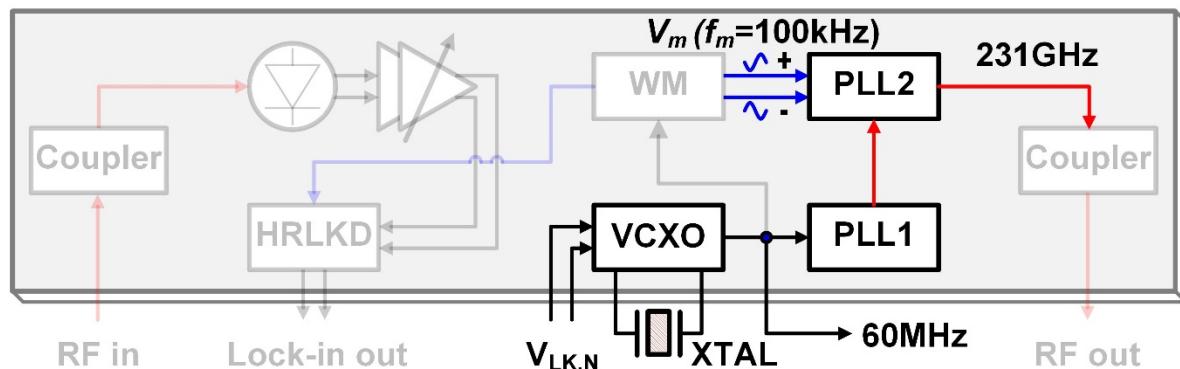
# System Architecture



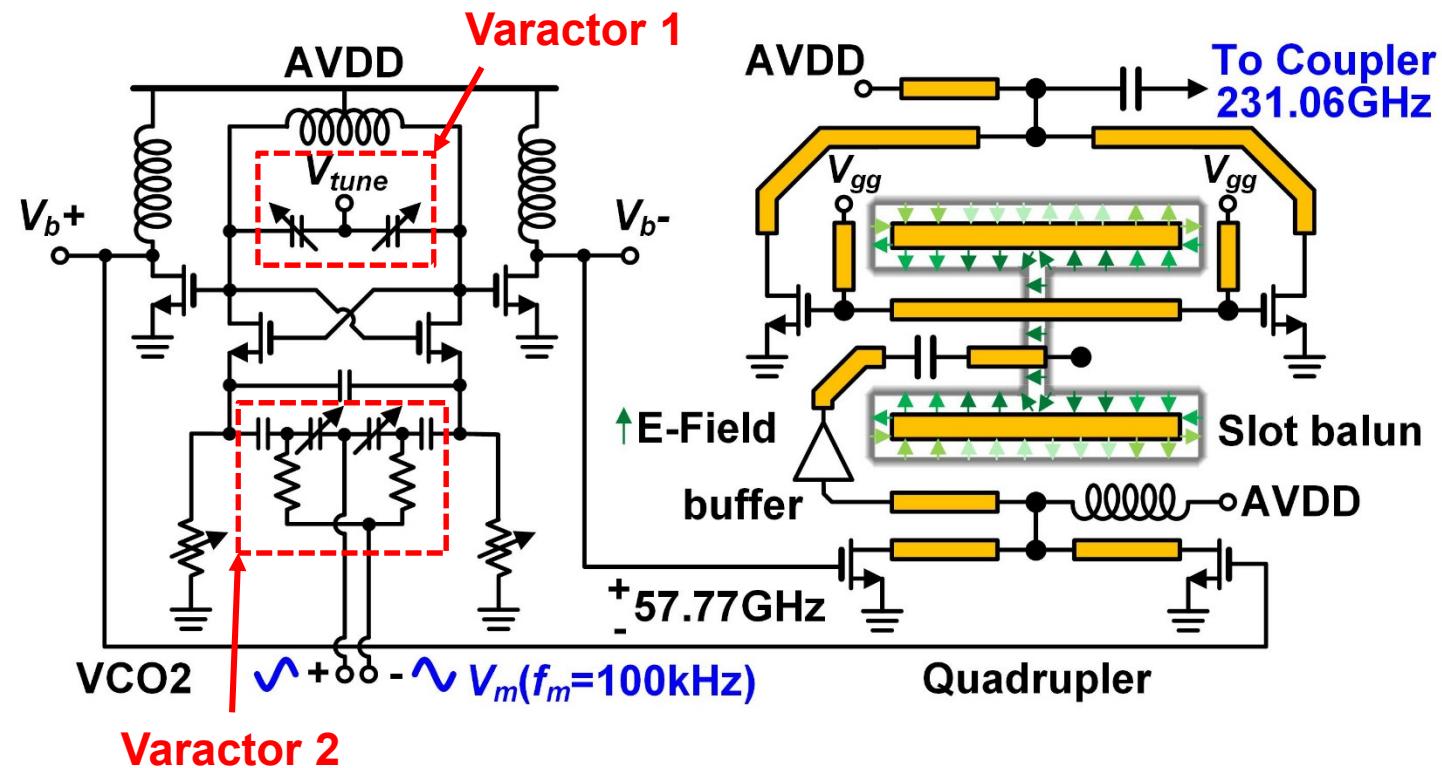
# TX: 231GHz Cascaded Two-Stage PLL



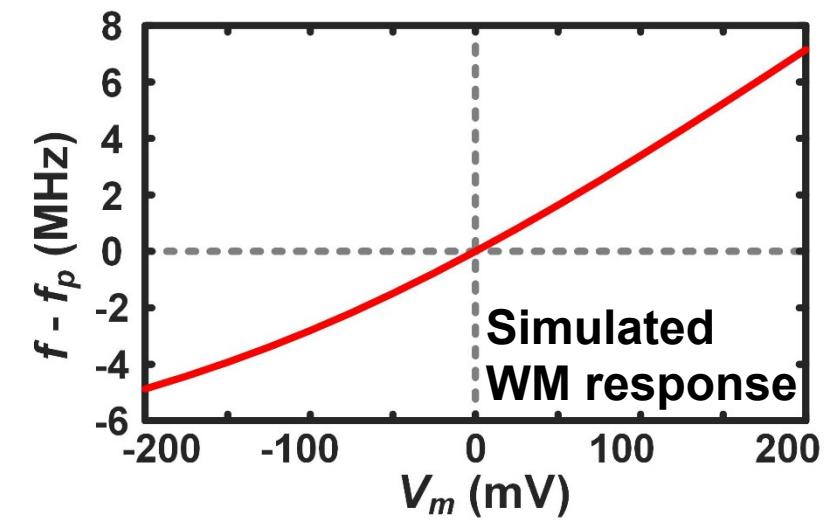
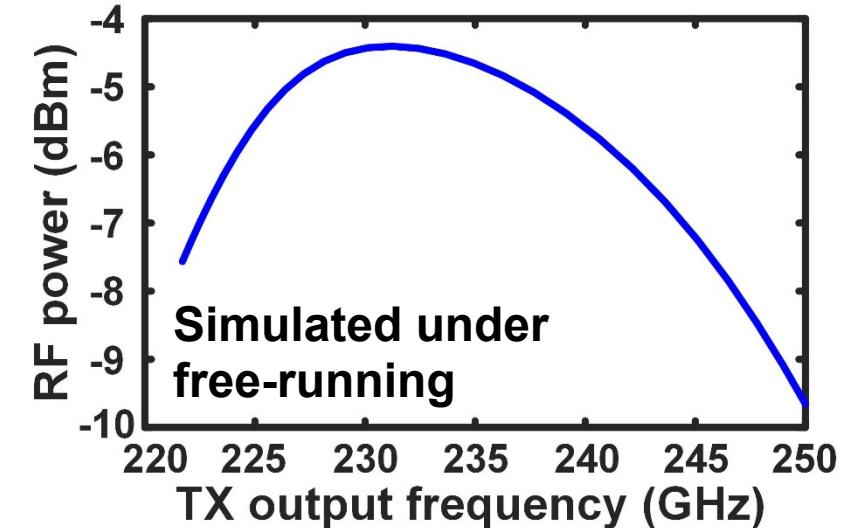
- **Freq. tunability:**  $\sim 1\%$  of line width  $f_{FWHM}$
- **27GHz (12%) bandwidth for line coverage**
- **Precise wavelength modulation (WM)**
  - $\Delta f/f_p \approx 10^{-5}$  ( $\Delta f \approx 2.5\text{MHz}$ ,  $f_p = 231.06\text{GHz}$ )



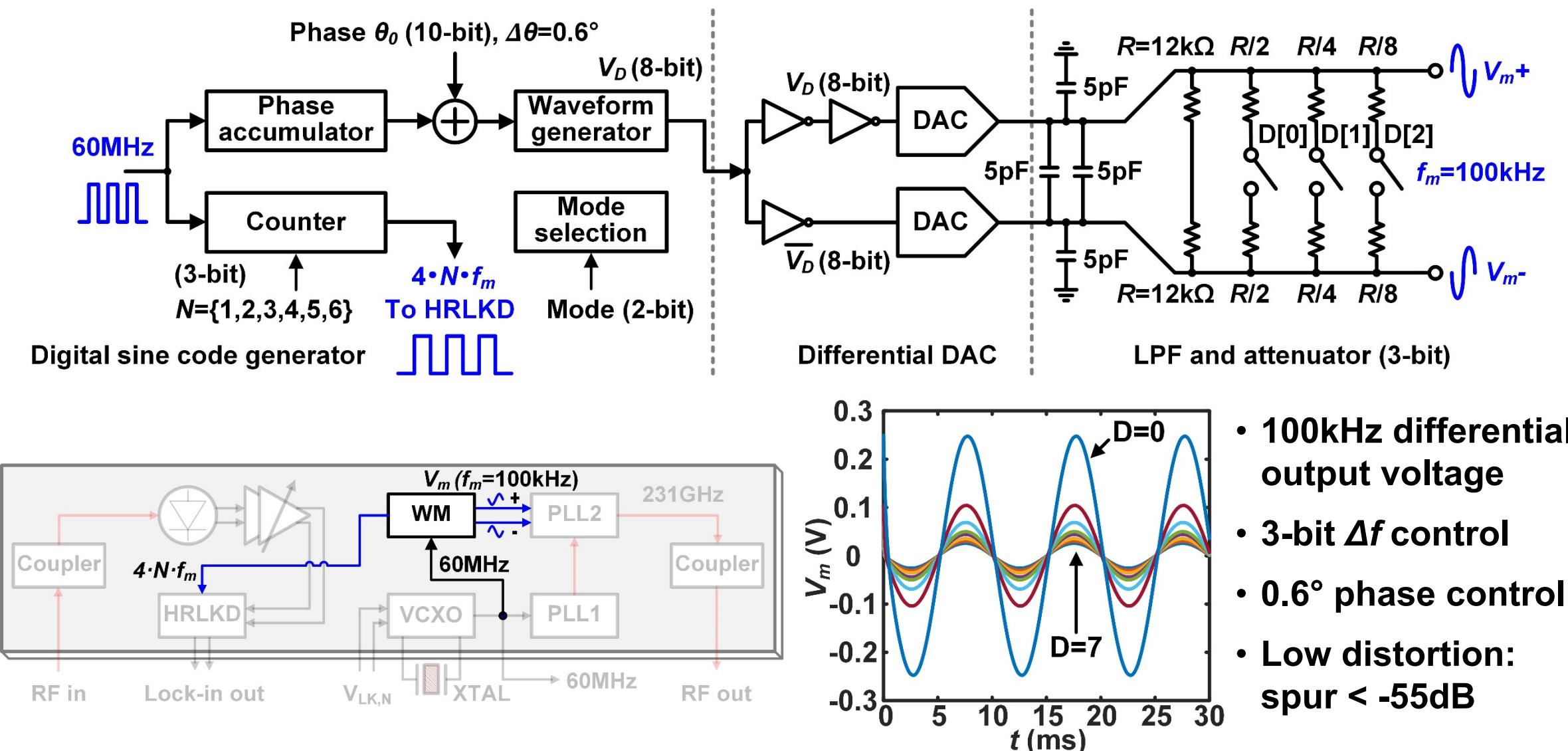
# TX PLL2: 57.77GHz VCO and 231GHz Quadrupler



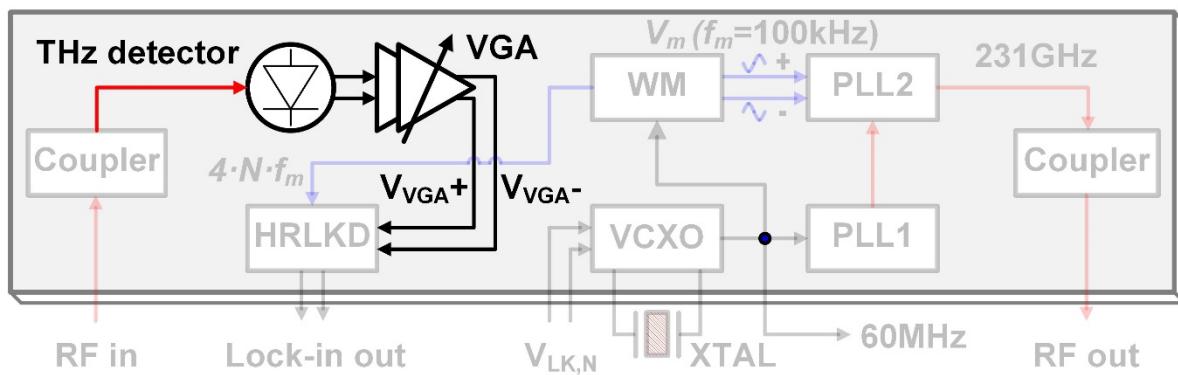
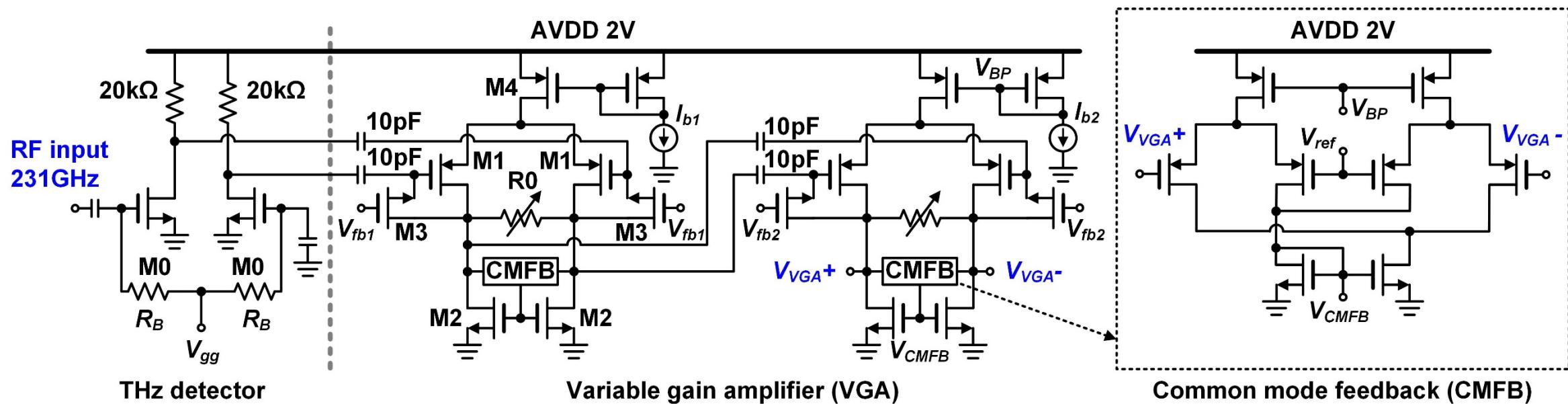
- Varactor 1: highly-sensitive for large PLL bandwidth
- Varactor 2: low sensitivity for wavelength modulation
  - $KVCO_{Varactor\ 1} / KVCO_{Varactor\ 2} \approx 10^3$



# TX: Wavelength Modulator (WM)

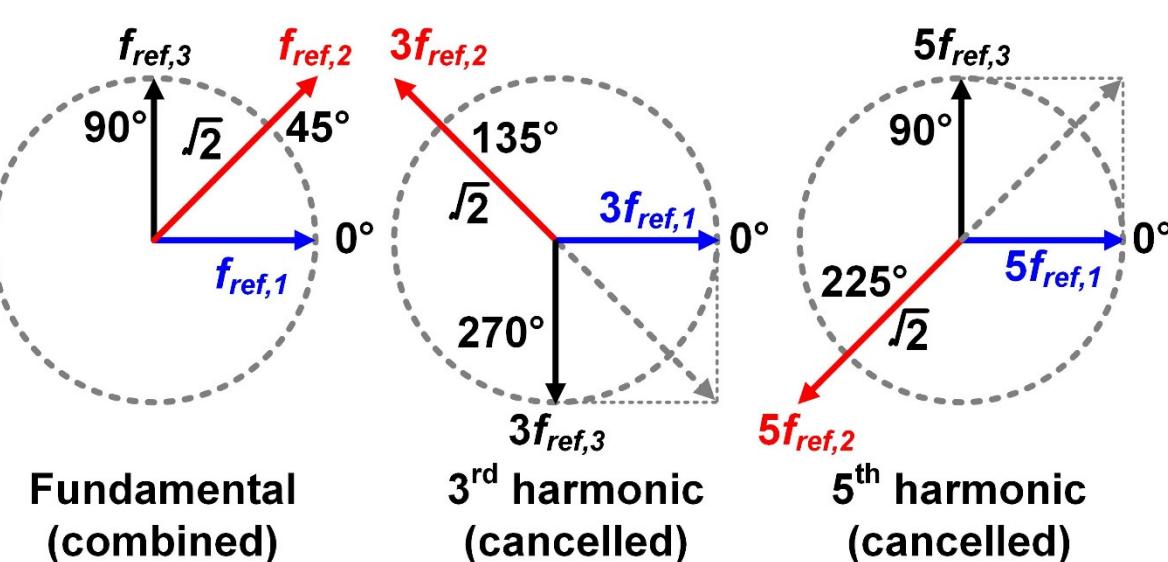


# RX: THz Detector and VGA

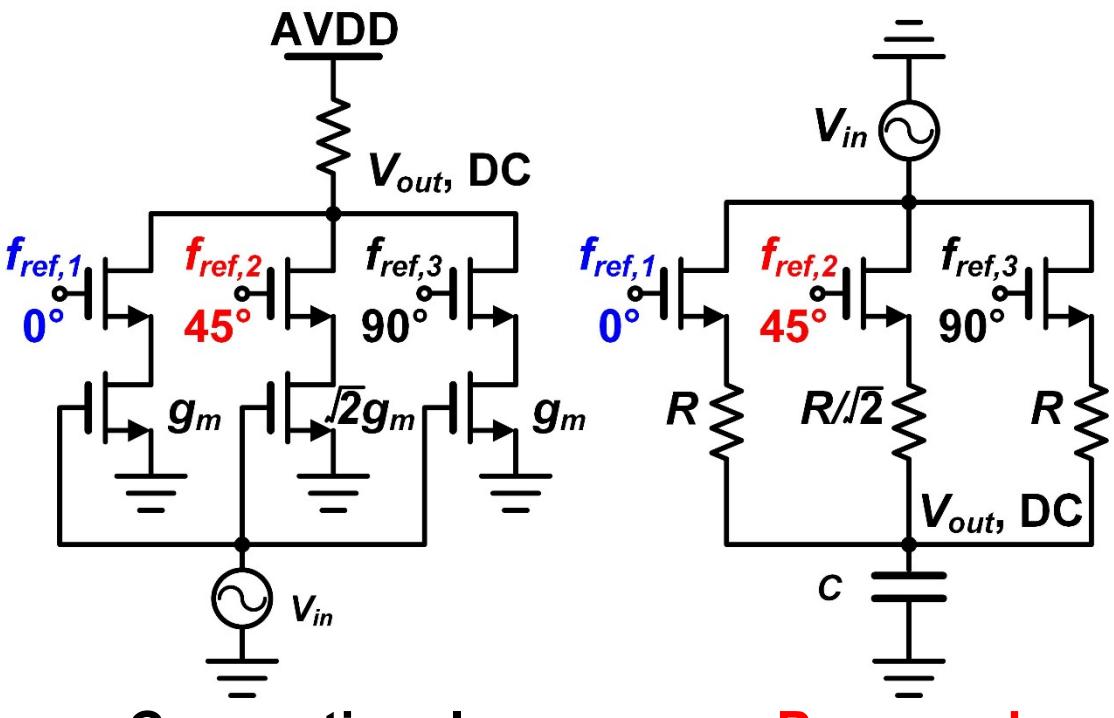
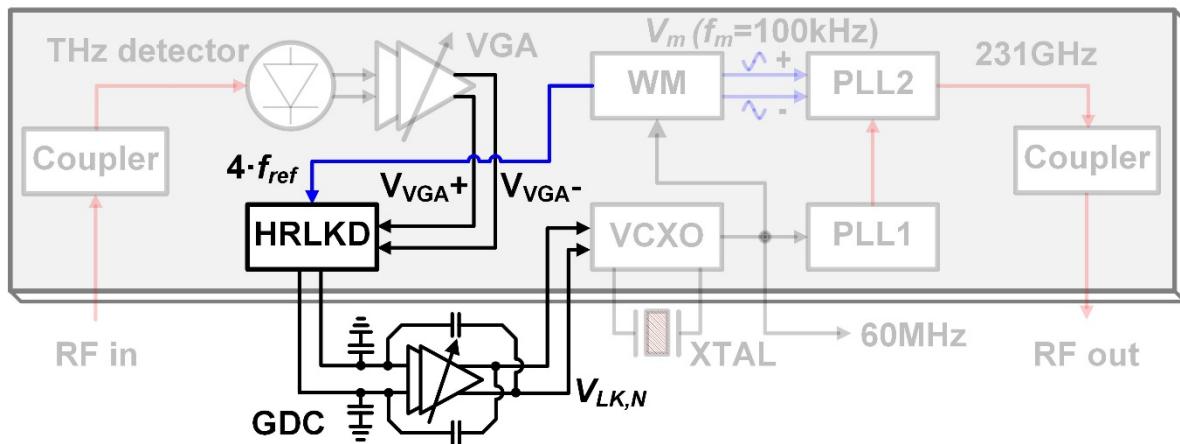


- **Sub-threshold NMOS pair → low noise THz square-law detector**
- **2-stage variable gain amplifier**
  - **65dB max gain / 10-bit control**
  - **AC coupled / monolithic integrated**

# RX: Harmonic Rejection Lock-in Detector (HRLKD)



Phasor diagram of harmonic rejection mixer

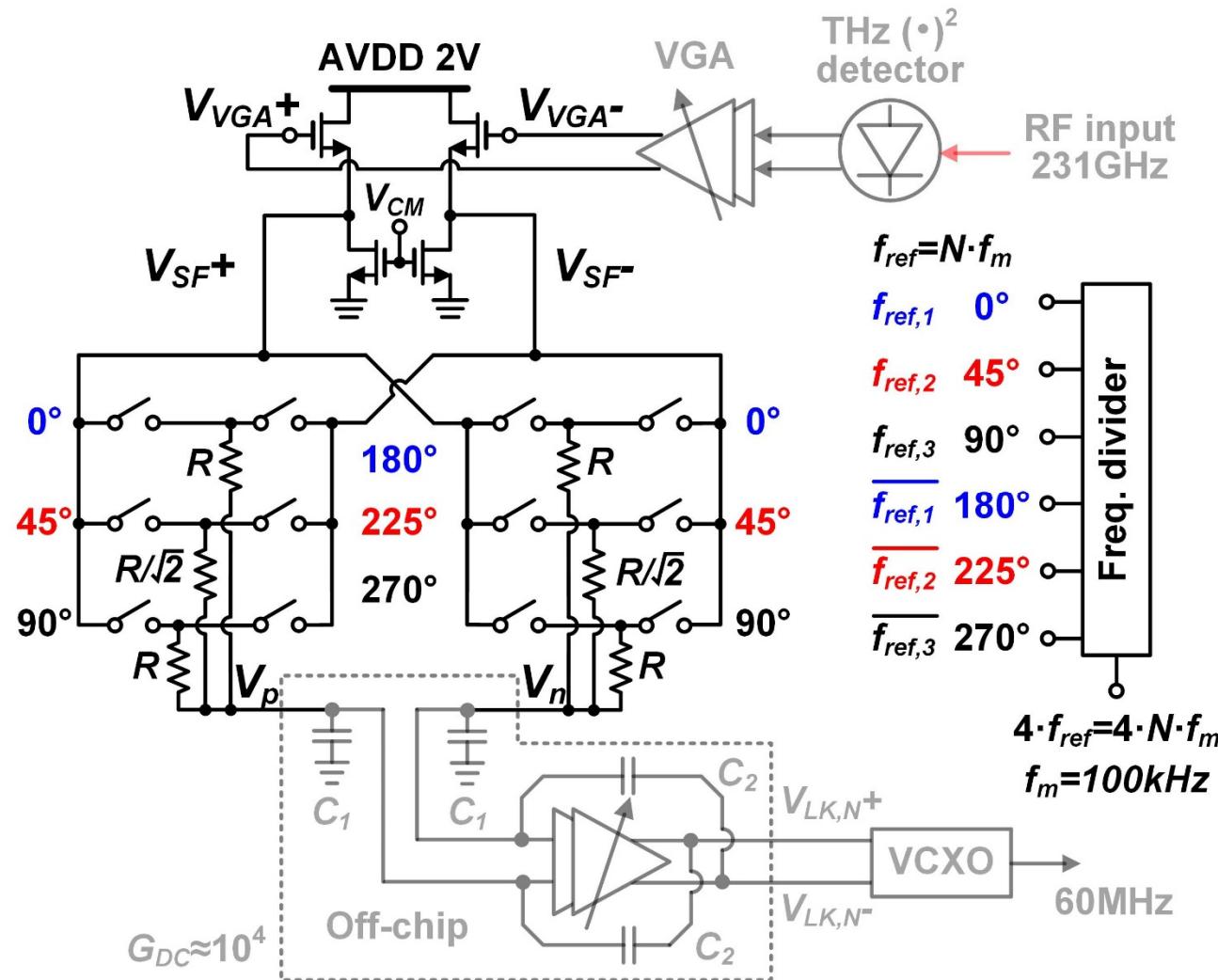


Conventional

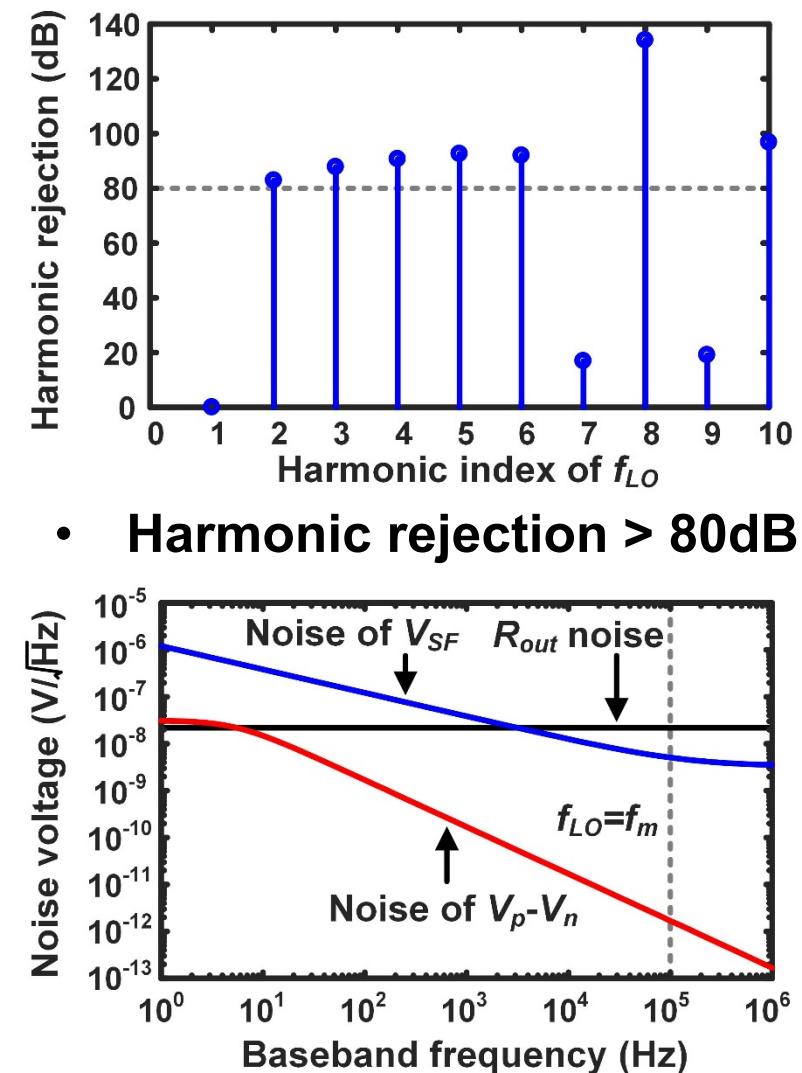
Proposed

- Convert  $N^{\text{th}}$  harmonic of  $f_m$  to DC
- Harmonic rejection of ref. clock  $f_{ref}$  for low interference and noise-folding
- Reduce flicker noise at DC output

# RX: Harmonic Rejection Lock-in Detector (HRLKD)

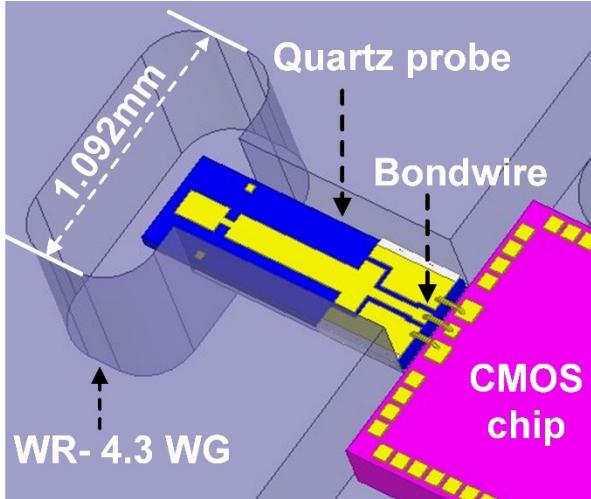


- DC offset  $V_p - V_n \approx 10\mu\text{V}$  ( $1\mu\text{V}$  change  $\rightarrow 10^{-10}$  drift)



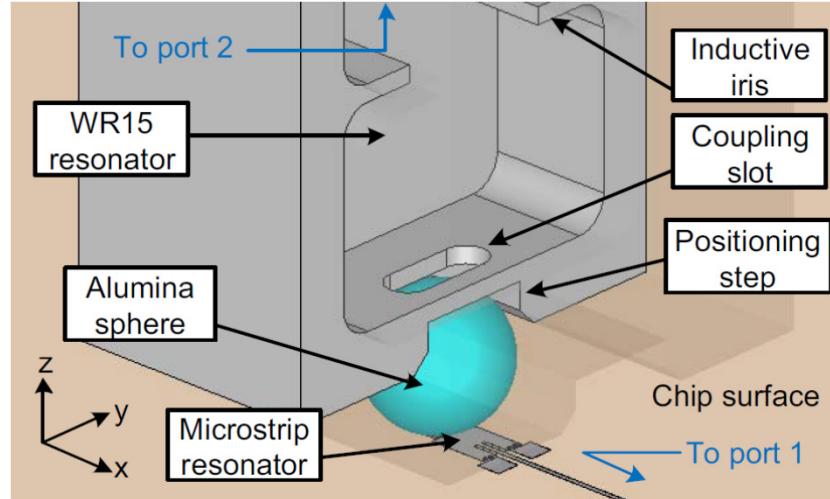
- Reduced DC flicker noise

# Chip-to-Waveguide Coupler



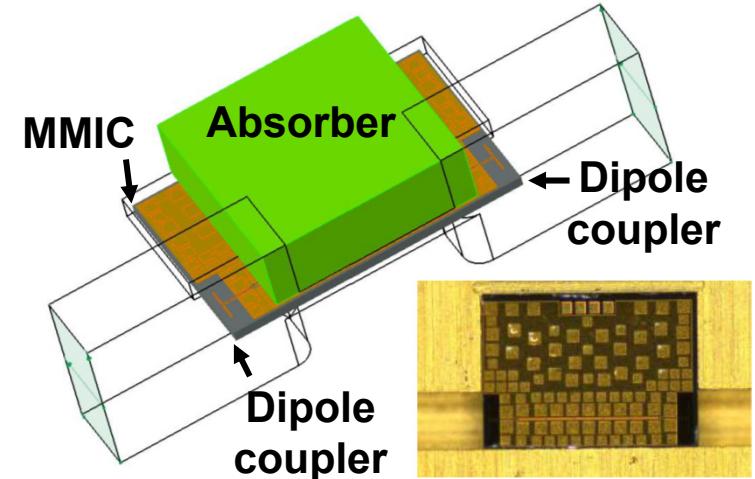
**E-plane quartz probe**

[C. Wang, et al., JSSC, 2018]



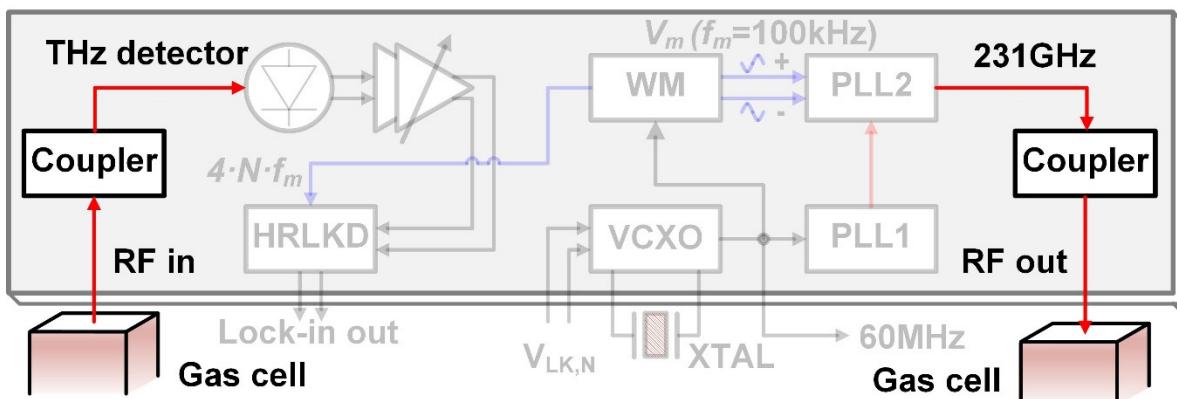
**Dielectric resonator**

[D. L. Cuenca, et al., EuMIC, 2017]



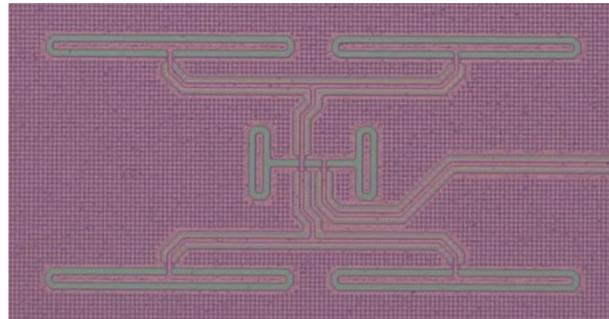
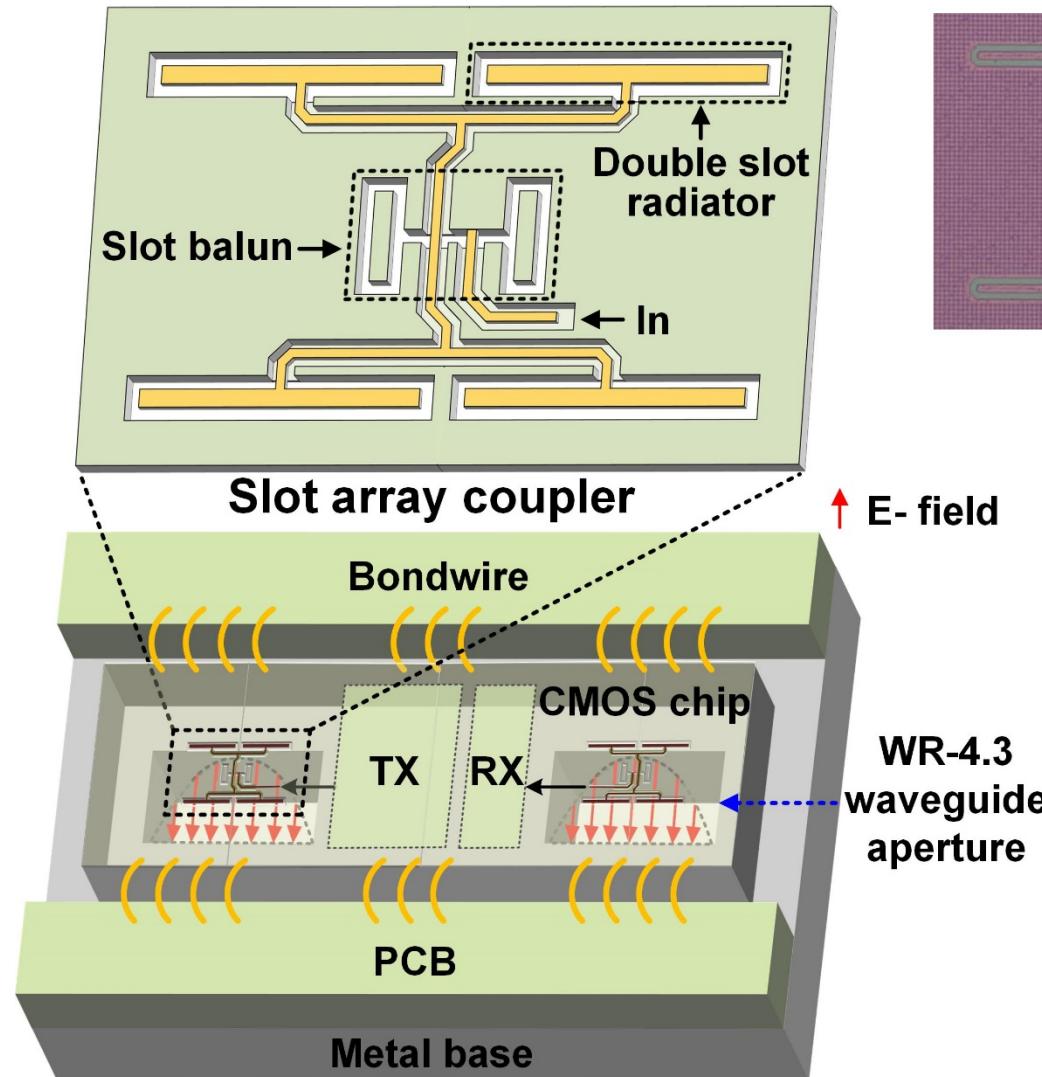
**Integrated dipole coupler**

[H. Song, et al., MWCL, 2016]

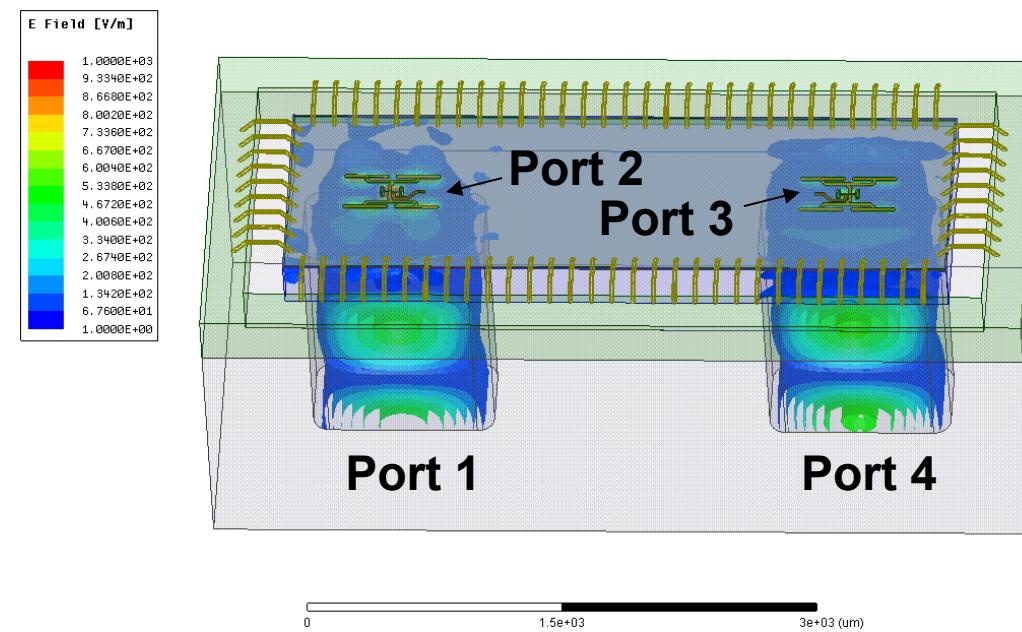


- Conventional designs
  - Costly external components
  - Special process/wafer thinning
  - Insufficient TRX isolation

# Slot Array Coupler: Architecture

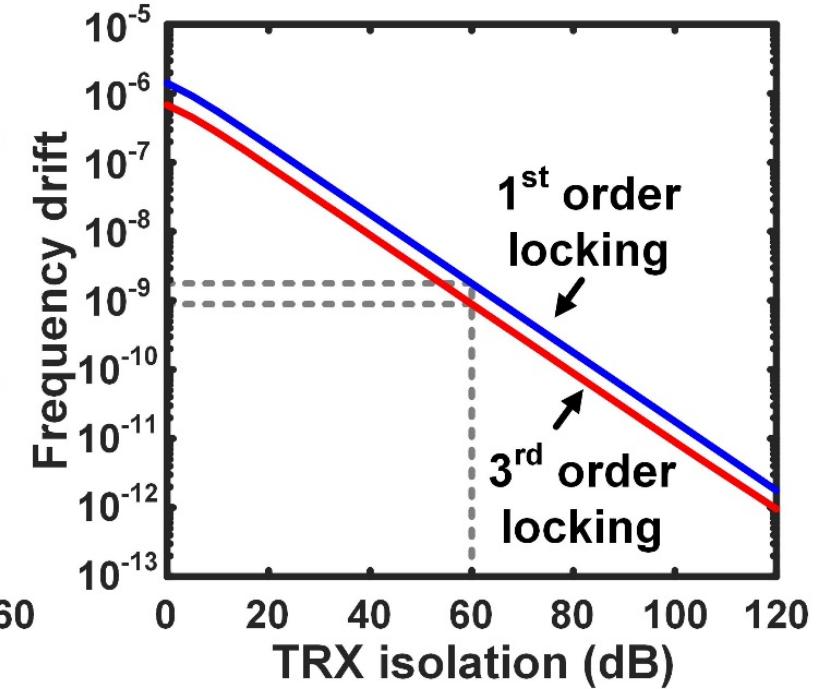
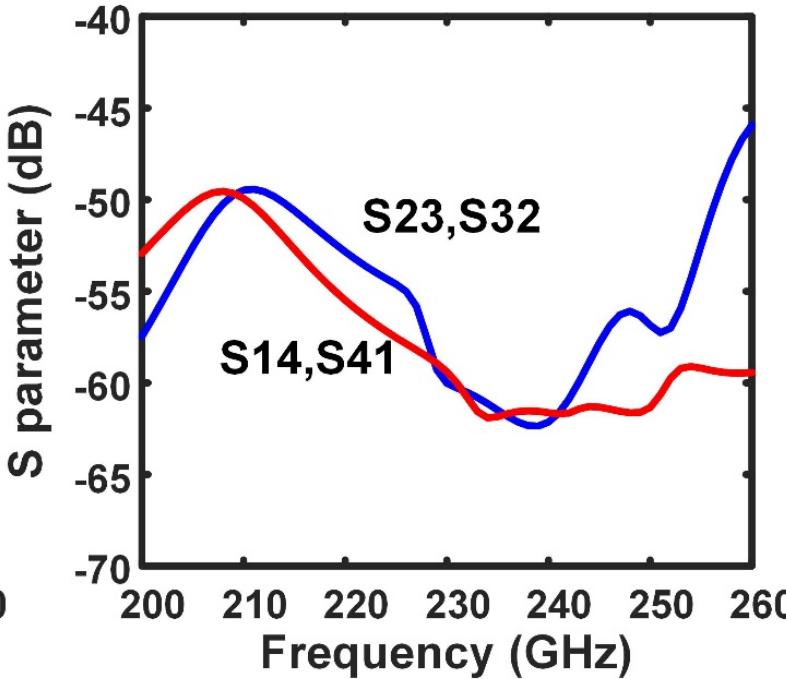
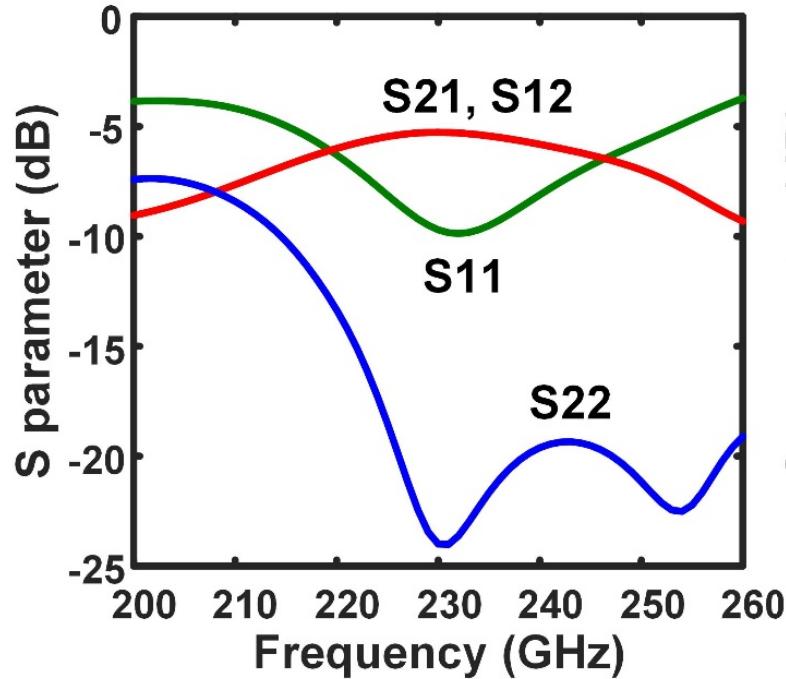


- Radiates downward into waveguide aperture through Si-substrate
- No external components
- No wafer thinning



Simulated E-field distribution

# Slot Array Coupler: Simulated Results



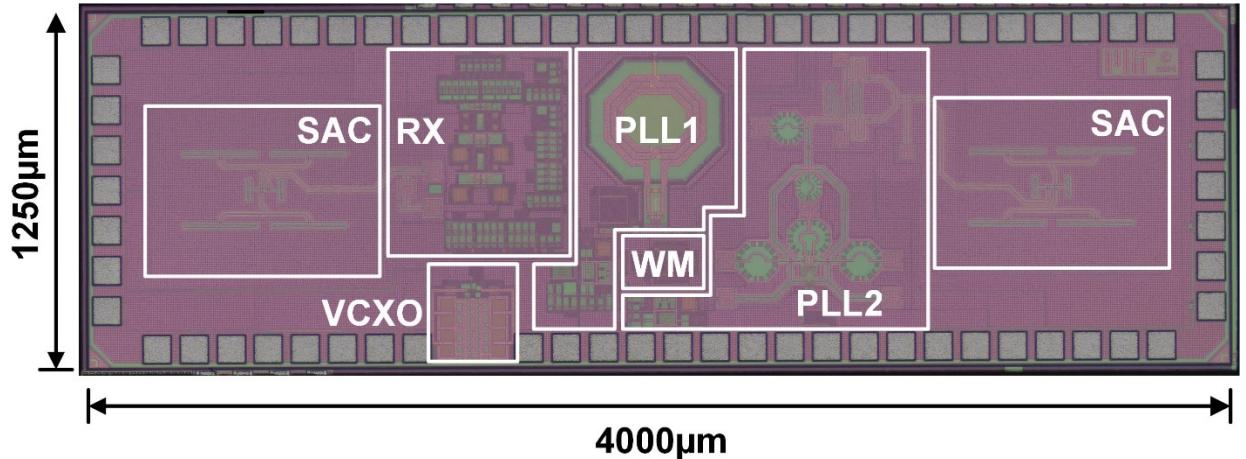
- Simulated loss = 5.2dB
- BW<sub>3dB</sub> = 21%
- 60dB simulated TX/RX isolation
- 10<sup>-9</sup> drift by 60dB isolation (removable w/ calibration)

# Outline

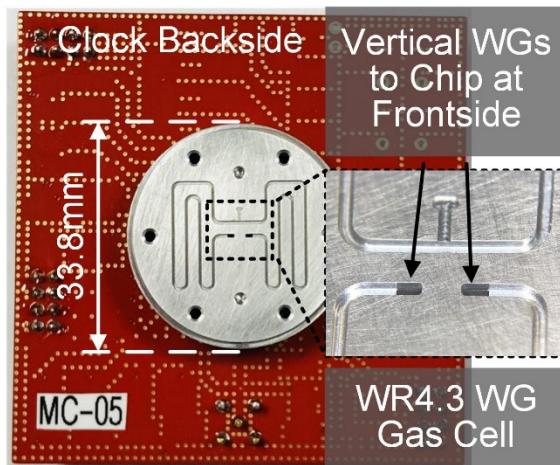
---

- Background
- High-order locking for long-term stabilization
- Architecture and circuit design
- **Measurement results**
- Conclusions

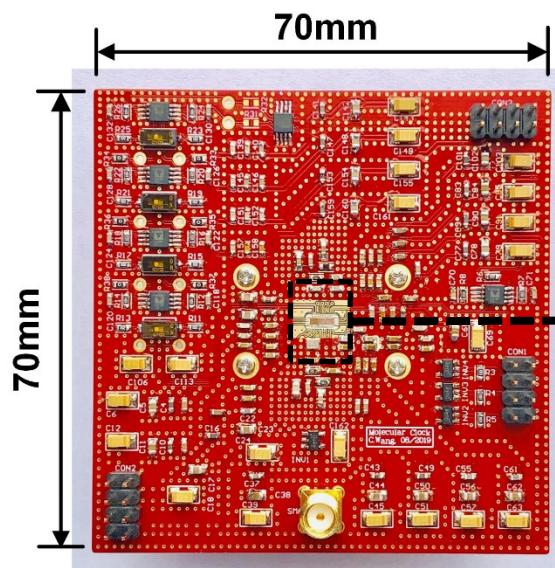
# Chip Photo and Packaging



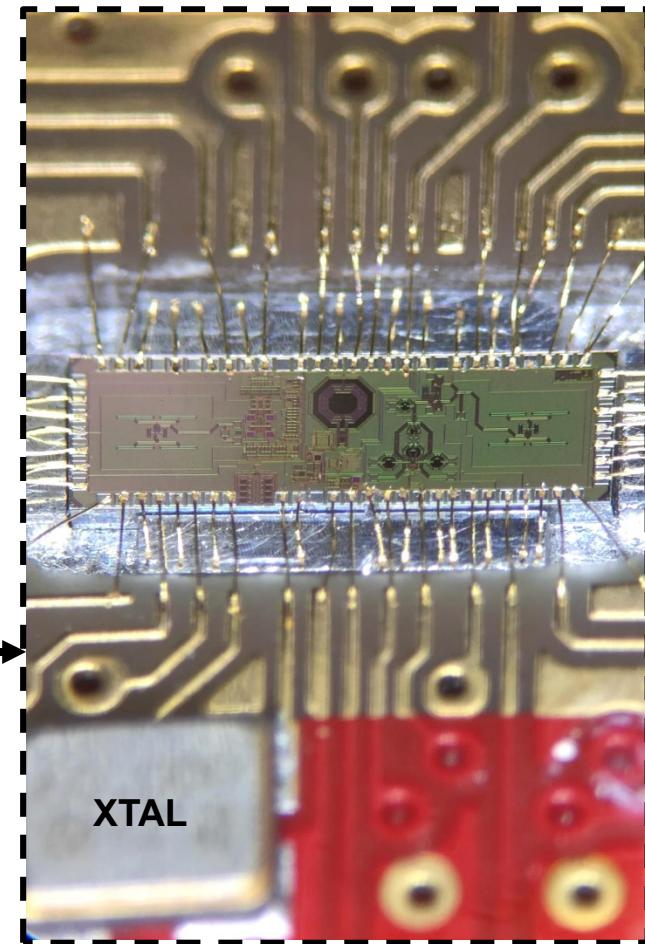
- TSMC 65nm CMOS process.



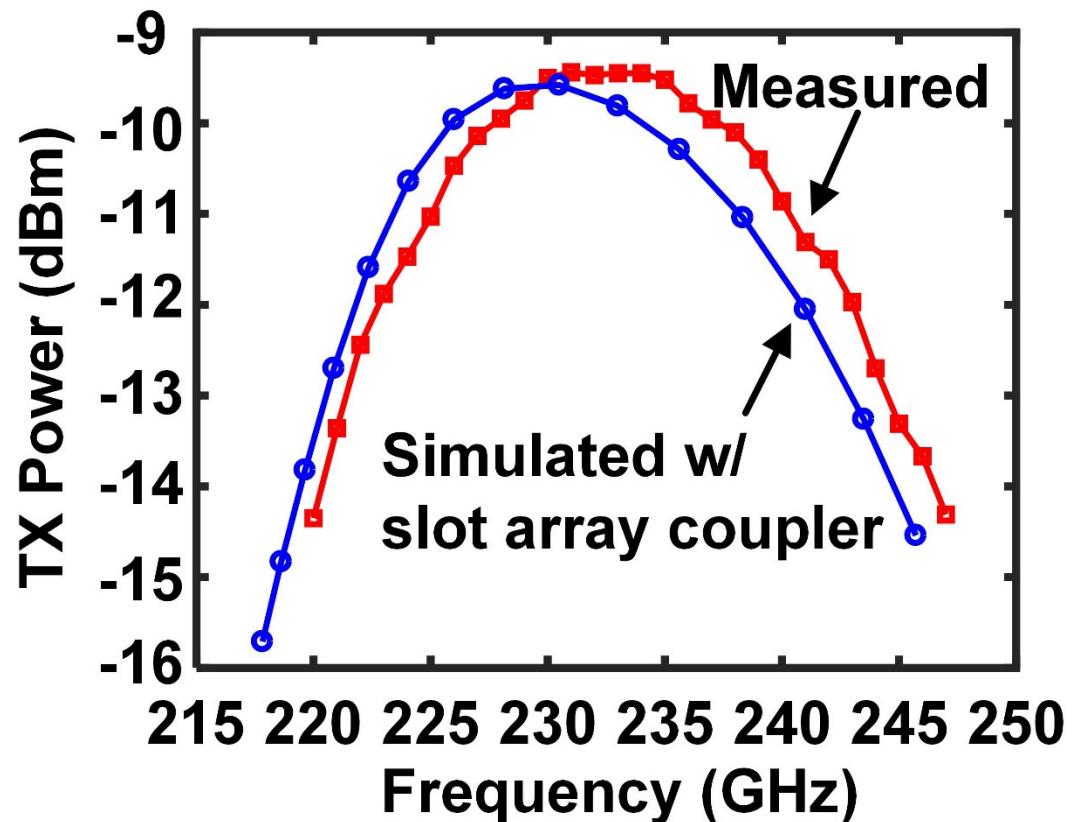
Molecular Cell (Cap Removed)



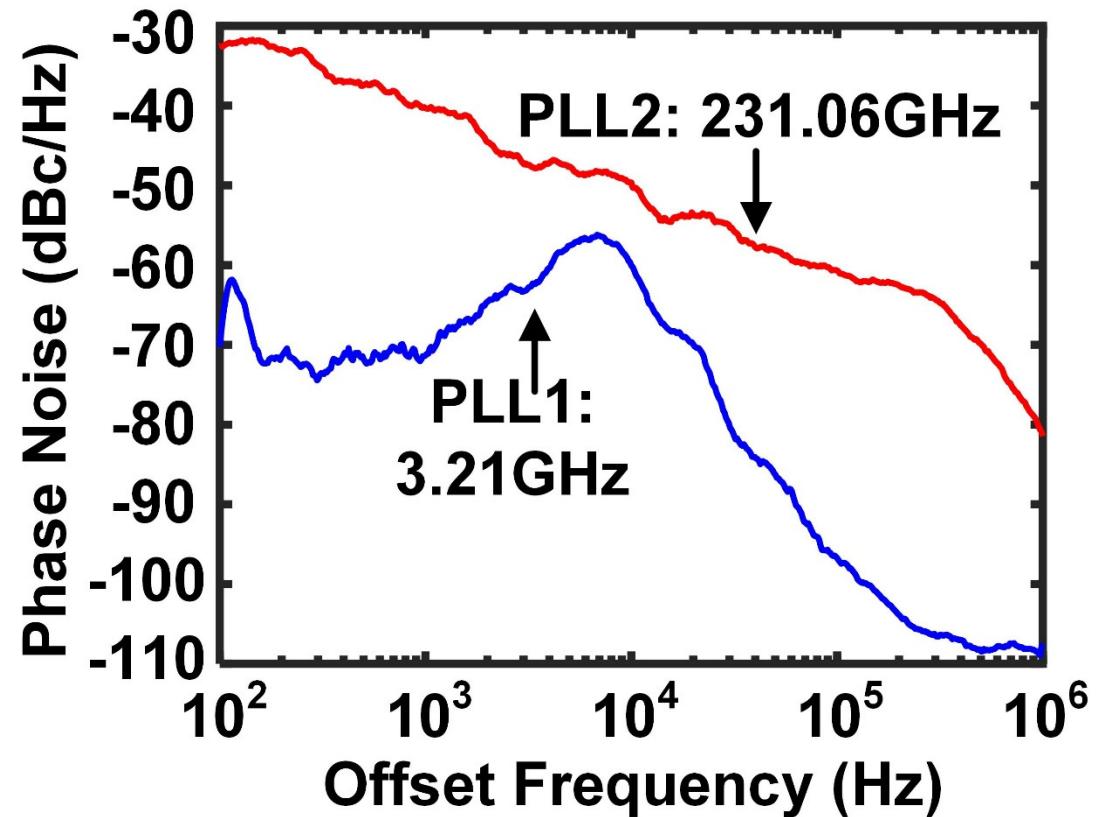
CMOS chip on PCB



# Measured RF Power and Phase Noise of TX

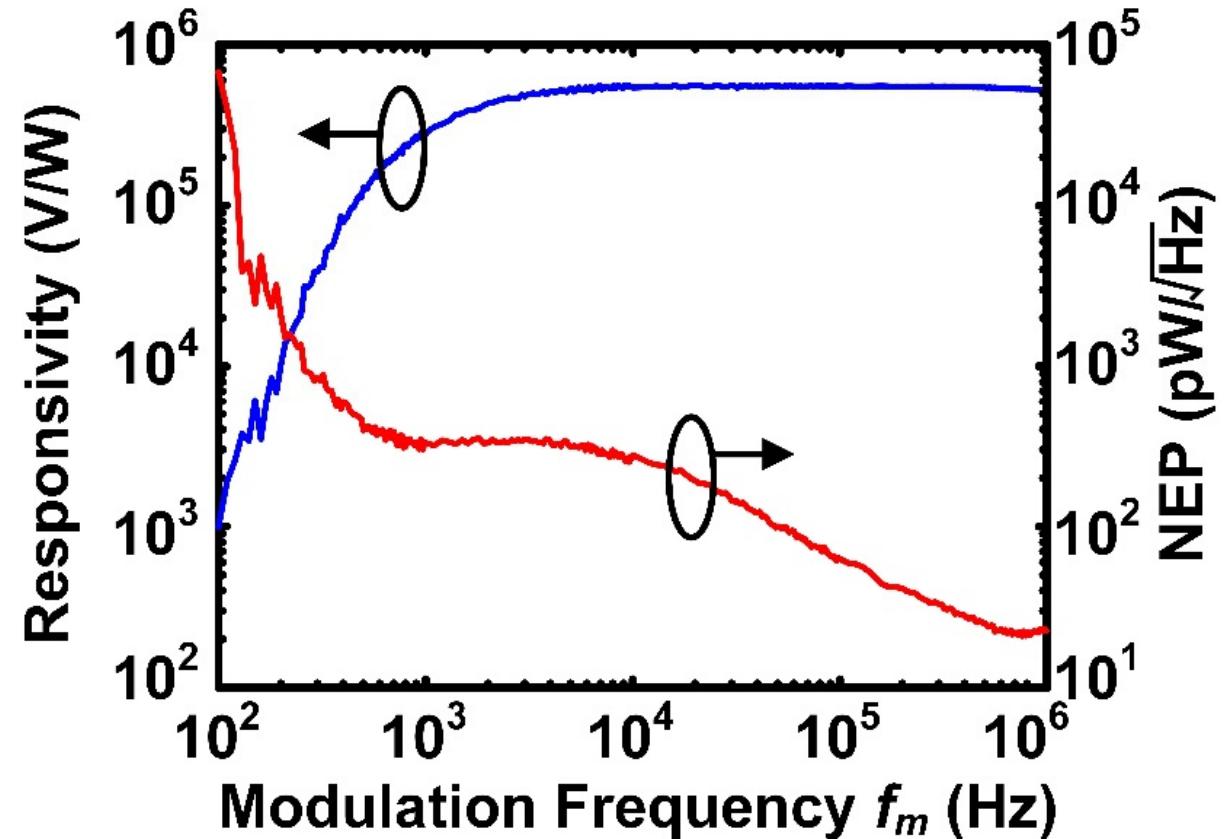
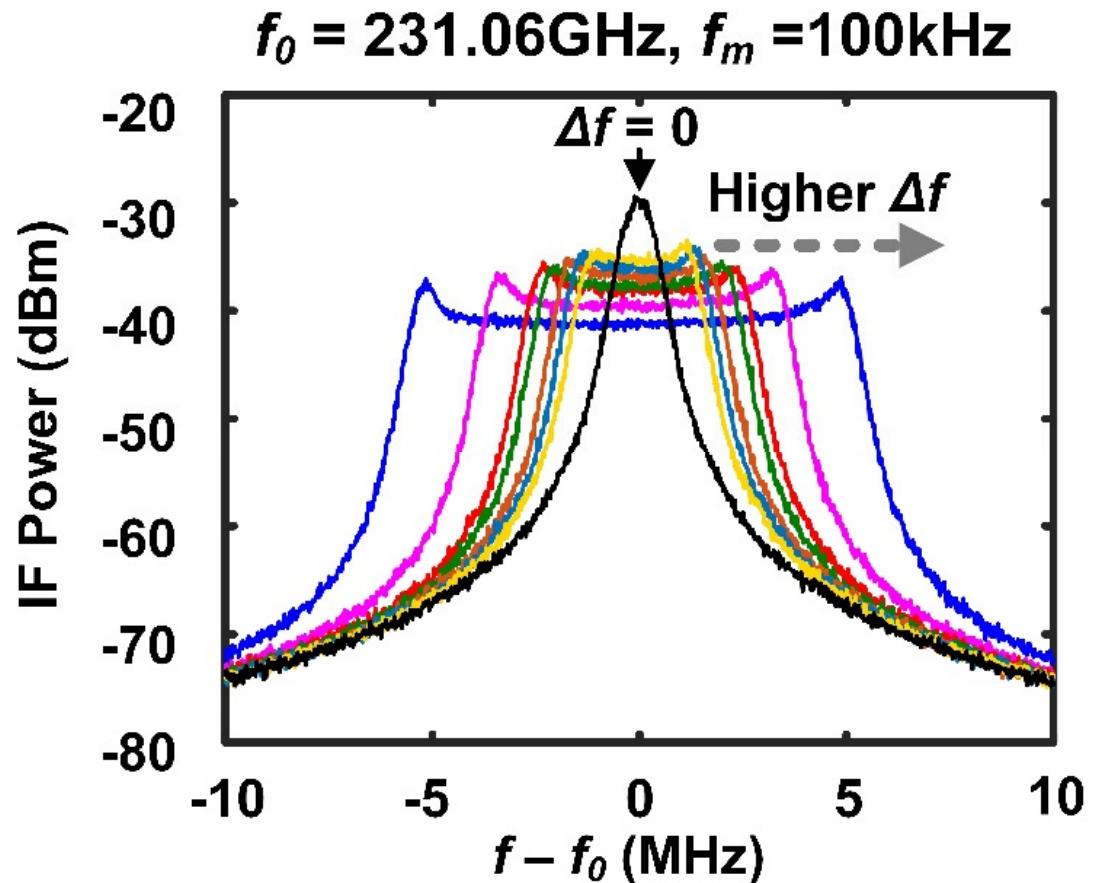


- $P_{RF} = -9.4\text{dBm}$  w/ slot array coupler
- PLL bandwidth: 27GHz (12%)



- Phase noise :  $-81.5\text{dBc/Hz}$ @1MHz
- PM-to-AM noise  $\rightarrow SNR_{PN} = 84\text{dB}$

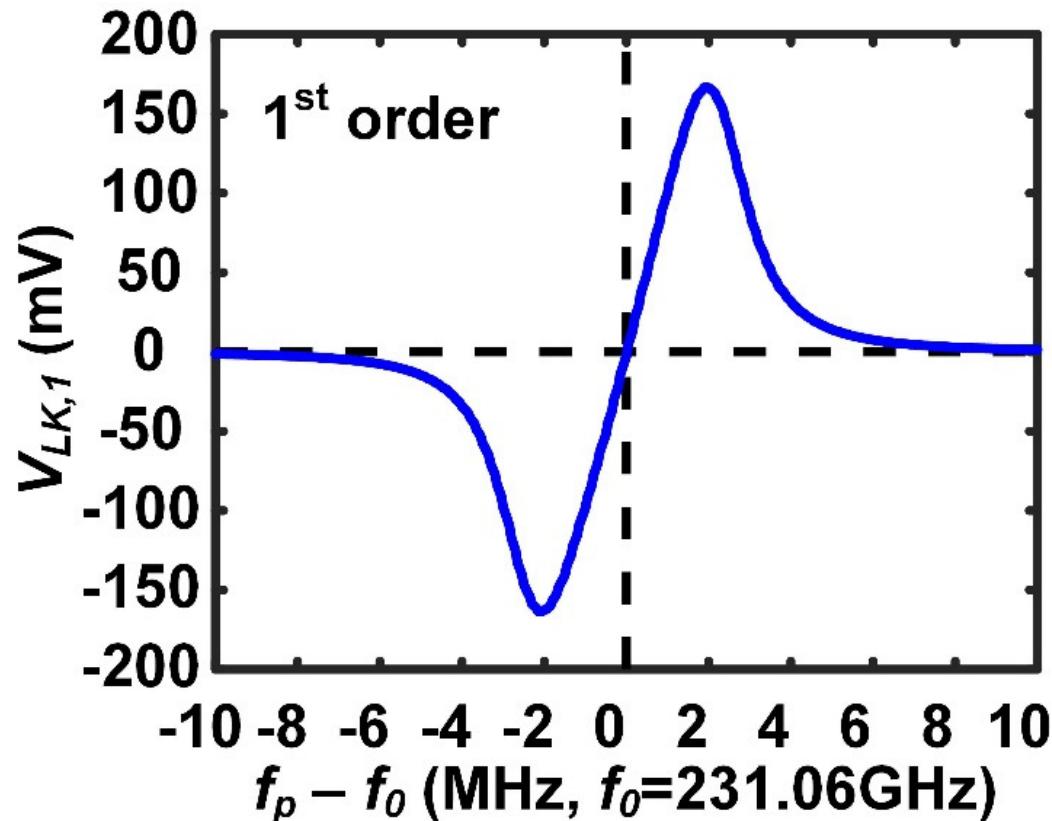
# Measured WMS Spectrum and RX Performance



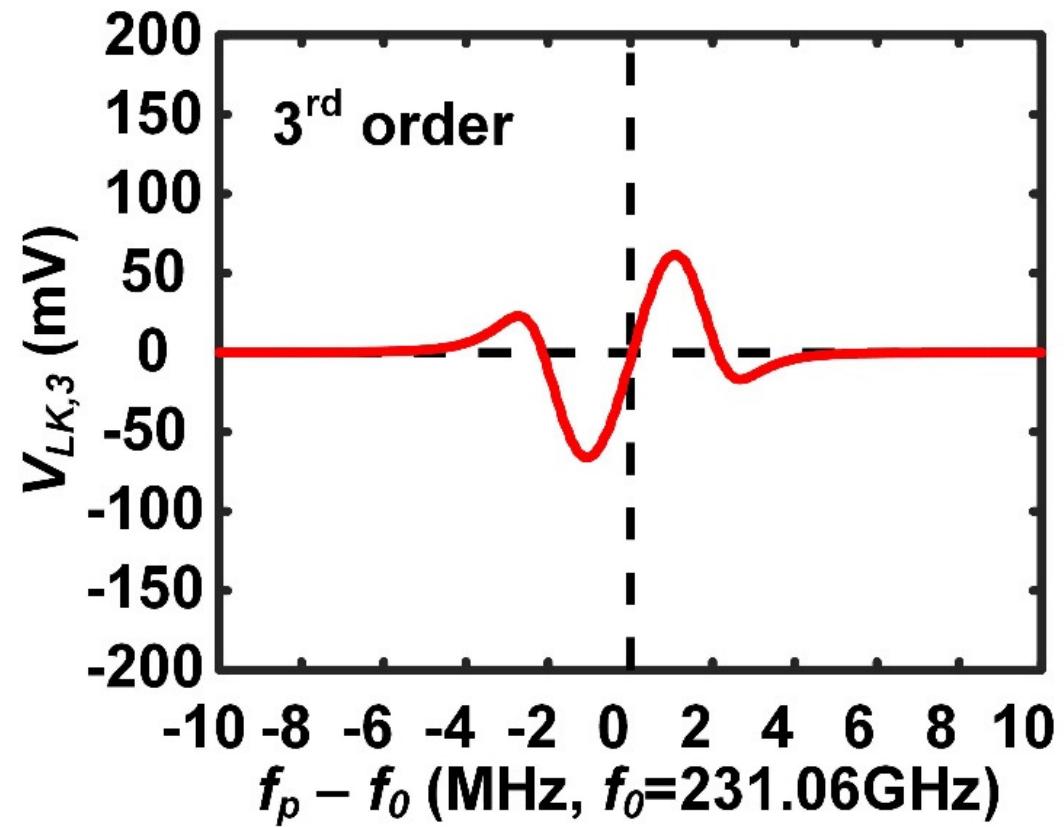
- Spectrum of TX probing signal with wavelength modulation

- NEP of RX w/ slot array coupler:  
 $62.8 \text{ pW}/\sqrt{\text{Hz}}$  at  $f_m = 100\text{kHz}$

# Measured Dispersion Curves and Allan Deviation

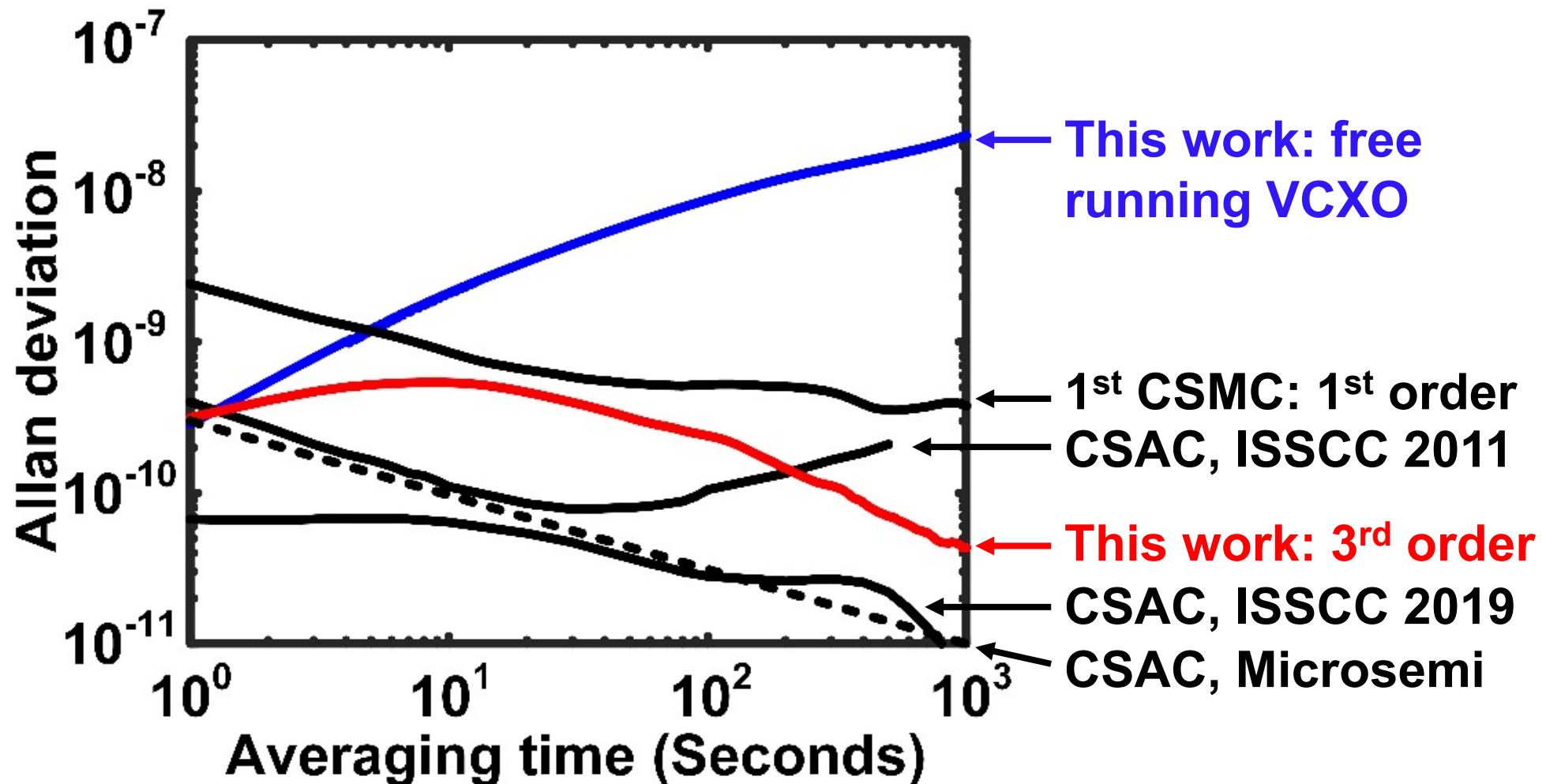


- 1<sup>st</sup> order curve: SNR = 84dB
- $V_{Offset} = 1.1\text{mV}$



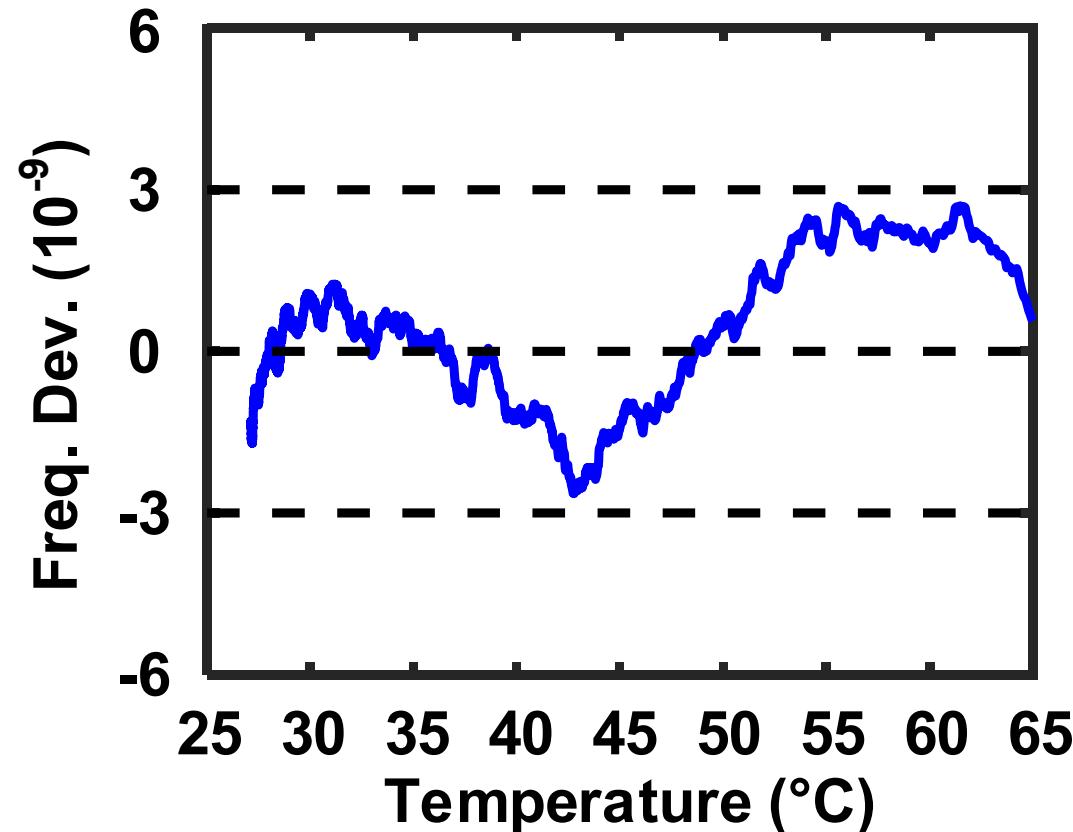
- 3<sup>rd</sup> order curve: SNR = 66dB
- $V_{Offset} = 4.3\mu\text{V}$  (256× smaller)

# Measured Allan Deviation by 3<sup>rd</sup> Order Locking

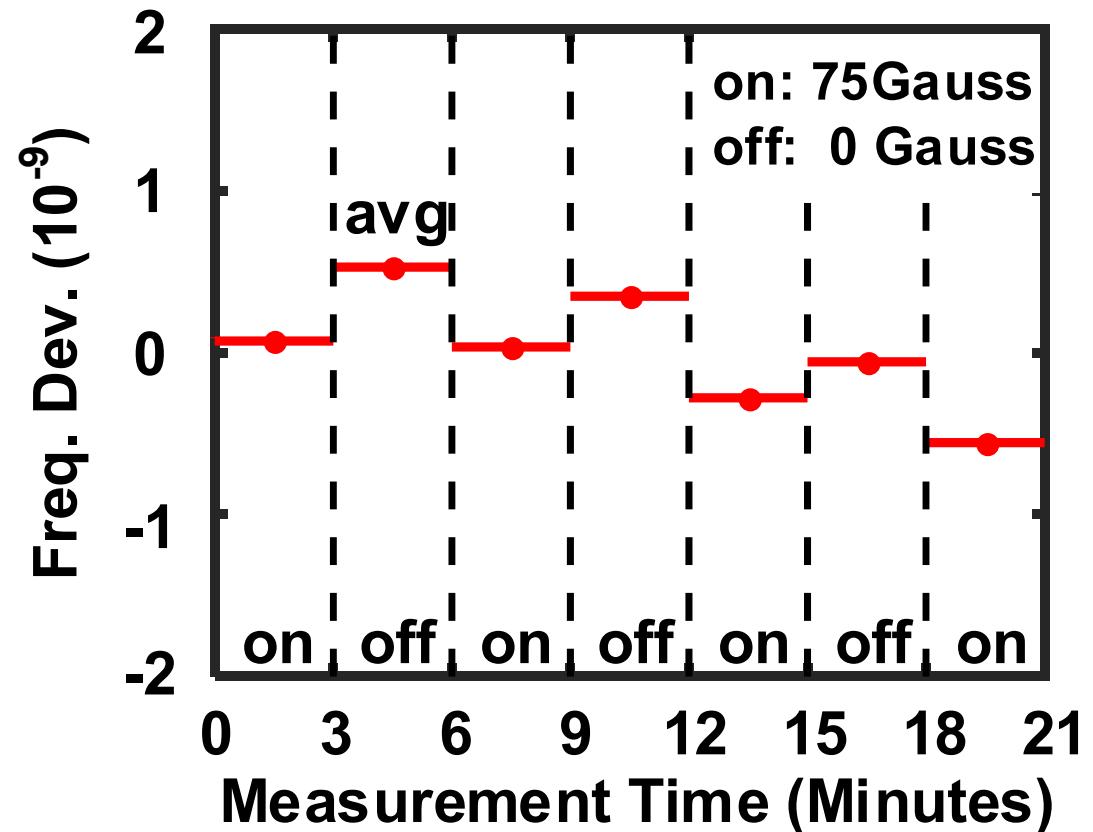


- Allan deviation:  $\sigma_y = 3.2 \times 10^{-10}$  @  $\tau = 1s$ ,  $4.3 \times 10^{-11}$  @  $\tau = 10^3s$

# Measured Temperature and Magnetic Sensitivity



- Drift  $< \pm 3 \times 10^{-9}$  in 27~65  $^{\circ}\text{C}$  w/ 2<sup>nd</sup> order temperature compensation



- Drift  $< \pm 2.9 \times 10^{-12}/\text{Gauss}$  w/o magnetic shield in CSAC

# Outline

---

- **Background**
- **High-order locking for long-term stabilization**
- **Architecture and circuit design**
- **Measurement results**
- **Conclusions**

# Performance Comparison Table

Parameters	SiTime [1]	Microsemi [3]	ISSCC2019 [4]	VLSI2018 [5]	This work
Mechanism	OCXO	$^{133}\text{Cs}$ CSAC	$^{133}\text{Cs}$ CSAC	$^{16}\text{O}^{12}\text{C}^{32}\text{S}$ MC	$^{16}\text{O}^{12}\text{C}^{32}\text{S}$ MC
Cost	Medium	High	High	Low	Low
Freq. (GHz)	0.06	4.6	4.6	231.061	231.061
Harmonics	N/A	1 <sup>st</sup> order	1 <sup>st</sup> order	1 <sup>st</sup> order	3 <sup>rd</sup> order
$\sigma_y (\tau=10^0\text{s})$	$3.0 \times 10^{-11}$	$3.0 \times 10^{-10}$	$8.4 \times 10^{-11}$	$2.4 \times 10^{-9}$	$3.2 \times 10^{-10}$
$\sigma_y (\tau=10^3\text{s})$	$4.0 \times 10^{-11}$	$1.0 \times 10^{-11}$	$0.8 \times 10^{-11}$	$3.8 \times 10^{-10}$	$4.3 \times 10^{-11}$
Temp. Drift <sup>a</sup>	$\pm 5.0 \times 10^{-9}$	$\pm 5.0 \times 10^{-10}$	$< \pm 1.0 \times 10^{-9}$	N/A	$\pm 3.0 \times 10^{-9}$
Mag. Sens. <sup>b</sup>	N/A	$\pm 9.0 \times 10^{-11}$	N/A	N/A	$\pm 2.9 \times 10^{-12}$
$T_{start-up}$ (s)	120	180	N/A	<1	<1
$P_{DC}$ (mW)	600	120	60	66	70

a. Measured temp. range: [1]: -20~70°C;  
[2], [3]: -10~70°C; This Work: 27~65°C;

b. Unit: Gauss<sup>-1</sup>.

[1] SiTime, *SiT5711*, 2019; [2] D. Ruffieux, *ISSCC*, 2011;  
[3] Microsemi, *SA.45s*, 2019; [4] H. Zhang, *ISSCC*, 2019;  
[5] C. Wang, *VLSI*, 2018.

# Acknowledgement

---

- This work is supported by National Science Foundation (CAREER ECCS-1653100 and ECCS-1809917), MIT Lincoln Lab, and a Texas Instruments Fellowship;
- The authors acknowledge Dr. Stephen Coy, Prof. Keith Nelson, and Prof. Robert Field of MIT for technical discussions and assistance;
- We appreciate the help from Qingyu (Ben) Yang on the experiments.



# A 660-676GHz 4x2 Oscillator-Radiator Array with Intrinsic Frequency Filtering Feedback for Harmonic Power Boost Achieving 7.4dBm EIRP in 40nm CMOS

Gabriel Guimarães, Patrick Reynaert  
KU Leuven, Belgium

