

A 605GHz 0.84mW Harmonic Injection-Locked Receiver Achieving $2.3\text{pW}/\sqrt{\text{Hz}}$ NEP in 28nm CMOS

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Self introduction

- Born in Bornem, Belgium, in 1995
- B.Sc. (2016) and M.Sc. (2018) degrees in electronics engineering from KU Leuven, Leuven, Belgium
- Since 2018: Research Assistant at MICAS, KU Leuven
 - Working towards Ph.D. degree
- Research interests: CMOS THz electronics for imaging and sensing applications



Outline

- **Introduction**
 - THz imaging in CMOS
 - Harmonic injection locking
- Proposed Harmonic Injection-Locked Receiver
- Measurements
- Conclusion

THz imaging in CMOS

Benefits

Resolution ~ frequency

Non-ionizing | Ionizing

Frequency	1THz	UV	X-ray 
Photon energy	4.1m eV	3-124 eV	124-124k eV

Dielectric contrast

$\lambda \downarrow \rightarrow$ integration on-chip

Low cost

Integration with digital logic

High yield

Applications

Challenges

THz imaging in CMOS

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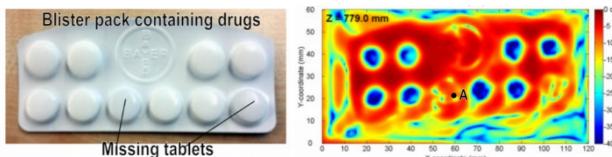
Low cost

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Applications

Inspection



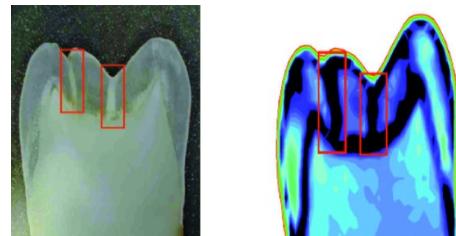
U. Pfeiffer, 2016

Security



NIST, 2017

Medical



D. Arnone, 2001

Challenges

THz imaging in CMOS

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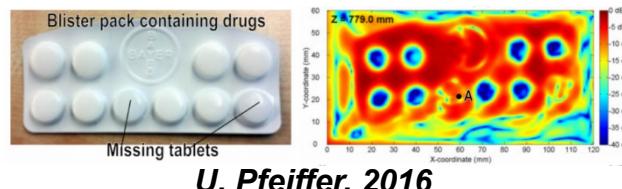
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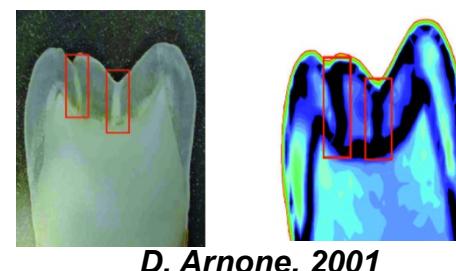
Inspection



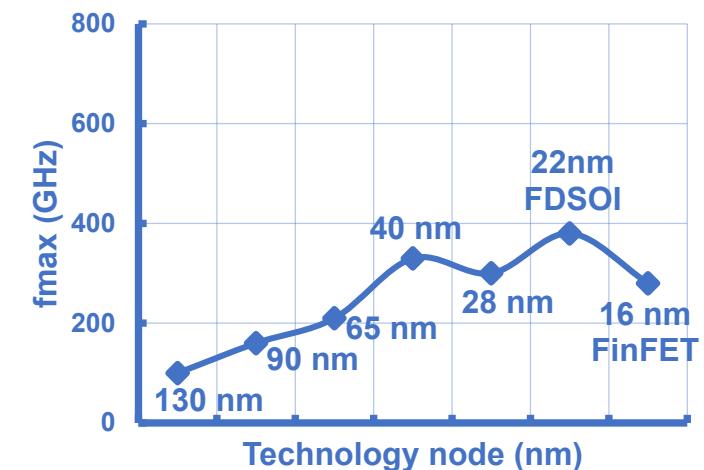
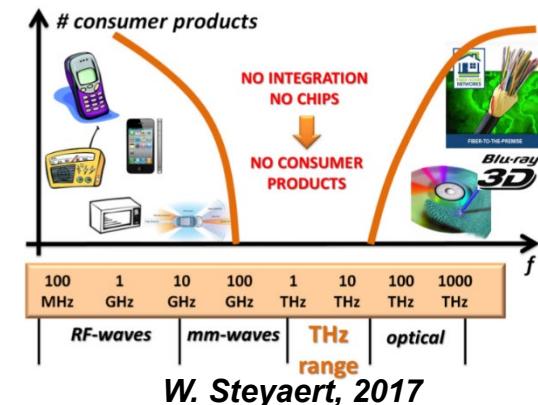
Security



Medical

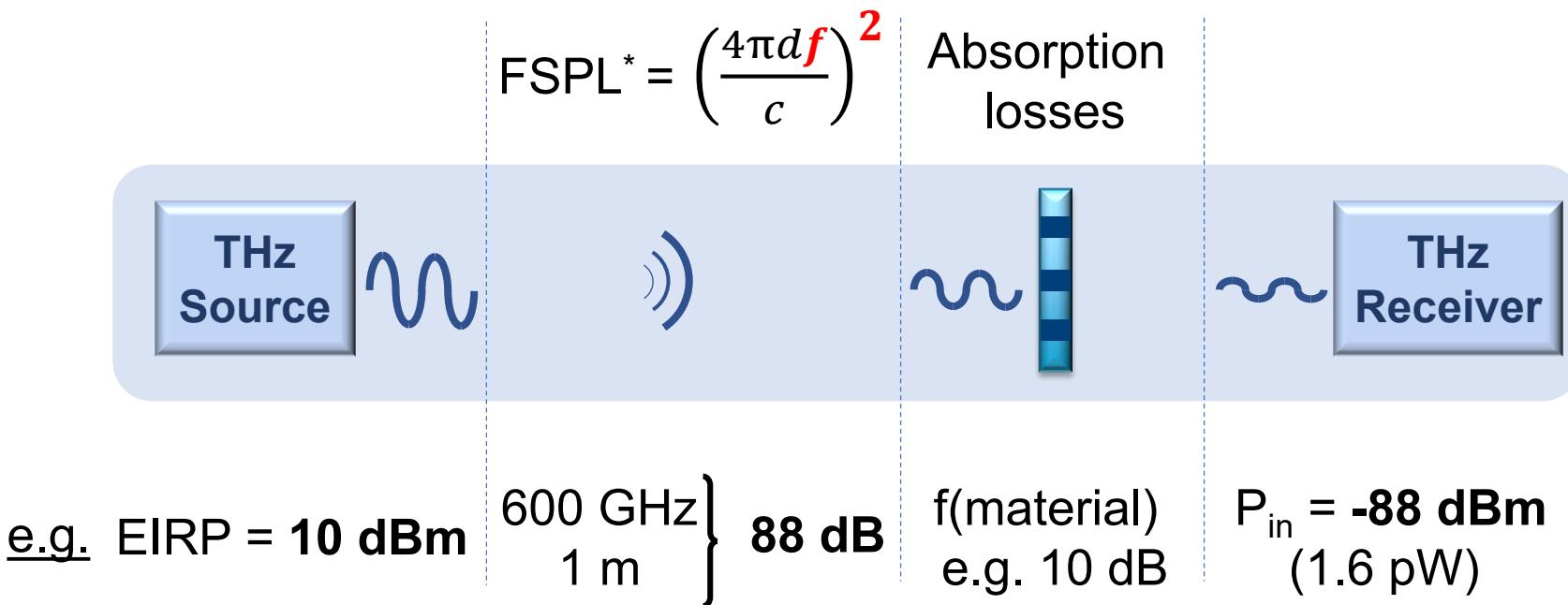


Challenges



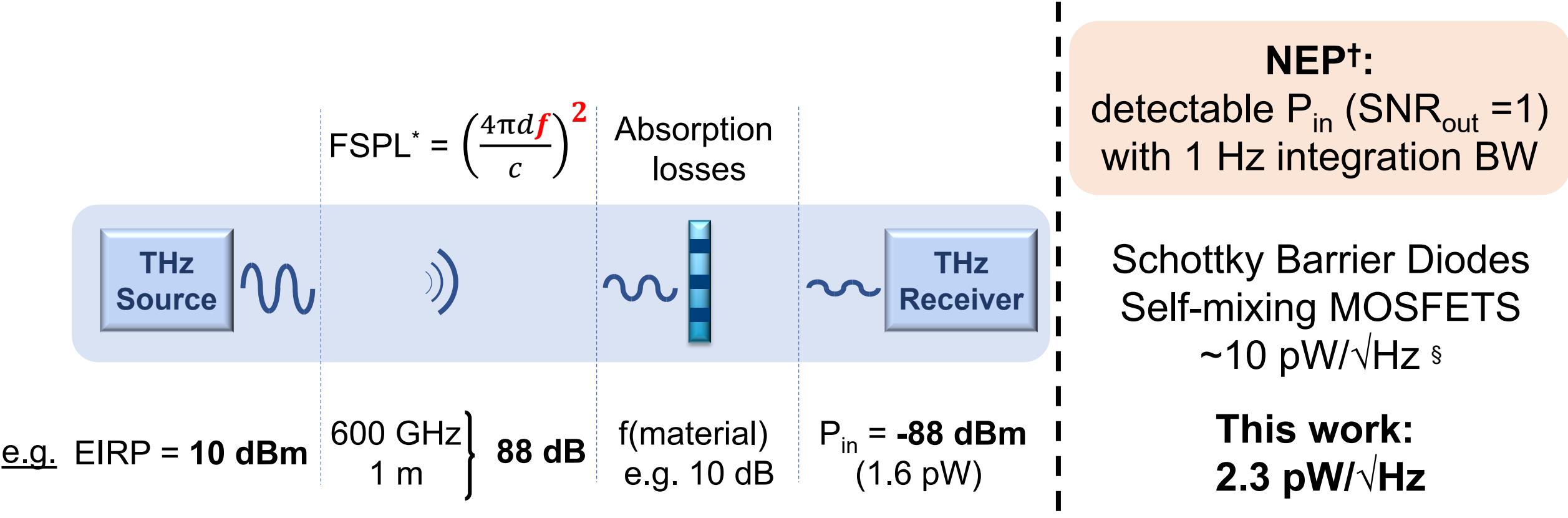
23.3: A 605 GHz 0.84 mW Harmonic Injection-Locked Receiver Achieving 2.3 pW/Hz NEP in 28 nm CMOS

THz imaging in CMOS



* Free Space Path Loss

THz imaging in CMOS



* Free Space Path Loss

† Noise Equivalent Power

Schottky Barrier Diodes
Self-mixing MOSFETS
 $\sim 10 \text{ pW}/\sqrt{\text{Hz}}$ §

This work:
 $2.3 \text{ pW}/\sqrt{\text{Hz}}$

§ Kim, 2016; Han, 2013;
Öjefors, 2010; Pfeiffer, 2013;
Jain, 2018.

Outline

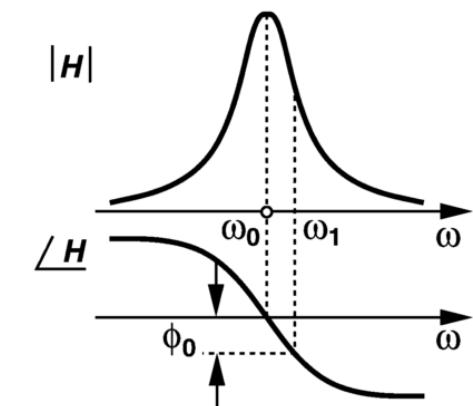
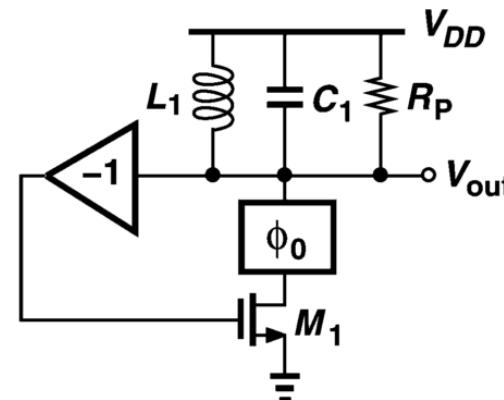
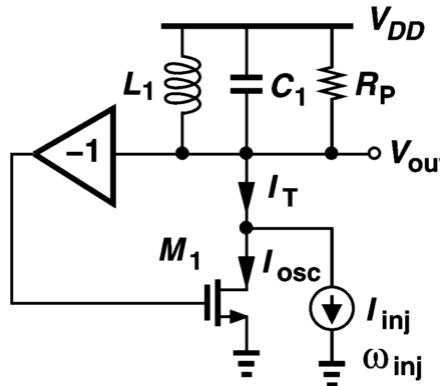
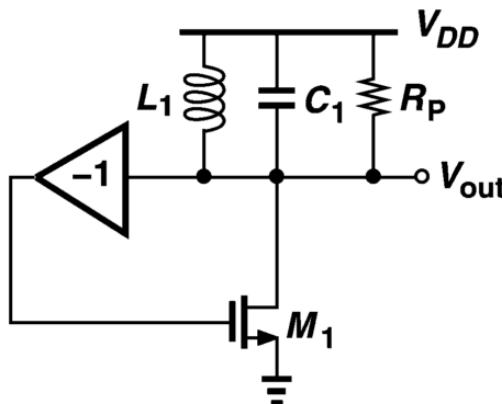
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 - THz imaging in CMOS
 - **Harmonic injection locking**
- Proposed Harmonic Injection-Locked Receiver
- Measurements
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Injection locking

Synchronization of pendulum clocks: ‘an odd sympathy’ - Huygens (1665)



Injection locking in LC tanks (Razavi,2004):



Harmonic injection locking

Locking to $f_{in} \sim f_0$, but also to $f_{in} \sim \frac{M}{N} \times f_0$ (M,N: integers)

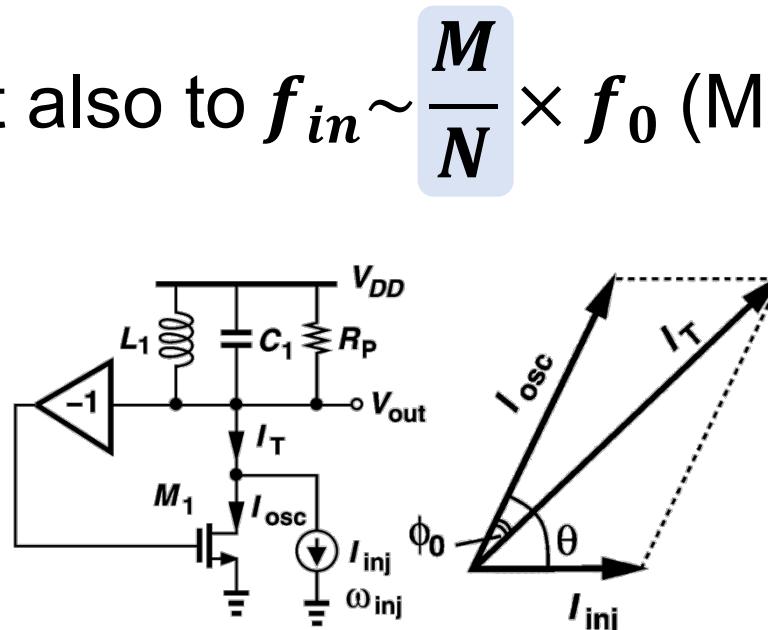
Applications:

Clock recovery

Synchronization

Demodulation:

Locking changes phase **and amplitude** of oscillation



$$I_T = \sqrt{I_{inj}^2 + I_{osc}^2 + 2I_{inj}I_{osc}\cos\theta}$$

$$\omega_{ILO} - \omega_{inj} = \frac{\omega_{ILO}}{2Q} \frac{I_{inj}\sin\theta}{I_{osc} + I_{inj}\cos\theta}$$

[Hajimiri 2019]

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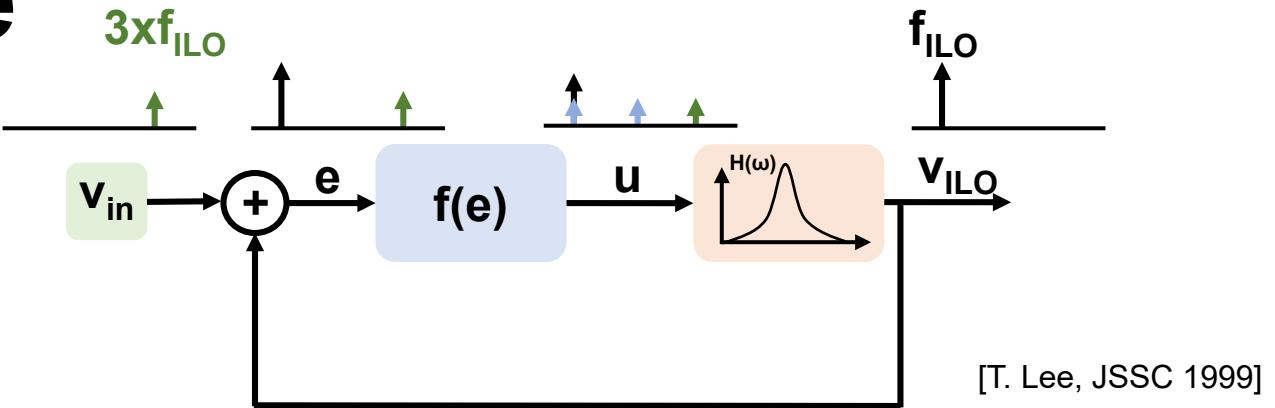
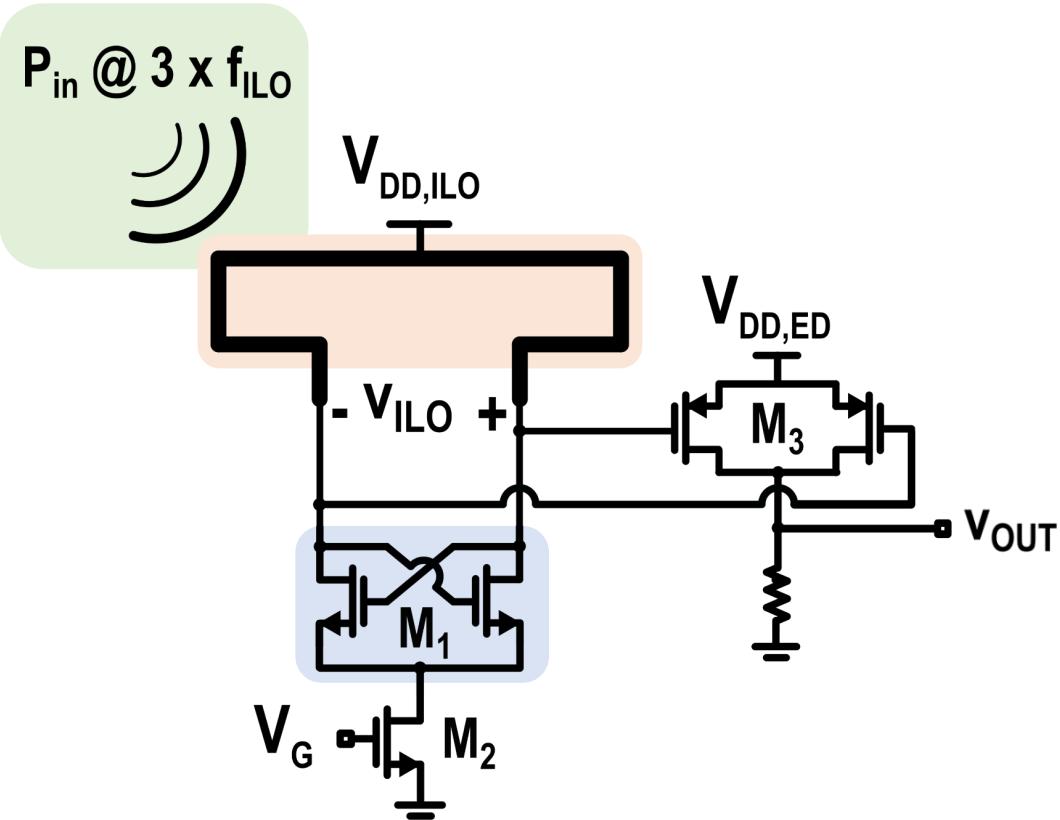
Above- f_{max} power detection



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Proposed receiver – working principle



Resulting fundamental oscillation amplitude:

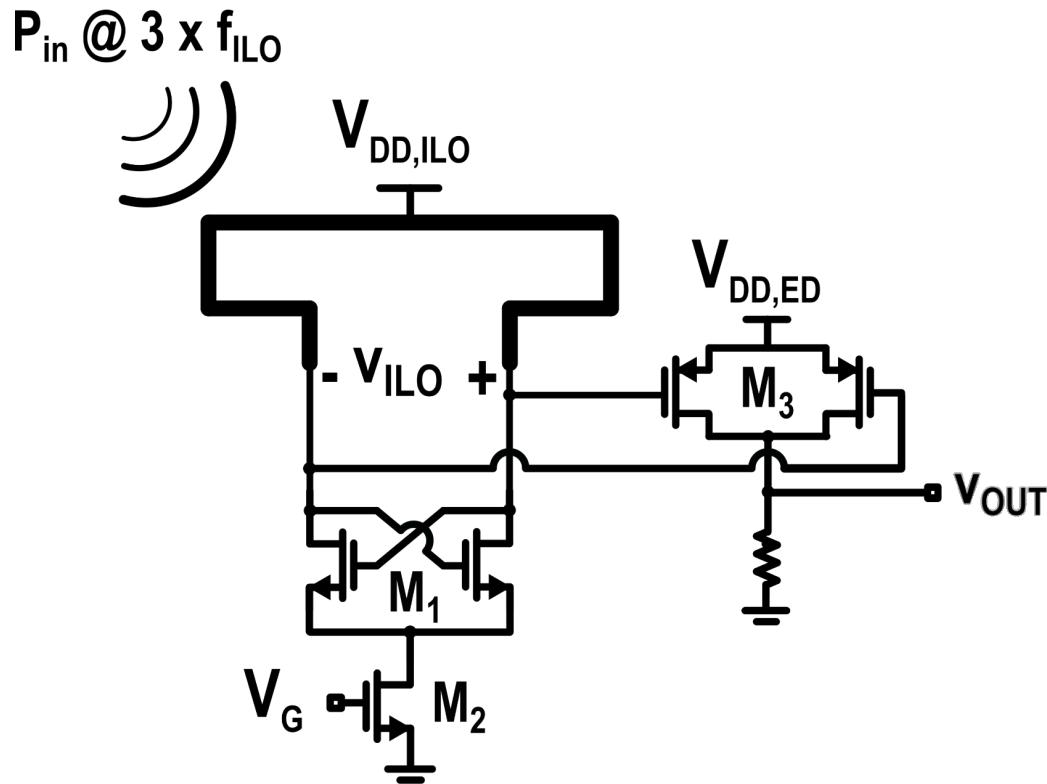
$$V_{ILO} = H_0 \left[K_{0,1} + \frac{1}{2} \sum_{m=1}^{\infty} K_{m,Nm\pm 1} \cos(m\theta) \right]$$

Lock characteristic:

$$2V_{ILO}Q \frac{\Delta\omega}{\omega_0} = \frac{H_0}{2} \sum_{m=1}^{\infty} K_{m,Nm\pm 1} \cos(m\theta)$$

$K_{m,n}$: intermodulation coefficient for $m\omega_{in}$, $n\omega_0$

Proposed receiver – advantages



Weak P_{in} @ $f > f_{max}$

~~mixer-first~~

Intermodulation in M_1 pair: area ✓

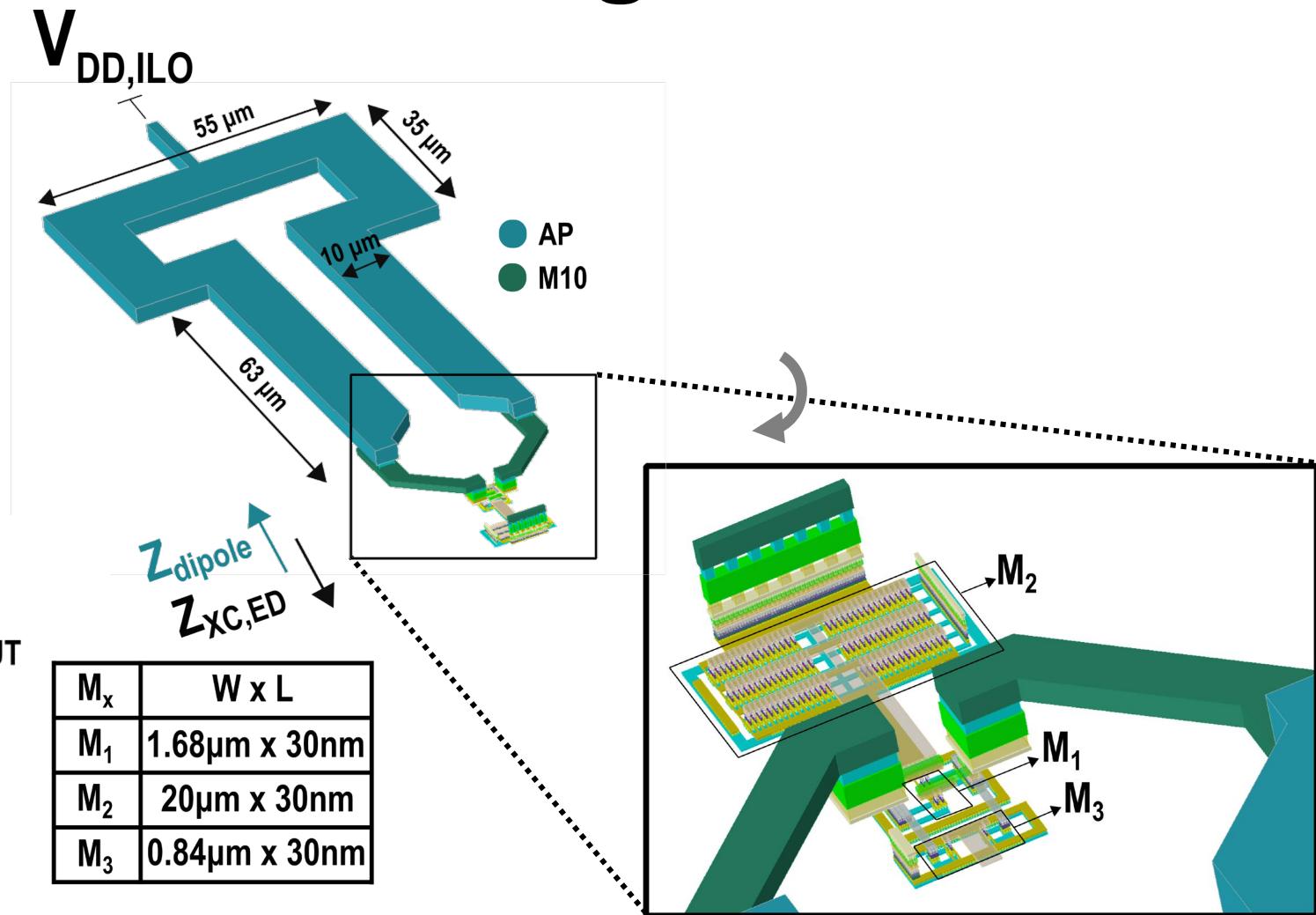
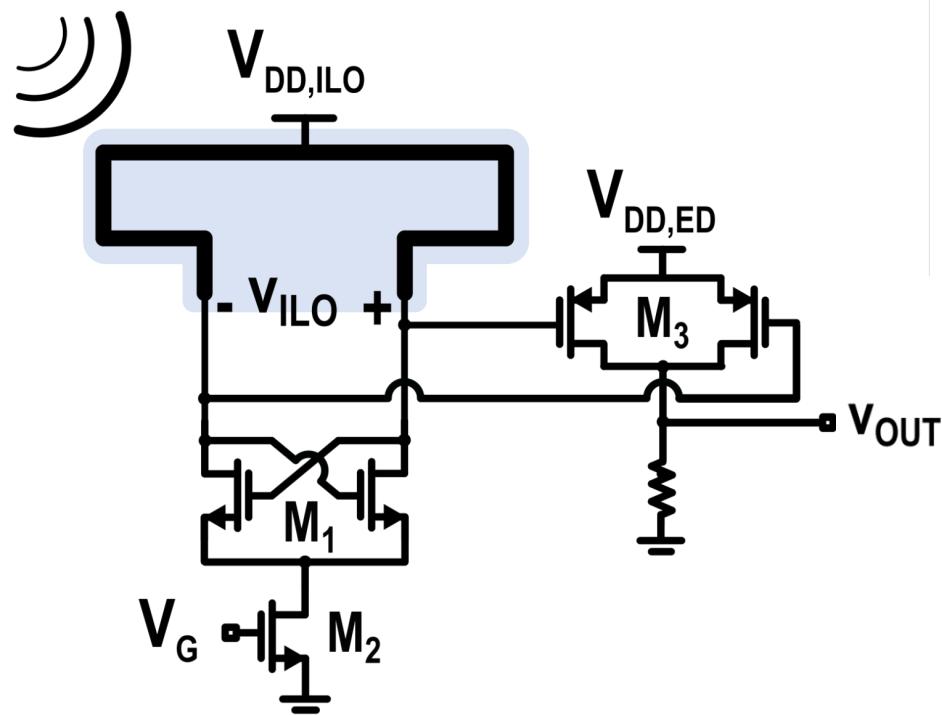
~~amplification stages~~

**Filtered (extremely high Q)
and amplified (oscillator feedback)
in oscillator itself: area, P_{DC} ✓**

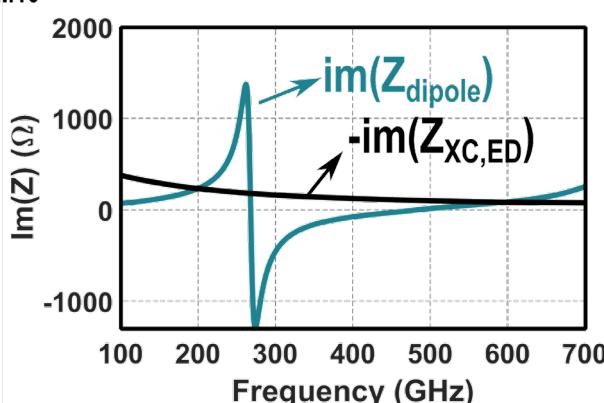
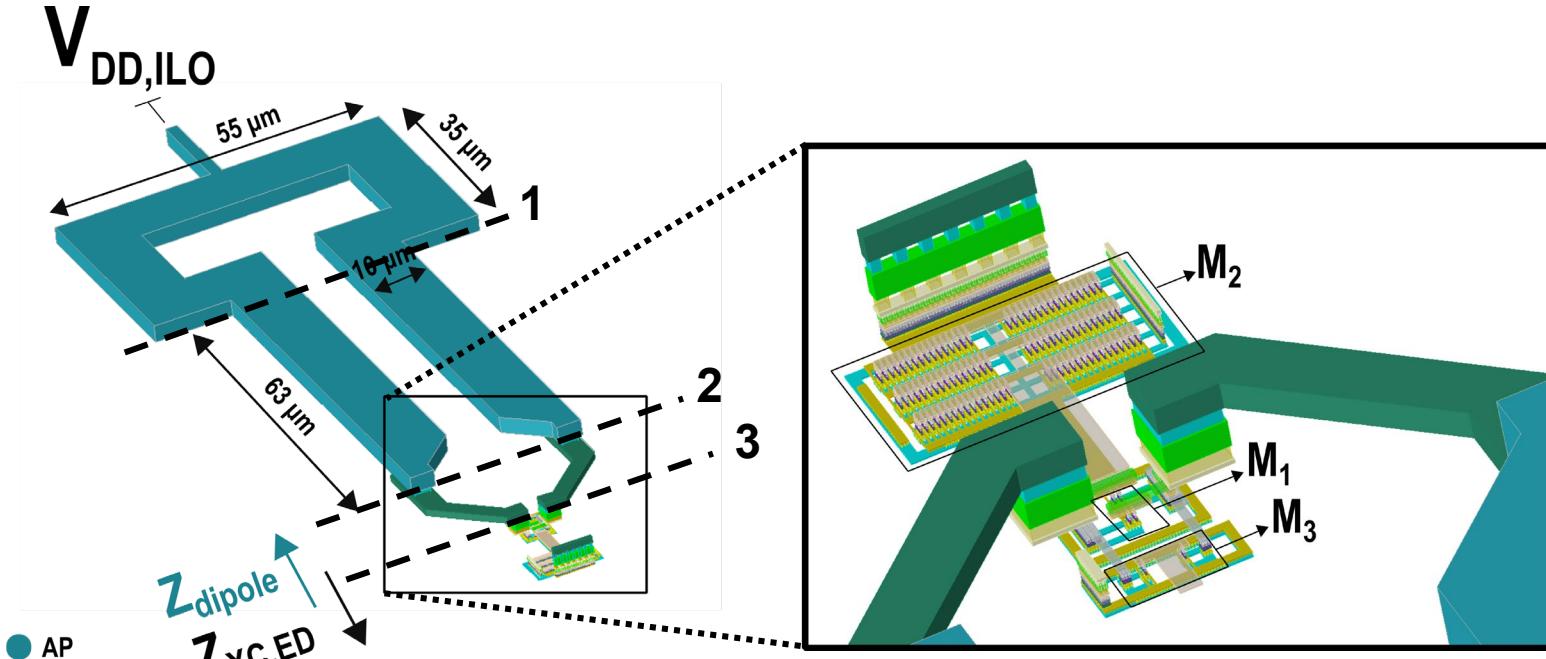
Low NEP, area and P_{DC}

Inductor – Antenna co-design

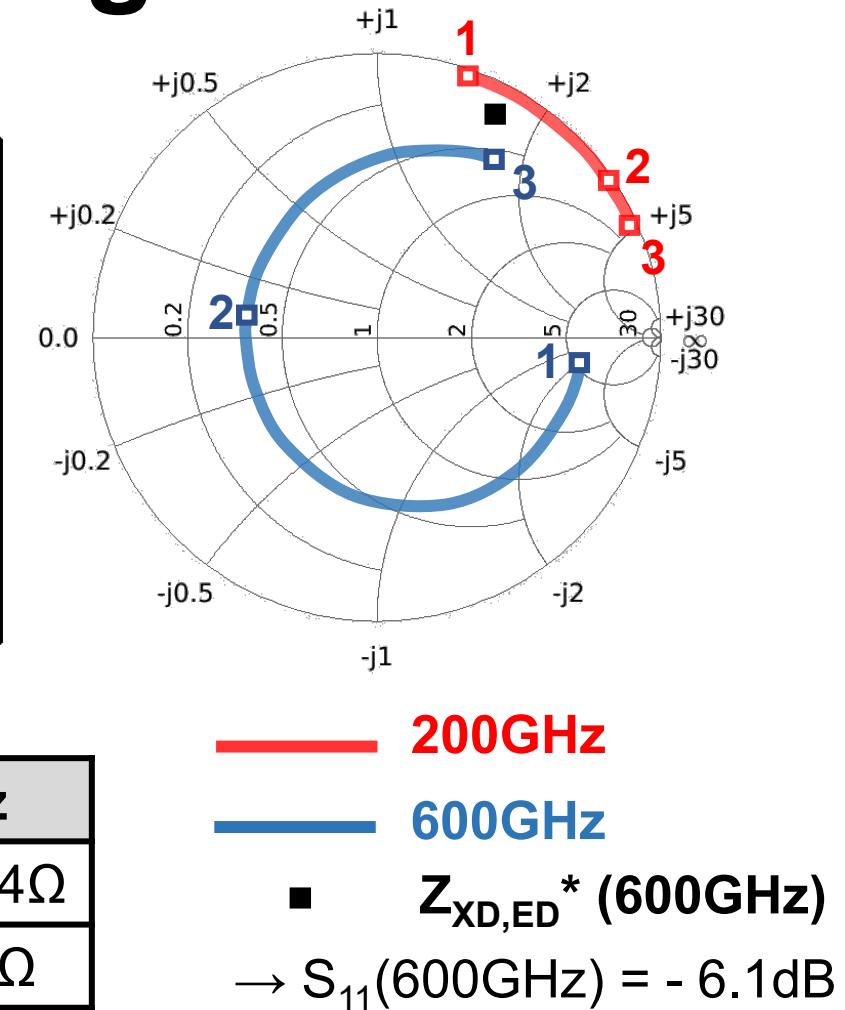
Oscillation @ 200 GHz
Folded dipole @ 600 GHz



Inductor – Antenna co-design



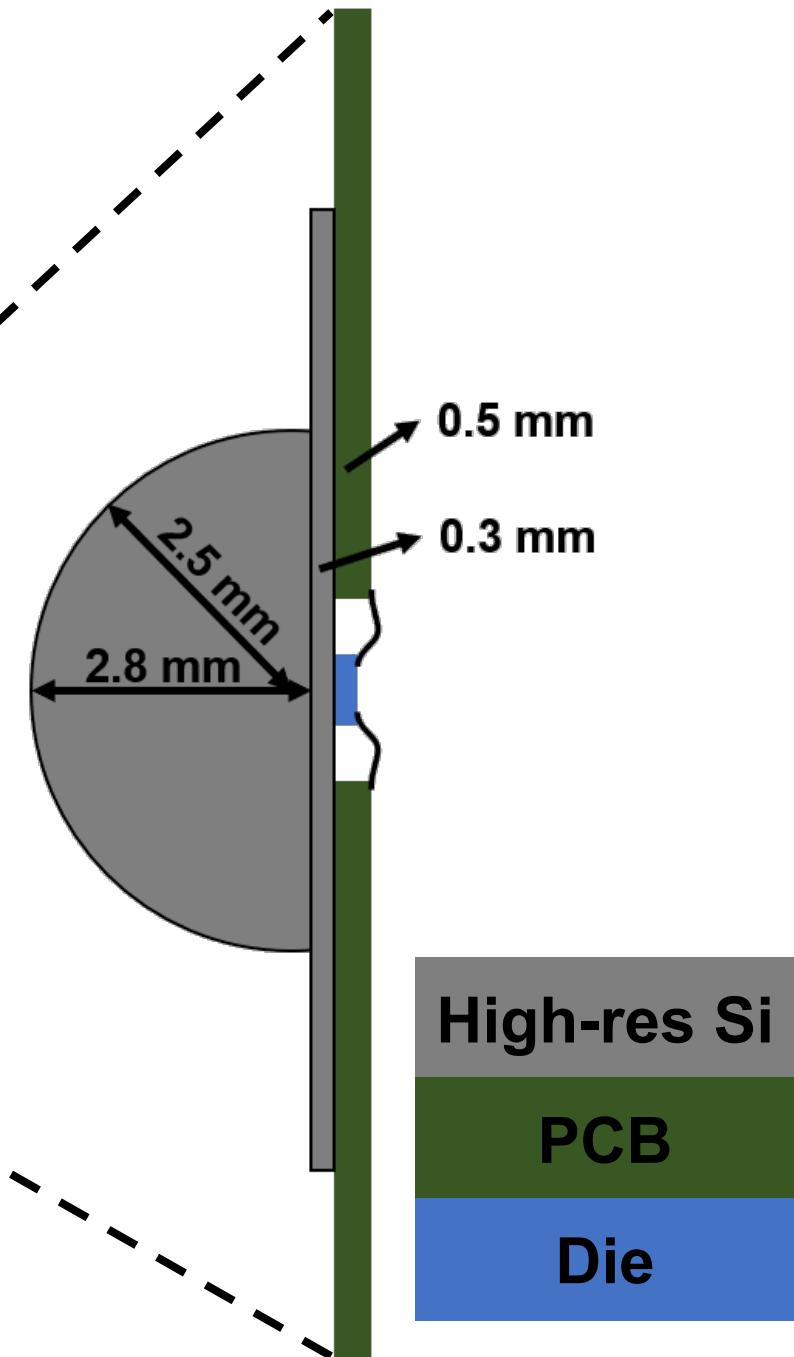
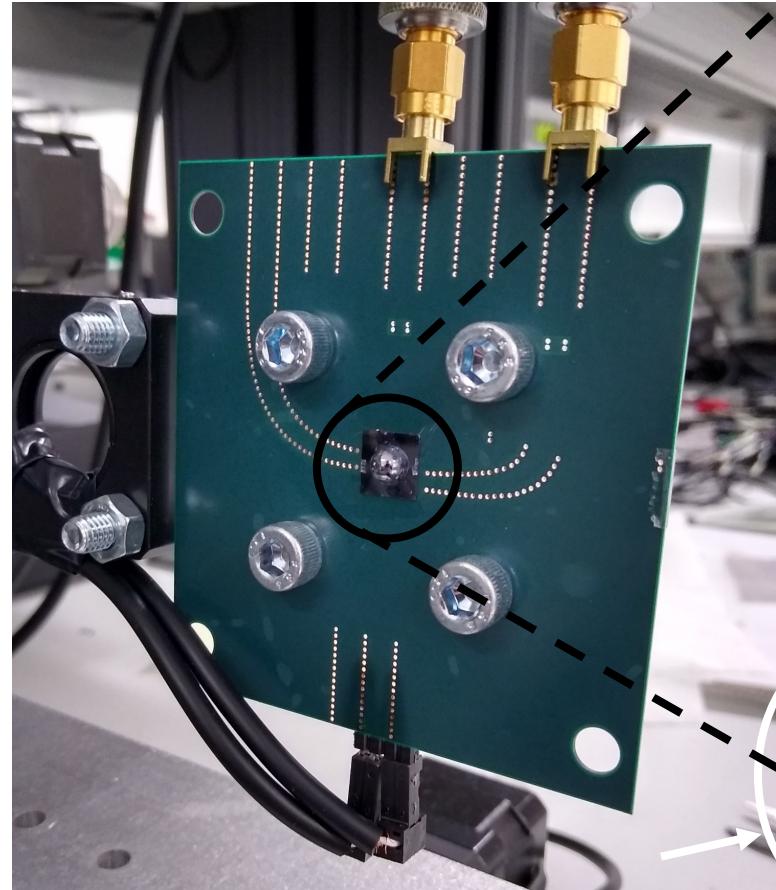
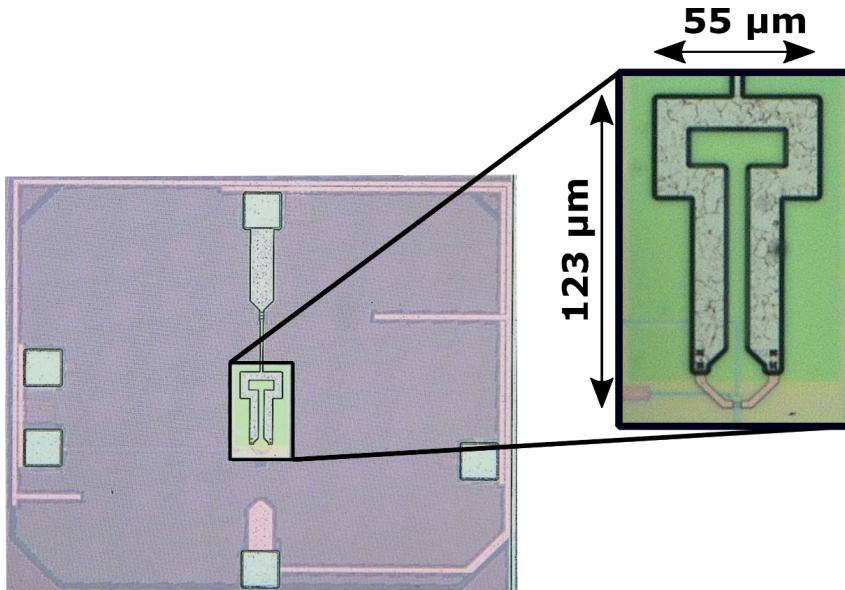
	200 GHz	600 GHz
$Z_{\text{XC},\text{ED}}$	$-48.5 - j \cdot 231 \Omega$	$10.2 - j \cdot 82.14 \Omega$
Z_{dipole}	$17.9 + j \cdot 231.8 \Omega$	$29 + j \cdot 85.5 \Omega$



Outline

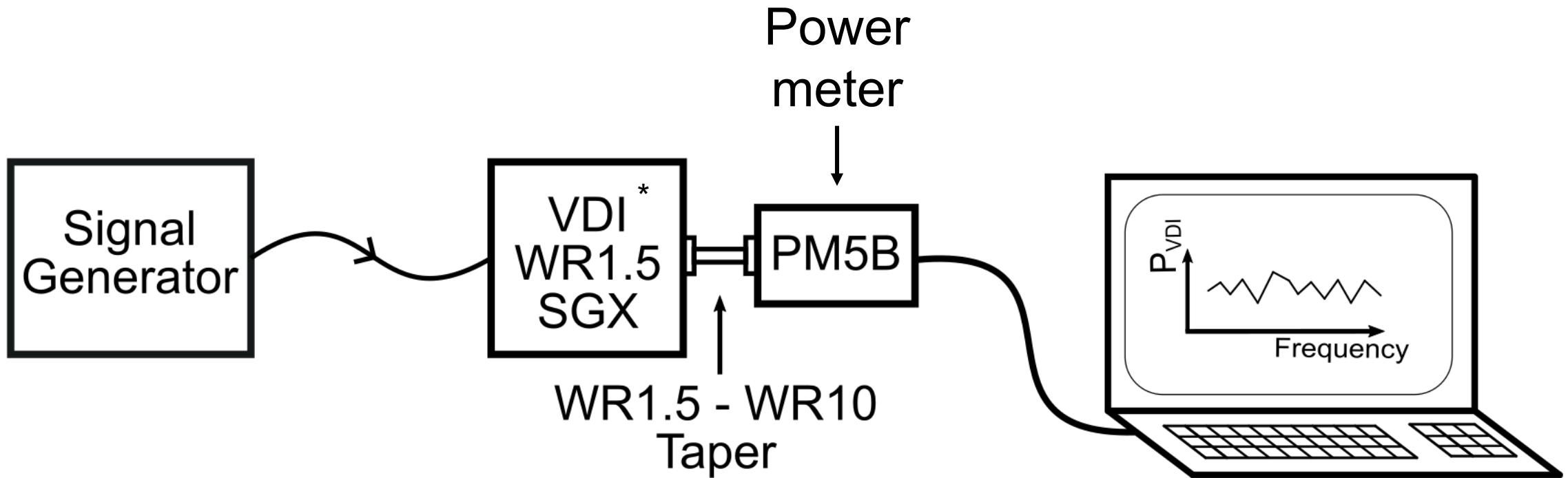
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Chip micrograph and lens-PCB assembly



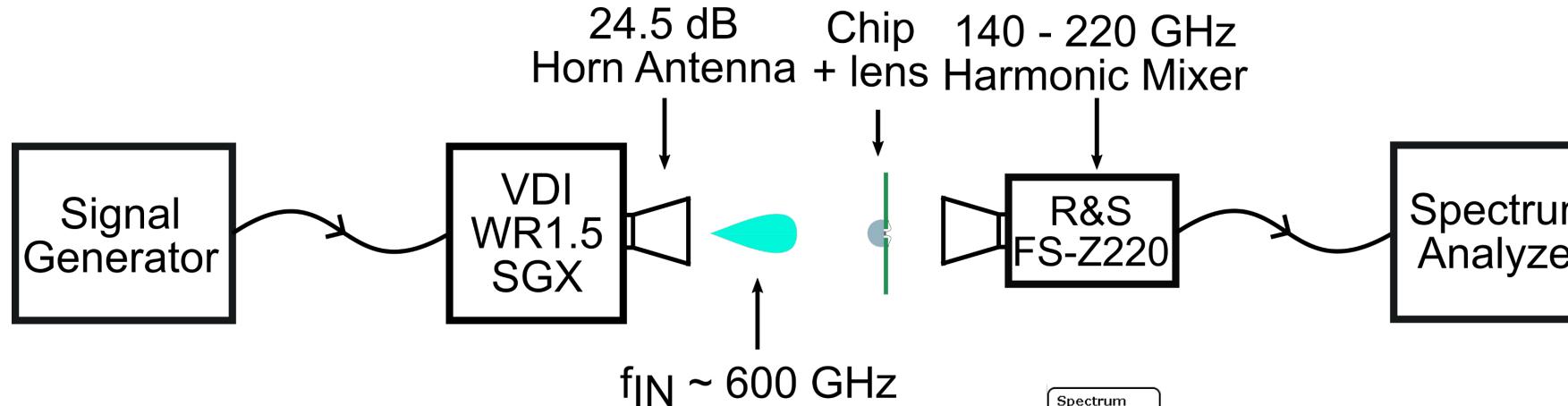
23.3: A 605 GHz 0.84 mW Harmonic Injection-Locked Receiver Achieving 2.3 pW/ $\sqrt{\text{Hz}}$ NEP in 28 nm CMOS

Power calibration



* Virginia Diodes
AMC-372

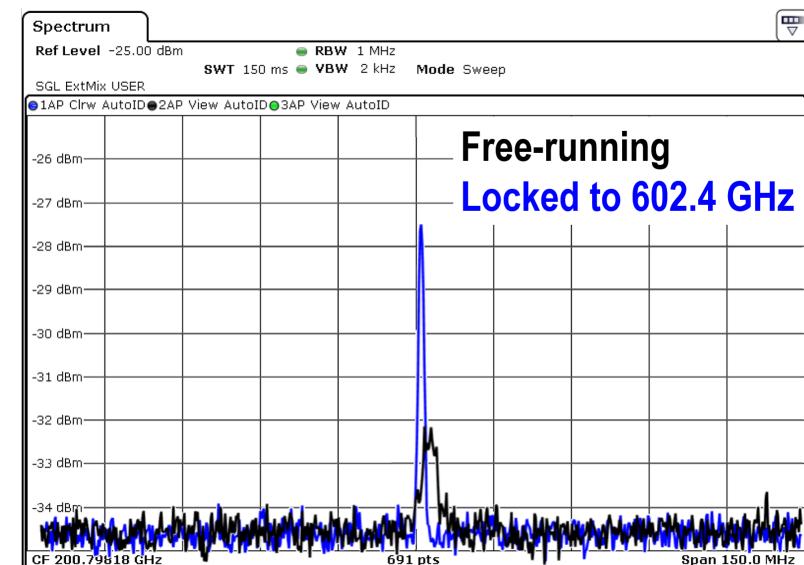
Harmonic injection locking demonstration



Inject $3xf_{ILO,0}$ ($\sim 600 \text{ GHz}$)

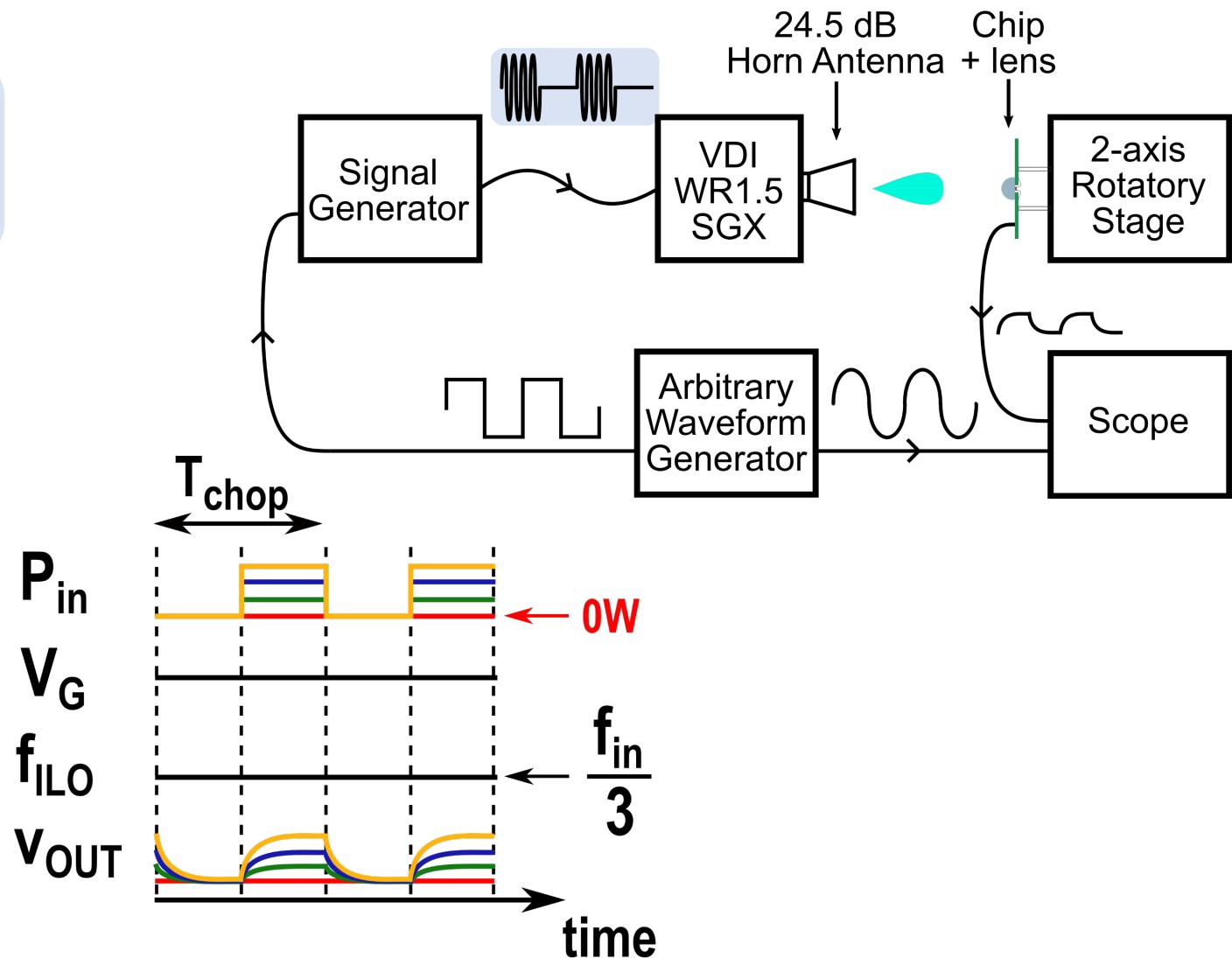
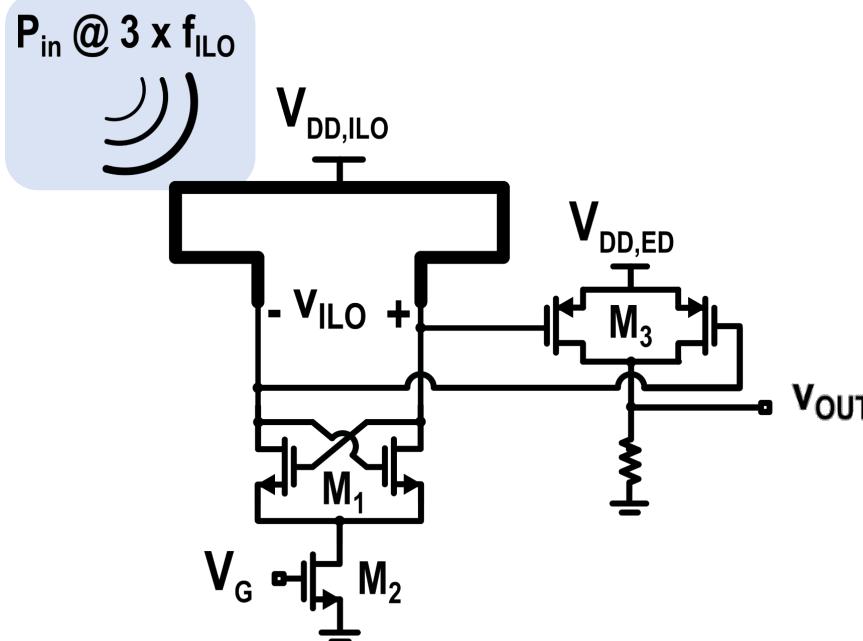
Observe f_{ILO} ($\sim 200 \text{ GHz}$)

→ Harmonic locking is clear



Modulation: off-chip

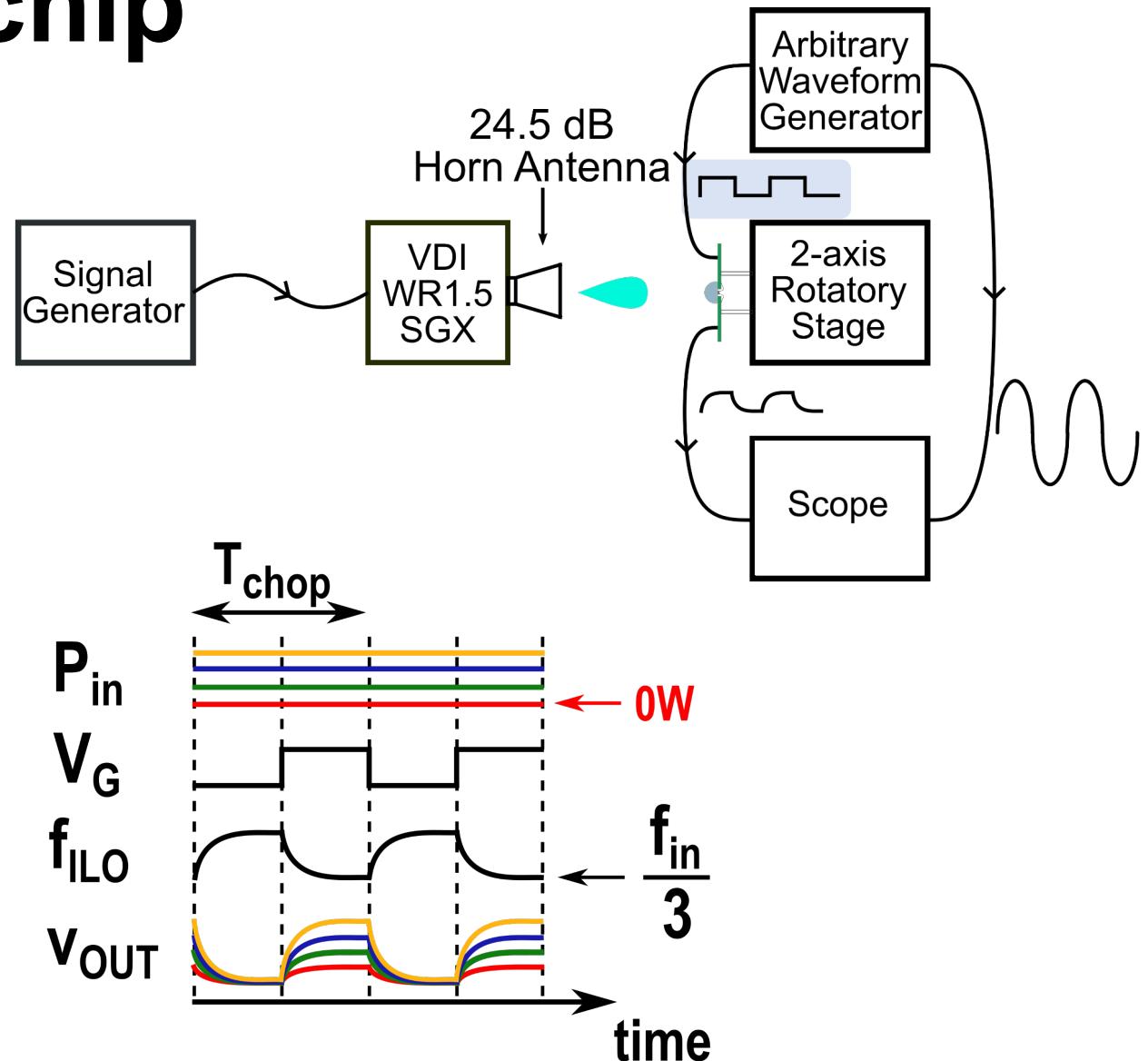
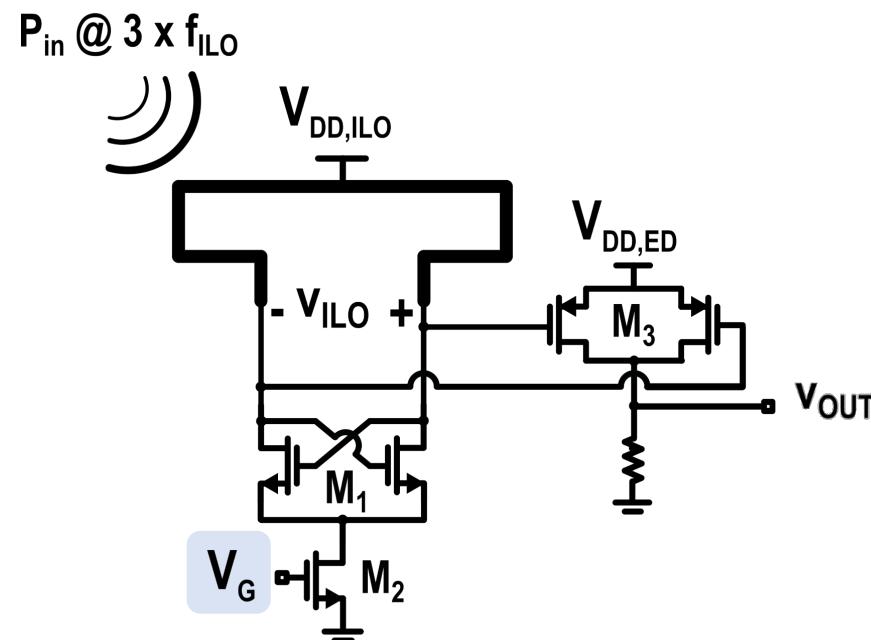
Input power modulation
Limited to ~ 10 kHz



23.3: A 605 GHz 0.84 mW Harmonic Injection-Locked Receiver Achieving 2.3 pW/Hz NEP in 28 nm CMOS

Modulation: on-chip

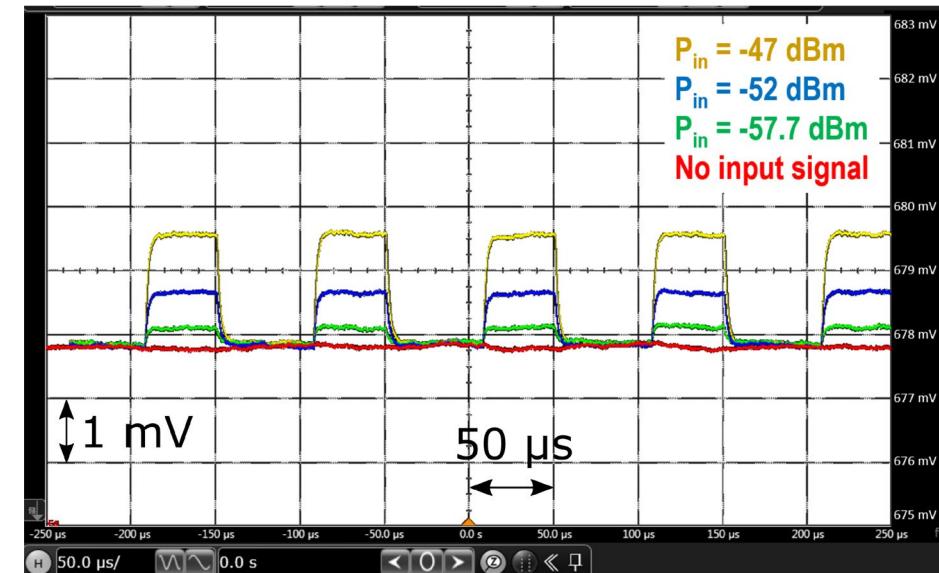
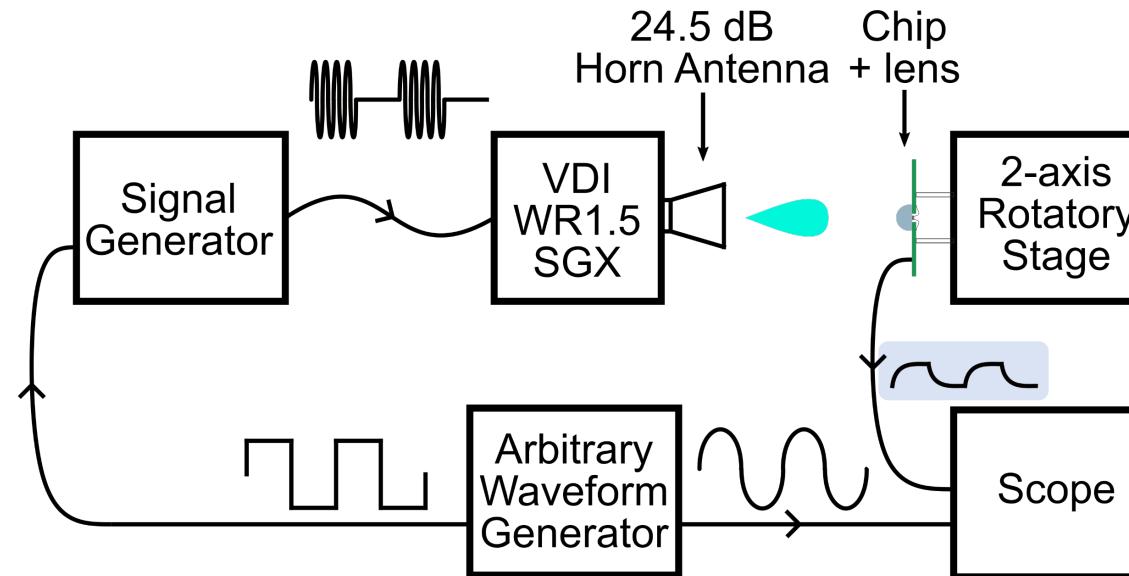
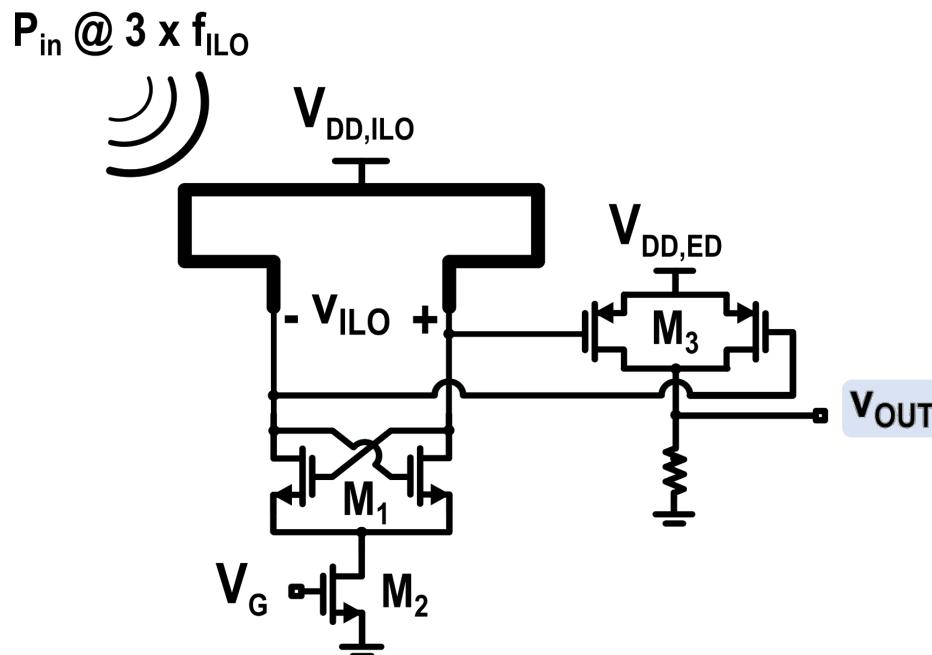
On-chip modulation
For minimum NEP



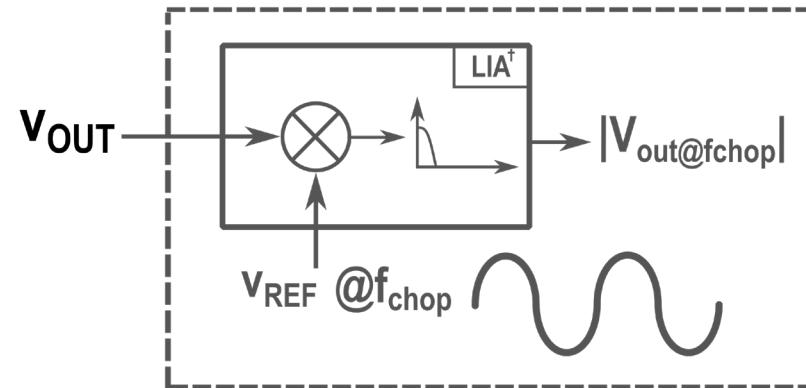
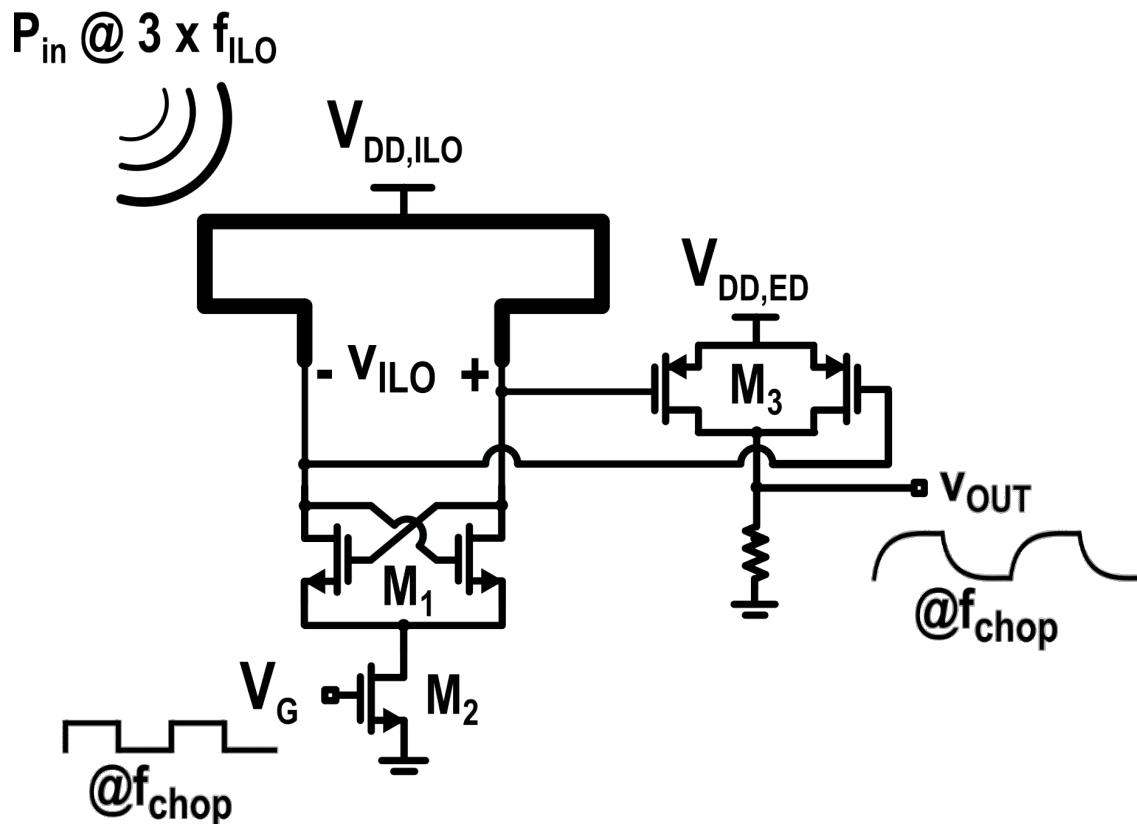
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Output signal

P_{in} modulated (ON-OFF)
 P_{in} ON $\rightarrow V_{out}$ high



Characterization with lock-in amplifier



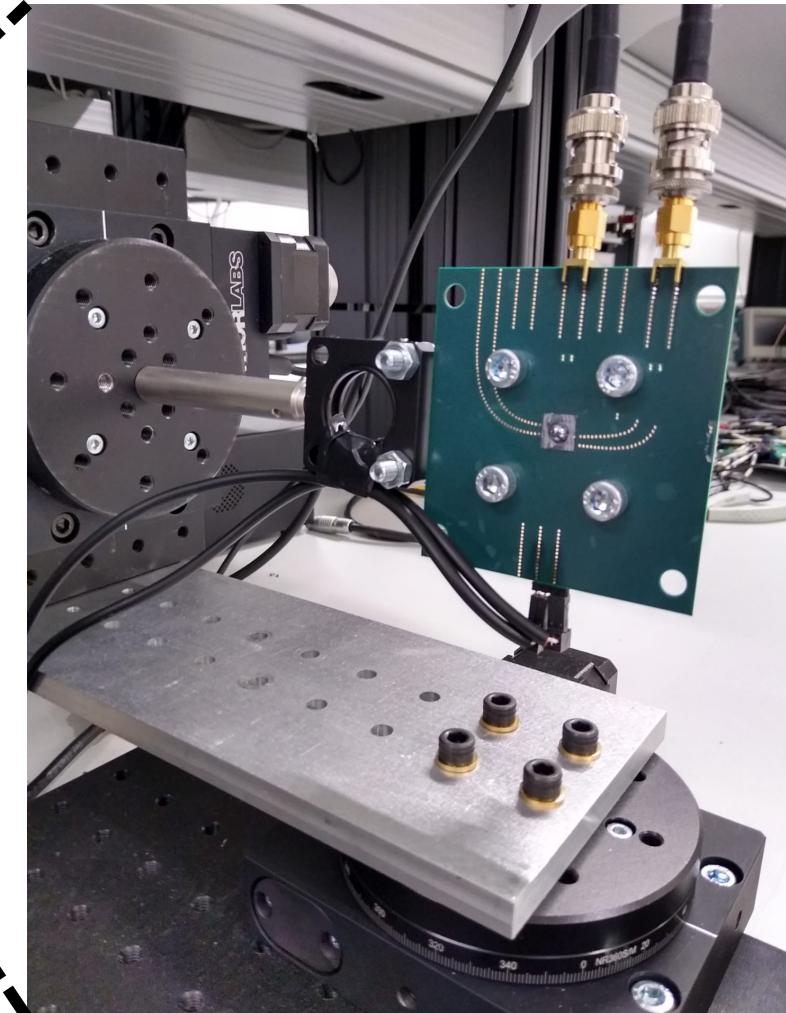
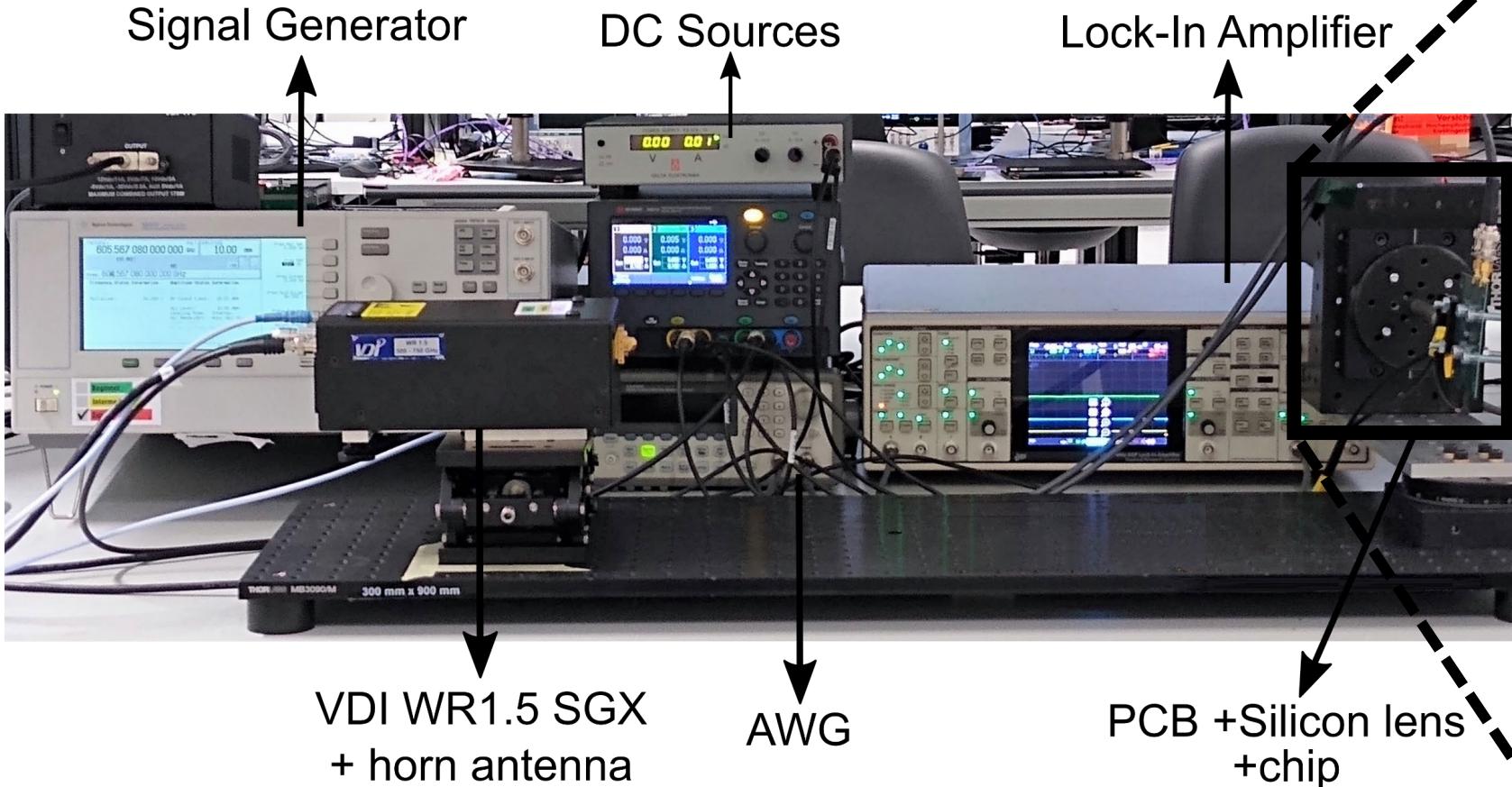
$$R_v = \frac{V_{out}@f_{chop}(V)^*}{P_{in}(W)}$$

$$NEP = \frac{\text{Noise Density (V}/\sqrt{\text{Hz})}}{R_v(\text{V}/\text{W})}$$

[†] Lock-in amplifier

* Relative to case without THz input

Characterization: measurement setup



23.3: A 605 GHz 0.84 mW Harmonic Injection-Locked Receiver Achieving 2.3 pW/Hz NEP in 28 nm CMOS

Lock-in amplifier: noise density

$$X_{\text{noise(SR865A)}} = \sqrt{\text{avg}(X_{\text{value}} - X_{\text{mean}})^2} \quad (\text{averaging time } \sim 200^*\tau)$$

$$\text{Noise density } \left(\frac{\text{V}}{\sqrt{\text{Hz}}} \right) = \frac{X_{\text{noise(V)}}}{\sqrt{\text{ENBW}}} \text{ and ENBW } \sim \frac{1}{\tau}$$

Typically: $X_{\text{noise}} \sim \sqrt{\text{ENBW}}$

- Time constant (τ) influences settling time and X_{noise} ,
but **not** the noise **density** → $\text{NEP} \neq f(\tau)$

NEP: a universal sensitivity FOM?

$\text{NEP} \neq f(\tau)$

- Compare detectors without knowing τ ☺
- τ only determines how easily signal is distinguished from noise

But, what if $\text{NEP} = f(\tau)$?

- Performance relative to other detectors depends on acquisition speed

Drift and τ -dependent NEP

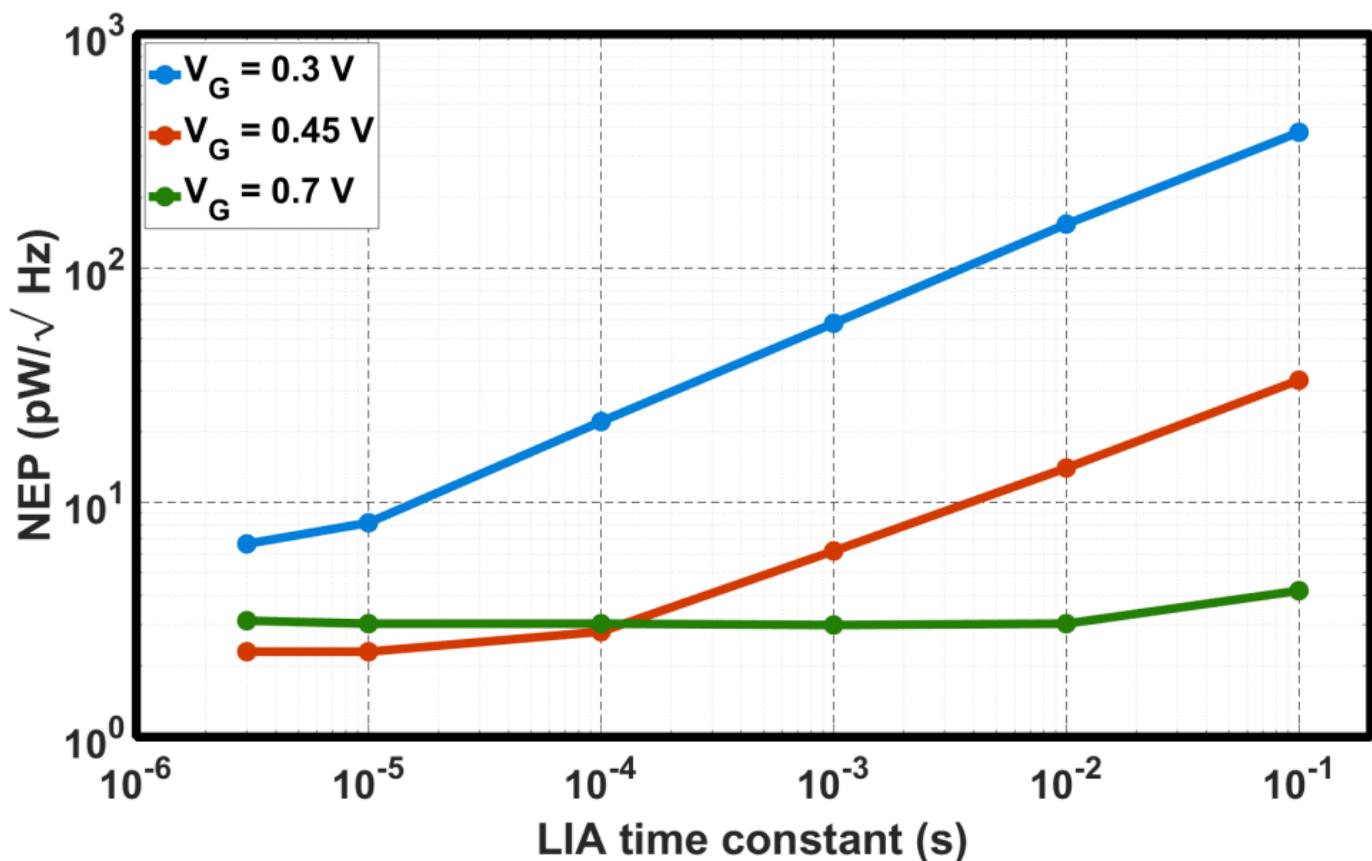
Oscillator is free-running and shows
drift-related variations as integration time increases

These show up as noise on the LIA X_{noise} reading

$\tau \uparrow \rightarrow X_{\text{noise}} \neq \sim \sqrt{\text{ENBW}}$ → Noise density not constant

→ $\text{NEP} = f(\tau)$!

Drift and τ -dependent NEP



$V_G \uparrow \rightarrow \text{drift} \downarrow$

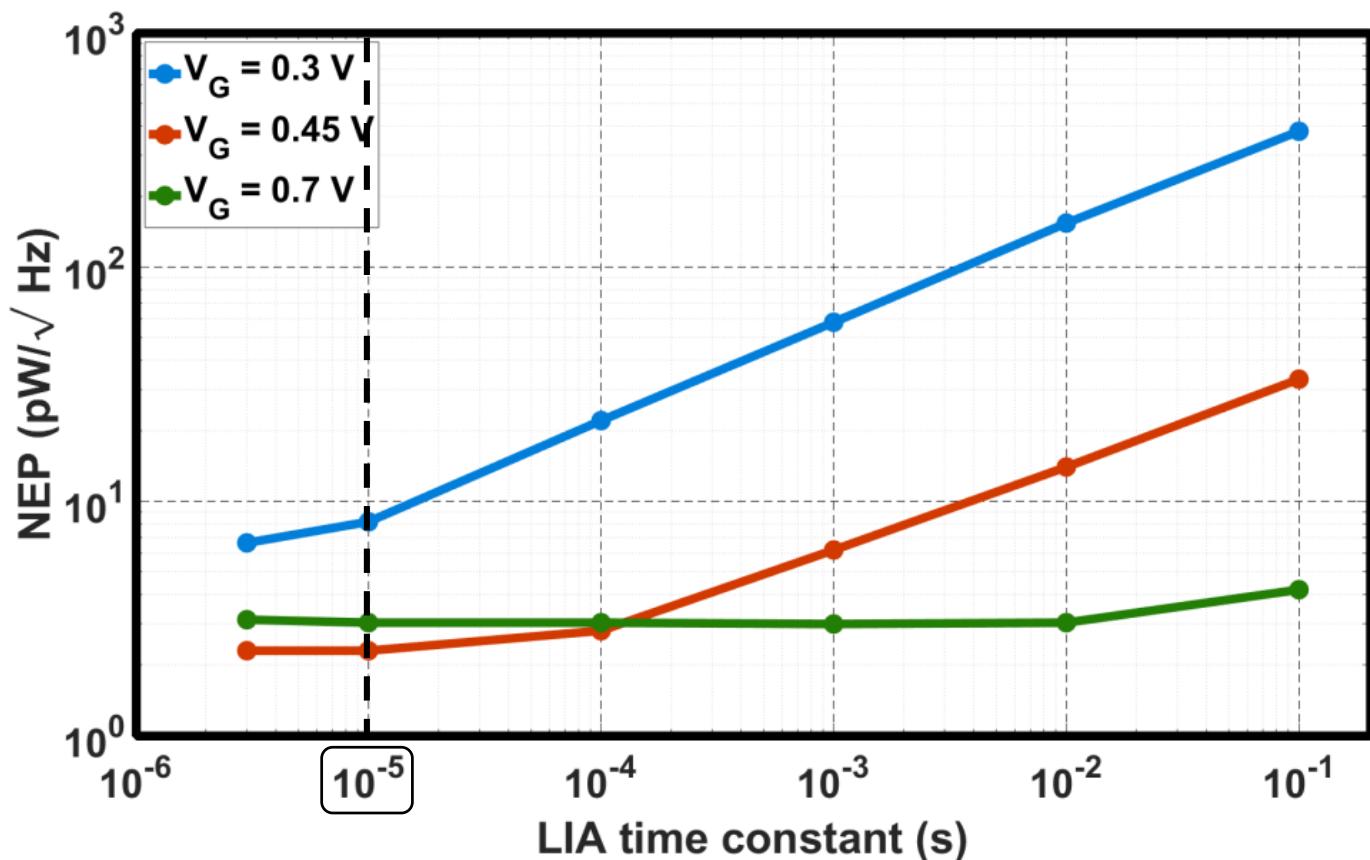


Influence of τ on NEP \downarrow

$$\text{ENBW}_{\text{SR865A}} = \frac{1}{4\tau}$$

for 1 RC stage

Drift and τ -dependent NEP



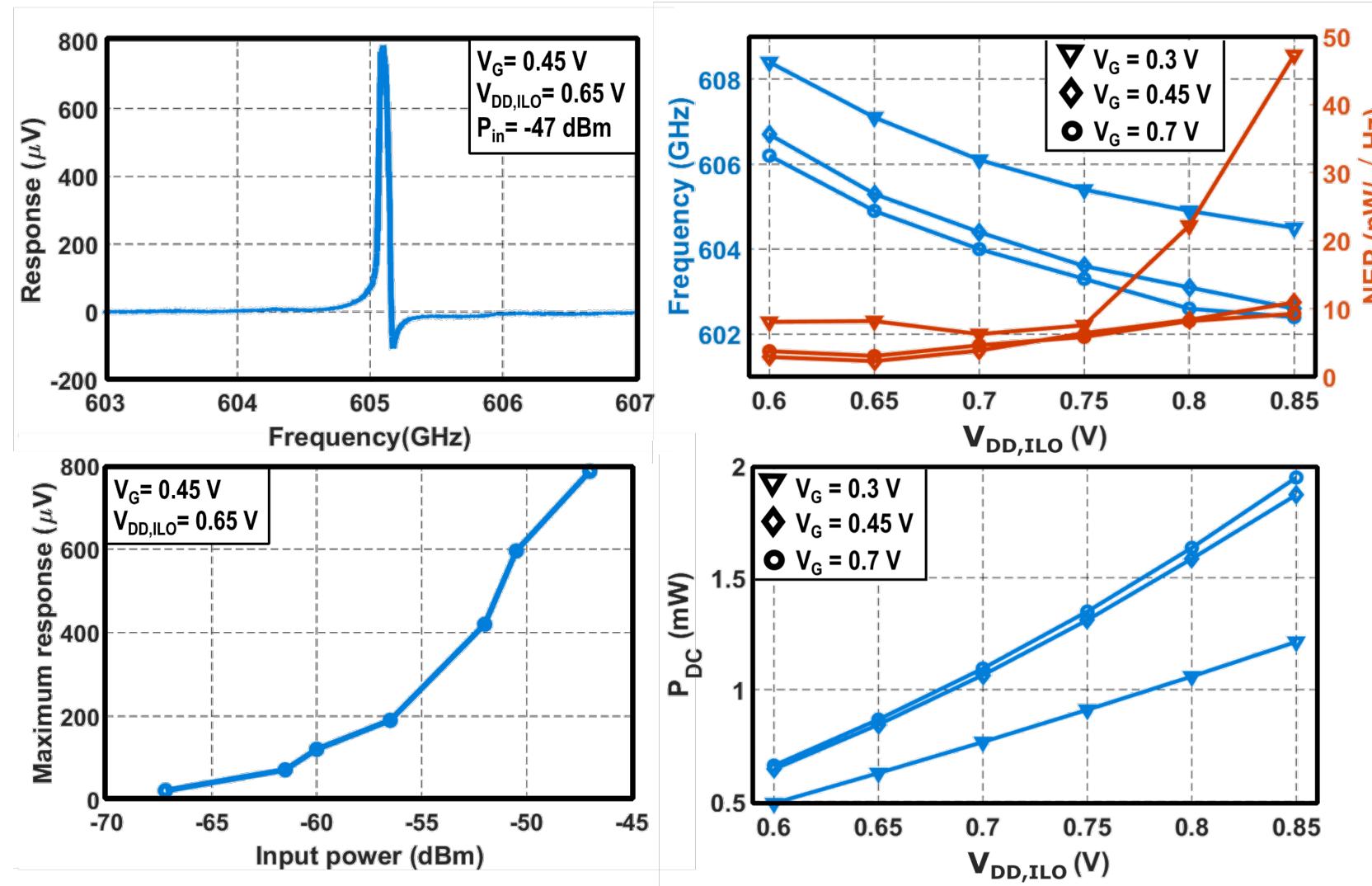
$V_G \uparrow \rightarrow \text{drift} \downarrow$



Influence of τ on NEP \downarrow

$$\begin{aligned} \text{ENBW}_{\text{SR865A}, 10\mu\text{s}} \\ = 0.9 \times \frac{1}{4\tau} = 22.5 \text{ kHz} \\ (\text{Correction factor for small time constants}) \end{aligned}$$

Characterization results

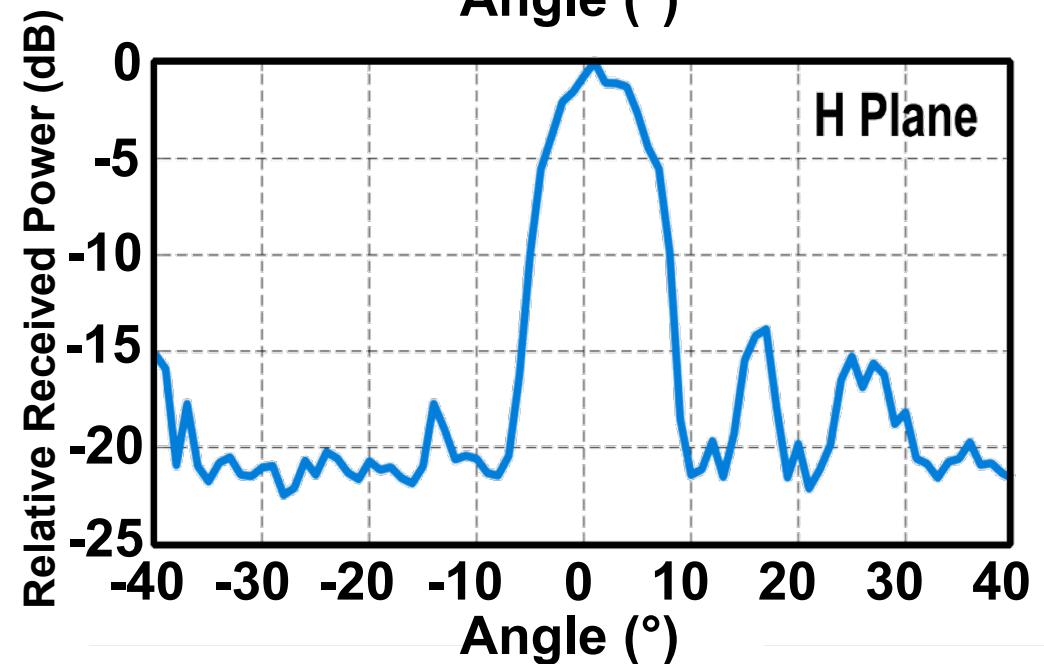
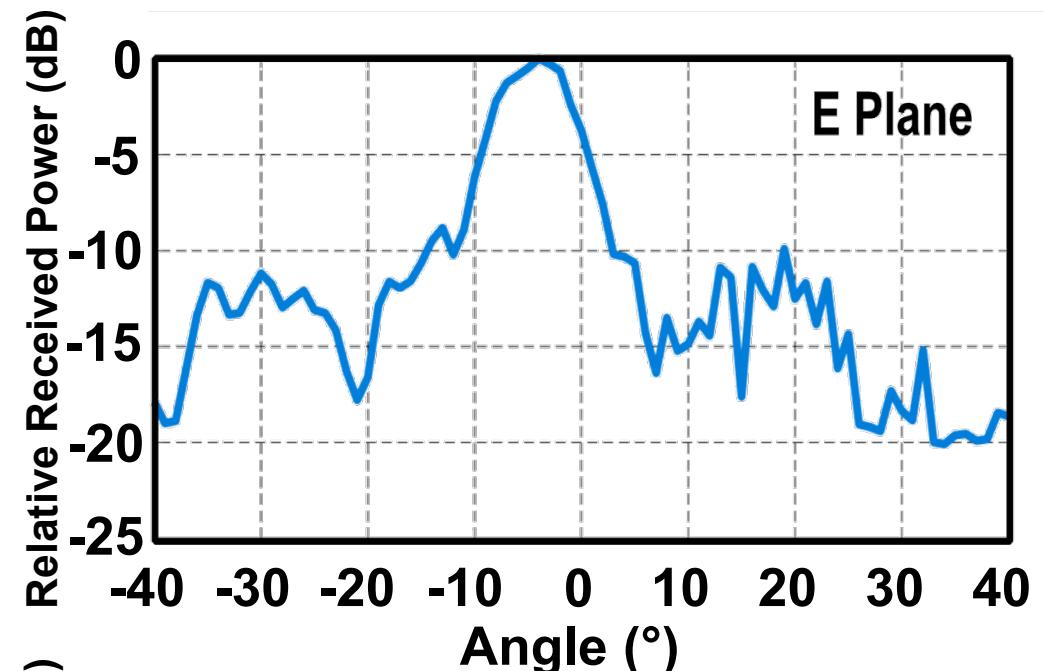


$\text{NEP}_{\min} = 2.3 \text{ pW}/\sqrt{\text{Hz}}$
 $R_v = 32 \text{ kV/W}$
 $@P_{in} = -57 \text{ dBm}$
 $f_{in} = 605.3 \text{ GHz}$
 $P_{DC} = 0.84 \text{ mW}$
 $f_{mod} = 1 \text{ MHz}$
 $\tau = 10 \mu\text{s}$
 $\text{ENBW} = 22.5 \text{ kHz}$

23.3: A 605 GHz 0.84 mW Harmonic Injection-Locked Receiver Achieving 2.3 $\text{pW}/\sqrt{\text{Hz}}$ NEP in 28 nm CMOS

Radiation pattern

- Silicon substrate
 - 300 μm
- Hyperhemispherical lens
 - 5 mm \varnothing
 - 2.8 mm thickness
 - No anti-reflective coating
- Measured directivity: 19.8 dBi



Comparison table

	This work	TTST 2013 [4]	TTST 2016 [5]	JSSC 2013 [6]	ESSCIRC 2010 [7]	IRMMW-THz 2013 [8]	EuMIC 2018 [9]
Technology	28nm CMOS	40nm CMOS	0.130µm CMOS	0.130µm CMOS	65nm SOI	65nm CMOS	22nm FD-SOI
Detector type	H-ILO	IM-SRR	Diode-NMOS	SBD	Self-mixing NMOS	Self-mixing NMOS	Self-mixing NMOS
Frequency (GHz)	605	495	820	860	650	724	855
R _v (V/W)	32k	3.18G *	3.46k/2.56k *	273	1.1k	2.2k	1.51k/ 180mA/W ‡
NEP (pW/√Hz)	2.3 §	0.1	12.6/36.2 ¶	42 ¶	50	14	23 / 12 ‡
P _{DC} /pixel (mW)	0.84	5.6 †	0.15	I _{bias} = 20µA	-	-	-
Area/pixel (µm ²)	6800	110000 †	25000 #	15000 #	22500	10000 #	10000

Estimated from die photograph

* Including low-noise baseband amplification

| Maximum/mean R_v and minimum/mean NEP out of array

† Excluding external low-noise opamp

‡ Current mode readout

§ $\tau=10\mu s$

¶ $\tau=10ms$

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Conclusion

The possibility of using Harmonic Injection Locking for above- f_{\max} power detection has been demonstrated in a compact, low-power implementation in 28nm CMOS

Using this technique, an NEP of $2.3 \text{ pW}/\sqrt{\text{Hz}}$ at 605 GHz has been achieved

This NEP is better than state-of-the-art CMOS power detectors above 500 GHz

Acknowledgements

- Research Foundation Flanders (FWO)
- EUROPRACTICE for MPW and design tool support
- Colleagues at MICAS



23.4: An 82fs_{RMS}-Jitter and 22.5mW-Power, 102GHz W-Band PLL Using a Power-Gating Injection-Locked Frequency Multiplier-Based Phase Detector in 65nm CMOS

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Yoonseo Cho¹, Chanwoong Hwang¹, Heein Yoon², and Jaehyouk Choi¹

¹KAIST, Daejeon, Korea ²Qualcomm, San Diego, CA

***Equally Credited Authors (ECAs)**

Self Introduction

Suneui Park, KAIST

❖ Contact information

Email: suneui@kaist.ac.kr

❖ Education

2013 – 2020

B.S. in ECE, Ulsan National Institute of Science and Technology, Ulsan, South Korea

M.S. in ECE, Ulsan National Institute of Science and Technology, Ulsan, South Korea

2020 – present

Ph.D. in EE, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea

❖ Research interests

Analog/mixed IC designs, especially mmW low phase noise and high frequency synthesizers



Outline

❖ Introduction

- Demands of Low-Jitter W-Band PLL
- Problems of Conventional W-Band PLLs

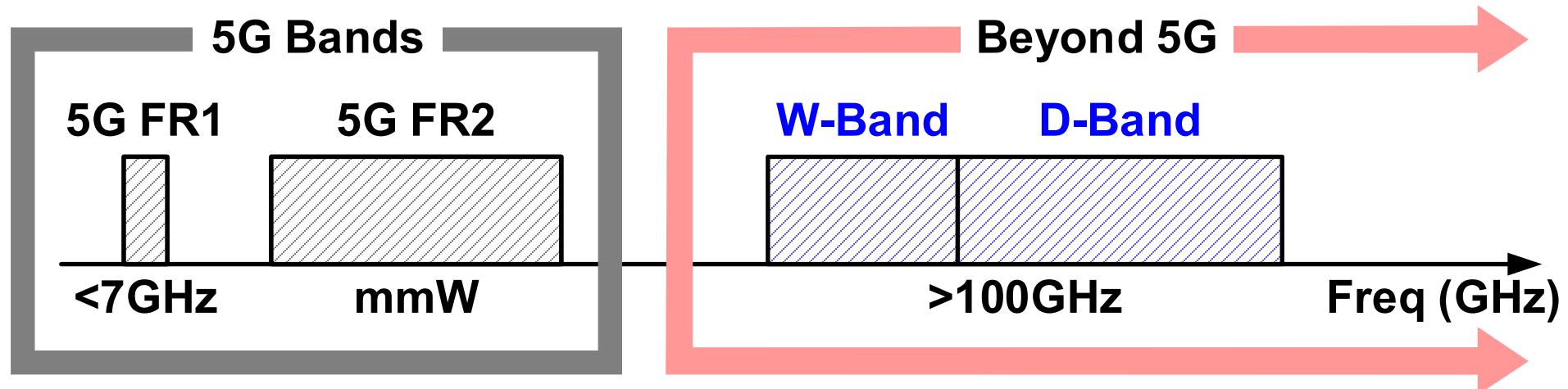
❖ Proposed W-Band PLL with PG-ILFM-based PD

- Concept of Proposed PG-ILFM-based PD
- Operation of PLL & Frequency Offset Canceller (FOC)
- Noise Analysis

❖ Measurements and Performance Comparison

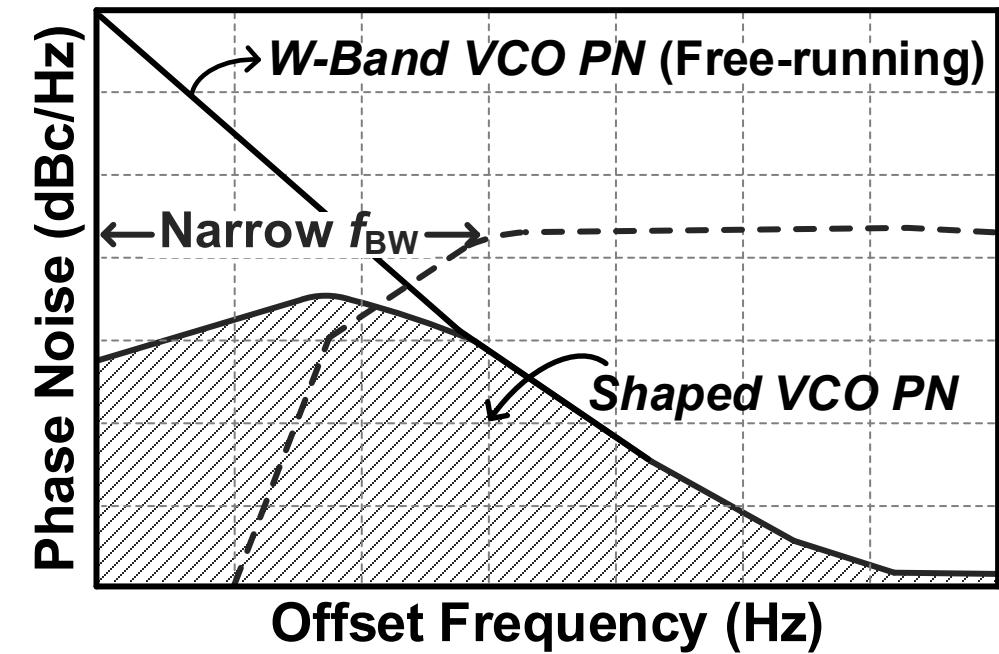
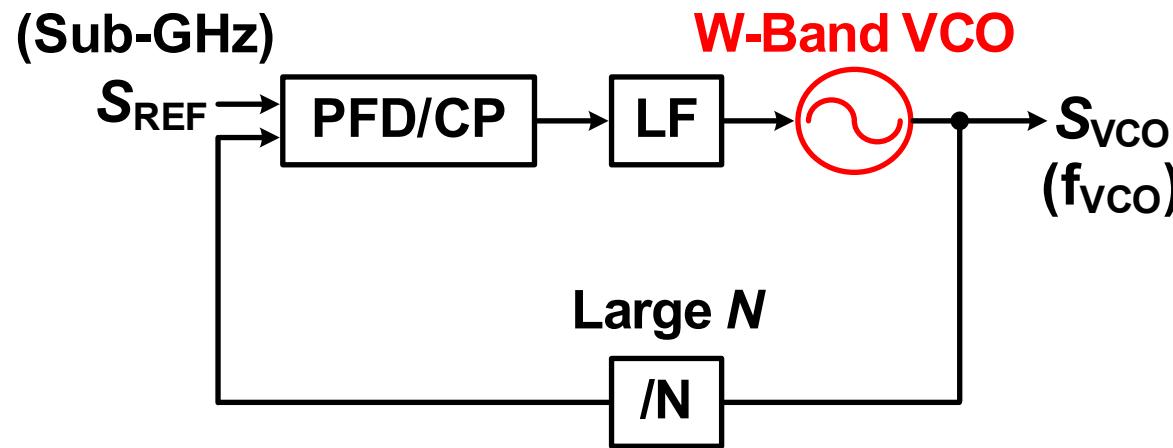
❖ Conclusions

Demands of Low-Jitter >100GHz PLL



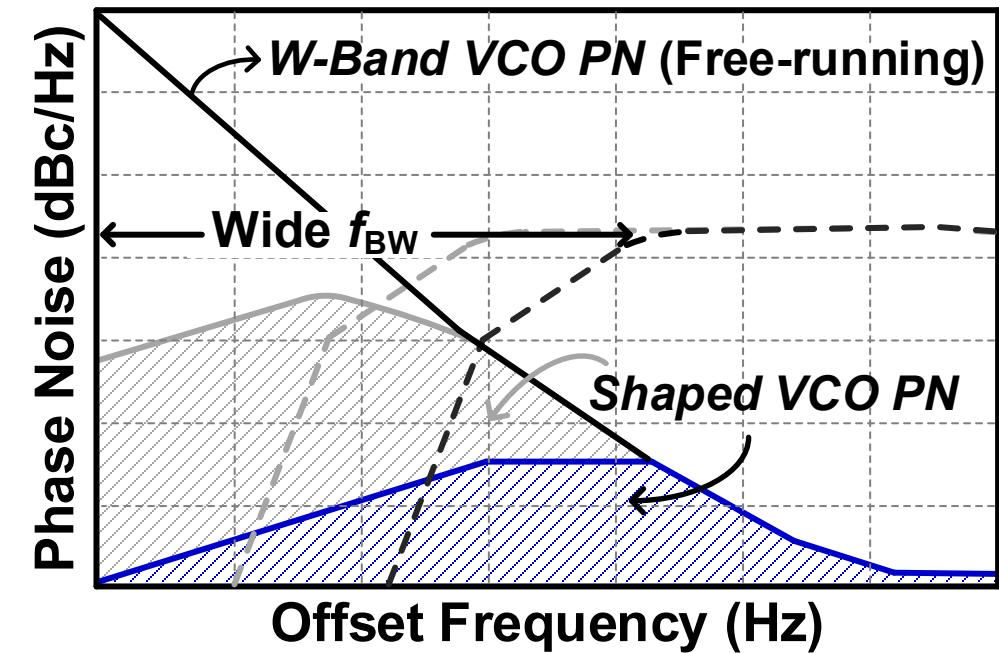
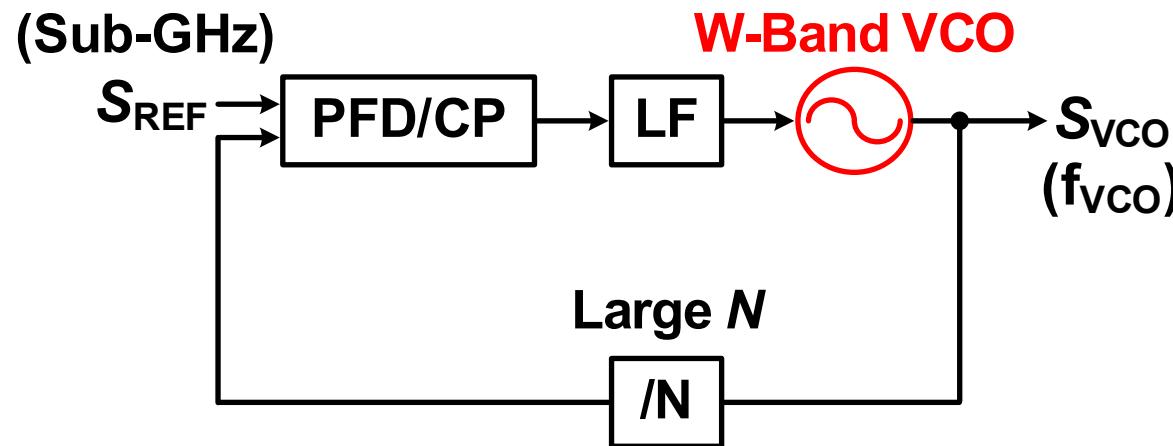
- ❖ For higher data rates for beyond 5G, even higher-frequency bands need to be considered to use wider bandwidth
- ➔ Need to explore W-Band and D-Band

Problems of Conventional W-Band CP PLL



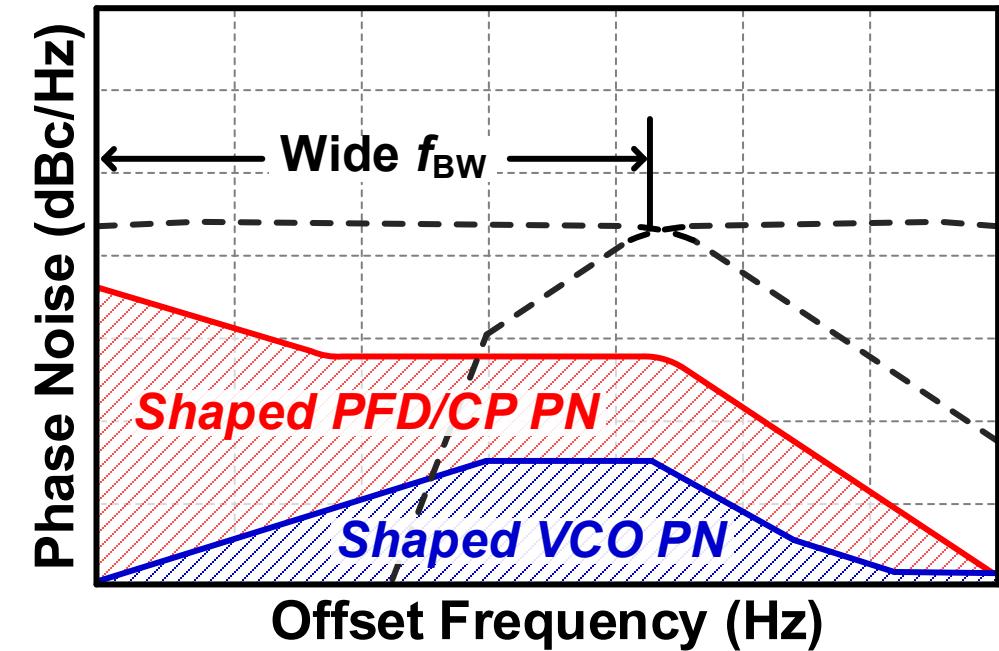
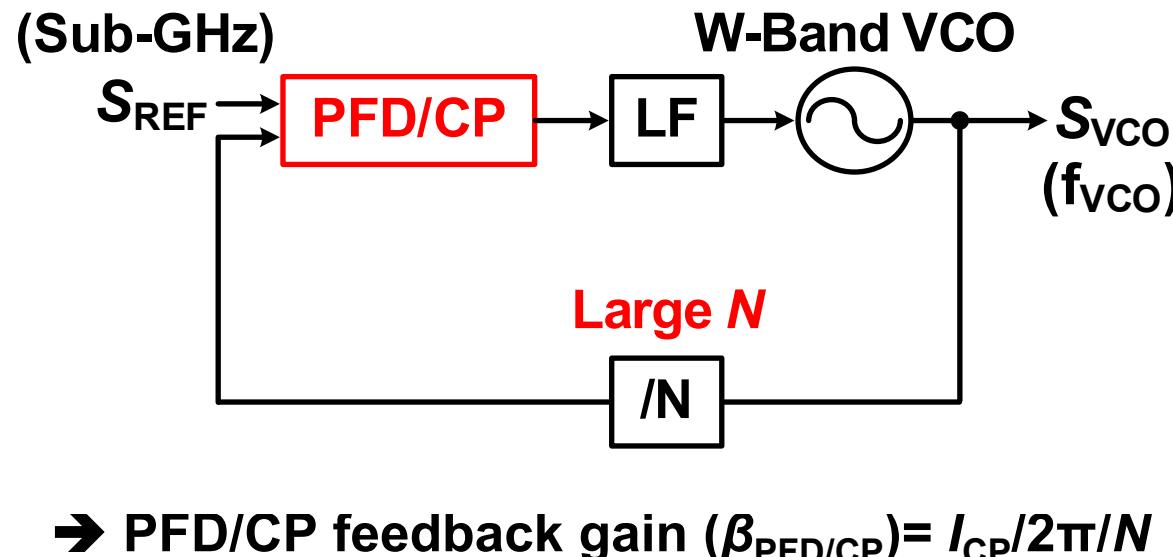
- ❖ To suppress poor PN of W-Band VCO (Q-factor < 3), wide PLL BW is required

Problems of Conventional W-Band CP PLL



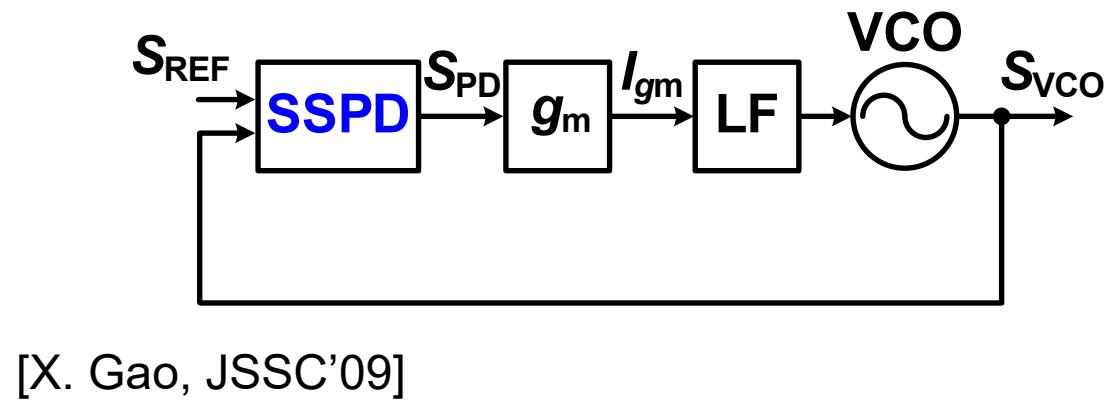
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Problems of Conventional W-Band CP PLL

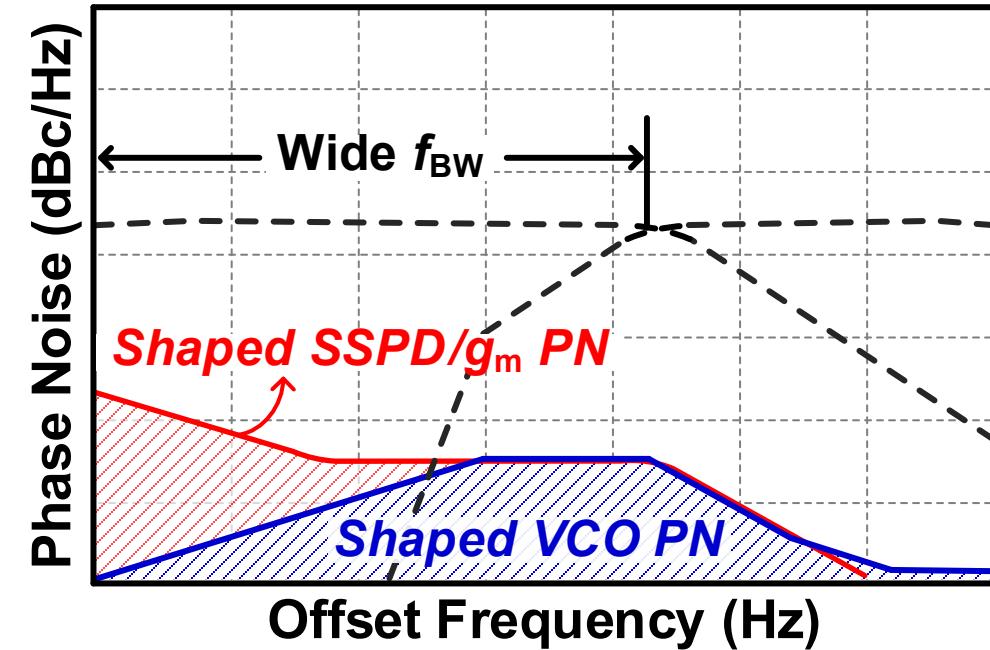
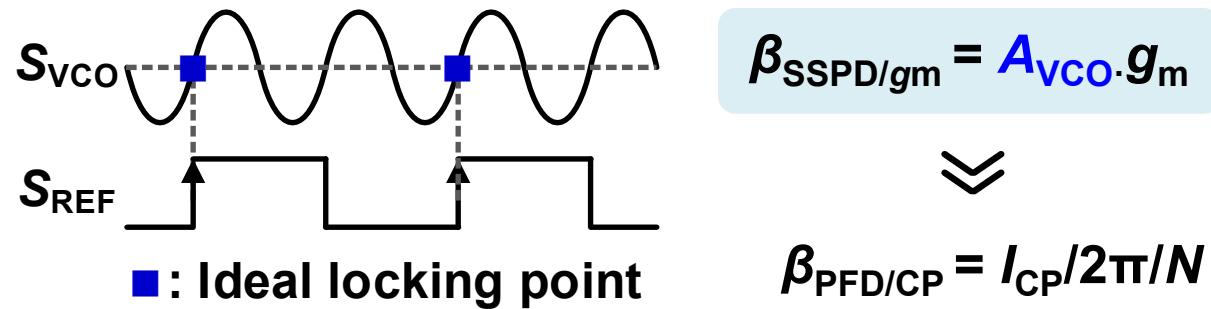


- ❖ With wide PLL BW & large N , **high in-band PN** is inevitable due to PFD/CP PN multiplied by N^2 ☹
- ❖ **Large power consumption** due to high frequency 100GHz divider ☹

Alternative Architecture: Sub-Sampling PLL

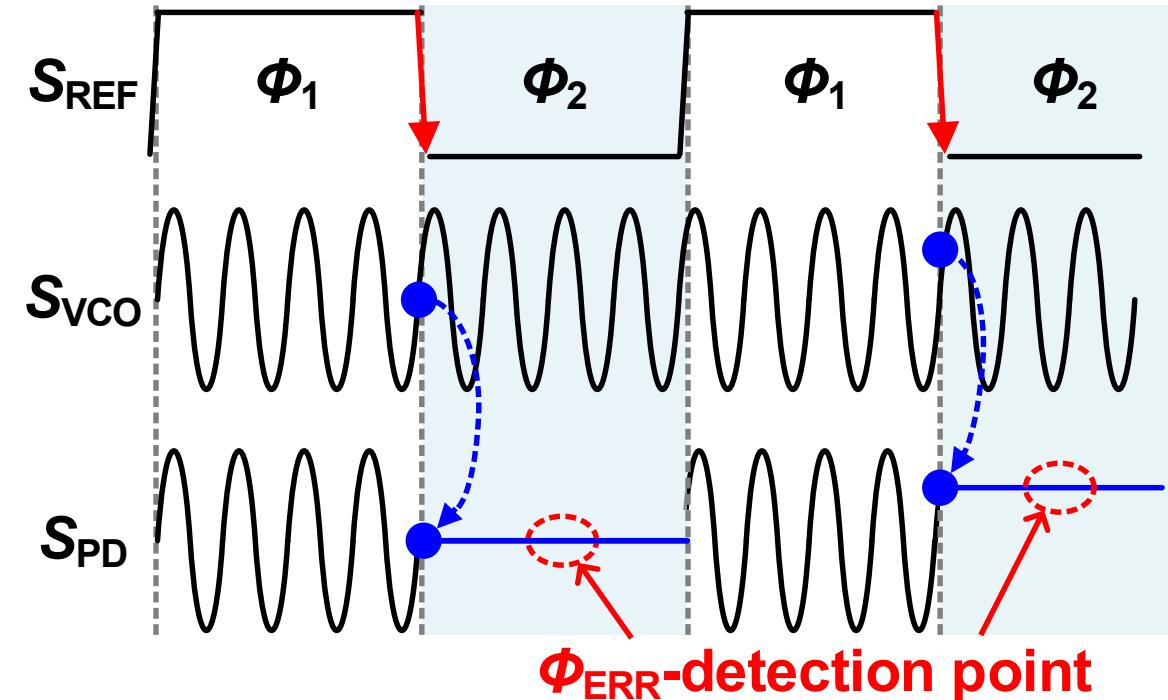
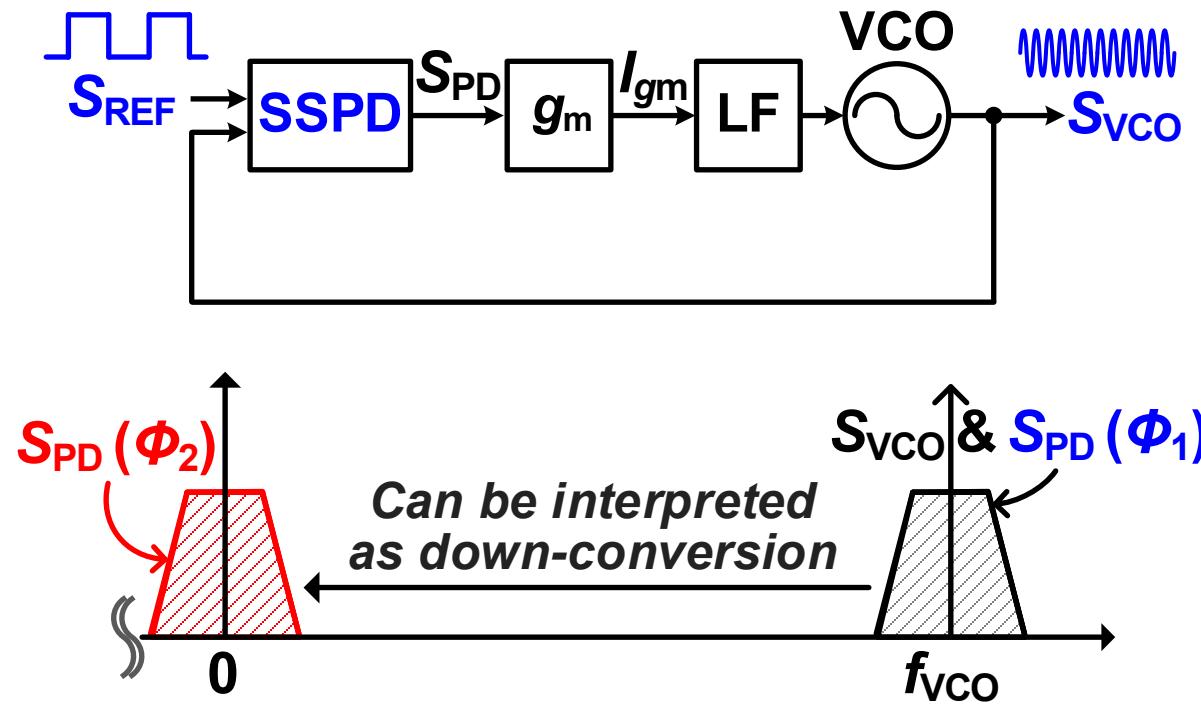


[X. Gao, JSSC'09]



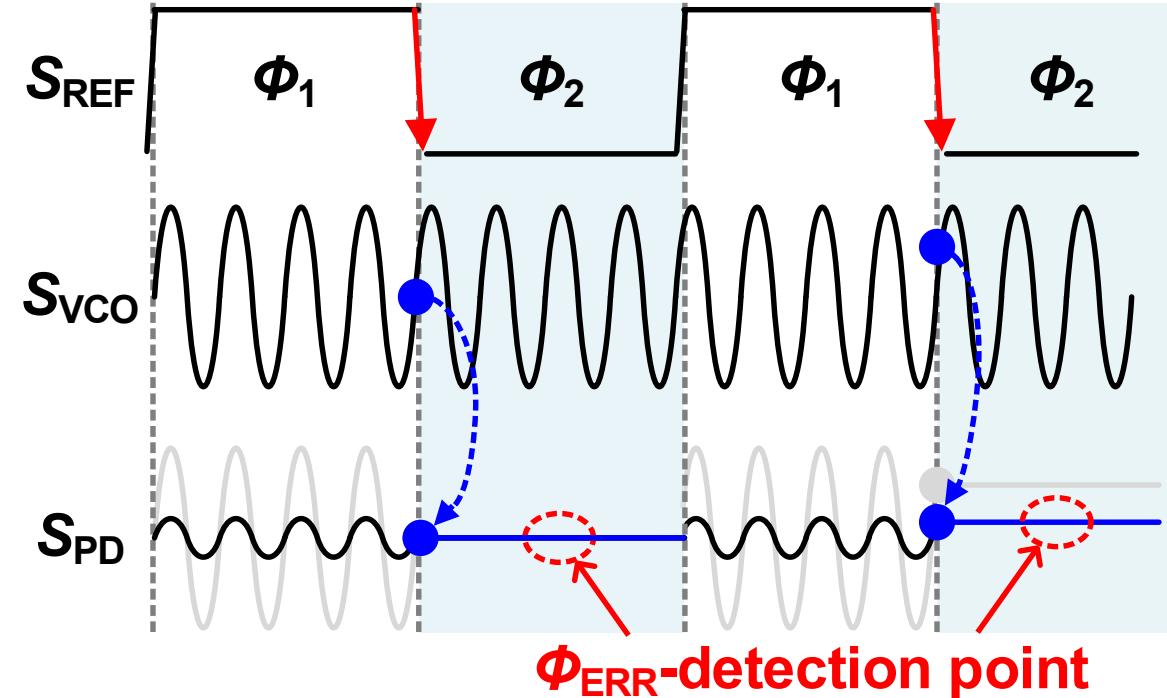
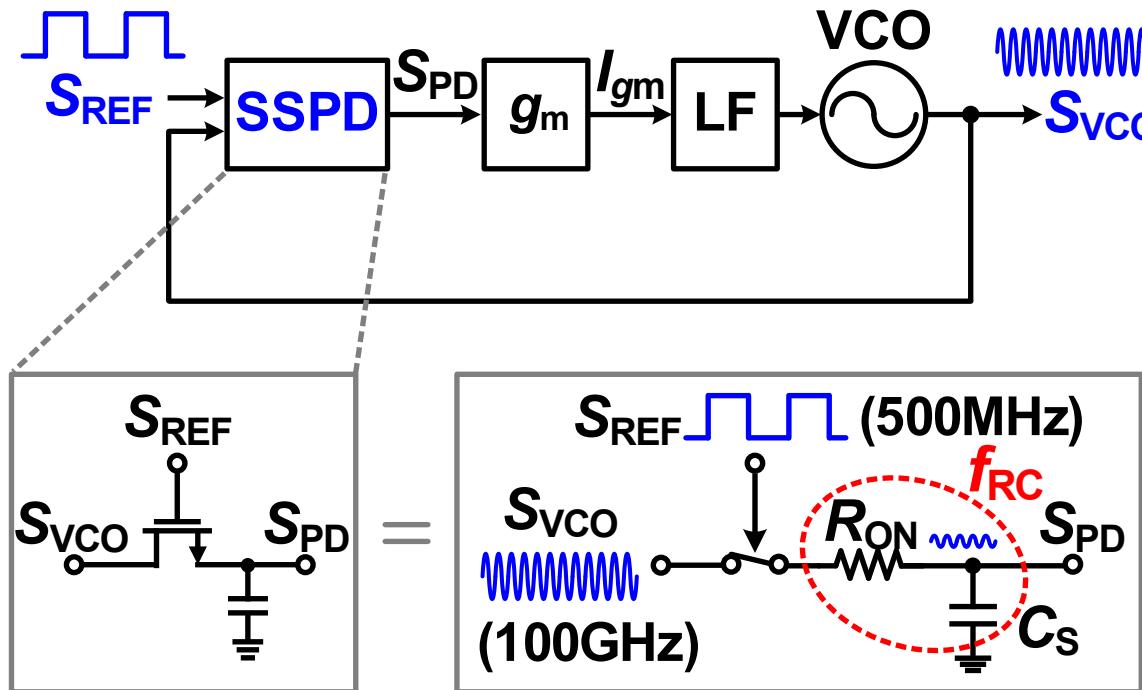
- ❖ Even with wide PLL BW & large N , high **SSPD gain** due to high VCO dv/dt slew rate can result in **low in-band PN** and thus **low overall jitter** 😊
- ❖ **Low power consumption** by eliminating high frequency divider 😊

Alternative Architecture: Sub-Sampling PLL



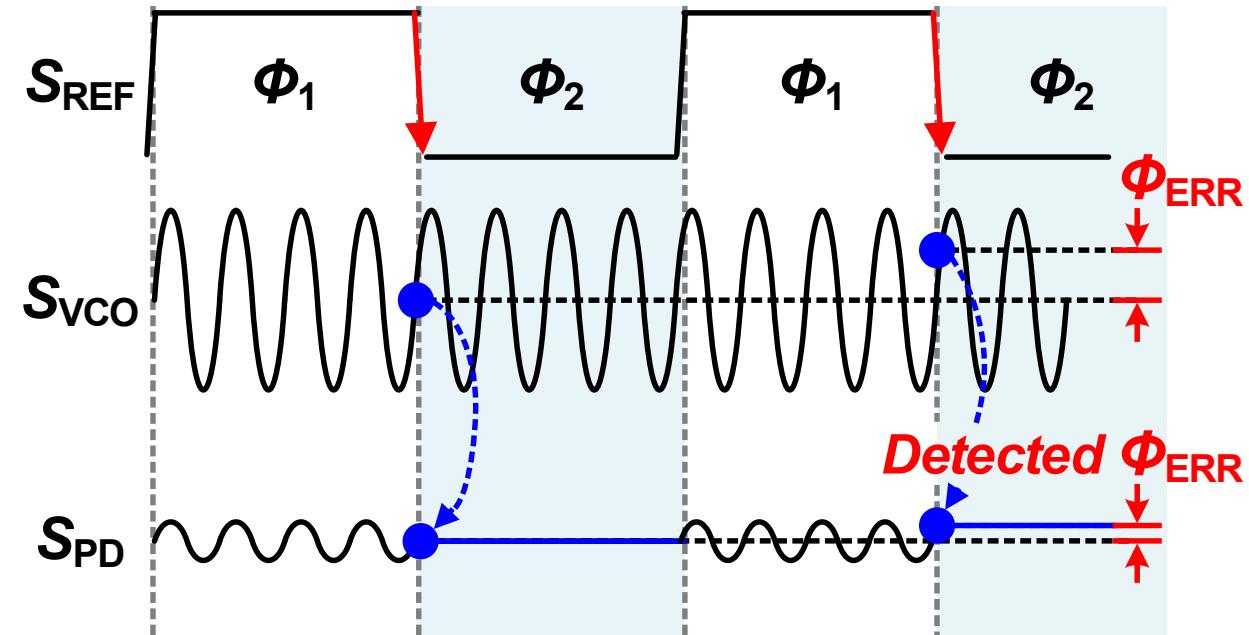
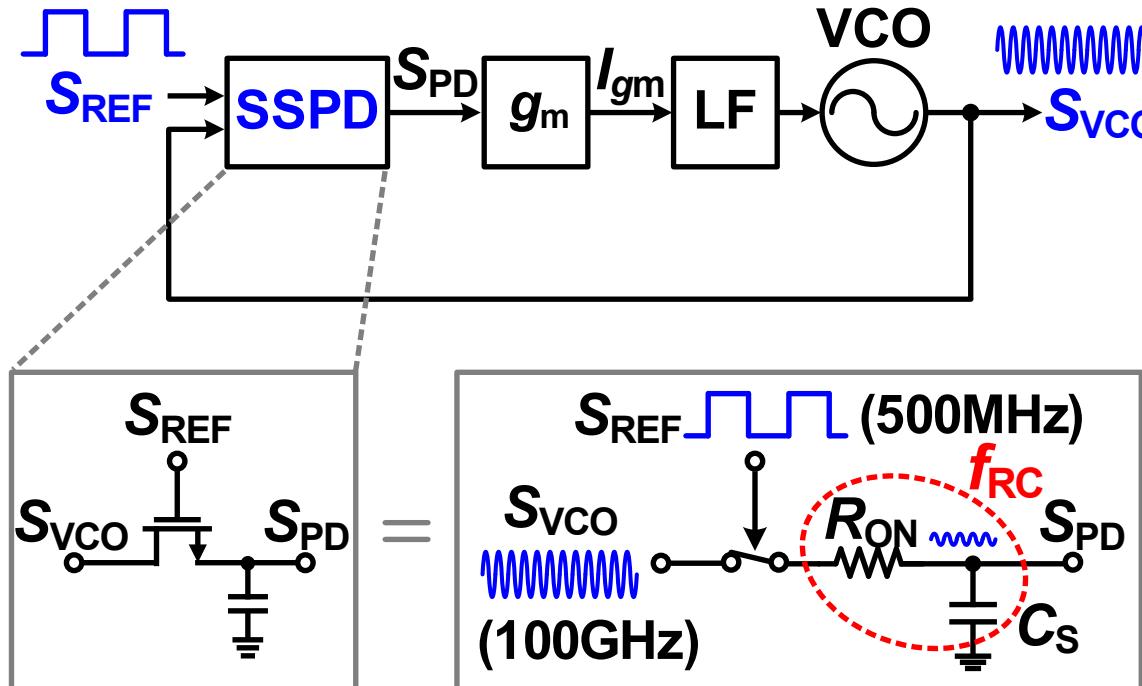
- ❖ SSPD operation interpreted as down-conversion of phase error (Φ_{ERR}) information
- ❖ No loss of Φ_{ERR} information in S_{PD}

Problems of Sub-Sampling PLL in W-Band



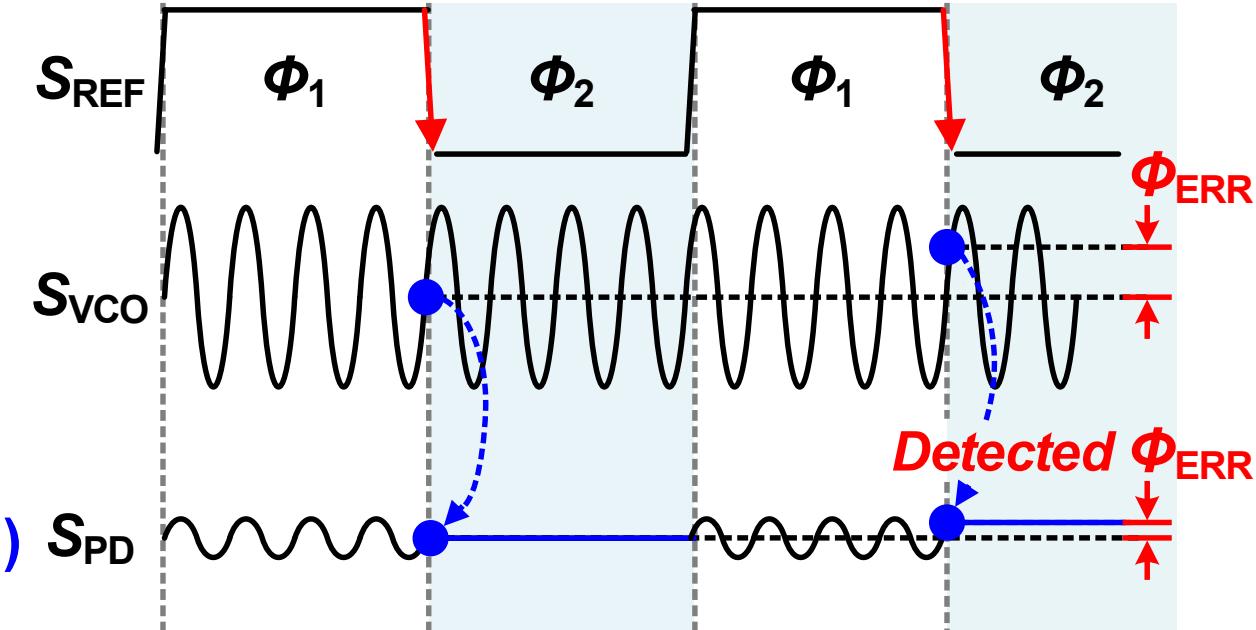
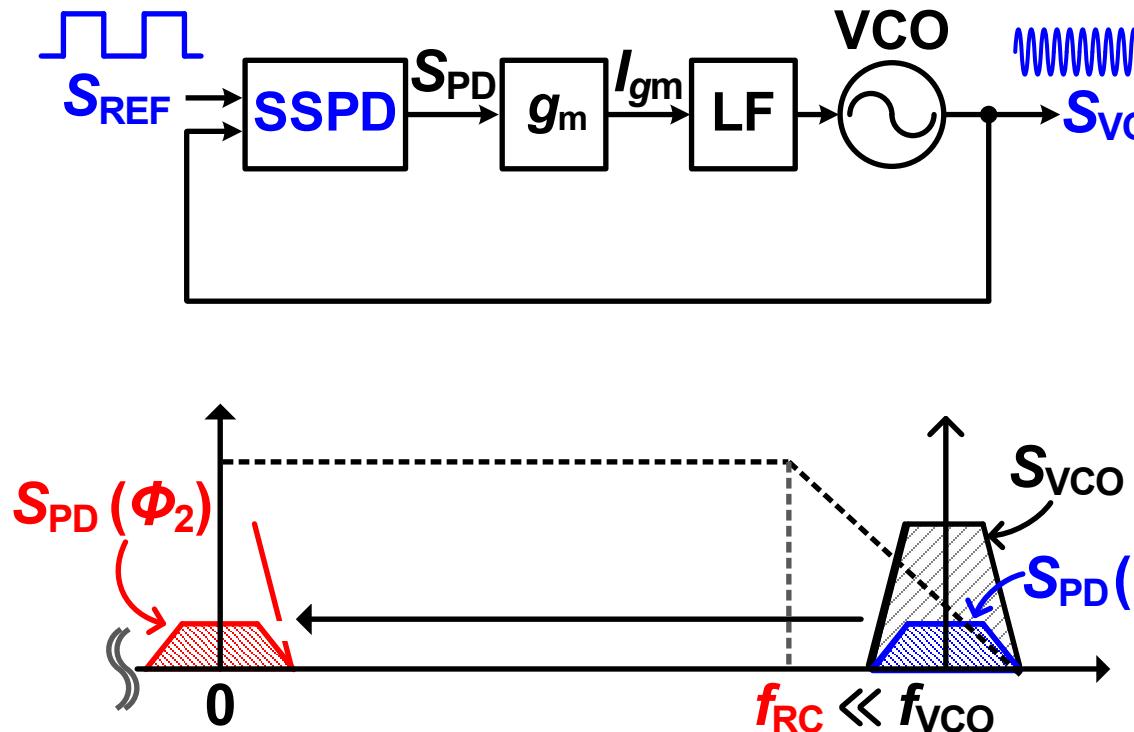
- ❖ In W-band, amplitude of S_{PD} is reduced by parasitic RC pole (f_{RC}) of PD switch
- ❖ Phase error (Φ_{ERR}) information is lost significantly

Problems of Sub-Sampling PLL in W-Band



- ❖ In W-band, amplitude of S_{PD} is reduced by parasitic RC pole (f_{RC}) of PD switch
- ❖ Phase error (Φ_{ERR}) information is lost significantly

Problems of Sub-Sampling PLL in W-Band



- ❖ In W-band, Φ_{ERR} info. is lost due to RC pole of PD switch before down-conversion
- ➔ Losing its merit of high ϕ_{ERR} -detection gain 😞

Outline

❖ Introduction

- Demands of Low-Jitter W-Band PLL
- Problems of conventional W-Band PLLs

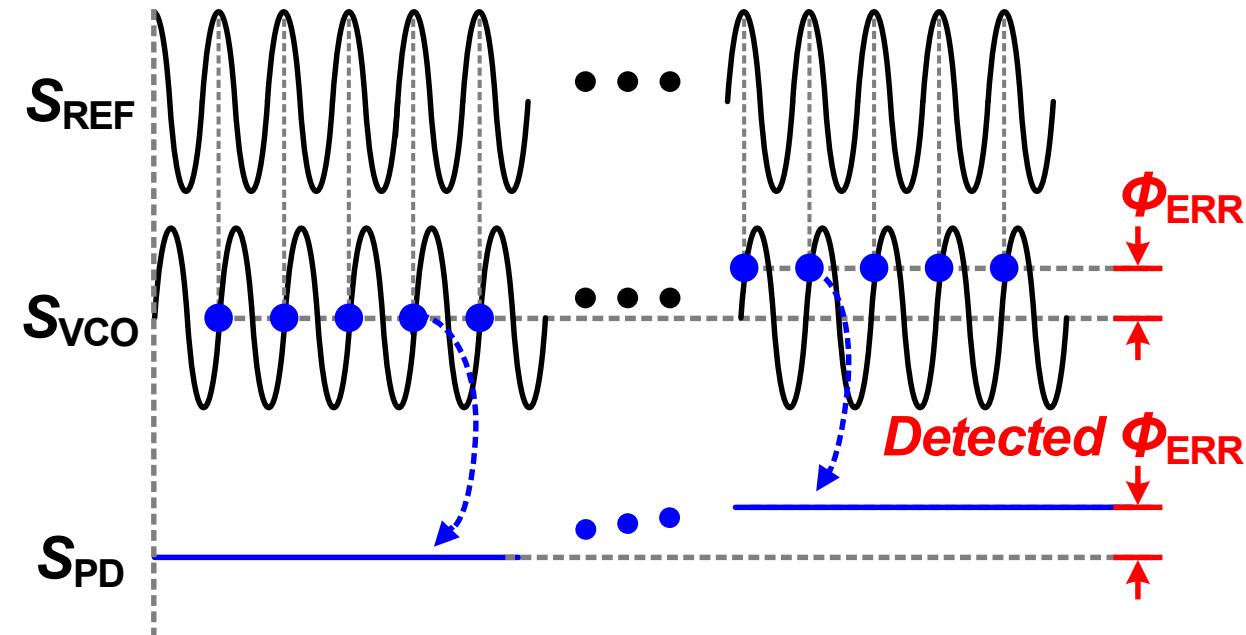
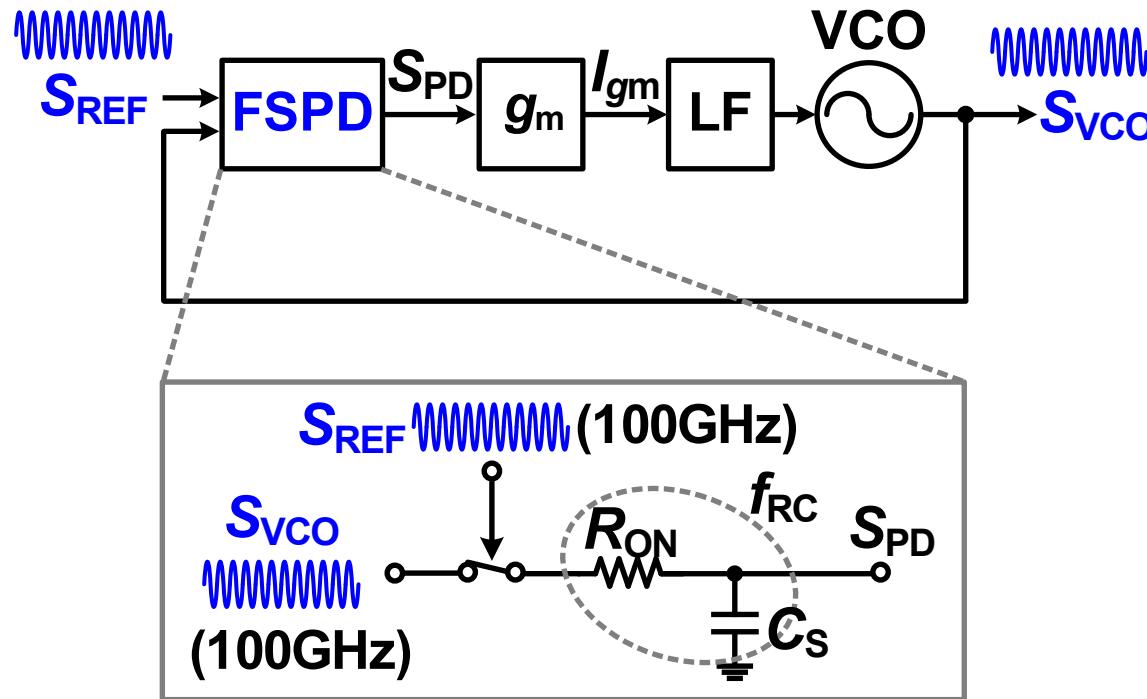
❖ Proposed W-Band PLL with PG-ILFM-based PD

- Concept of Proposed PG-ILFM-based PD
- Operation of PLL & Frequency Offset Canceller (FOC)
- Noise Analysis

❖ Measurements and Performance Comparison

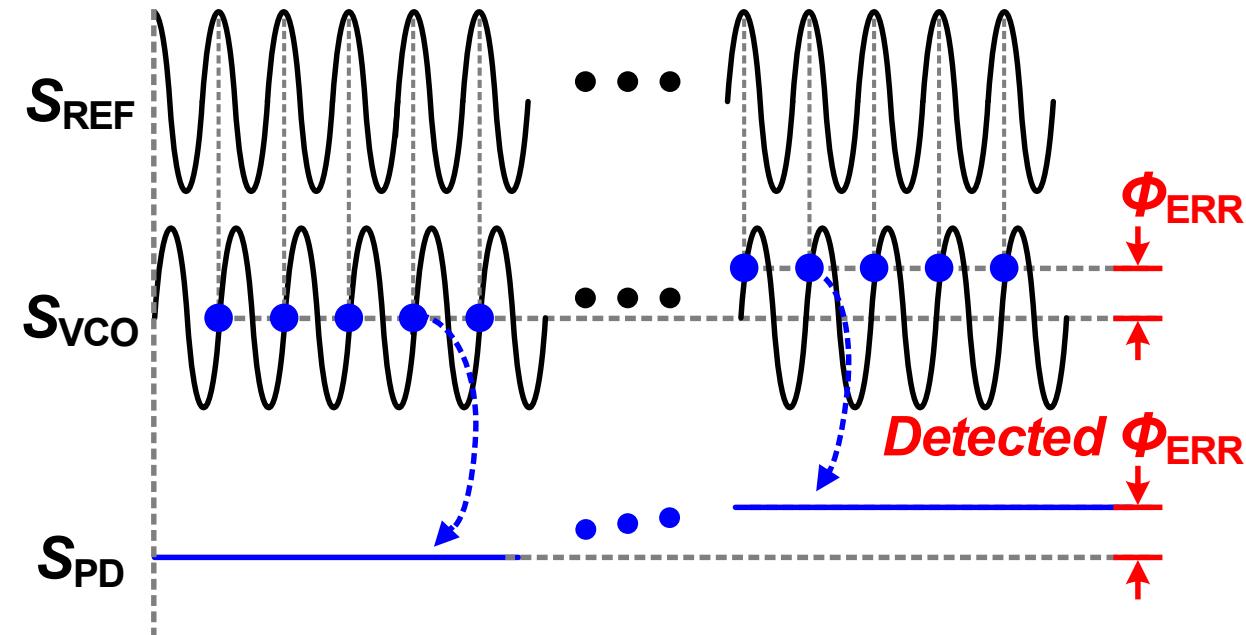
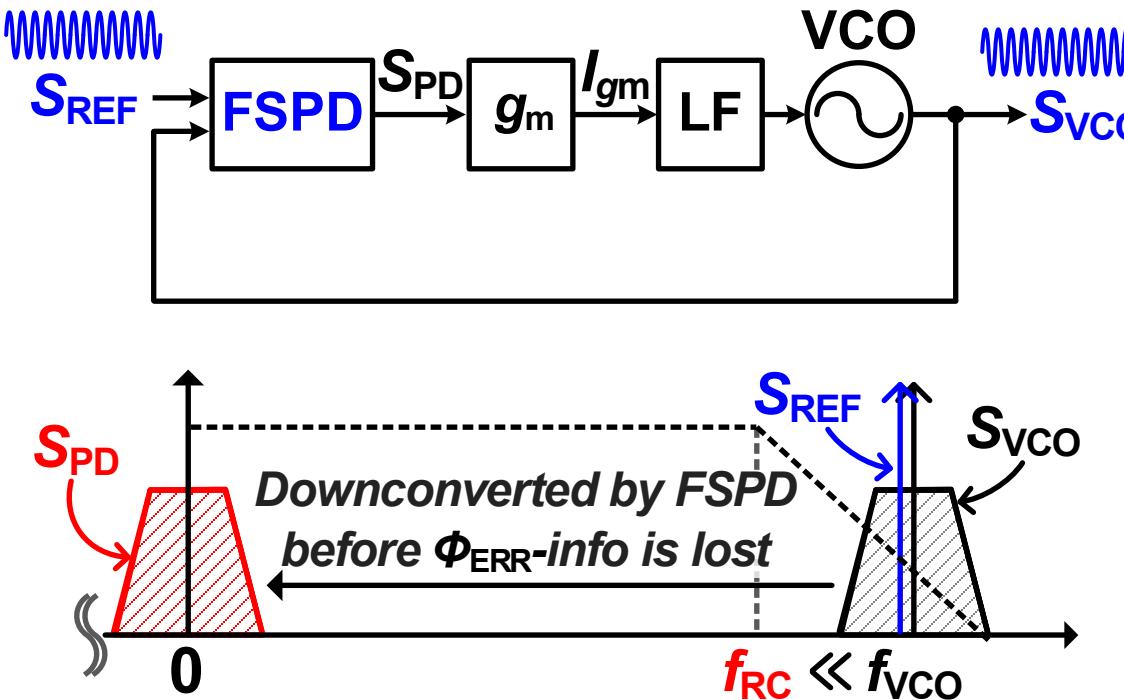
❖ Conclusions

Concept of Fundamental-Sampling PD-based W-Band PLL



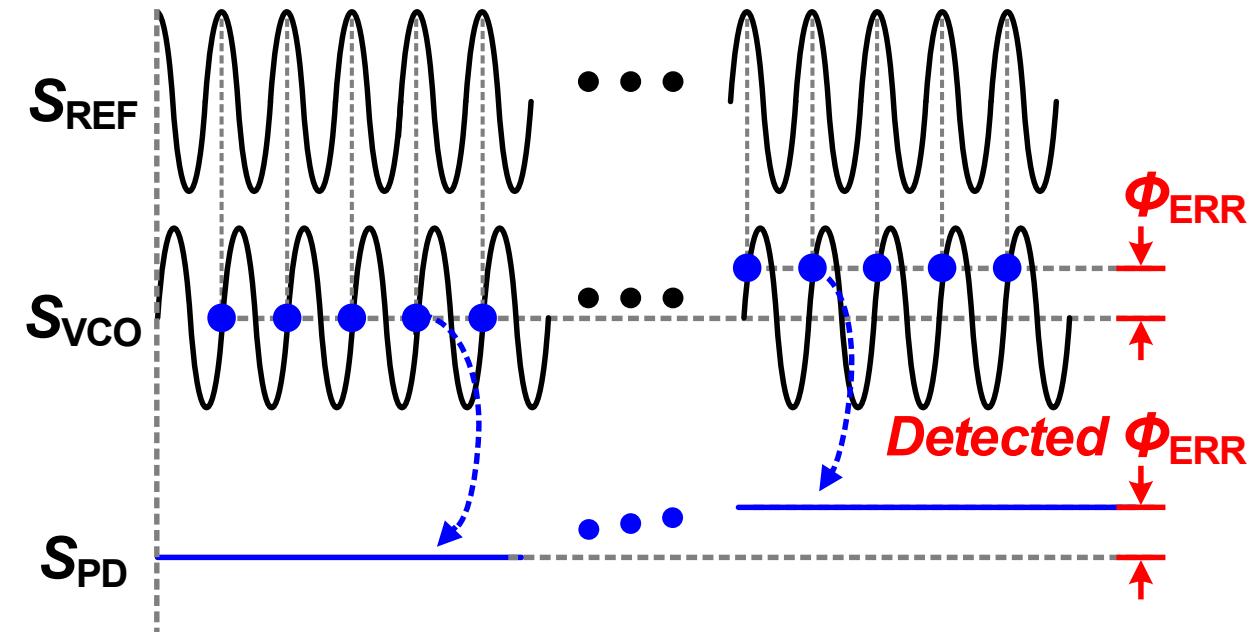
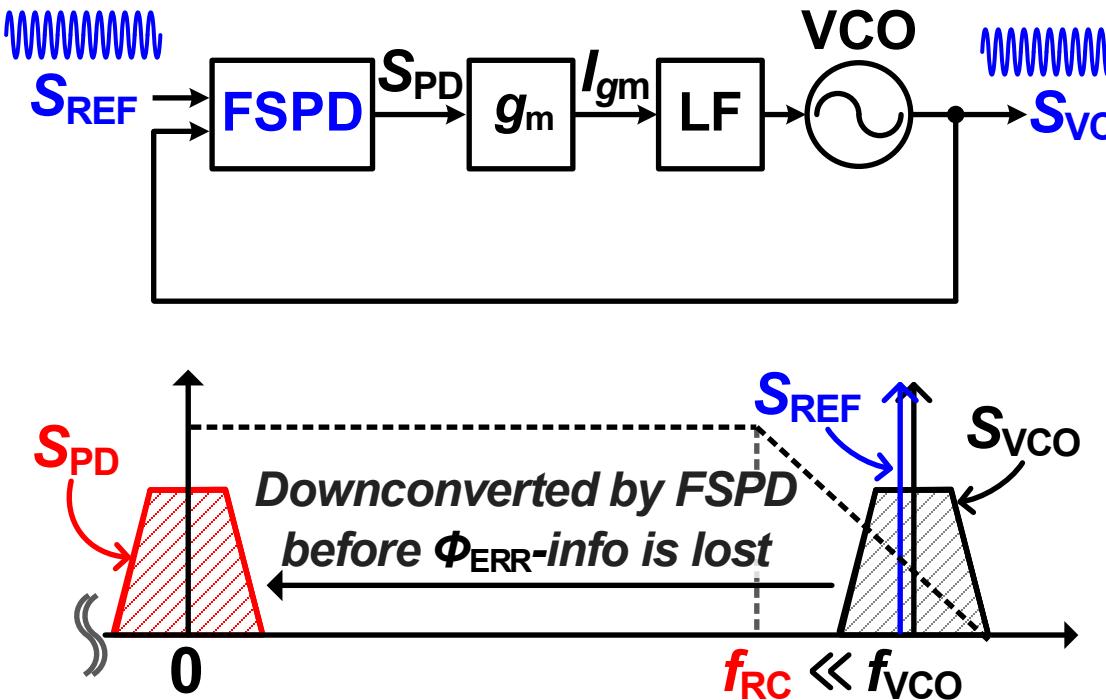
- ❖ Fundamental sampling PD (FSPD): sampling S_{vco} with S_{REF} having same freq.
- ❖ If we can use 100GHz S_{REF} ,
 Φ_{ERR} information can be detected without loss due to the RC pole of PD SW

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 Φ_{ERR} information can be detected without loss due to the RC pole of PD SW

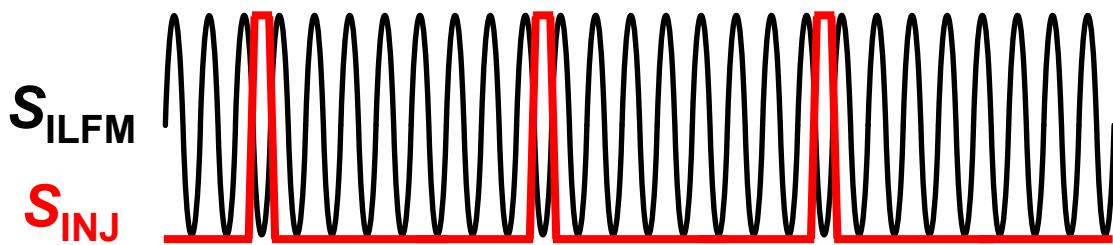
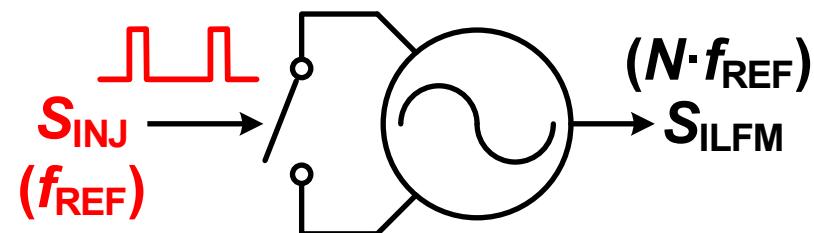
Concept of Fundamental-Sampling PD-based W-Band PLL



- ❖ Fundamental sampling signal should have...
- ➔ Low jitter at a **high frequency** near f_{VCO} in W-band ☹
- ➔ But **no need to be continuous** ☺

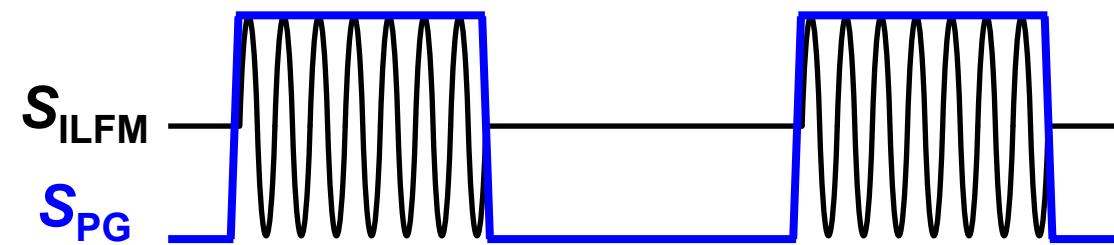
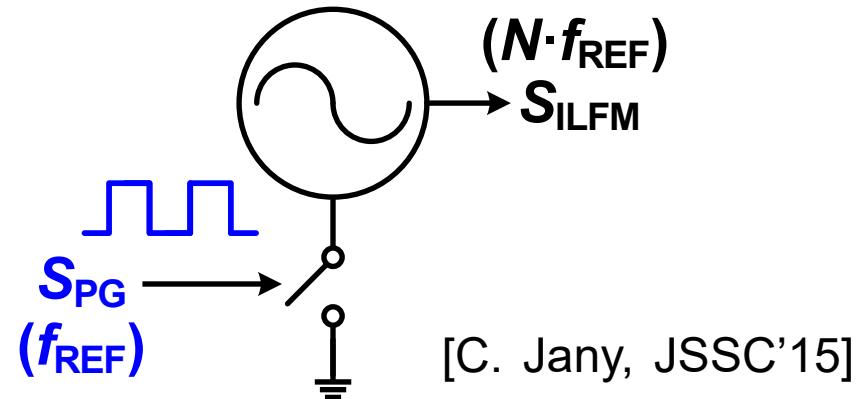
How to Generate 100GHz Sampling Frequency?

Typical Injection Locked FM (ILFM)



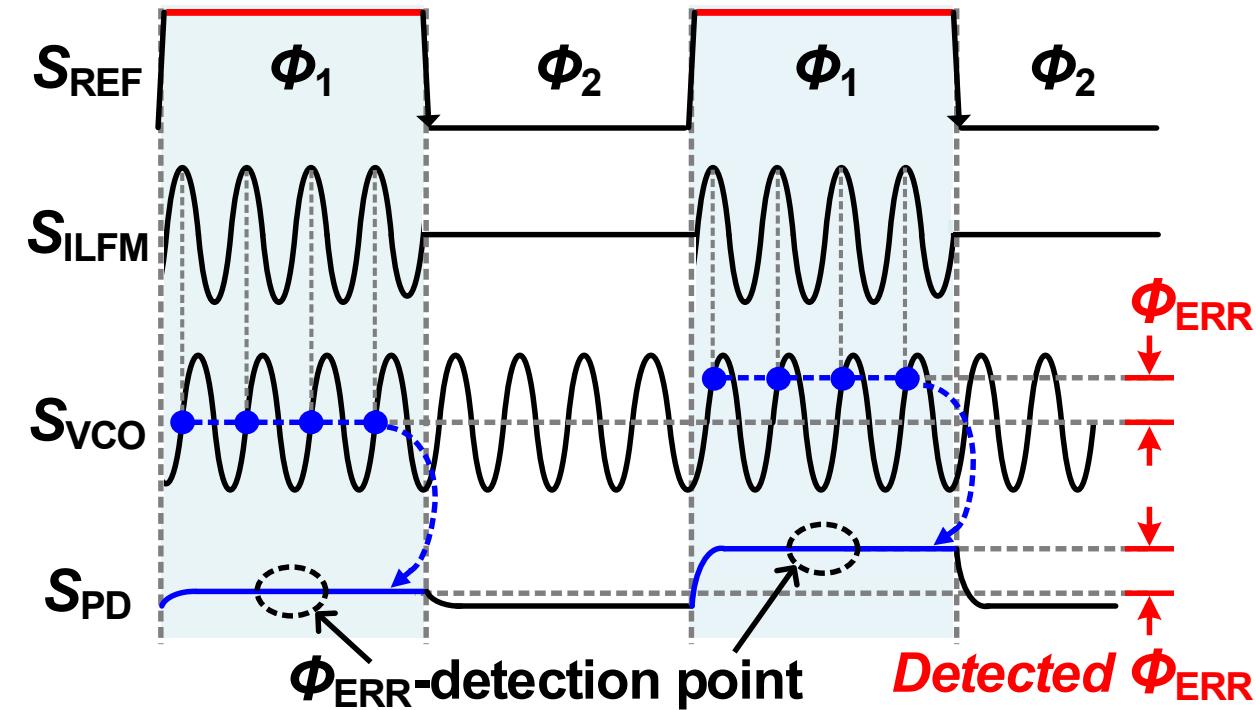
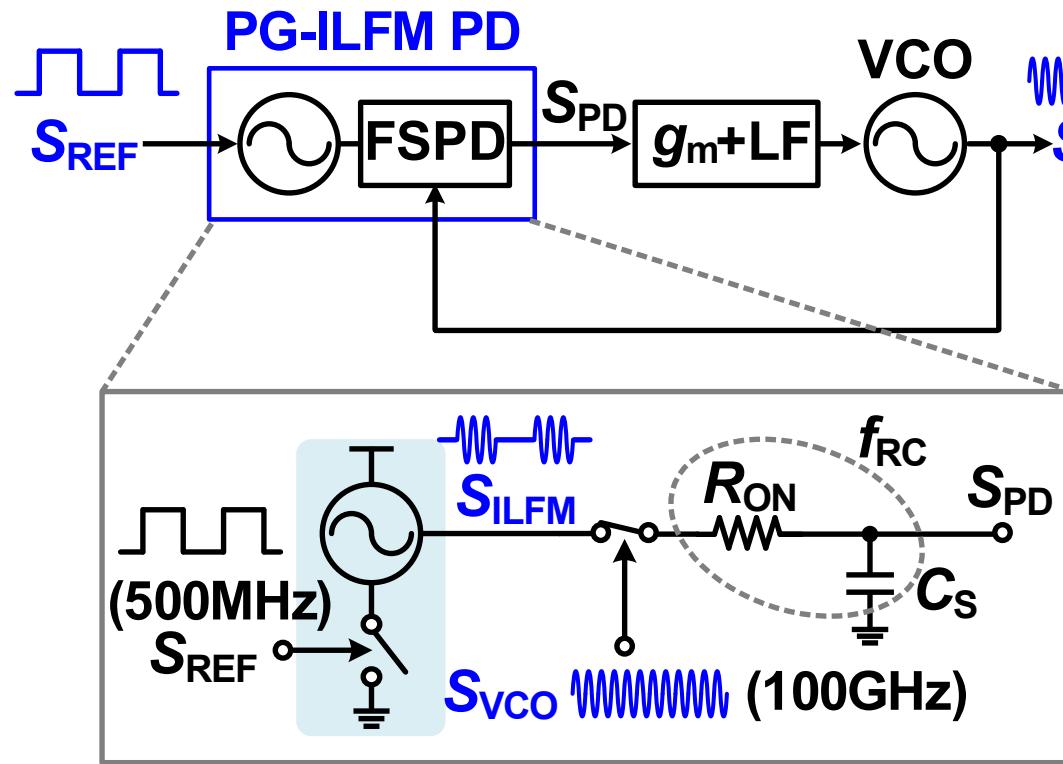
- ❖ Short-pulse injection to output node
→ Narrow lock range & poor jitter for large N more than 100 ☹

Power-Gating ILFM (PG-ILFM)



- ❖ Repetitive on/off the power of VCO
→ Wide lock range & low jitter for large N more than 100 ☺

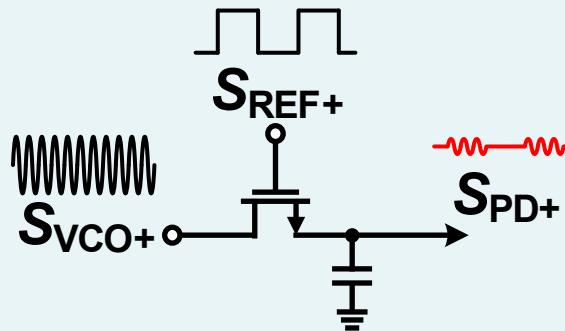
Concept of Proposed PG-ILFM PD-based W-Band PLL



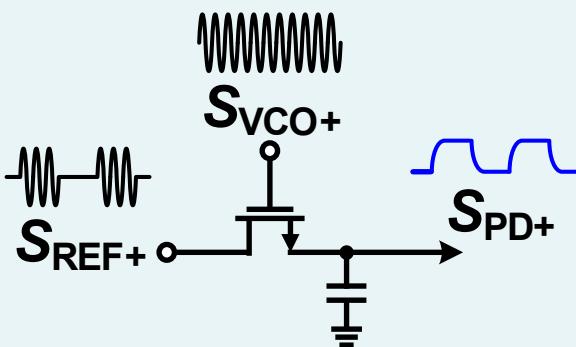
- ❖ Using power-gating ILFM (PG-ILFM) and fundamental sampling PD (FSPD), high Φ_{ERR} -detection gain can be achieved in W-Band ☺

Simulation for Φ_{ERR} -Detection Gain Comparison

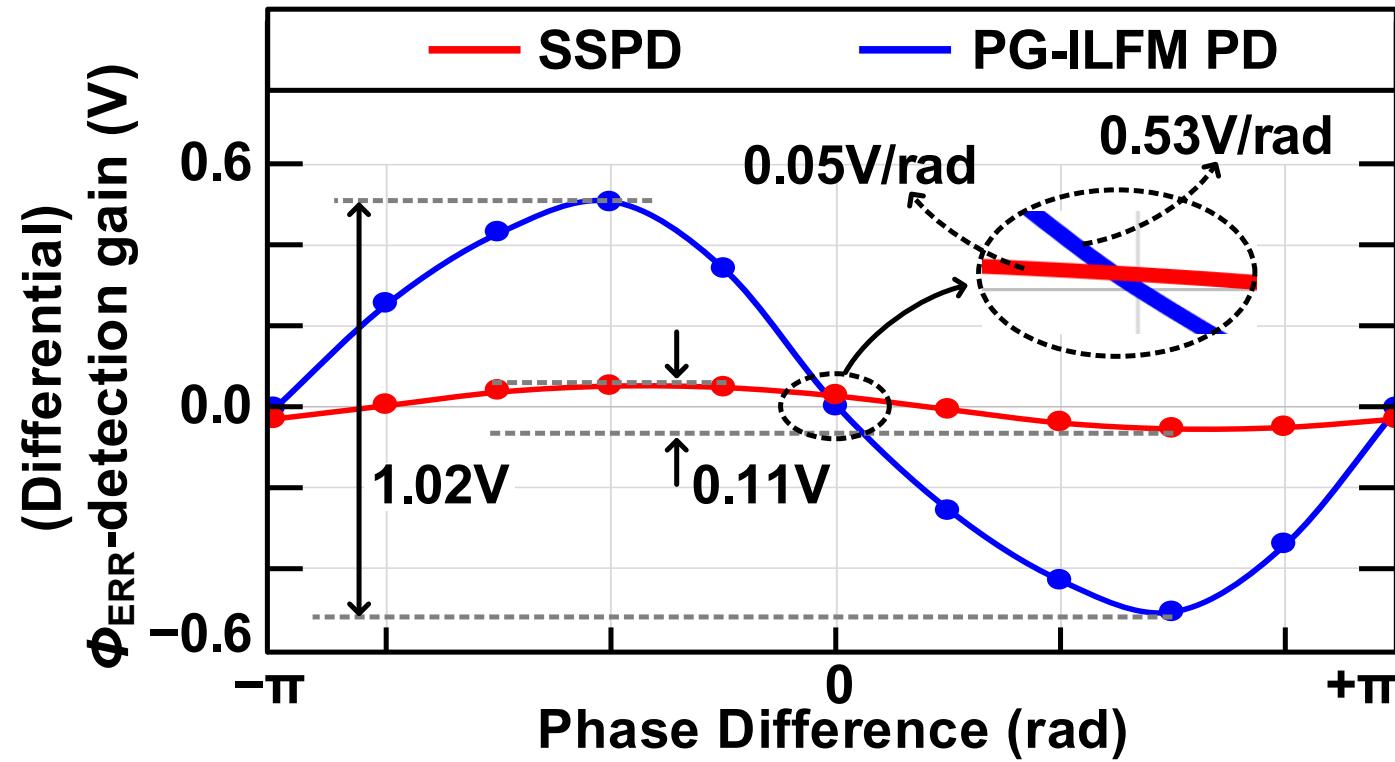
Sub-Sampling PD ☹



PG-ILFM-based PD ☺

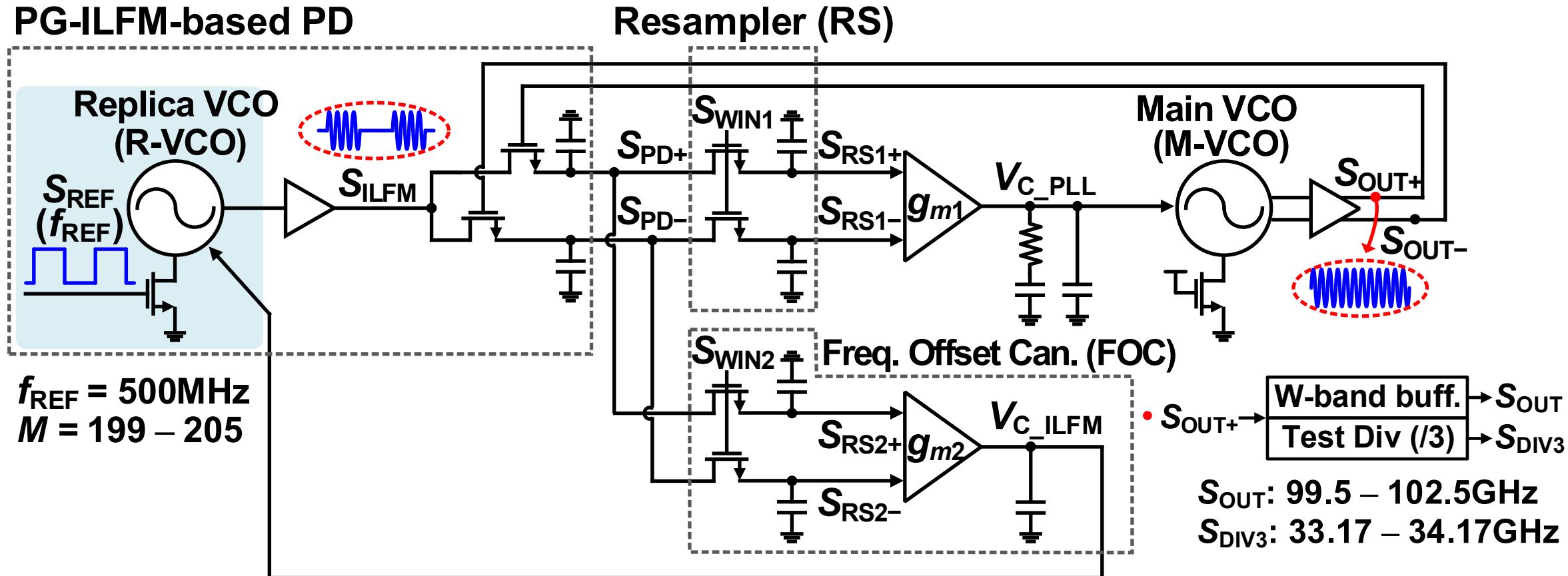


- $f_{\text{REF}} = 500\text{MHz}$, $f_{\text{VCO}} = 102\text{GHz}$, $N = 204$
- NMOS switch size = 700n/60n



→ PD gain (V/rad) of PG-ILFM PD = 0.53 >> SSPD = 0.05

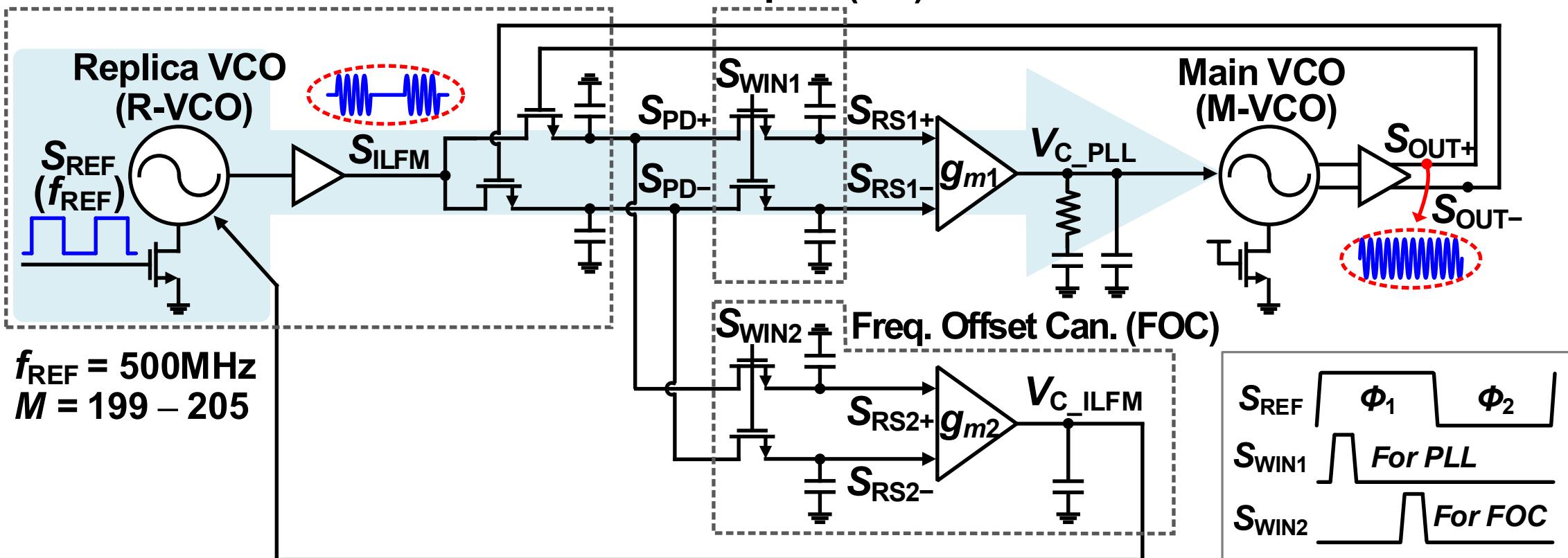
Overall Architecture of Proposed W-Band PLL w/ FOC



- ❖ Consisting of PG-ILFM-based PD, Resampler (RS), Freq. Offset Canceller (FOC), g_m amplifier, LF, and Main VCO

W-Band PLL

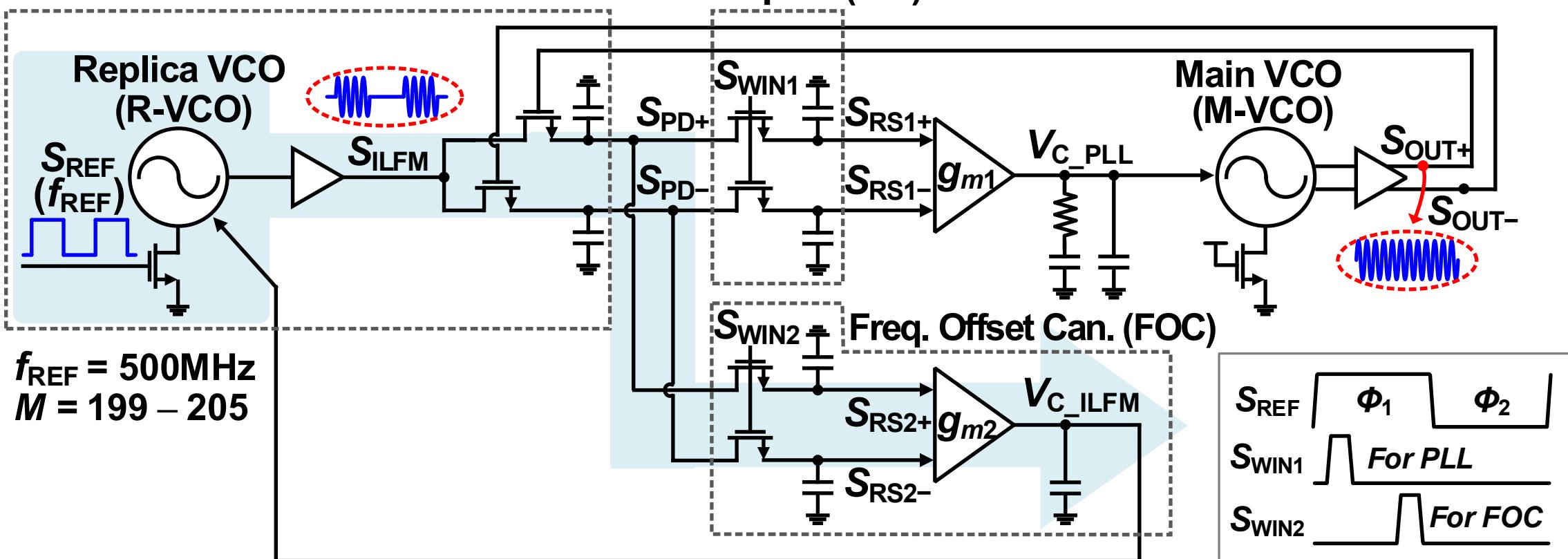
PG-ILFM-based PD



❖ Main PLL: to remove Φ_{ERR} of PLL output

Frequency Offset Canceller (FOC)

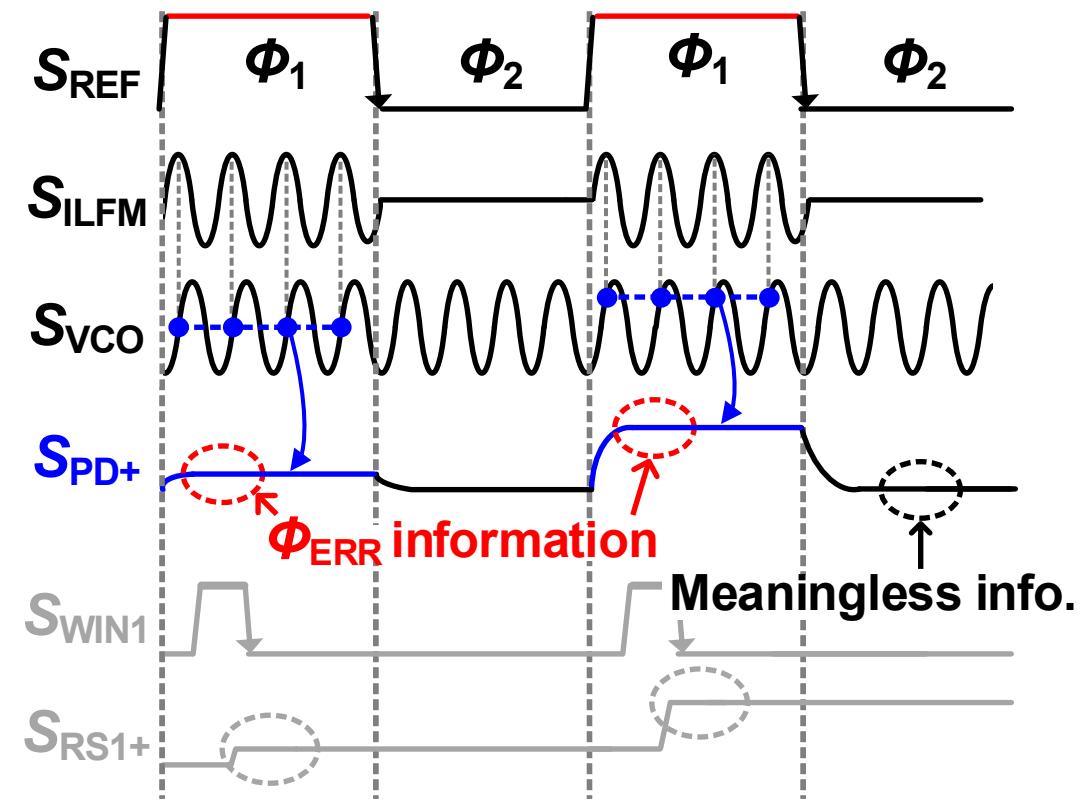
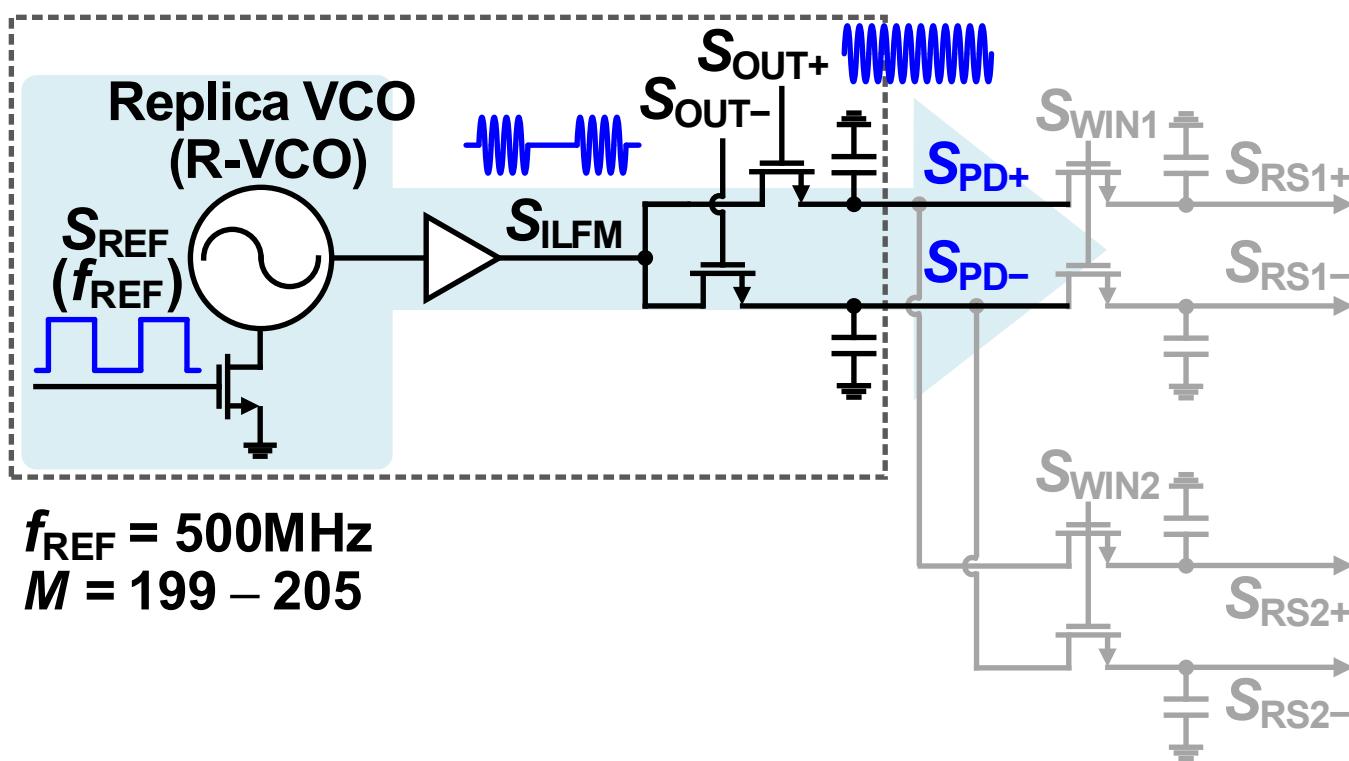
PG-ILFM-based PD



- ❖ Freq. Offset Canceller (FOC): to cancel freq. offset btw. main and replica VCOs
- ❖ PLL and FOC operate sequentially in different points of ϕ_1

Operation of PG-ILFM-based PD

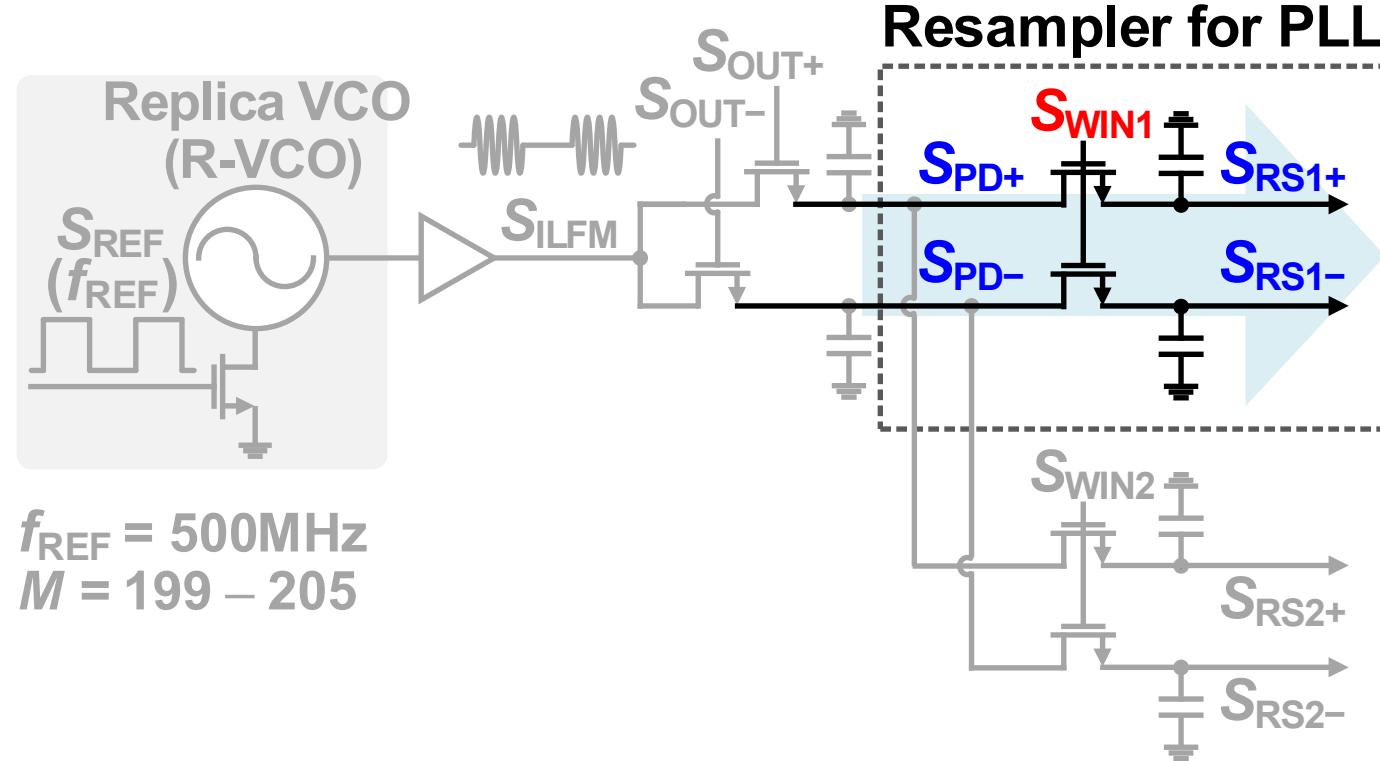
PG-ILFM-based PD



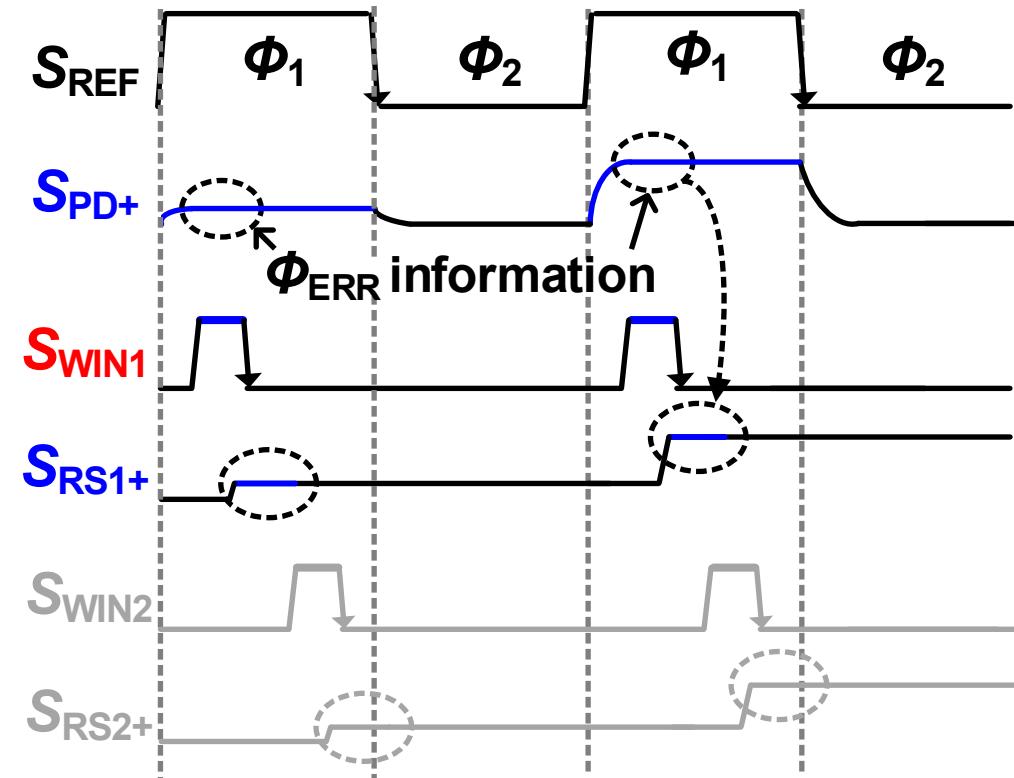
- ❖ During Φ_1 , Φ_{ERR} information obtained in S_{PD}

Operation of Resampler of W-Band PLL

PG-ILFM-based PD



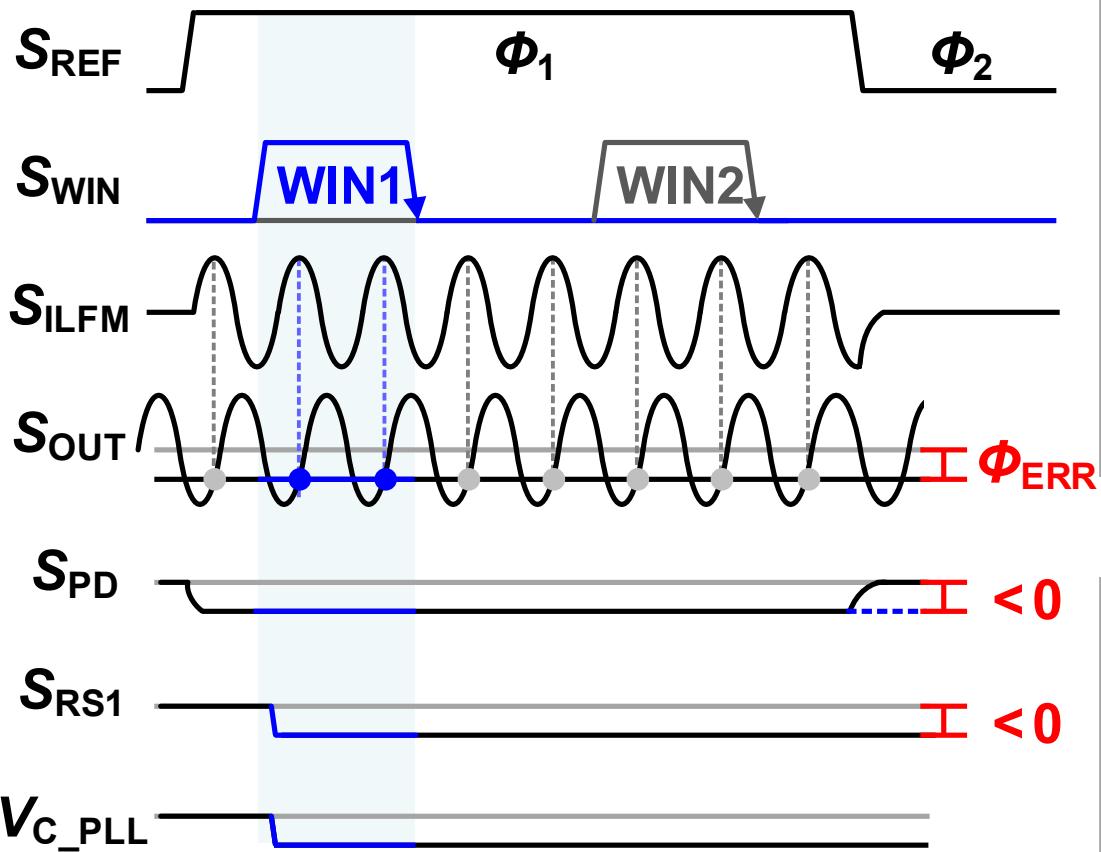
$$f_{\text{REF}} = 500\text{MHz}$$
$$M = 199 - 205$$



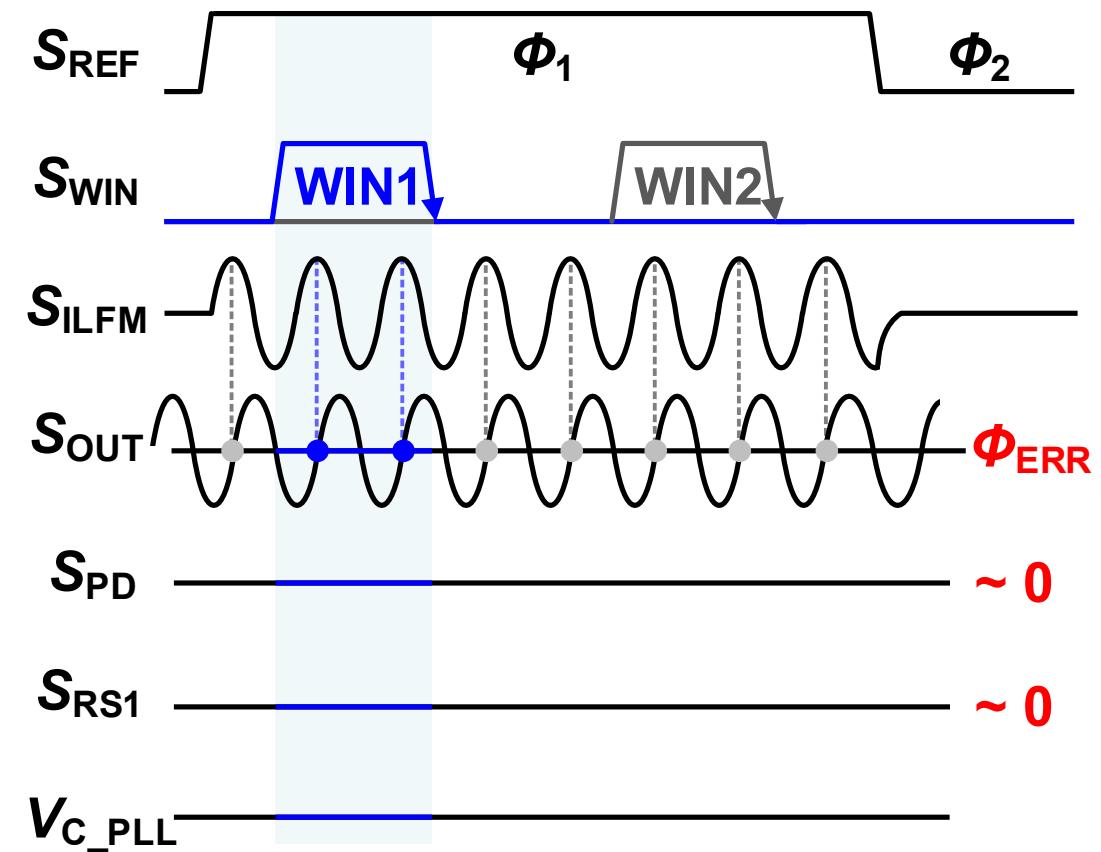
- ❖ $S_{\text{WIN}1}$ transferring only meaningful information of ϕ_{ERR} in S_{PD} to $S_{\text{RS}1}$
- ❖ Resampler suppressing spurs at f_{REF} multiples

Timing Diagram of PLL Operation

Case I) $\Phi_{\text{ERR}} \neq 0$

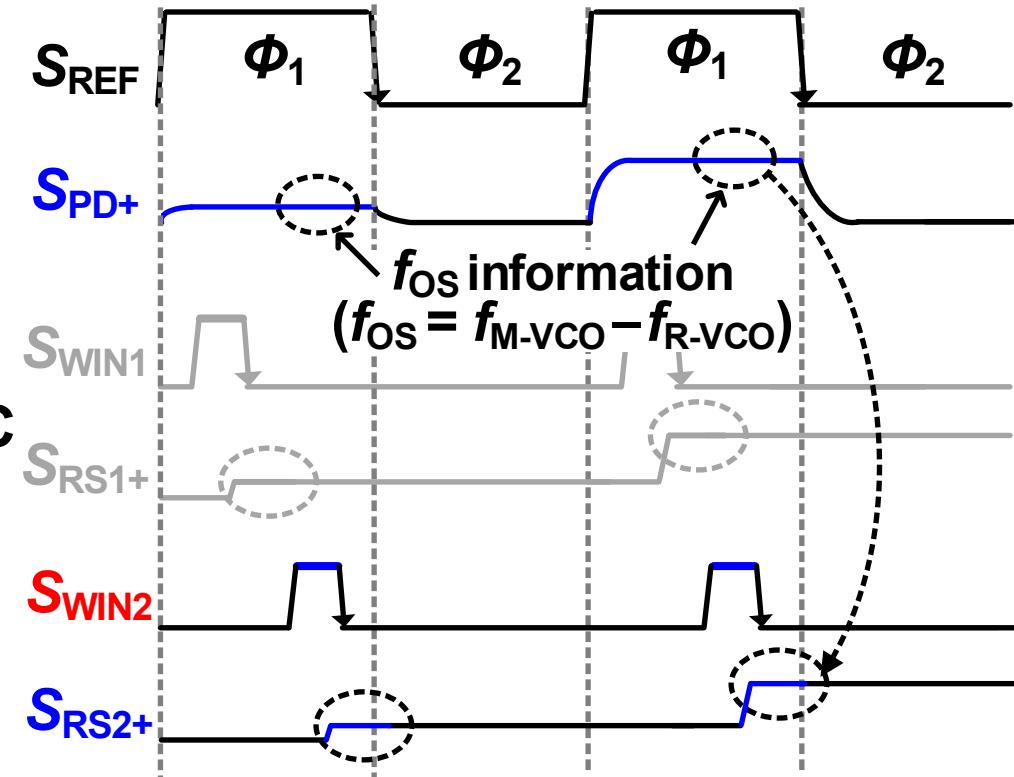
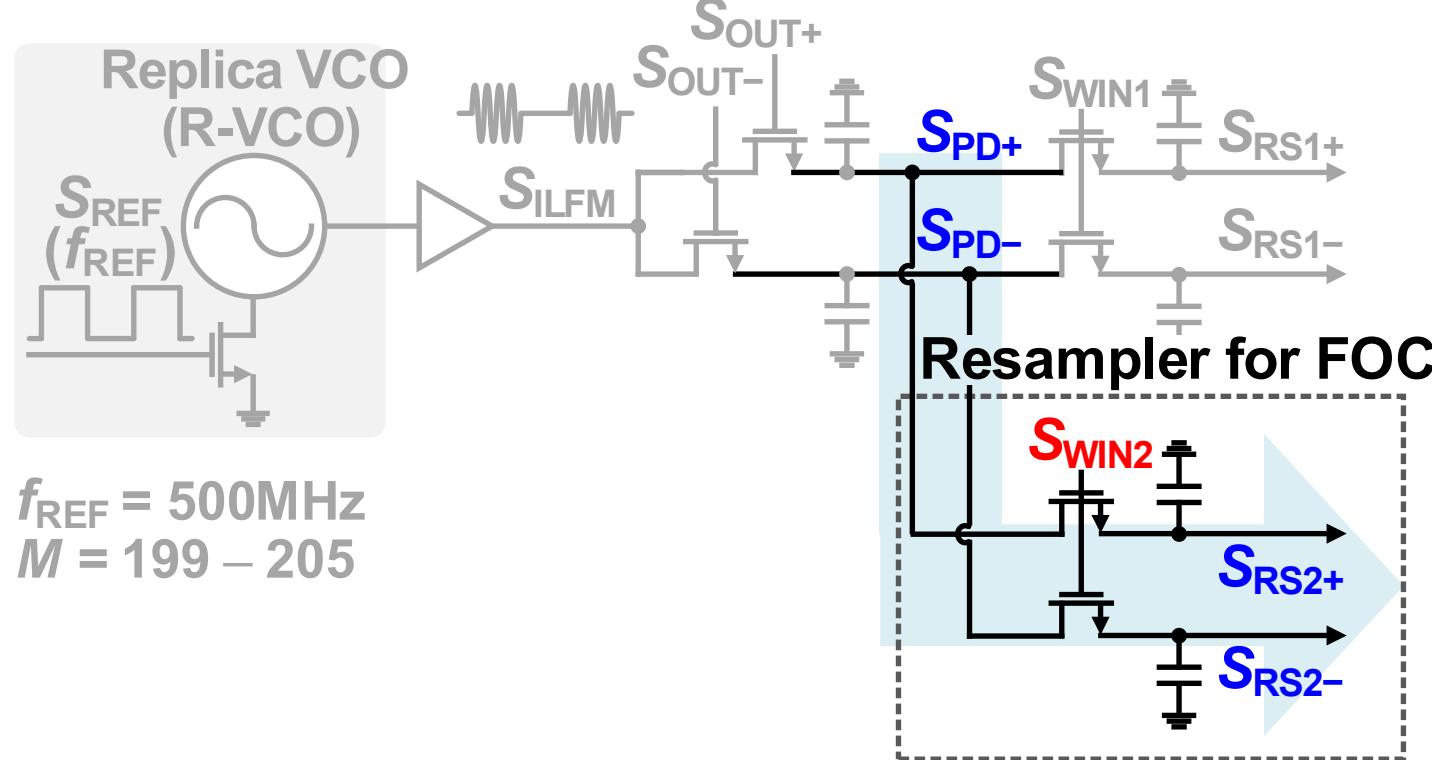


Case II) $\Phi_{\text{ERR}} = 0$



Operation of Resampler of FOC

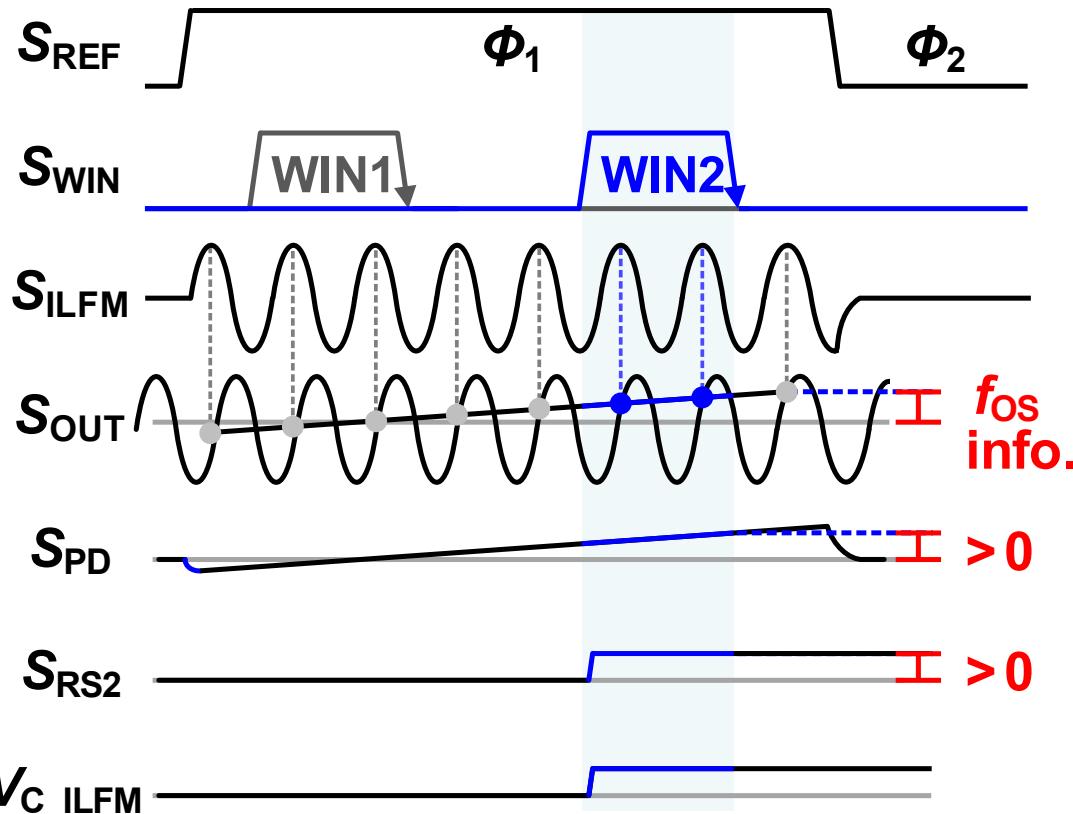
PG-ILFM-based PD



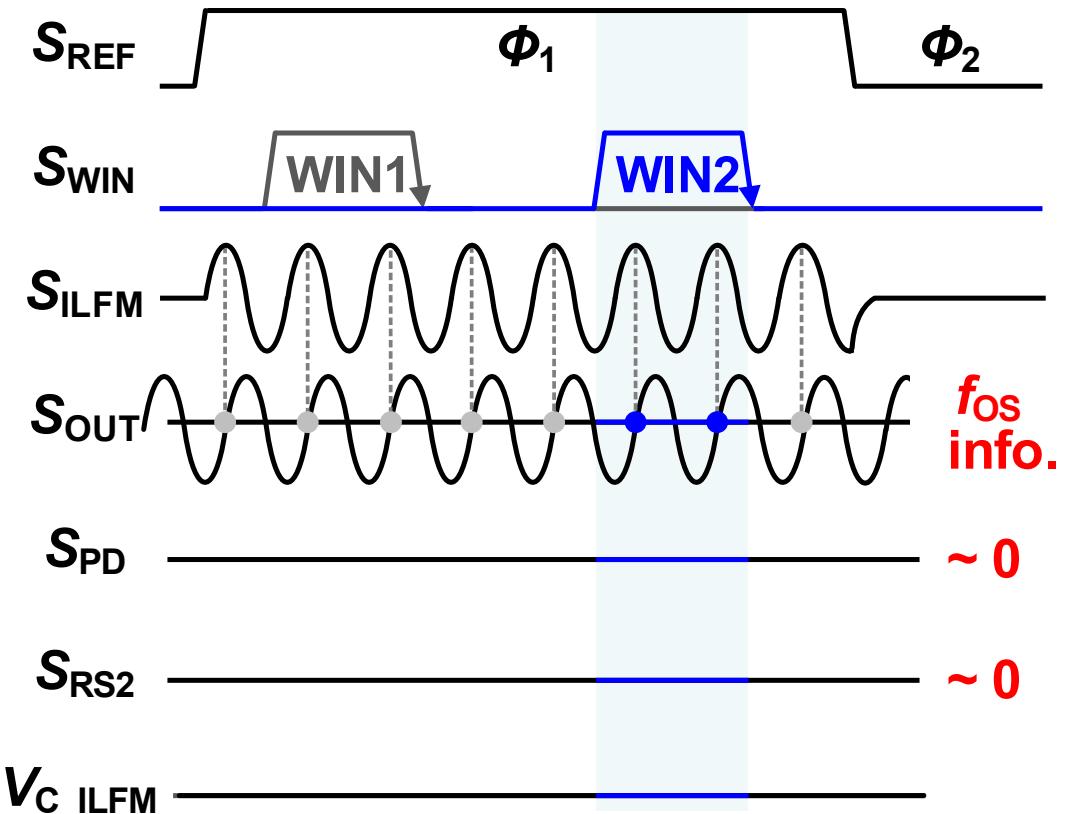
- ❖ FOC canceling frequency offset between M-VCO and R-VCO
- Maintaining high Φ_{ERR} -detection gain, thereby generating ultra-low jitter S_{OUT}
- ❖ S_{WIN2} transferring information of f_{os} & time-interleaved operation with S_{WIN1}

Timing Diagram of FOC Operation

Case I) $f_{R\text{-vco}} < f_{M\text{-vco}} = N \cdot f_{\text{REF}}$

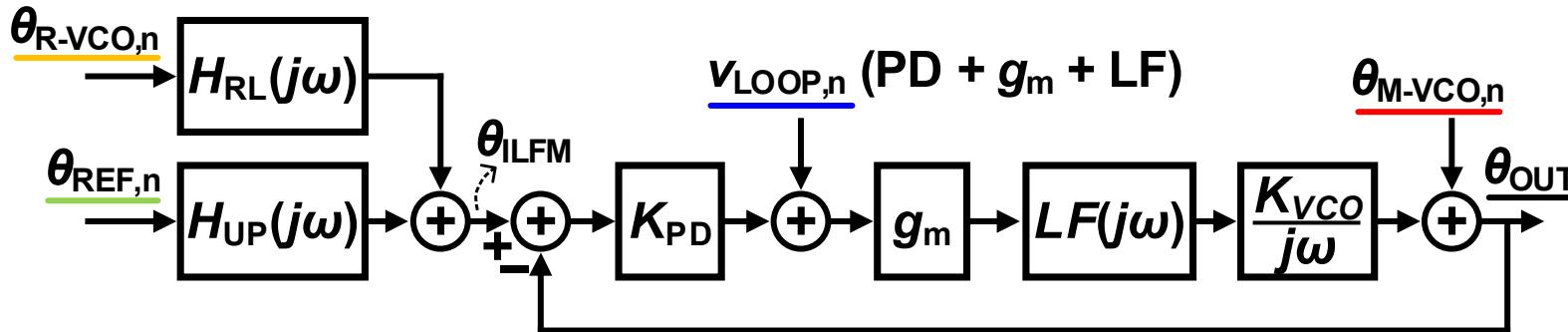


Case II) $f_{R\text{-vco}} = f_{M\text{-vco}} = N \cdot f_{\text{REF}}$



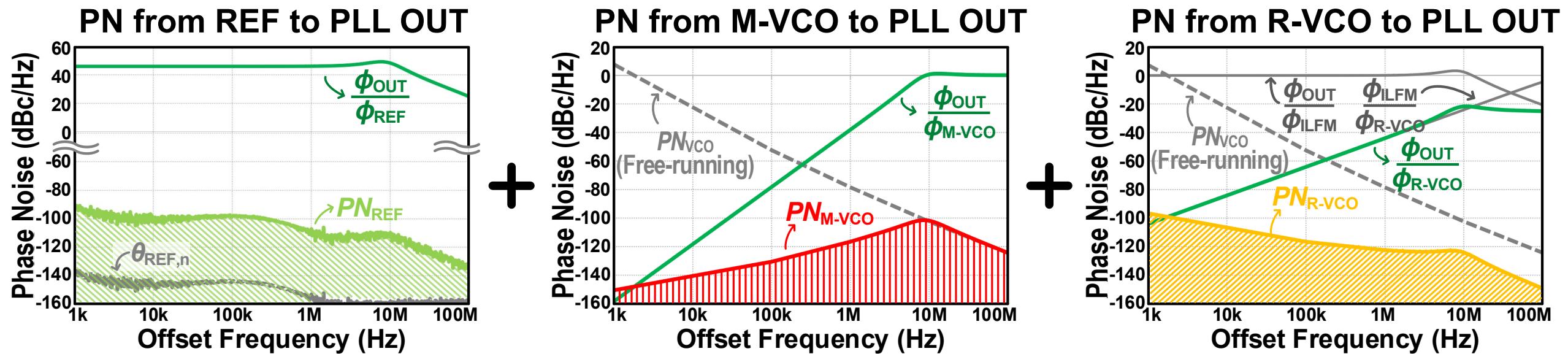
❖ f_{OUT} locked to $N \cdot f_{\text{REF}}$ since PLL BW \gg FOC BW

Noise Analysis of W-Band PLL ($K_{PD} = 0.53\text{V/rad}$)



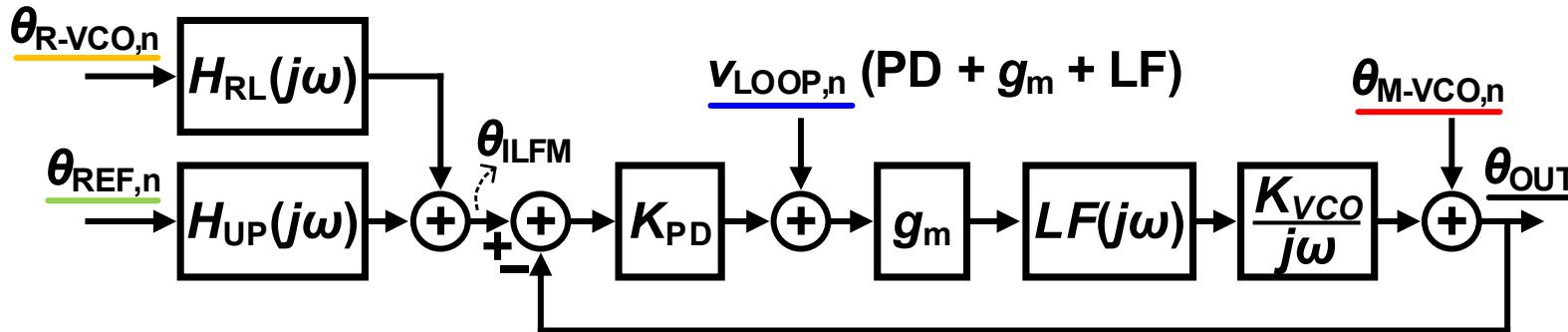
$$H_{UP}(j\omega) = \frac{N \cdot \beta \cdot e^{-j\omega T_{REF}/2}}{1 + (\beta - 1)e^{-j\omega T_{REF}/2}} \frac{\sin(\omega T_{REF}/2)}{\omega T_{REF}/2}$$

$$H_{RL}(j\omega) = 1 - \frac{\beta \cdot e^{-j\omega T_{REF}/2}}{1 + (\beta - 1)e^{-j\omega T_{REF}/2}} \frac{\sin(\omega T_{REF}/2)}{\omega T_{REF}/2}$$



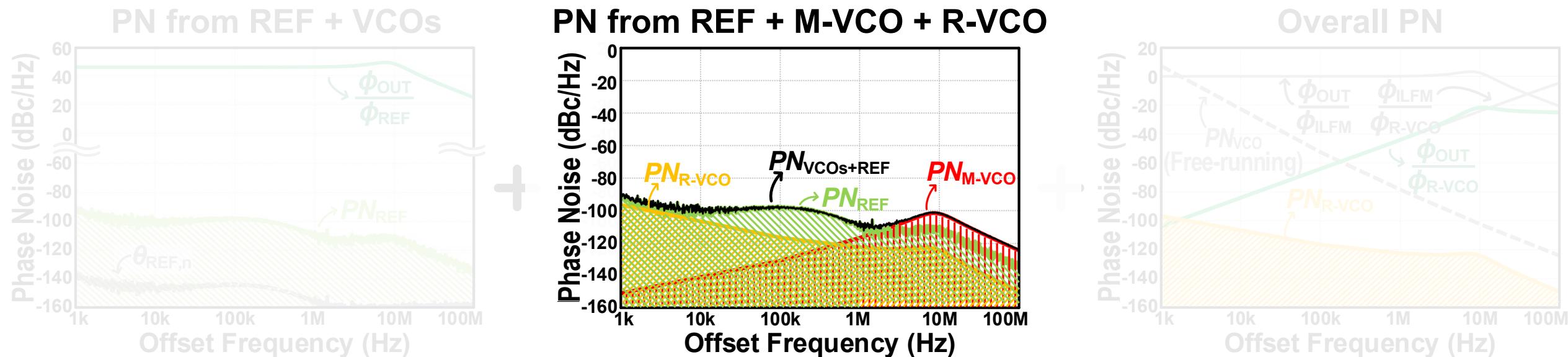
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- ❖ Due to wide Inj. BW & PLL BW, PN of W-band R-VCO can be ignored

Noise Analysis of W-Band PLL ($K_{PD} = 0.53\text{V/rad}$)



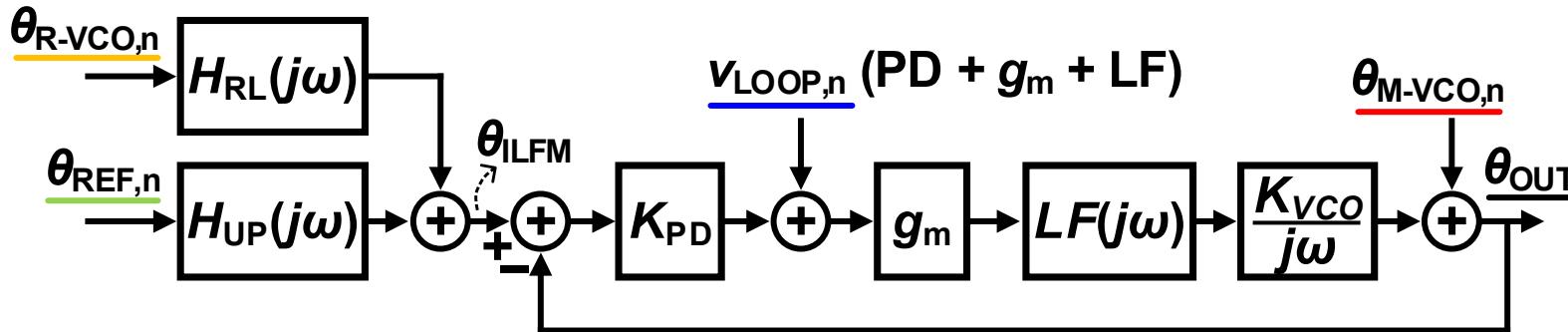
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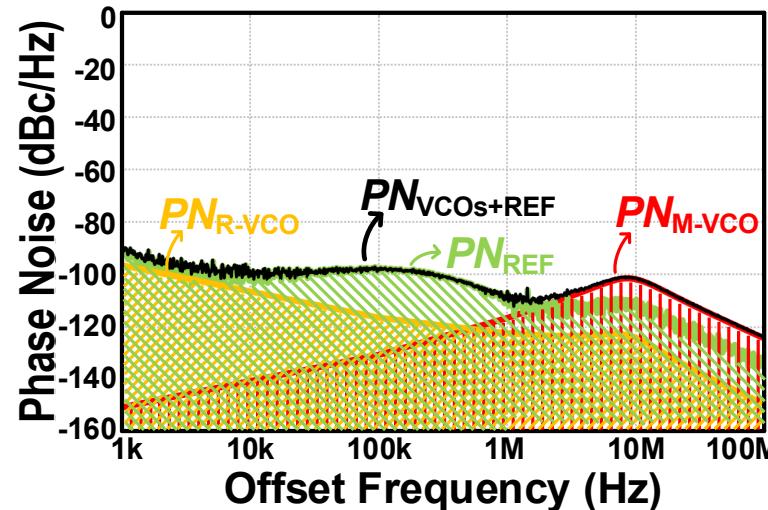
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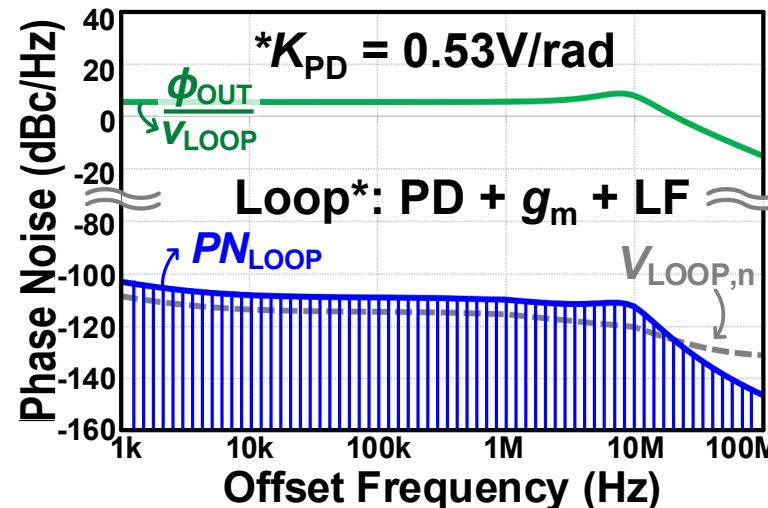
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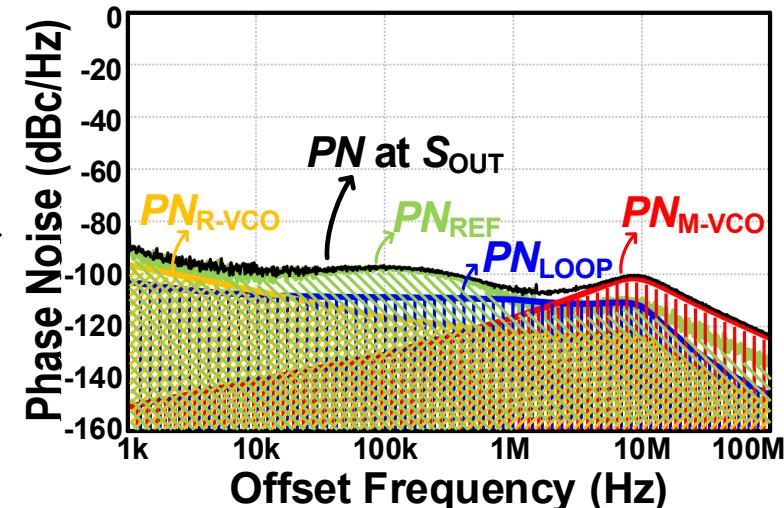
PN from REF + VCOs



PN from Loop*

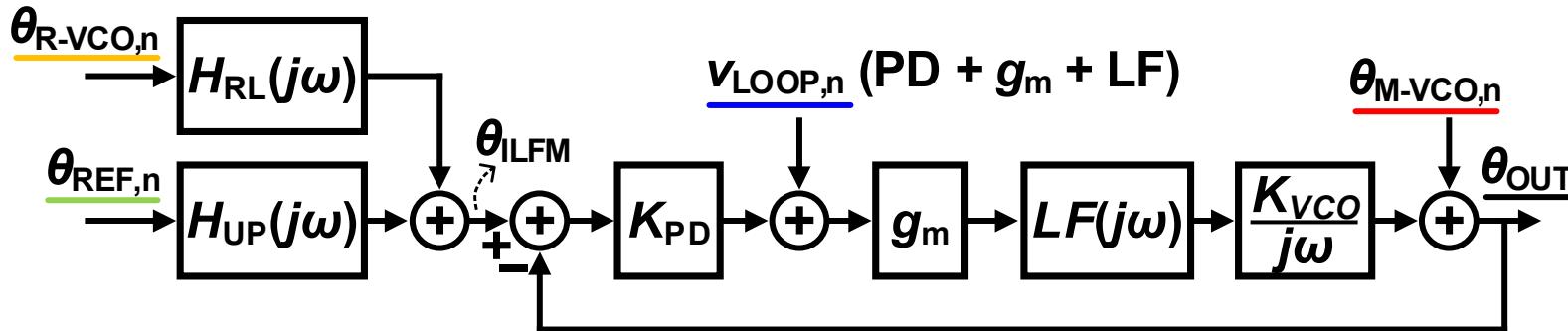


Overall PN



❖ Due to high gain of K_{PD} , PN_{LOOP} have non-critical impact on the overall noise

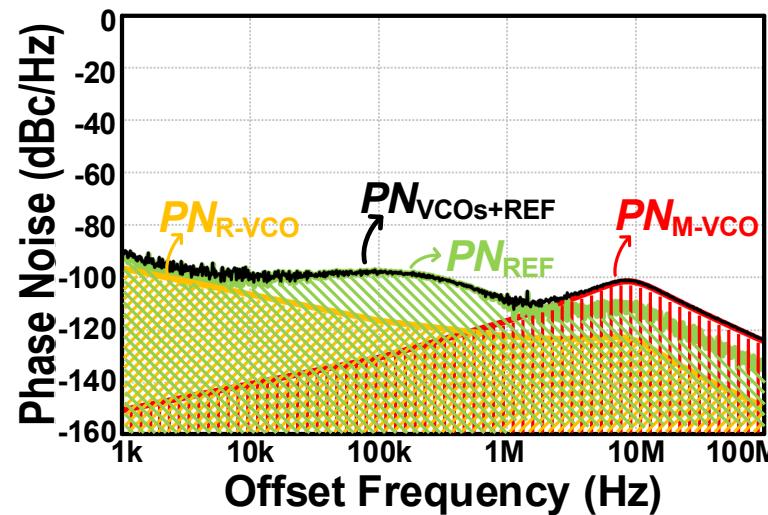
Noise Analysis of W-Band PLL ($K_{PD} = 0.05V/\text{rad}$)



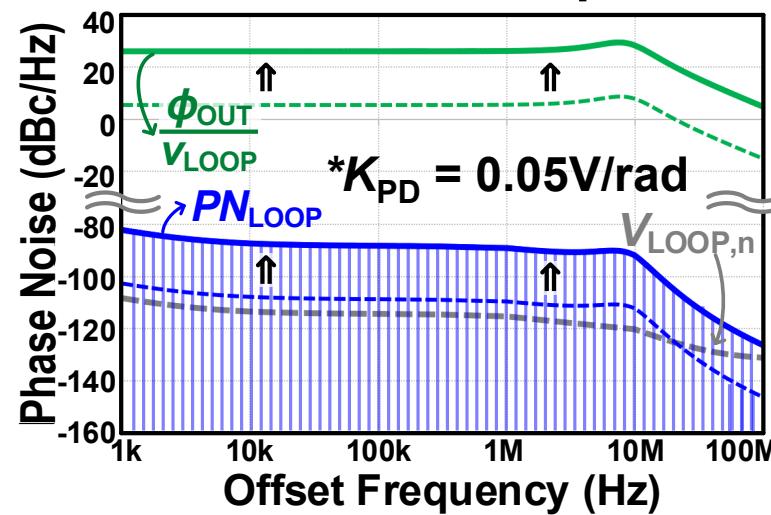
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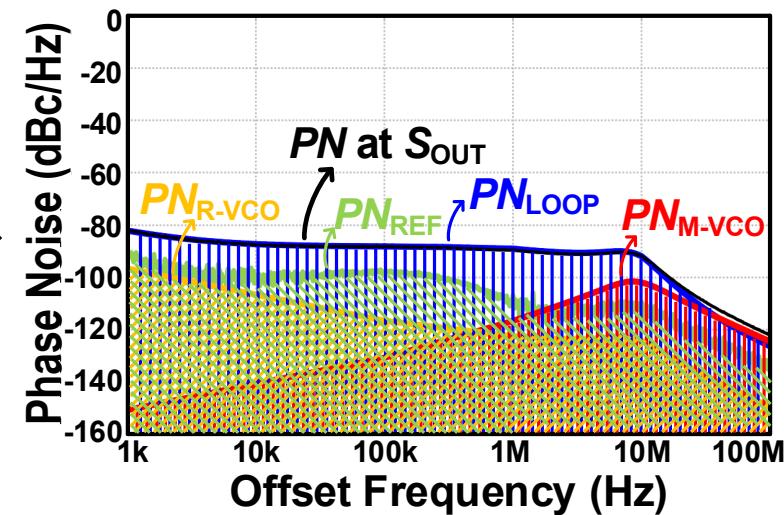
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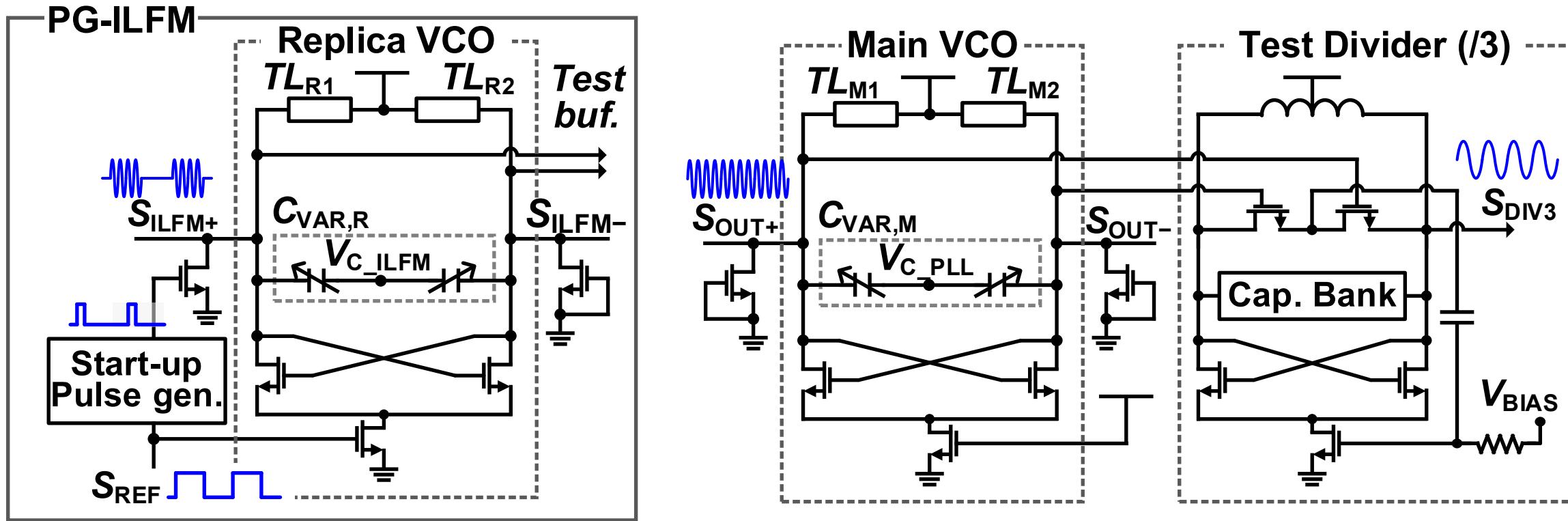


Overall PN



❖ When low gain of K_{PD} , overall PN degraded significantly due to high PN_{LOOP}

PG-ILFM, Main VCO, and Test Divider



- ❖ **Replica VCO (R-VCO) having same architecture of Main VCO (M-VCO)**
- ❖ **Start-up pulse generator used to minimize start-up time**
- ❖ **Test divider (/3) used for phase noise measurement**

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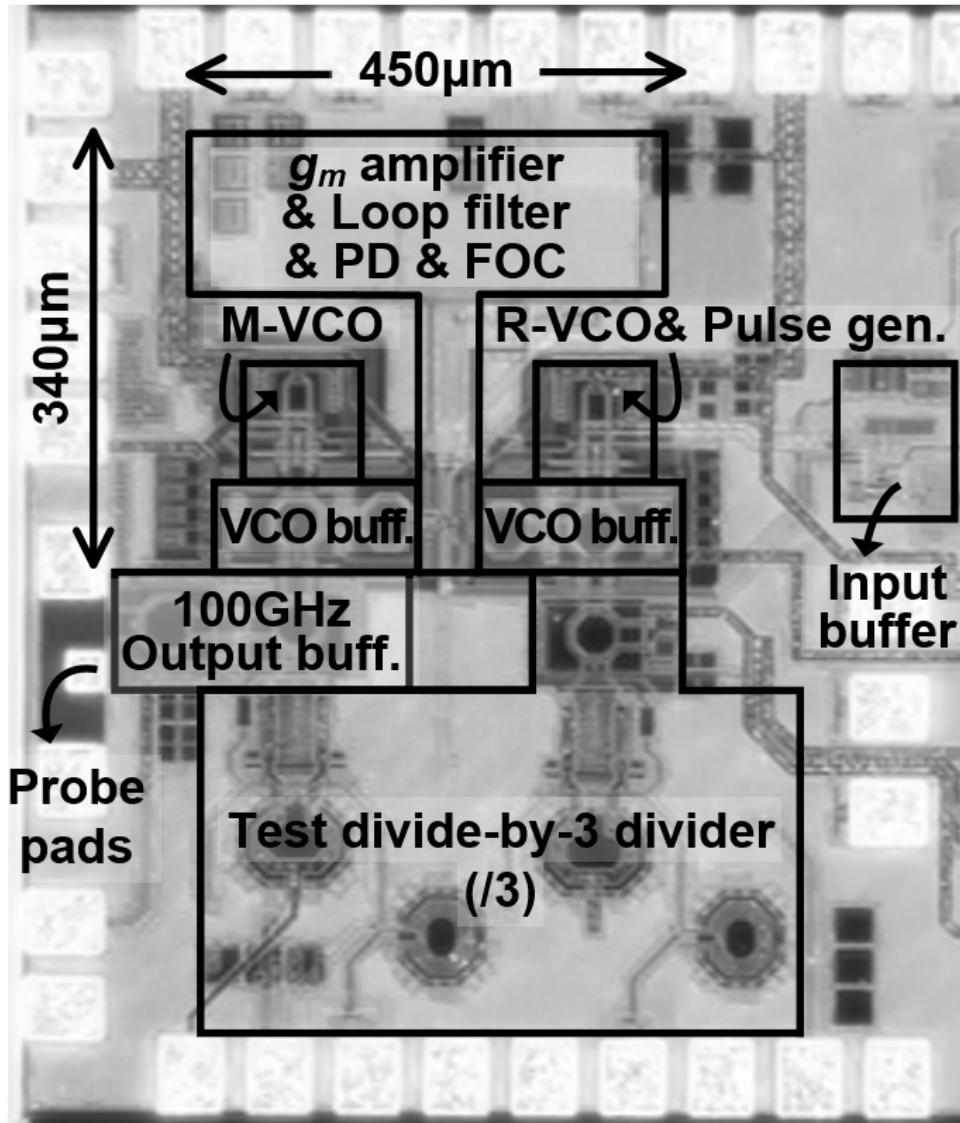
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❖ Measurements and Performance Comparison

❖ Conclusions

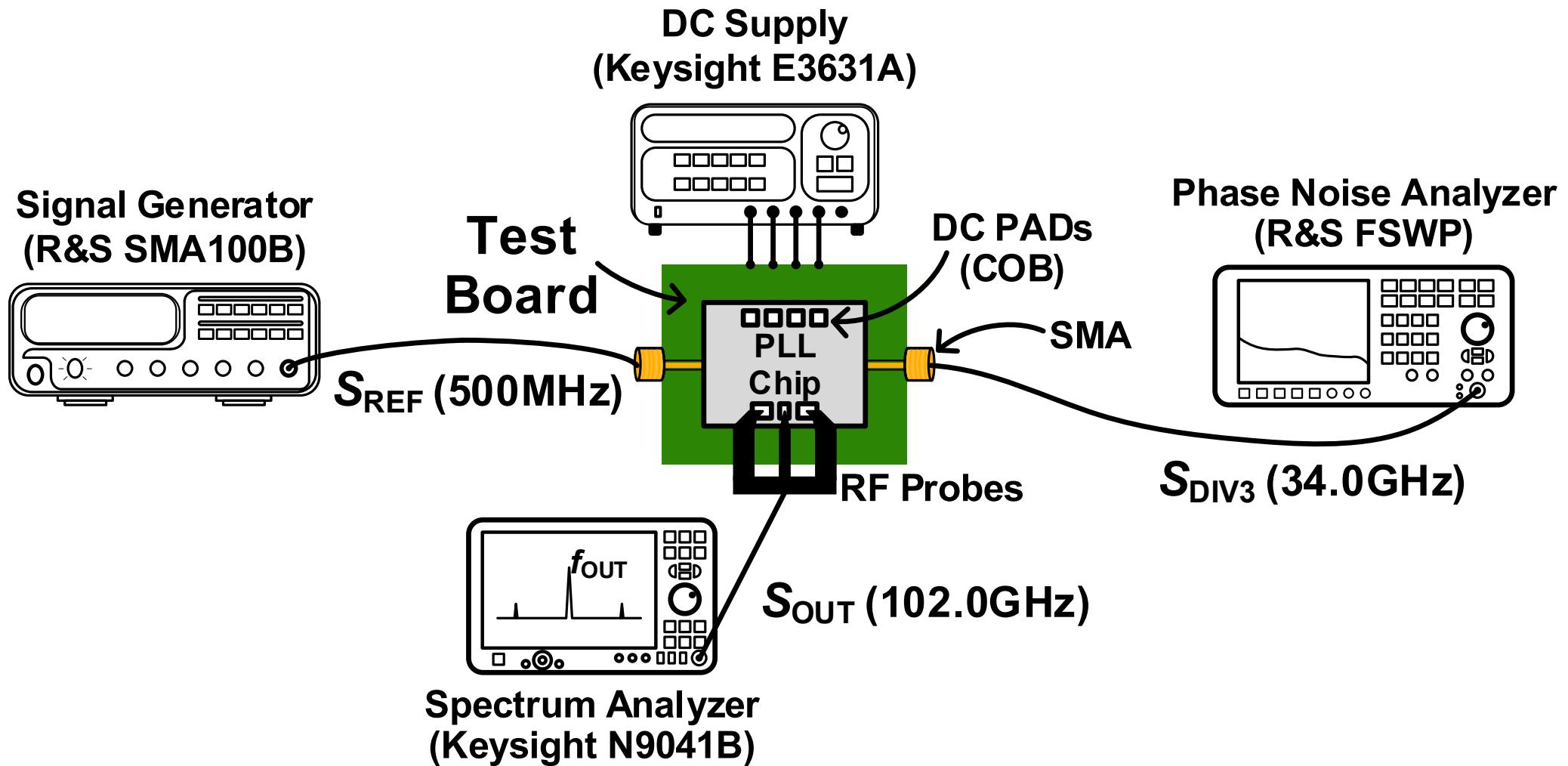
Die Photograph



- ❖ 65nm CMOS
- ❖ Active area: 0.16mm²
- ❖ Power: 22.5mW

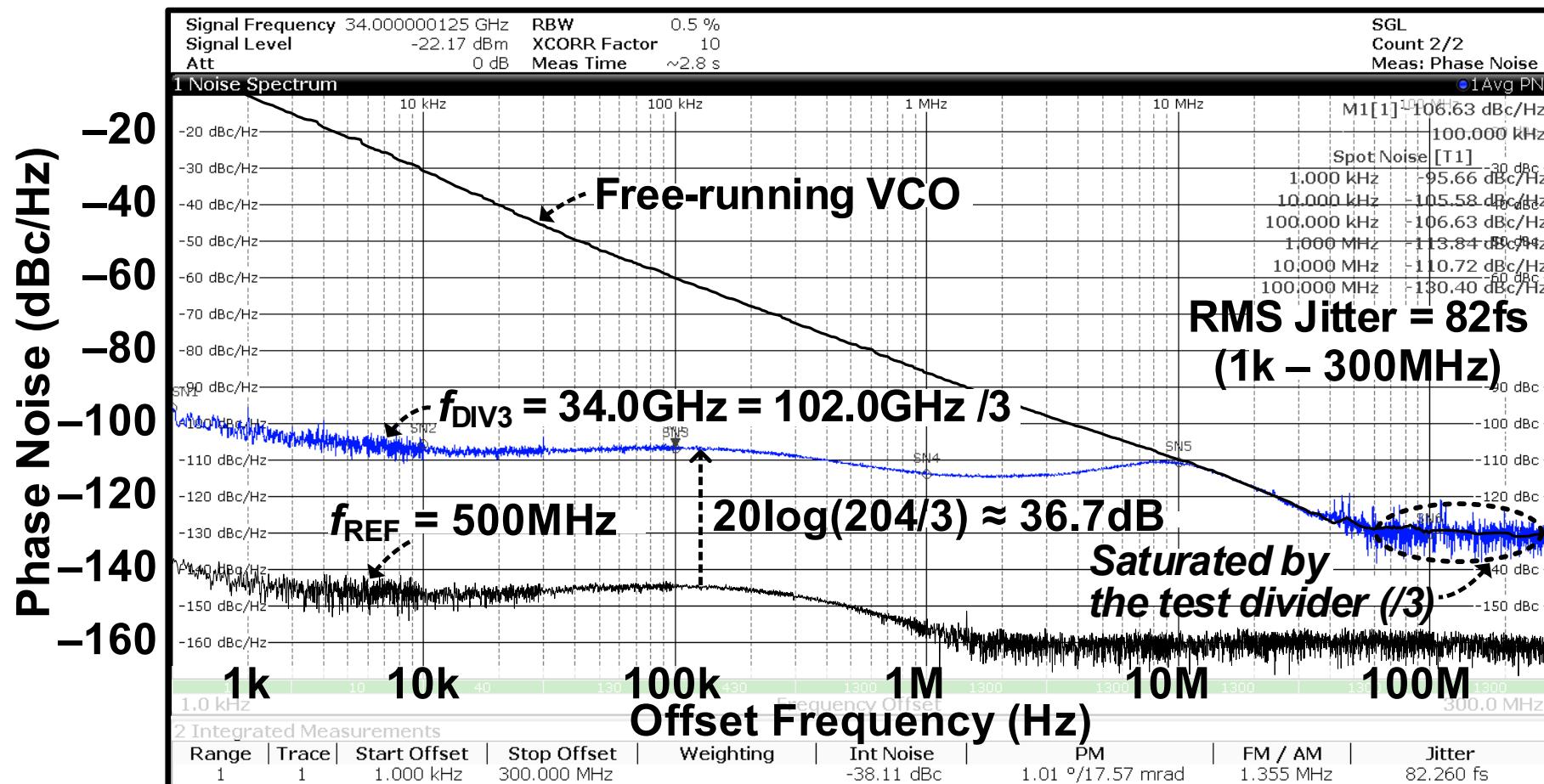
Power Consumption (mW)	
M-VCO	8.0
R-VCO	4.5
Gm amplifier & PD & FOC	2.0
VCOs' buffers	7.0
Start-up Pulse gen.	1.0
Total	22.5

Measurement Setup



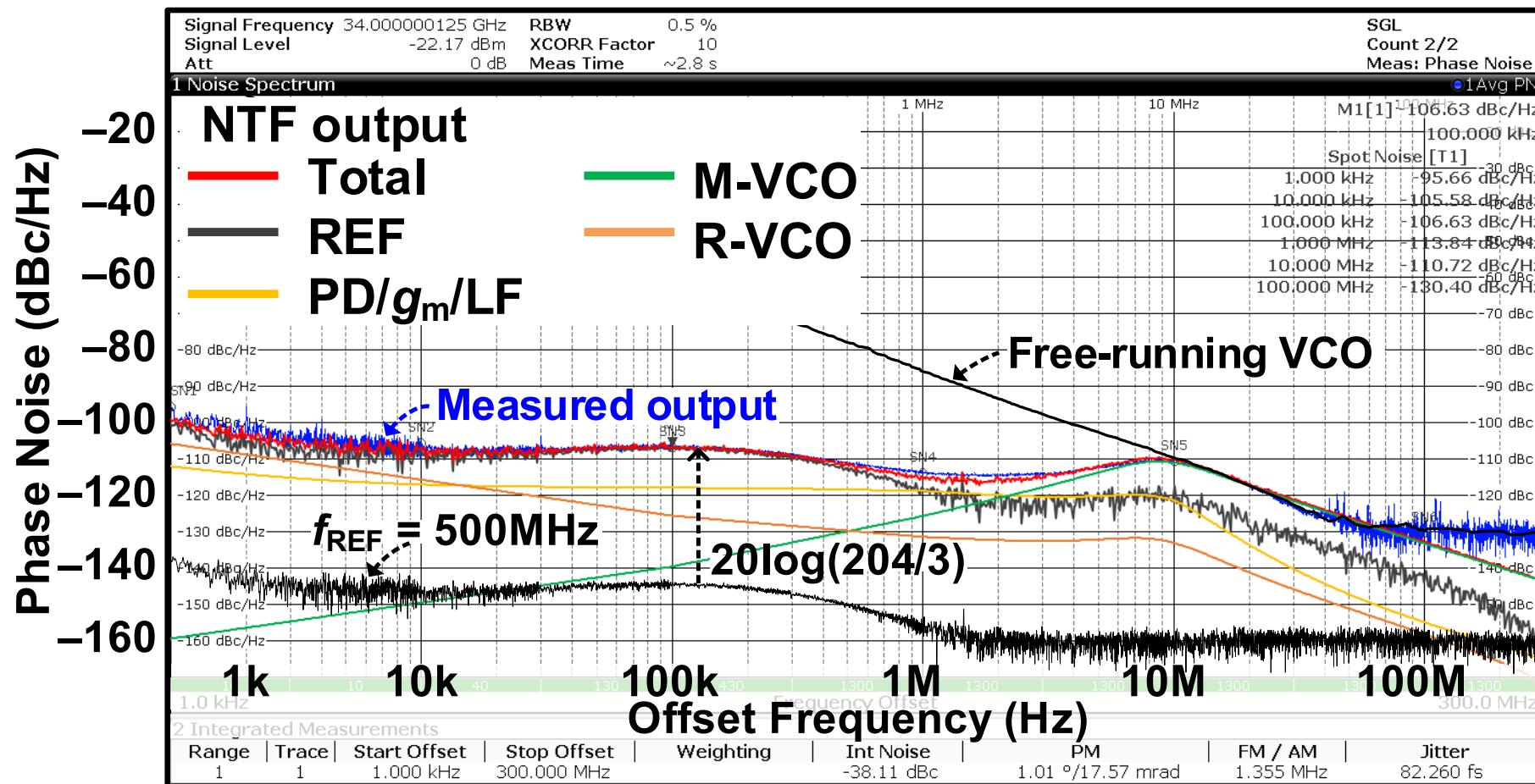
23.4: An 82fs_{RMS}-Jitter and 22.5mW-Power, 102GHz W-Band PLL Using a Power-Gating Injection-Locked Frequency Multiplier-Based Phase Detector in 65nm CMOS

Measured PN @ $f_{\text{OUT}}=102.0\text{GHz}$ ($f_{\text{DIV3}}=34.0\text{GHz}$)



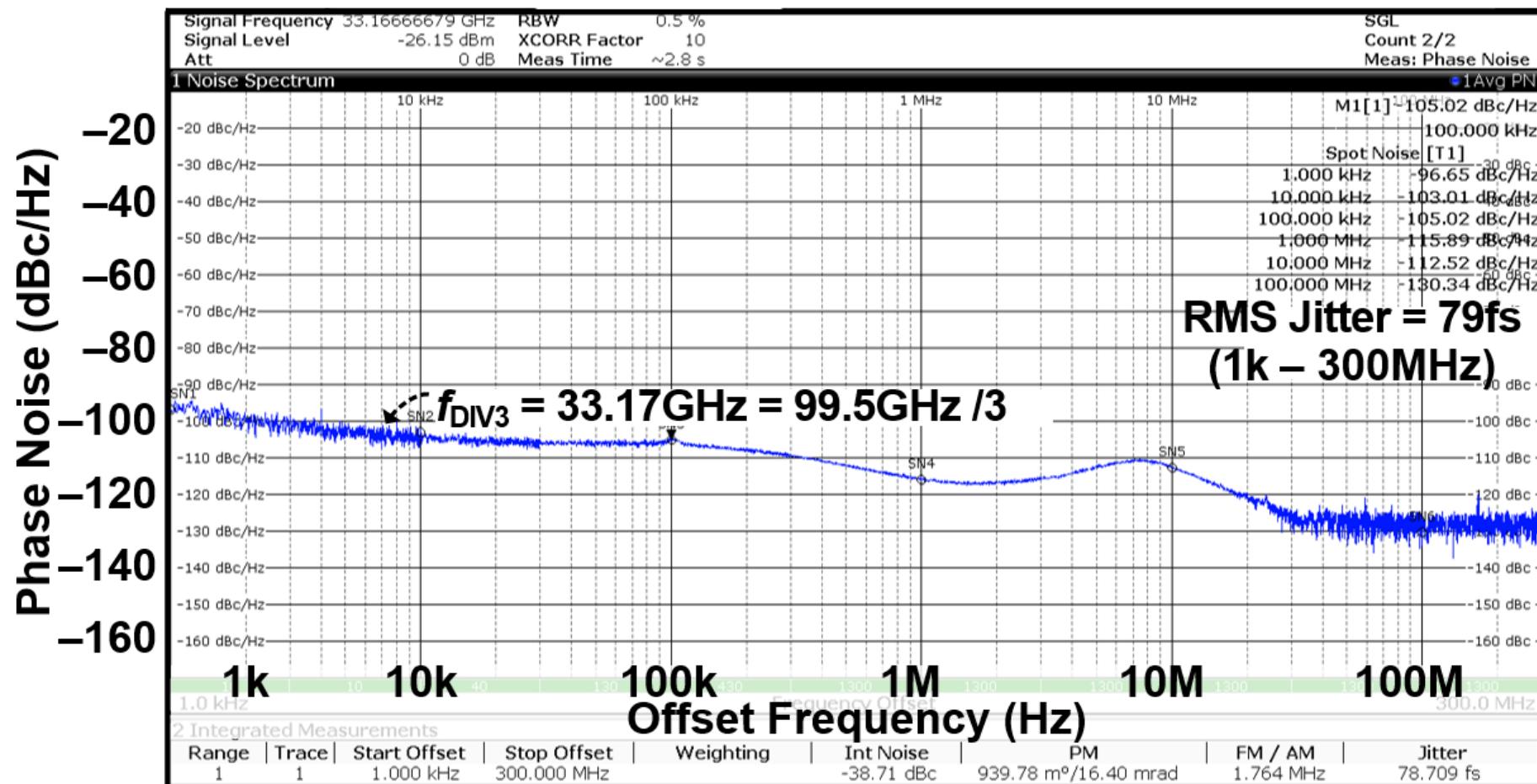
- ❖ Divide-by-3 test divider used for measurement
- ❖ 1MHz-PN: -104.3dBc/Hz @ 102.0GHz ❖ RMS jitter: 82fs

Measured PN @ $f_{\text{OUT}}=102.0\text{GHz}$ ($f_{\text{DIV3}}=34.0\text{GHz}$)



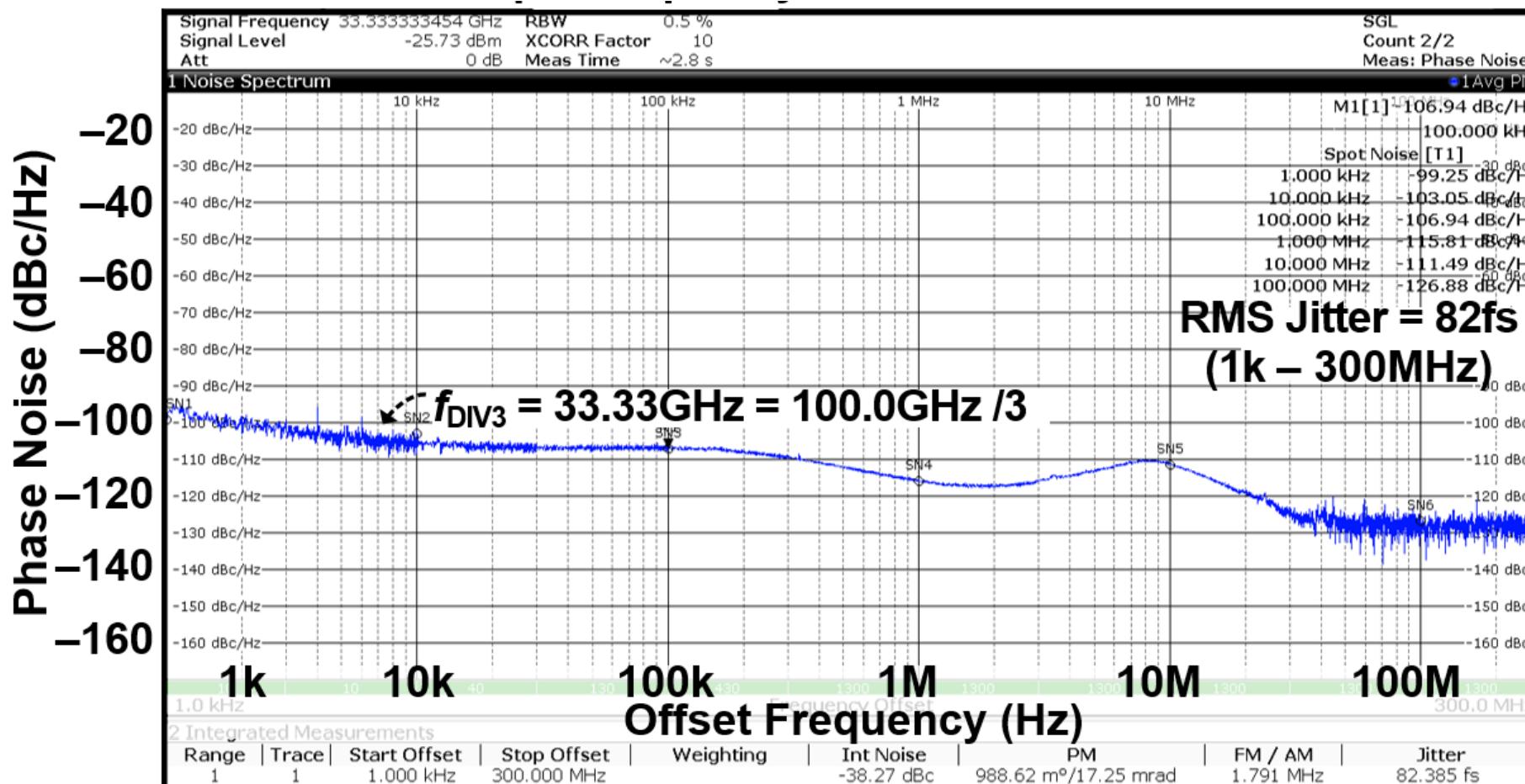
❖ Measured PN matched to expected PN according to noise model

Measured PN @ $f_{\text{OUT}}=99.5\text{GHz}$ ($f_{\text{DIV3}}=33.17\text{GHz}$)



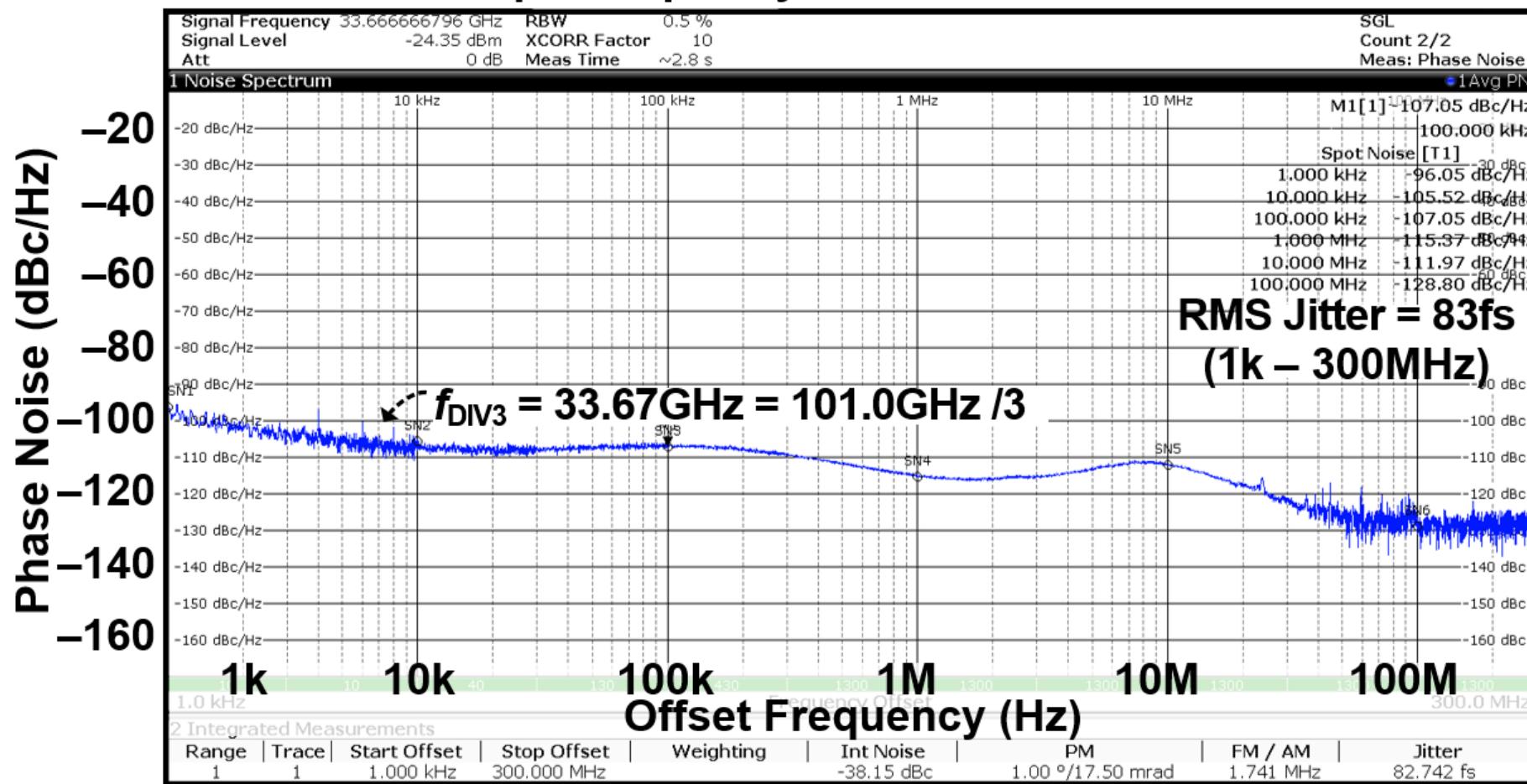
- ❖ Divide-by-3 test divider used for measurement
- ❖ 1MHz-PN: -106.3dBc/Hz @ 99.5GHz ❖ RMS jitter: 79fs

Measured PN @ $f_{\text{OUT}}=100.0\text{GHz}$ ($f_{\text{DIV3}}=33.33\text{GHz}$)



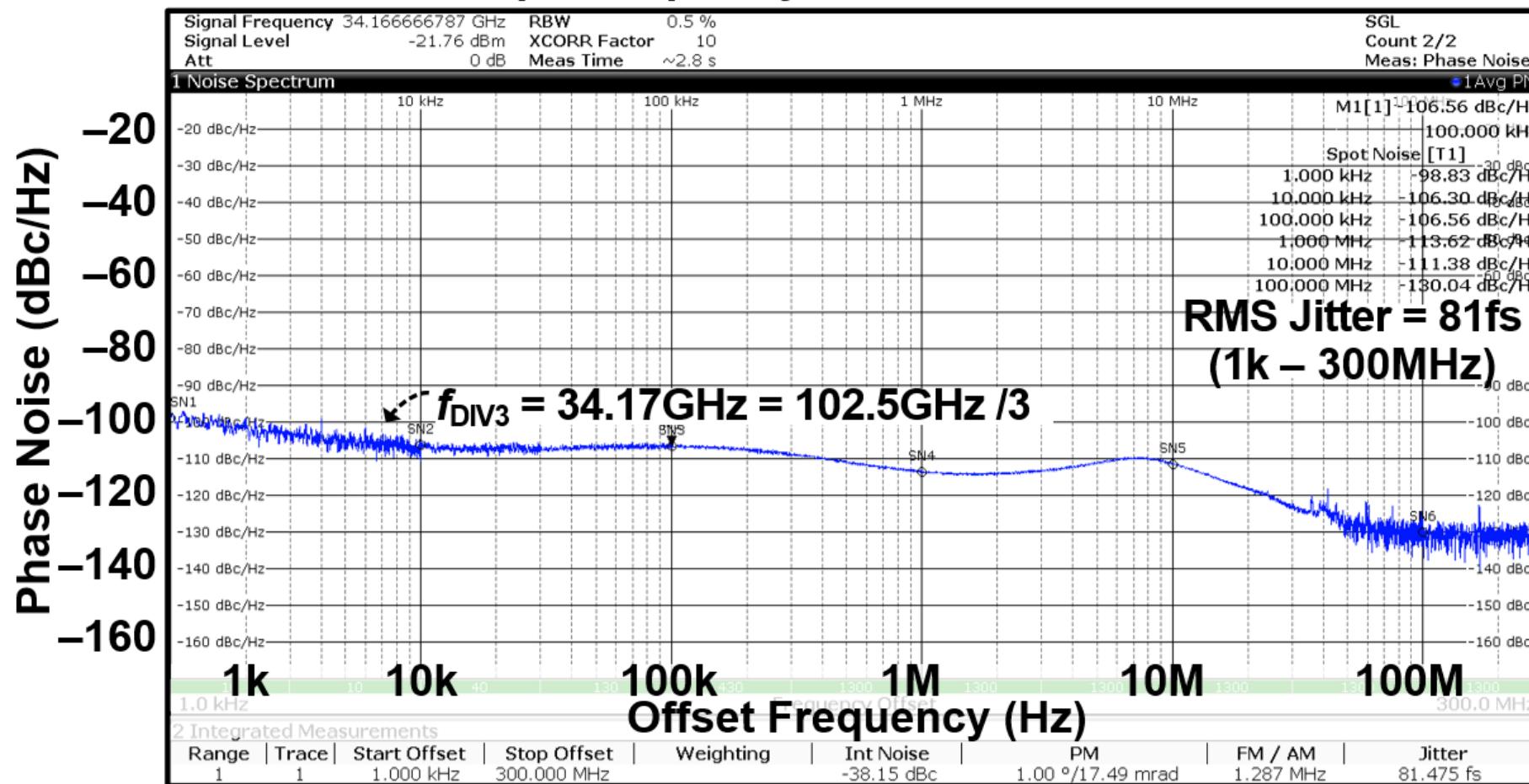
- ❖ Divide-by-3 test divider used for measurement
- ❖ 1MHz-PN: -106.3dBc/Hz @ 100.0GHz ❖ RMS jitter: 82fs

Measured PN @ $f_{\text{OUT}}=101.0\text{GHz}$ ($f_{\text{DIV3}}=33.67\text{GHz}$)



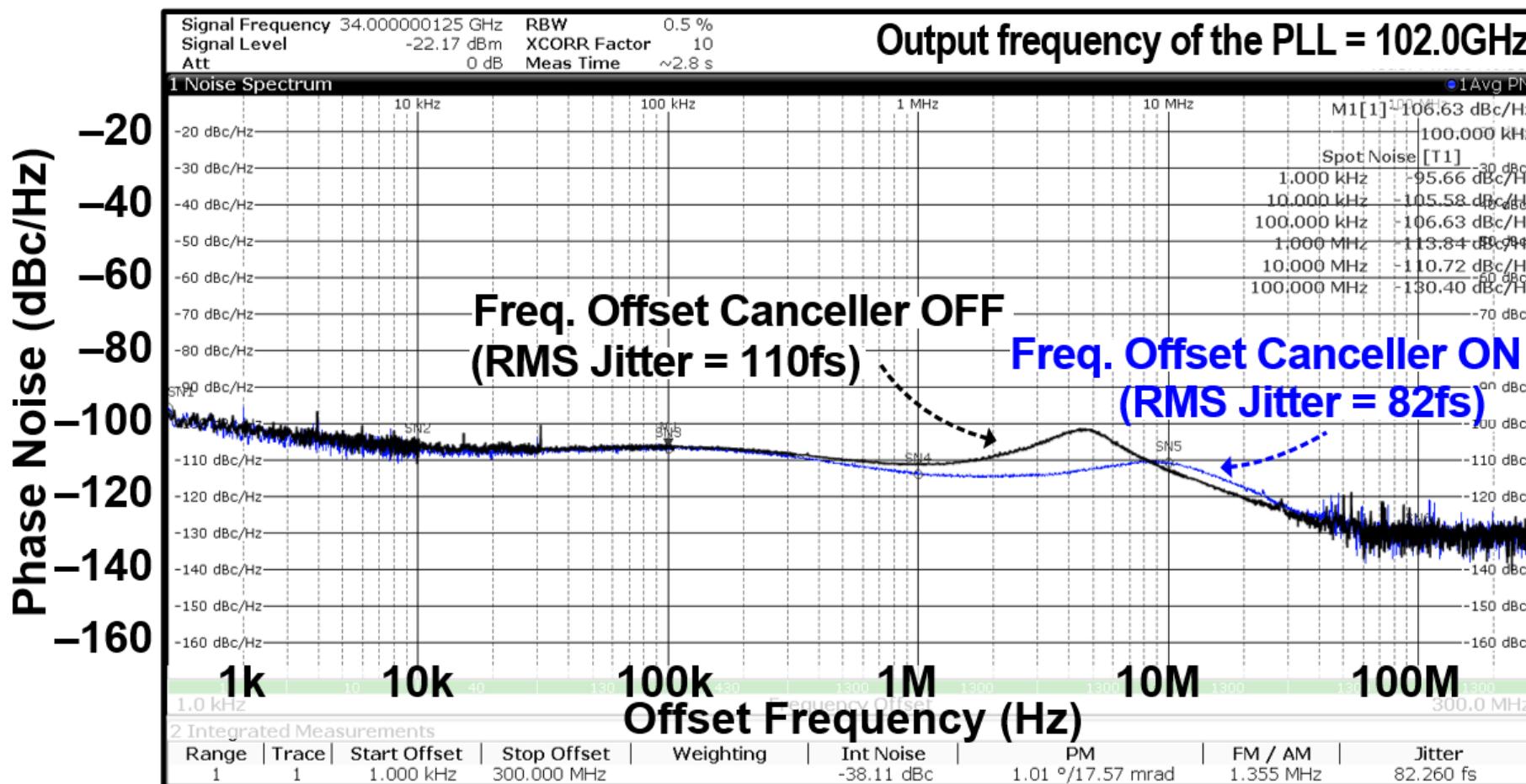
- ❖ Divide-by-3 test divider used for measurement
- ❖ 1MHz-PN: -105.8dBc/Hz @ 101.0GHz ❖ RMS jitter: 83fs

Measured PN @ $f_{\text{OUT}}=102.5\text{GHz}$ ($f_{\text{DIV3}}=34.17\text{GHz}$)



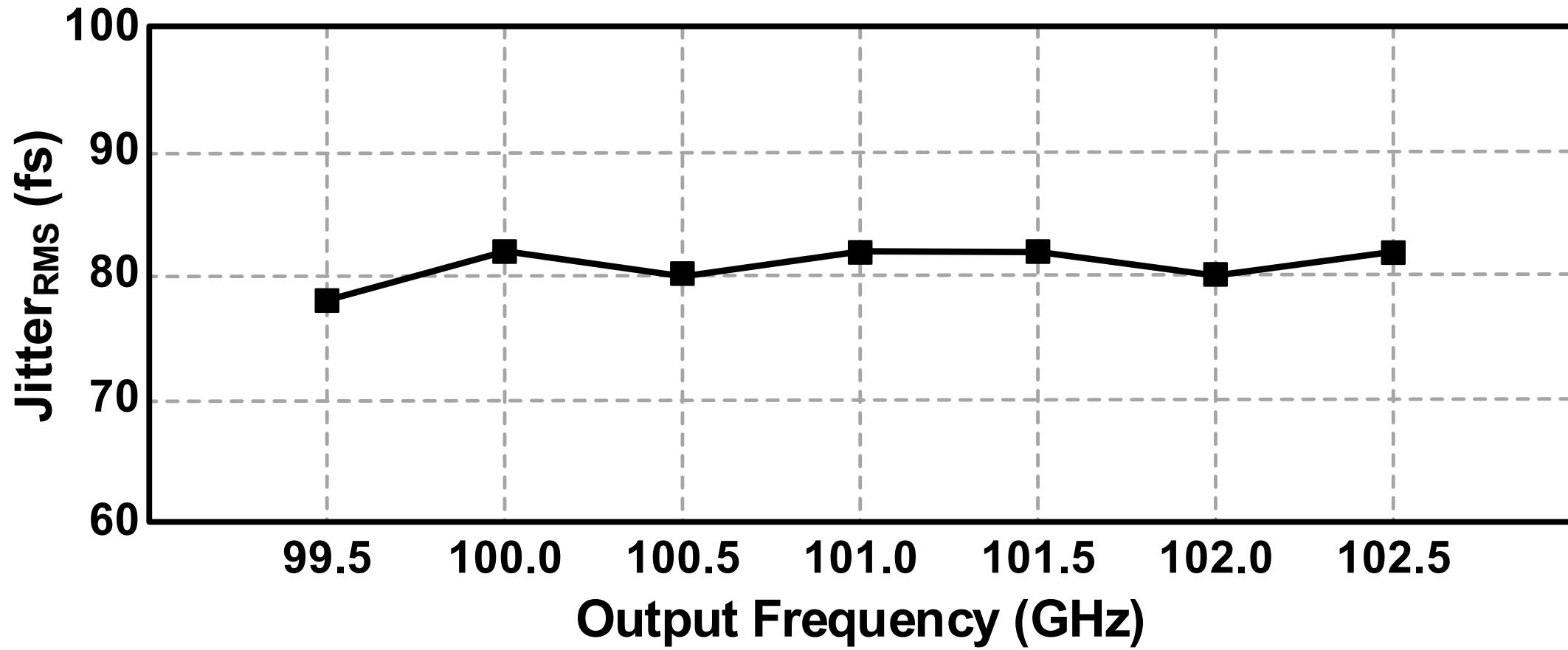
- ❖ Divide-by-3 test divider used for measurement
- ❖ 1MHz-PN: -104.1dBc/Hz @ 102.5GHz ❖ RMS jitter: 81fs

Measured PN When FOC Turned ON/OFF



- ❖ FOC canceling frequency offset between M-VCO and R-VCO
- PLL maintaining wide BW and ultra-low jitter 😊

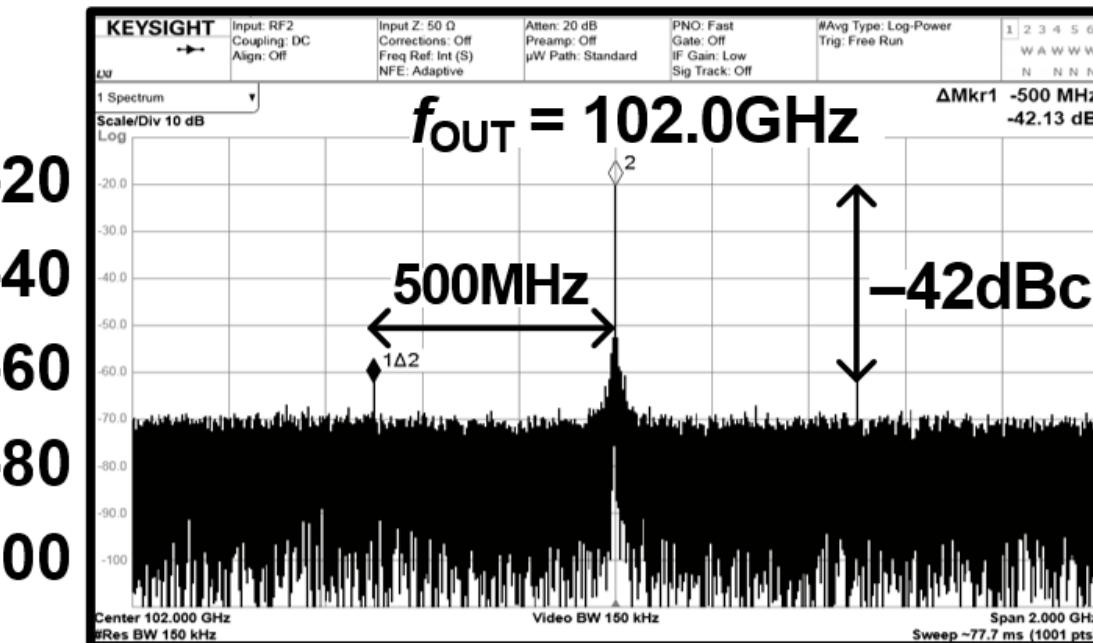
Measured Jitter_{RMS} across Output Frequencies



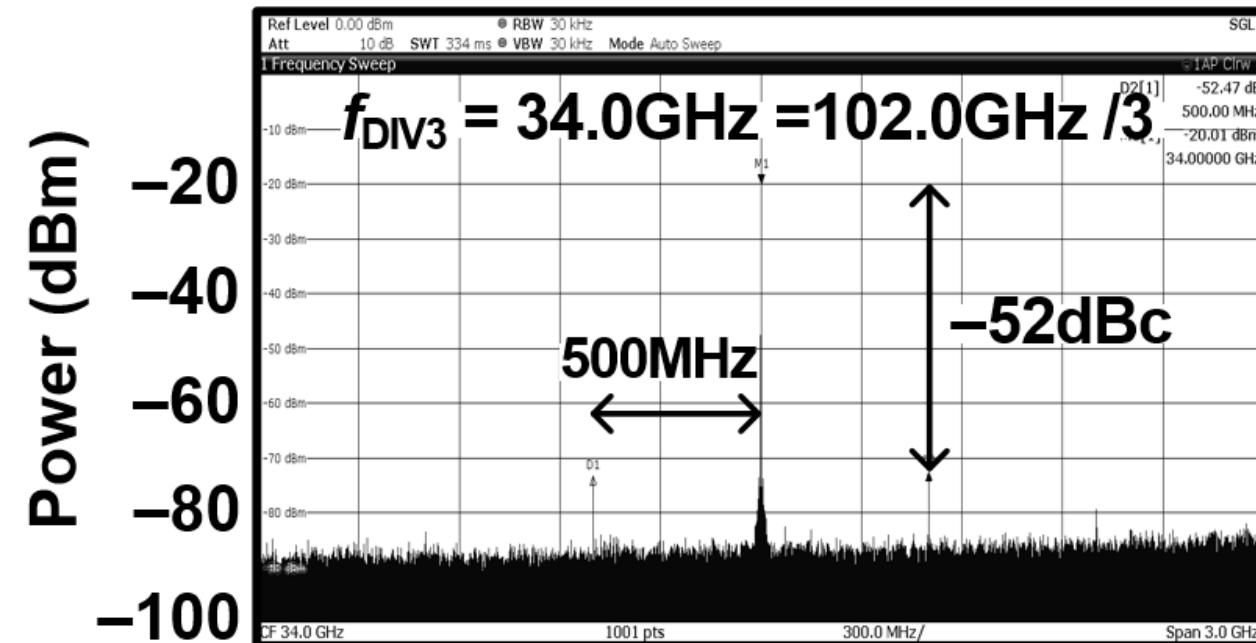
❖ Achieving ultra-low jitter consistently across output frequencies

Measured Spectrum @ $f_{\text{OUT}} = 102.0\text{GHz}$ ($f_{\text{DIV3}} = 34.0\text{GHz}$)

- $f_{\text{OUT}} = 102.0\text{GHz}$



- $f_{\text{DIV3}} = 34.0\text{GHz}$



- ❖ Reference spur @ 102.0GHz: -42dBc
- ❖ Reference spur @ 34.0GHz: -52dBc (measured using divide-by-3 test divider)

Performance Comparison

	This work	ISSCC'09 [2] K. Tsai	TMTT'14 [3] S. Kang	ISSCC'18 [4] Z. Huang	RFIC'14 Y. Chao	VLSI'19 [1] X. Liu
Process	65nm CMOS	65nm CMOS	130nm SiGe	65nm CMOS	65nm CMOS	65nm CMOS
Architecture	PG-ILFM-based PD Direct W-band PLL	Direct W-band PLL	Direct W-band PLL	Direct W-band DPLL	50GHz PLL + Push-push(x2)	23GHz PLL + ILFM (x4)
Type	Integer-N	Integer-N	Integer-N	Integer-N	Integer-N	Integer-N
Supply (V)	1.2/ 0.8	1.2	3.3/ 2.5/ 1.2	1.2/ 0.8	1.2/ 0.6	N/A
Output Freq, f_{OUT} (GHz)	99.5 – 102.5	95.1 – 96.5	92.7 – 100.2	82.0 – 107.6	96.8 – 108.5	80.0 – 104.0
Reference Freq, f_{REF} (MHz)	500	375	1500	125	195	100
Multiplication Factor (N)	199 – 205	256	64	656 – 864	512	800 – 1040
Reference Spur (dBc)	-42	-52	< -60	< -34	-40	-40
1MHz PN (dBc/Hz) @ f_{OUT} (GHz)	-104.3 @102	-75.7 @95.5	-102.0 @95.0	-79.0 @107.6	-88.0 @99.4	-93.0 @100.8
Jitter _{RMS} , σ_t (fs) (1k – 300MHz)	82 (1k – 300MHz)	2220 (1k – 10MHz)	71 (1M – 1GHz)	278 (1k – 10MHz)	170* (10k – 10MHz)	137 (10k – 10MHz)
Power, P_{DC} (mW)	22.5	43.7	469.3	35.5	14.1	23.6**
Active Area (mm ²)	0.16	0.70	0.93	0.36	0.39	0.41**
FOM _{JIT} *** (dB)	-248.2	-216.7	-236.2	-235.6	-243.8	-243.5

*Calculated from the PN graph in Fig. 8 of [RFIC'14, Y. Chao] **Power and area only for the W-band ***FOM_{JIT} = 10log($\sigma_t^2 \cdot P_{\text{DC}}$)

Outline

❖ Introduction

- Demands of Low-Jitter W-Band PLL
- Problems of conventional W-Band PLLs

❖ Proposed W-Band PLL with PG-ILFM-based PD

- Concept of Proposed PG-ILFM-based PD
- Operation of PLL & Frequency Offset Canceller (FOC)
- Noise Analysis

❖ Measurements and Performance Comparison

❖ Conclusions

Conclusions

- ❖ **Proposed W-band PLL using PG-ILFM-based PD can**
 - Suppress in-band PN with the high Φ_{ERR} -detection gain and, thus,
 - Extend the PLL BW to suppress the poor PN of W-band VCO
- ❖ **Proposed FOC can keep PLL BW wide by canceling frequency mismatch between main VCO and replica VCO**
- ❖ **Proposed W-band PLL using PG-ILFM-based PD achieves excellent jitter performance of 82fs RMS jitter at 102GHz output with low power of 22.5mW, and small area of 0.16mm²**