ISSCC 2020

SESSION 29

Emerging RF & THz Techniques

A 0.42THz 9.2dBm 64-Pixel Source-Array SoC with Spatial Modulation Diversity for Computational Terahertz Imaging

Ritesh Jain, Philipp Hillger, Janusz Grzyb, and Ullrich R. Pfeiffer

IHCT, University of Wuppertal, Germany

Outline

- Motivation
- Reciprocal & Computational THz imaging
- THz source array SoC
  - Architecture
  - Circuit design and simulations
  - Measurement results
  - Imaging results
- Summary and outlook

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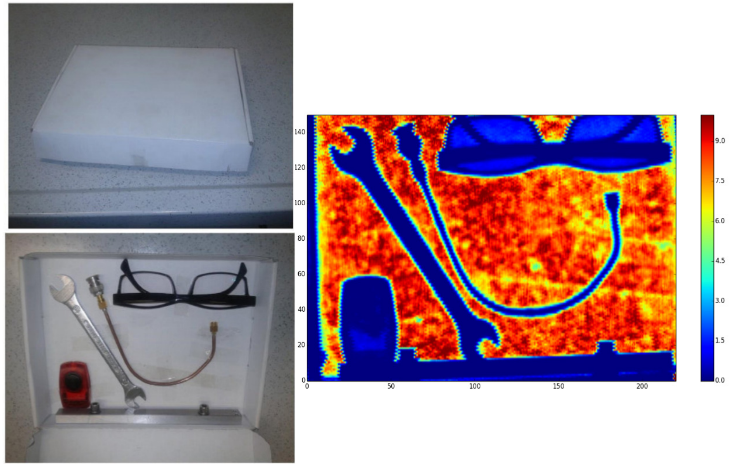
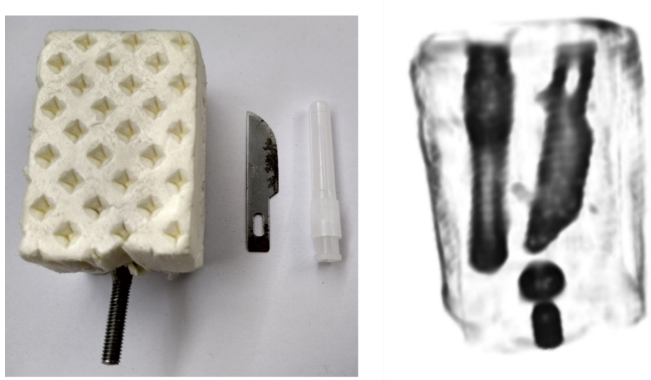
Motivation

Imaging with terahertz (THz) radiation



0.65THz transmission images
F. Landskron, B.Sc. Thesis, Uni. Wuppertal, 2014

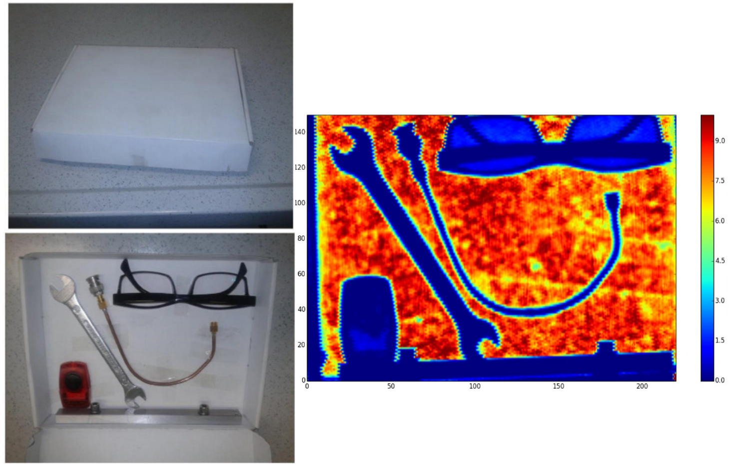


0.43THz CT image, P. Hillger et al., IEEE TTST 2019

- Penetrates dielectrics
- Strong reflection from metals
- Strong absorption by water
- Better resolution than mmWave
- Better material contrast than X-rays
- Biologically safe

Motivation

Imaging with terahertz (THz) radiation



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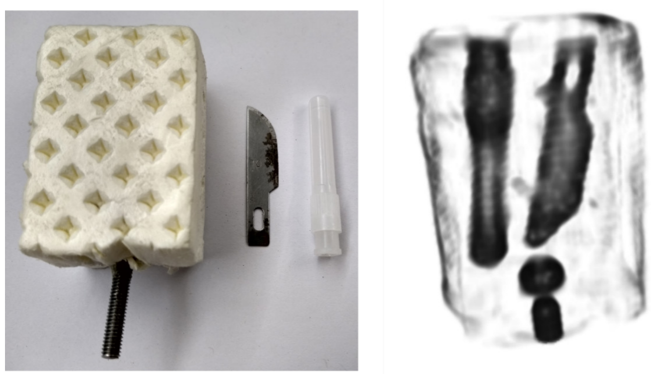

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Silicon integrated THz components

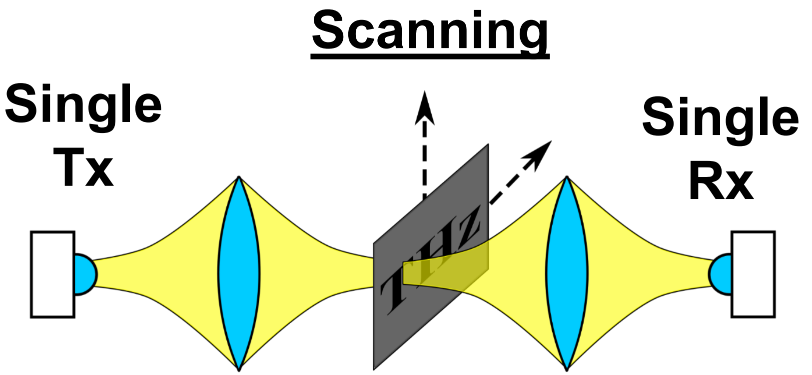
Low cost
Simple
Power efficient
Reliable / Mature Tech.

Innovations?

Industrial THz imaging systems

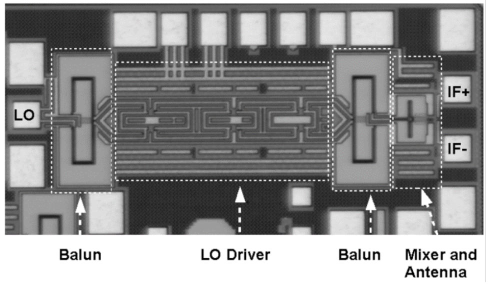
High speed
High DR
High sensitivity
High resolution
Large aperture/ Field-of-view (FoV)

THz imaging over the years



- ✓ Excellent SNR
- ✗ Slow scanning (< 0.01 fps)

P_{DC} = 0.43mW
Sensitivity ~ 0.1fW
Area ~ 0.72mm^2



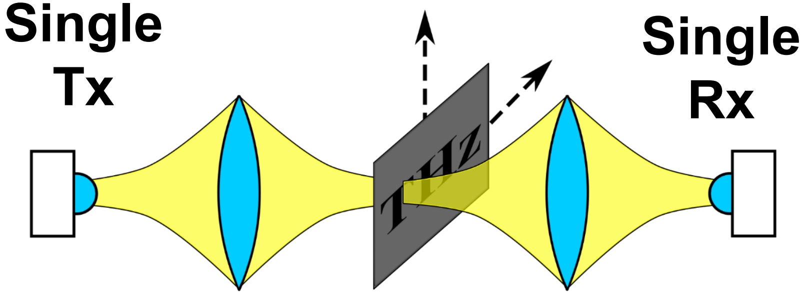
0.65THz SiGe receiver
(E. Öjefors, U. Pfeiffer, ***ISSCC 2010)***

THz imaging over the years

Scanning

Single Tx

Single Rx



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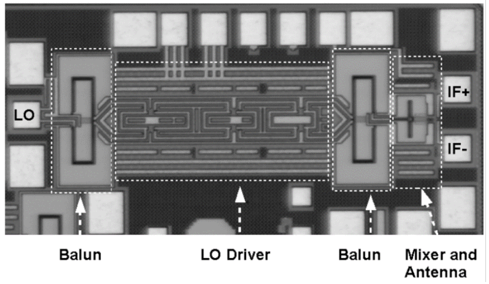

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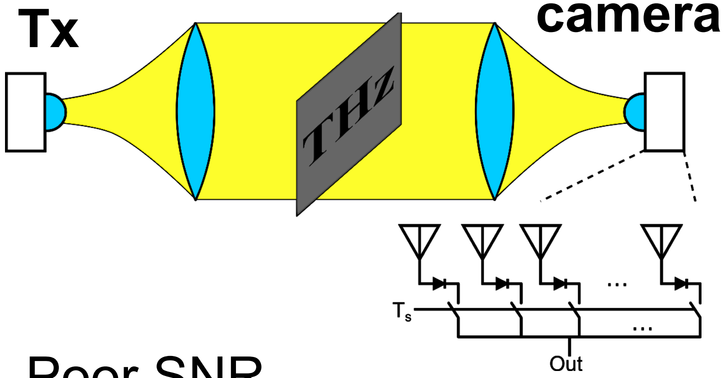
Single-shot, sensor array

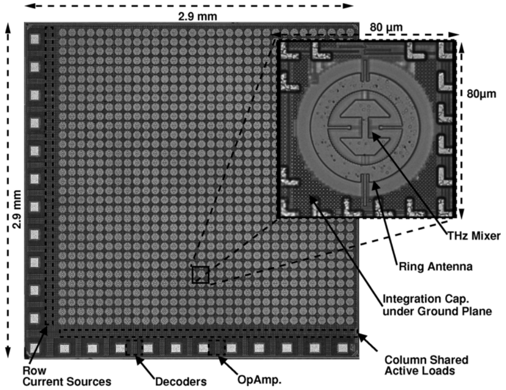
Single Tx

THz camera



- × Poor SNR
- ✓ Video imaging (~ 25 fps)

P_{DC} = 2.56mW
Sensitivity ~ 12nW
Area ~ 8.5mm^2



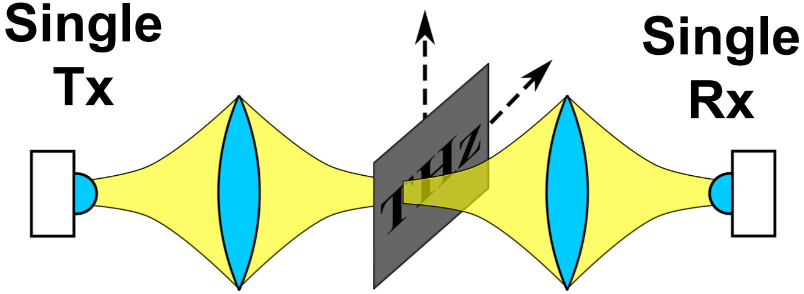
1k-pixel THz camera in 65nm CMOS
(H. Sherry et al., ***ISSCC* 2012**)

THz imaging over the years

Scanning

Single Tx

Single Rx



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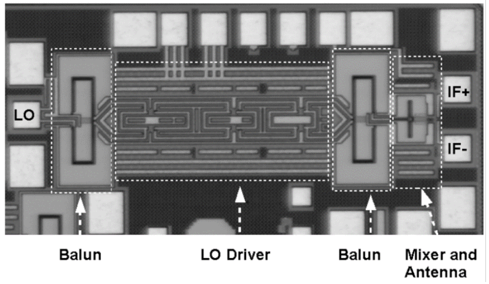

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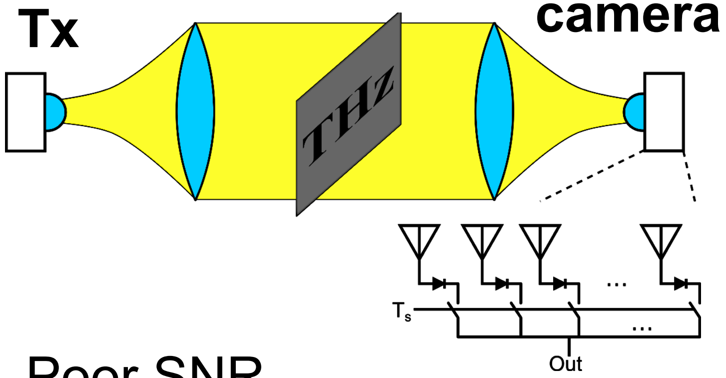

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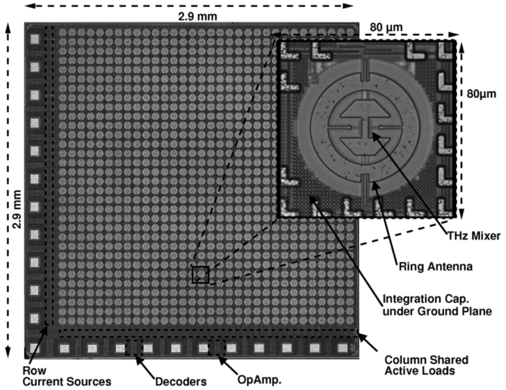
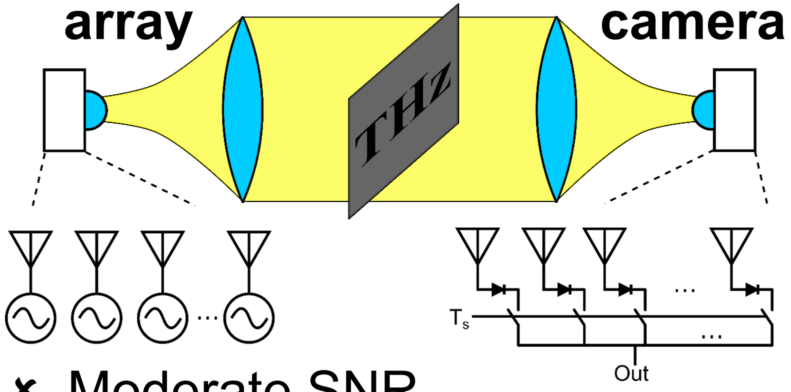


1k-pixel THz camera in 65nm CMOS
(H. Sherry et al., ***ISSCC* 2012**)

Single-shot, all silicon

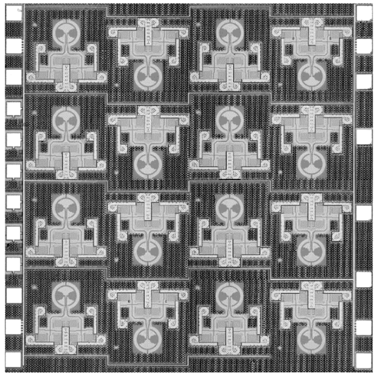
THz source array

THz camera



✗ Moderate SNR

✓ Video imaging (~ 25 fps)



P_{DC} = 2.5W
Pout ~ 1mW
Area ~ 4.2mm^2
4x4 unlocked pixels
(TPO)

0.53THz source array
(U. Pfeiffer et al., ***ISSCC* 2014**)

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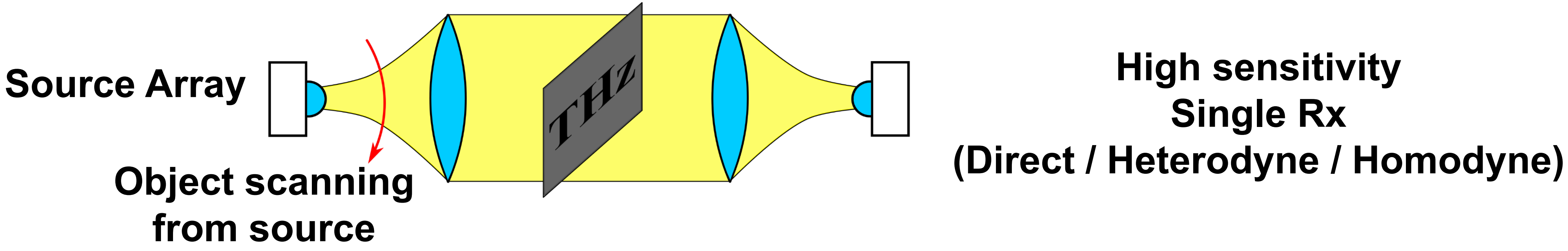
Reciprocal THz imaging (single pixel camera)

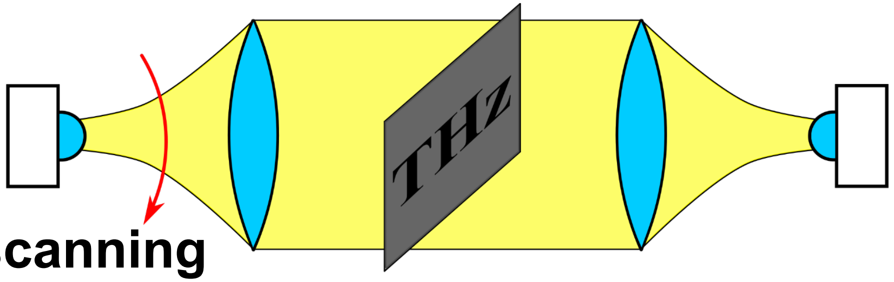
Leveraging source arrays for further SNR improvement



Reciprocal THz imaging (single pixel camera)

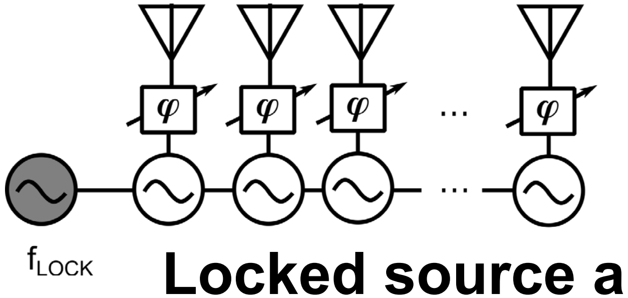
Leveraging source arrays for further SNR improvement

Source Array



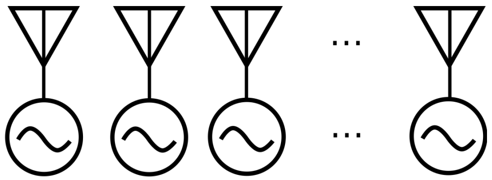
Object scanning from source

High sensitivity
Single Rx
(Direct / Heterodyne / Homodyne)



Locked source array

- ✓ Beam-steering systems
- ✓ Phase information
- ✓ Power combining
- ✗ Complex (costly)
- ✗ Limited scalability



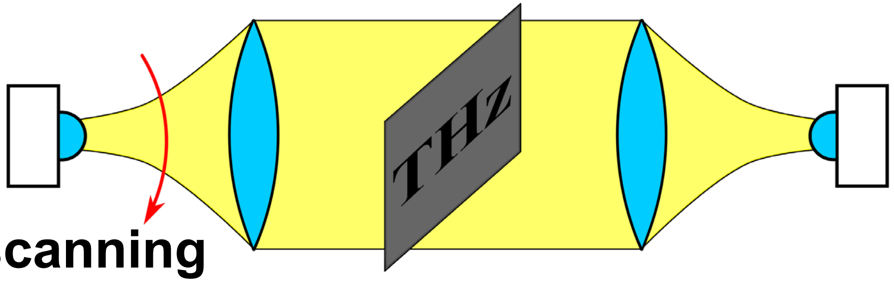
Unlocked source array

- ✓ Electronic switching
- ✓ Diffused illumination
- ✓ Infinitely scalable to 1000s pixels (ex. Thermal bottleneck)
- ✗ No coherent power combining

Reciprocal THz imaging (single pixel camera)

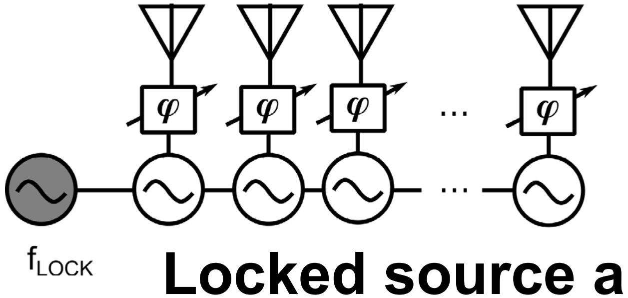
Leveraging source arrays for further SNR improvement

Source Array



Object scanning from source

High sensitivity Single Rx (Direct / Heterodyne / Homodyne)



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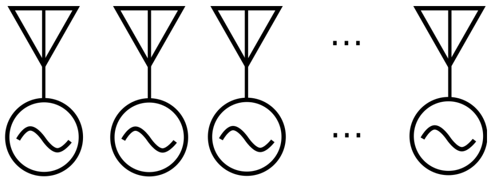

Unlocked source array
- ✓ Electronic switching
- ✓ Diffused illumination
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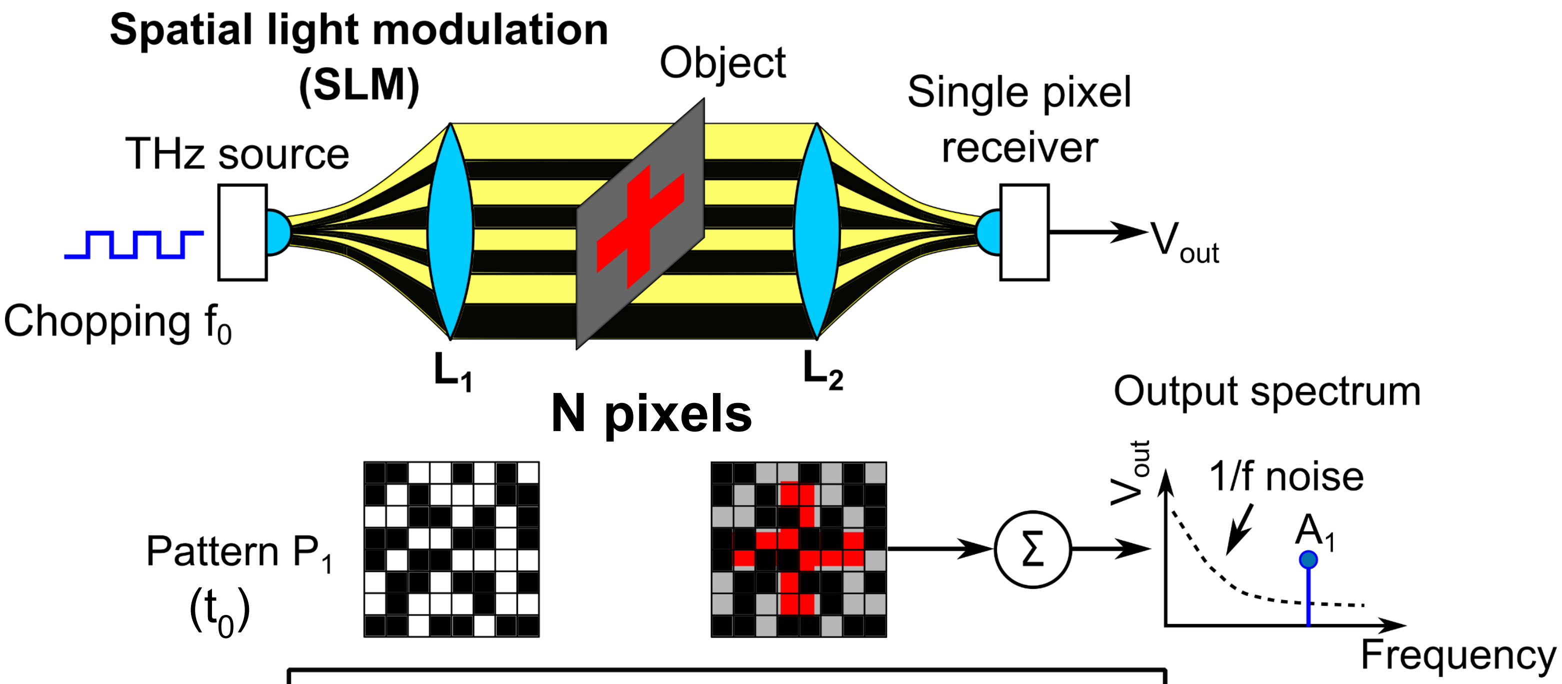
- × No coherent power combining

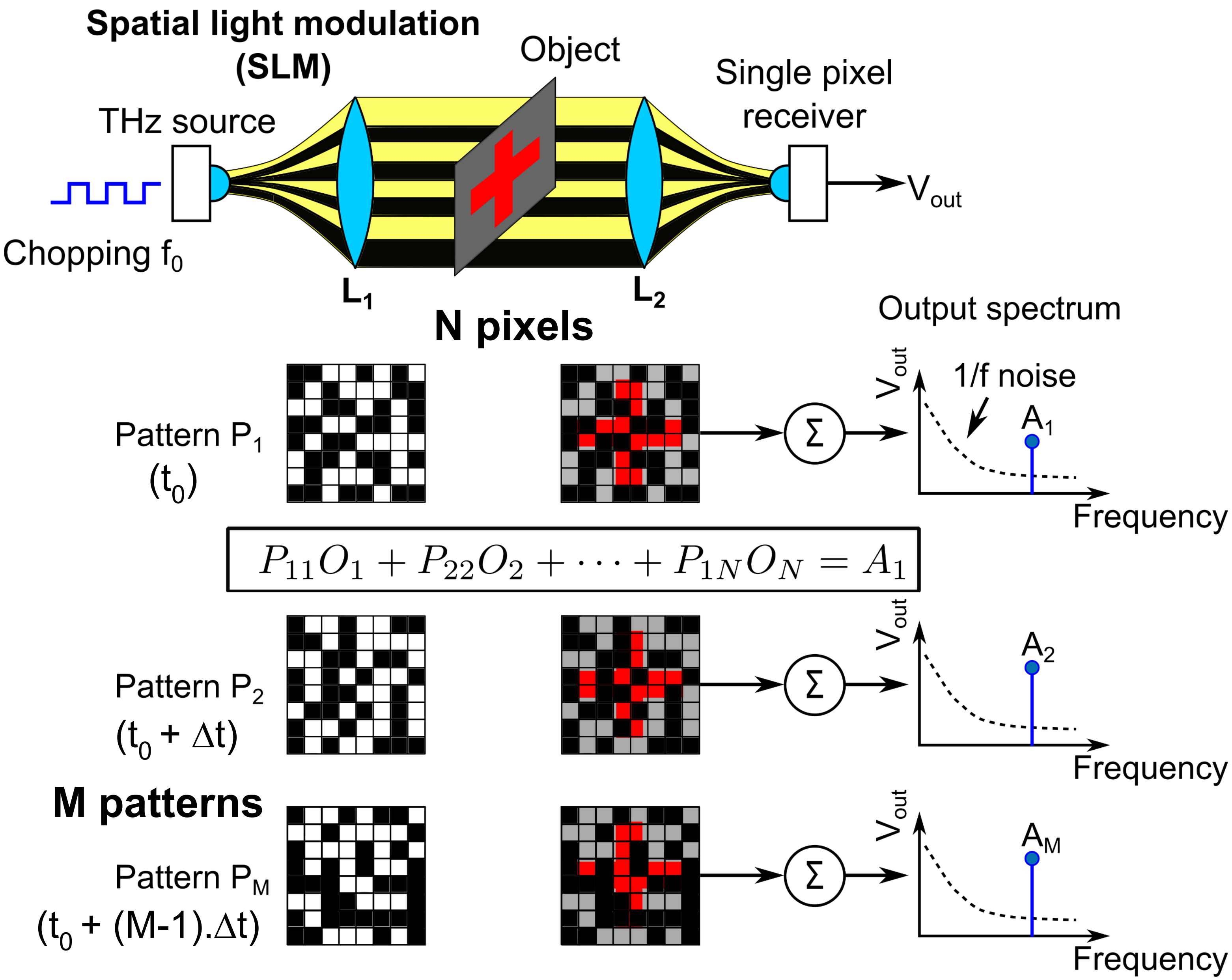
Smart source array ?
- Reconfigurable
- Scalable (multi-chip)
- Fast imaging
- High SNR and DR
- Low complexity
- Computational imaging

Computational THz imaging



$$P_{11}O_1 + P_{22}O_2 + \cdots + P_{1N}O_N = A_1$$

Computational THz imaging



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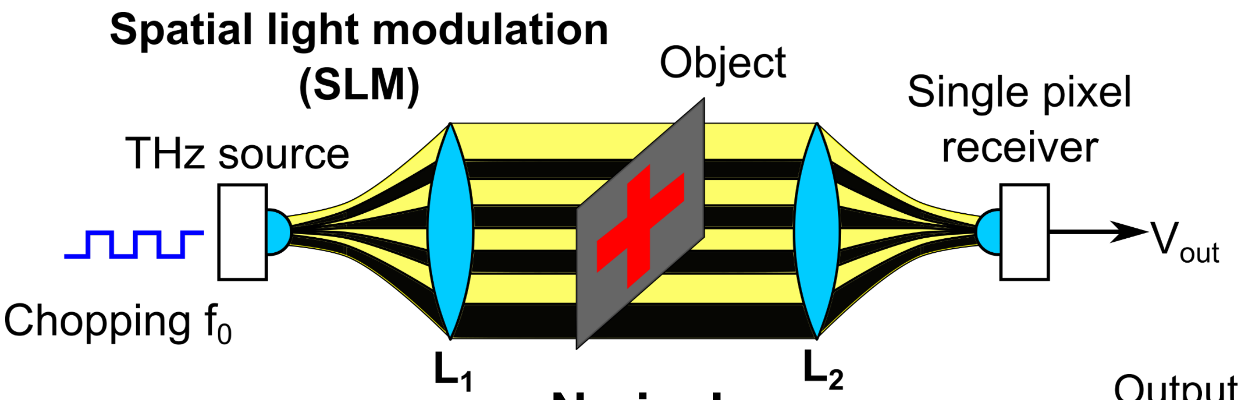
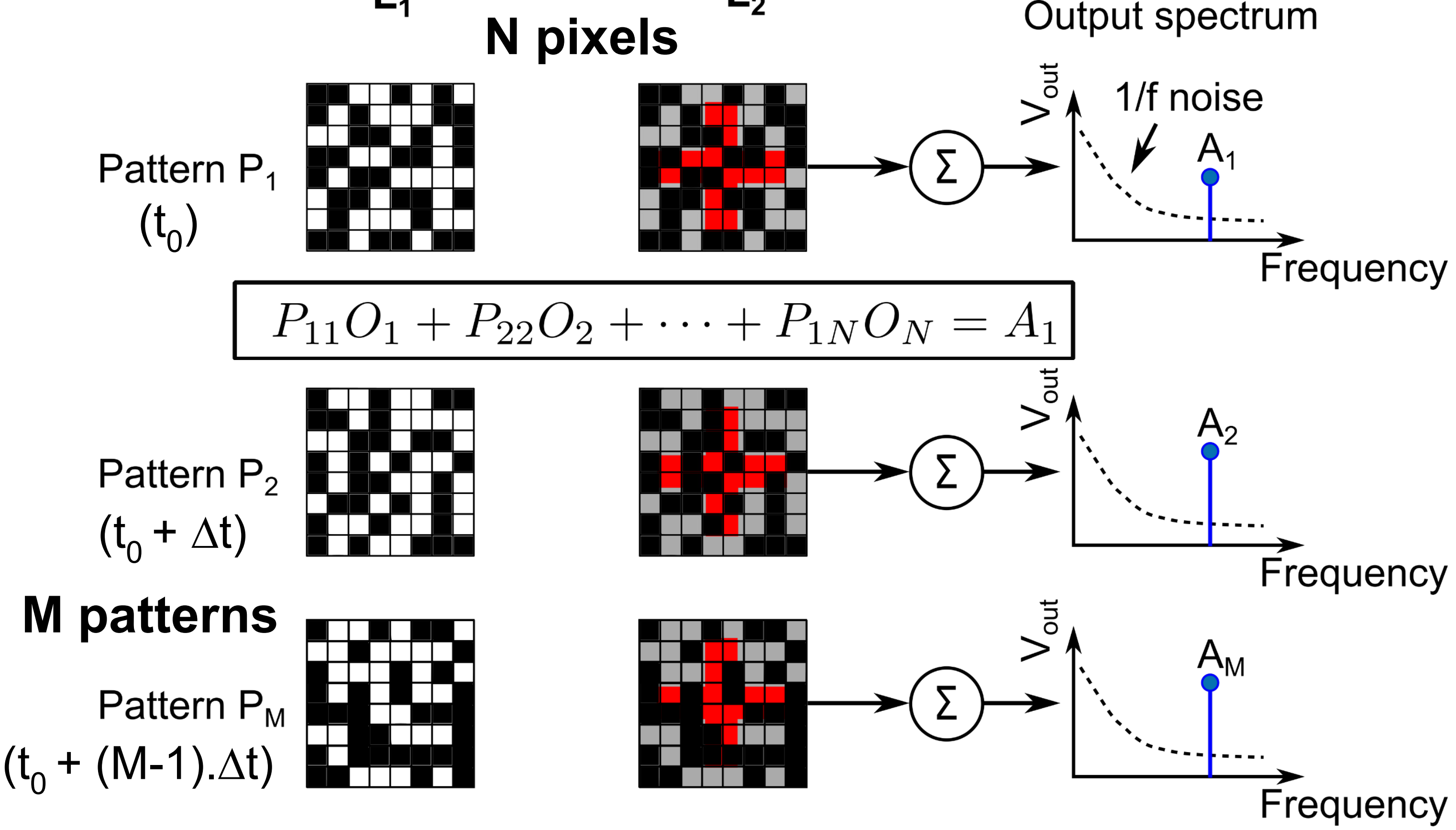




$$\boxed{P_{11}O_1 + P_{22}O_2 + \cdots + P_{1N}O_N = A_1}$$

$$\underbrace{\begin{bmatrix} P_{11} & P_{12} & \cdots & P_{1N} \\ P_{12} & P_{22} & \cdots & P_{2N} \\ \vdots & & & \\ P_{M1} & P_{M2} & \cdots & P_{MN} \end{bmatrix}}_{\substack{\boldsymbol{\Phi} \\ \text{Pattern matrix}}} \cdot \underbrace{\begin{bmatrix} O_1 \\ O_2 \\ \vdots \\ \vdots \\ O_N \end{bmatrix}}_{\substack{\mathbf{X} \\ \text{Object vector}}} = \underbrace{\begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ A_M \end{bmatrix}}_{\substack{\mathbf{Y} \\ \text{Measurement vector}}}$$

Φ.X = Y	(Measurement)
Y = Φ^{-1}.X	(Reconstruction)

M = N = rank(**P**) [Deterministic]

⟹ **Unique solution**

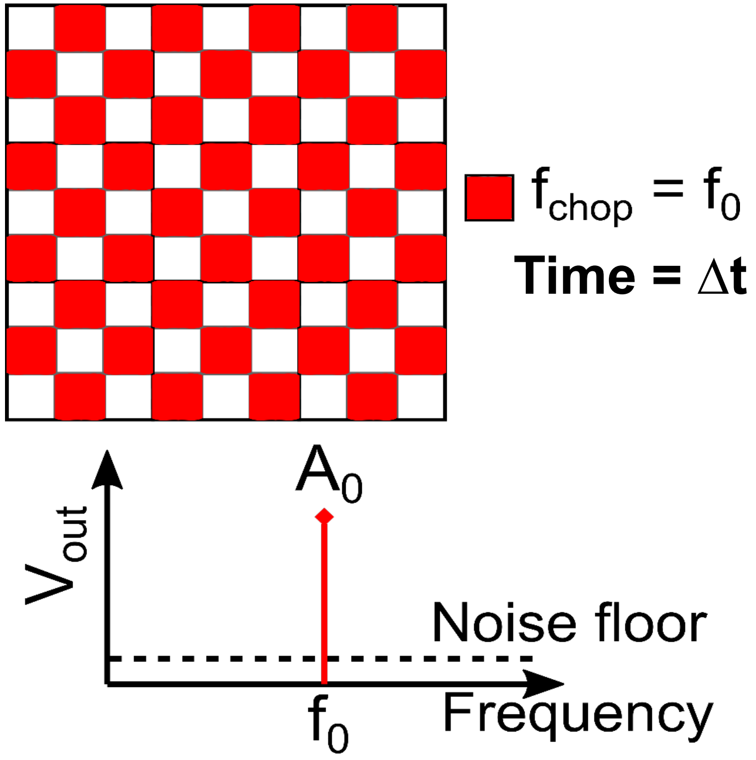
M < N [Under-determined]

⟹ **Compressive sensing**

⟹ **Pattern recognition**

Computational THz imaging (contd.)

Single chopping frequency

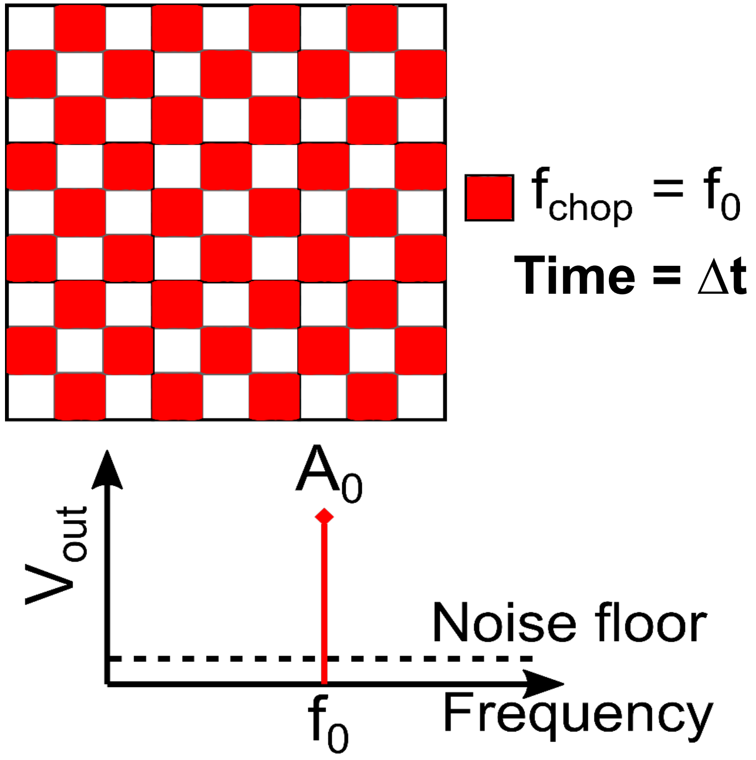


More on pixels ⟹ Higher SNR

Sequential patterns ⟹ Slower

Computational THz imaging (contd.)

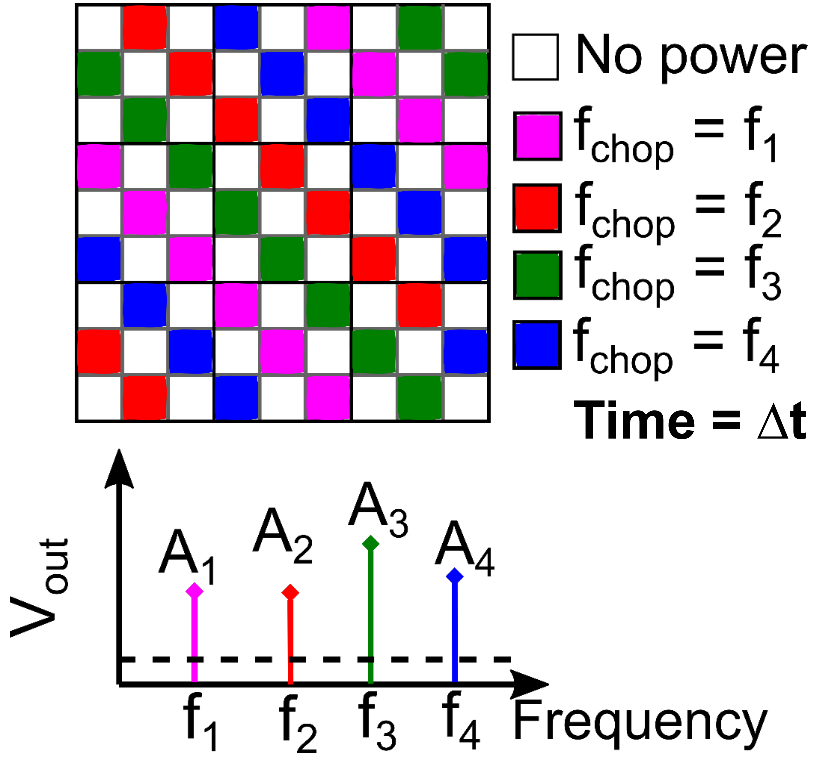
Single chopping frequency



☺ **More on pixels ⟹ Higher SNR**

☹ **Sequential patterns ⟹ Slower**

Frequency division multiplexing (FDM)

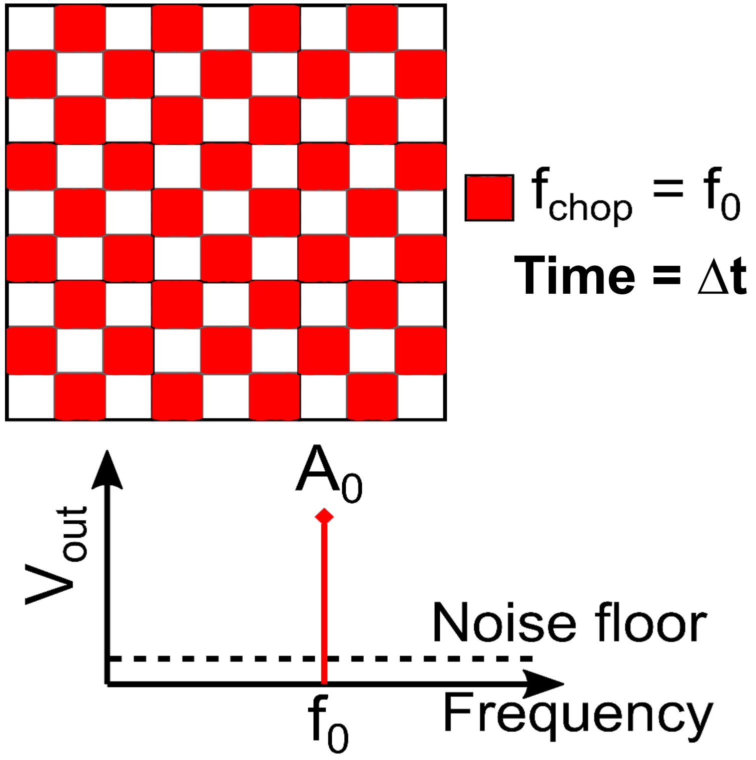


☺ **More frequencies ⟹ Faster**

☹ **Lesser pixels per pattern ⟹ Lower SNR**

Computational THz imaging (contd.)

Single chopping frequency



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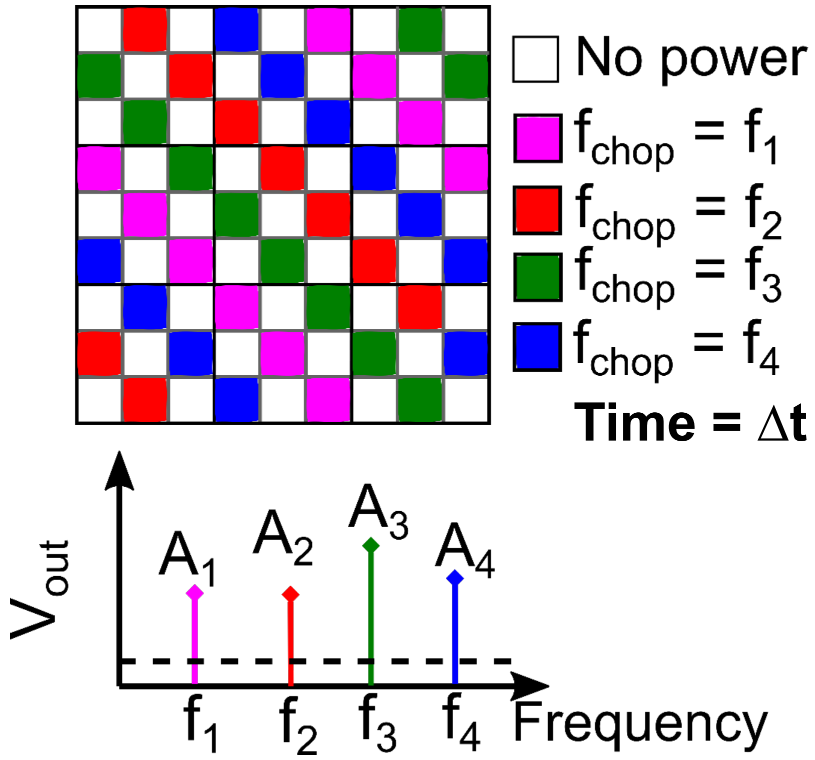

Runtime reconfigurability

- ☺ **More on pixels ⟹ Higher SNR**
- ☹ **Sequential patterns ⟹ Slower**

- ☺ **More frequencies ⟹ Faster**
- ☹ **Lesser pixels per pattern ⟹ Lower SNR**

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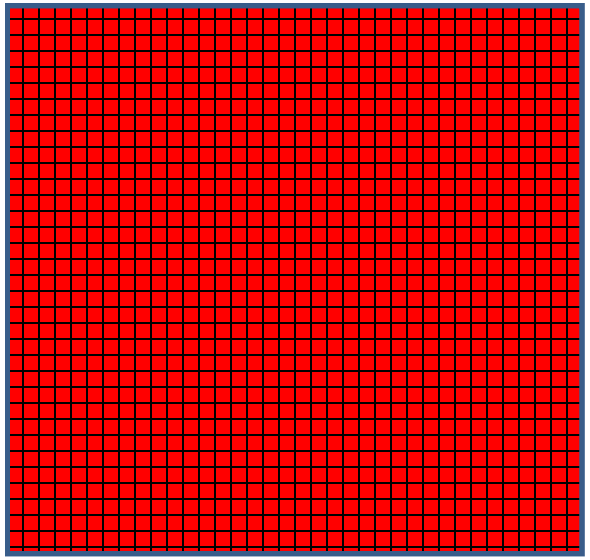
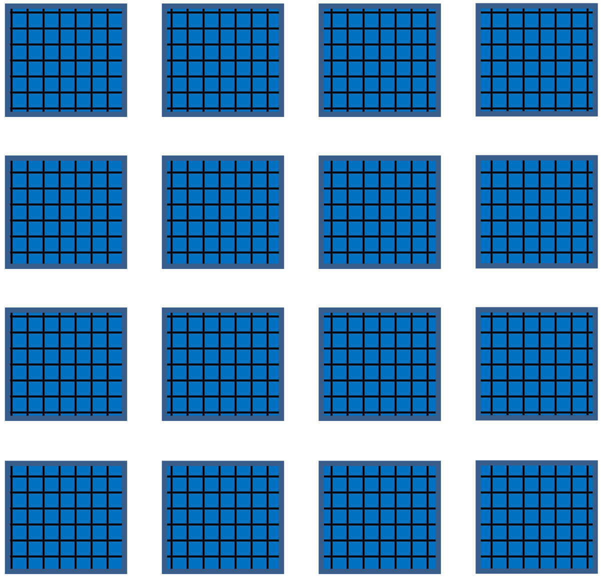
- **THz source array SoC**
  - **Architecture**
  - **Circuit design and simulations**
  - **Measurement results**
  - **Imaging results**
- Summary and outlook

How many pixels on a single SoC?

Single 32x32 pixel array



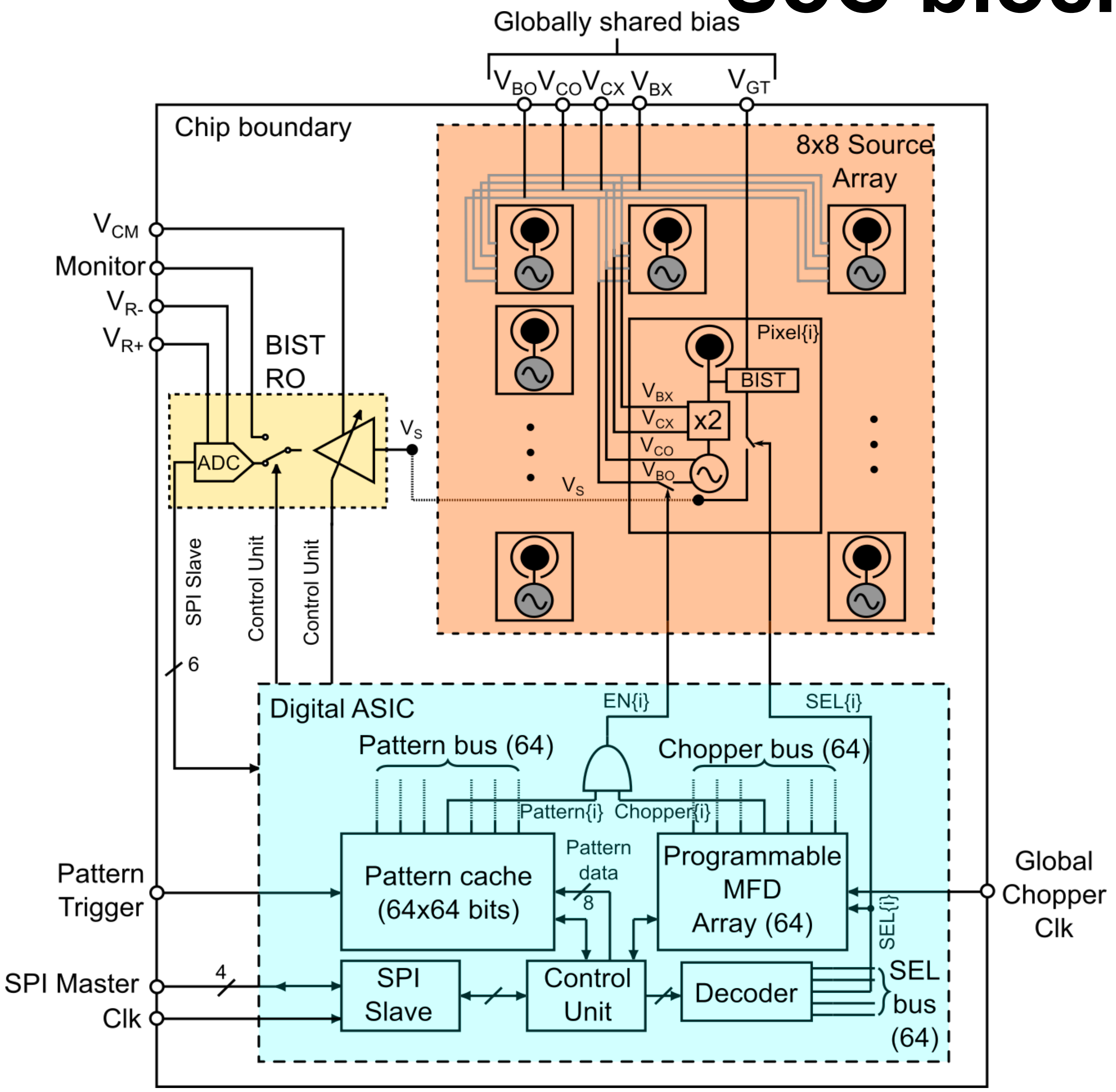
16 chips - 8x8 pixel array each



Multi-chip modules allow a more elegant system design

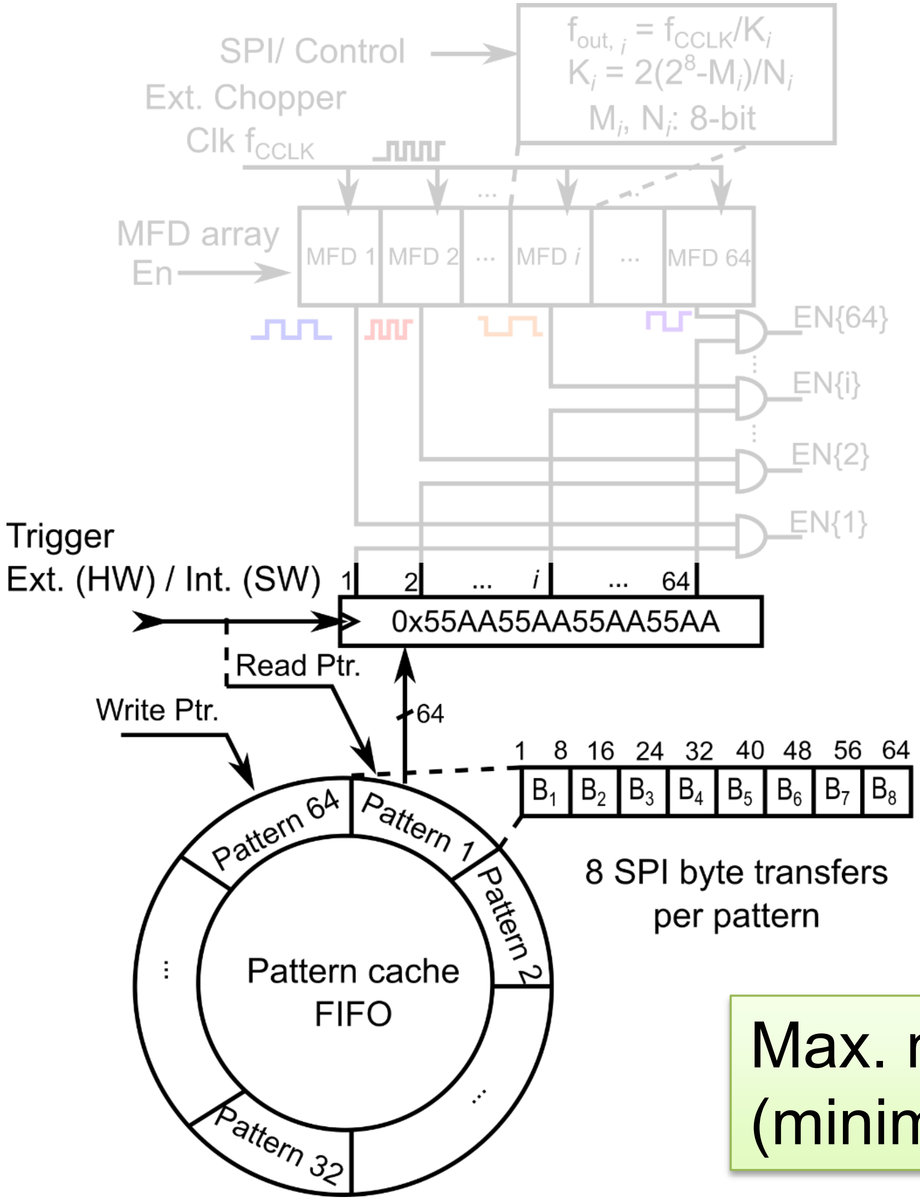
Cost (∝ Area)	Larger (144mm^2)	Lower by x16 (~9mm^2)
Thermal bottlenecks	Severe	Manageable
Variability	High	Manageable
Optics	Bulky / expensive	Lighter / cheaper

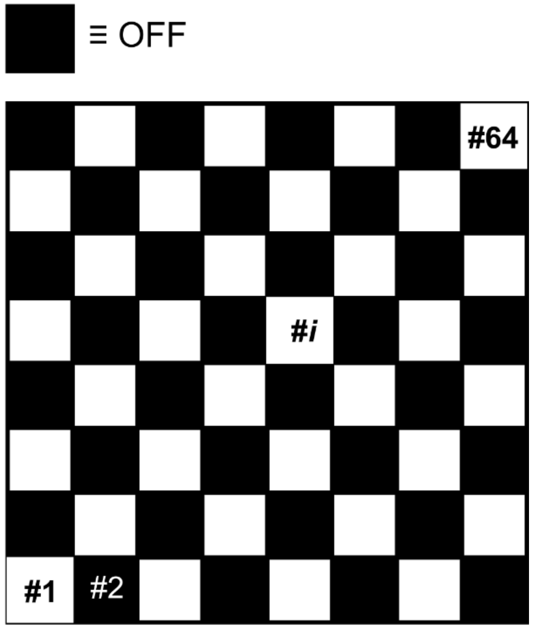
SoC block diagram



- IHP 0.13µm SiGe BiCMOS (f_T/f_{Max}=350/450GHz)
- 8x8 free-running antenna-coupled 0.42THz sources
- 4kbits circular buffer pattern cache with external edge trigger
- 64-element modulo frequency divider (MFD) array with shared global chopper clock
- Multiplexed radiation power **built-in self test (BIST)** with on-chip digital readout
- Shared RF supply lines
- On-chip SPI interface

Digital pattern reconfiguration and chopping



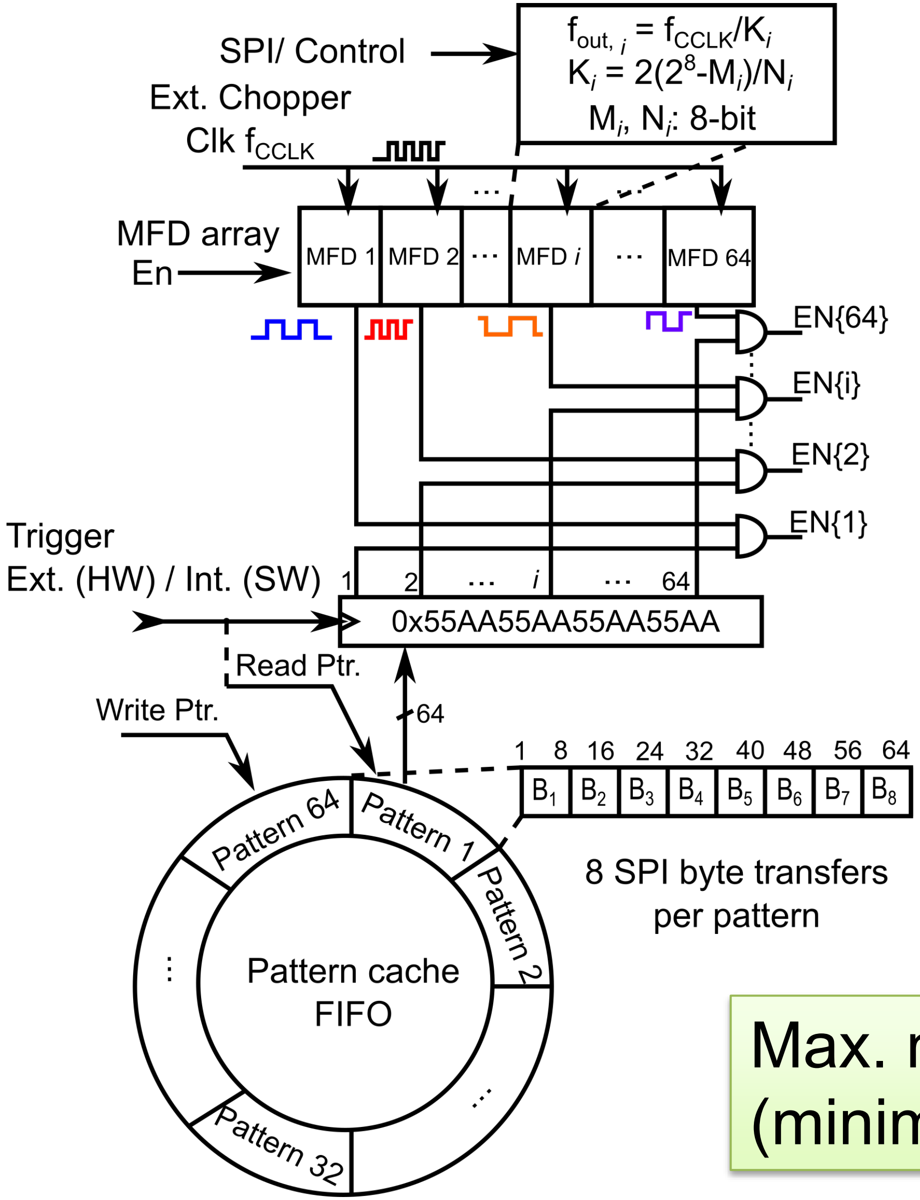


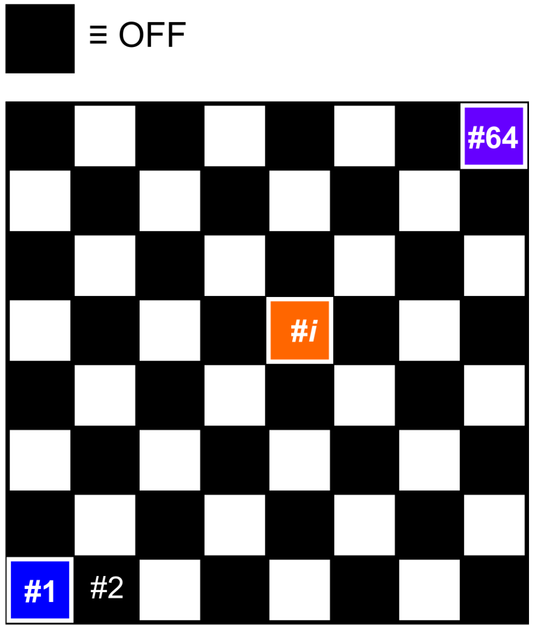
Illumination plane (pixel pattern)

- Interactive & batch pattern upload
- Trigger synchronized infinite pattern loop with batch upload
- Independent pixel-wise chopping control
- Possible chopping freq. $f_{CCLK}/2$ to $f_{CCLK}/512$ for each pixel

Max. number of patterns = number of pixels (minimal condition for free-running operation)

Digital pattern reconfiguration and chopping





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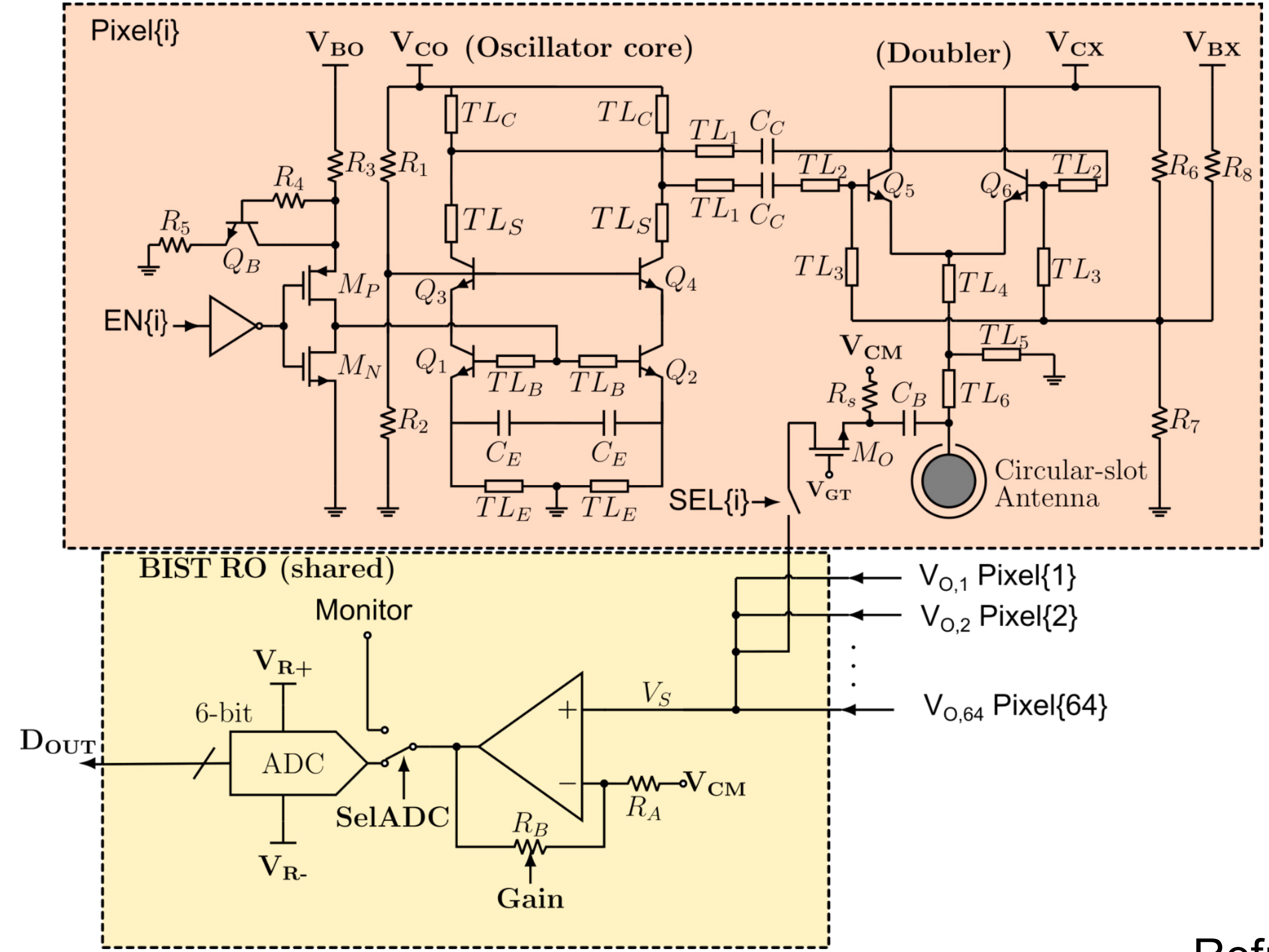
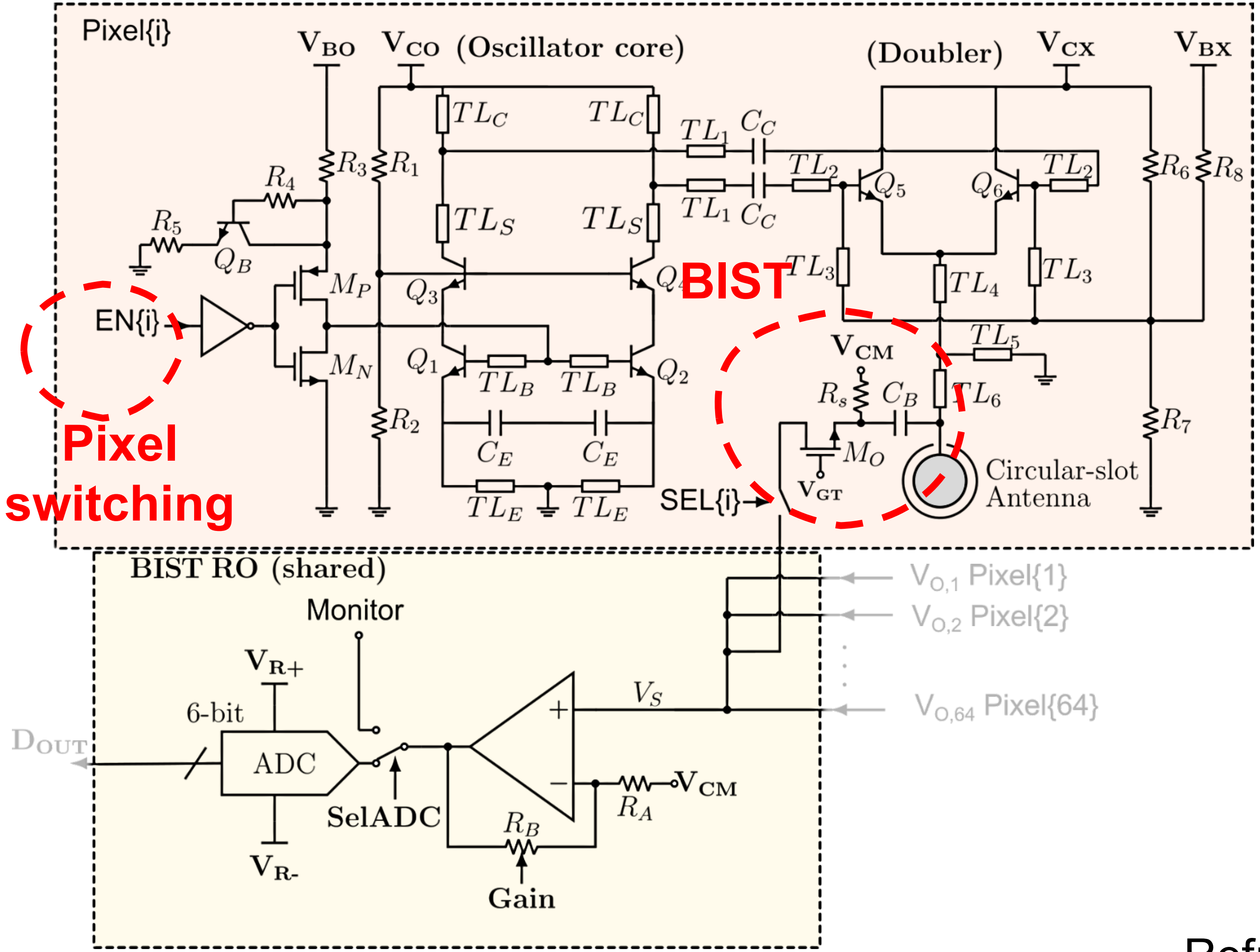
Source pixel design



- Fundamental Colpitts oscillator (simulated f_{osc} ≈ 220GHz)
- Common-collector doubler
- Sim. peak P_{rad} ≈ -1.86dBm
- Oscillator switching at base node (sim. max. freq. ≈ 8.33MHz)
- On-chip circular slot antenna
- Coupled NMOS power detector M_O (sim. coupling ≈ -15.1dB)
- Programmable BIST signal gain and digital readout

Ref: P. Hillger et al., *RFIC 2017*

Source pixel design



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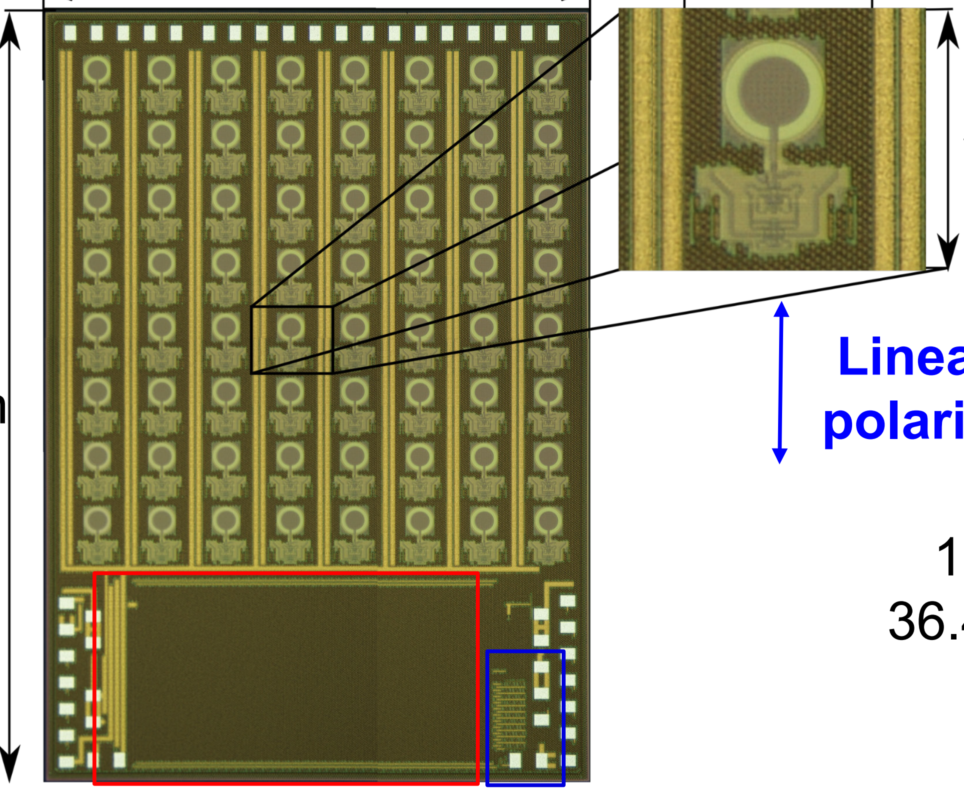
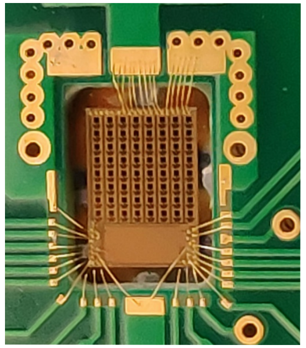
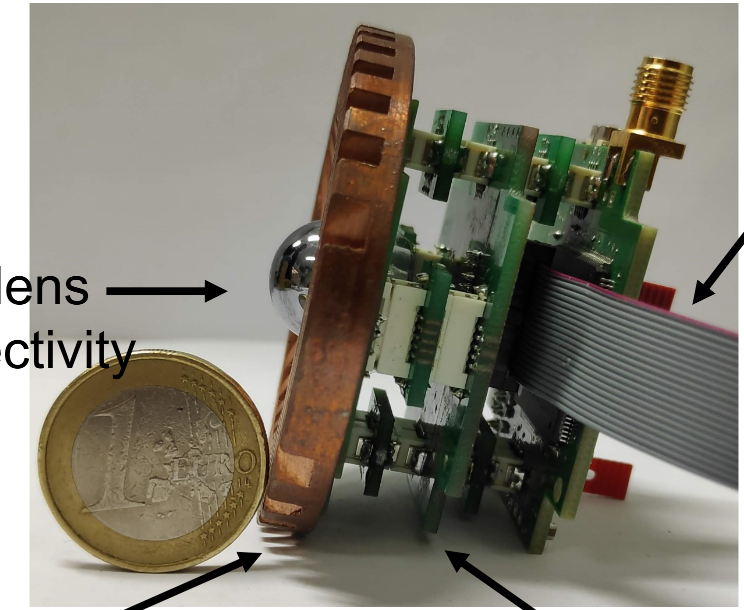
Chip micrograph and packaging







Pixel cross-coupling

RF substrate modes

- ✓ Hyperhemispherical Si-lens[1]

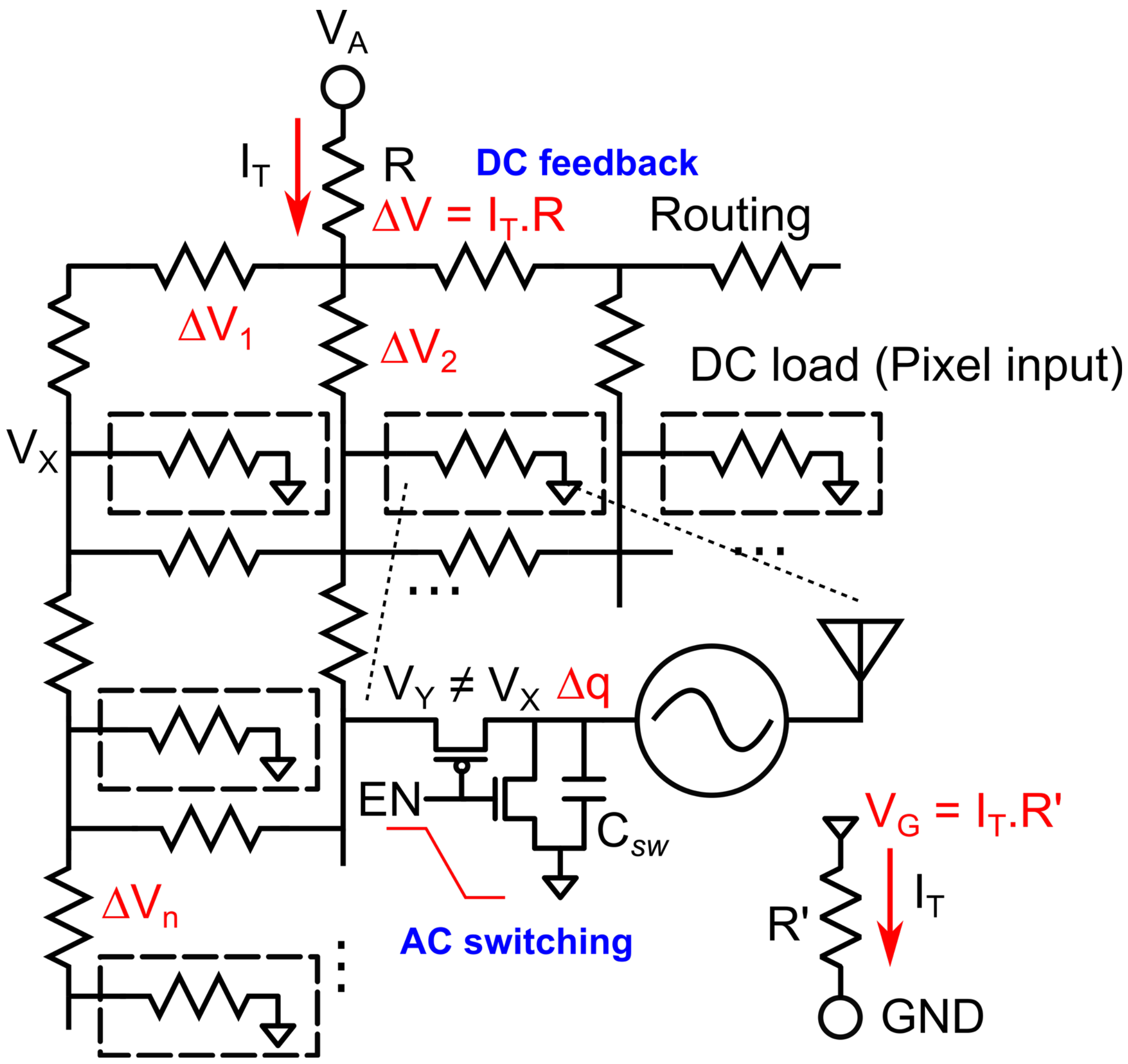
AC switching noise

- ✓ Low impedance termination at switch

DC feedback/IR drop

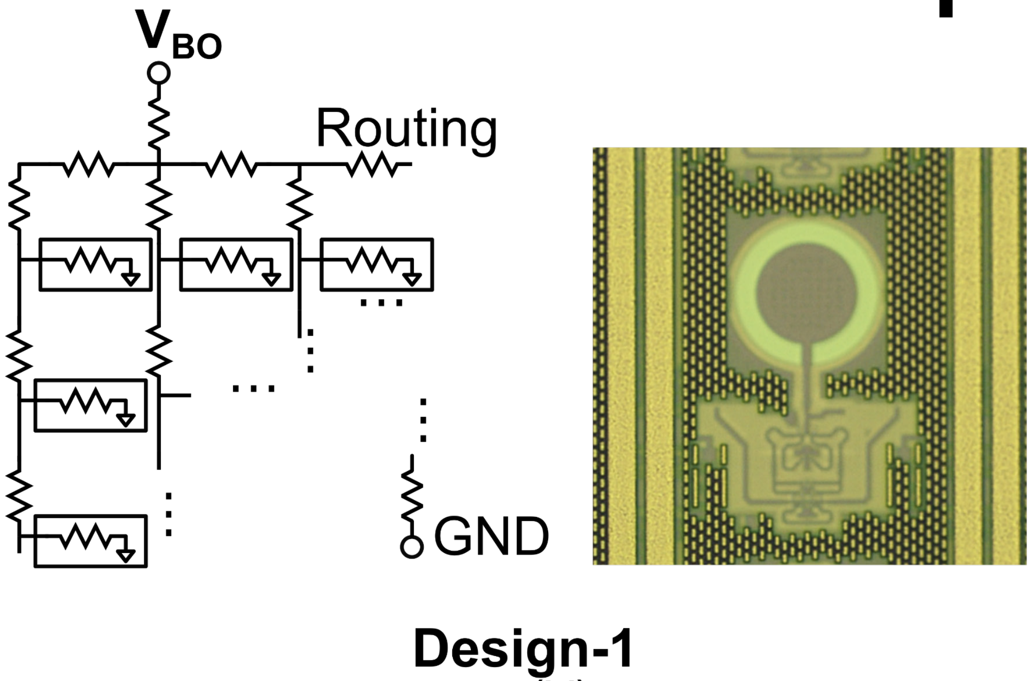
- ✓ Low resistance (0.3Ω/mm) supply routing with multiple pads
- ✓ Distributed wire mesh

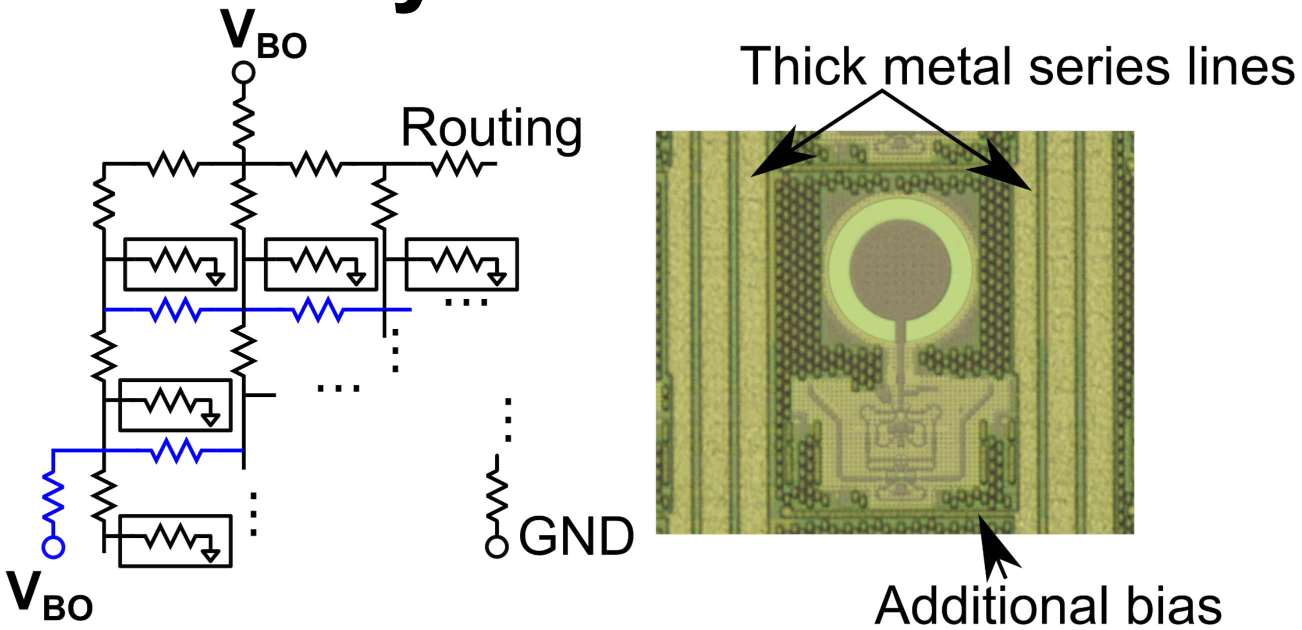
On-chip power monitoring (BIST) to calibrate any residual coupling

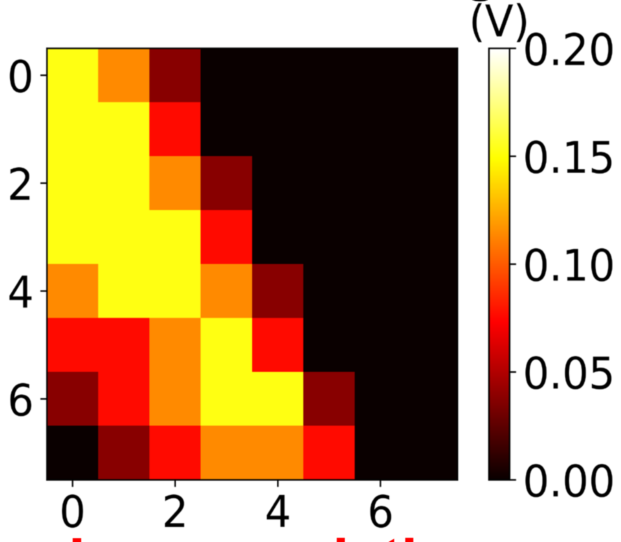


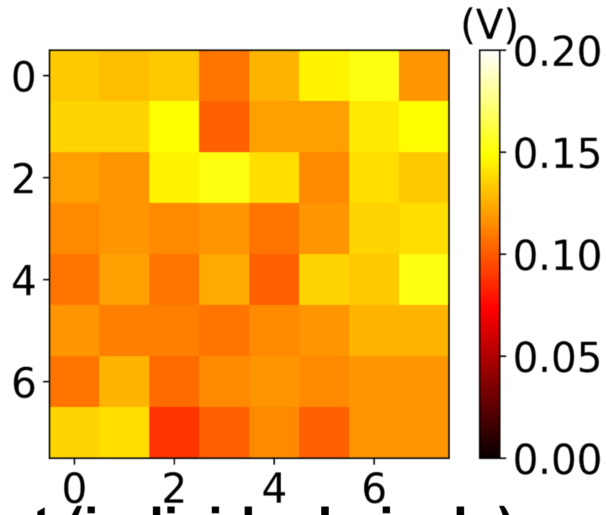
[1]J. Grzyb, U. Pfeiffer, *Journal Infrared, Millimeter, and THz Waves*, Oct. 2015

Two experimental layouts









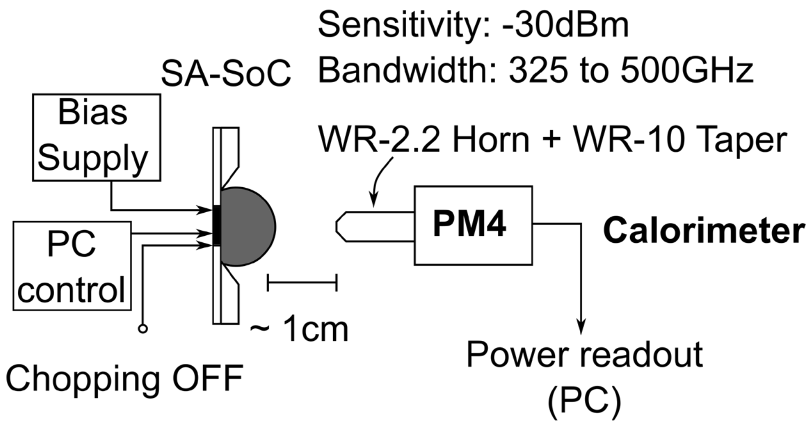
Design-2 modified at TM1-TM2 masks

< 3dB variation

Measured BIST output (individual pixels)

RF characterization setups

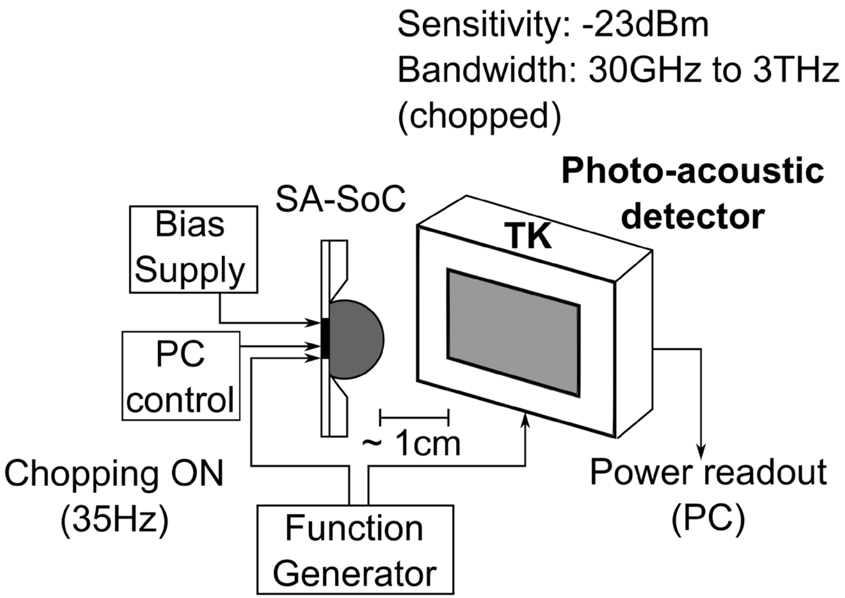
RF power (single pixel)



(Setup-A)

- ✓ Fundamental cut-off
- ✗ Sensitive to IR
- ✗ Small aperture

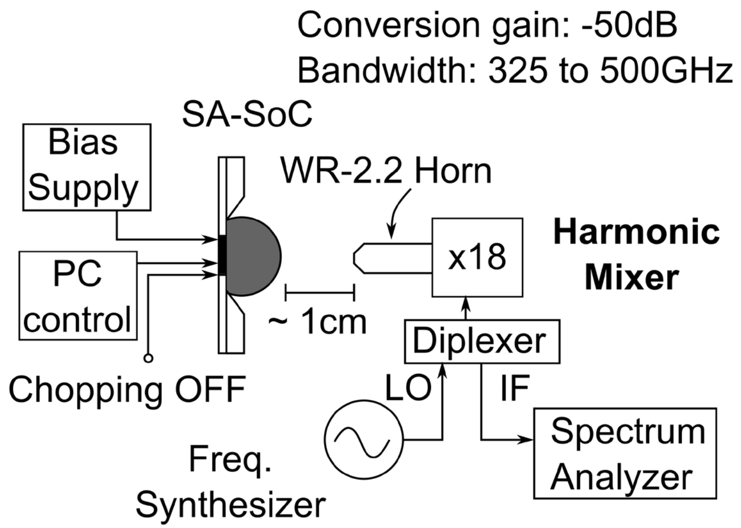
RF power (single pixel/array)



(Setup-B)

- ✓ Insensitive to IR
- ✓ Larger aperture
- ✗ All tones up to 3THz

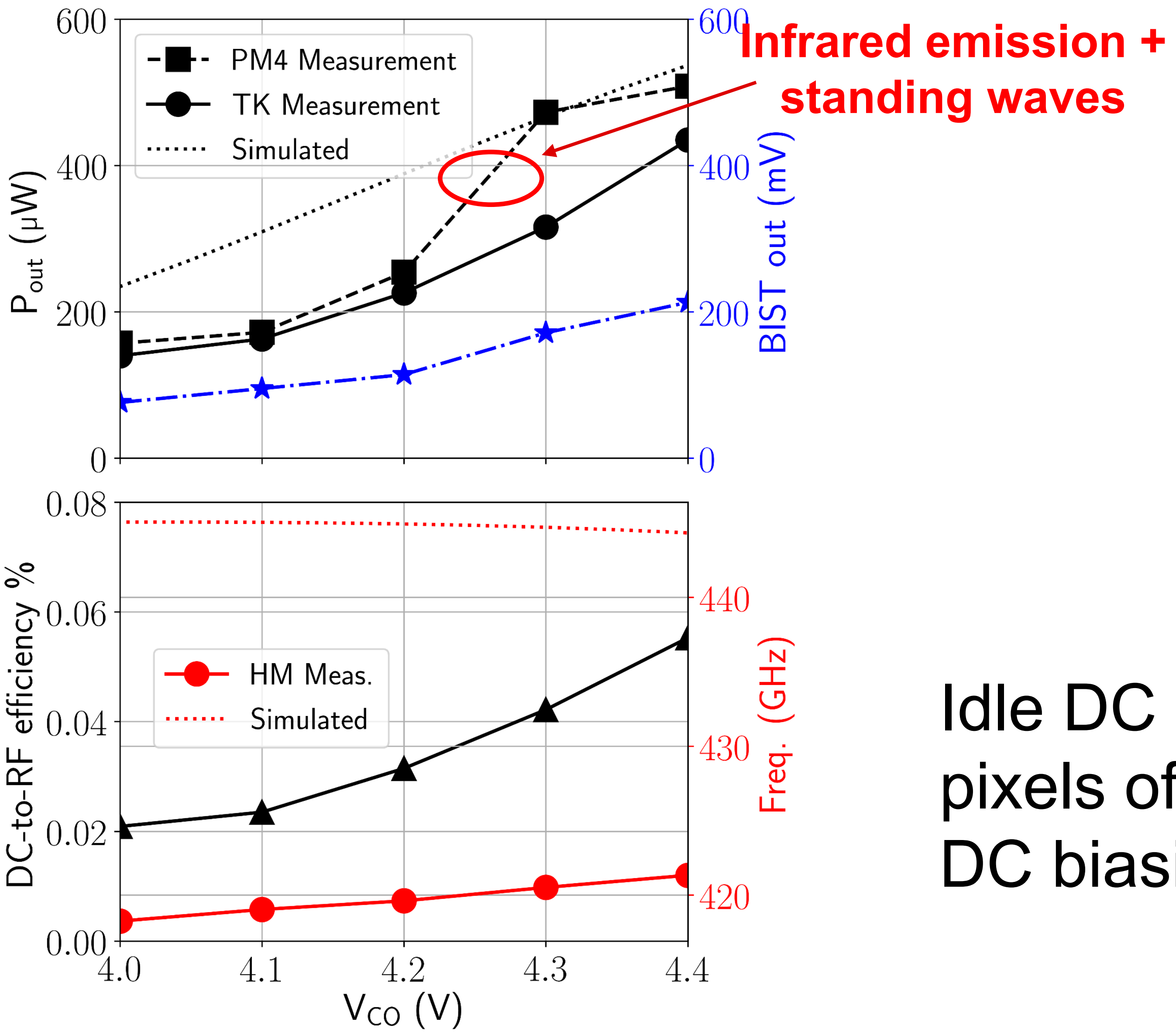
RF freq. (single pixel)

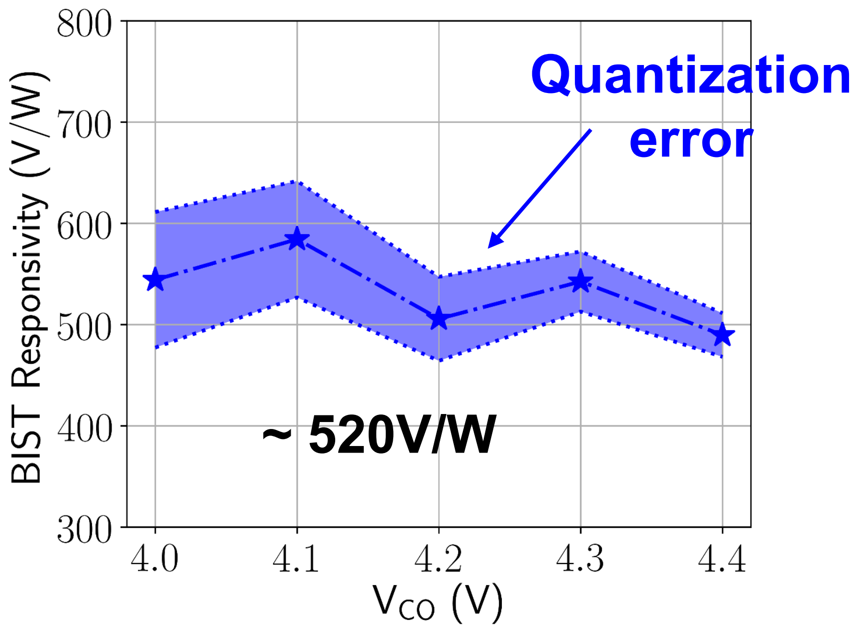


(Setup-C)

- ✓ IF freq. detection
- ✗ High conversion losses

Characterization results: single pixel

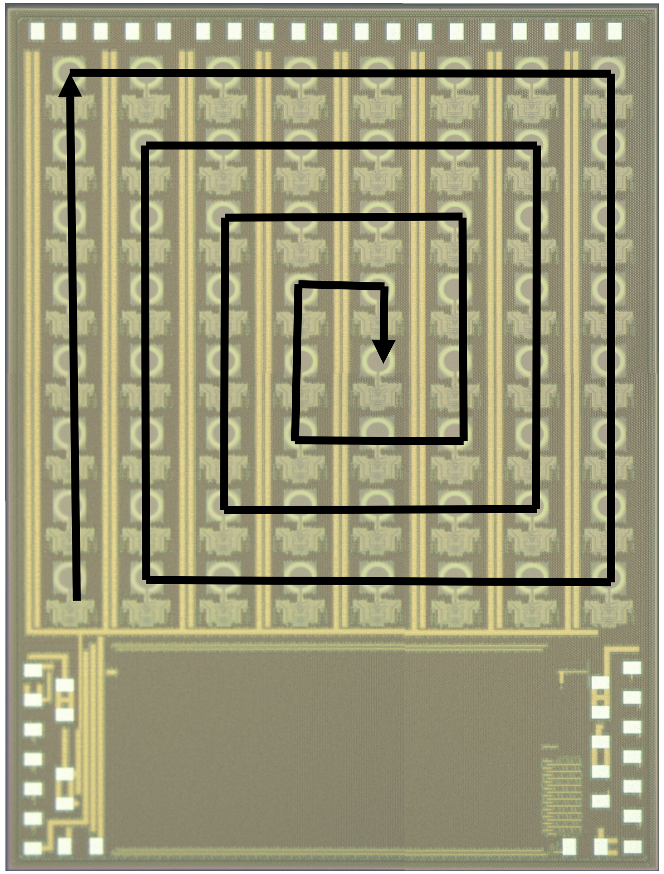


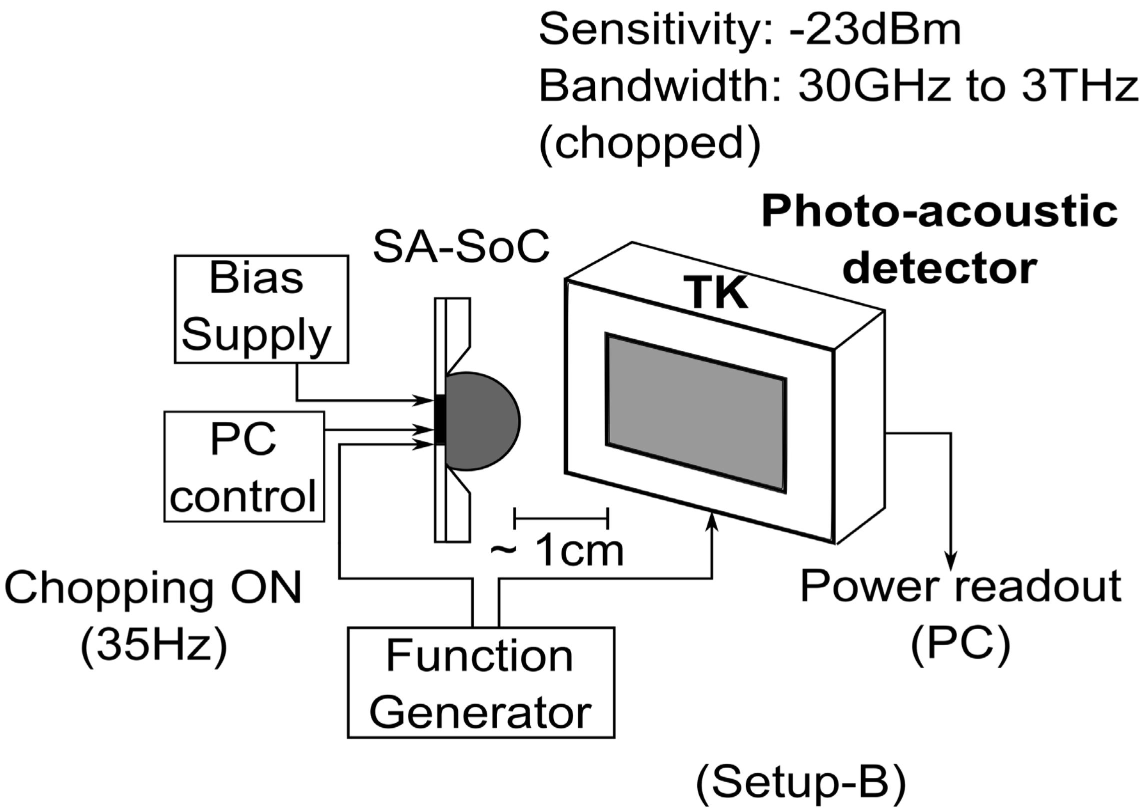


Idle DC power consumption (all pixels off) ~ **0.8W** due to resistive DC biasing.

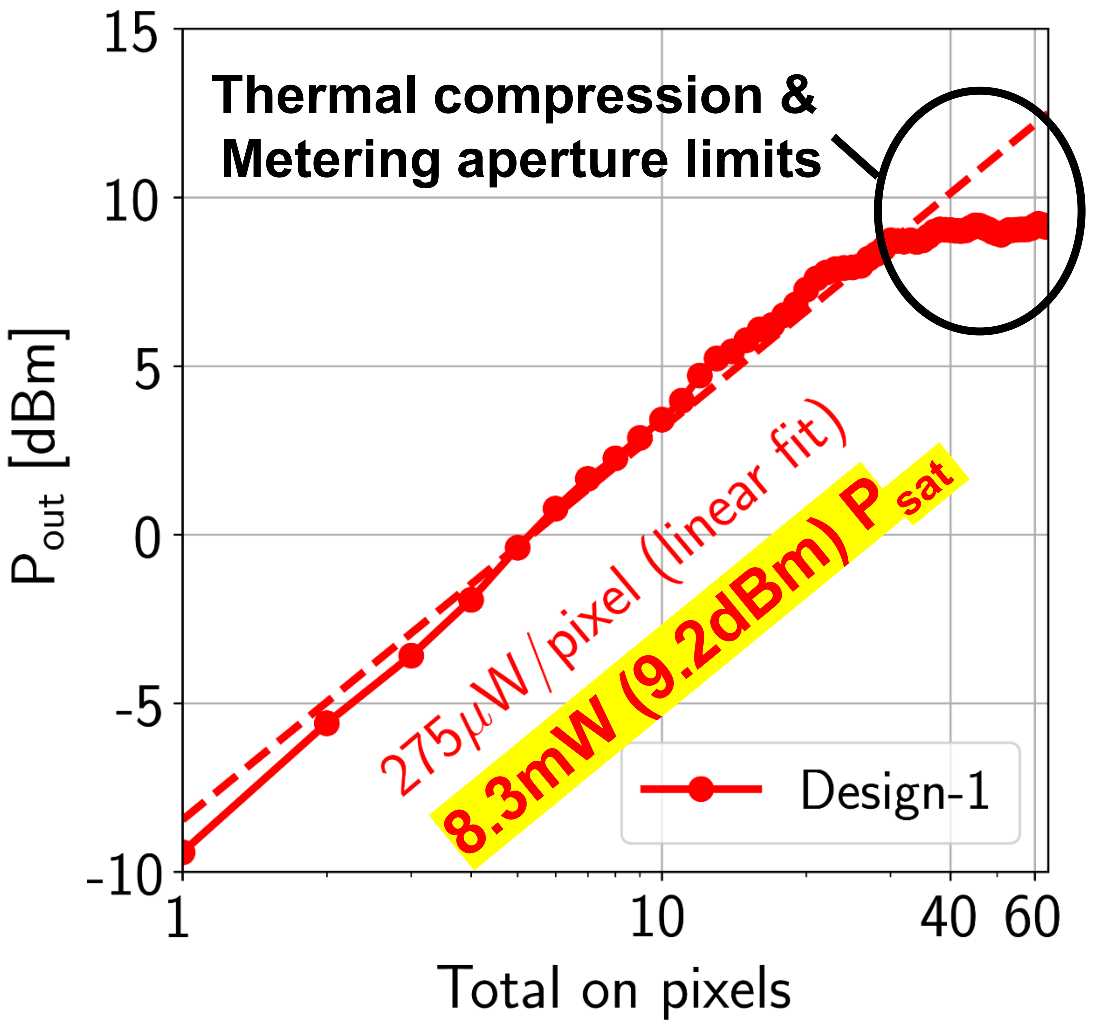
Net power measurement for array

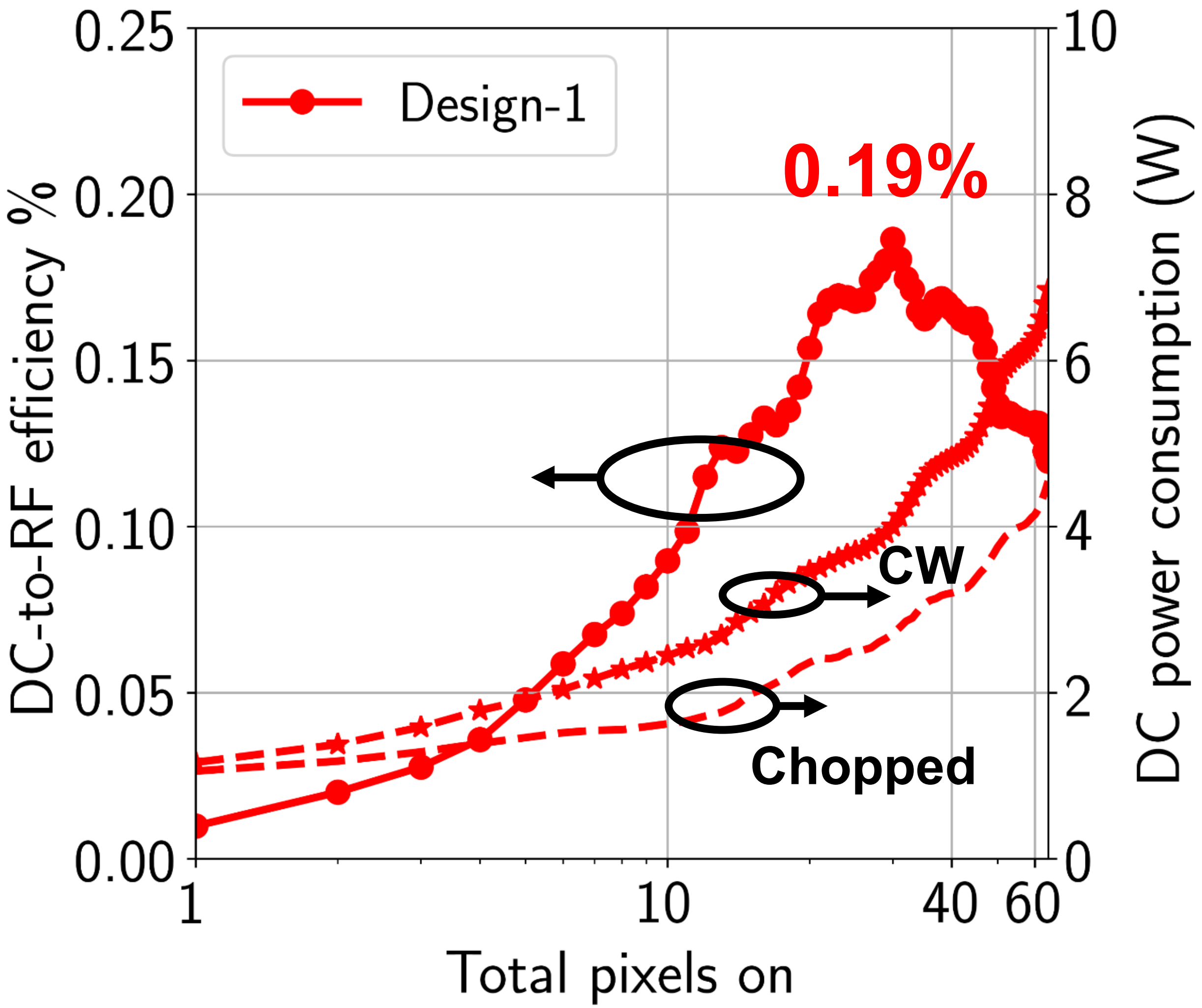
Pixel turn off sequence



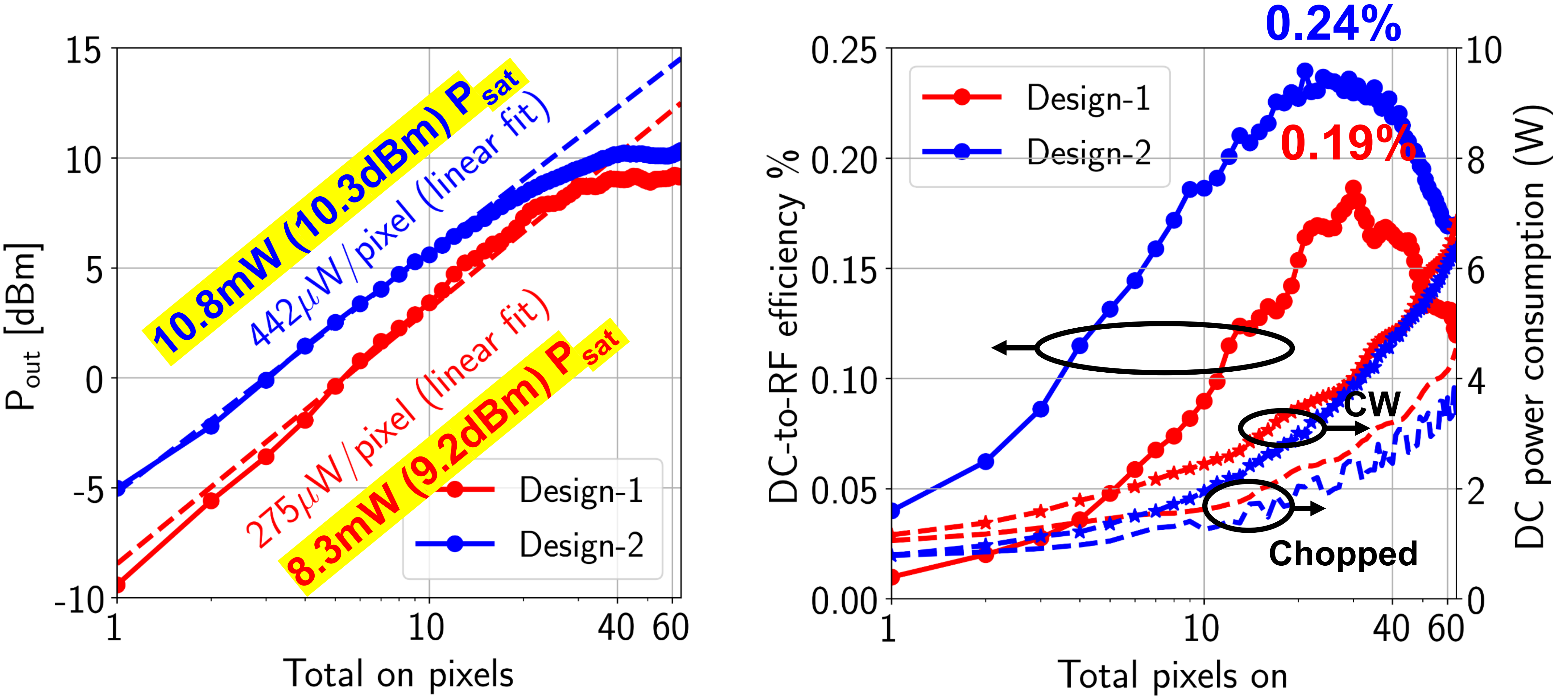


Characterization results: array



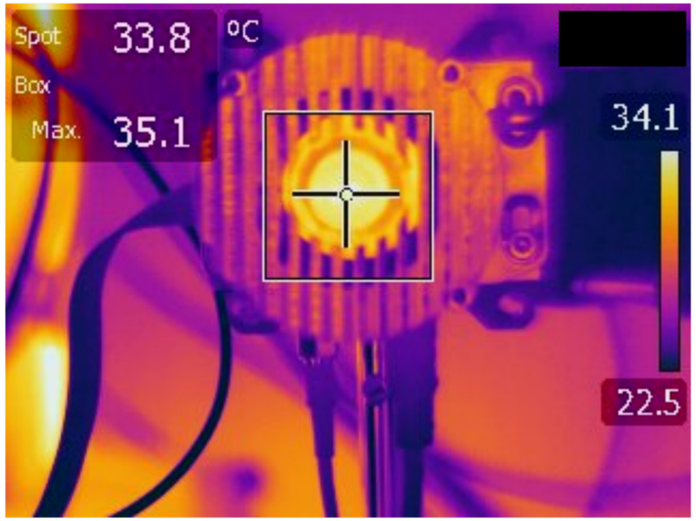


Characterization results: array

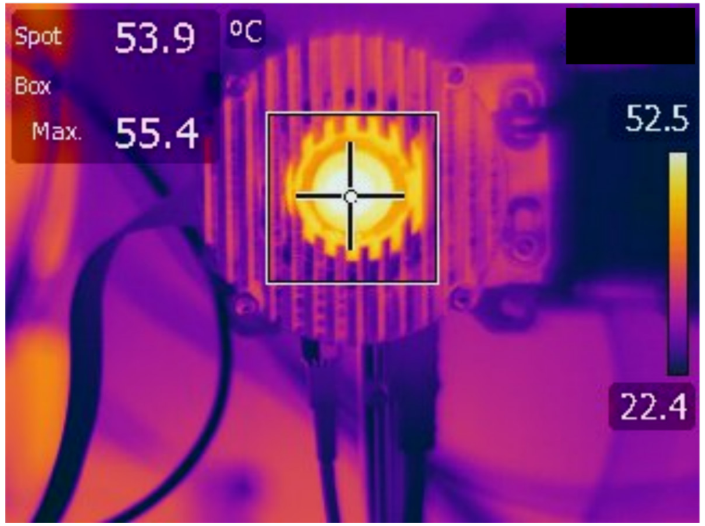


P_{1dB} at 25th pixel; P_{3dB} at 48th pixel → Linear for < 37% sparse pattern

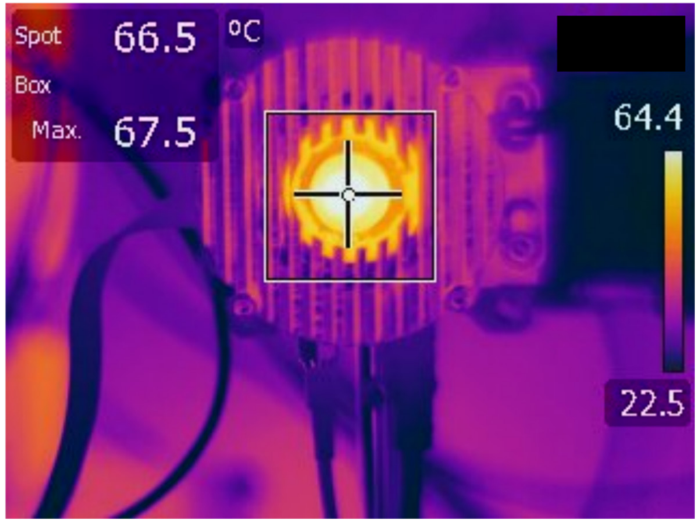
Thermal aspects



Idle (all pixels off)
P_{DC} ~ 0.8W



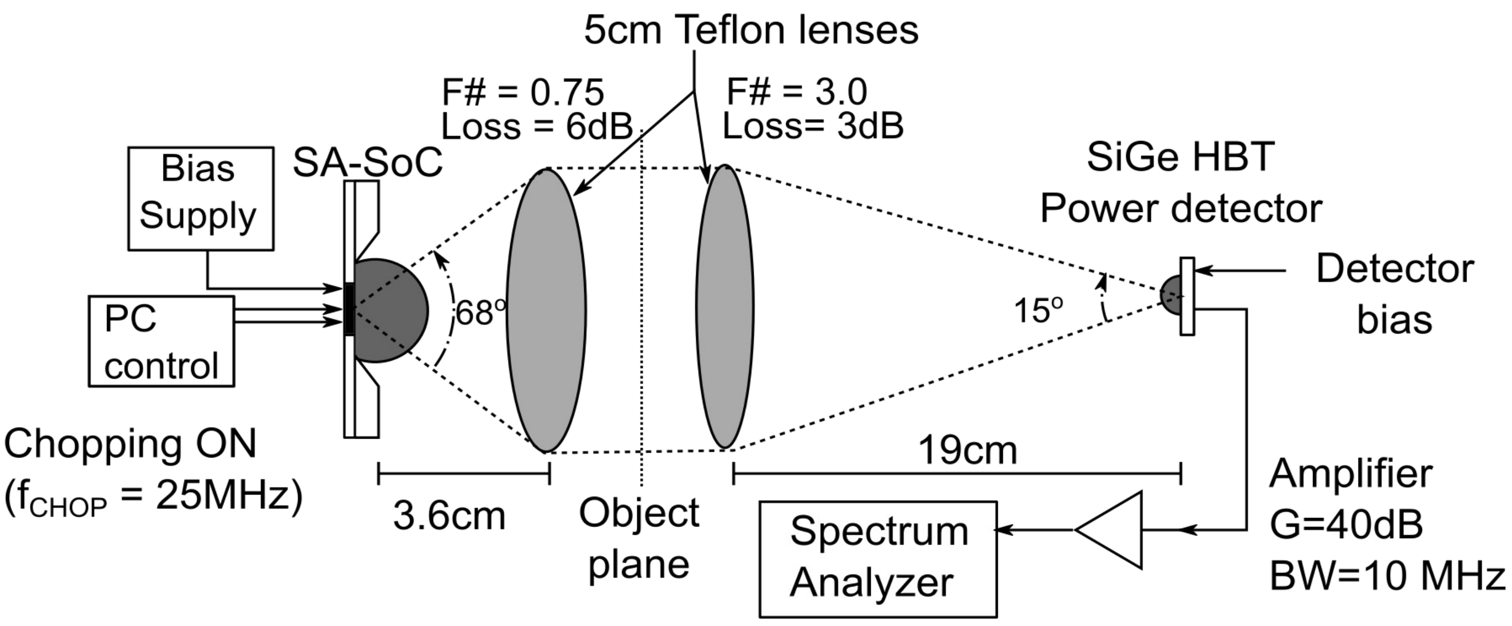
50% sparse (32 pixels off)
P_{DC} ~ 2.8W

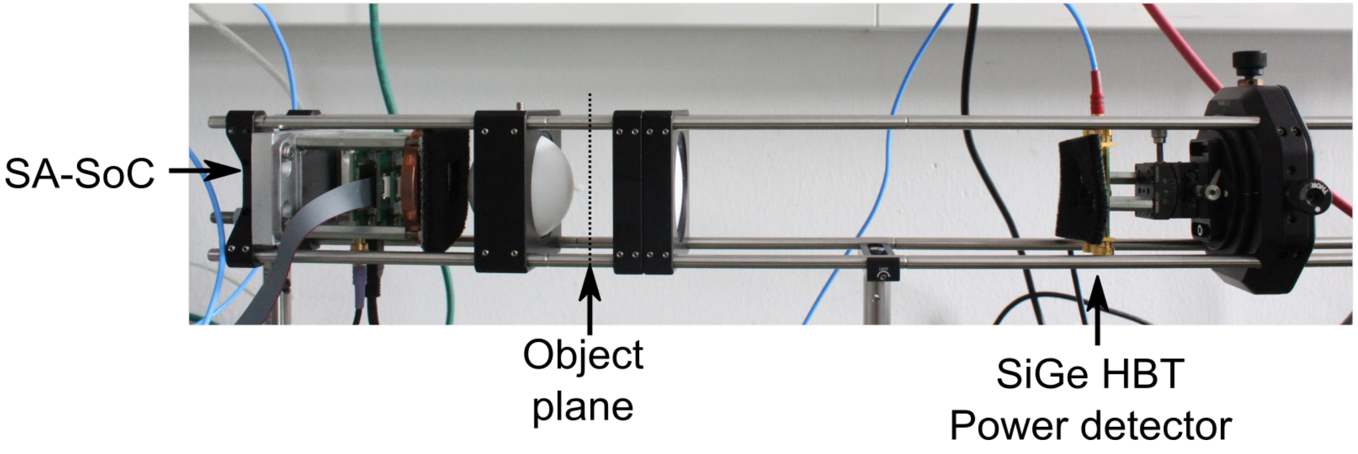


All pixels on
P_{DC} ~ 4.5W

Global chopping (1MHz) turned on in all cases!

System characterization & imaging setup



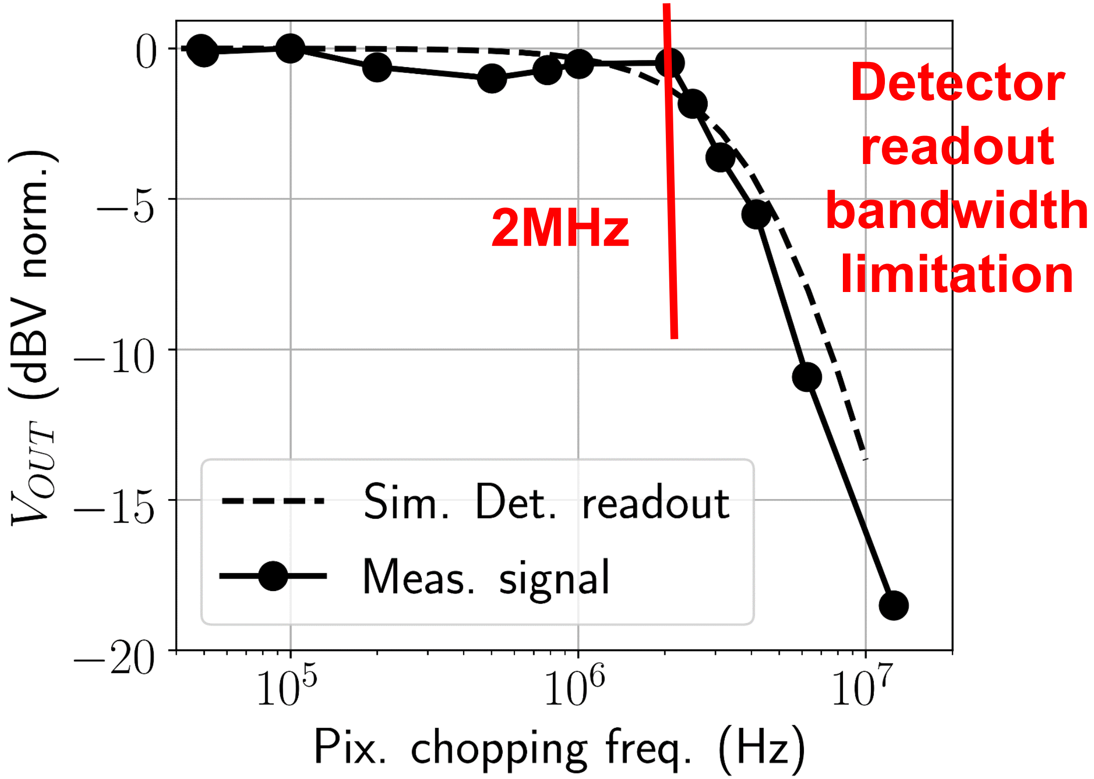


- Matched optics
- Embedded lens losses
- HBT power detector
- **NEP ~ 8pW/ $Hz^{0.5}$**
- **R_V ~ 700V/W**

[Ref: M. Andree et al., IEEE *IMS* 2019]

System characterization results

Sim. Maximum switching freq. = 8.33MHz

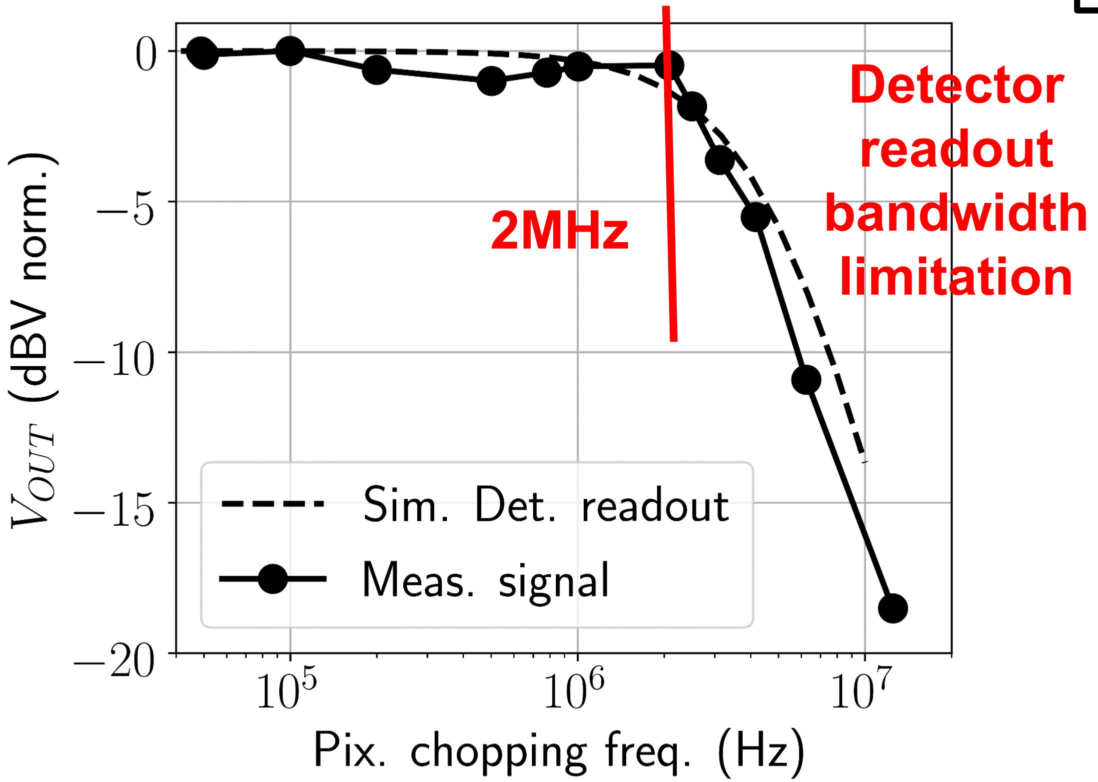


Switching freq. characterization

For 64 pattern image: 2MHz × (1/64) = 31250 fps max.

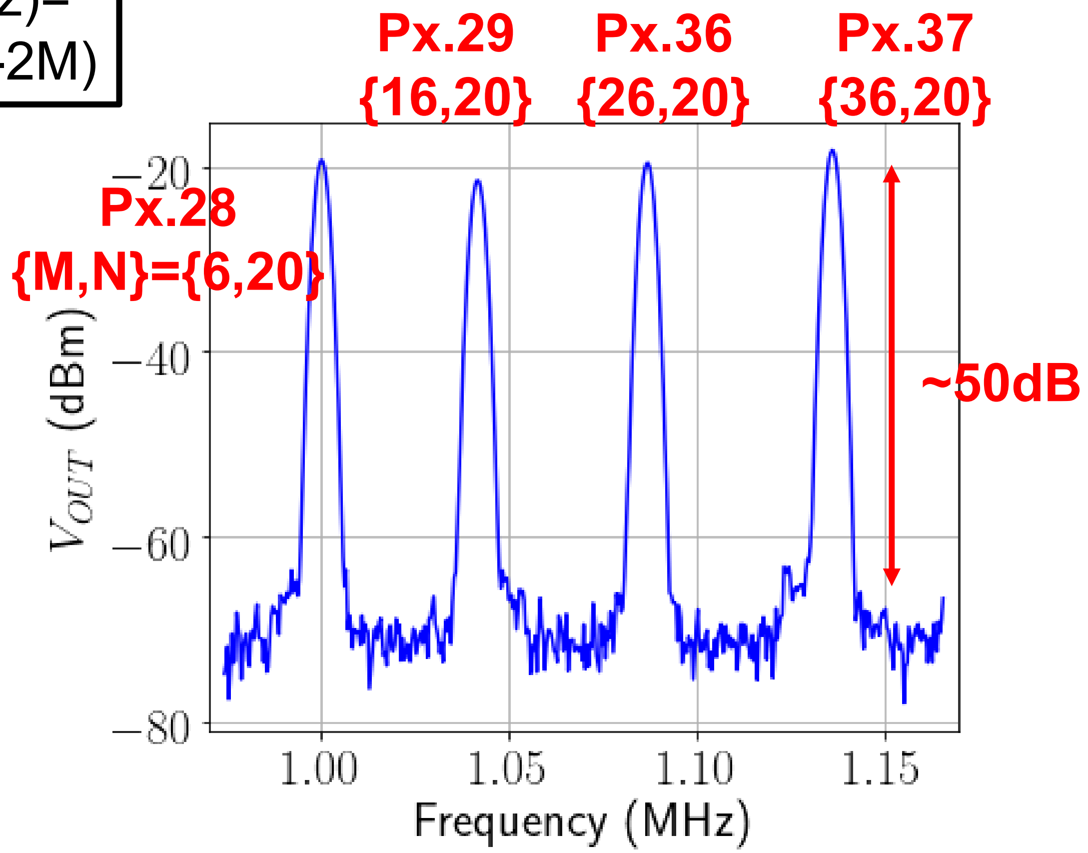
System characterization results

Sim. Maximum switching freq. = 8.33MHz



Switching freq. characterization

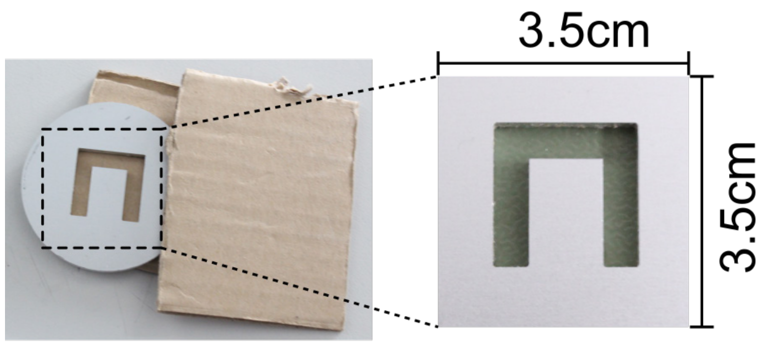
f_{CHOP} (MHz)= 25×N/(512-2M)



Chopping freq. multiplexing (Detector signal spectrum)

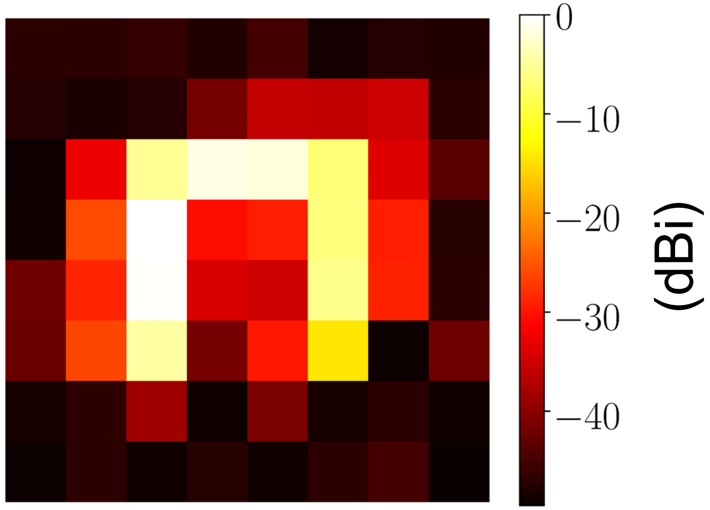
For 64 pattern image: 2MHz × (1/64) = 31250 fps max.

Imaging results



Object

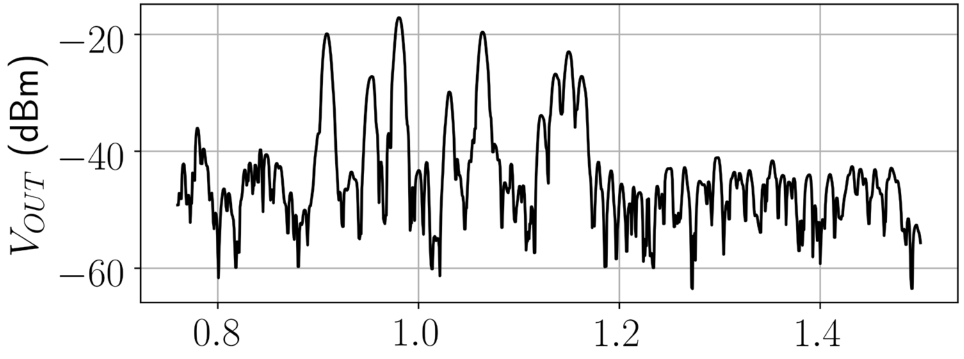
Test 1: Single pixel switching
f_{CHOP} (global) = 1MHz
Software defined pattern trigger



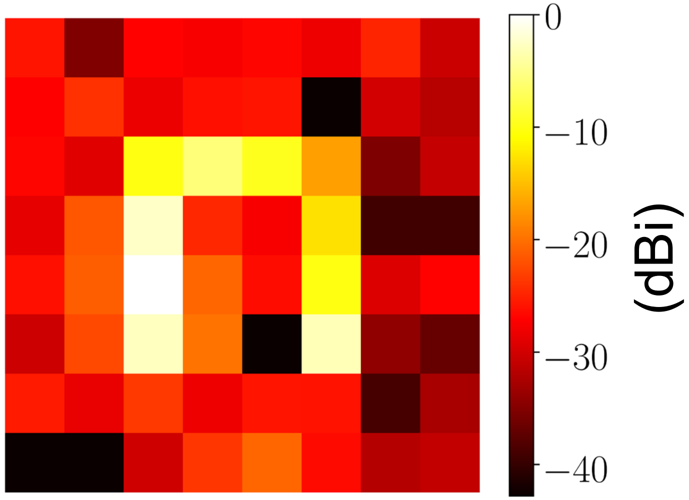
Acquisition time ~ 15s
(incl. >13s SA read time)

Test 2: Frequency multiplexing
f_{CHOP} = 0.76MHz – 1.47MHz
(M = 125-188, N=8)

Single shot spectra
(100ms acq. time)



Reconstructed Image



Demo session DS2
25fps (40ms/frame)

State-of-the-art comparison

	This work (Design-1)	This work (Design-2)	ISSCC 2014	JSSC 2015	ISSCC 2014	TMTT 2013	JSSC 2018
Technology	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130nm SiGe	130nm SiGe	65nm bulk CMOS	45nm SOI CMOS	130nm SiGe
Freq.(GHz)	420	420	530	317	338	420	1010
Rad. Power(dBm)	9.2	**10.3**	0	5.2	-0.9	-10	-10.9
Coherent	No	No	No	Yes	Yes	Yes	Yes
EIRP(dBm)	32.8[1,3]	--	25[2]	22.5	17.1	3	13.1
Radiators	64	64	16	16	16	8	91
Power/pix.(dBm)	-3.6[3]/-6.5[4]	-- / -3.54[4]	-11.3[3]	-6.84[5]	-12.9[5]	-19.03[5]	-30.5[5]
Freq. Tuning(%)	0.7	0.7	3.2[1]	0.06	2.1	10	-
DC-to-RF Eff.(%)	0.19	0.24	0.04	0.54	0.053	0.014	0.0073
Area(mm2)	12.6	12.6	4.2	2.1	3.9	10.26	1
Spatial Mod. Rate	2MHz	2MHz	-	Not Applicable			
FDM (chopping)	Yes	Yes	No				
BIST/ calibration?	Yes	Yes	No				
SoC Integration?	Yes	Yes	No				

[1]Single px., estimated; [2]Single px. ; [3]Peak; [4]Avg., linear fit; [5]Net coherent output power normalized to number of radiators

Outline

- Motivation
- Reciprocal & Computational THz imaging
- THz source array SoC
  - Architecture
  - Circuit design and simulations
  - Measurement results
  - Imaging results
- **Summary and outlook**

Summary and outlook

- 8x8 pixels **unlocked array** at 0.42THz
- 10.3dBm net P_{out} (unlocked), 0.24% peak efficiency (Design-2)
- Integrated ASIC for
  - Pixel pattern programming
  - Programmable FDM
  - BIST and digital readout
  - SPI interface
- Switching speed > 2MHz
- **Fast (up to 31kfps), high SNR (> 50dB) imaging with single pixel camera**
- **Potential multi-chip module integration for large-scale systems**

World's first dedicated THz source array for reciprocal, computational THz imaging

Acknowledgments

- DFG individual grant SI-STAR
- DFG priority program SPP 1798 CoSIP Phase-I
- E. Ashna, R. Zatta, and W. Förster; IHCT, University of Wuppertal
- Dr. Bernd Heinemann, IHP Microelectronics

QUESTIONS ?

A 0.59THz Beam-Steerable Coherent Radiator Array with 1mW Radiated Power and 24.1dBm EIRP in 40nm CMOS

Kaizhe Guo and Patrick Reynaert
KU Leuven, Leuven, ESAT-MICAS, Leuven, Belgium

Outline

- Background and Challenge
- Coherent Radiator Array Design

  -Array Architecture

  -Oscillator Core

  -Coupling Structure

  -Antenna
- Measurement
- Conclusion

Outline

- Background and Challenge
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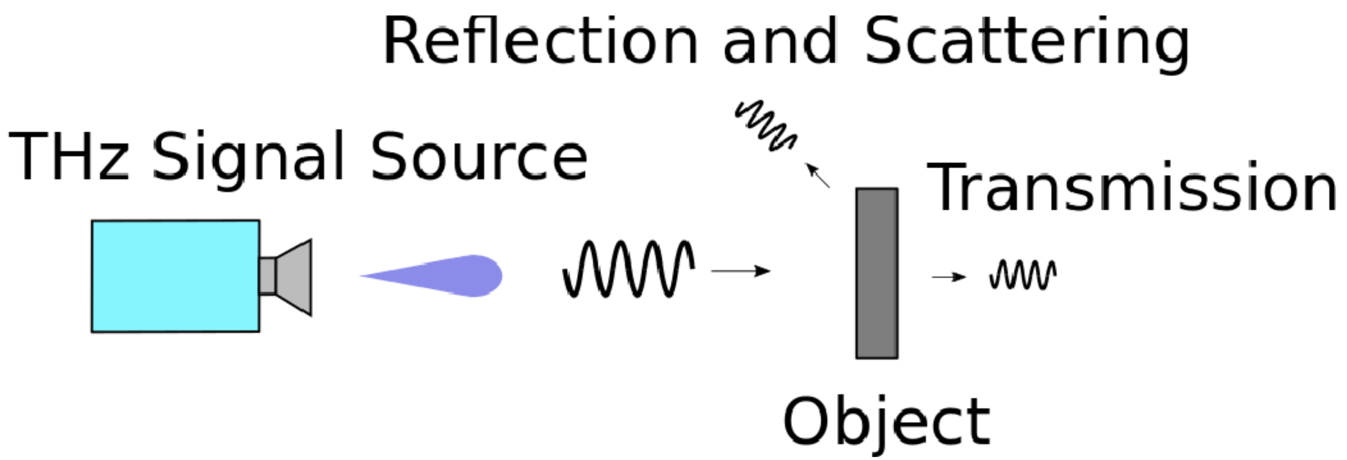
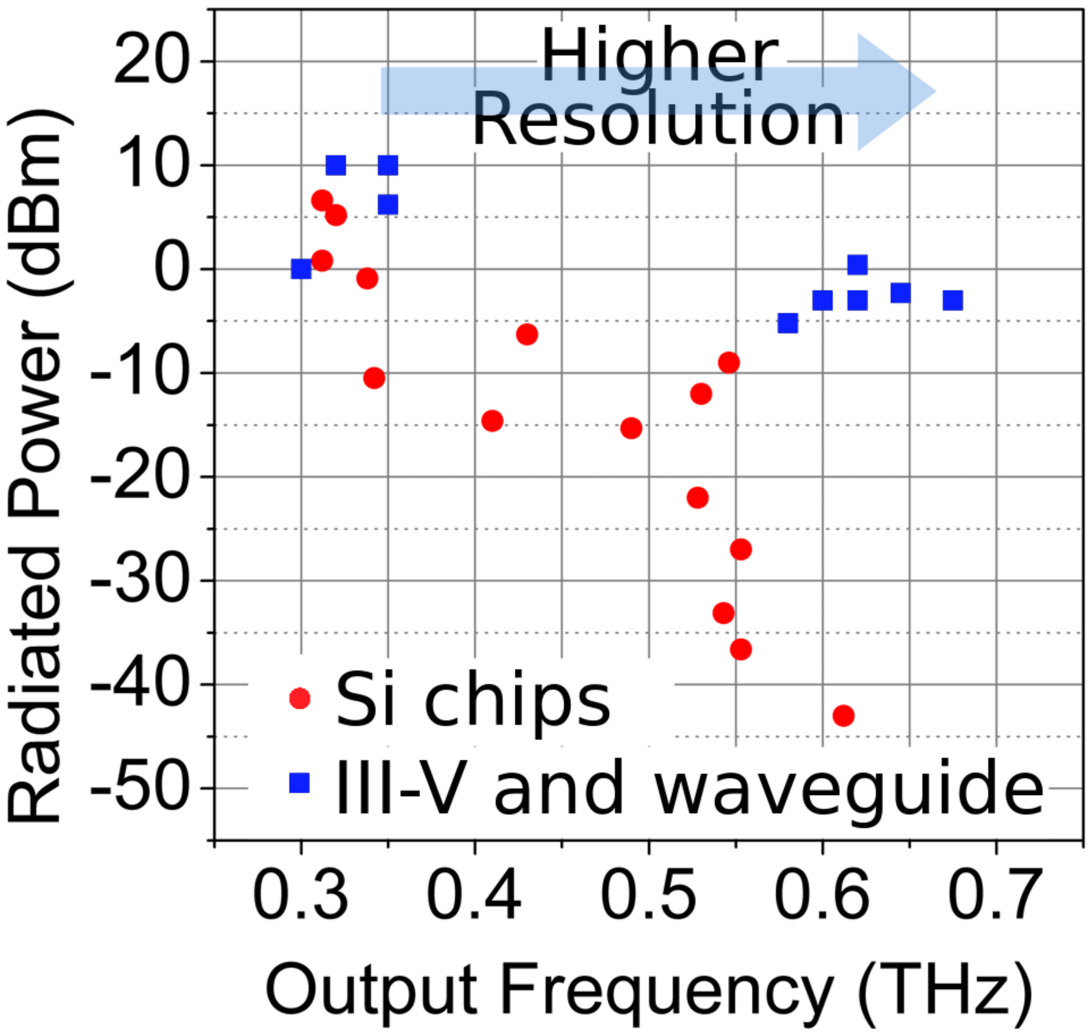
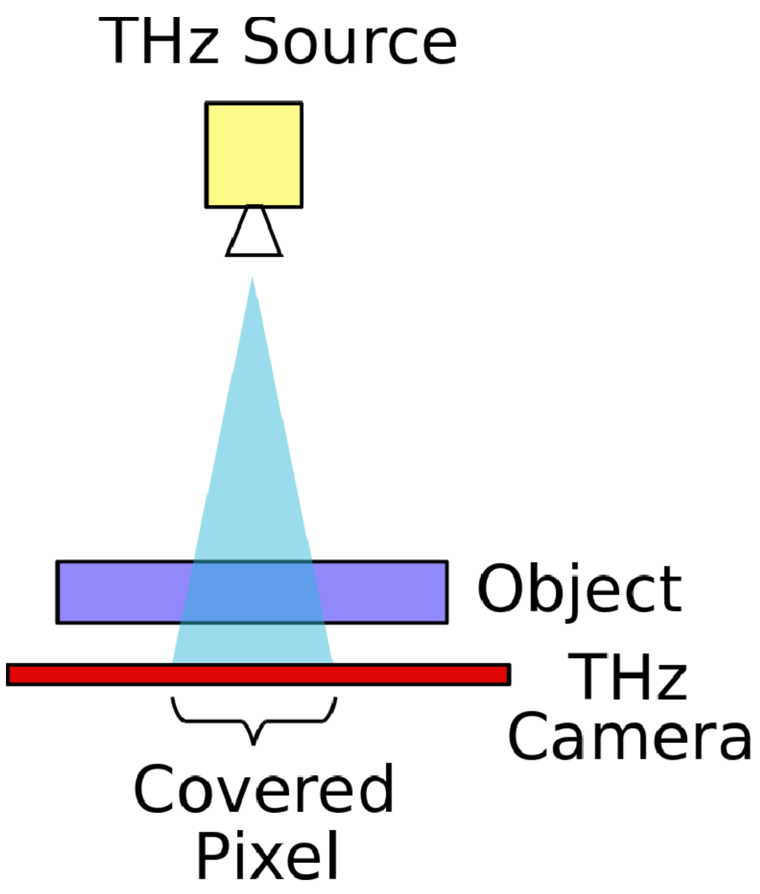
Signal Source in Active THz imaging System





- CMOS chips: cheap and compact
- Low power at high frequency

How to Illuminate More Area



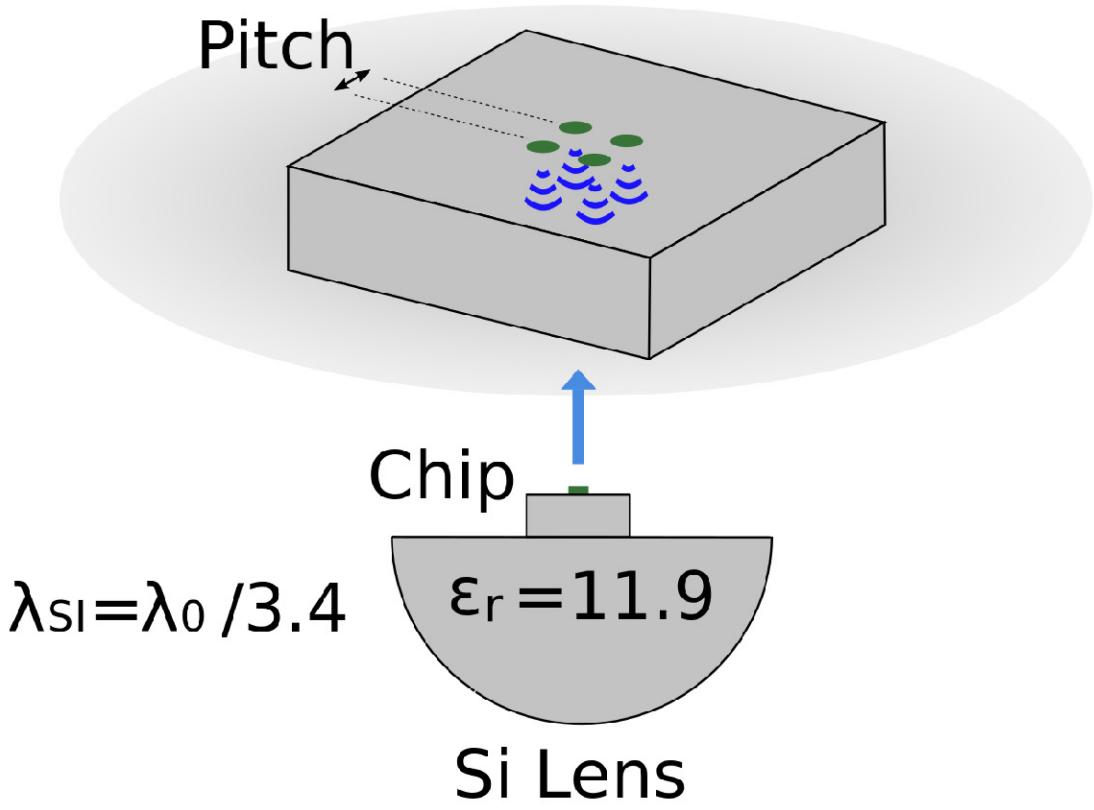
- More radiator elements

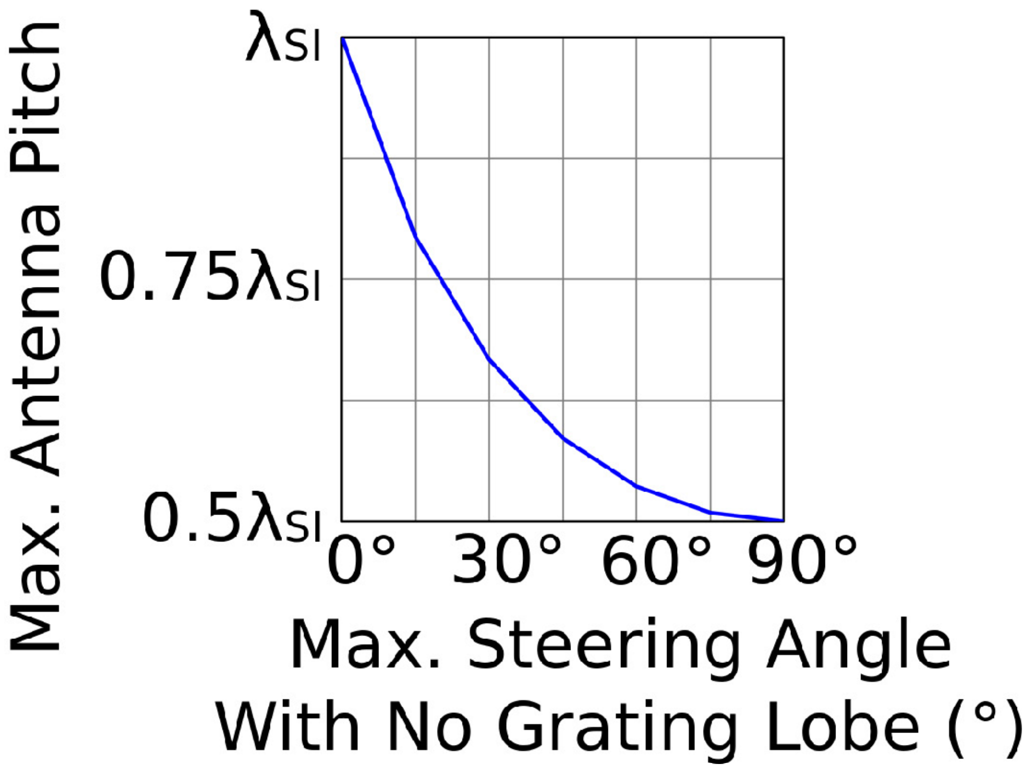
Element Number in the Radiating Source (P_{rad})	Covered Pixel Number With Total NEP of 12nW and SNR of 20dB
1 Element (28μW)	23
36 Elements (1mW)	830

- Beam-steering

Beam-Steering Approach	Speed of Beam-Steering
Mechanical Scanning	Determined by Mechanical Limits
Electronic Beam-Steer	Faster Speed

Challenge: Small Antenna Pitch





- Larger scan range ➡ smaller pitch ➡ smaller radiator dimension
- 30° max. steering angle: pitch$\leq 0.66\lambda_{SI}$(100μm@0.59THz)

Outline

- Background and Challenge
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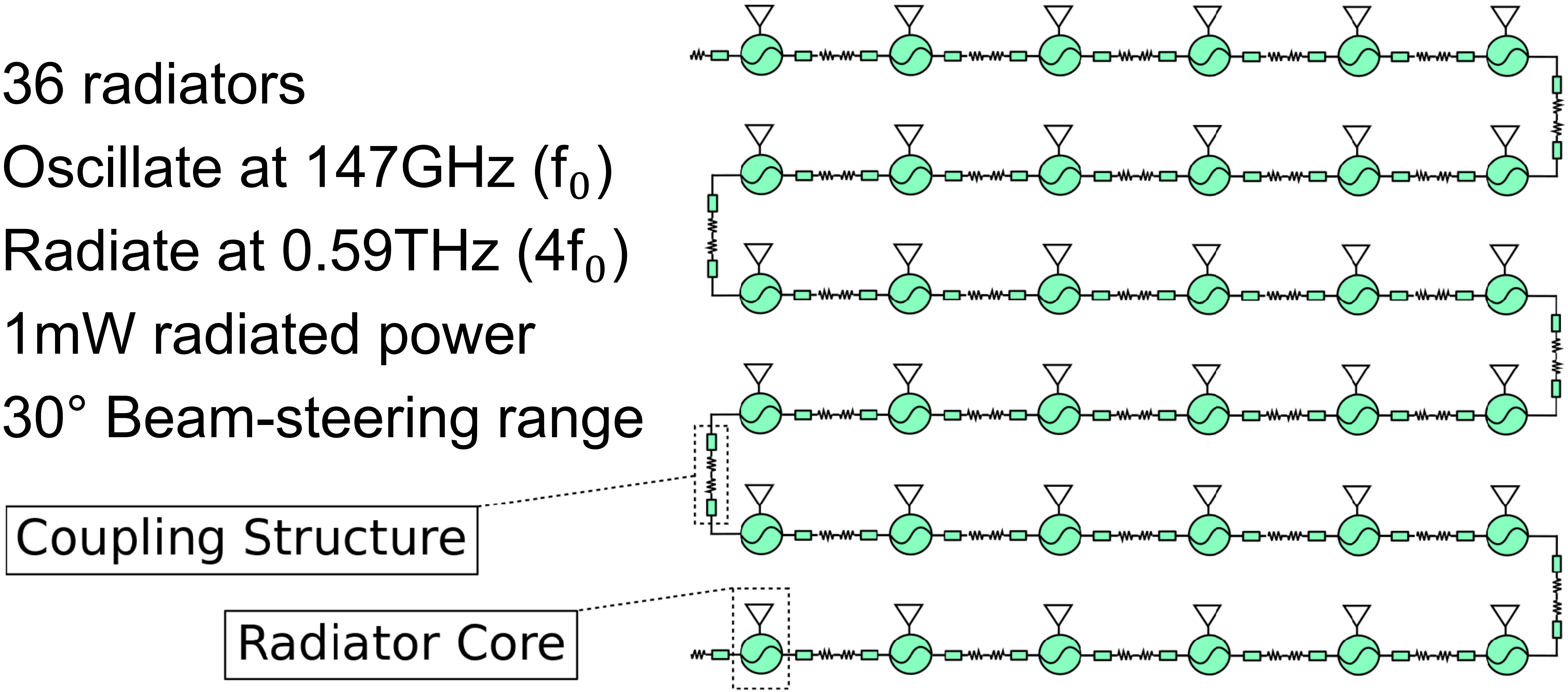
- Measurement
- Conclusion

Coherent Radiator Array in 40nm CMOS

- 36 radiators
- Oscillate at 147GHz (f_0)
- Radiate at 0.59THz ($4f_0$)
- 1mW radiated power
- 30° Beam-steering range



Outline

- Background and Challenge
- Coherent Radiator Array Design
  - -Array Architecture
  - -Oscillator Core
  - -Coupling Structure
  - -Antenna
- Measurement
- Conclusion

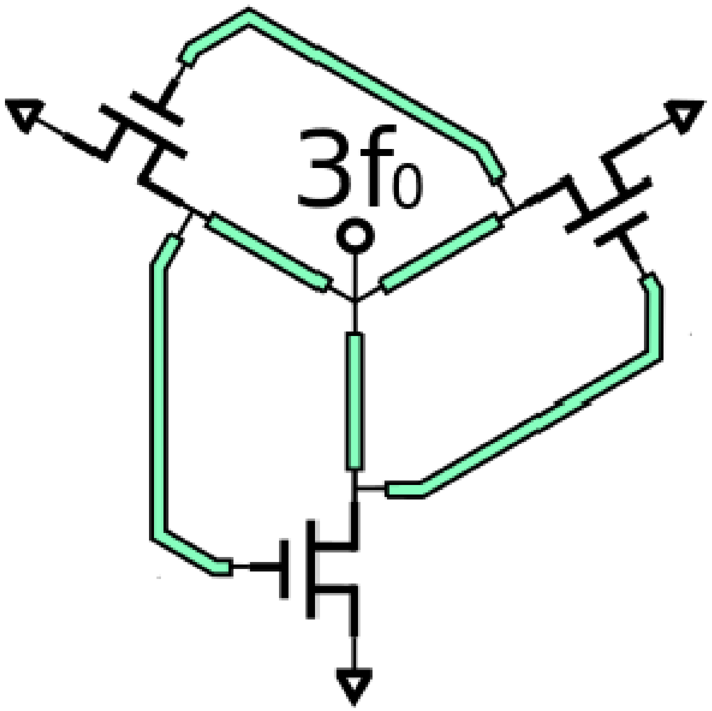
Requirement of Oscillator Core

- Compact layout (radiator pitch $\leq$100μm)
- Symmetric layout, easy to couple a large number of oscillators
- The output power of a single oscillator needs to be good

Comparison of Oscillator Topology

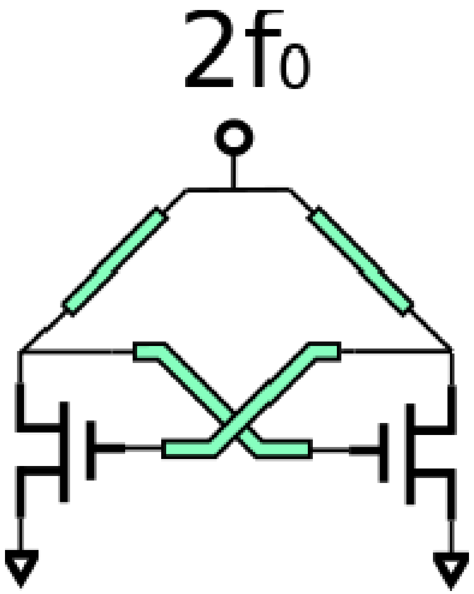
- Triple-push oscillator:

  -Asymmetric



- Push-push oscillator:

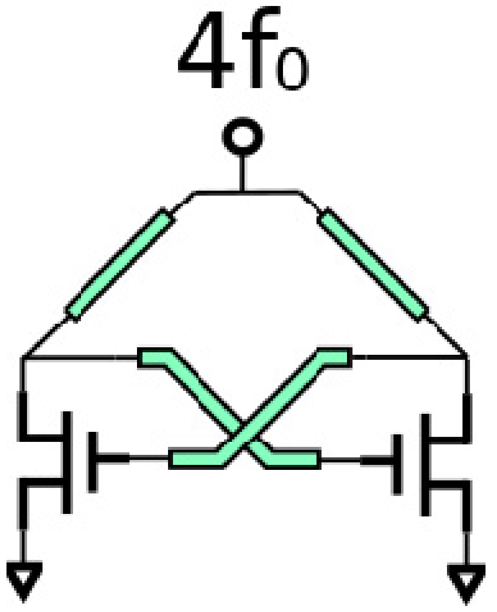
  -Low output frequency



Comparison of Oscillator Topology

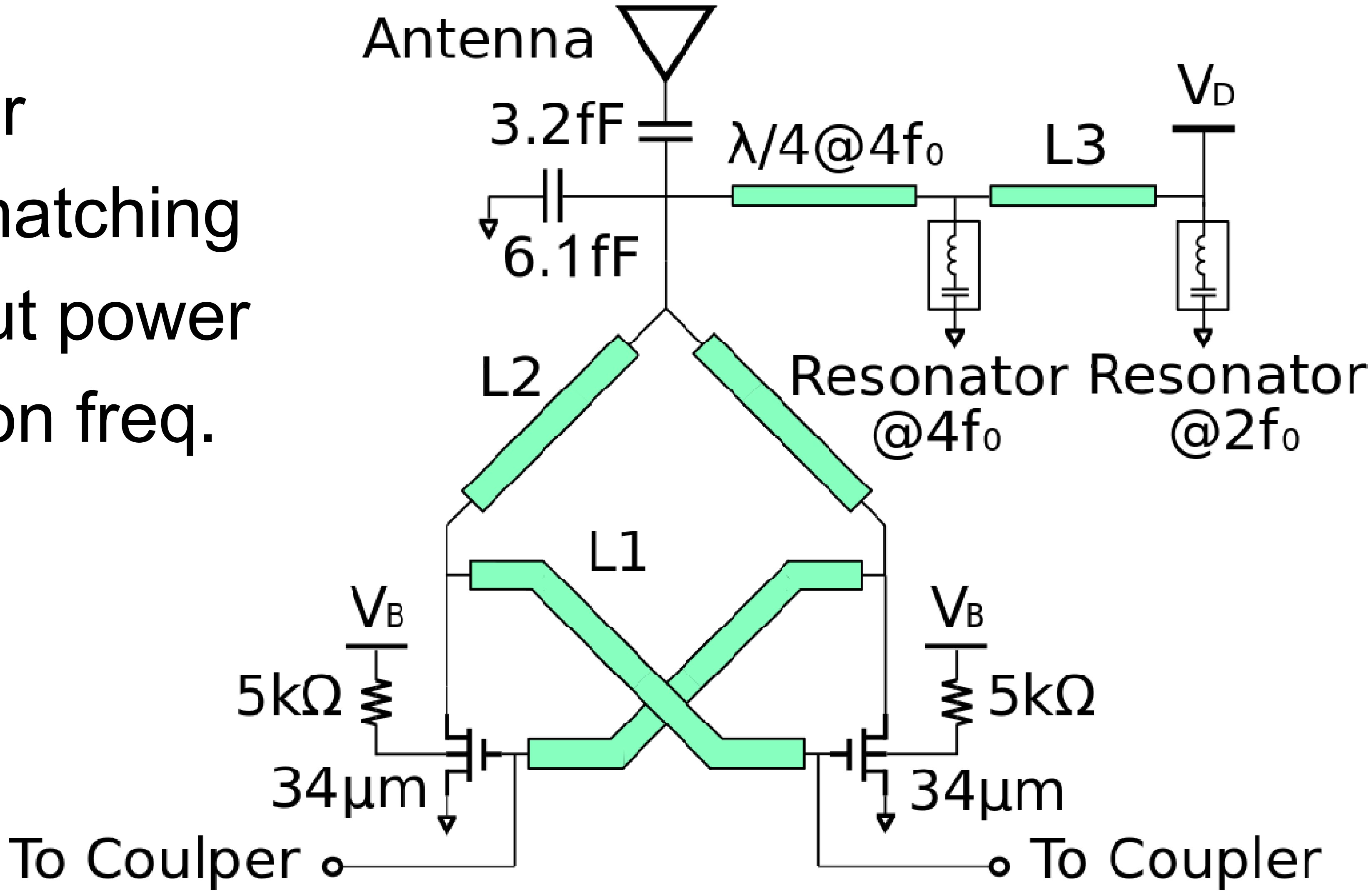
- Push-push oscillator with 4th harmonic extraction:
  - Compact and symmetric layout
  - High output frequency

- Design techniques are needed to increase the 4th harmonic output power.



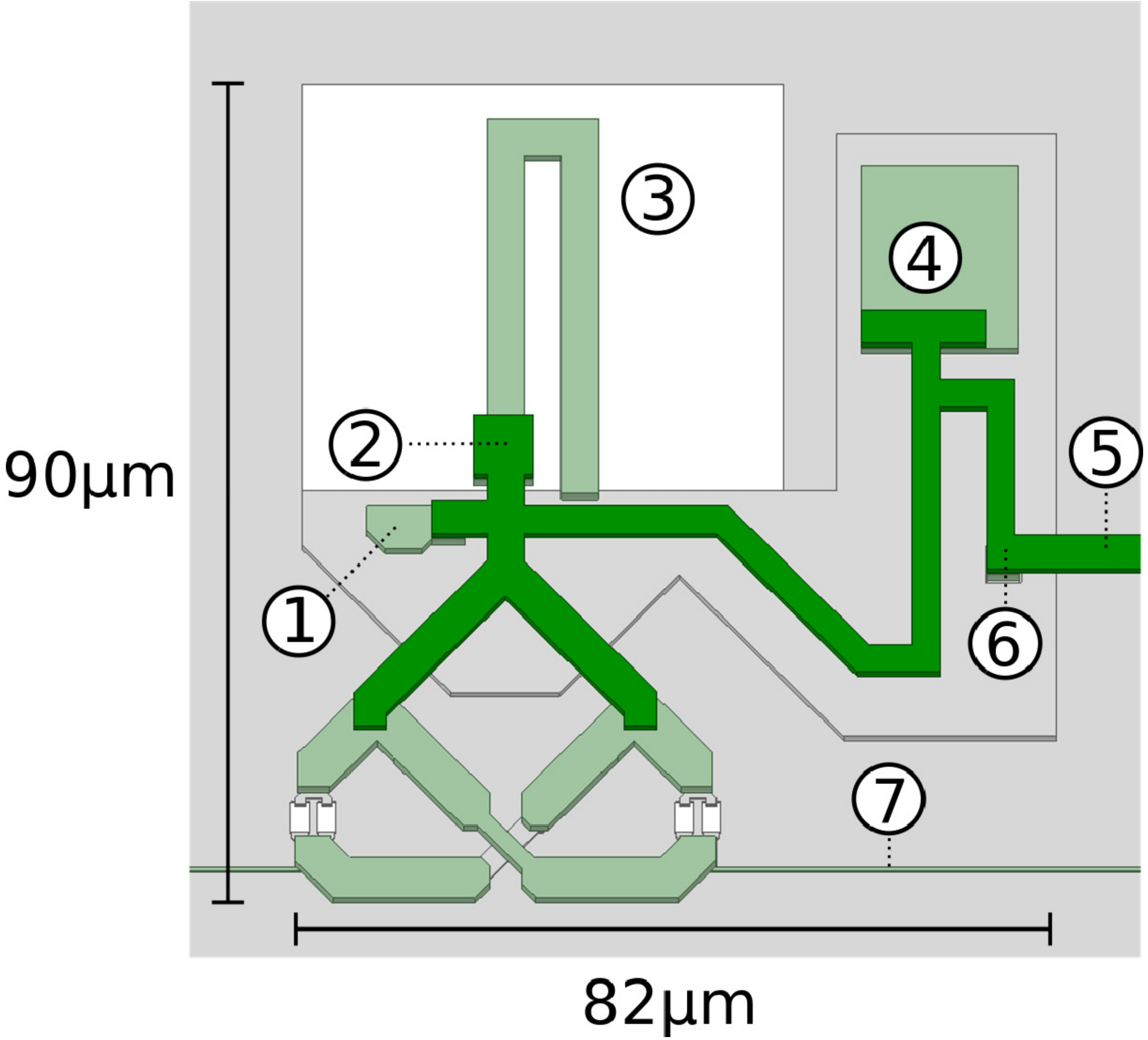
Schematic of Radiator Core

- Cross-coupled pair
- L-type capacitor matching
- L1, L3 boost output power
- V_B adjust oscillation freq.

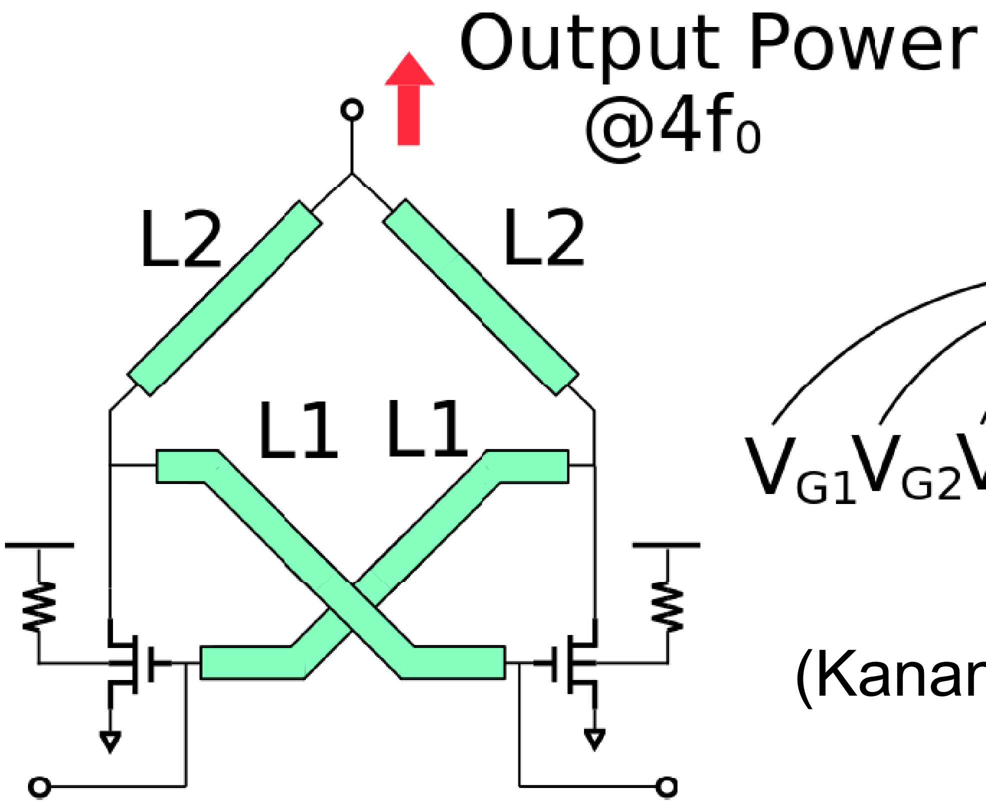


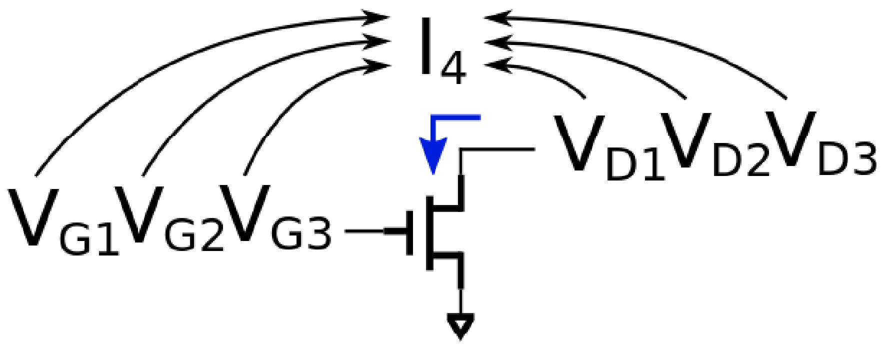
Layout of Radiator Core

1. Parallel capacitor
2. Series capacitor
3. Antenna
4. $4f_0$ resonator
5. DC supply line
6. $2f_0$ resonator
7. Coupling line

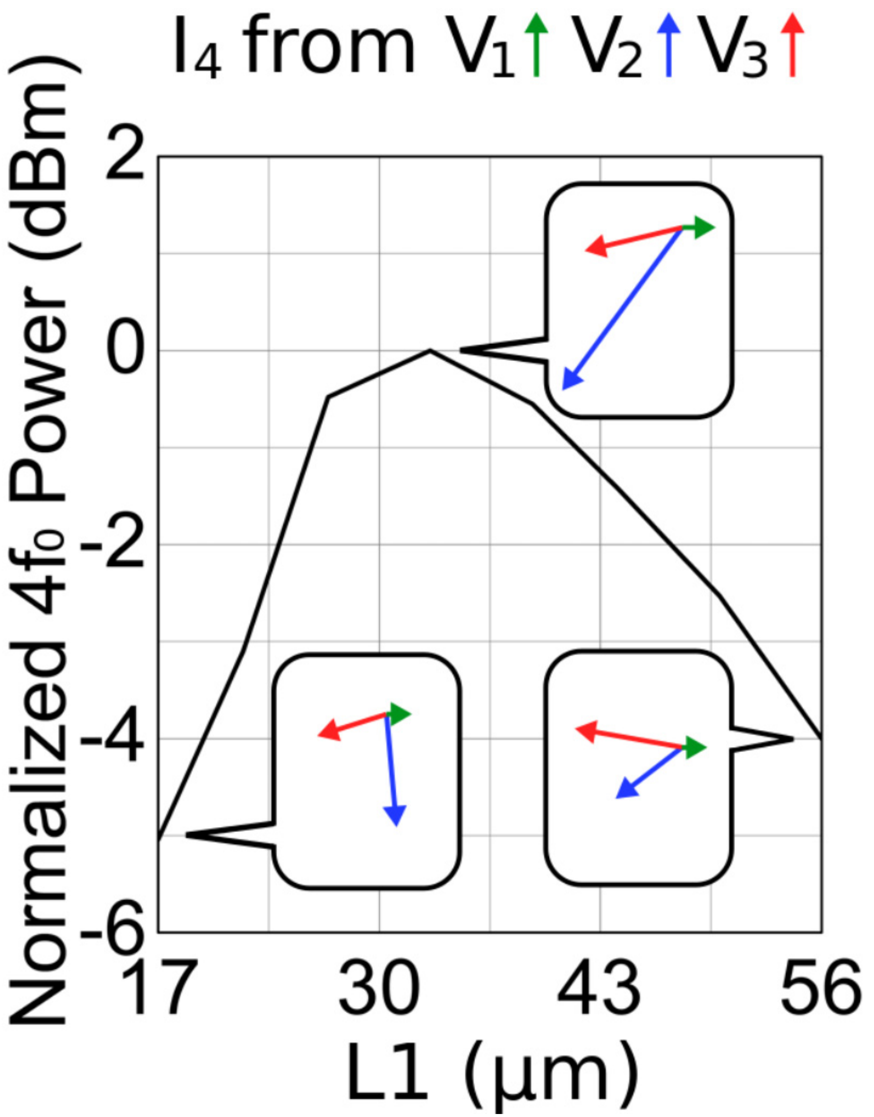


Boost $4f_0$ Power



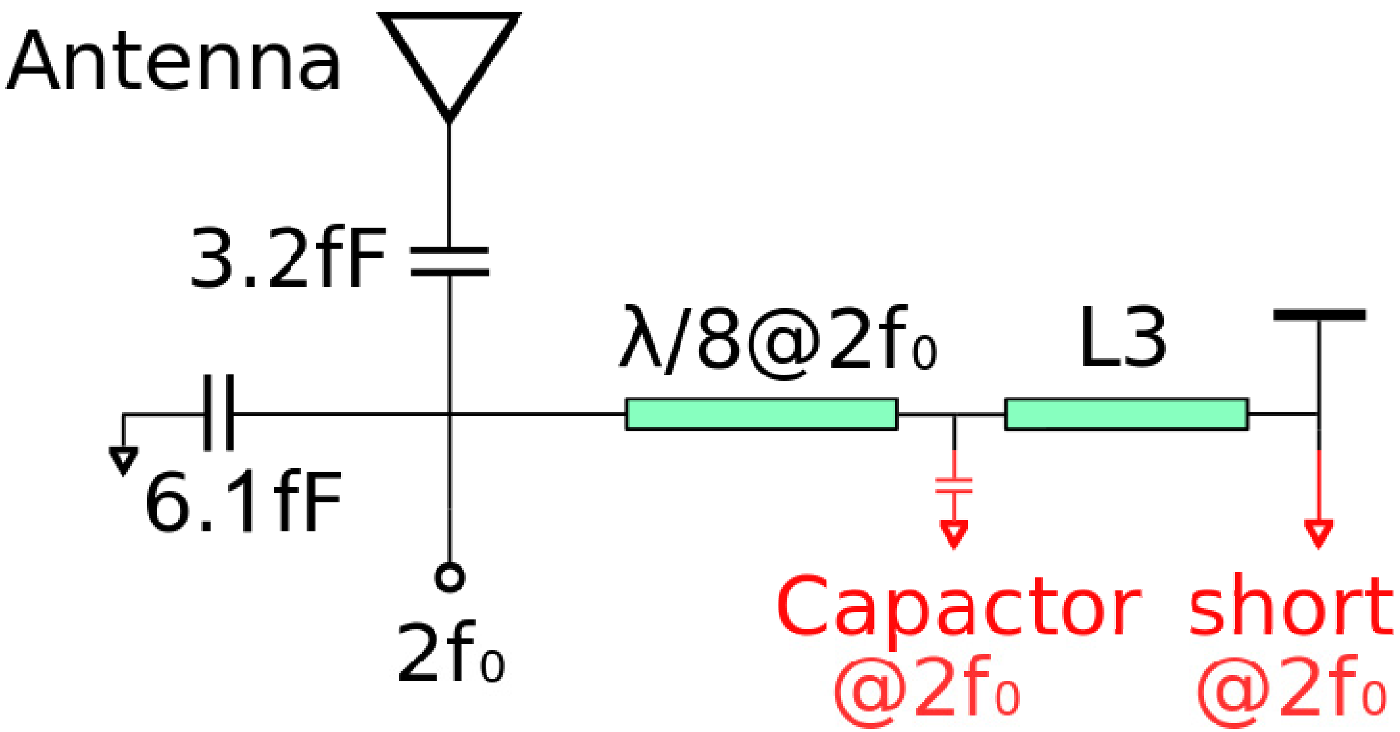


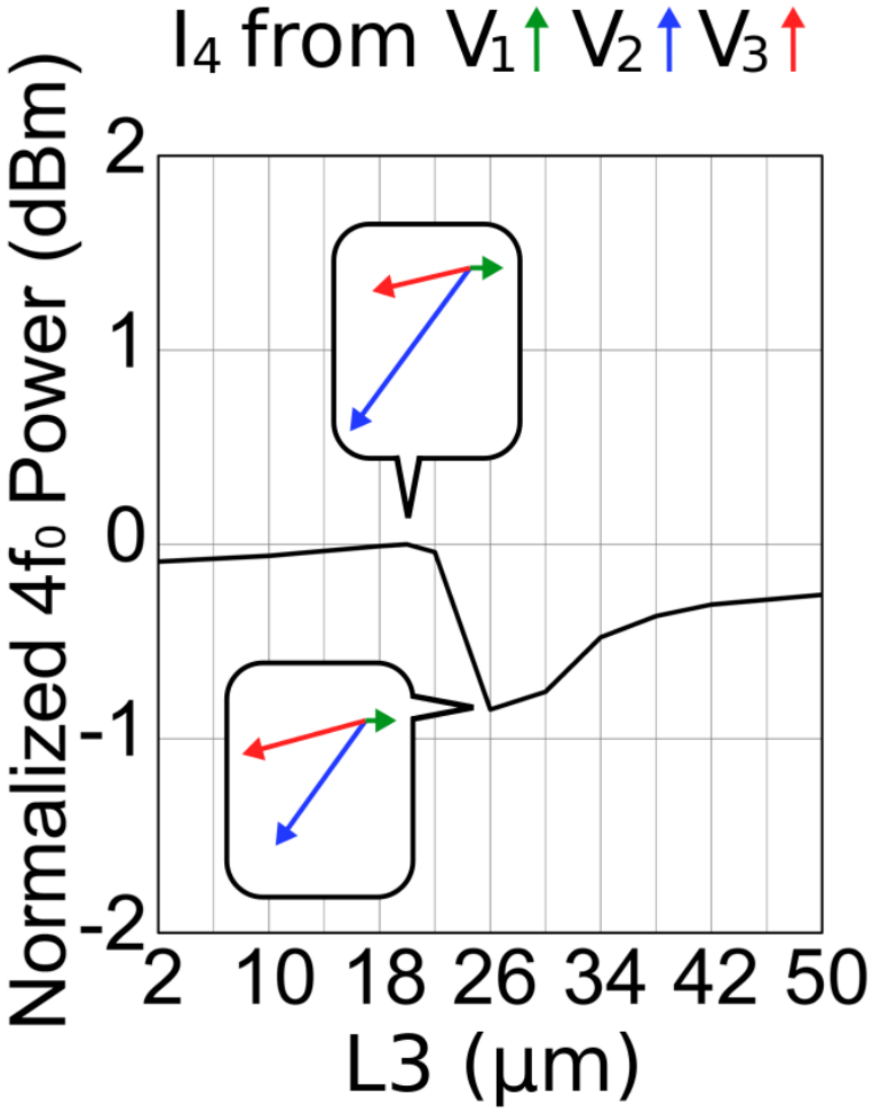
(Kananizadeh, TMTT, 2017)



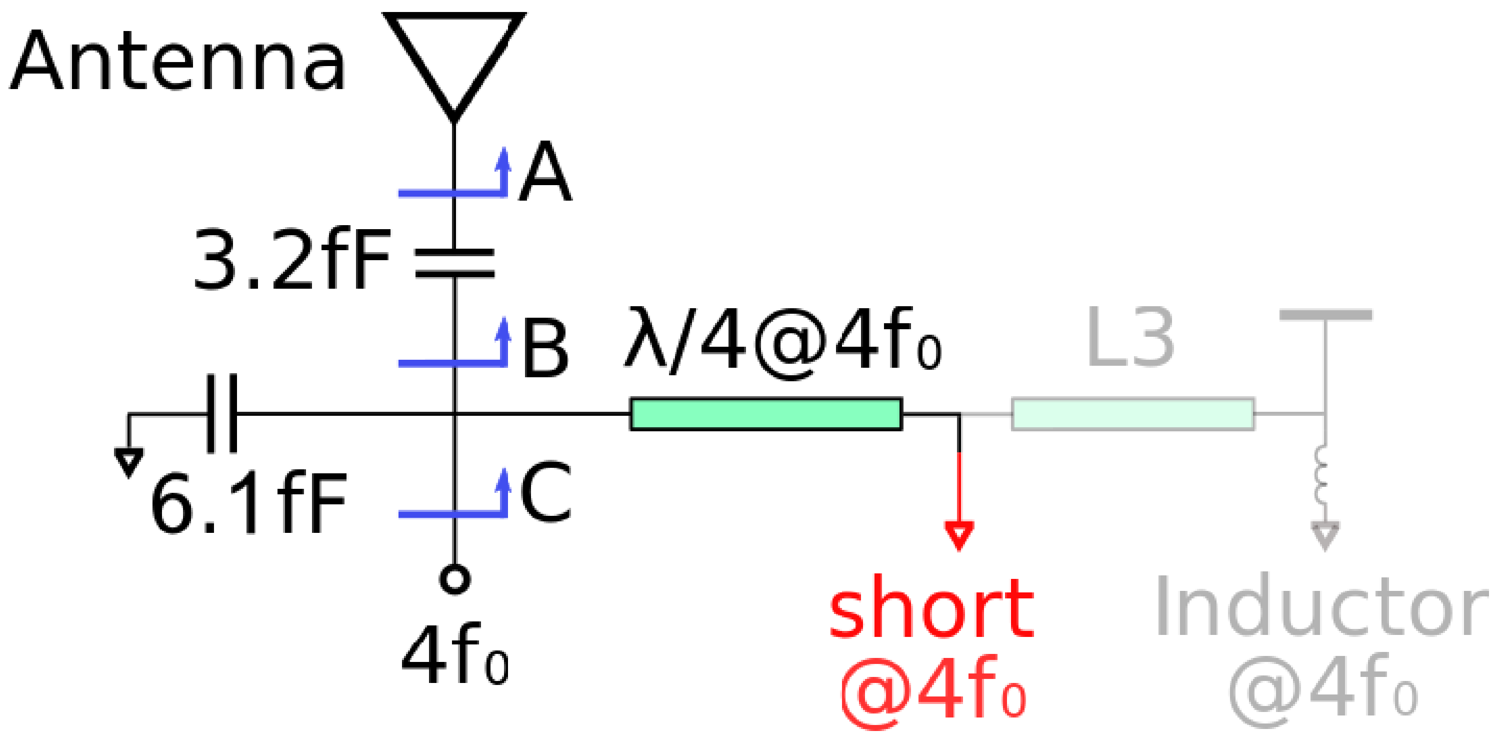
- When L1 is swept, L2 is also changed to fix oscillation freq.

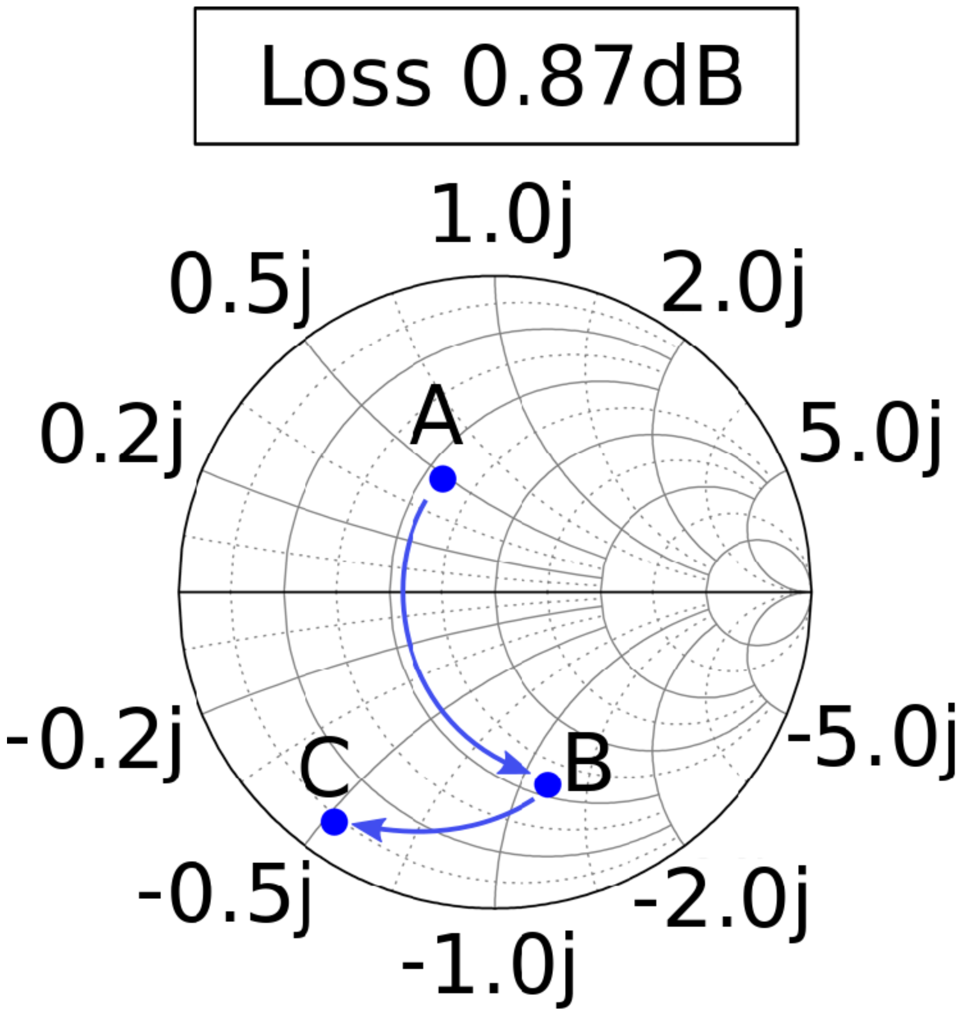
Boost $4f_0$ Power





Impedance Matching at $4f_0$





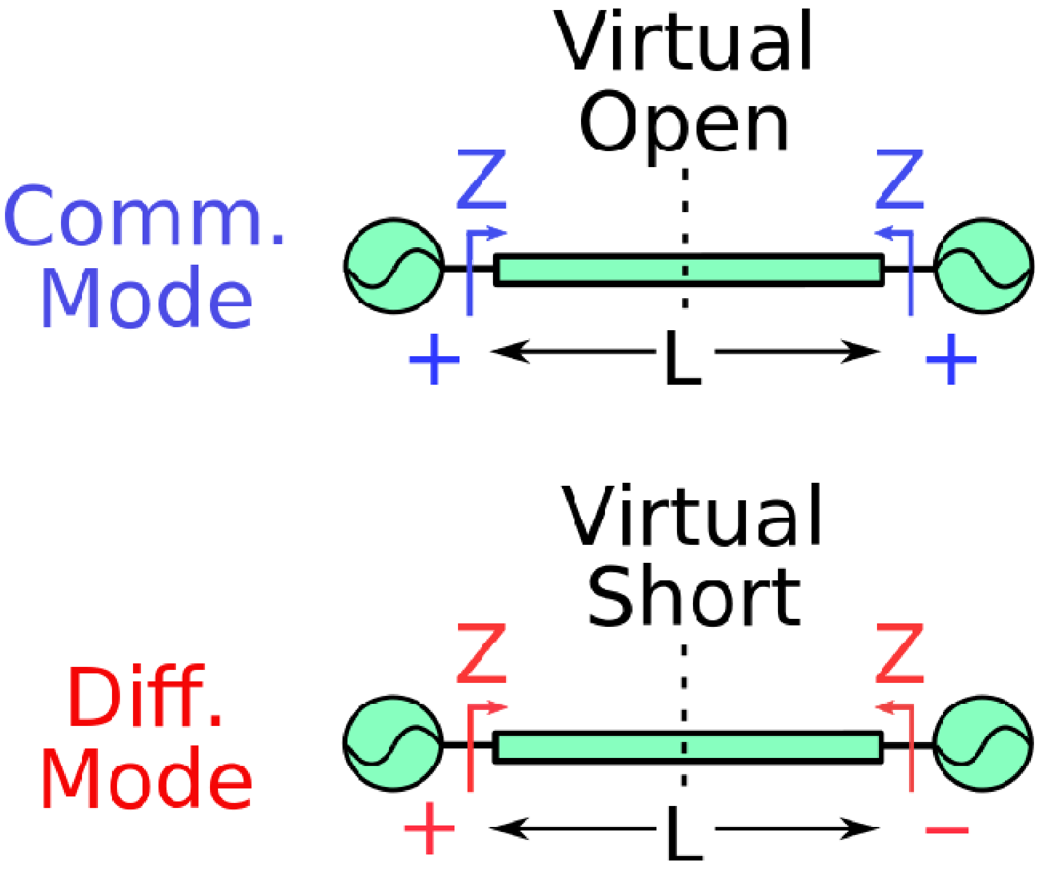
Outline

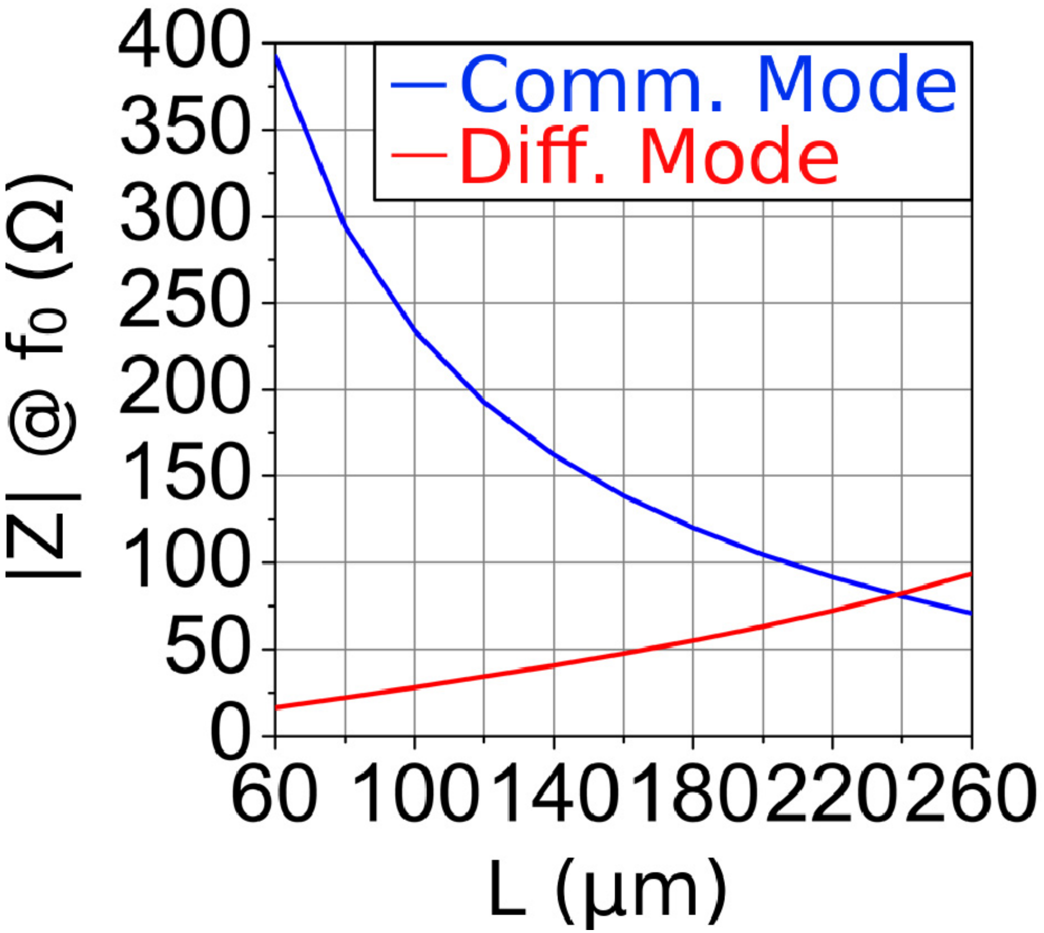
- Background and Challenge
- Coherent Radiator Array Design
  - -Array Architecture
  - -Oscillator Core
  - -Coupling Structure
  - -Antenna
- Measurement
- Conclusion

Requirement of Coupling Structure

- The coupling structure needs to be short (radiator pitch $\leq$100μm)
- Low impact on the performance of core circuit
- Scalable to large number

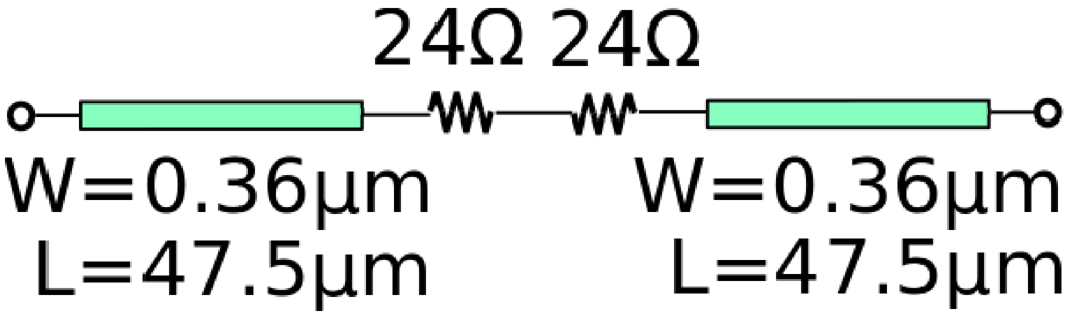
Comparison of Coupling Method

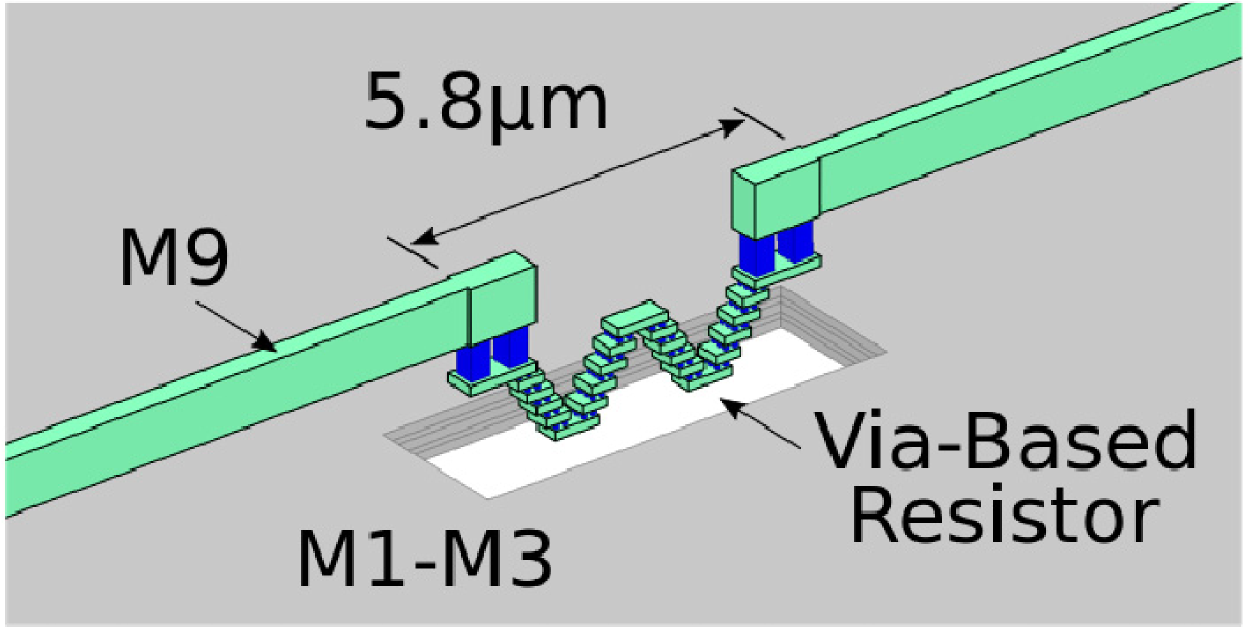




- Comm. mode has lower impact for short oscillator distance

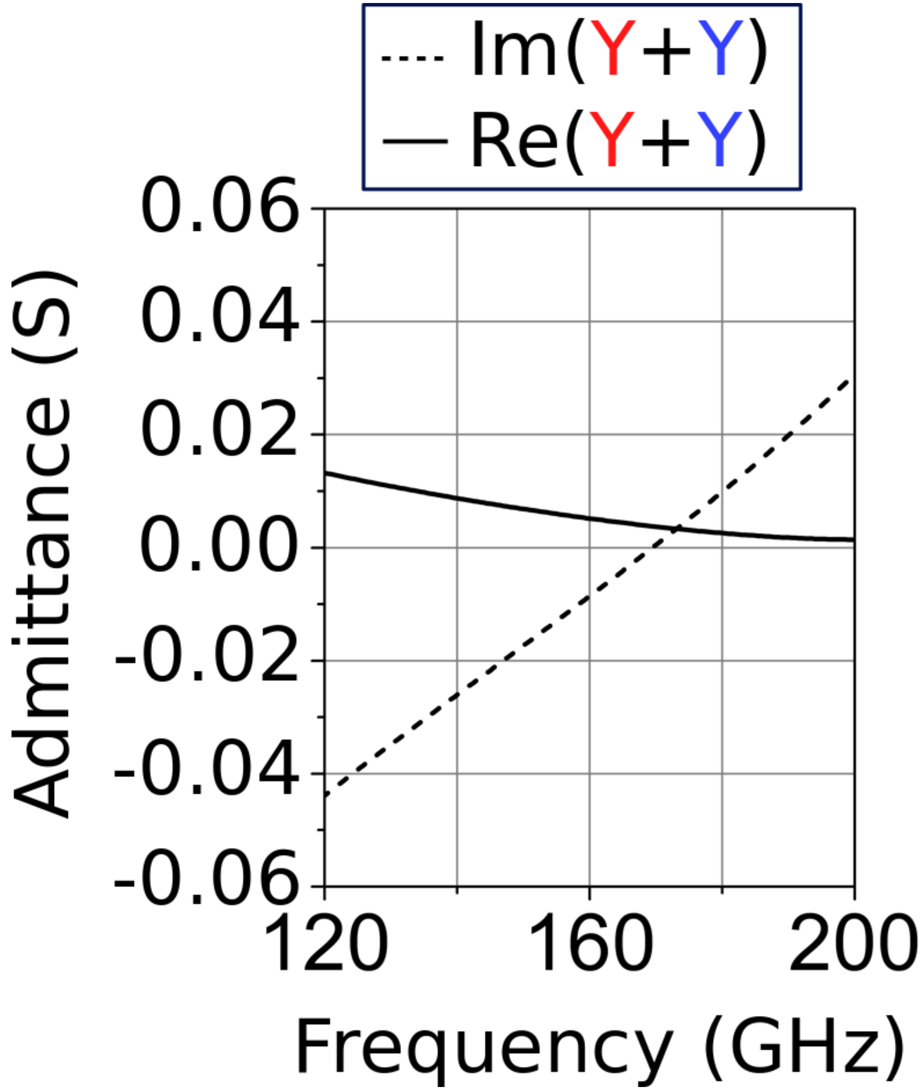
Coupling Structure





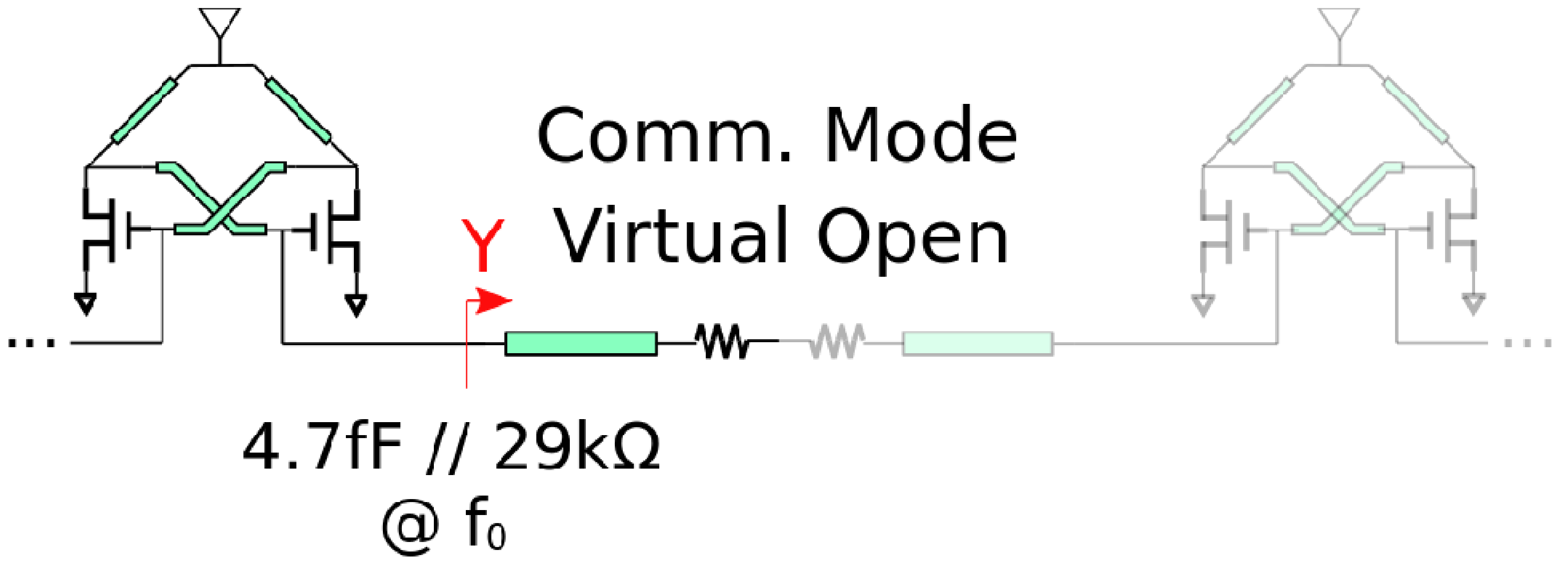
- Narrow microstrip line for low capacitance
- Via resistor with 0.5fF parasitic capacitance
- 120 vias to reduce process variation

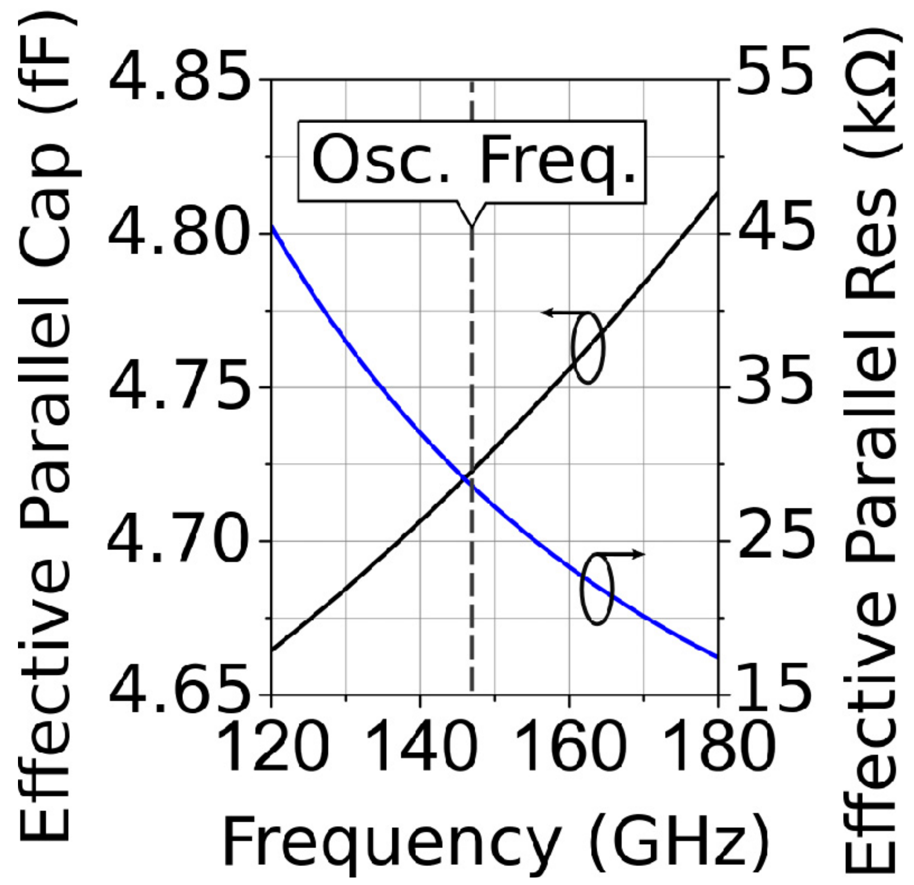
Suppression of the Unwanted Diff. Mode



- When Im(Y+Y)=0, Re(Y+Y)>0
- Differential mode is avoided

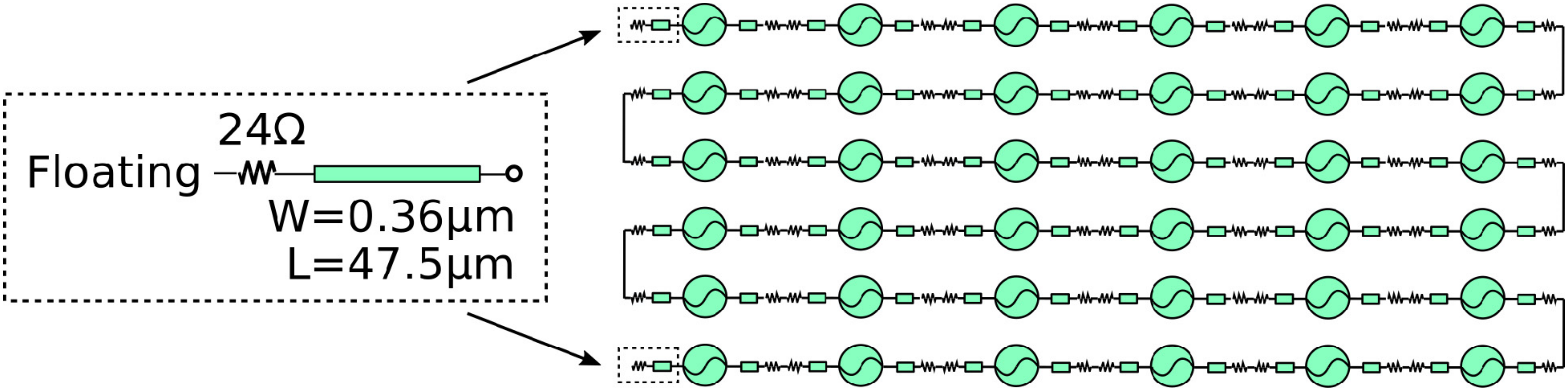
Impact of the Coupling Structure





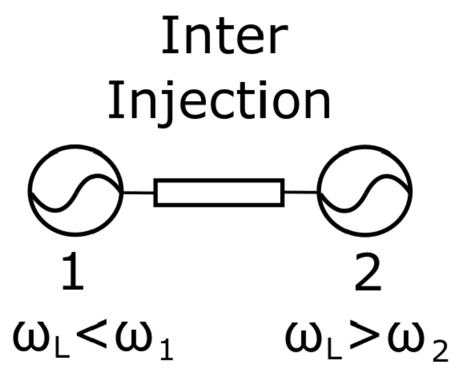
- 6.7% effective capacitance in the Oscillator tank
- 0.1dB reduction of the output power

Dummy Coupling Structure

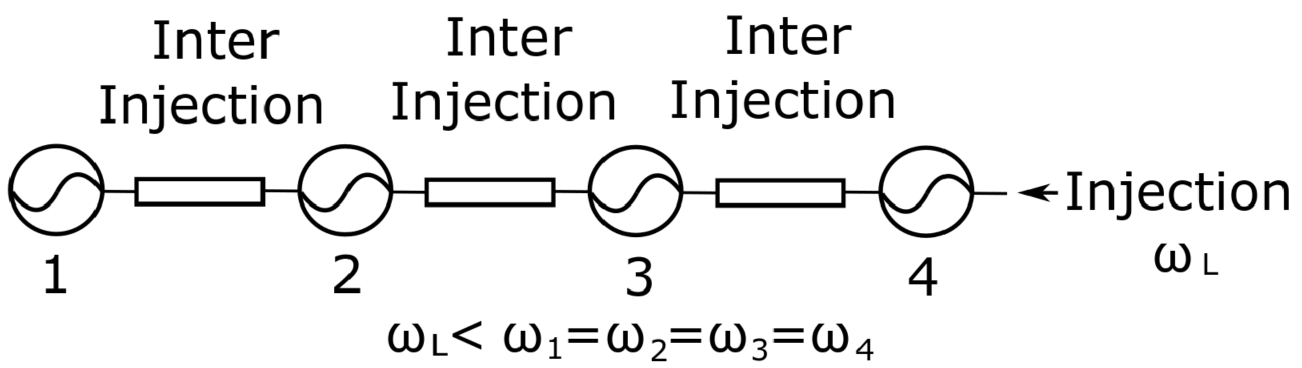


- The floating end perfectly duplicate the virtual open
- No imbalance is caused

Beam Steering Capability



$\theta_1 \neq \theta_2$

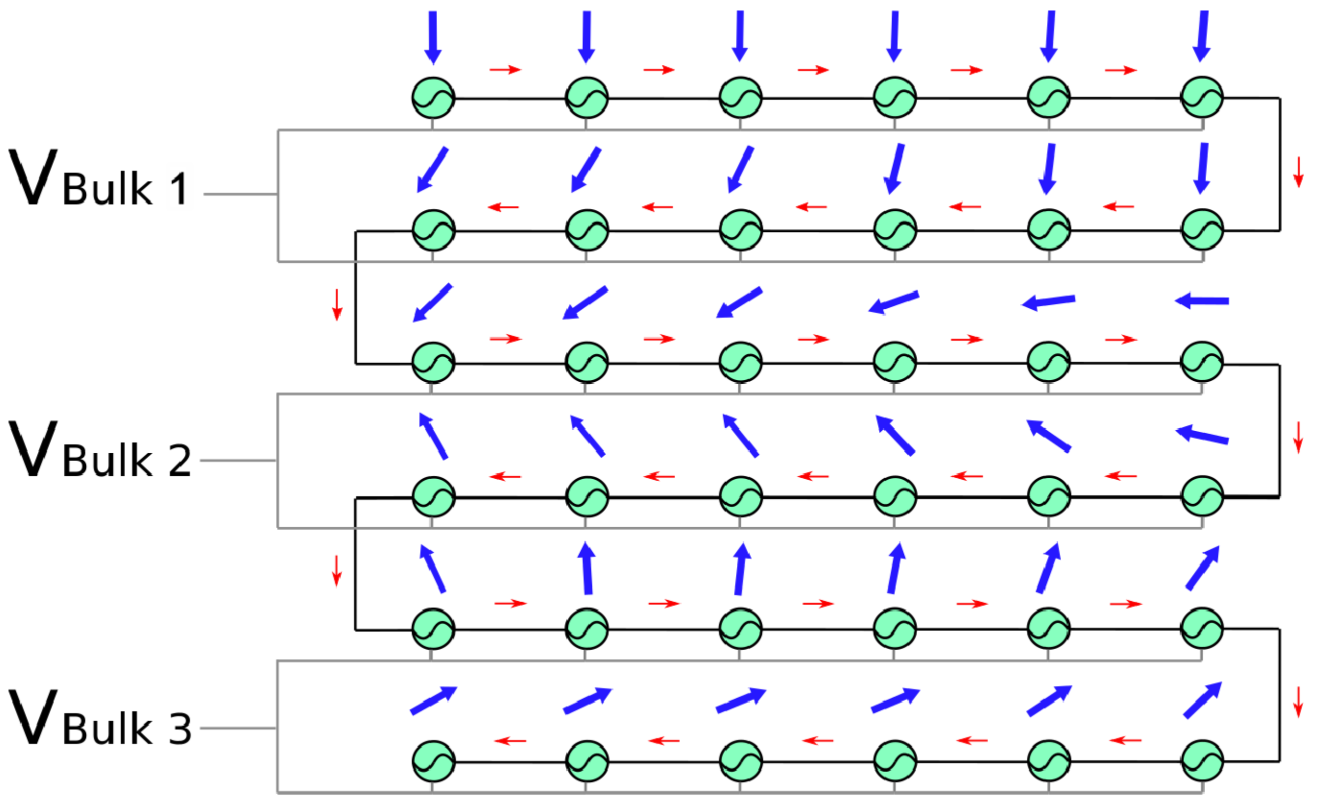


$\theta_1 \neq \theta_2 \neq \theta_3 \neq \theta_4$

For an oscillator chain including multiple oscillators with the same free-run oscillation frequency, when an injection at a different frequency is given from the edge, a gradual phase change is caused in the oscillator chain.

Beam Steering Capability

(Liao, TMTT, 1993)



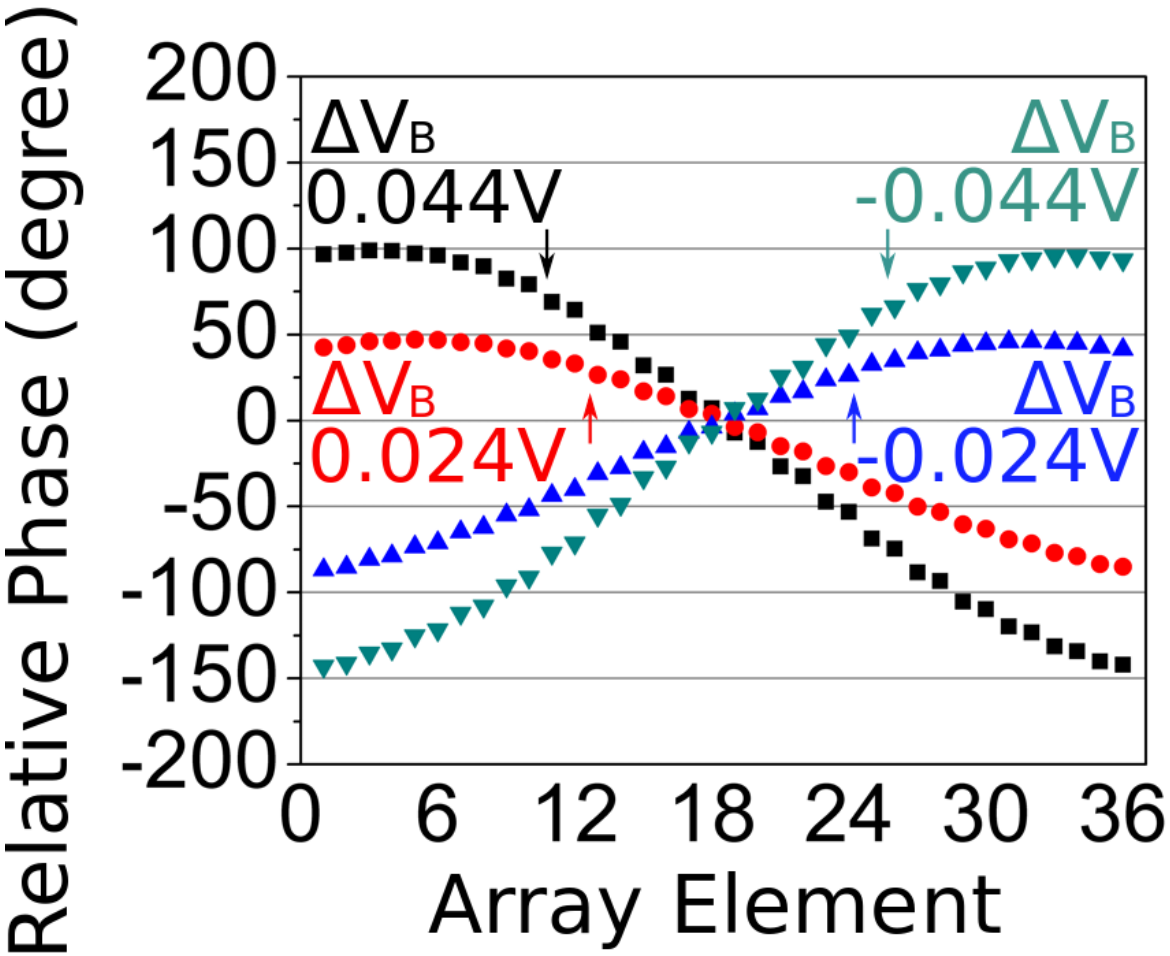
Bulk Voltage Difference

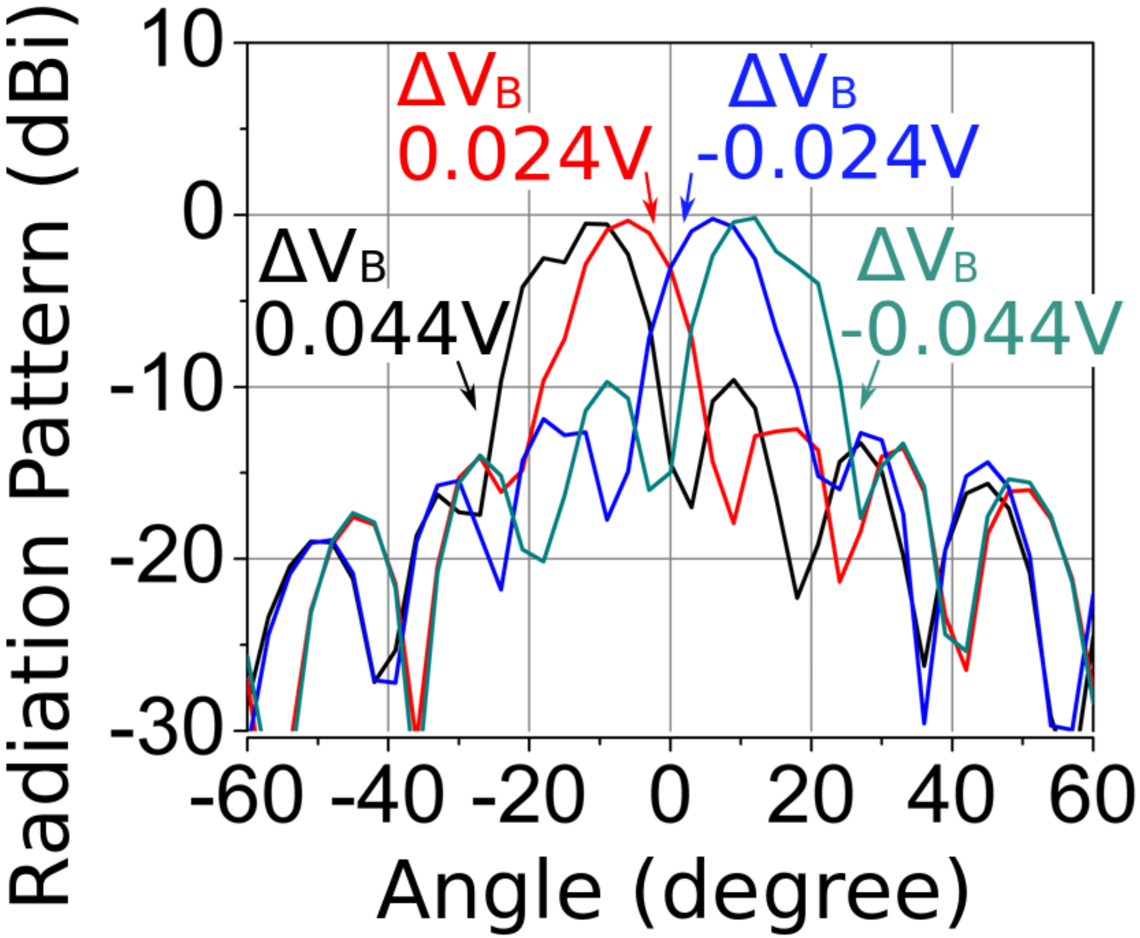
No Coupling → Different Frequency

Coupling → Gradual Phase Progress

This work

Simulation of Beam Steering





Outline

- Background and Challenge
- Coherent Radiator Array Design

  -Array Architecture

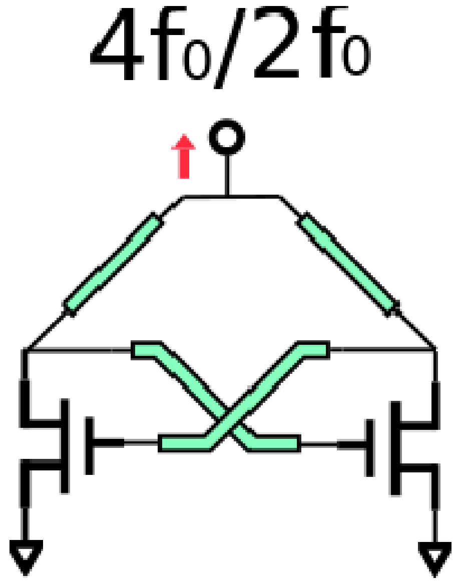
  -Oscillator Core

  -Coupling Structure

  -Antenna
- Measurement
- Conclusion

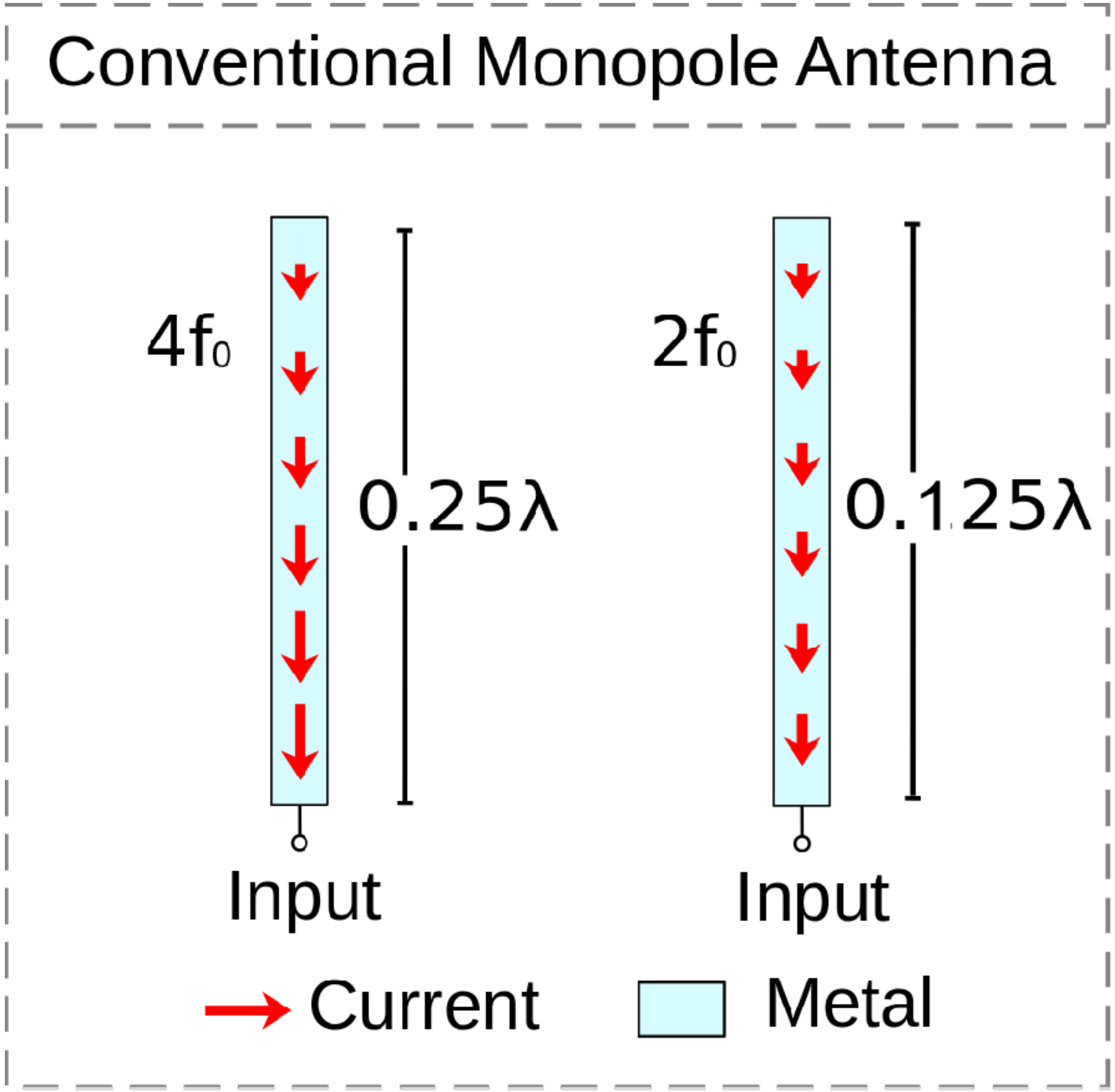
Requirement and Comparison of Antenna

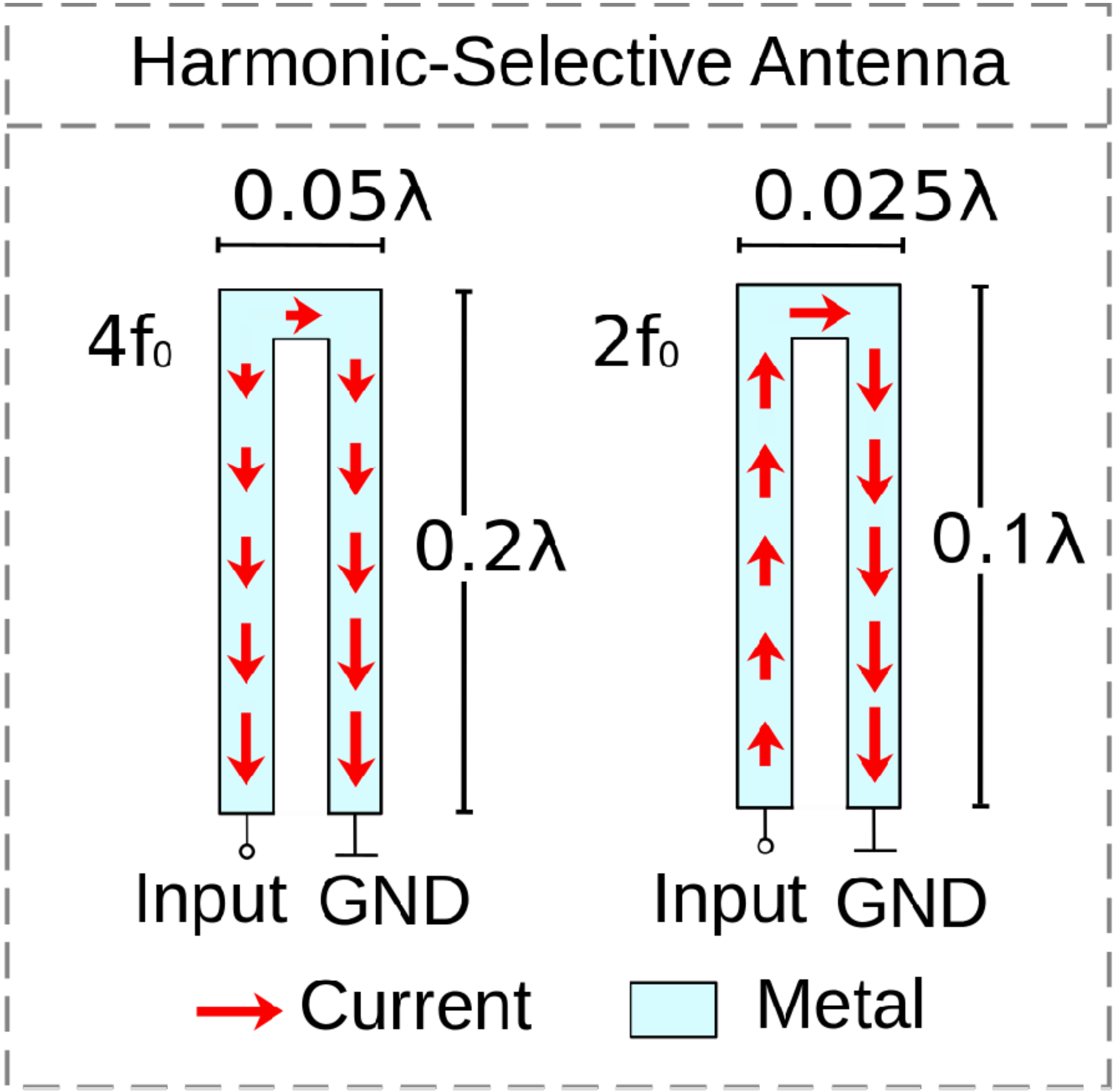
- Compact size (radiator pitch ≤100μm)
- Suppress radiation of 2nd harmonic



	Dipole/Slot	Monopole	Harmonic-Selective Antenna
Antenna Dimension	λ/2	λ/4	λ/4
Leakage Suppression	No	No	Yes

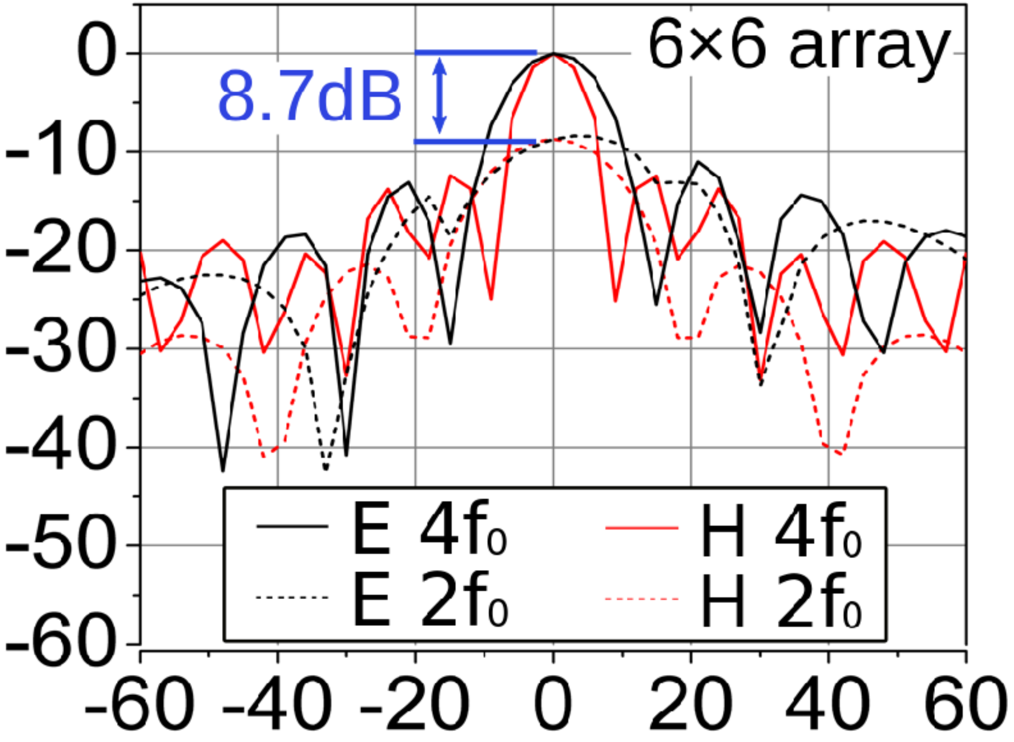
Harmonic Selective Antenna



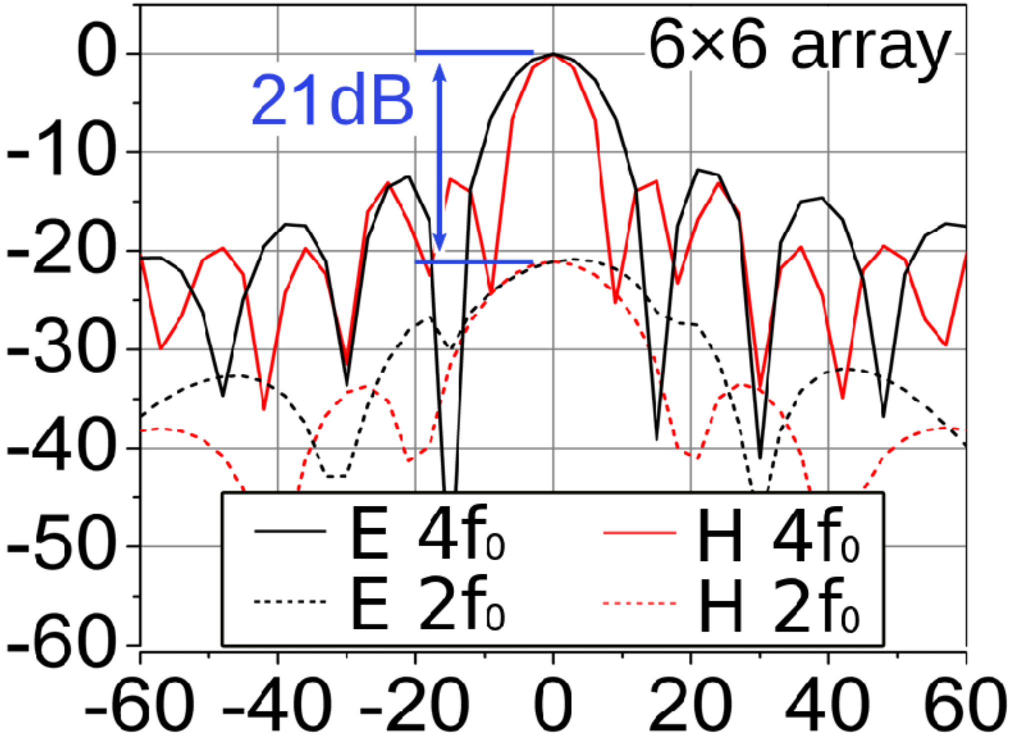


Radiation Pattern Comparison

Conventional Monopole Antenna



Harmonic-Selective Antenna



Outline

- Background and Challenge
- Coherent Radiator Array Design
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  -Oscillator Core
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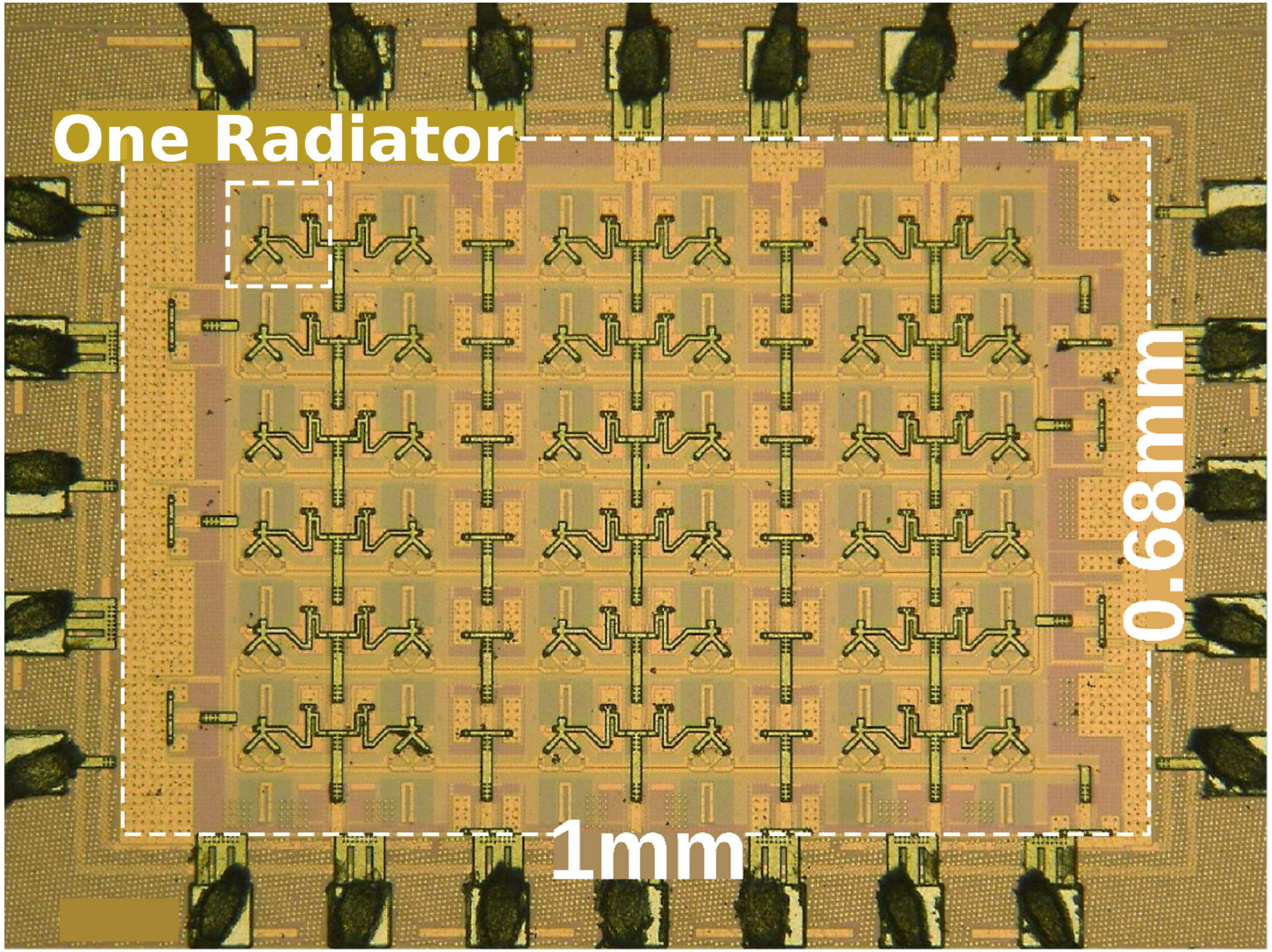
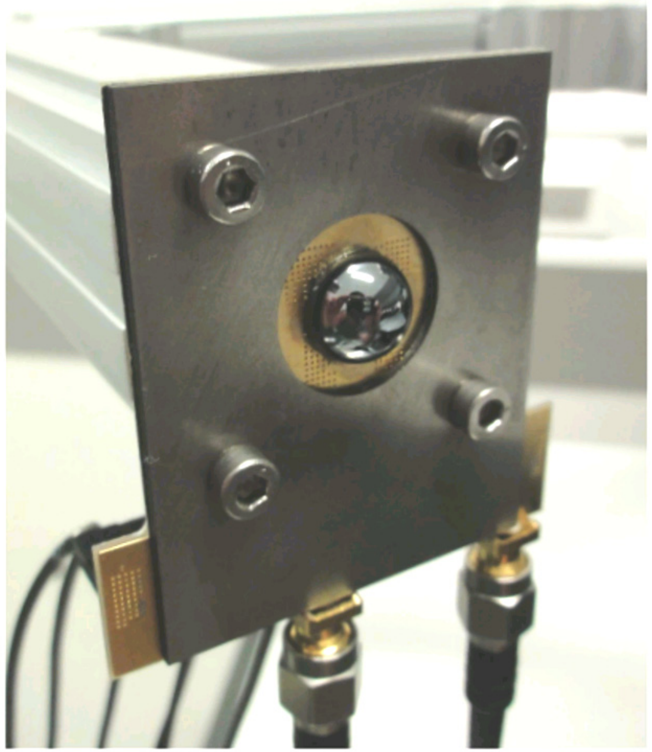
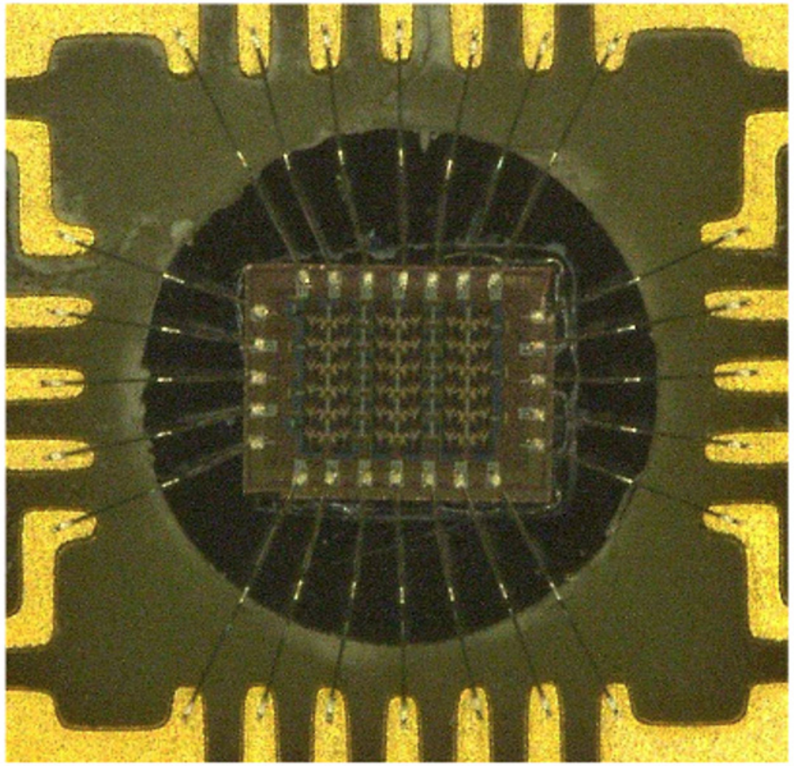
Die Photograph

- 40nm bulk CMOS
- $0.68mm^2$



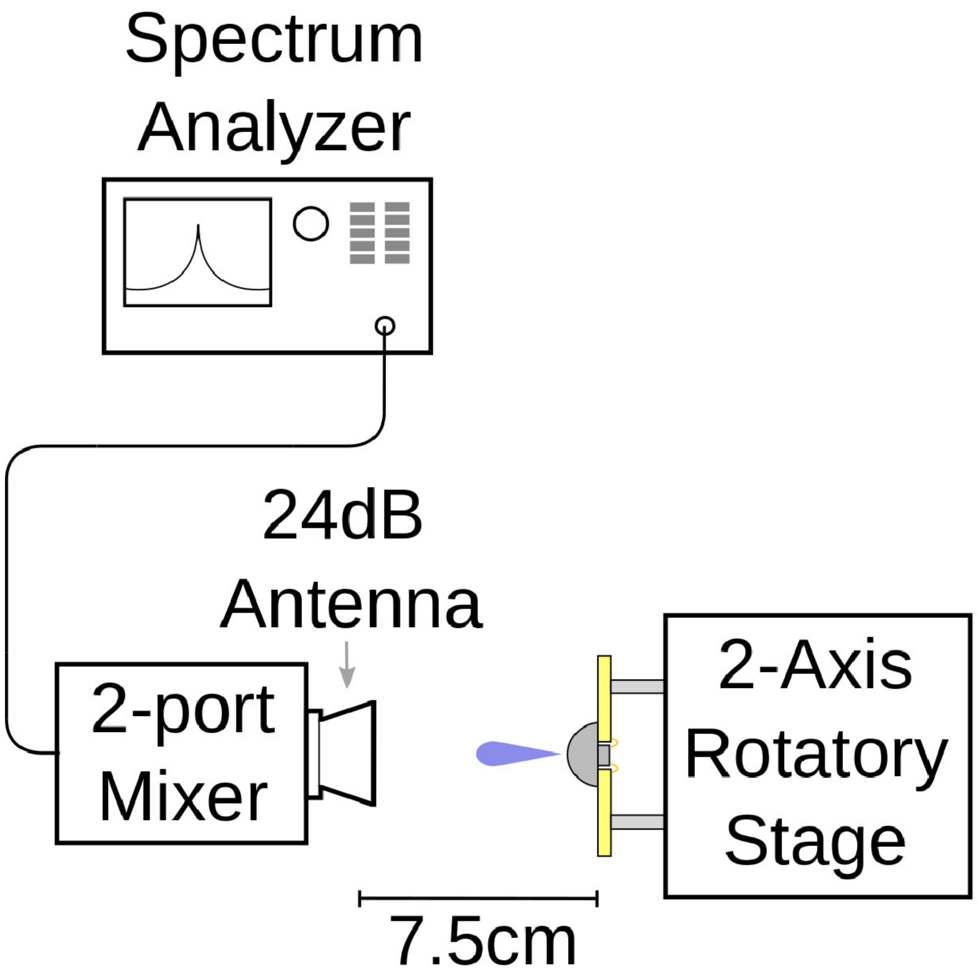
Chip Package for Back-side Radiation

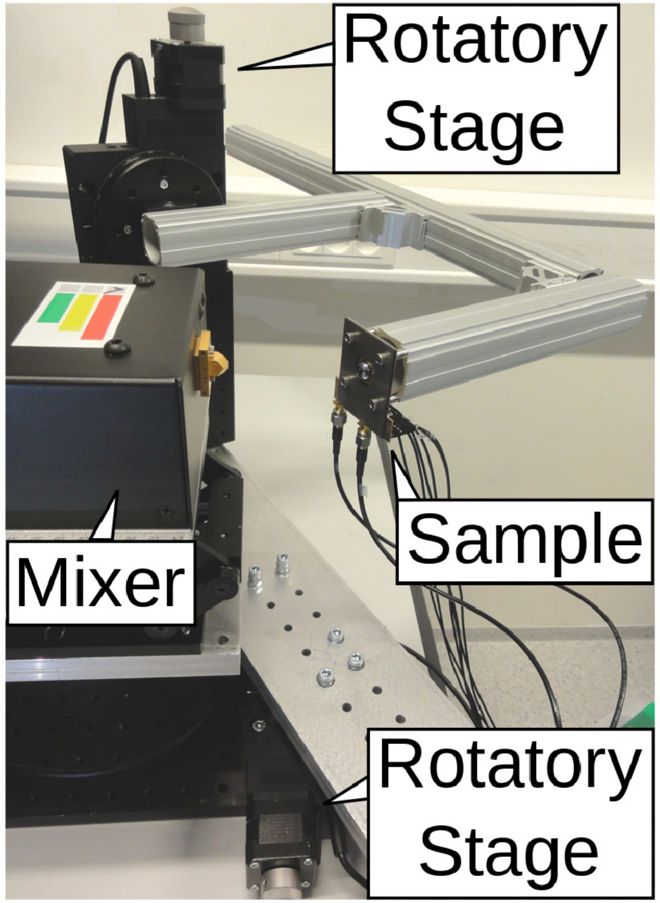




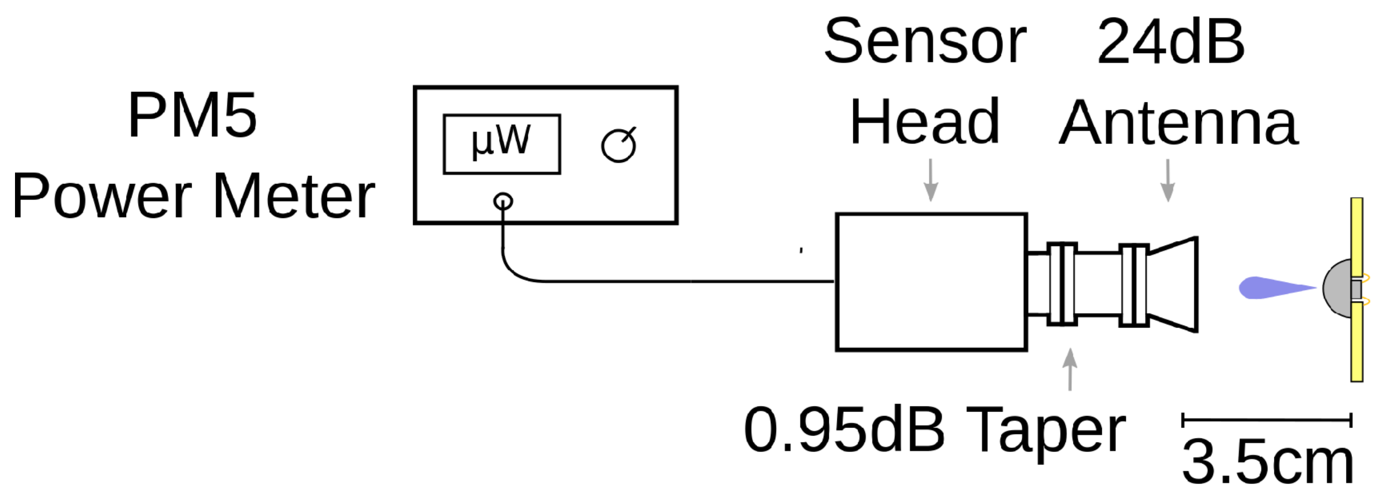
Hemispherical silicon lens with 10mm diameter.

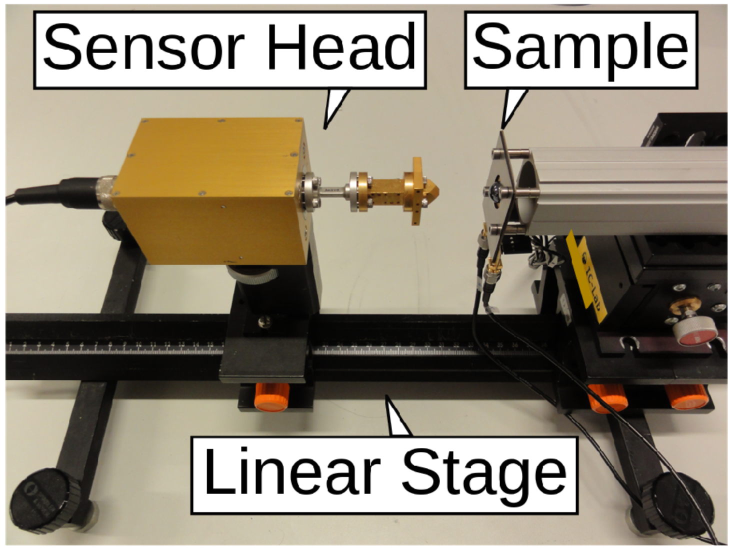
Test Equipment

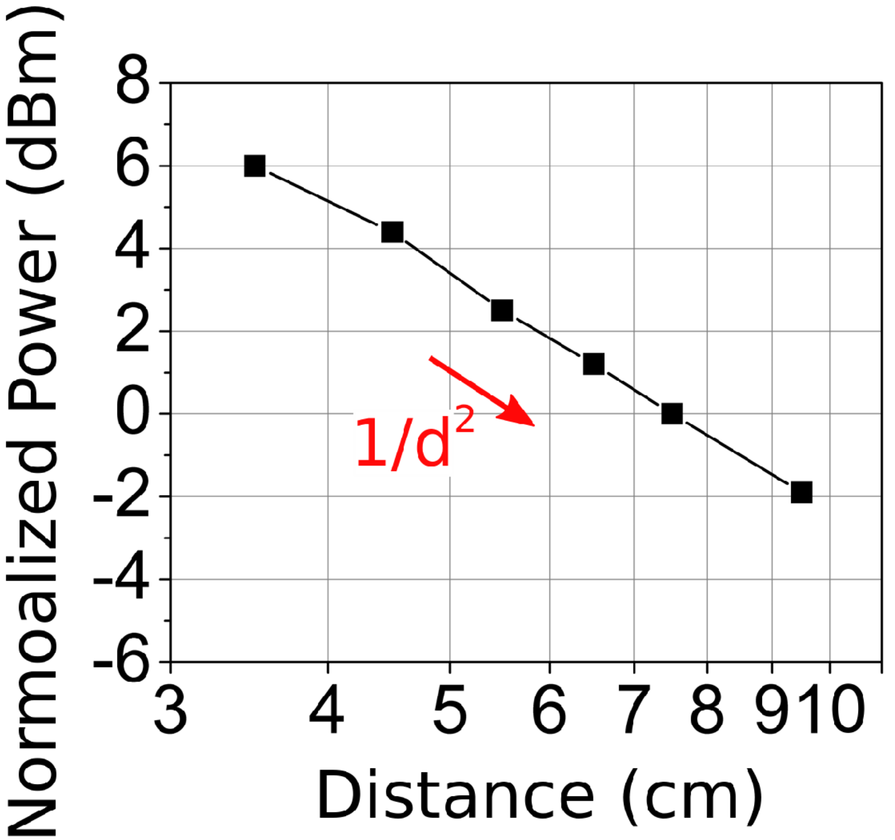




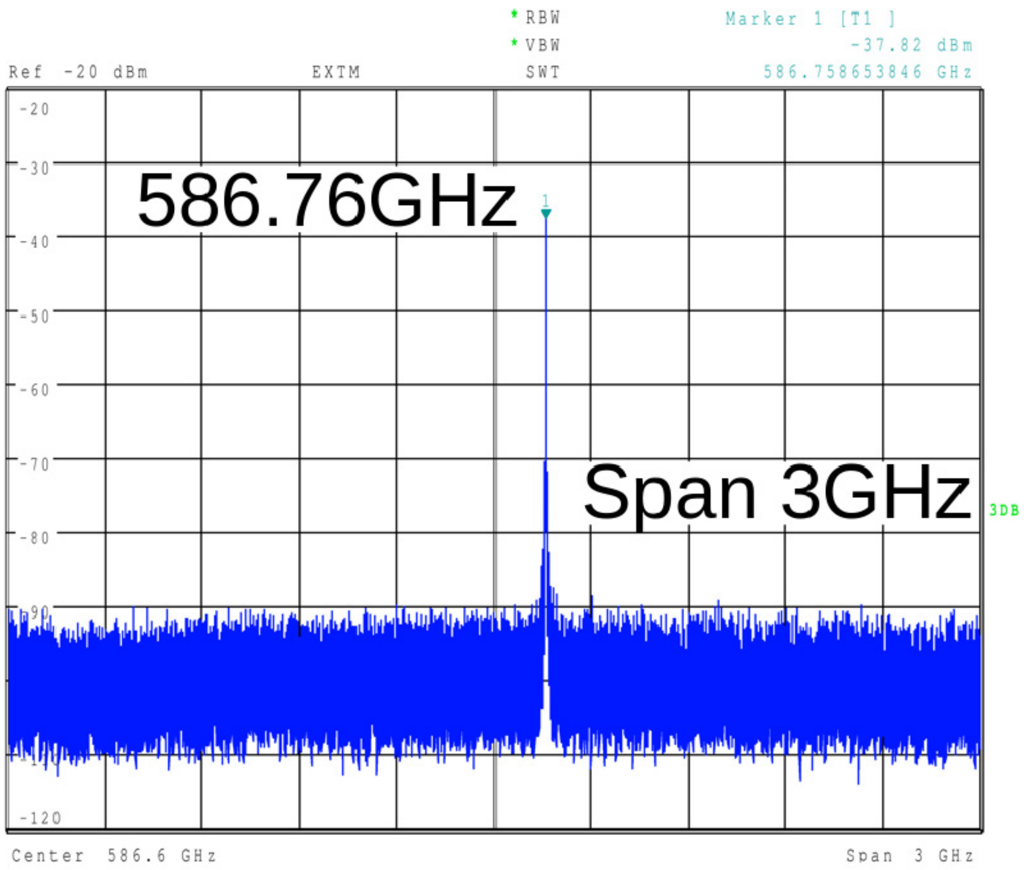
Test Equipment



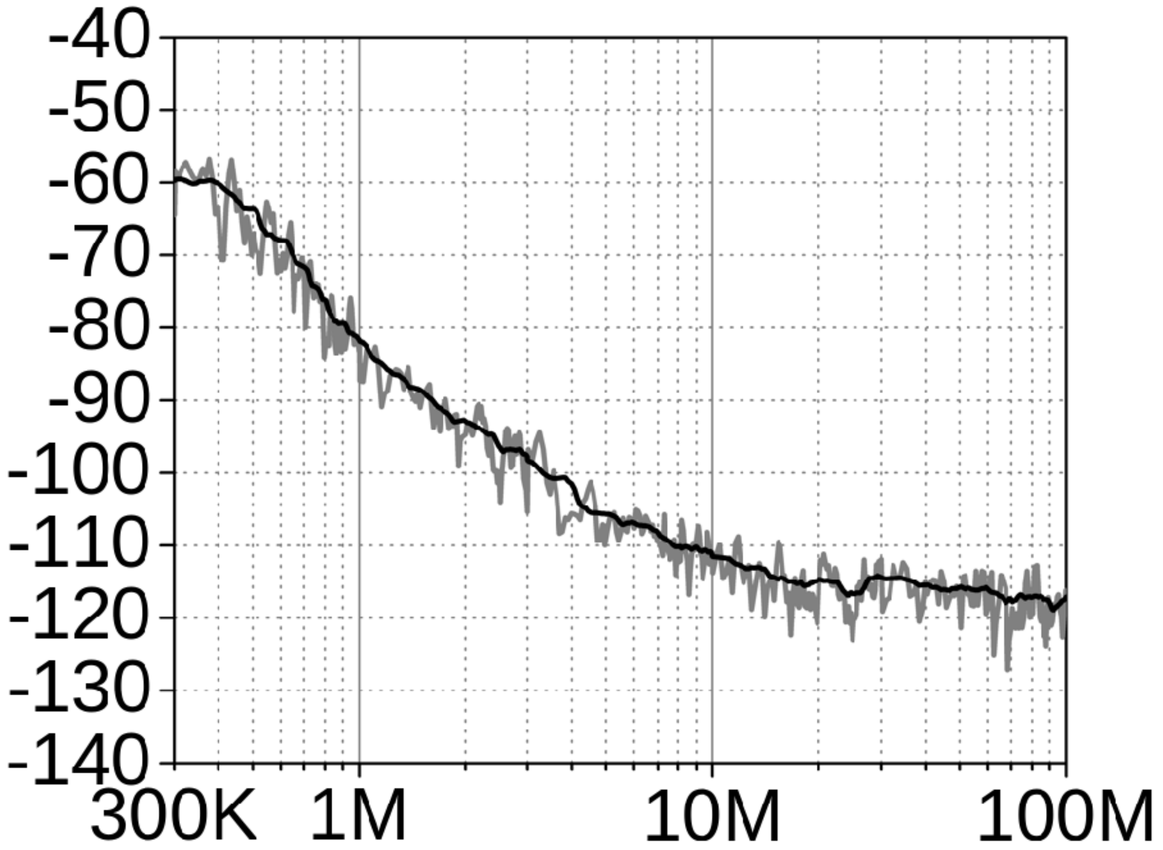




Measured Spectrum and Phase Noise

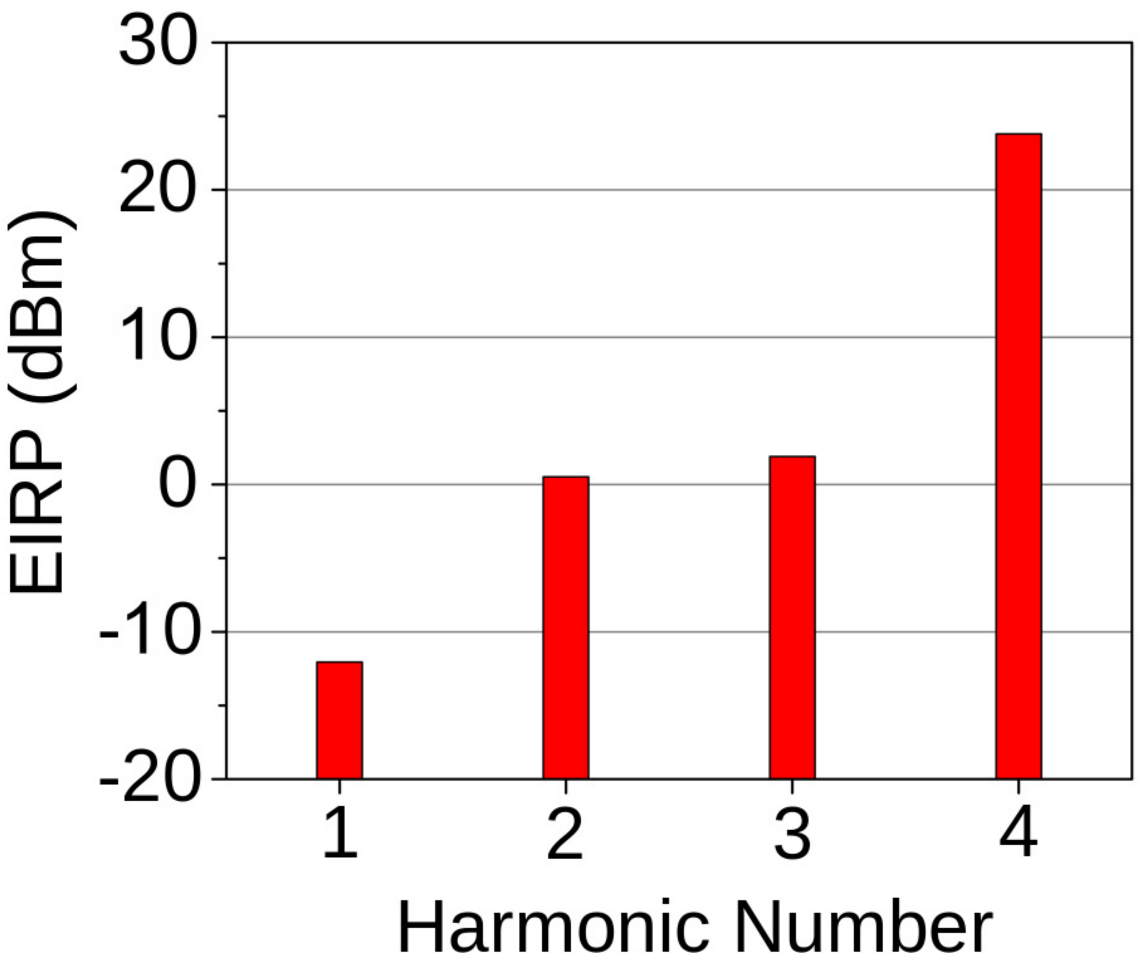


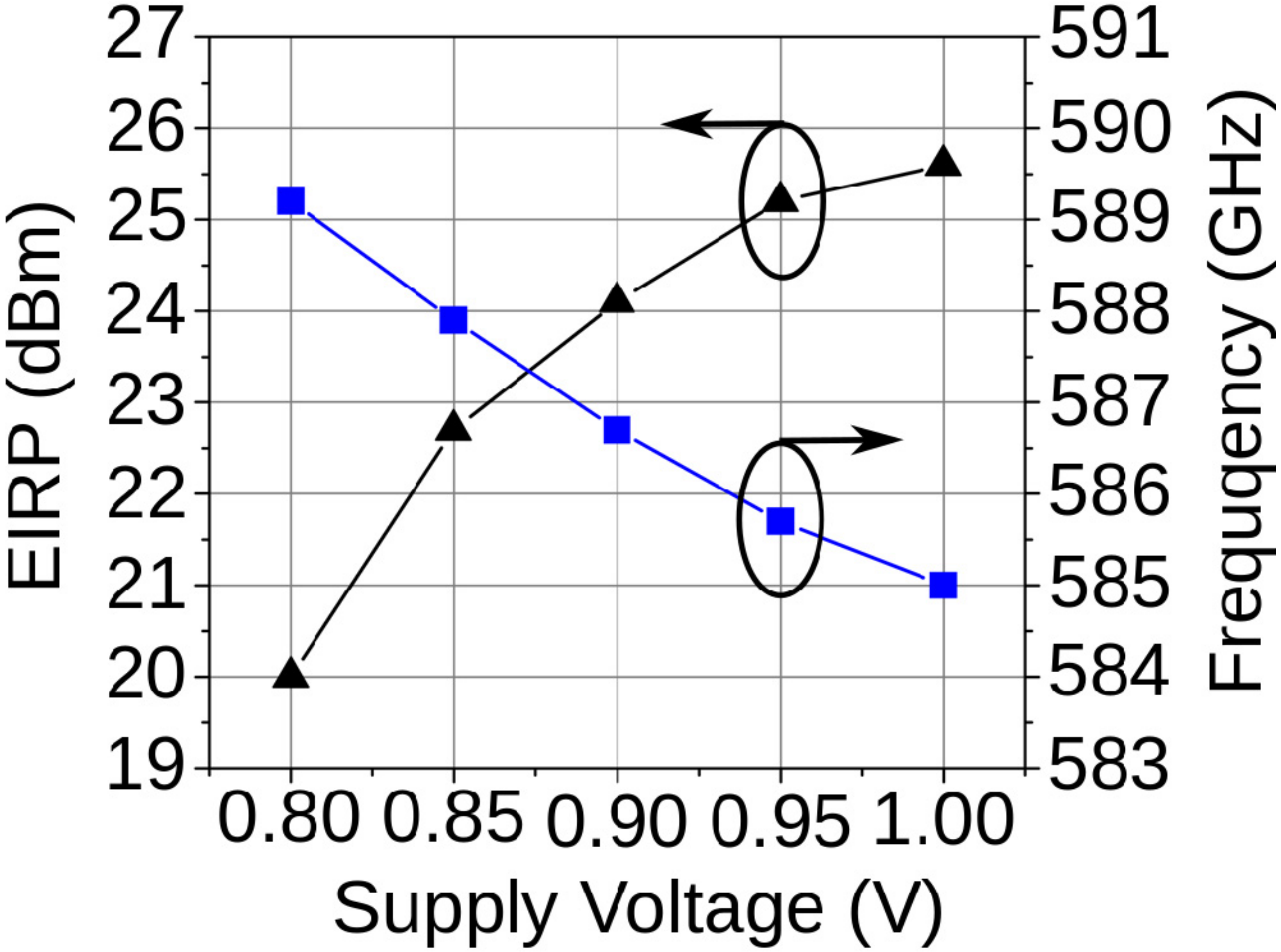
Spectrum at $4f_0$



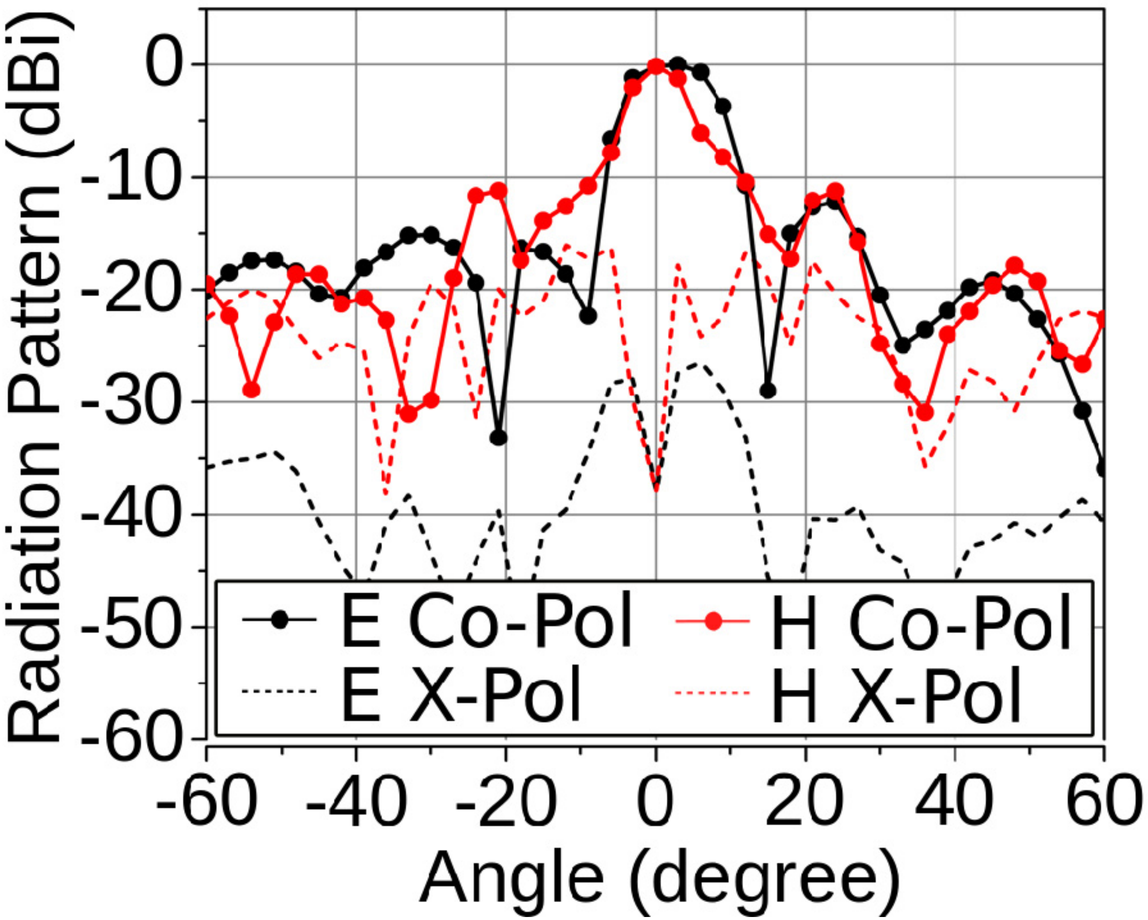
Phase Noise at $4f_0$

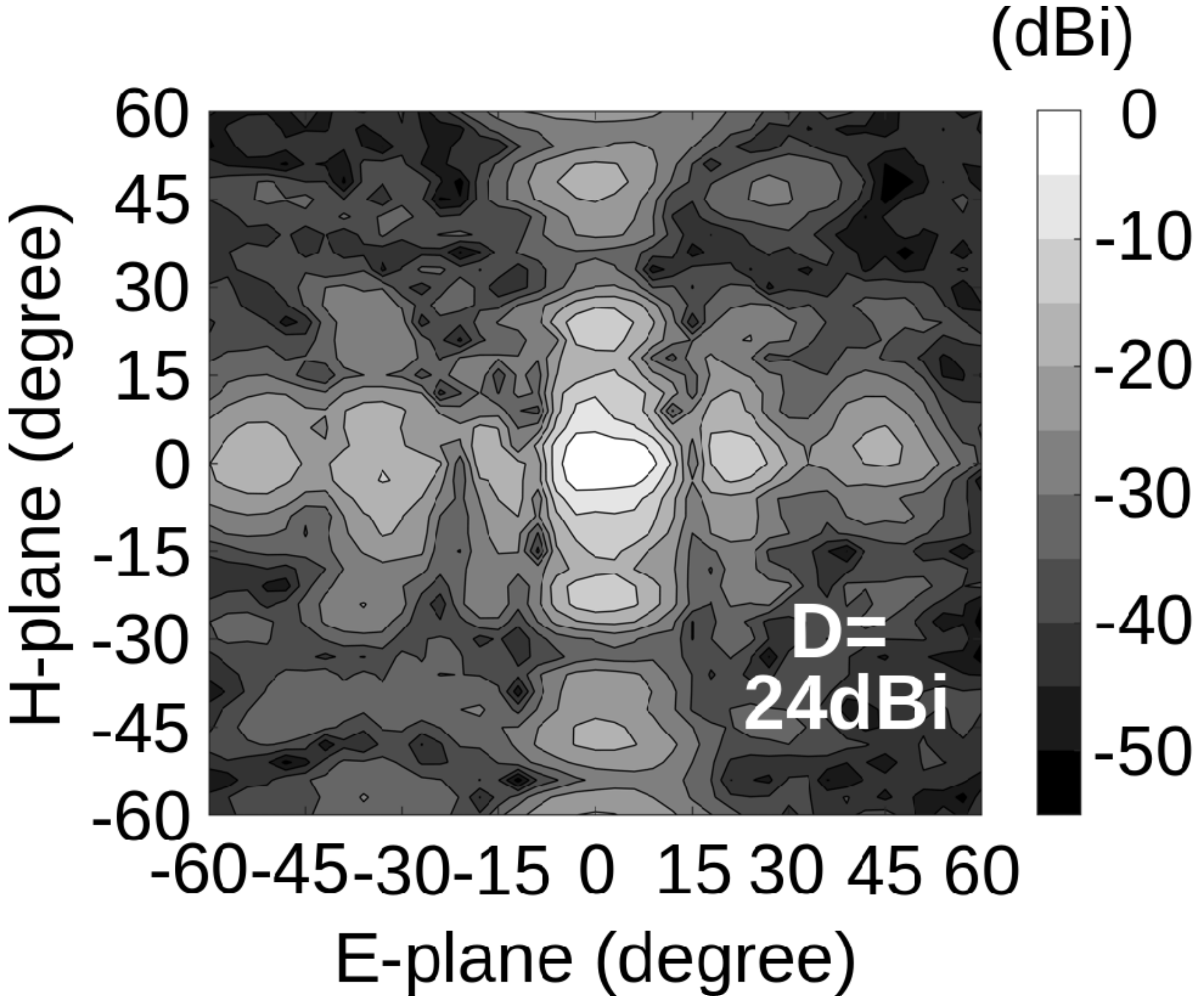
Measured EIRP



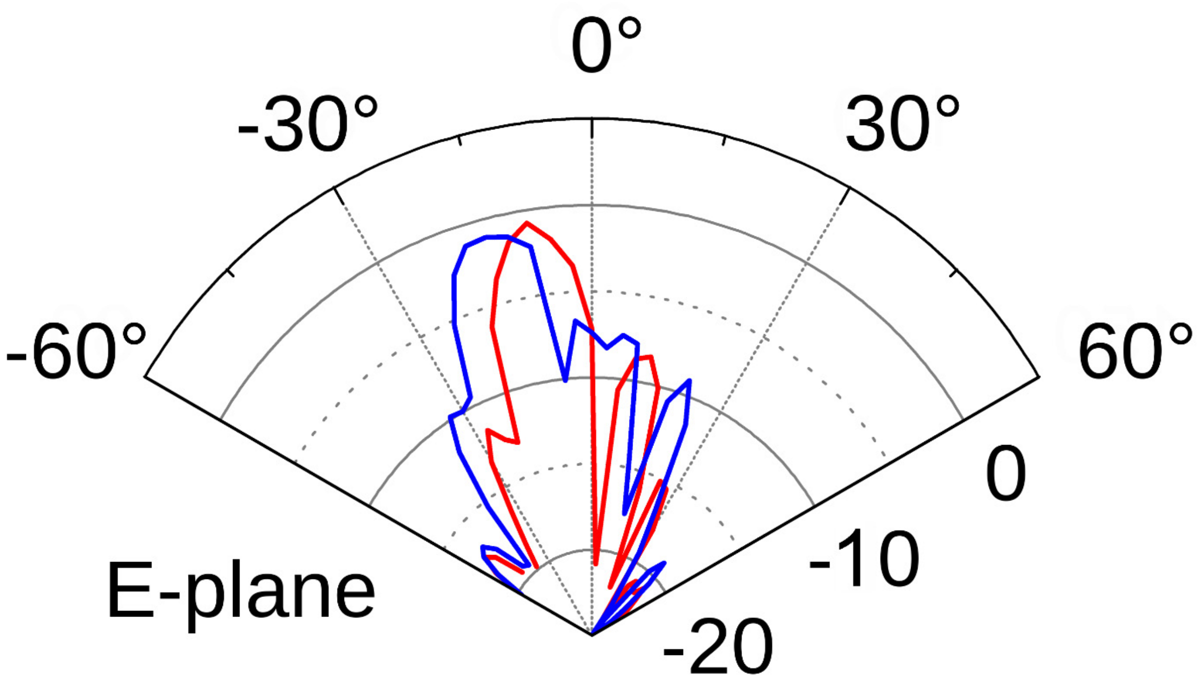


Measured Radiation Pattern

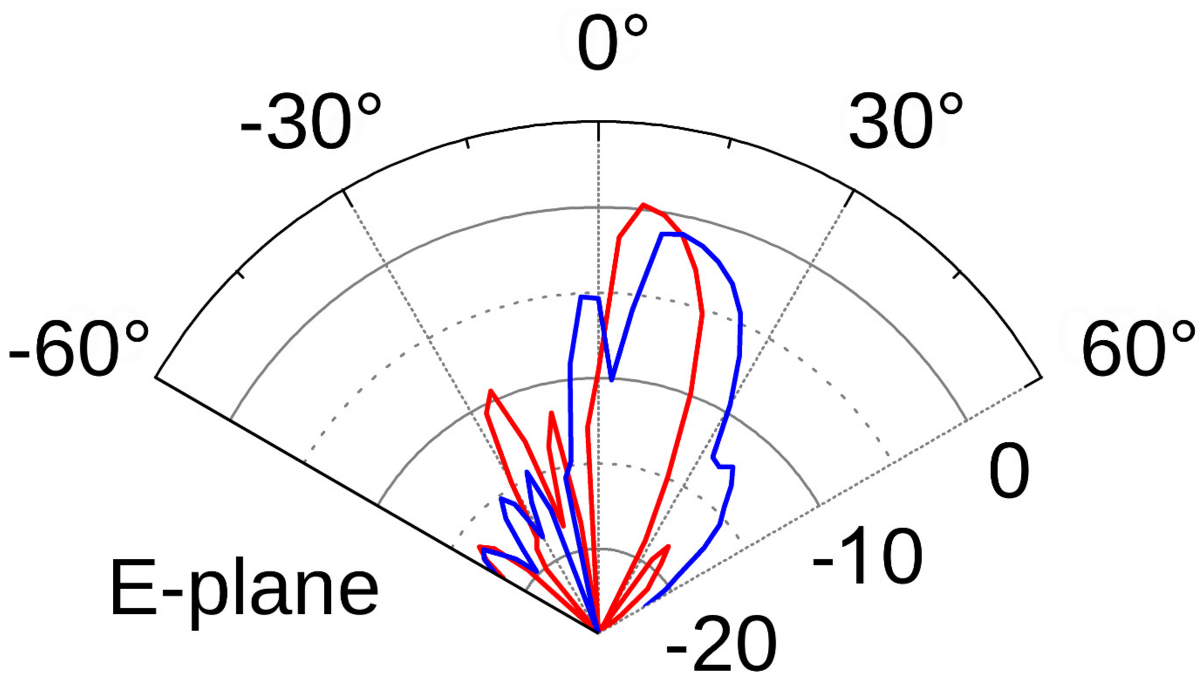




Measured Beam Steering



Normalized Radiation Pattern (dBi)



Normalized Radiation Pattern (dBi)

Comparison Table

	This Work	JSSC19	ISSCC14	ISSCC16	JSSC15
Frequancy (GHz)	586.7	531.5	530	553	498
EIRP (dBm)	24.1*	2.3	25	N/A	N/A
Directivity (dBi)	24	14.3	37	N/A	N/A
Radiated Power (dBm)	0.1*	-12	-12**	-27	-16.6***
Tuning Range (%)	0.7	0.9	3.2	3.8	5.1
DC Power (W)	1.278	0.26	0.156	0.172	0.425
DC-to-THz Efficiency (‰)	0.8	0.24	0.4	0.01	0.051
Phase Noise at 1MHz (dBc/Hz)	-82	-N/A	-N/A	-74	-87

* An extral 1.5dB output power can be achieved by increasing the supply from 0.9V to 1V.

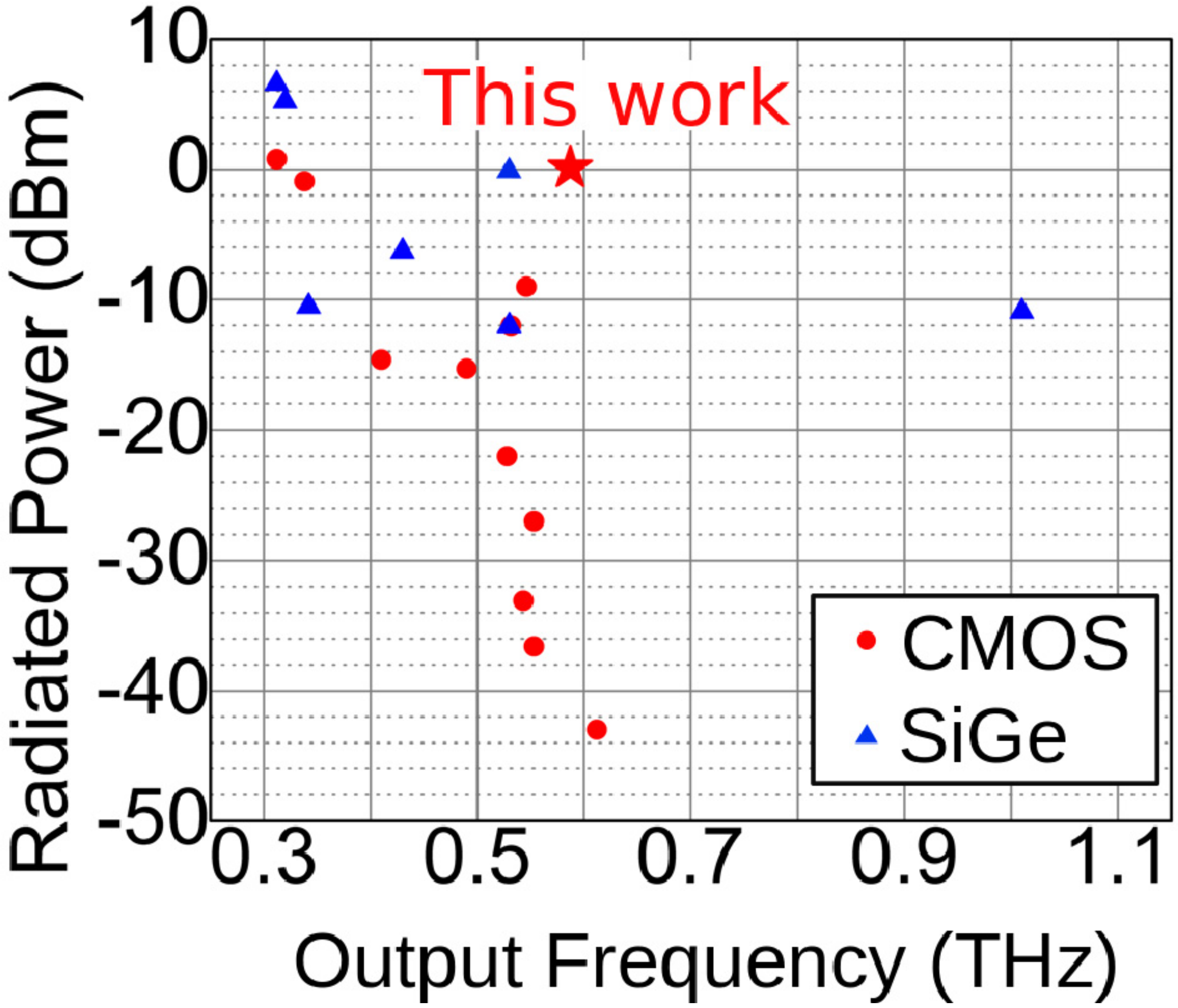
** Radiated power of a single source pixel in a non-coherent oscillator array.

*** Measured on wafer using probe.

Comparison Table

	This Work	JSSC19	ISSCC14	ISSCC16	JSSC15
Beam Steering (°)	30	60	No	No	No
Array Size	36(6×6)	4(1×4)	16(4×4)	1	1
Area (mm^2)	0.68	2.5	4.2	2.79	0.5
P_{rad} Per Element (dBm)	-15.5	-18	-12	-27	-16.6
P_{rad}/ Area ($\mu W/mm^2$)	1505	25	238	0.7	44
Technology (f_{max})	40nm Bulk CMOS (300GHz)	40nm Bulk CMOS (300GHz)	130nm SiGe (500GHz)	65nm Bulk CMOS (240GHz)	90nm SiGe (350GHz)

Comparison of Radiated Power



Conclusion

- A compact oscillator core with 4th harmonic boosting and a harmonic selective antenna were presented.
- 36 oscillators are coupled together.
- An output power of 1mW is achieved at 0.59THz.
- A beam steering range of 30 degree is achieved.