

Session 23 Overview: *THz Circuits and Front-Ends*

RF SUBCOMMITTEE



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The THz frontier continues to be pushed by mainstream-CMOS circuits with excellent performance. The papers present diverse circuits and front-ends extending state of the art on linearity, signal generation/steering, and detection sensitivity. The first paper presents a THz upconverter leveraging the benefit of parametric gain using optimally biased varactors for enhanced even-order harmonic generation. A THz 2D beam-steering pixel-array source with the capability to spatially and electronically steer is presented in the second paper. The session continues with an ultra-low power and area THz detector with leading-edge noise performance and concludes with a W-band PLL demonstrating best-in-class jitter and FoM.

9:15 AM

23.1 270-to-300GHz Double-Balanced Parametric Upconverter Using Asymmetric MOS Varactors and a Power-Splitting-Transformer Hybrid in 65nm CMOS

Zhiyu Chen, University of Texas, Dallas, TX

In Paper 23.1, the University of Texas, Dallas, presents a 270-to-300GHz double-balanced parametric upconverter based on asymmetric MOS varactors and a power-splitting-transformer hybrid in 65nm CMOS. Among upconverters operating near 300GHz, the paper reports the highest conversion gain and 1st-order linearity.



9:23 AM

23.2 A 436-to-467GHz Lens-Integrated Reconfigurable Radiating Source with Continuous 2D Steering and Multi-Beam Operations in 65nm CMOS

Hossein Jalili, University of California, Davis, CA

In Paper 23.2, the University of California, Davis, presents a reconfigurable lens-integrated 436-to-467GHz radiating source with the peak directivity of 26dBi, 51-to-95mW power consumption, and continuous uninterrupted 2D electronic beam scanning leveraging multiple steering methods. The circuit is capable of supporting high-resolution and fast imaging for THz applications.



9:31 AM

23.3 A 605GHz 0.84mW Harmonic Injection-Locked Receiver Achieving 2.3pW/√Hz NEP in 28nm CMOS

Ariane De Vroede, KU Leuven - MICAS, Leuven, Belgium

In Paper 23.3, KU Leuven presents a 605GHz sub-1mW harmonic injection-locked receiver achieving 2.3pW/√Hz noise-equivalent power (NEP) in a 28nm CMOS process. The paper introduces a new approach for THz detection with the lowest published NEP for CMOS detectors operating above 500GHz.



23

9:39 AM

23.4 An 82fs_{rms}-Jitter and 22.5mW-Power, 102GHz W-Band PLL Using a Power-Gating Injection-Locked Frequency-Multiplier-Based Phase Detector in 65nm CMOS

Suneui Park, KAIST, Daejeon, Korea

In Paper 23.4, KAIST presents a PLL that can directly generate an ultra-low-jitter W-band signal. The 65nm-CMOS 102GHz W-band PLL uses a gated injection-locked frequency-multiplier-based phase detector to achieve 82fs_{rms} jitter.



23.1 270-to-300GHz Double-Balanced Parametric Upconverter Using Asymmetric MOS Varactors and a Power-Splitting-Transformer Hybrid in 65nm CMOS

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Wireless communication at ~300GHz is drawing attention due to its potential to support a high data-rate using the wide available bandwidth. Transmitters operating at ~300GHz have been reported in [1-5]. In order to support the high-order modulation, high data-rate, and an increased range, the transmitter must have a high output 1dB compression point (OP_{1dB}) and a wide bandwidth. Unfortunately, instead of OP_{1dB} , only the saturated output power levels, P_{sat} , of the CMOS transmitters [3-5] are reported. A 272GHz CMOS amplifier has been reported in [6], but it only achieves an OP_{1dB} of -10.18dBm and a 3dB bandwidth of less than 5GHz. Broadband power amplification at 300GHz in CMOS is not practical since the transistor f_{max} is ~350GHz or less. Due to this, the CMOS-transmitter linear output power is limited by the upconversion mixer OP_{1dB} . Unfortunately, the mixers operating near 300GHz suffer from low conversion gain (CG) and OP_{1dB} .

This work demonstrates a 270-to-300GHz double-balanced fundamental upconverter that employs asymmetric accumulation-mode MOS varactors (ASVARs) [7] in a 65nm foundry CMOS process and that achieves OP_{1dB} of -6.2dBm (-5.2dBm excluding the loss of output balun for measurements), maximum CG of -11.2dB (-9.2dB excluding the losses of input and output baluns for measurements) benefiting from the 3dB Manley-Rowe gain [8], and a 3dB bandwidth of ~25GHz. The mixer also provides a P_{sat} greater than -3dBm. The maximum CG and OP_{1dB} are the highest among upconverters operating near 300GHz fabricated in any integrated-circuit technologies including III-V technologies. The mixer is the first to employ ASVARs and can be integrated with the modulator in [3] to generate QPSK signals at ~285GHz.

Figure 23.1.1 shows a conceptual schematic of a parametric upconverter. The theoretical maximum CG of reactive mixing is the ratio between radio frequency (RF) and intermediate frequency (IF), when local oscillator (LO) frequency is lower than RF, and if power at only RF, IF, and LO frequencies is allowed to flow [8]. The reactive mixing can provide gain. Although the practical CG is lower due to the losses of reactive elements and termination networks, it is intrinsically higher than that of mixing using transistors. Compared to the transistors in CMOS, varactors have lower loss, and their dynamic cut-off frequency $(1/C_{min} - 1/C_{max})/(2\pi R_c)$ can be ~3THz [7]. A schematic and a cross-section of ASVARs are shown in Fig. 23.1.1. ASVARs consist of two n-type varactors (n-VARs) connected in parallel. The gate voltage of ASVAR (V_G) and the n-well voltage of one of the n-VARs (V_{NW}) can be independently set to control the shape of the capacitance-voltage (C-V) curve (Fig. 23.1.1, Middle). Having a stair-cased C-V curve suppresses odd-order harmonic generation while enabling even-order harmonic generation [7]. This simplifies the termination of unwanted harmonics and intermodulation products required for the Manley-Rowe gain.

The proposed ASVAR upconverter is shown in Fig. 23.1.2. It takes an IF signal centered at 150GHz and upconverts to RF at ~290GHz with an LO signal at 135 to 140GHz. This LO and IF combination allows a wide bandwidth operation and image rejection while enabling the LO driver implementation in CMOS. The finger width-to-length ratio of the ASVAR is $W/L=0.8\mu m/0.15\mu m$. The number of fingers, N_f , of 24 for each n-VAR is chosen for an LO power of 10dBm with $V_G=-0.3V$ and $V_{NW}=0.1V$. At this bias, the varactors can support an LO signal swing between 1.3V and -1.3V while keeping the voltage across the gate dielectric layer at less than 1V. When LO reaches the negative peak, both n-VARs are in the depletion region. Because the voltage is divided between the gate dielectric and depletion layers, a significantly larger voltage can be applied across the n-VAR [7]. Harmonic load-pull simulation is utilized to maximize CG and to determine the optimum termination for IF, LO, and RF ports, respectively.

An ASVAR is a one-port device requiring additional circuits for isolation of LO and the signals at RF and IF. A fully differential hybrid structure using a power-splitting transformer is utilized for signal isolation. The structure of the hybrid and the top views of IF, LO, and RF paths are shown in Fig. 23.1.3. The transformer is formed using the Aluminum layer (~1μm thick) and the top copper layer, M10 (~3μm thick). A differential IF signal is fed to the primary inductor and split into all four ASVARs through the two secondary inductors while a differential LO signal is fed to the center taps of the secondary inductors through grounded coplanar waveguides (GCPWs) to provide LO signals to ASVAR#1 and #3 that are in phase as well as to ASVAR#2 and #4. A 9μm

long transmission line (T_1) is inserted between each ASVAR and the output of secondary inductors for RF matching. Since the LO and IF signals applied to ASVAR#1 have the same phase relation as that applied to ASVAR#2, the top RF signals generated from ASVAR#1 and #2 are in phase. Similarly, the bottom RF signals generated from #3 and #4 are in phase while they are out of phase from the top ones. The in-phase RF signals at the top or bottom are combined using two 15fF metal-oxide-metal (MOM) capacitors (C_1). Because each of the feeding ports for IF and LO and combining junctions for RF is a virtual ground to the other two, the IF, LO, and RF ports in the hybrid are isolated. The transformer is sized to provide the optimum terminations from the harmonic load-pull simulation of the ASVAR. The simulated primary and secondary (two) inductances are 83 and 45pH with Q of 15 and 24 at 150GHz. Unfortunately, additional GCPWs for LO feed ($T_{3,1,2}$) and RF extraction (T_2) break the symmetry of the structure (Fig. 23.1.3 (Bottom Right)). In particular, $T_{3,1}$ and $T_{4,1}$ on the top cross T_2 while $T_{3,2}$ and $T_{4,2}$ at the bottom do not. To reduce the resulting imbalance by lowering the parasitic capacitance, $T_{3,1,2}$ at the crossing points are implemented using M7 (~0.4μm thick) while T_2 for RF extraction is implemented using the top copper layer (M10). The LO GCPWs are also extended ($T_{4,1,2}$) with the same M7 line at the crossing point to improve balance. This asymmetry leads to a leakage power at $2f_{LO}$. Wideband baluns formed using Al and M10 layers with a loss of ~1dB are included at all three ports to enable single-ended measurements. MOM caps C_2 to C_4 and GCPW T_5 are used for matching.

The upconverter is fabricated in a 65nm CMOS process and occupies a total area of 550×545μm² including bond pads (Fig. 23.1.7). Figure 23.1.4 shows the measured CG and OP_{1dB} versus frequency. The maximum CG is -11.2dB and -11.4dB with a 10dBm LO at 140 and 135GHz, respectively. The corresponding 3dB bandwidth is 25 and 29GHz, respectively. The measured OP_{1dB} varies within 0.5dB over the bandwidth. The gate and n-well DC bias voltages were -0.3 and 0.1V, respectively. Figure 23.1.5 shows the measured RF power versus IF power and CG versus LO power. For an LO power at the bond pad of 10dBm at 140GHz, the measured OP_{1dB} is -6.4dBm. The CG saturates at ~-10.4dB with an LO power of ~13dBm. For an LO power of 10dBm, a -22dBm leakage at $2f_{LO}$ is present at the output due to the asymmetry due to the LO distribution and RF extraction networks. The performance of the upconverter is summarized along with the previously reported upconversion mixers with the RF output of ~300GHz in Fig. 23.1.6. The upconverter reported in this paper demonstrates the highest OP_{1dB} and CG compared with the other upconverters including those fabricated using III-V devices. These results are particularly critical for mixer-last transmitters operating near 300GHz for high data-rate communication. This work suggests that upconverters using ASVARs in CMOS at ~300GHz have superior performance because of the Manley-Rowe gain and better power capability.

Acknowledgement:

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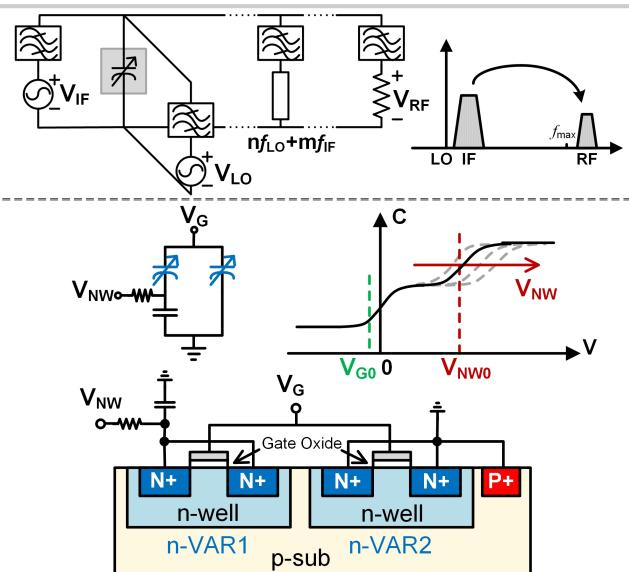


Figure 23.1.1: A conceptual schematic of a parametric upconverter. A schematic, cross-section, and C-V curve of an asymmetric MOS varactor.

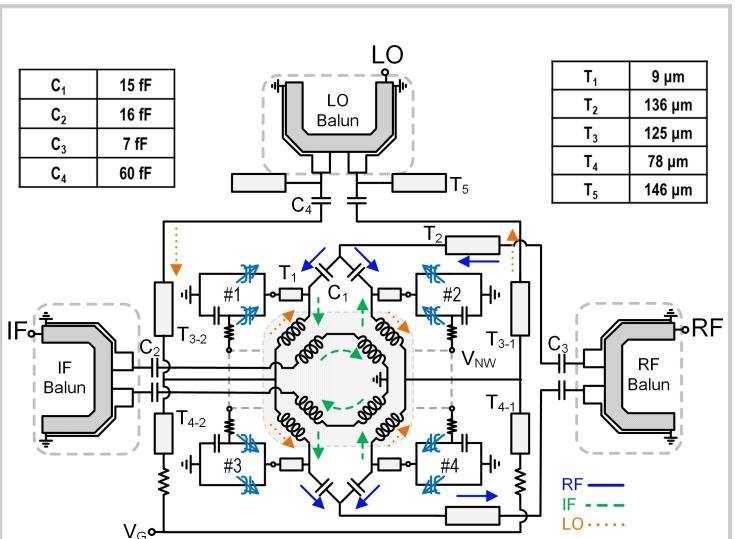


Figure 23.1.2: Circuit diagram of the proposed double-balanced ASVAR upconverter.

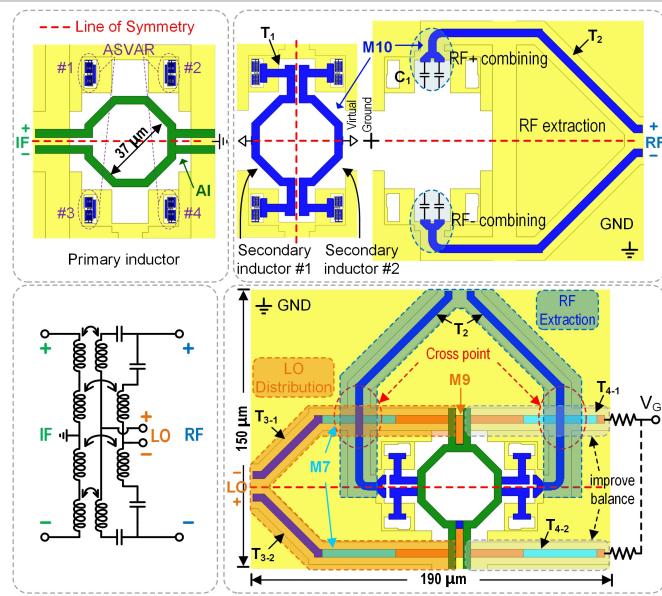


Figure 23.1.3: Differential power-splitting-transformer hybrid.

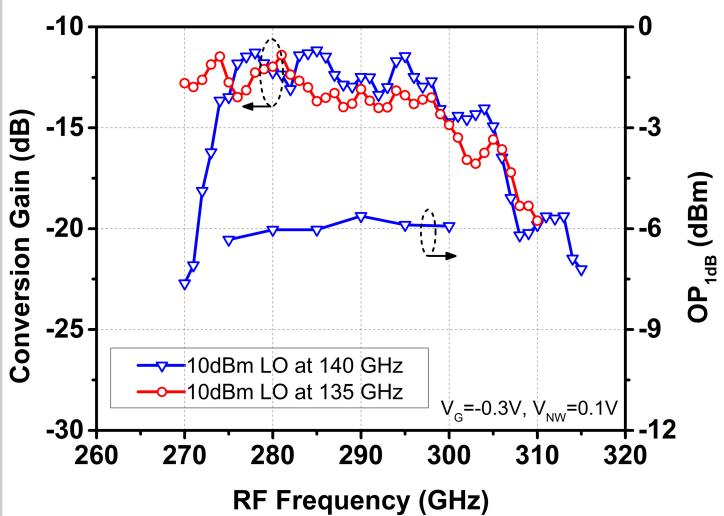


Figure 23.1.4: Measured conversion gain (CG) versus RF frequency with 10dBm LO at 135 and 140GHz. Measured OP_{1dB} versus RF frequency with 10dBm LO at 140GHz.

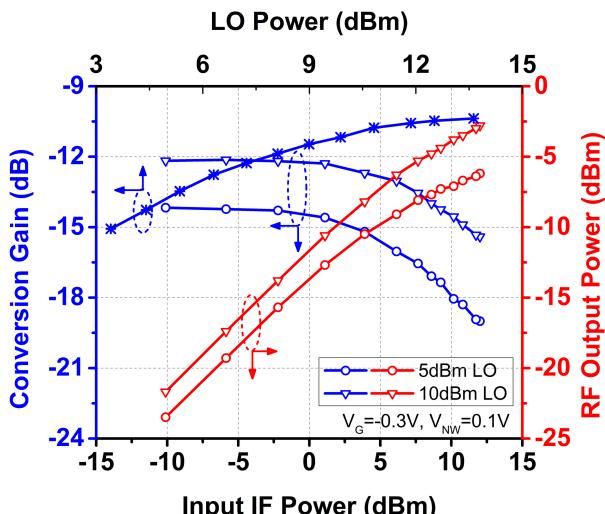


Figure 23.1.5: Measured output power and conversion gain versus input IF (155GHz) power at the LO (140GHz) power of 5 and 10dBm, and measured CG versus LO (140GHz) power.

Reference	[1]	[2]	[3]	[4]	[5]	This Work
Topology	Single-ended Resistive	Single-balanced Half-Gilbert	Double-balanced Passive-Gilbert	Single-balanced Square ^(b)	Double-balanced Reactive	
RF (GHz)	270-302	280-320	285-315	289-311	252-275	270-299
IF (GHz)	0-32	0-20	110-140	144-166	120-143	135-164
LO (GHz)	270	300	175	145	132	135
P _{LO} (dBm)	6.5	-5	--	--	--	10
Max CG ^(a) (dB)	-15	-15	--	--	--	-11.4
OP _{1dB} ^(a) (dBm)	-16.5	--	--	--	--	-7.5
P _{sat} ^(a) (dBm)	--	--	-6	-14.5 ^(c)	-7.6 ^(c)	>-3 ^(d)
P _{DC} ^(a) (mW)	0	22	0	19.95 ^(c)	0	0.3
Area ^(e) (mm ²)	1	--	0.02 ^(e)	0.05 ^(c/e)		0.3
Technology	80nm InP	250nm InP	65nm CMOS	40nm CMOS	40nm CMOS	65nm CMOS

^(a) Mixer only. ^(b) Doubler-based. ^(c) Per channel. ^(d) Limited by instrument. ^(e) Estimated from die photo.

Figure 23.1.6: Performance summary and comparison with the prior-art upconverters with RF of ~300GHz. P_{sat}, OP_{1dB}, power consumption are normalized by the number of chains combined.

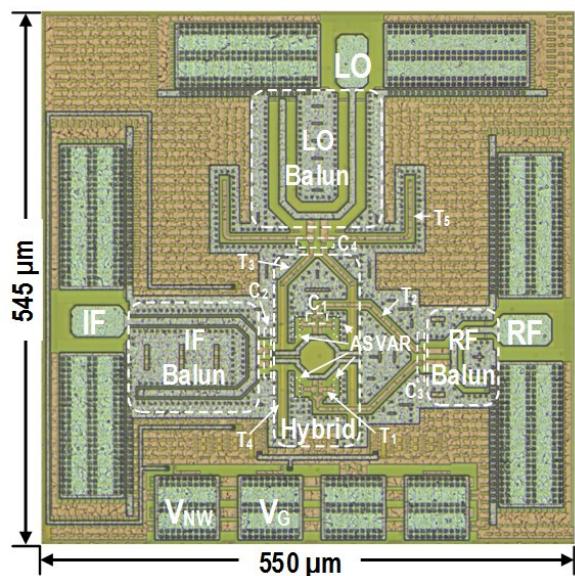


Figure 23.1.7: Die micrograph.

23.2 A 436-to-467GHz Lens-Integrated Reconfigurable Radiating Source with Continuous 2D Steering and Multi-Beam Operations in 65nm CMOS

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High-resolution and fast imaging/sensing at THz requires highly directive steerable beams for scanning the object. A coherent array of coupled sources could improve the radiated power but requires mechanical and slow scanning of the object [1]. Phased array systems could use beam steering to scan the object at a higher speed, but in both coherent-array and phased-array systems, large array sizes with high power consumption are needed to generate a highly directive and narrow beam for high image resolution [2-4]. Although Si lens can be used to increase directivity in a phased array, the steering capability is significantly diminished [5]. Therefore, arrays of non-coherent sources are used with Si lens to illuminate different parts of the object with each source with high directivity [6]. The firing angle of each source is determined by the ratio of its displacement (L_{dis}) from the lens center to the lens radius (R_{lens}), as shown in Fig. 23.2.1 [1]. However, this type of source can only illuminate the object in discrete steps determined by beam spacing, which in turn is limited by the inevitable distance between adjacent sources on the chip. Being constrained to independent single pixels for illumination leads to loss of resolution and blind spots between the neighboring beams (Fig. 23.2.1). A larger lens can improve the resolution by reducing the beam spacing but at the cost of a smaller total scanning range.

This paper presents a lens-integrated, wideband, and reconfigurable 450GHz 3x7 array that combines two different methods of beam steering: antenna displacement and phase shifting. This way we can achieve both high directivity and fine scanning resolution through continuous steering between the beams of the adjacent pixel sources while consuming little power. In the implemented array, each pixel source is capable of injection locking to its adjacent cells if they are turned on at the same time. Therefore, single pixels or a subsection of the array can be turned on with phase/frequency locking between the activated cells, firing the beam at the desired directions (Fig. 23.2.1). Furthermore, the circuit is capable of multi-beam radiation by simultaneous activation of subarrays without intersecting corners. To increase the resolution and cover the blind spots between two adjacent beams produced by individual cells, the two cells can be activated simultaneously, and by controlling their relative phase shift through coupling, the beam is steered within the blind spot.

Figure 23.2.2 shows the circuit structure of the implemented array. The unit cells consist of standing wave oscillators (SWO) with 4th-harmonic extraction and radiation by on-chip folded slot antennas [1]. Each cell is coupled to its neighboring units with a MOM capacitor (C_c) in both horizontal and vertical directions. The use of this capacitor allows us to control the gate bias (V_g) of each cell independently making it possible to turn individual cells on and off or to create a phase shift between two adjacent cells by changing their relative V_g [4]. Transistor switches are placed at the four corners of each cell and are controlled by the gate bias. When a cell is off, the switch is automatically closed thus turning C_c into a termination capacitor for the adjacent cells, suppressing the loading effect from the off cells, and, therefore, preserving frequency and output power levels. If the cell is on, this switch is open, allowing the cell to couple to its neighboring unit through C_c and extending the length of the standing wave formed on the gate lines. The loss of the switch is minimized by its placement at the nodes of this standing wave. The formation of injection and termination paths are shown in Fig. 23.2.2. Essentially, when a subsection of the array is on, C_c capacitors act as coupling capacitors between the activated cells and also as terminations at the edges of this subsection.

As shown in Fig. 23.2.2, the grounded C_c s between the cells shunt part of the injection power. Therefore, larger C_c values increase this injection leakage but also result in stronger series injection and better termination at the edges of the cells, creating a trade-off on the size of C_c . The capacitor is designed to ensure robust coupling and adequate termination for both 1x2 and 2x1 cases. The measured locking range for these two scenarios is shown in Fig. 23.2.3 demonstrating a wide locked ΔV_g (the difference between gate voltages of the coupled cells) of $-135mV < \Delta V_g < 140mV$ and $-150mV < \Delta V_g < 150mV$ for 1x2 and 2x1 cases, respectively. This wide ΔV_g helps create significant phase shifts between the cells and perform fine beam steering. Figure 23.2.3 presents the single-tone radiation patterns of both cases along with a 2x2 case, demonstrating the agility and robustness of the proposed coupling technique. Figure 23.2.3 also shows the measured radiation patterns of two independent sections at 436 and 450GHz frequencies, demonstrating simultaneous multi-beam/multi-frequency and 2D-beam-steering capabilities of the circuit.

The thickness of the Si wafer between the chip substrate and hemispherical lens (L_{ext}) has a significant impact on the radiation behavior with its optimum value, $L_{ext}=\sim 1.5mm$, maximizing the single antenna directivity (D) for $R_{lens}=5mm$ (Fig. 23.2.4) [1]. At $L_{ext}=1.5mm$, each one of the two cells fire at a different angle with high directivity resulting in two distinct, narrow, and non-overlapping lobes (Fig. 23.2.3). This limits the beamforming capabilities of the array. However, if L_{ext} is increased to 2mm, the less directive wider beams from each cell overlap, and the superposition of the two steers the direction of the beam toward the middle of the two beams associated with the individual cells. This pattern superposition also combines the radiated power from the two cells and restores EIRP close to that of a single source with an optimum L_{ext} of 1.5mm (Fig. 23.2.5). Furthermore, by creating a phase shift between the two cells through ΔV_g and performing beam steering, the described blind spot between the two beams is covered with similarly directive beams. The measured result in Fig. 23.2.4 demonstrates an uninterrupted coverage of $\pm 28^\circ$ and $\pm 8^\circ$ in the E-plane and H-plane, respectively. The scanning range in both directions can be further increased by scaling the size of the array.

The chip was fabricated in a 65nm CMOS process (Fig. 23.2.7) and was mounted inside an opening in the PCB to a high-resistivity undoped Si wafer. Additional wafers were added to implement $L_{ext}=1.5$ and 2mm. A silicon lens with a 5mm radius was used and all presented radiation patterns were measured at a far-field distance of 14cm. The frequency of the radiated power is characterized using an even-harmonic mixer (EHM) and is shown in Fig. 23.2.5 along with the circuit power consumption. The operation frequency overlap of single and 1x2 configurations covers 435.8 to 467.3GHz resulting in 7% tuning range. Each cell consumes ~50mW at the center frequency from a 1V supply voltage. Due to the limited sensitivity of the PM5 power meter, the mixer loss is characterized with a power meter at frequencies of interest and is used to measure EIRP. The result is shown in Fig. 23.2.5 with the maximum EIRP of 3.6dBm from a 1x2 configuration with $L_{ext}=2mm$ at 450GHz. Figure 23.2.5 also shows the measured directivity versus steering angle with the peak directivity of 26dBi. The high directivity in all directions along with continuous beam steering enables high-resolution operation in an imaging/sensing system.

Figure 23.2.6 presents a comparison of this work with the prior art. Compared to lens-less implementations, this source delivers the same continuous steering operation but with more directivity at significantly lower power consumption. Among lens-integrated sources, it demonstrates continuous and high-resolution scanning range with no blind spots and wider-band operation compared to [6] and higher directivity, 2D scanning capability, and ~2x steering angle at significantly lower power consumption compared to [5].

Acknowledgement:

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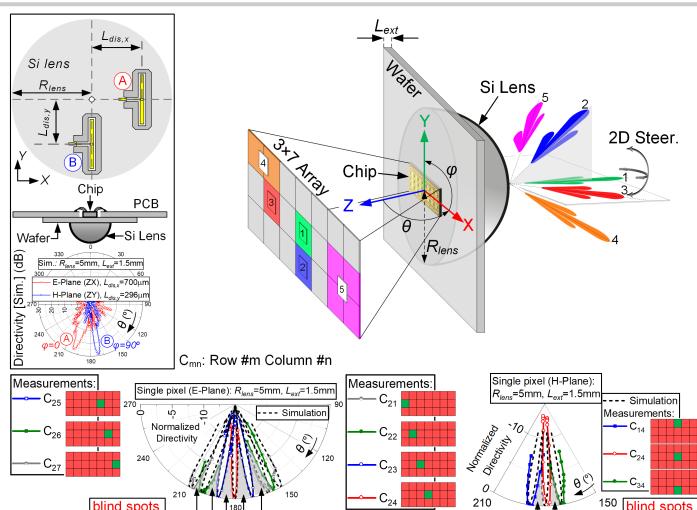


Figure 23.2.1: Activation of various sections of the reconfigurable array steers the beam in different directions (top right) due to displacement from the lens center (top left). Mere single-pixel activation creates blind spots for imaging/sensing between beams (bottom).

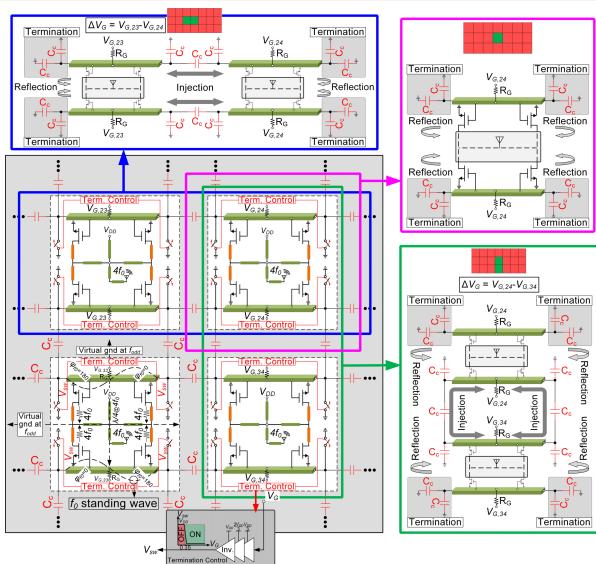


Figure 23.2.2: The structure of the implemented array with the coupling capacitor mesh and the circuit operation when a single pixel, 1x2, or 2x1 section is activated.

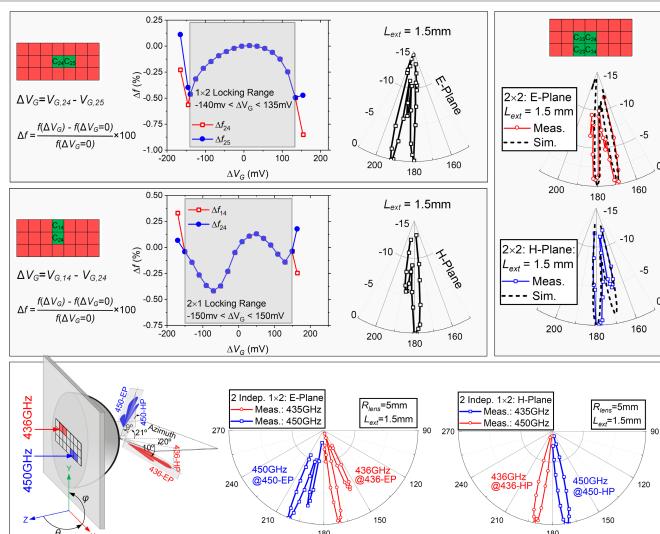


Figure 23.2.3: Measured locking ranges and radiation patterns of the array (top), and simultaneous multi-beam radiation at separate frequencies with 2D beam steering (bottom).

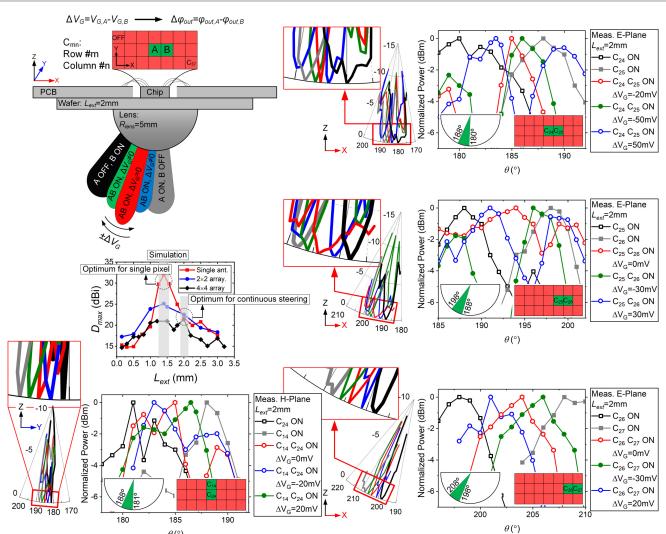


Figure 23.2.4: Measured beam patterns for fine and coarse beam steering showing the coverage of the blind spots between discrete steering steps by creating a variable phase shift between two activated adjacent cells.

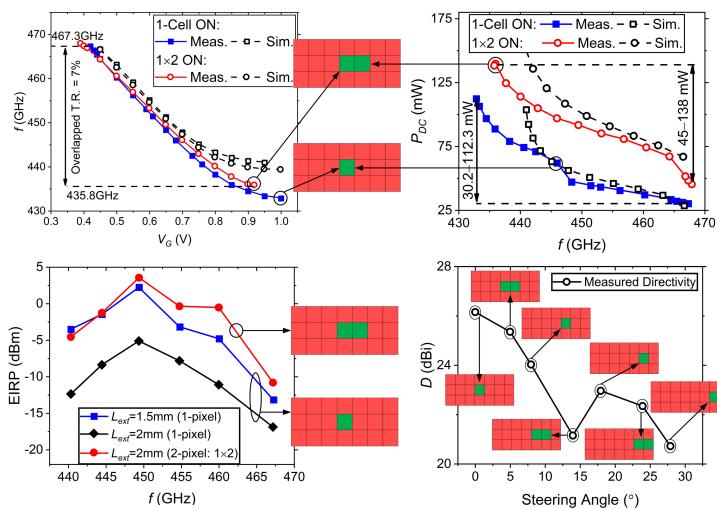


Figure 23.2.5: Measured frequency, power consumption, EIRP versus frequency, and directivity versus steering angle of the radiating source.

	Array Size	Radiation	Tech.	f _{max} (GHz)	f _c (GHz)	Scan Range (°)	T.R. (%)	Peak Directivity (dBi)	Peak EIRP (dBm)	P _{DC} (W)	Area (mm ²)
This Work	3x7 ¹	Folded Slot Ant. + Si Lens ($R_{lens}=5\text{mm}$)	65nm CMOS	340	450	56/16 (2D)	7	25.35 ²	3.6 ³	0.095 ²	4
								26.15 ³	-5.1 ³	0.051 ³	
ISSCC 2014 [2]	4x4	Patch Ant.	65nm CMOS	N/A	338	45/50 (2D)	2.1	18 ⁴	17	1.54	3.9
ISSCC 2020 [3]	4x4	Patch Ant.	65nm CMOS	250	416	60/60 (2D)	1.7	17 ⁴	14	1.45	4.1
JSSC 2019 [4]	2x2	Patch Ant.	0.13μm SiGe	215	344	128/53 (2D)	15.1	11.7	4.9	0.45	1.2
ISSCC 2020 [5]	6x6	Folded Monopole + Si Lens ($R_{lens}=5\text{mm}$)	40nm CMOS	300	586.7	30 (1D)	0.7	24	24.1	1.278	0.68
ISSCC 2020 [6]	8x8	Circular Slot Ant. + Si Lens ($R_{lens}=7.5\text{mm}$)	0.13μm SiGe	500	420	68° (2D) (discrete)	0.7	36.4 ⁶	32.8 ⁶	6.9 ⁷	12.6
JSSC 2020 [1]	25	Folded Slot Ant. + Si Lens $R_{lens}=12.5\text{mm}$ $R_{lens}=5\text{mm}$	65nm CMOS	340	459	0	8.9	21.1	19.3	1.18	3.94
								16.8	14.7		

¹Reconfigurable ²Two-cell (1x2) activation ³Single cell activation ⁴Based on EIRP - P_{rec} ⁵7.5° beam spacing ⁶Estimated: Single pixel ⁷All pixels ON

Figure 23.2.6: Comparison of the implemented chip performance with prior art.

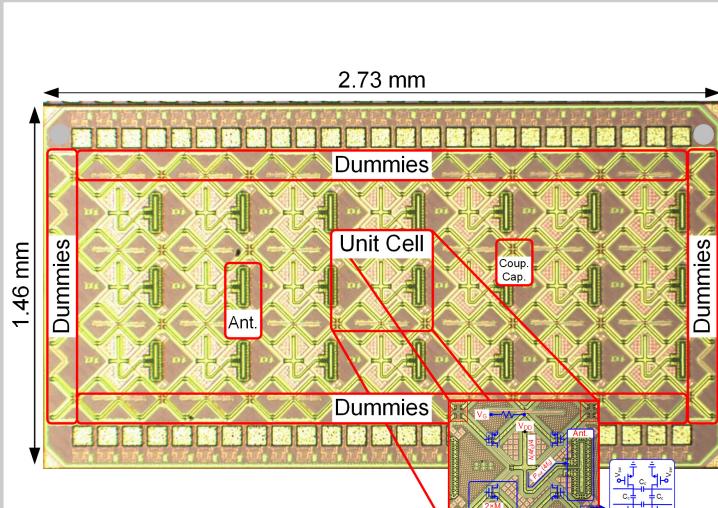


Figure 23.2.7: Die micrograph.

23.3 A 605GHz 0.84mW Harmonic Injection-Locked Receiver Achieving 2.3pW/Hz NEP in 28nm CMOS

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The use of THz signals for imaging and sensing, enabling numerous applications in object characterization, medical, security, and other fields, has gained large interest in recent years. Both THz transmitters and receivers have been successfully implemented in commercial CMOS technologies, bringing numerous advantages: low cost, the possibility of integration with standard digital logic, and high yield. Nevertheless, efficient power generation in silicon technologies is still a challenge above the maximum frequency of oscillation (f_{\max}). Therefore, improving the sensitivity of terahertz detectors is crucial. As f_{\max} in CMOS is saturating, new circuit architectures are required for efficient and sensitive THz detection. So far, Schottky Barrier Diodes and self-mixing MOSFETs have been the most successful topologies in CMOS above 500GHz, attaining noise-equivalent powers (NEP) around 10pW/Hz [5-9]. The presented work breaks this barrier and achieves a minimum NEP of 2.3pW/Hz at 605GHz.

In this paper, a new approach to terahertz detection is proposed. It uses harmonic injection locking to detect power above f_{\max} . The sensitivity of a free-running oscillator to injected signals close to its oscillation frequency and the resulting phenomenon, called injection locking, have been extensively studied [1]. As explained in [2], an oscillator with free-running frequency f_0 can also be influenced by harmonic interferers at $(M/N) \times f_0$, where the N^{th} harmonic of the input signal interacts with the M^{th} harmonic of the oscillator. Harmonic injection-locked oscillators (H-ILOs) are well known for their use in frequency synthesis and FSK demodulation [3]. In this work, however, the possibility of using H-ILO for above- f_{\max} power detection by injection locking to the third harmonic is demonstrated. The injection locking principle provides the necessary sensitivity by extremely-high-quality filtering of the weak input signal. The inherent feedback of the oscillator converts this weak input signal to a strong oscillation, which is easily detectable with an envelope detector. This strong amplification of very weak signals, realized without power-hungry and noisy amplification stages, results in a very low NEP.

The locking of an oscillator does not only result in a fixed phase relation to the injected signal, but it also influences the oscillation amplitude [2]. By measuring the oscillation amplitude, the amount of injected power can thus be determined. Combined with harmonic injection, this property can be used to achieve highly sensitive THz detection. The circuit diagram is shown in Fig. 23.3.1. At the core of the receiver is an injection-locked oscillator (ILO) running at ~200GHz. The ILO is followed by an envelope detector, which tracks the oscillation amplitude. The input signal is at a frequency of ~600GHz. To couple the input signal into the ILO tank, one can use injection transistors, which decouple the antenna from the ILO. However, these transistors would increase the power consumption, lower the fundamental oscillation frequency by introducing parasitic capacitance, and introduce additional noise without amplifying the input signal as it is above f_{\max} . In the proposed topology, these injection transistors are omitted by combining a folded dipole antenna and the ILO inductor into one element, which is carefully designed to accommodate oscillation at 200GHz while efficiently coupling the 600GHz input signal into the ILO cross-coupled pair. An additional benefit of this approach is the area reduction, which results from the merging of the dipole and the inductor. The final dimensions of the folded dipole are shown in Fig. 23.3.2.

In the absence of input power, the oscillator is free-running at a frequency f_{ILO} with an oscillation amplitude $V_{\text{ILO},0}$. When a signal is received with a frequency f_{in} of approximately $3 \times f_{\text{ILO}}$, it inter-modulates with the existing f_{ILO} in the ILO. This is done by the cross-coupled pair (M_1), which operates as a mixer. If the relevant intermodulation product at $f_{\text{in}} - 2 \times f_{\text{ILO}}$ falls in the lock range of the ILO, it influences its oscillation amplitude [3]. The envelope detector (M_3) that follows the ILO thus generates an output signal related to the injected power. The dimensions of M_3 result from a trade-off between parasitic capacitance (smaller size for higher f_{ILO}) and low 1/f noise (larger size for lower noise). The power consumption and area of the envelope detector are negligible compared to the ILO. Figure 23.3.3 shows the measured spectra of the ILO with and without input power at the third harmonic. The locking of the ILO to its third harmonic is clearly visible. To avoid degradation by 1/f noise, the input power can be chopped as shown in Fig. 23.3.1. The chip output for different third harmonic input power levels, measured with a scope, is also shown in Fig. 23.3.3. In this measurement, the input power is chopped at 10kHz. Alternatively, the bias voltage of transistor M_2 can be modulated. This removes the need for signal modulation at the transmitter side.

The voltage responsivity is defined as $R_v = V_{\text{out}@f\text{chop}} / P_{\text{in}}$. For the chip characterization, the response $V_{\text{out}@f\text{chop}}$ is measured using a lock-in amplifier. The measurement setup is shown in Fig. 23.3.4. The assembly of the chip on a hyper-hemispherical silicon lens results in a measured directivity of 19.8dBi, which has been de-embedded in the shown measurement results. Figure 23.3.4 also shows the frequency response as well as the peak response for different input powers. The asymmetry in the frequency response is a known phenomenon as discussed in [2].

The critical figure-of-merit for THz power detectors is the NEP (W/Hz), defined as $[\text{Noise Density (V/Hz)} / [R_v (\text{V/W})]]$, which has to be minimized. It is the input power resulting in an SNR_{out} of 1 with an integration time of 0.5s. To minimize the NEP, the circuit is operated at a modulation frequency of 1MHz. This modulation is performed at the gate voltage of M_2 , as the modulation frequency of the signal-generation measurement equipment is limited to 10kHz. The bias and amplitude of this gate voltage are optimized for minimum NEP, resulting in a toggling of the ILO between two different frequencies, instead of completely turning the ILO off and on. The detection frequency can be tuned by changing the supply and bias voltages, as shown in Fig. 23.3.5. For $V_G = 0.3V$, the oscillation of the ILO is barely present, resulting in a high noise density. Combined with the decreased responsivity as $V_{\text{DD,ILO}}$ approaches $V_{\text{DD,ED}} = 0.9V$, this causes a strong increase in the NEP. The minimum NEP is reached at a frequency of 605.3GHz and is 2.3pW/Hz. The H-ILO combines a high-frequency selectivity with a tuning range of 6GHz (Fig. 23.3.5), which makes the topology suitable for frequency scanning. To fully benefit from this frequency selectivity and tunability, frequency calibration can be implemented by tuning the ILO until locking to a known input tone is achieved.

The comparison table in Fig. 23.3.6 shows that the achieved minimum NEP of 2.3pW/Hz is better than what was reported for CMOS power detectors above 500GHz. Only the work in [4] achieves a lower NEP at 495GHz, but this comes at a cost of increased power consumption and area. On the die micrograph in Fig. 23.3.7, the active area of only $6800\mu\text{m}^2$ is indicated, which is the smallest area of a CMOS power detector above 490GHz with NEP below 50pW/Hz in Fig. 23.3.6. The presented circuit introduces an approach to above- f_{\max} power detection, achieving low NEP in a commercial CMOS technology while consuming low DC power and low area.

Acknowledgement:

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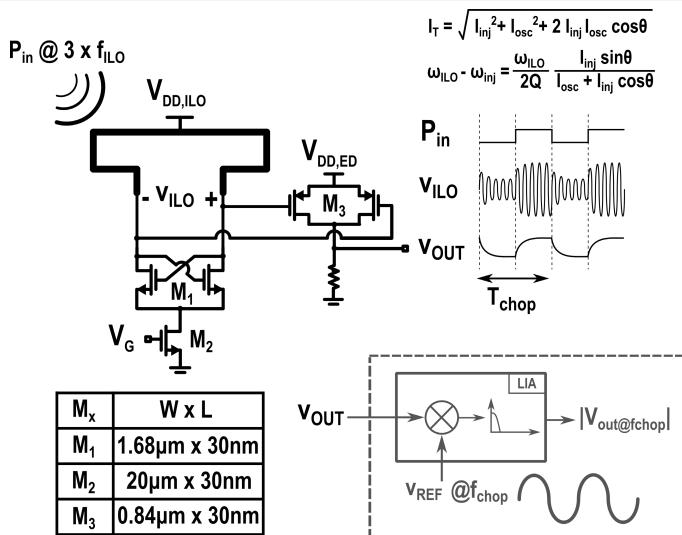


Figure 23.3.1: Circuit diagram and transistor sizes (left). Relevant waveforms (top-right). Conversion of chip output to the amplitude of its sinusoidal component at the chopping frequency using a lock-in amplifier (bottom-right).

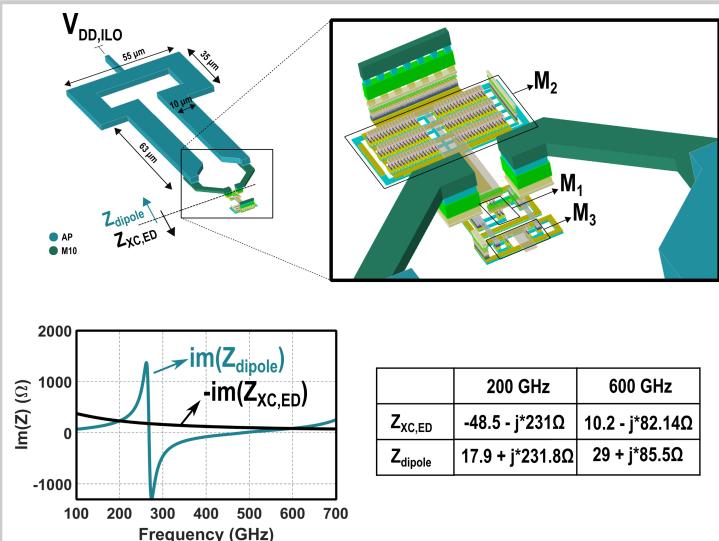


Figure 23.3.2: Layout of the proposed topology with folded dipole dimensions (top). The impedance of the folded dipole and of the cross-coupled pair with the envelope detector (bottom).

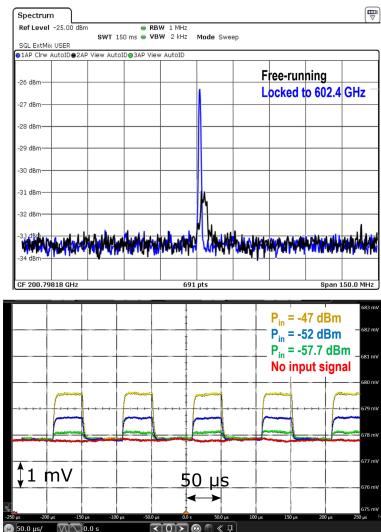


Figure 23.3.3: Frequency spectrum, measured with a WR5 horn antenna, showing unlocked and locked spectra of the ILO (top). Output time signal for different third-harmonic input-power levels (bottom).

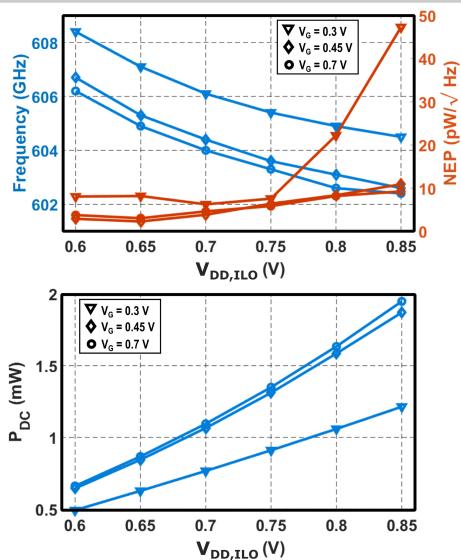


Figure 23.3.5: Measured tuning range. The minimum NEP is 2.3pW/√Hz ($R_v = 32\text{kV/W}$ at $P_{in} = -57\text{dBm}$) at $f_{in} = 605.3\text{GHz}$ and $P_{DC} = 0.84\text{mW}$.

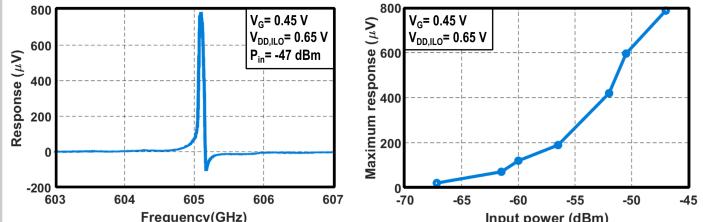
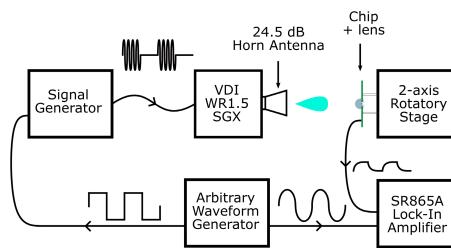


Figure 23.3.4: Measurement setup for input power modulation (top). Measured frequency response (bottom-left) and maximum response for different input powers (bottom-right).

	This work	TTST 2013 [4]	TTST 2016 [5]	JSSC 2013 [6]	ESSCIRC 2010 [7]	IRMMW-THz 2013 [8]	EuMIC 2018 [9]
Technology	28nm CMOS	40nm CMOS	0.130µm CMOS	0.130µm CMOS	65nm SOI	65nm CMOS	22nm FD-SOI
Detector type	H-ILO	IM-SRR	Diode-NMOS	SBD	Self-mixing NMOS	Self-mixing NMOS	Self-mixing NMOS
Frequency (GHz)	605	495	820	860	650	724	855
R _v (V/W)	32k	3.18G *	3.46k/2.56k *†	273	1.1k	2.2k	1.51k/ 180mA/W ‡
NEP (pW/√Hz)	2.3	0.1	12.6/36.2 †	42	50	14	23 / 12 ‡
P _{DC} /pixel (mW)	0.84	5.6 †	0.15	I _{bias} = 20 µA	-	-	-
Area/pixel (µm ²)	6800	110000 †	25000 #	15000 #	22500	10000 #	10000

[#] Estimated from die photograph

* Including low-noise baseband amplification

| Maximum/mean R_{in} and minimum/mean NEP out of array

[†] Excluding external low-noise opamp.

[†] Excluding external low
[‡] Current mode readout

Figure 23.3.6: Comparison to prior-art CMOS power detectors operating above 490GHz with NEP below 50pW/ $\sqrt{\text{Hz}}$.

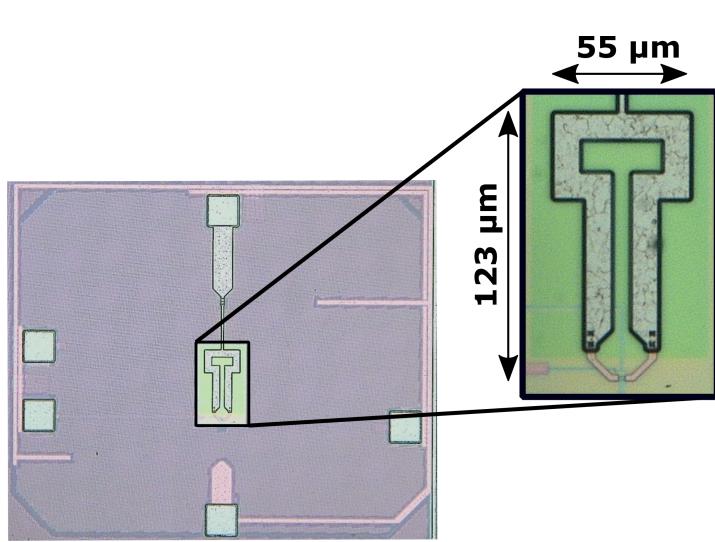


Figure 23.3.7: Die micrograph with the indication of the active area.

23.4 An 82fs_{rms}-Jitter and 22.5mW-Power, 102GHz W-Band PLL Using a Power-Gating Injection-Locked Frequency-Multiplier-Based Phase Detector in 65nm CMOS

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As the utilization of the mm-wave spectrum becomes active, designers' interests are shifting to even higher frequencies in the W-band. Given their potential use as carrier frequencies for the next-generation mobiles (i.e., beyond 5G), these W-band signals must have ultra-low phase noise (PN). Currently, the most popular solution to generate such frequencies is with a cascaded architecture: a first-stage PLL generates a low-PN signal at a relatively low frequency at which the VCO LC tank has a high Q factor, and following frequency multipliers (FMs) increase the frequency to the W-band [1]. Although various FMs have been proposed, all of them are limited in their ability to achieve a high multiplication factor, M . Push-push or harmonic-selection circuits have high conversion losses. Injection-locked FMs (ILFs) require multiple stages due to their narrow lock ranges, which increase power consumption and complexity. Thus, single-stage direct PLLs [2-4] would be preferred if they could have a sufficiently wide loop bandwidth to suppress the poor PN of a W-band VCO. Subsampling PLLs (SSPLLs) are suitable for extending the bandwidth since they have low in-band PN due to the high phase-error (ϕ_{ERR}) detection gain of a subsampling phase detector (PD). Nevertheless, when SSPLLs operate in the W-band, the degradation of PN is unavoidable because the ϕ_{ERR} detection gain decreases as the frequency of the VCO, f_{VCO} , increases. As described at the left of Fig. 23.4.1, when the switch of the PD, SW_{PD} , is closed, the output of the PD, S_{PD} , should track the signal of the VCO, S_{VCO} , closely. However, when f_{VCO} increases to the W-band, the amplitude of S_{PD} is reduced significantly by a parasitic pole that is present due to the turned-on resistance of SW_{PD} , R_{ON} , and the sampling capacitor, C_s . When SW_{PD} is turned off, ϕ_{ERR} is detected in S_{PD} , but its magnitude is already suppressed significantly relative to that in S_{VCO} . This effect also can be interpreted in the frequency domain where S_{VCO} is suppressed by a low-pass filter before the information of ϕ_{ERR} is extracted at the baseband frequencies.

In this paper, we present a direct W-band PLL with an ultra-low PN using a power-gating ILFM (PG-ILFM)-based PD that can maintain a high ϕ_{ERR} -detection gain even when f_{VCO} is very high (right part of Fig. 23.4.1). The key idea is to convert the information of ϕ_{ERR} to the baseband before it is reduced by the parasitic pole. To do so, first, the PG-ILFM of the proposed PD generates S_{ILFM} that periodically has the targeted frequency, i.e., $M \cdot f_{\text{REF}}$, where f_{REF} is the frequency of the reference clock, S_{REF} . In the PG-ILFM, the replica VCO (R-VCO) is turned on and off repeatedly by S_{REF} so that its phase errors can be completely reset at f_{REF} [5]. Since this mechanism induces a strong injection locking, different from typical ILFs, the PG-ILFM can be easily locked to the targeted high-order harmonic of f_{REF} (e.g. $M \geq 200$), and its lock range can reach the theoretical maximum. Then, by mixing this S_{ILFM} with S_{VCO} , the detected ϕ_{ERR} at the baseband S_{PD} can maintain its original magnitude so that the PG-ILFM PD can have a high ϕ_{ERR} detection gain. As this high ϕ_{ERR} detection gain suppresses the in-band noise of the following loop building blocks, we can have a wide bandwidth of the PLL that can suppress the poor PN of the W-band LC VCO significantly. Since the S_{ILFM} is discontinuous and available only during ϕ_1 , it cannot be an output signal by itself, but it can be used to detect a ϕ_{ERR} in the main VCO (M-VCO) that generates a continuous and low-jitter S_{VCO} .

Figure 23.4.2 shows the overall architecture of the proposed W-band PLL. After the PG-ILFM-based PD, the resampler is used to transfer only the meaningful information of ϕ_{ERR} to the following g_m amplifier. The bottom left of Fig. 23.4.2 shows that, while the R-VCO is turned off (ϕ_2), $S_{\text{PD}+}$ and $S_{\text{PD}-}$ float and have meaningless information. However, using a window signal, S_{WIN} , the resampler generates $S_{\text{RS}+}$ and $S_{\text{RS}-}$, which are the refined versions of $S_{\text{PD}+}$ and $S_{\text{PD}-}$, respectively. In the frequency domain, the role of the resampler can be understood to suppress spurs at the multiples of f_{REF} . The g_m amplifier generates current-carrying charges that are proportional to the difference between $S_{\text{RS}+}$ and $S_{\text{RS}-}$. Then, the control voltage, V_c , is adjusted in the direction of removing ϕ_{ERR} . A background frequency-offset canceller (FOC) was designed to remove the frequency offset of the R-VCO relative to the M-VCO, preventing the possible degradation of jitter due to this offset. The operation of the FOC is explained in Fig. 23.4.3. The bottom right of Fig. 23.4.2 shows the noise-transfer functions (NTFs) of the main building blocks and their noise contributions to S_{OUT} . The NTF of the M-VCO ($\phi_{\text{OUT}}/\phi_{\text{M-VCO}}$) is a high-pass filter with a cutoff frequency at the bandwidth of the PLL,

$f_{\text{BW,PLL}}$. However, the NTF of the R-VCO ($\phi_{\text{OUT}}/\phi_{\text{R-VCO}}$) is a bandpass filter since it is high-pass filtered by the PG-ILFM and also low-pass filtered by the PLL. Since the bandwidth of the PG-ILFM, $f_{\text{BW,ILFM}}$, is much larger than $f_{\text{BW,PLL}}$, the gain in the passband is very low; thus, only the M-VCO affects the overall PN. Due to a high ϕ_{ERR} detection gain, the noise contributions of the PD, the resampler, and the g_m amplifier are also negligible. This analysis corresponds to the measurement results in which the in-band PN was determined by the PN of S_{REF} , while the skirt was determined by the PN of the M-VCO.

Figure 23.4.3 shows the schematics of the VCOs. In the PG-ILFM, the injection of S_{REF} to the tail transistor periodically turns the R-VCO on and off, making $S_{\text{ILFM}\pm}$ locked to the target W-band frequency, $M \cdot f_{\text{REF}}$. To help the R-VCO restart quickly to minimize the start-up time that is very sensitive to noise, a short pulse of S_{REF} is injected into $S_{\text{ILFM}+}$ through an NMOS. The potential causes of the mismatch between the M-VCO and the R-VCO, such as parasitic capacitances, signal lines, and shielding layers, were carefully addressed during the design and layout. Inevitable mismatches remaining despite these efforts can be removed by the proposed FOC. The bottom left of Fig. 23.4.3 shows the mechanism of the FOC. Since the bandwidth of the PLL is much wider than that of the FOC, the frequency of the M-VCO, f_{OUT} , can be locked to $M \cdot f_{\text{REF}}$ before the offset is removed. When the free-running frequency of the R-VCO, $f_{\text{R-VCO}}$, has an offset from f_{OUT} , the relative phases of S_{ILFM} with respect to S_{OUT} are changing during ϕ_1 . However, after the offset is removed by controlling $V_{c,\text{ILFM}}$, these relative phases become constant as the peaks of S_{ILFM} are aligned with the mid-points of S_{OUT} at which the slope is the highest. The simulation results at the bottom right of Fig. 23.4.3 compare the ϕ_{ERR} detection gain of the PG-ILFM PD with that of a conventional SSPD. It shows that, without the loss by the parasitic pole, the PG-ILFM PD can have a much higher ϕ_{ERR} detection gain.

The proposed direct W-band PLL in 65nm CMOS consumes 22.5mW of power when generating a 102GHz f_{OUT} with a 500MHz f_{REF} . Figure 23.4.4 shows the PN of S_{OUT} at 102GHz ($M = 204$) along with the PN of the free-running M-VCO. For accurate measurements, the PNs were measured at 34GHz using an on-chip divide-by-3 test divider. Due to the wide bandwidth of the PLL that can reduce the poor PN of the W-band VCO and the high gain of the PG-ILFM-based PD that can suppress the in-band PN of the loop building blocks, a very low rms jitter was achieved, i.e., 82fs integrated from 1kHz to 300MHz. When f_{OUT} was restored to 102GHz, the 1MHz PN was -104.3dBc/Hz . The bottom of Fig. 23.4.4 shows two spectra of S_{OUT} : one was measured directly at 102GHz by on-chip probing, and the other was measured via the test divider. The top of Fig. 23.4.5 shows that the FOC was able to make the PLL maintain a wide bandwidth and an ultra-low jitter by removing the frequency offset between the two VCOs. The bottom of Fig. 23.4.5 shows that this W-band PLL achieved a low jitter consistently across f_{OUT} s. Among designs shown in the table in Fig. 23.4.6, this work achieved the lowest 1MHz PN and the best jitter FoM. It also used the smallest active area due to its one-stage direct PLL architecture requiring no ILFD at the feedback path.

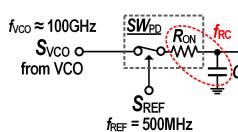
Acknowledgement:

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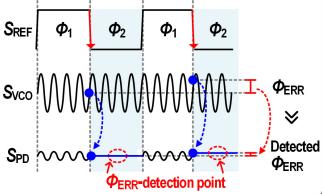
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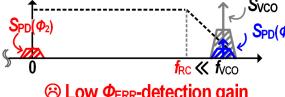
Conventional W-band Sub-sampling PD



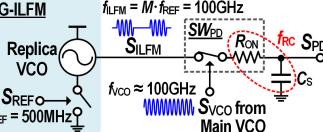
Interpretation in Time Domain



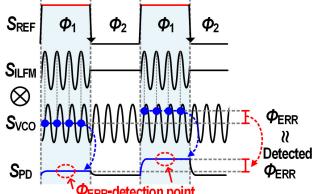
Interpretation in Frequency Domain



Proposed W-band PG-ILFM-based PD



Interpretation in Time Domain

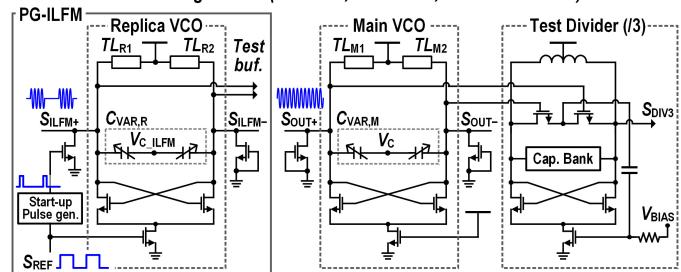


Interpretation in Frequency Domain



Figure 23.4.1: Conceptual diagrams and interpretations of the conventional W-band sub-sampling PD (left); and the proposed W-band PG-ILFM-based PD (right).

Schematics of Building Blocks (PG-ILFM, Main VCO, and Test Divider)



Mechanism of Freq. Offset Canceller (FOC)

f _{OUT} is locked to M·f _{REF} (\because BW _{PLL} >> BW _{FOC})	
f _{R-VCO} < f _{OUT}	f _{R-VCO} = f _{OUT}
S _{REF}	Φ ₁ Φ ₂ Φ ₁ Φ ₂
S _{ILFM}	Wavy waveforms
S _{OUT}	Wavy waveforms with I > 0
V _{C_{ILFM}}	↑

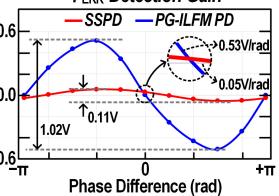
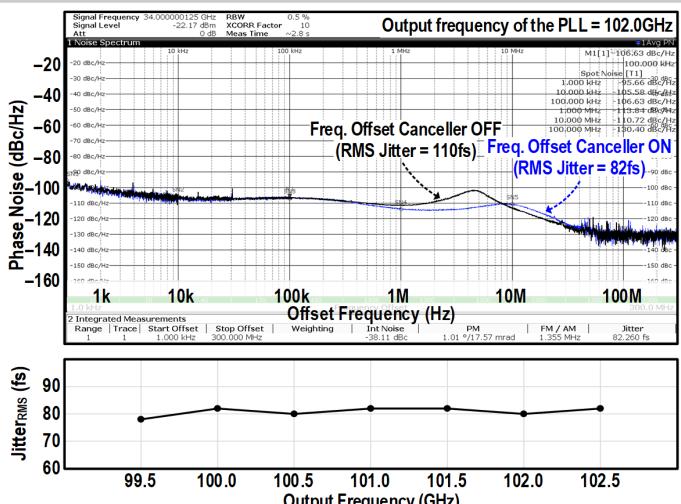
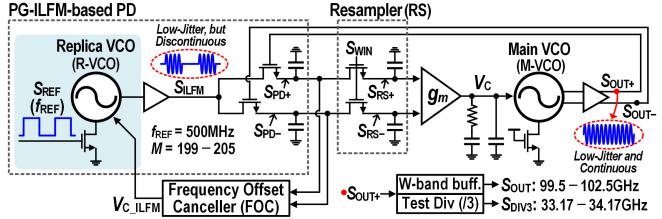
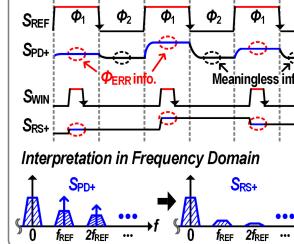
Φ_{ERR}-Detection GainFigure 23.4.3: Schematics of the PG-ILFM, the main VCO, and the test divider (top); the detection mechanism of the frequency offset canceller, and the ϕ_{ERR} detection gain of the PD (bottom).

Figure 23.4.5: Measured phase noise of the 102.0GHz output signal (measured at 34.0GHz using the on-chip divide-by-3 test divider) when the frequency offset canceller was turned on and off (top); measured rms jitter across different output frequencies (bottom).

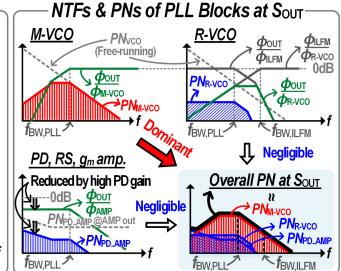
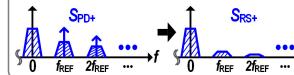
Proposed W-band PLL with PG-ILFM-based PD



Effect of Resampler



Interpretation in Frequency Domain

Figure 23.4.2: Overall architecture of the proposed W-band PLL with a PG-ILFM-based PD (top); the effect of the resampler, and NTFs and PNs of PLL blocks at S_{OUT} (bottom).

Output frequency of the PLL = 102.0GHz

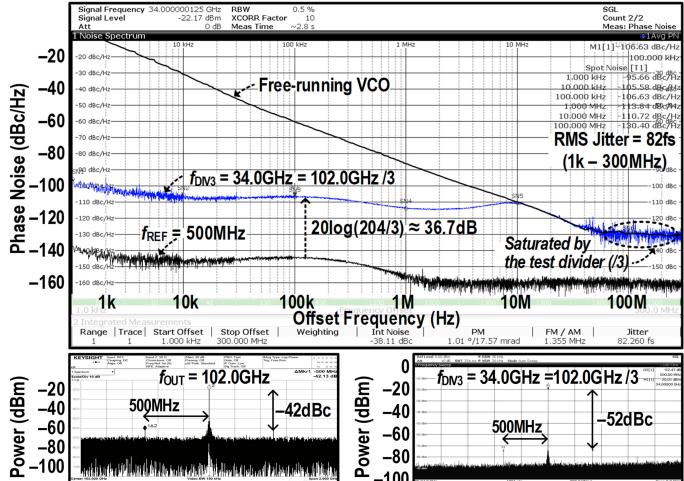
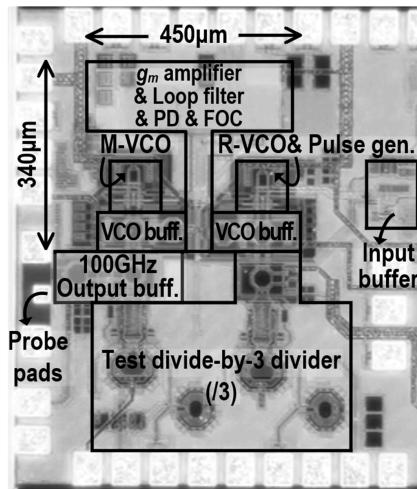


Figure 23.4.4: Measured phase noises of the 102.0GHz output (measured at 34.0GHz using the on-chip divide-by-3 test divider), the free-running of the M-VCO, and the reference clock (top); and the spectra of the 102.0GHz-output signal using an on-chip probe and the on-chip test divider (bottom).

	This work	ISSCC'09 [2] K. Tsai	TMTT'14 [3] S. Kang	ISSCC'18 [4] Z. Huang	RFIC'14 Y. Chao	VLSI'19 [1] X. Liu
Process	65nm CMOS	65nm CMOS	130nm SiGe	65nm CMOS	65nm CMOS	65nm CMOS
Architecture	PG-ILFM-based PD Direct W-band PLL	Direct W-band PLL	Direct W-band PLL	50GHz PLL + Push-push(x2) + ILFM (x4)	23GHz PLL + Push-push(x2) + ILFM (x4)	
Type	Integer-N	Integer-N	Integer-N	Integer-N	Integer-N	Integer-N
Supply (V)	1.2/0.8	1.2	3.3/2.5/1.2	1.2/0.8	1.2/0.6	N/A
Output Freq. f _{OUT} (GHz)	99.5 to 102.5	95.1 to 96.5	92.7 to 100.2	82.0 to 107.6	96.8 to 108.5	80.0 to 104.0
Reference Freq. f _{REF} (MHz)	500	375	1500	125	195	100
Multiplication Factor (M)	199 to 205	256	64	656 to 864	512	800 to 1040
Reference Spur (dBc)	-42	-52	< -60	< -34	-40	-40
1MHz PN (dBc/Hz) @ f _{OUT} (GHz)	-104.3 @ 102	-75.7 @ 95.5	-102.0 @ 95.0	-79.0 @ 107.6	-88.0 @ 99.4	-93.0 @ 100.8
Jitter _{rms} , σ _t (fs)	82 (1k to 300MHz)	2220 (1k to 10MHz)	71 (1M to 1GHz)	278 (1k to 10MHz)	170* (10k to 10MHz)	137 (10k to 10MHz)
Power, P _{Dc} (mW)	22.5	43.7	469.3	35.5	14.1	23.6**
Active Area (mm ²)	0.16	0.70	0.93	0.36	0.39	0.41**
FOM _{JIT} *** (dB)	-248.2	-216.7	-236.2	-235.6	-243.8	-243.5

*Calculated from the PN graph in Fig. 8 of [RFIC'14, Y. Chao] **Power and area only for the W-band ***FOM_{JIT} = 10log(σ²·P_{Dc})

Figure 23.4.6: Performance comparisons with prior-art W-band frequency synthesizers.



Power Consumption (mW)	
M-VCO	8.0
R-VCO	4.5
g_m amplifier & PD & FOC	2.0
VCO buffers	7.0
Start-up Pulse gen.	1.0
Total	22.5

Figure 23.4.7: Die micrograph and power breakdown. The power of the R-VCO is approximately half that of the M-VCO due to its 50%-duty-cycle operation.