

Non-Magnetic $0.18\mu\text{m}$ SOI Circulator with Multi-Watt Power Handling Based on Switched-Capacitor Clock Boosting

**Aravind Nagulu, Tingjun Chen, Gil Zussman,
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Columbia University, New York, NY



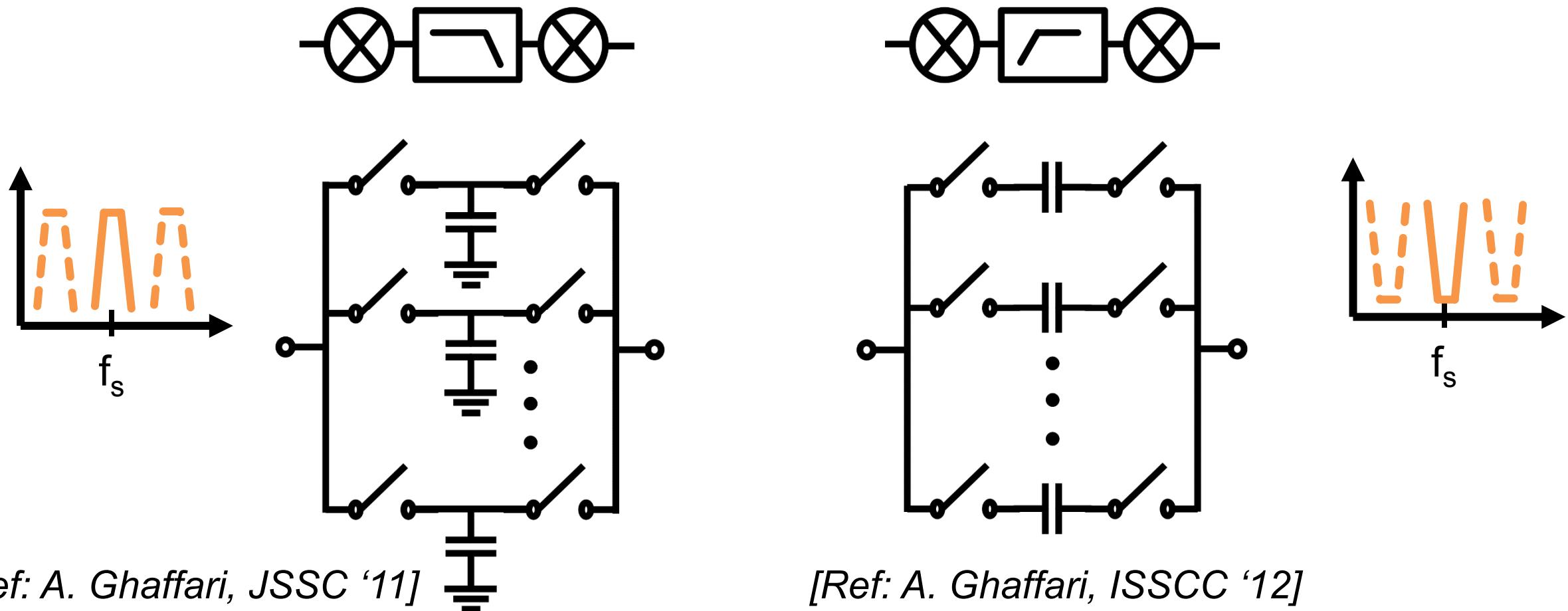
Overview

- Introduction
- Switched-Capacitor Clock Boosting
- Magnetic-Free Circulator Architecture
- Measurements
- Full-Duplex Wireless Link
- Conclusion

Overview

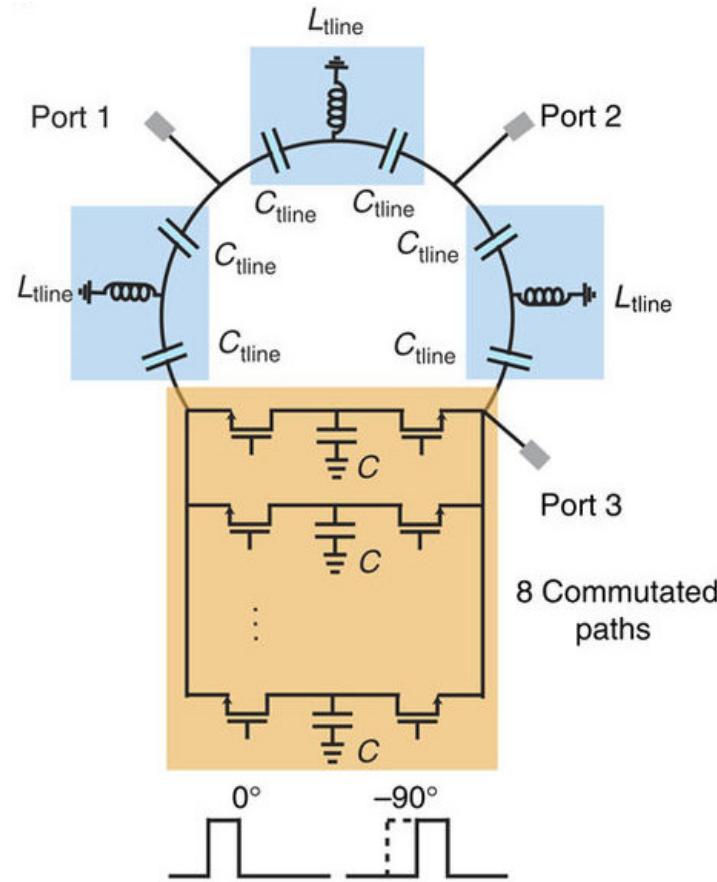
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N-Path Bandpass/Notch Filters

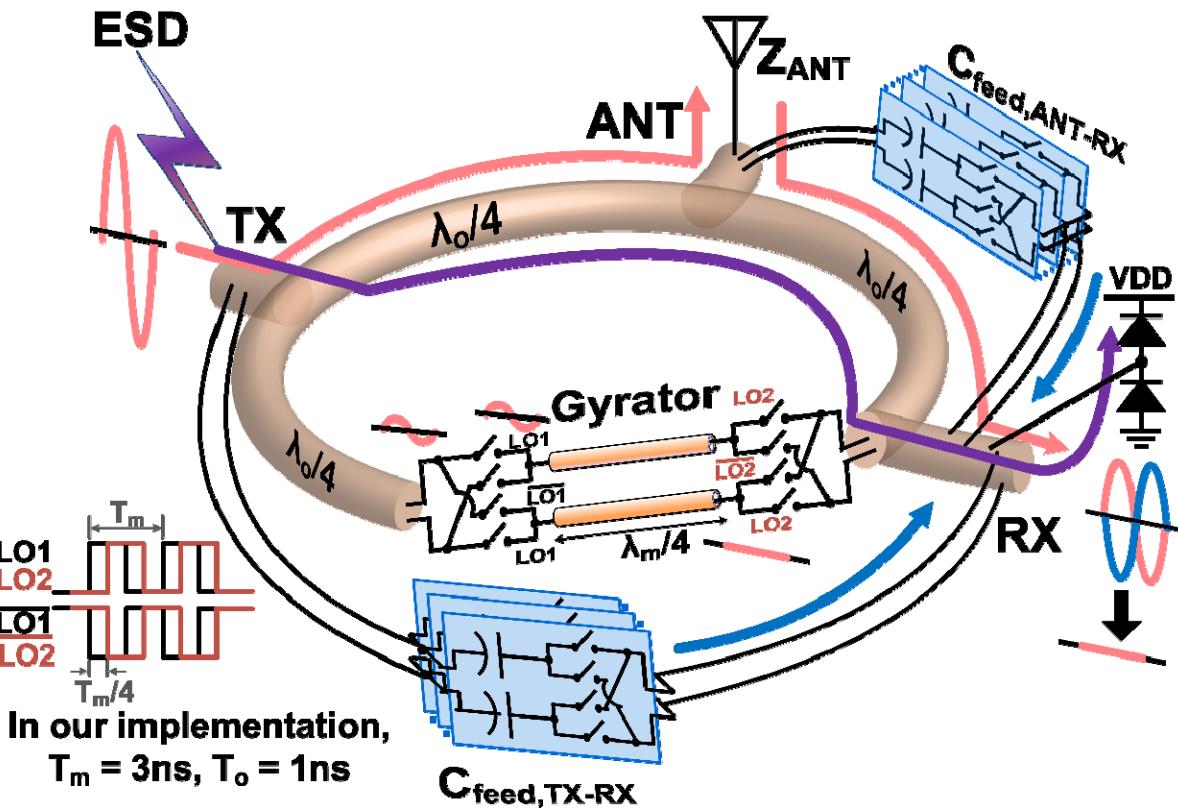


N-Path switched capacitors networks provide wide range of tunable filters in a compact form factor

Non-Magnetic CMOS Circulators



[Ref: N. Reiskarimian, ISSCC '16]

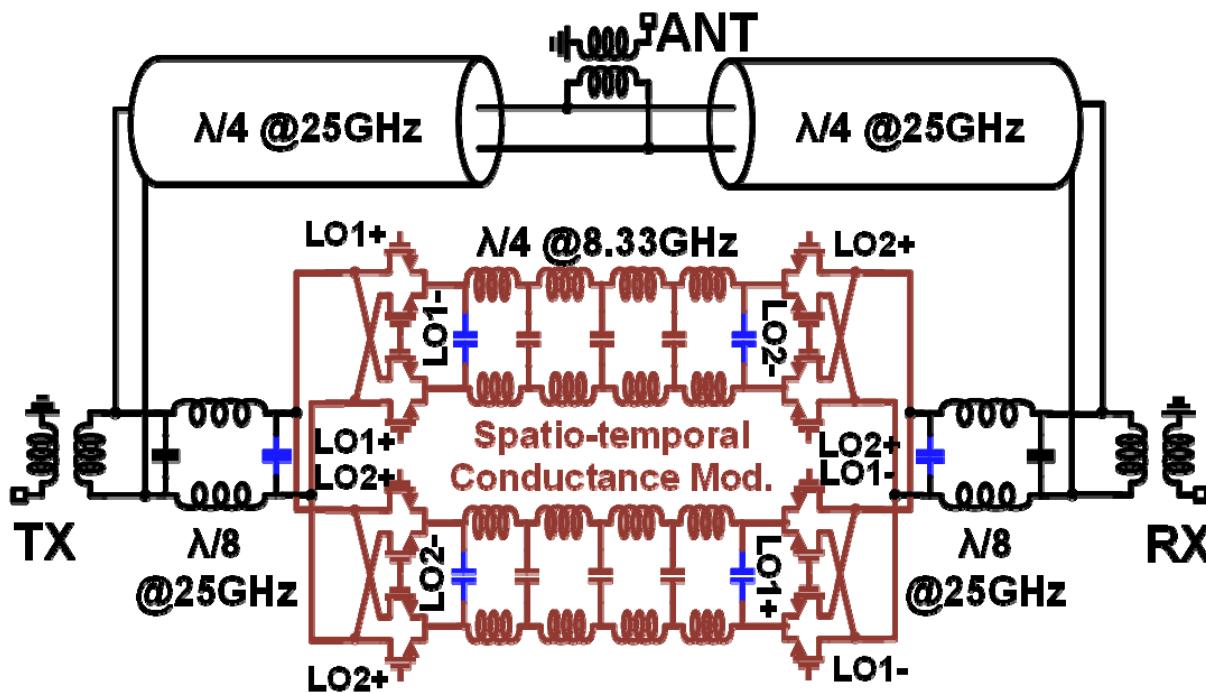


[Ref: A. Nagulu, RFIC '18]

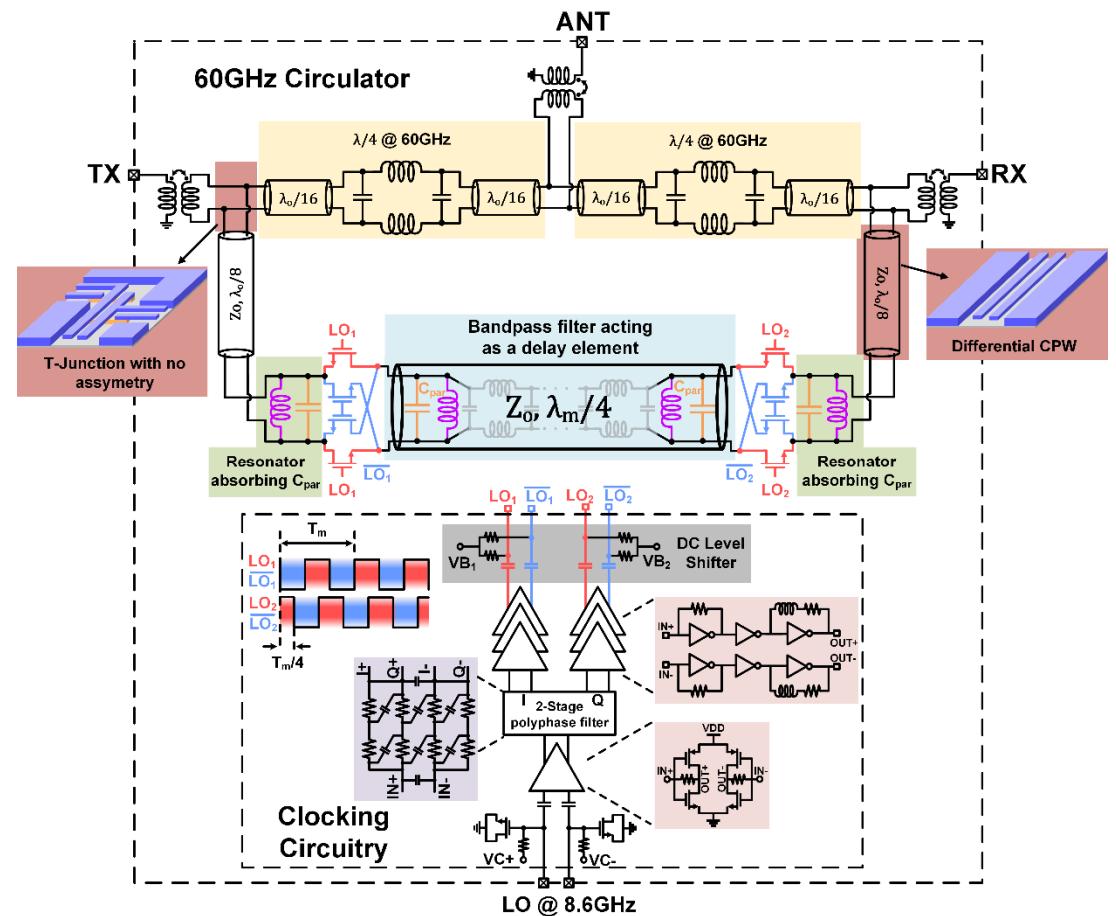
*Best Paper Award 1st Place

Switched capacitor and switched-transmission line circuits enabled CMOS integrated non-reciprocal circulators at RF.

Non-Magnetic LPTV CMOS Circulators



[Ref: T. Dinc, ISSCC '17]

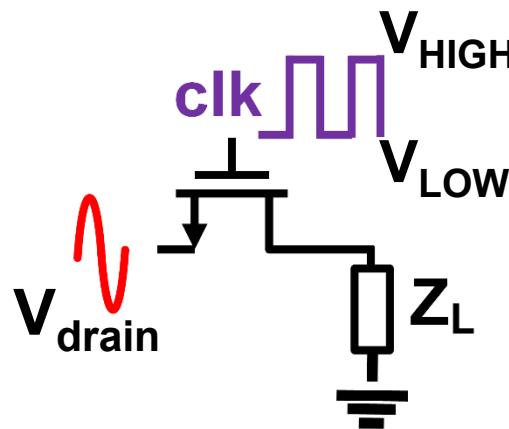


[Ref: A. Nagulu, ISSCC '19]

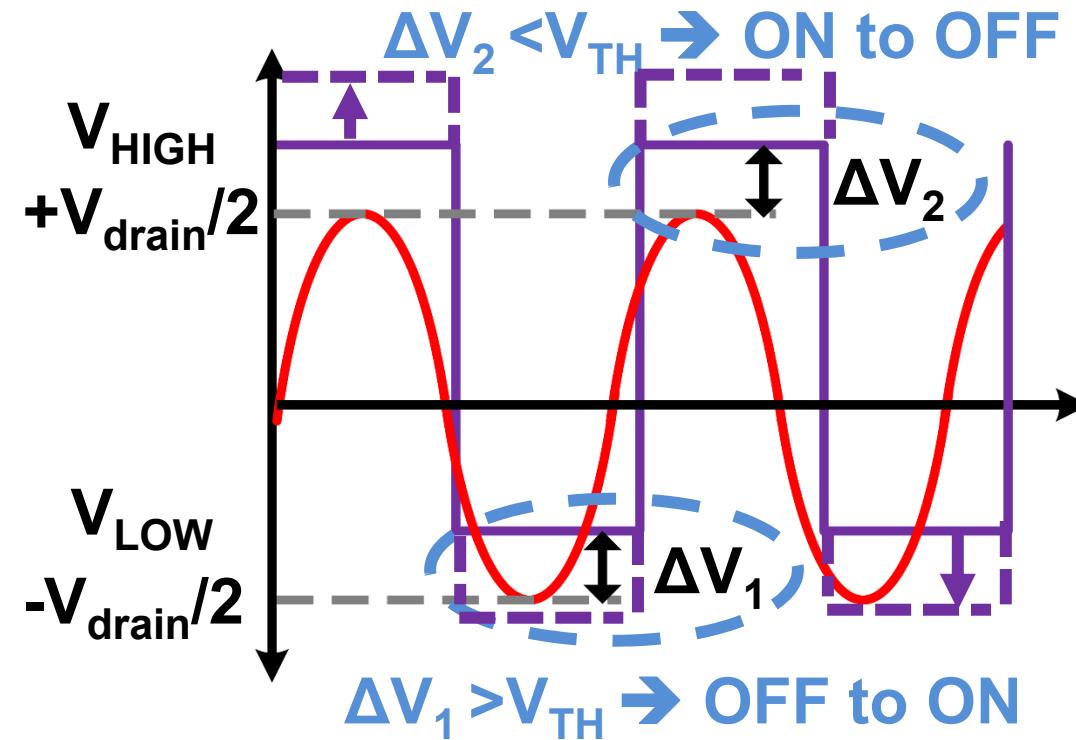
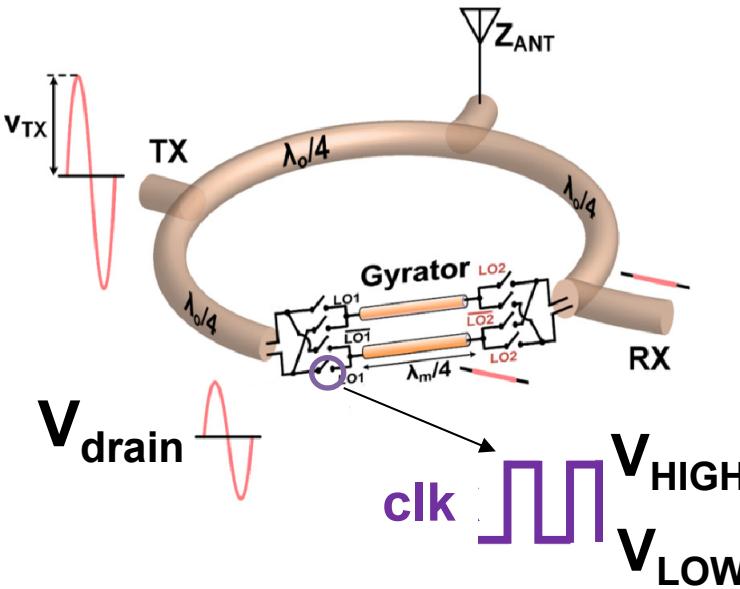
Switched-transmission line and switched-BPF circuits
enabled CMOS integrated millimeter-wave circulators.

Power Handling Limitation in Switches

N-Path Filters & Passive Mixers



CMOS Circulators

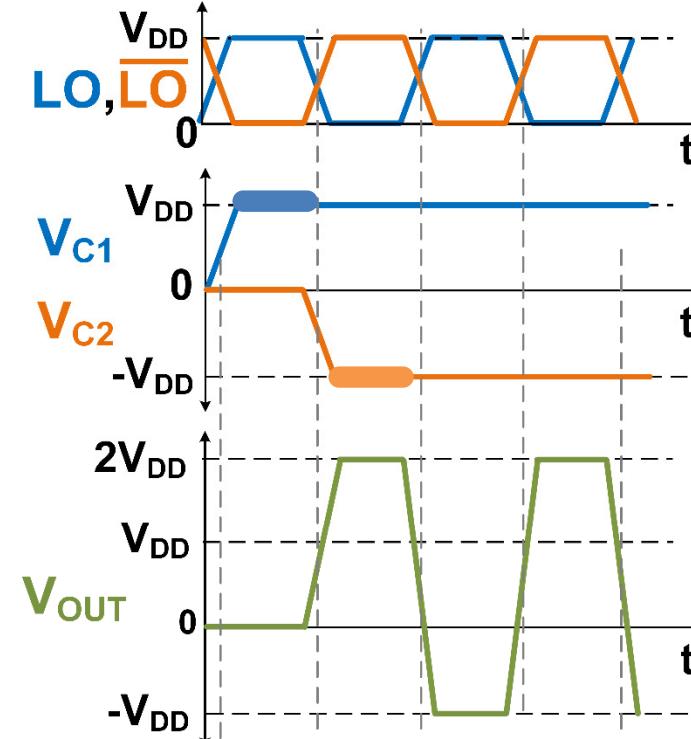
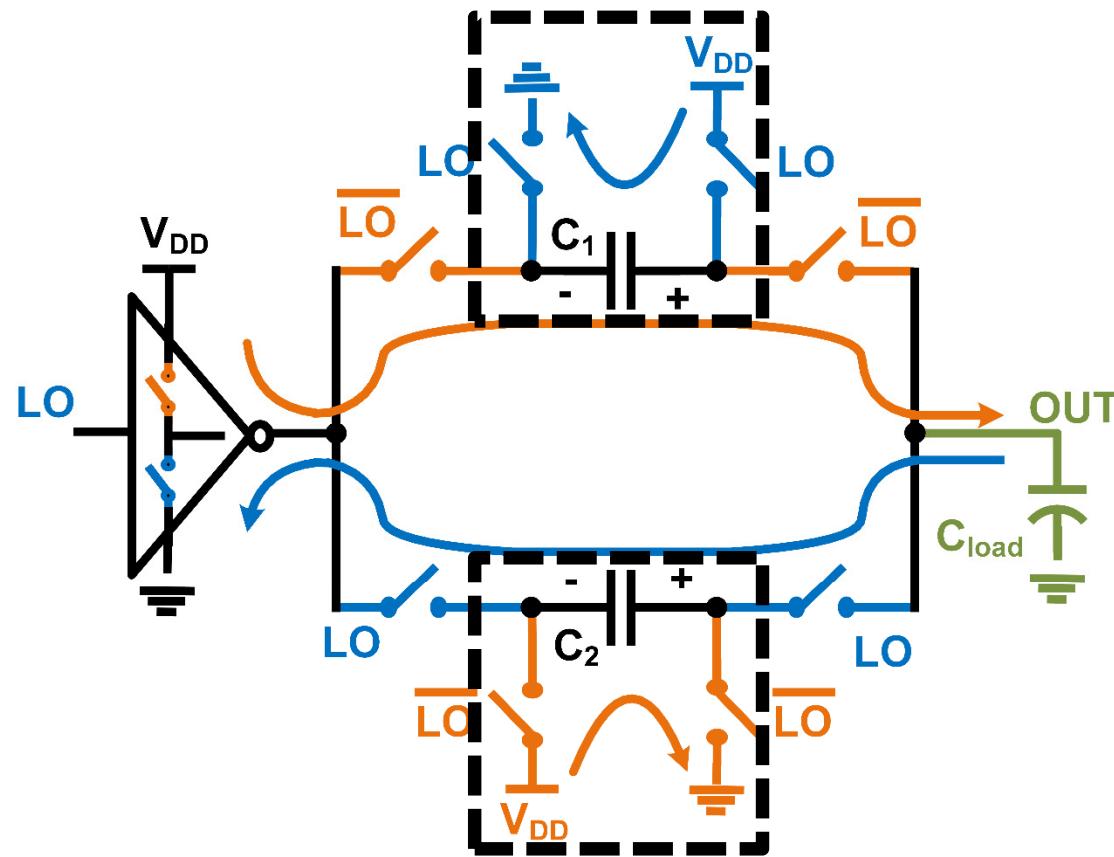


- \uparrow Power handling: $\uparrow V_{HIGH}$ and $\downarrow V_{LOW} \rightarrow \uparrow$ Supply Voltage
- Driver power consumption \propto (Supply Voltage) 2
- Voltage difference between any two terminals should be $< 2V_{DD}$

Overview

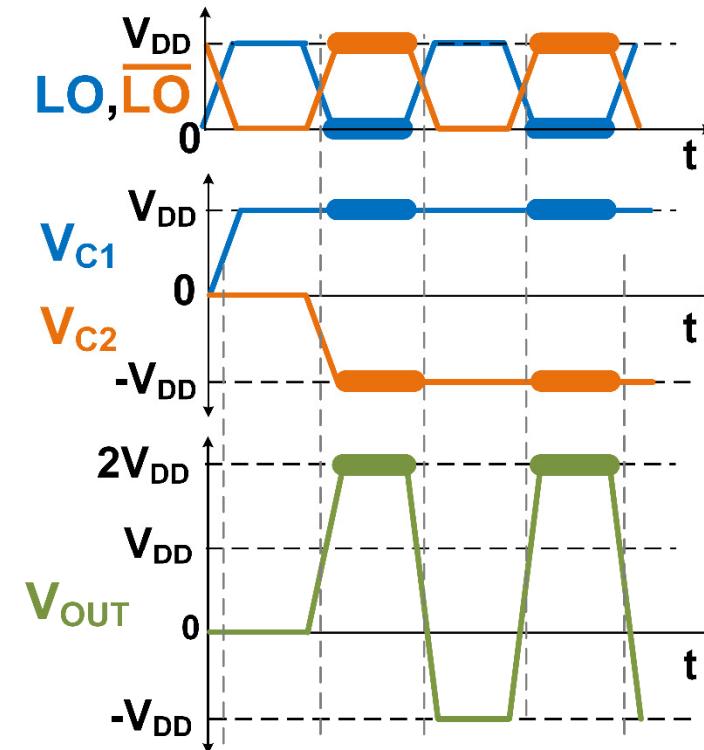
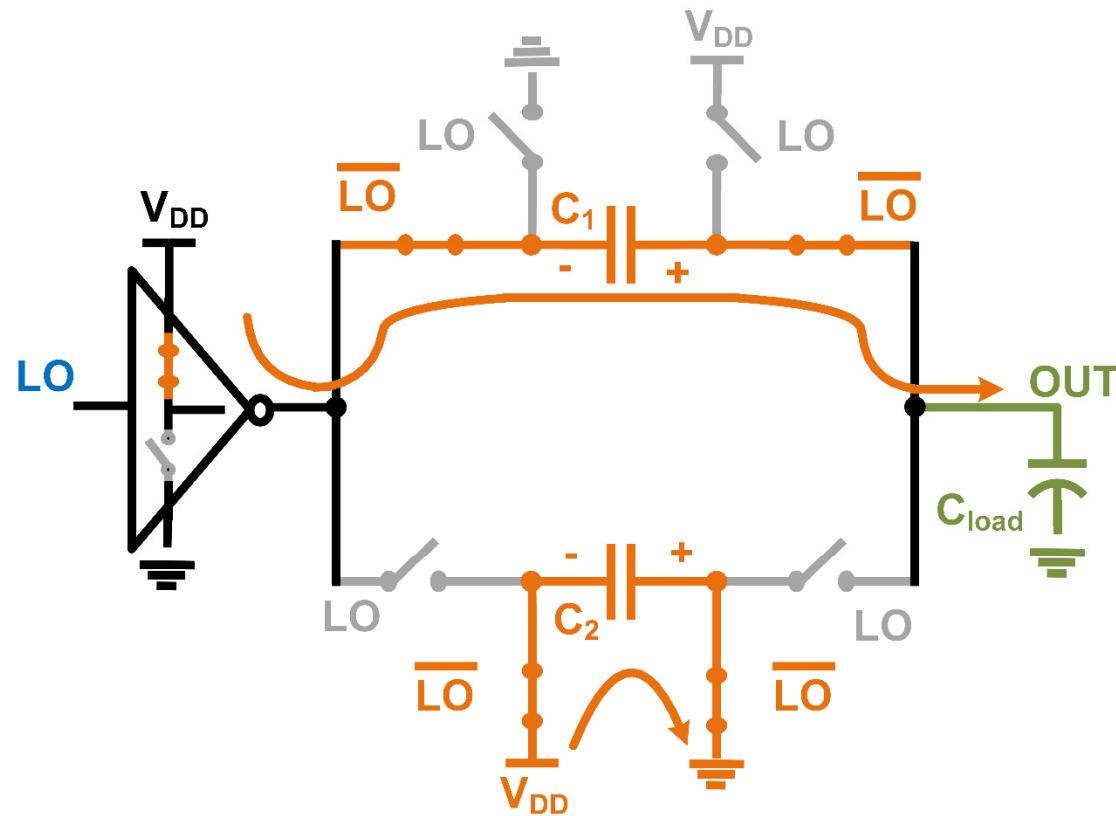
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Switched-Capacitor Clock Boosting



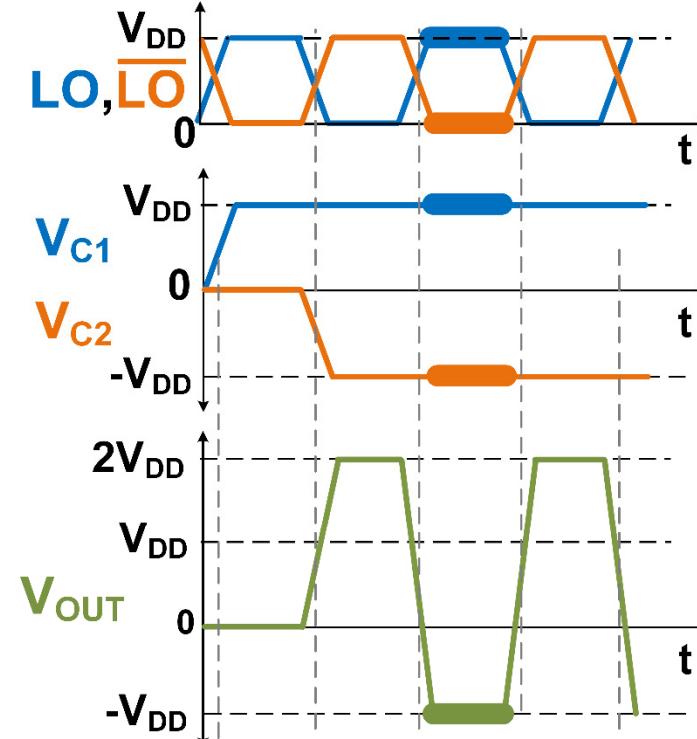
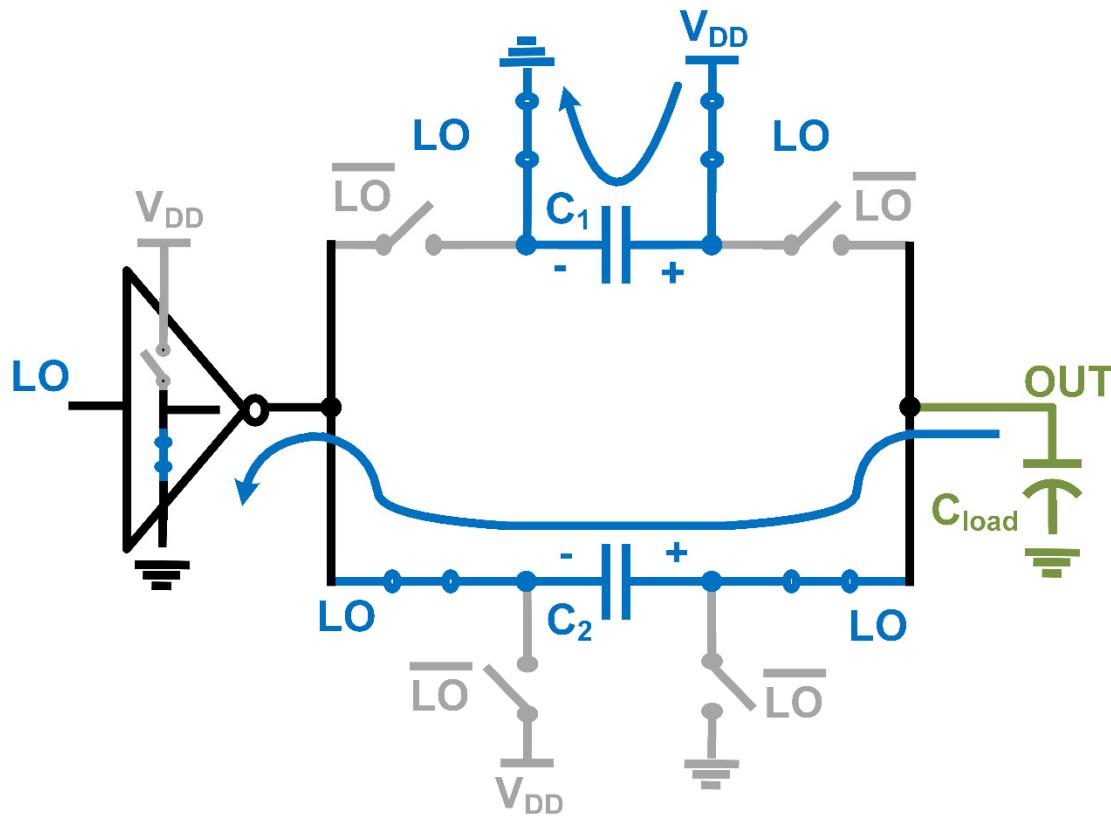
- Concept diagram of the switched-capacitor clock boosting technique providing 3x clock voltage swing.
- Capacitors C_1 and C_2 are charged to $+V_{DD}$ and $-V_{DD}$ respectively.

Circuit Operation: LO is LOW



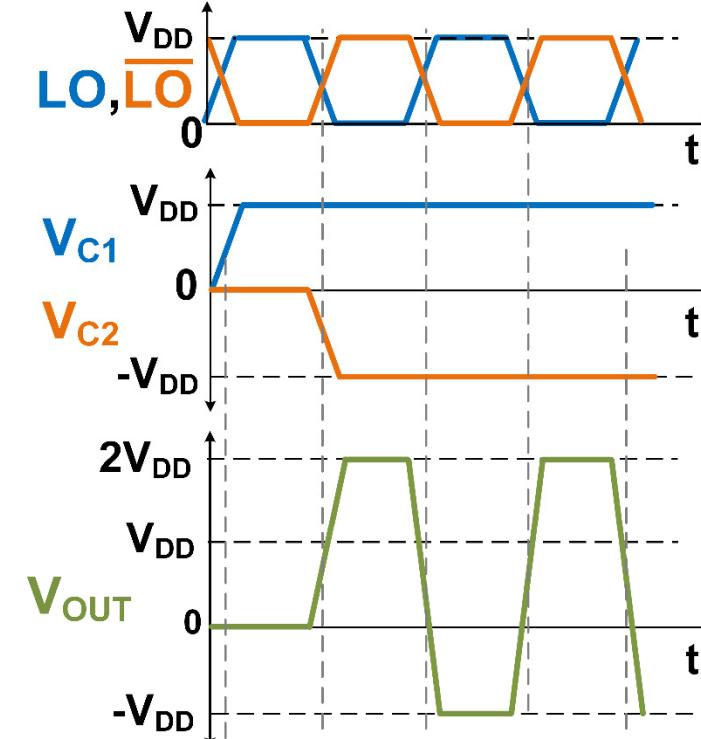
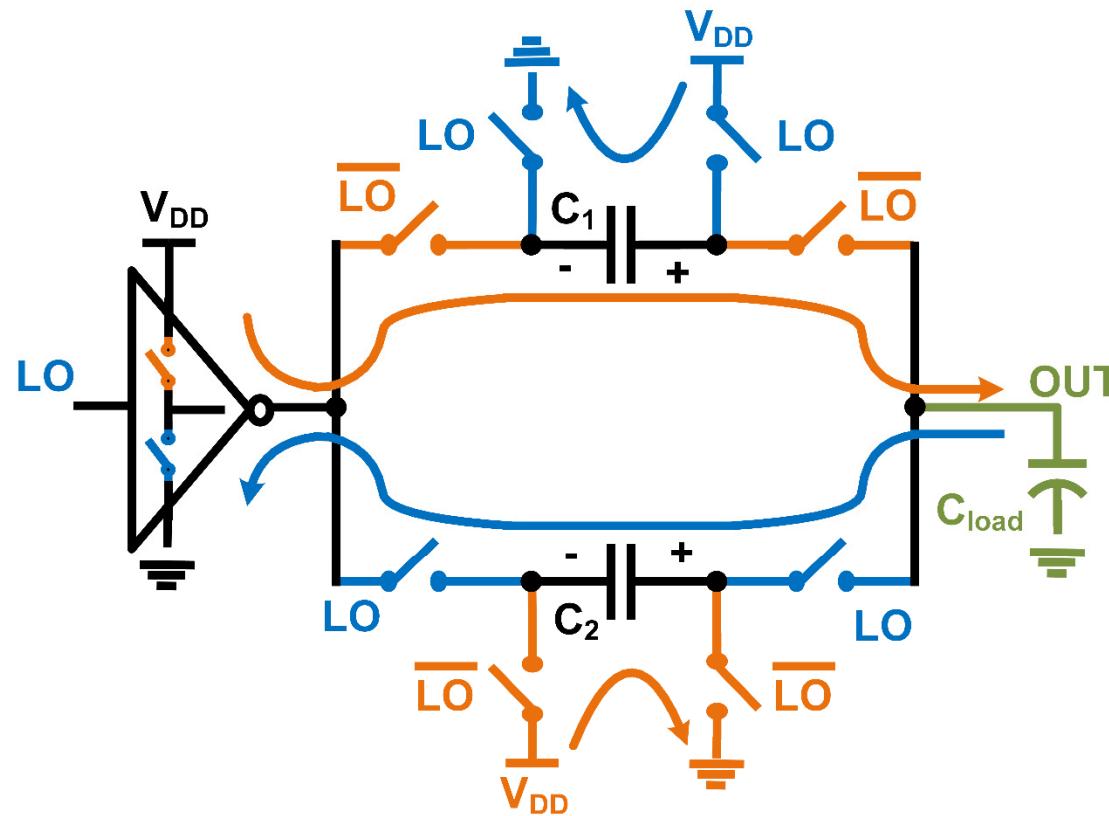
$$V_{load}(t) = \overline{LO}(t) + V_{C1}(t) \times \left(\frac{\overline{LO}(t)}{V_{DD}} \right) + V_{C2}(t) \times \left(\frac{LO(t)}{V_{DD}} \right)$$

Circuit Operation: LO is High



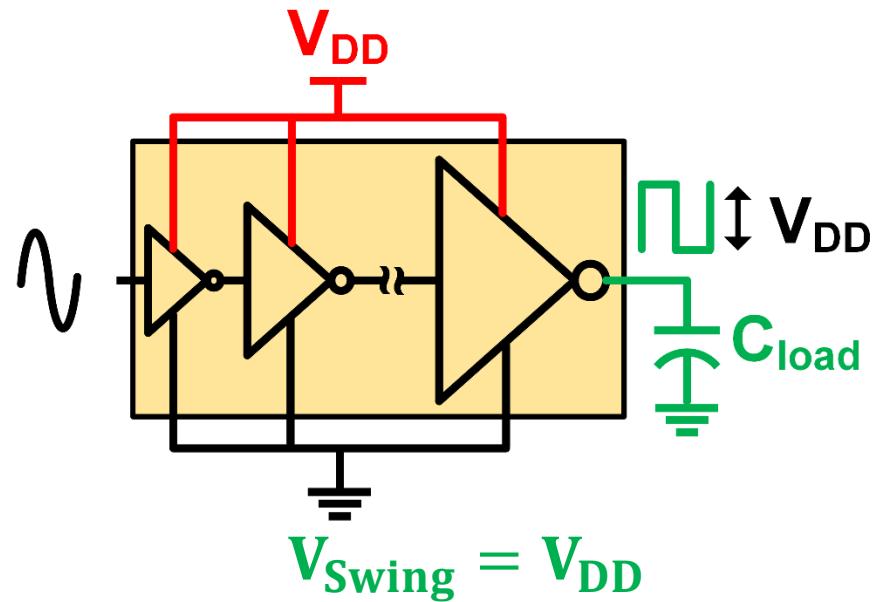
$$V_{load}(t) = \overline{LO}(t) + V_{c1}(t) \times \left(\frac{\overline{LO}(t)}{V_{DD}} \right) + V_{c2}(t) \times \left(\frac{LO(t)}{V_{DD}} \right)$$

Switched-Capacitor Clock Boosting



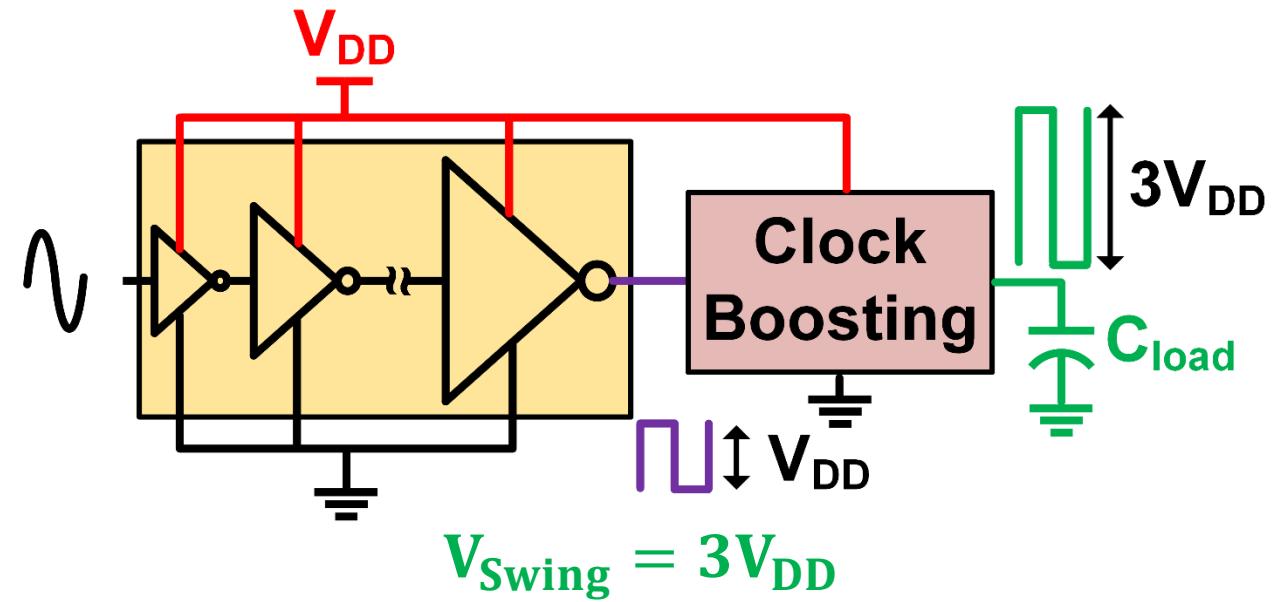
Switched-capacitor clock boosting technique generated a clock swing of $3V_{DD}$ from a driver supply voltage of V_{DD} .

Comparison of Power Consumption



Clock path with fanout of 2

$$P_{DC} \sim \underbrace{f_{clk} V_{swing}^2 C_{LOAD}}_{P_{Drive}} + \underbrace{f_{clk} V_{swing}^2 C_{LOAD}}_{P_{Load}}$$

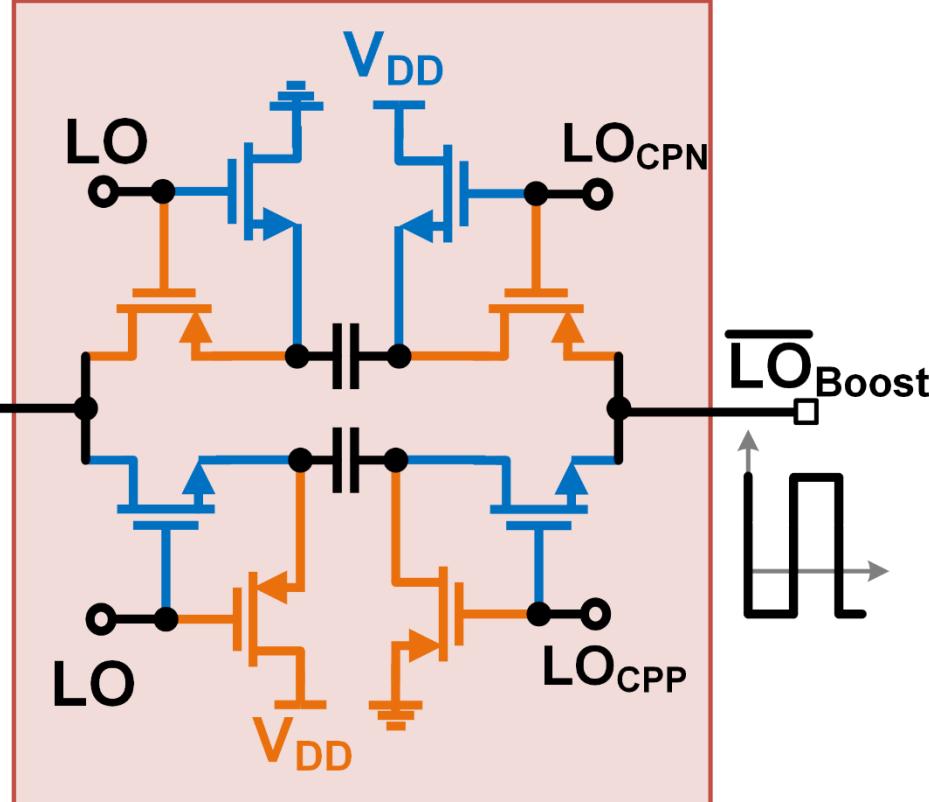
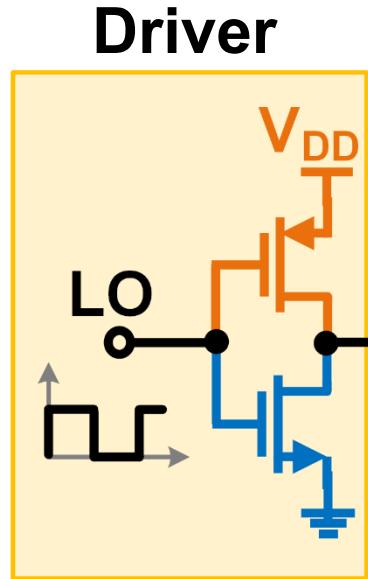


$$P_{DC} \sim \underbrace{\frac{f_{clk} V_{swing}^2 C_{LOAD}}{9}}_{P_{Drive}} + \underbrace{f_{clk} V_{swing}^2 C_{LOAD}}_{P_{Load}}$$

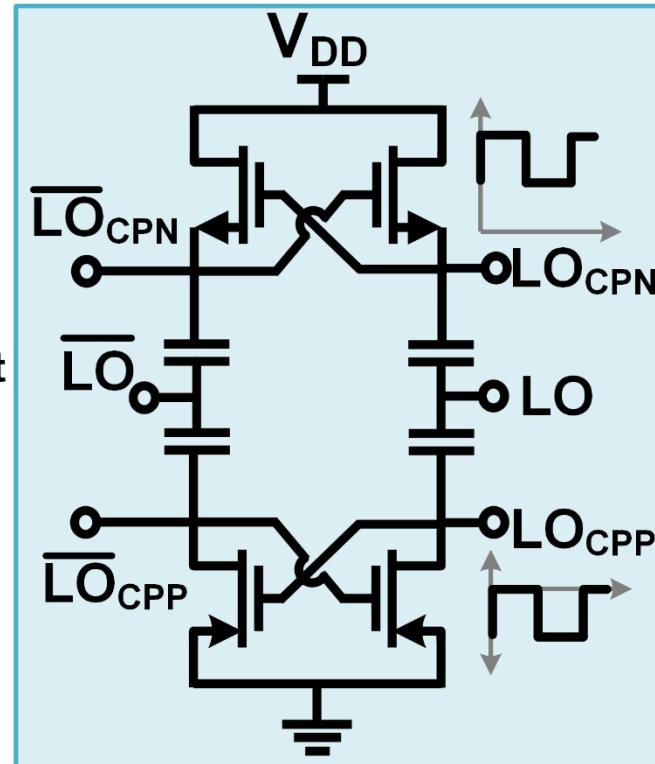
Clock boosting reduces the clocking power consumption by ~45% in a clock path design with fanout of 2 for same V_{swing} .

Circuit Diagram

Clock Boosting Circuit



Level Shifters

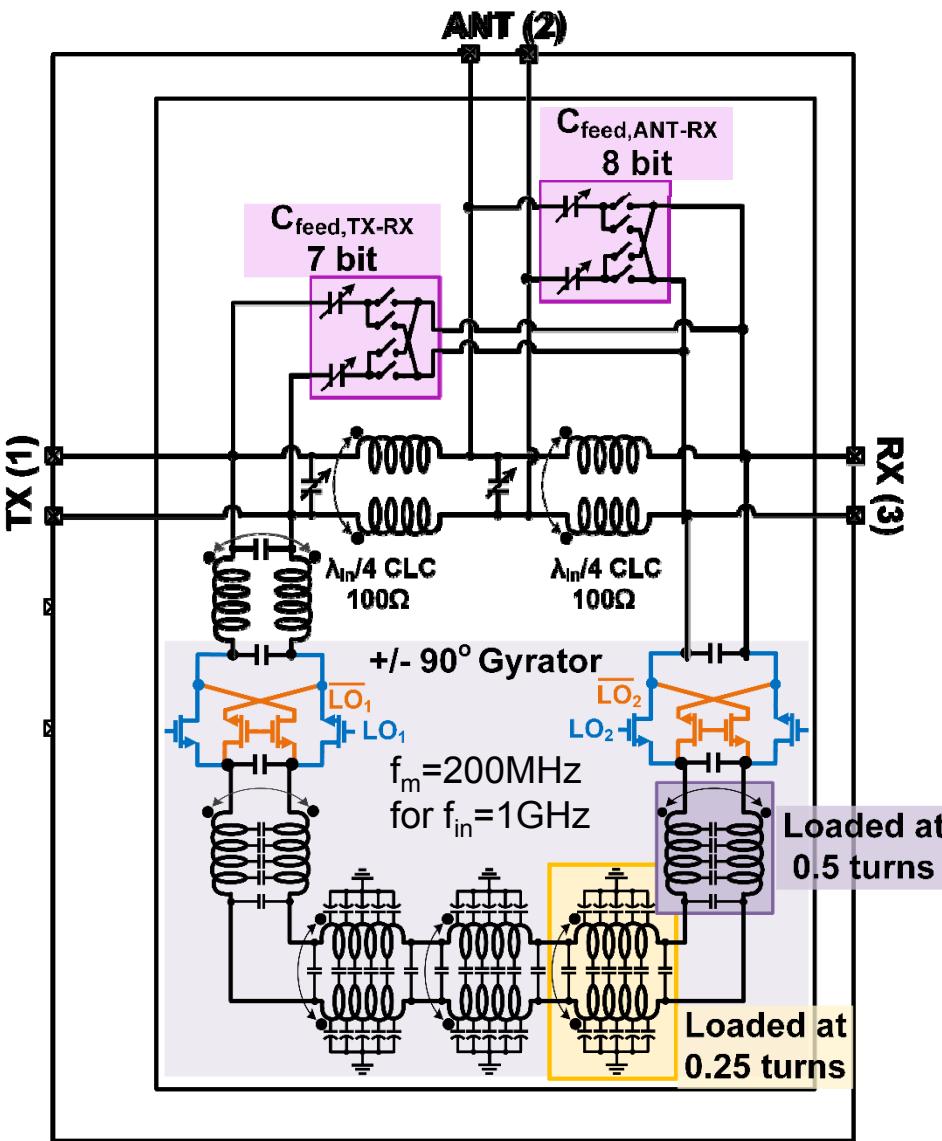


- Voltage difference between any two terminals is $<2V_{DD}$
- Minimal degradation in the rise/fall time
- Inbuilt level shifters were designed to generate the level shifted gate drives

Overview

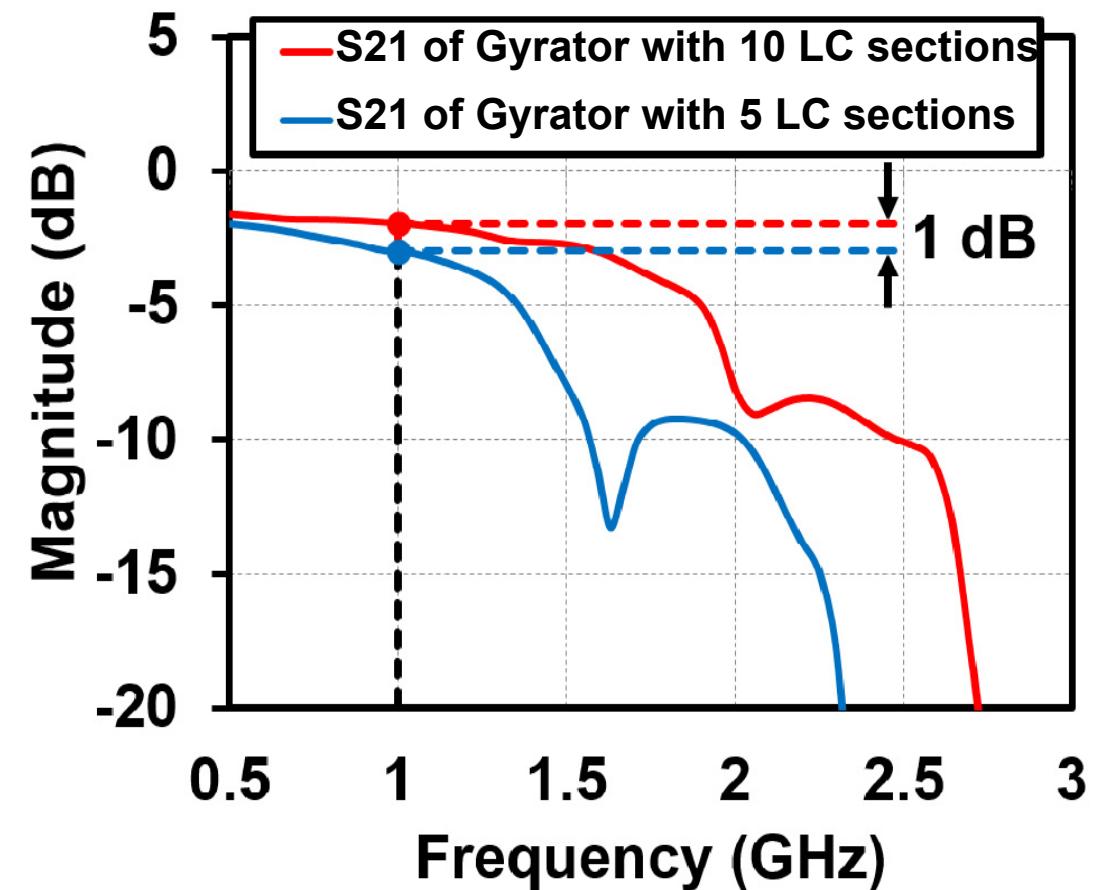
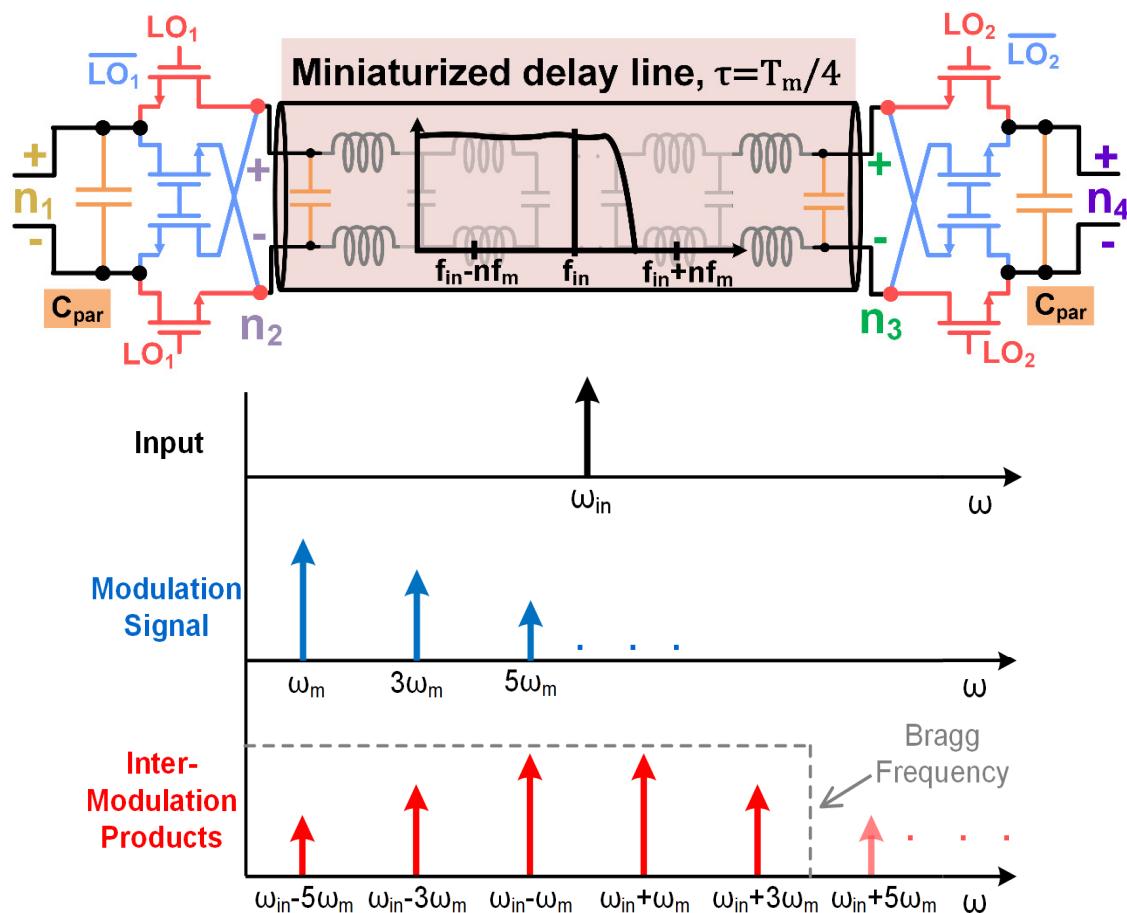
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2.5W, 1GHz CMOS Circulator Core



- LPTV gyrator based on **partially-reflecting switched-transmission** lines.
- The t-line in the gyrator is miniaturized using **5 periodically loaded inductors** to enable compact form-factor.
- For 1GHz modulation, gyrator switches are modulated at **200MHz to save power consumed**.
- The $3\lambda/4$ line is miniaturized using 3-CLC π -sections.
- Tunable I/Q capacitors enable **VSWR coverage**.

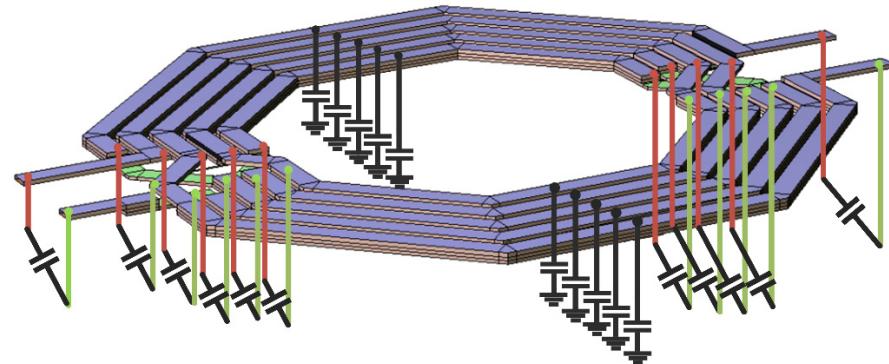
Losses Due to T-line Miniaturization



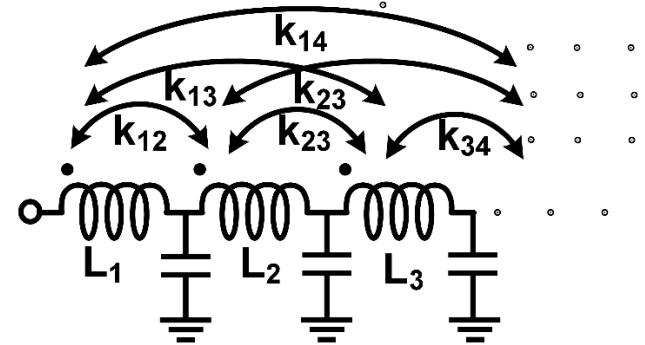
- Cut-off frequency of t-line filters higher modulation products, resulting in loss.
- **Area $\propto 1/\text{Insertion Loss}$.**

Multi-Turn Periodically Loaded Inductors

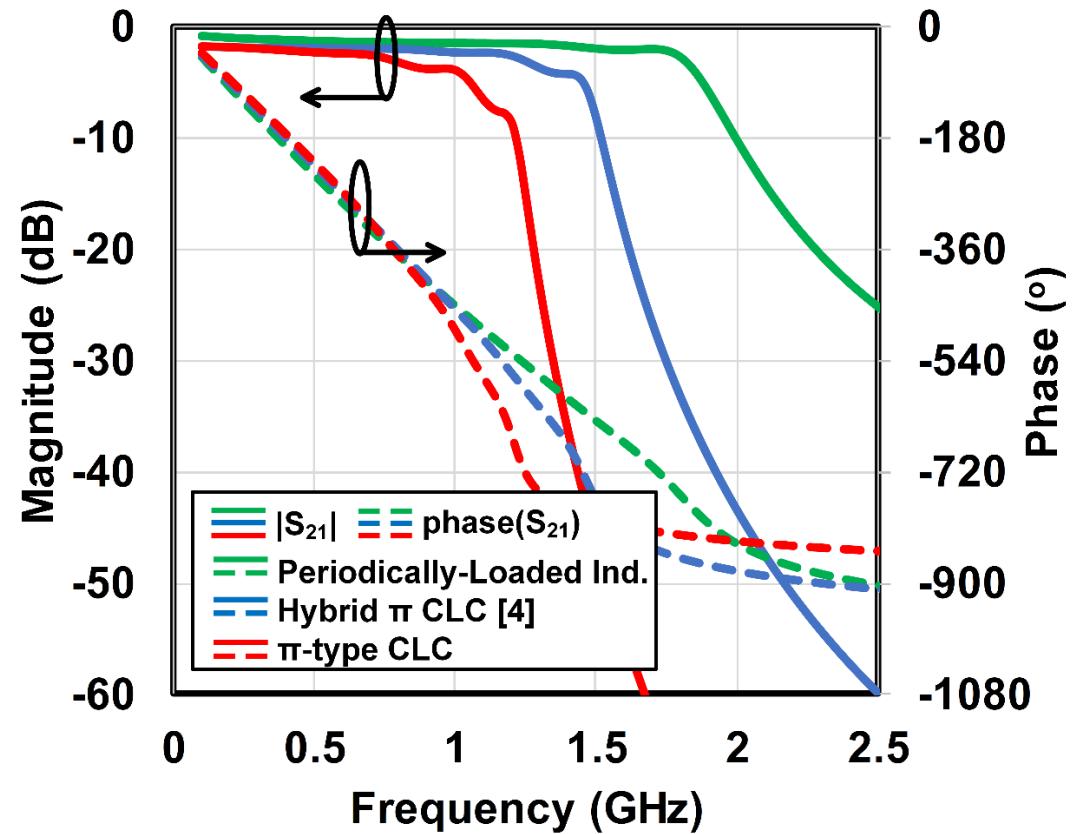
24-Tap Capacitively Loaded Inductor



Equivalent Half-Circuit

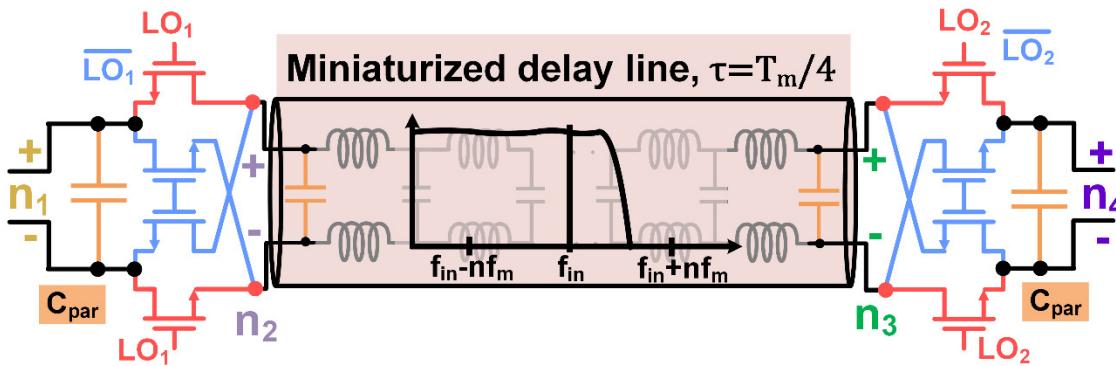


SPs of various techniques



- With a same area, t-line with periodically loaded inductors provide 1.8× higher Bragg Frequency compared to a regular CLC section t-line.
- This approaches improved the insertion losses of the circulator by 0.5dB.**

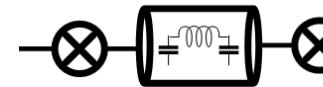
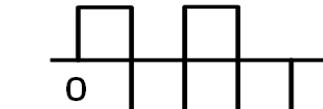
Reducing Power Consumption



$$Z_o = \sqrt{\frac{L}{C}}; \tau_d = N\sqrt{LC}$$

$\uparrow C$
 $\uparrow \tau_d \text{ ☺}; \downarrow Z_o \text{ ☹}$

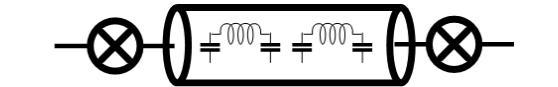
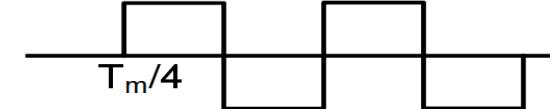
Case - I



High Power Consumption

Low Delay
(Low Area)

Case - II

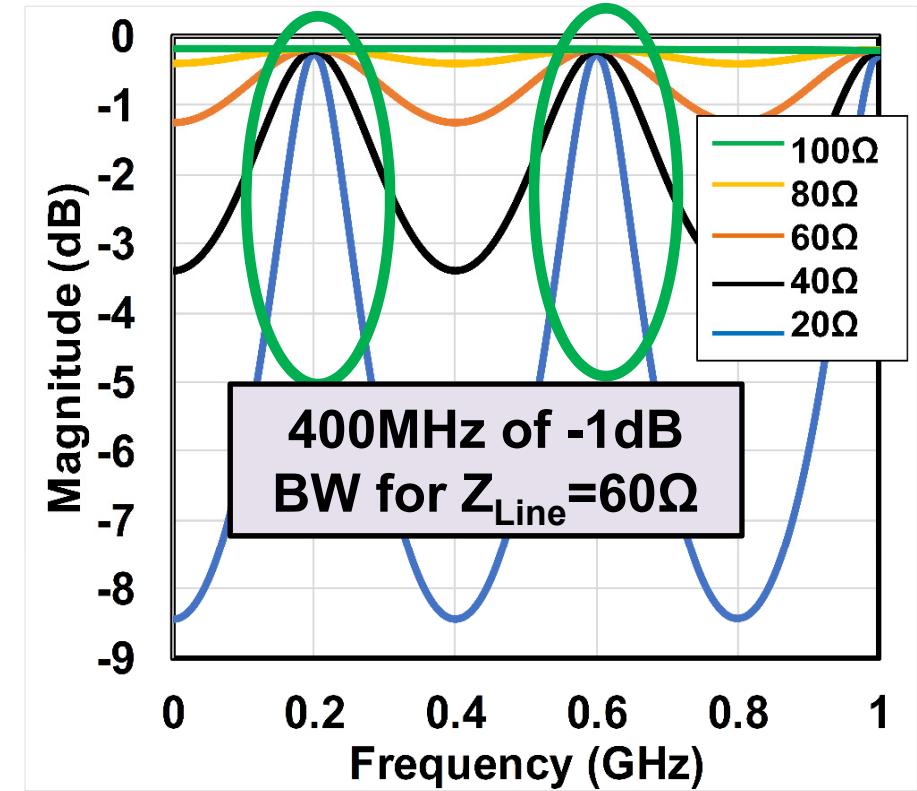
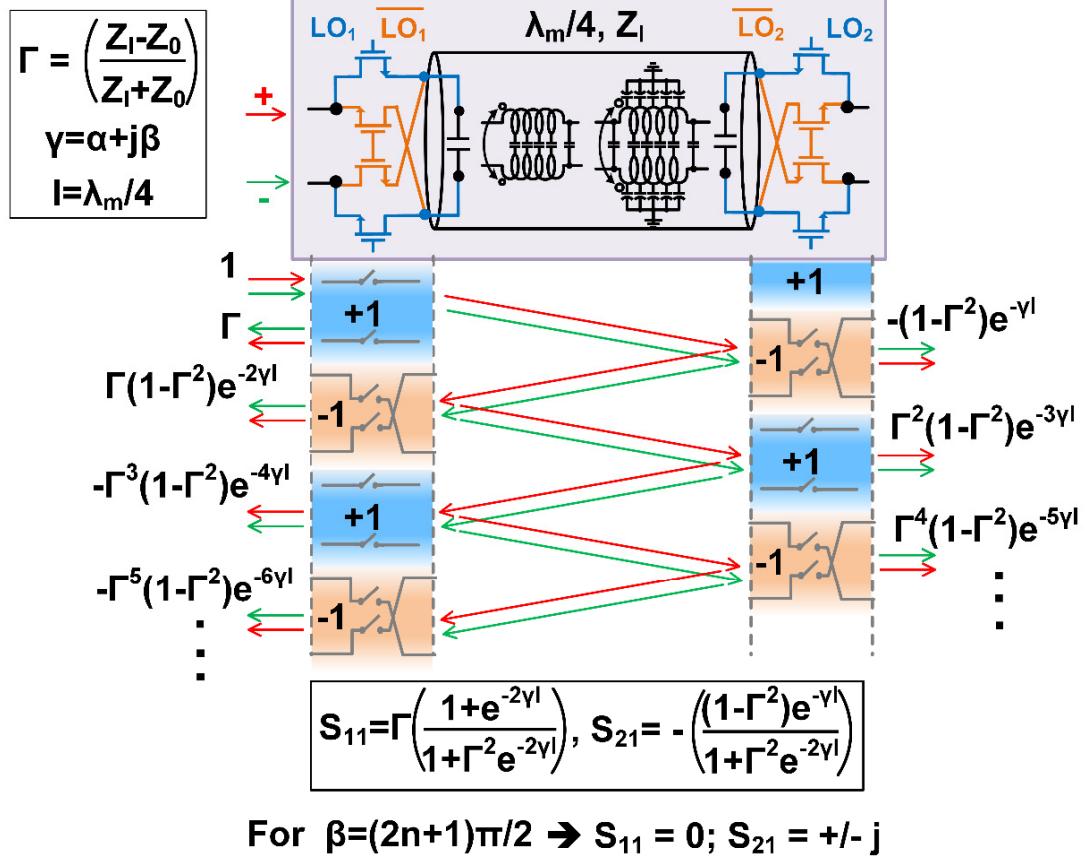


Low Power Consumption

High Delay
(High Area)

- Power consumption \propto Mod. Freq. $\propto 1/(\text{Delay of t-line})$
- Propagation delay can be increased without any area penalty by increasing the capacitance in the line, which reduces the characteristic impedance of the line.

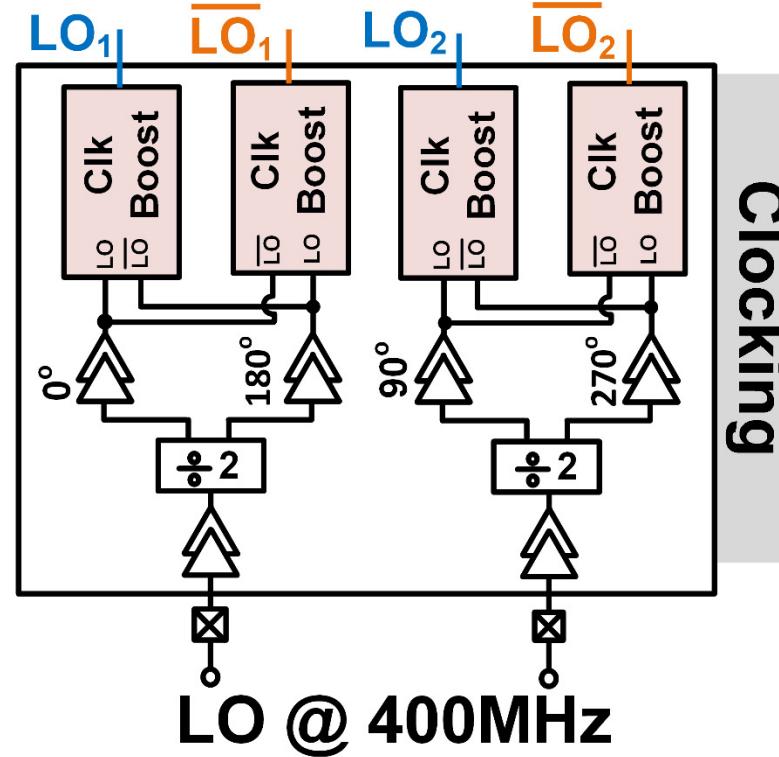
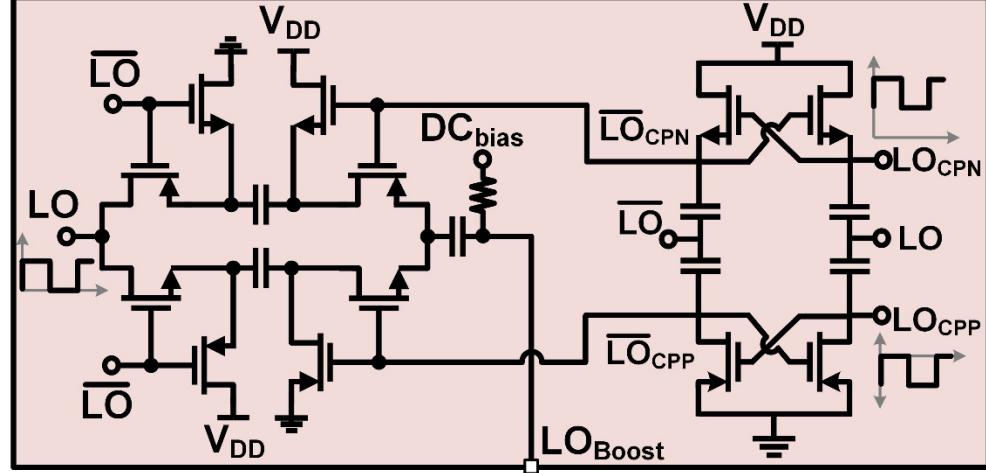
Gyrator Based on Partially Reflecting Lines



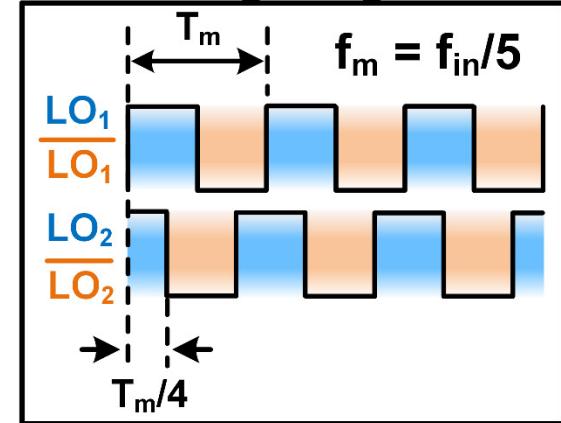
- Lower impedance → Higher Capacitance → Lower Area.
- The performance of the gyrator does not degrade at the odd-multiples.
- The circulator at odd-multiples results in no insertion losses degradation

Circulator Clock Path

Adiabatic Clock Boosting

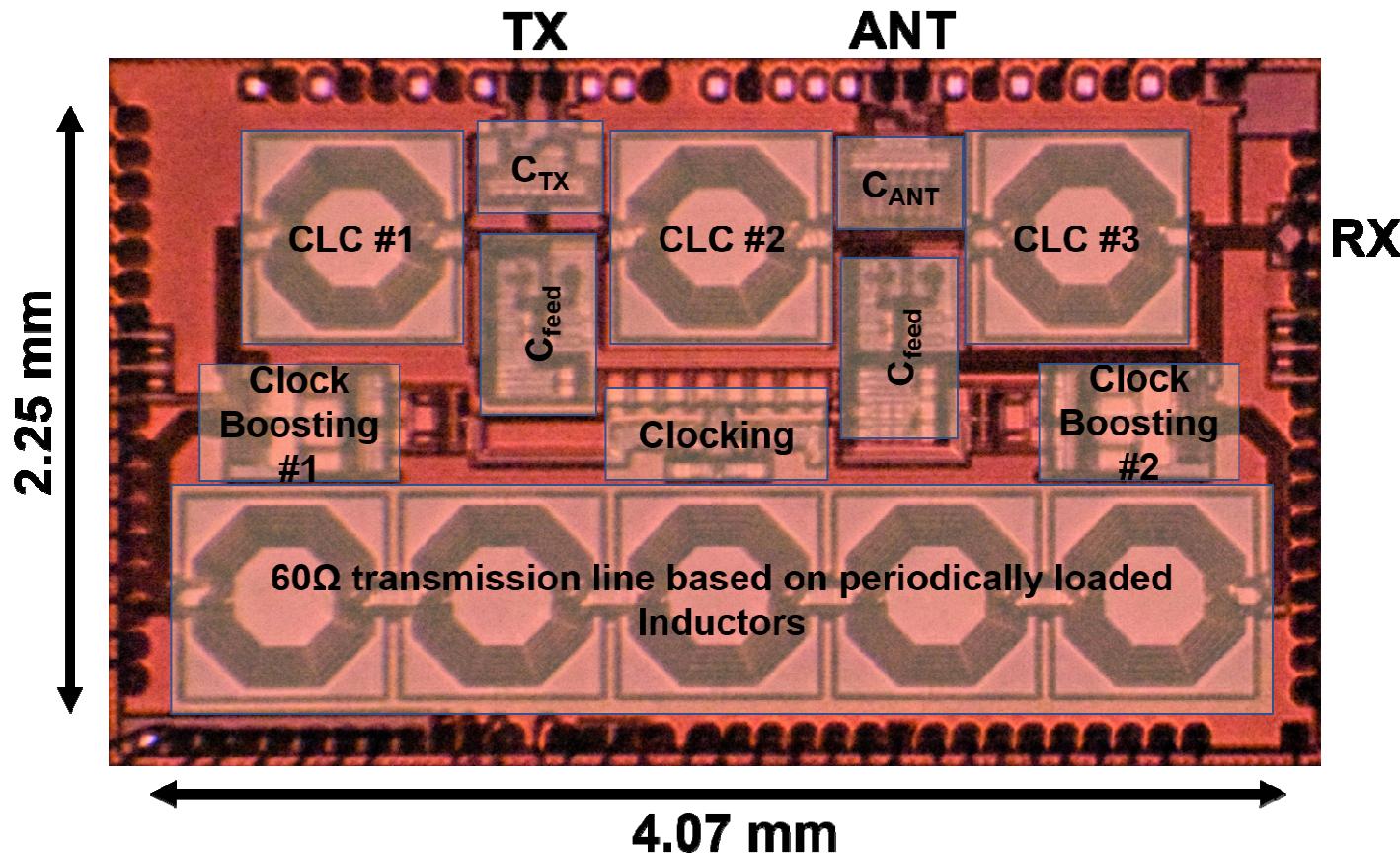


Timing Diagram



- Clock path with adiabatic clock boosting circuitry.
- The clock path consumes 39mW from a 1.5V supply for a 200MHz modulation.

Chip Photo

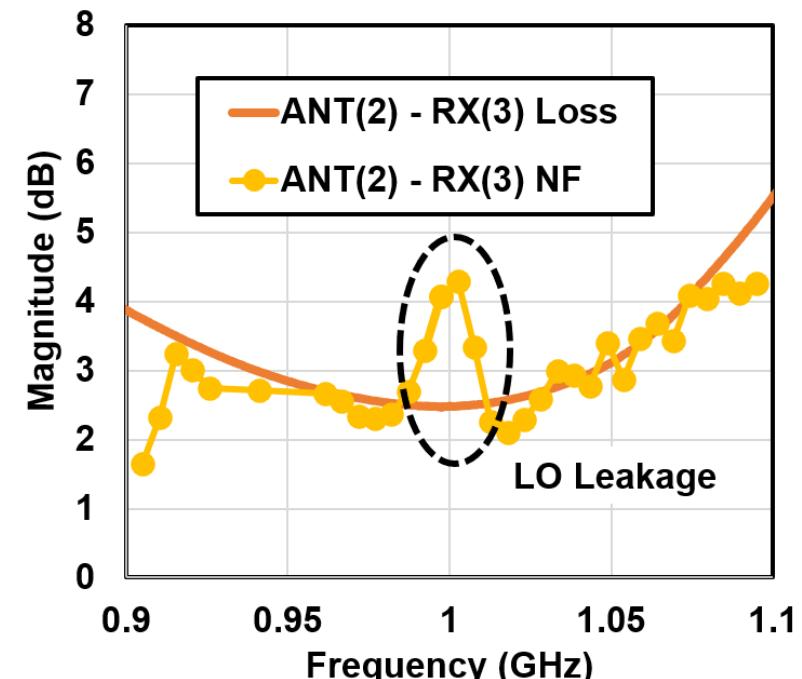
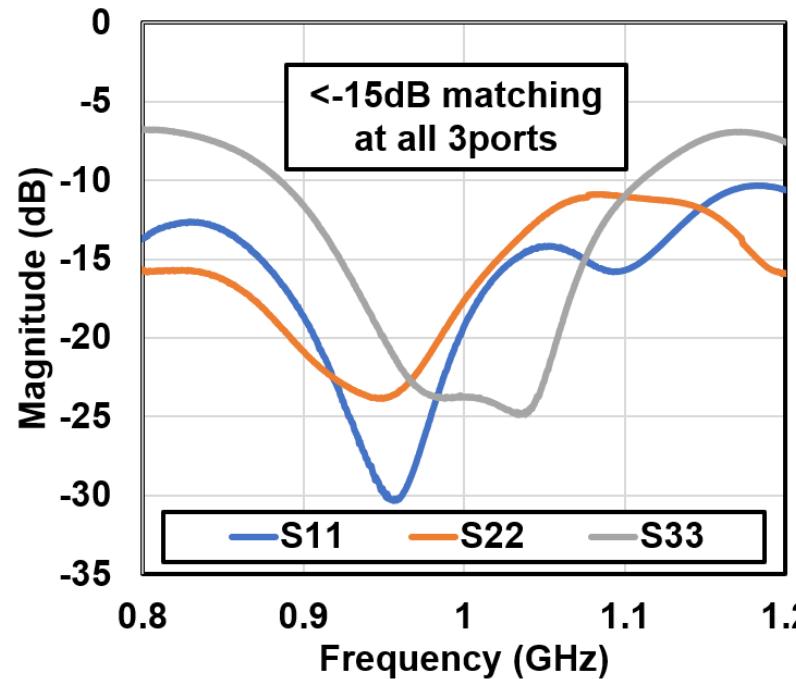
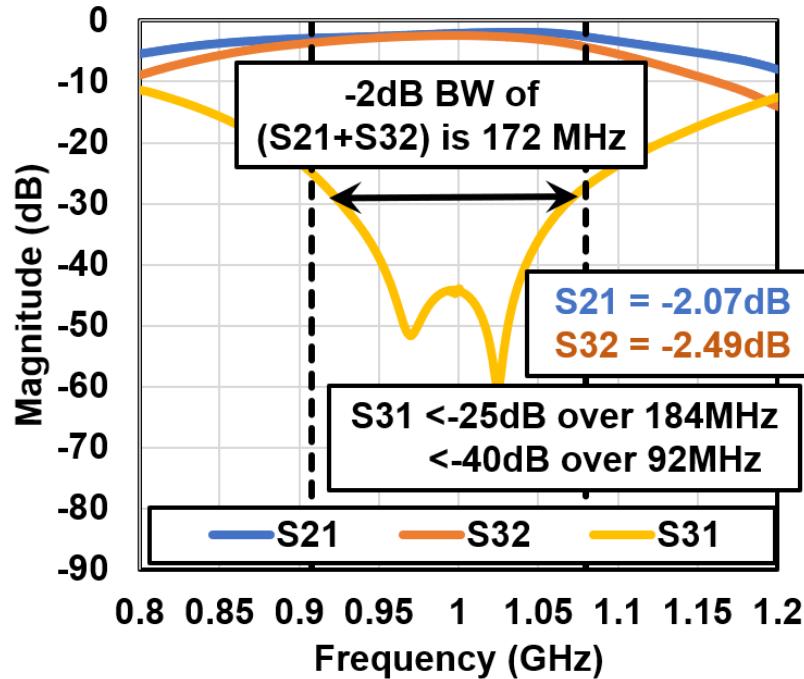


- The circulator prototype was implemented in a 180nm SOI CMOS process.
- The chip occupies an area of 9.1mm²

Overview

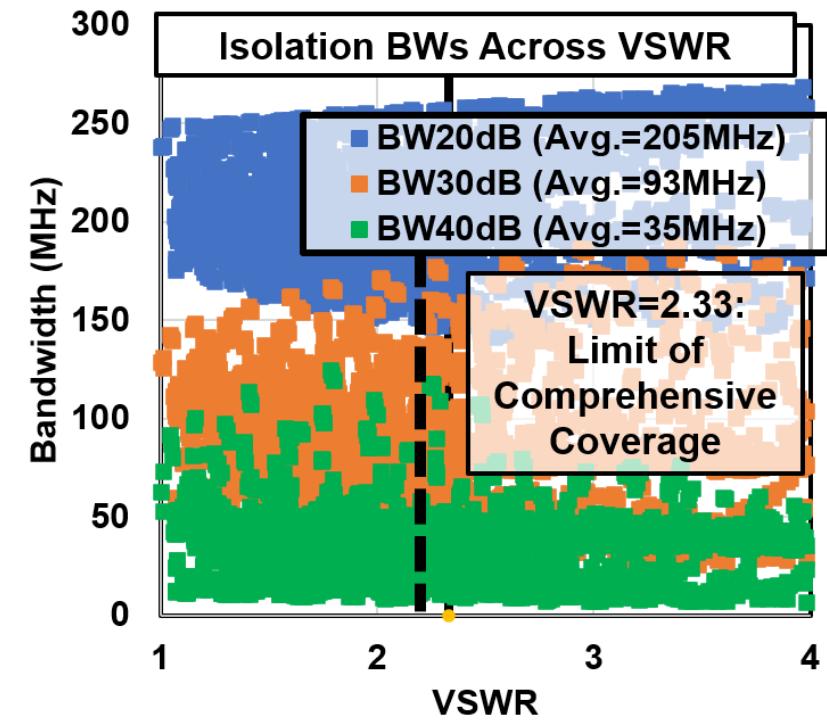
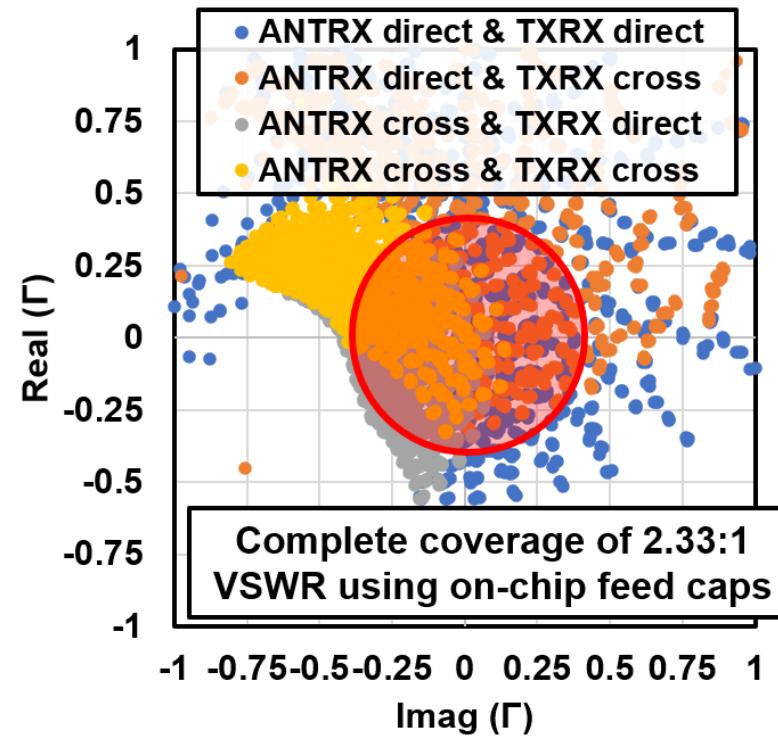
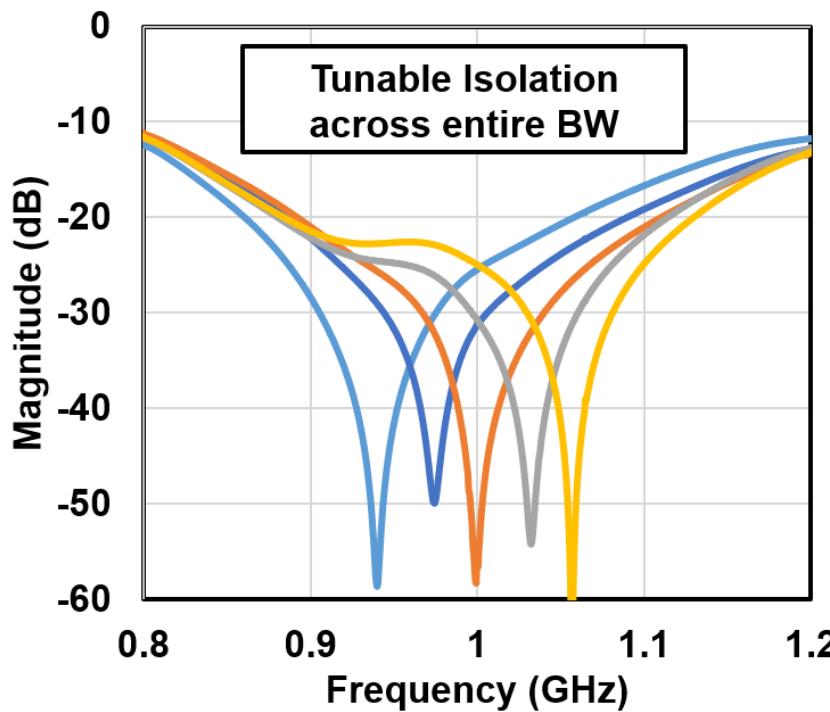
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CMOS Circulator S-Parameters & Noise Figure



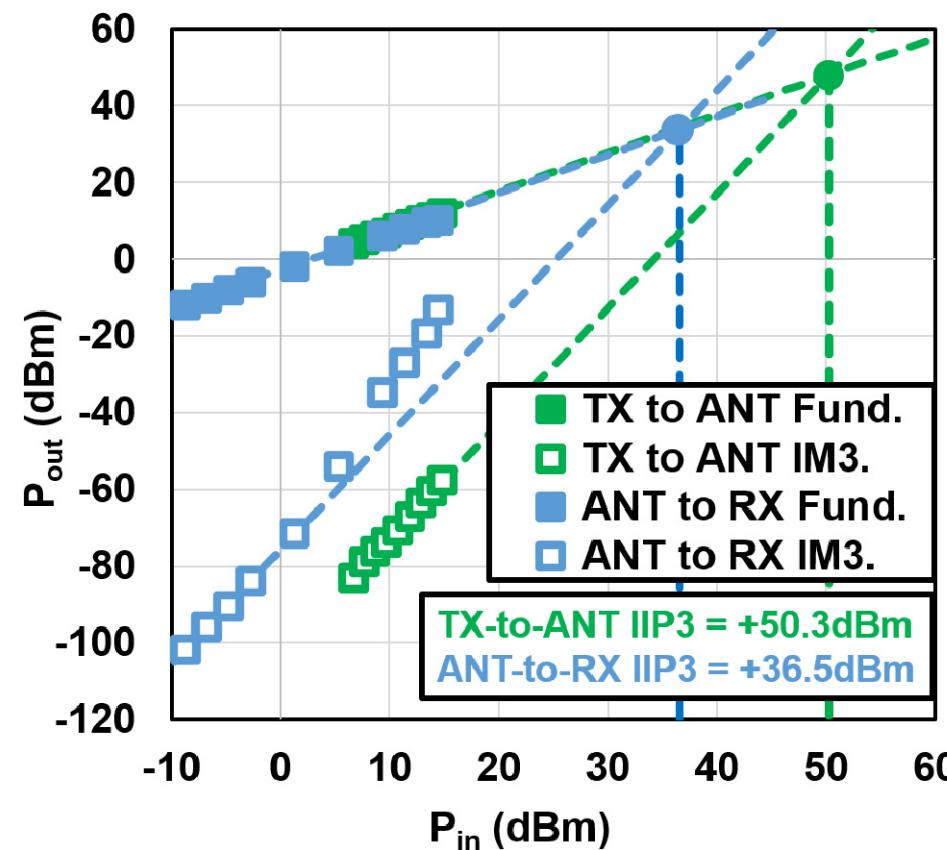
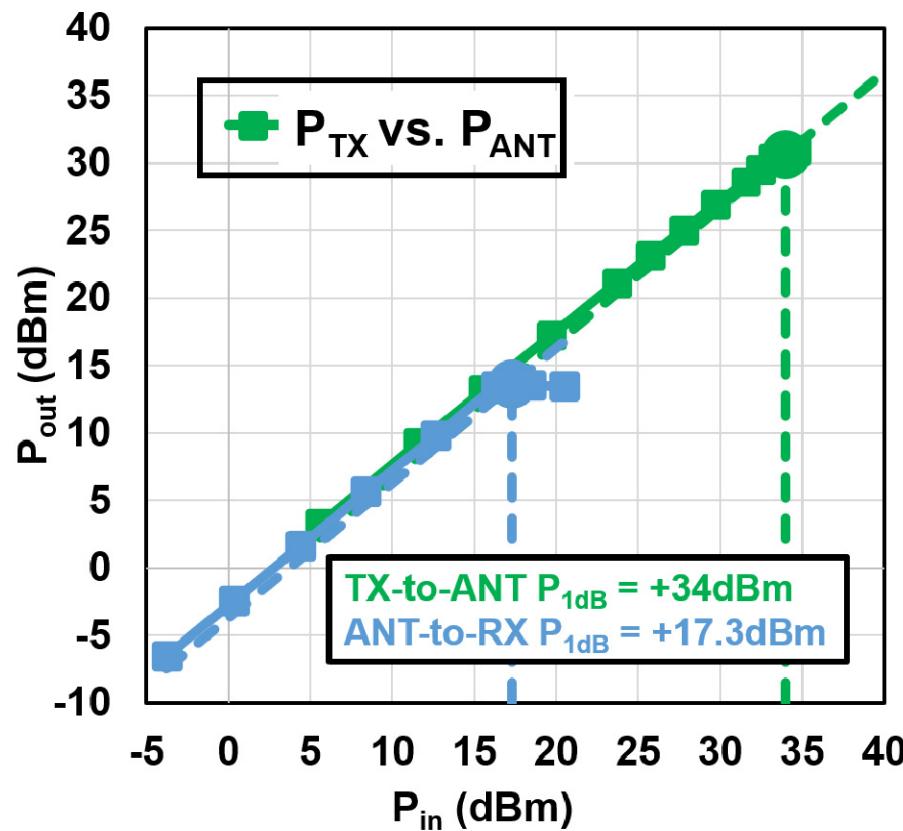
- We measured transmission losses of 2.07dB and 2.5dB, and their sum degrades by 2dB over a BW of 172MHz.
- Measured isolation is >40dB over a BW of 92MHz.
- Noise figure is consistent with ANT-RX loss, showing no degradation from phase noise of the clock path.

>40dB Iso. Across the BW and 2.33:1 VSWR



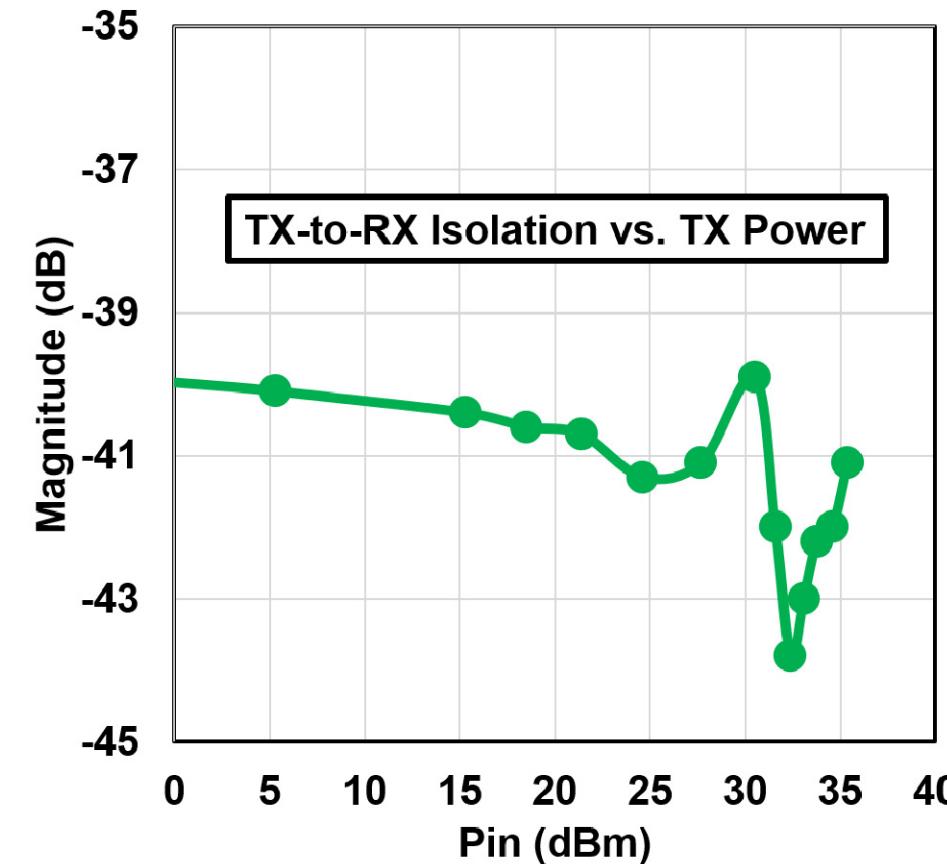
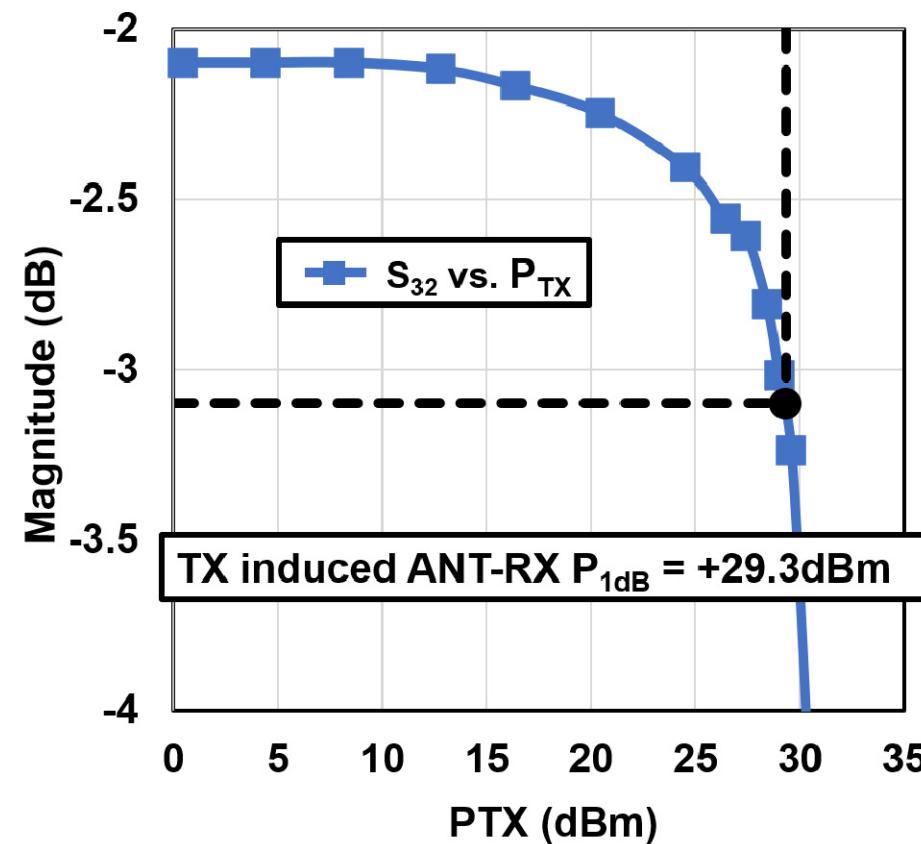
- Using the tuning capacitors:
 - The isolation can be tuned across the transmission BW.
 - >40dB isolation can be achieved across 2.33:1 antenna VSWR.
 - Average 20dB, 30dB and 40dB isolation BWs are 205MHz, 93MHz, 35MHz.

Circulator IIP3 and P1dB



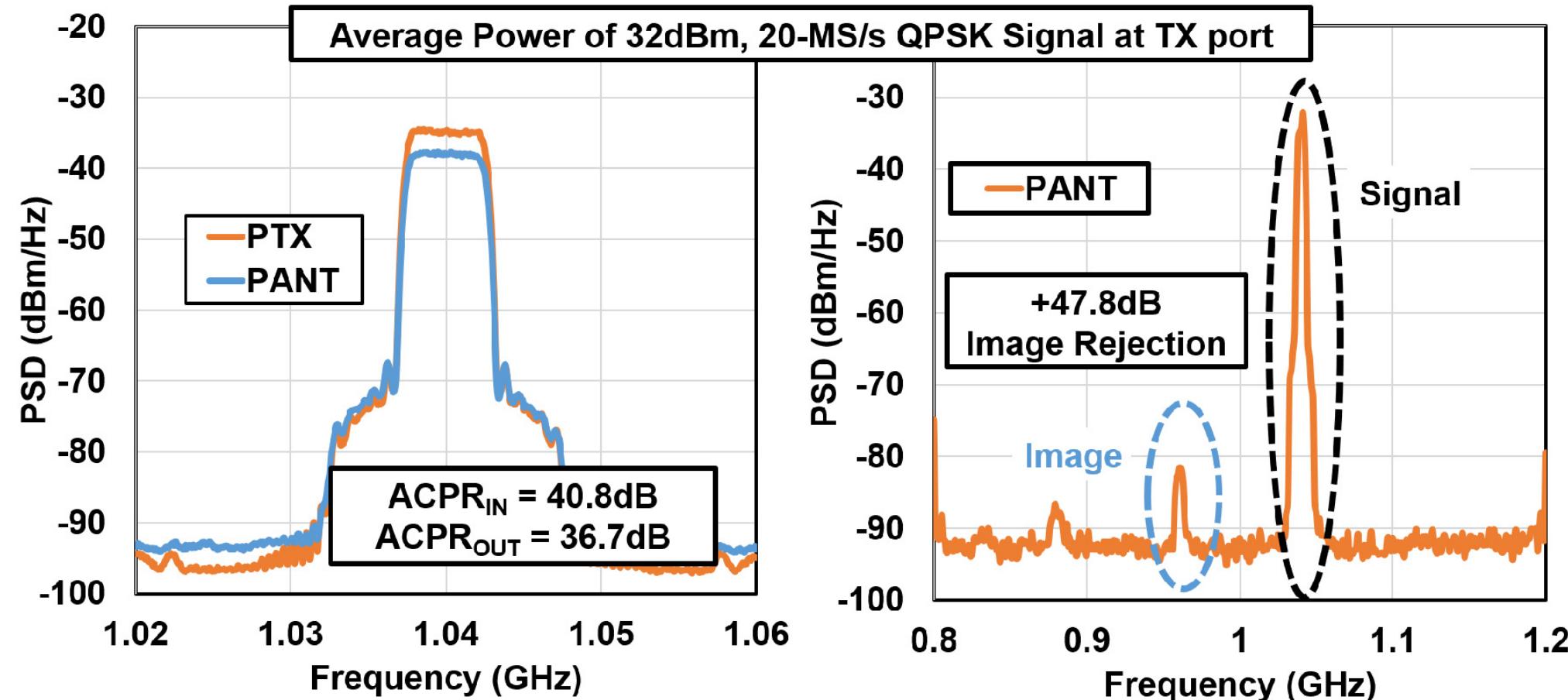
- We measured TX-to-ANT and ANT-to-RX IP1dBs to be +34dBm and +17.3dBm respectively, thanks to the clock boosting circuit.
- Measured TX-to-ANT and ANT-to-RX IIP3s are +50.3dBm and +36.5dBm.

TX-induced ANT-RX Loss and Iso. Compression



- Measured TX-induced ANT-to-RX P_{1dB} is +29.3 dBm.
- >40dB isolation is achieved across a wide range of TX powers.

Transmission of Modulator TX signals

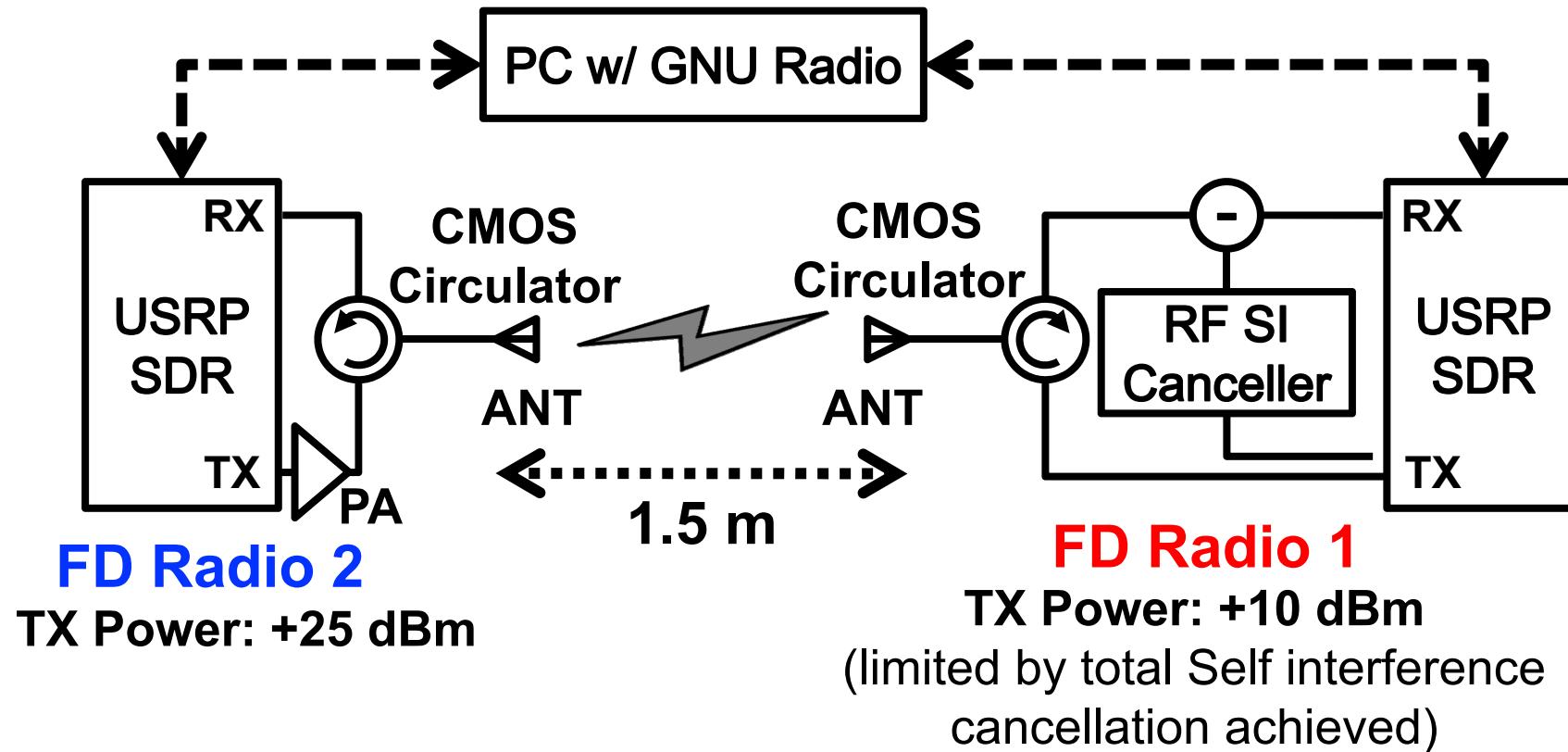


- ACPR has degraded by 4dB when operated close to TX-ANT compression.
- Image rejection was measured to be +47.7dB.

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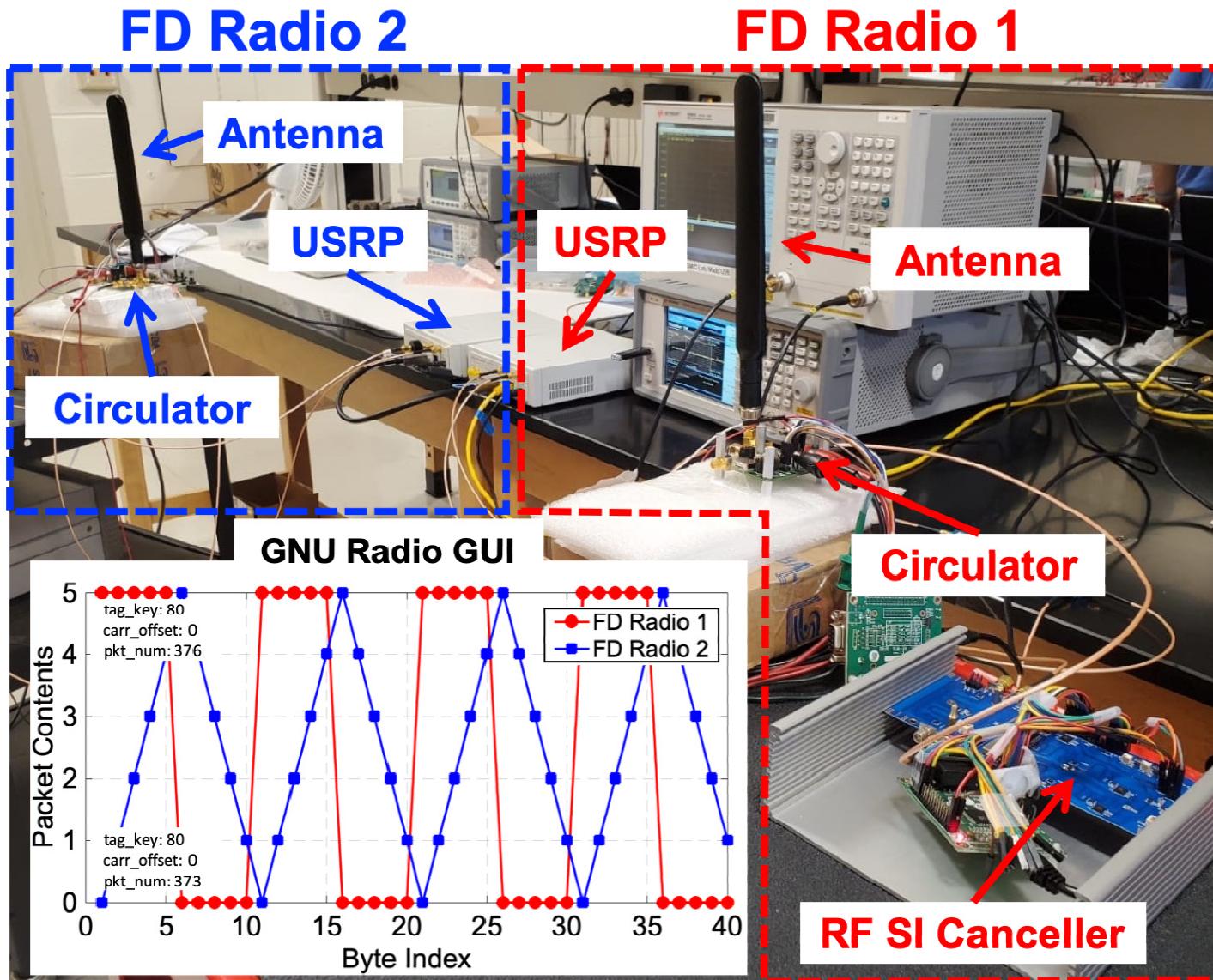
Full-Duplex Wireless Link: Block Diagram



- 10MHz OFDM-QPSK modulated packets are transmitted and received.
- Real-time digital self interference cancellation and packet decoding is performed.

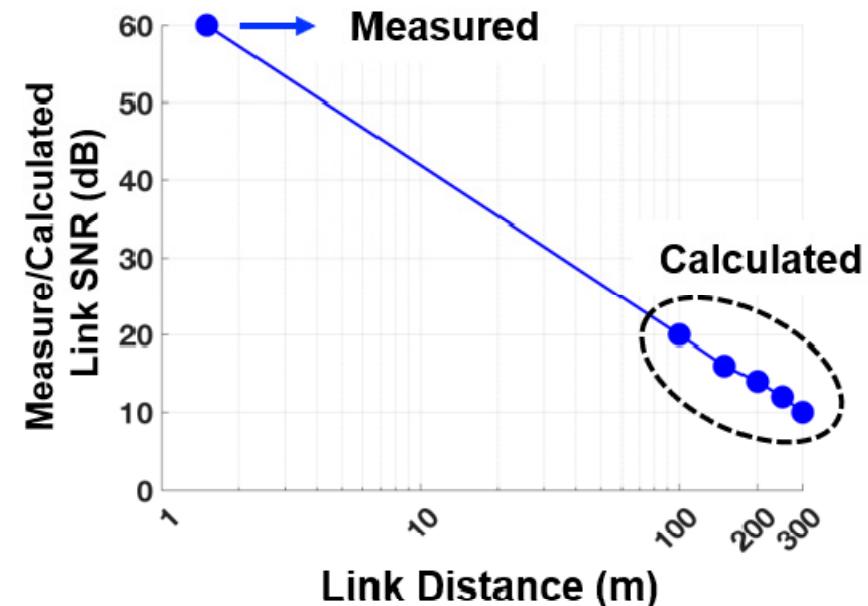
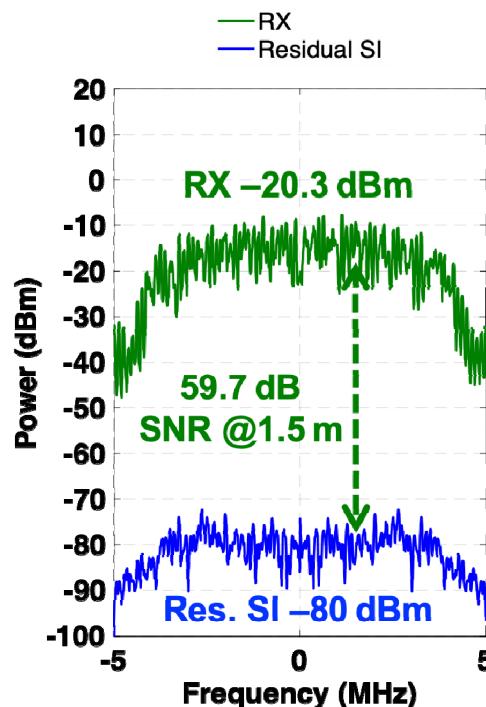
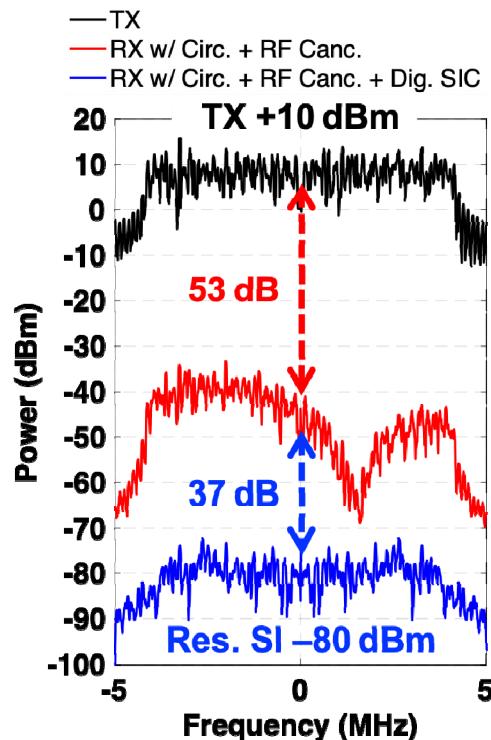
- Block diagram of the Full-duplex wireless link featuring the CMOS circulators.
- Radio 1 - CMOS circulator, an RF canceler and a USRP: $P_{TX} = +10\text{dBm}$.
- Radio 2 consists of a CMOS circulator, Power Amp, and a USRP: $P_{TX} = +25\text{dBm}$.

Full-Duplex Wireless Link: Lab Setup



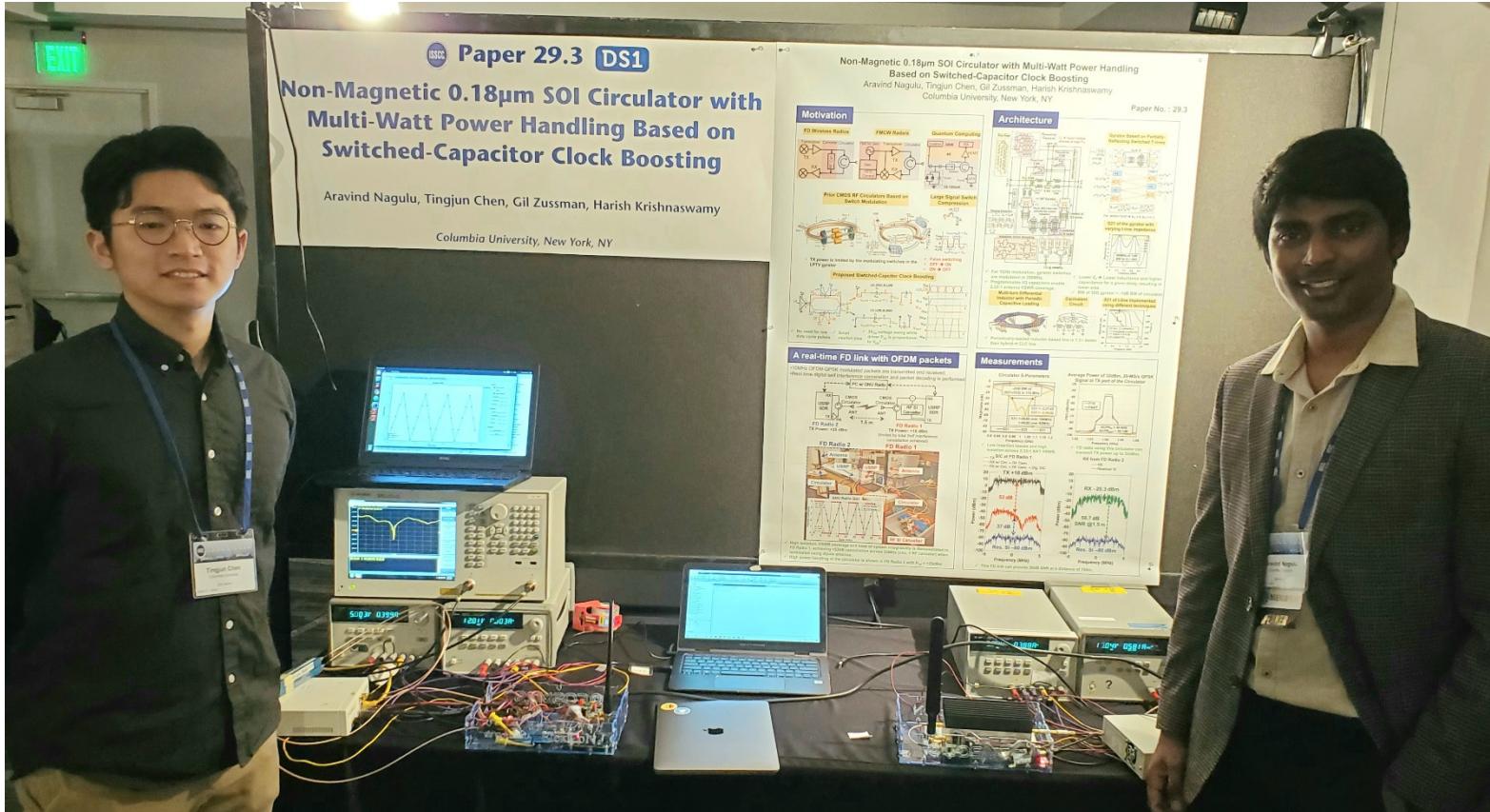
Lab measurement setup
when both the radios
were terminated with a
commercially available
LTE antenna.

Full-Duplex Wireless Link: Measurements



- A total SIC of +90dB has been measured in Radio 1 while transmitting +10dBm.
- Radio 1 received a signal with SNR = 60dB for a 1.5m over the air link measurement.
- This link is equivalent to a 100m link with SNR =20dB.

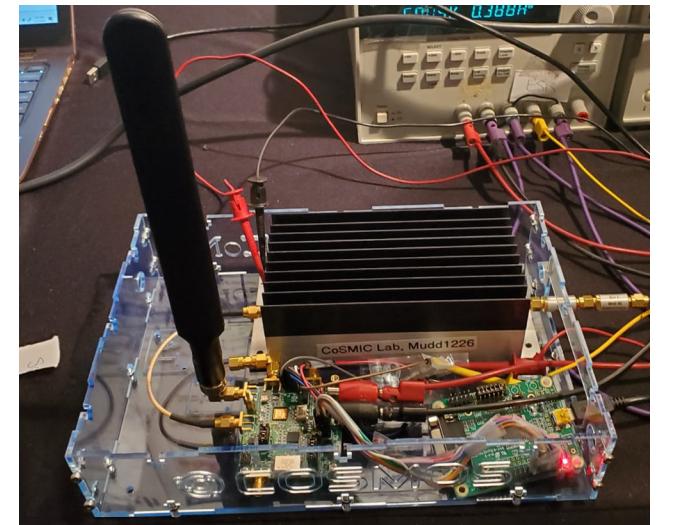
Full-Duplex Wireless Link Demonstration



Radio #1



Radio #2



A full-duplex wireless link featuring this CMOS circulator was demonstrated in DS#1, ISSCC 2020.

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Conclusion

- A novel clock boosting technique has been produced that generated at drive signal of **$3V_{DD}$ from a supply voltage of V_{DD}** .
- A fully-integrated magnetic-free passive switched-transmission-line circulator is presented that exploits various linearity and power handling enhancement techniques to achieve **+34dBm TX power handling with a +50dBm TX-ANT IIP3**.
- Concepts of gyrator with **partially-reflecting t-lines** and **periodically loaded inductors** were discussed.
- Loss-free, Inductor-free antenna balancing technique enables **high isolation over ANT VSWR of 2.33:1**.

Acknowledgements

- This work was supported by the DARPA SPAR and NSF EFRI programs.
- Our thanks to
 - Dr. Timothy Hancock, Dr. Troy Olsson and Dr. Ben Epstein of DARPA for feedback and comments,
 - Prof. Andrea Alu of CUNY for feedback and comments,
 - CoSMIC lab members for discussion.

Thank you for your attention.

High-Performance Isolators and Notch Filters Based on N-Path Negative Transresistance

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Harish Krishnaswamy¹

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² MIT, Cambridge, MA

***Equally-Credited Authors (ECAs)**

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Presentation Outline

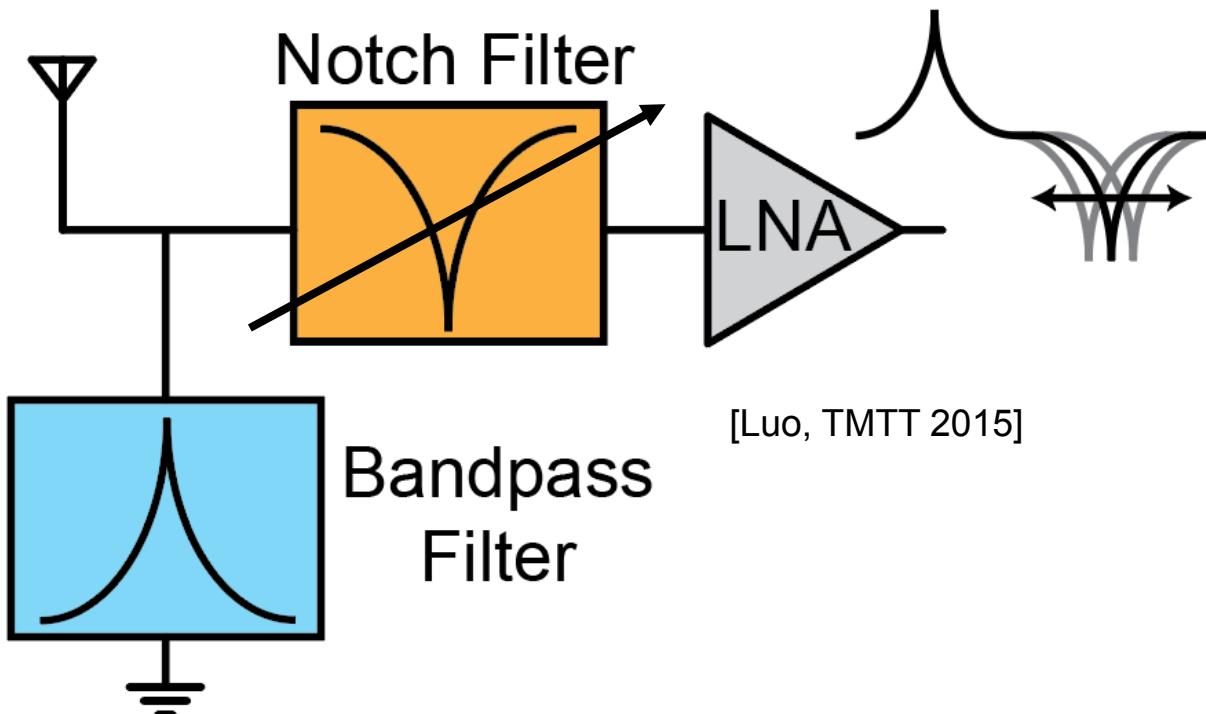
- Introduction
- Negative Transresistance Concept in N-Path Structures
- N-Path Notch Filter and RF Isolator Structures
- Circuit Implementations
- Measurement Results
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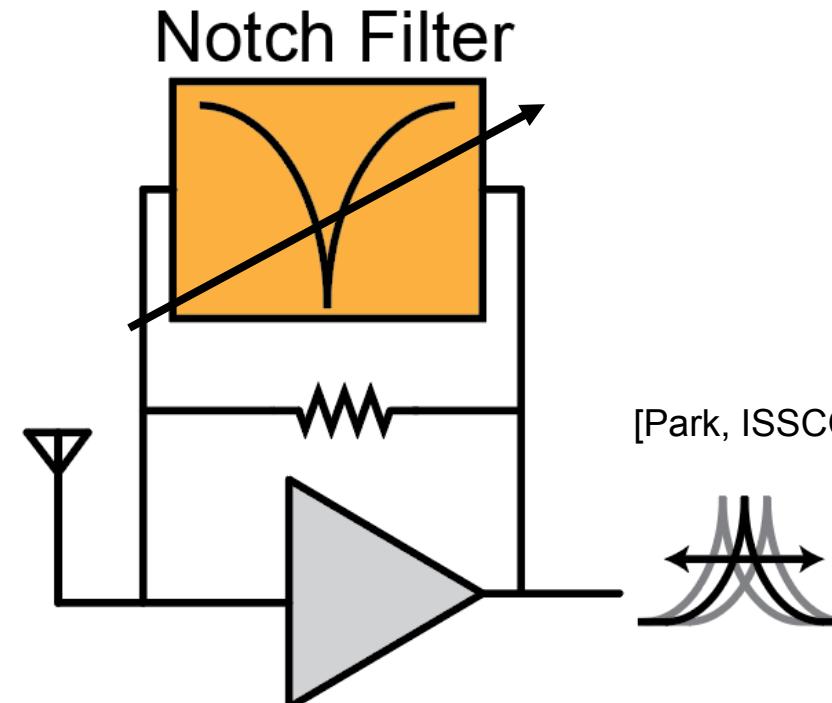
Applications of Notch Filters

Blocker Tolerant Receivers



[Luo, TMTT 2015]

Channel-Selection Filtering

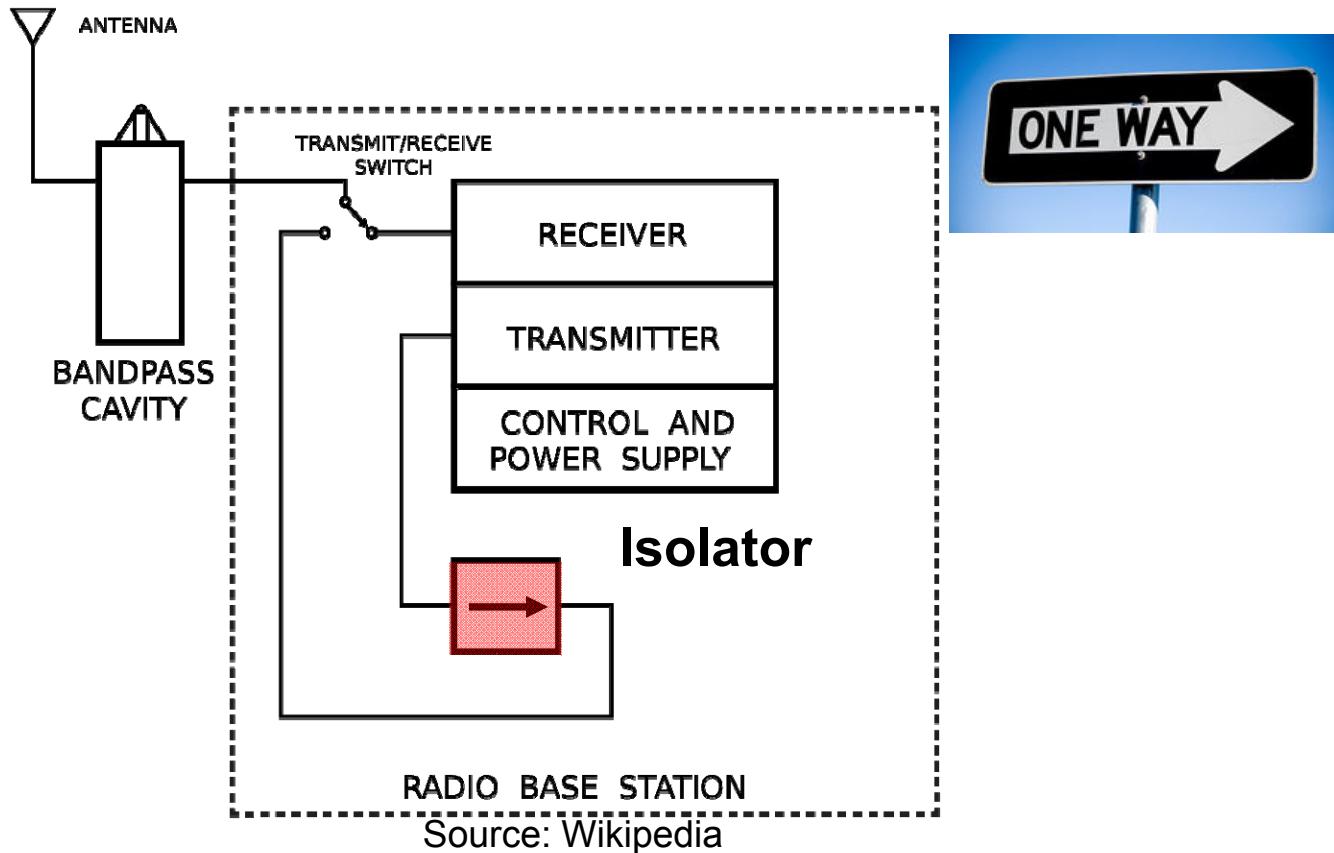


[Park, ISSCC 2014]

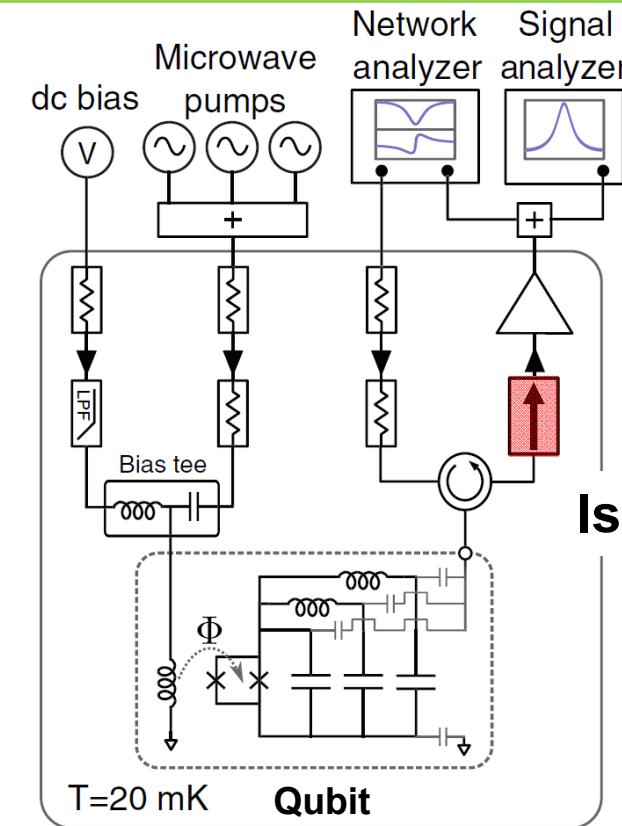
Notch filters find widespread application in blocker tolerant systems and to select closely-spaced frequency channels.

Applications of Isolators

Preventing Back-Reflections in Base Stations



Superconducting Quantum Systems



Isolators are essential to suppress reflections in various applications.

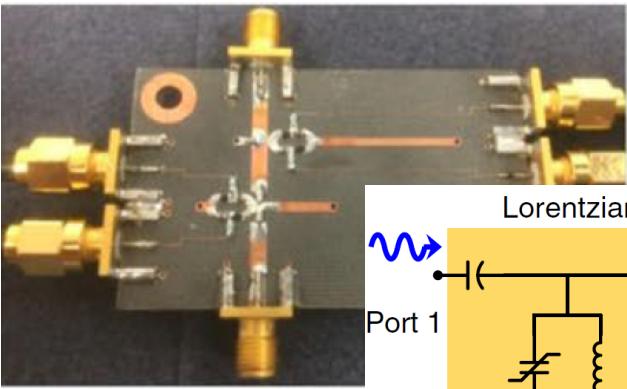
Breaking Reciprocity

Ferrite-Based

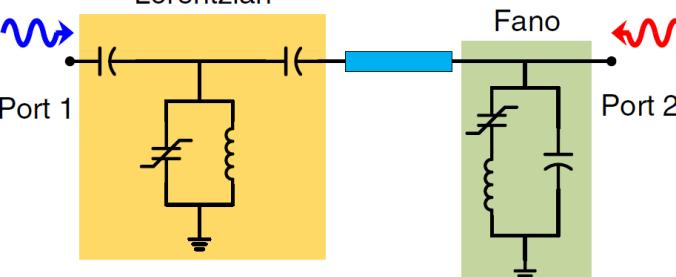


Nonlinearity-Based

RF port 2

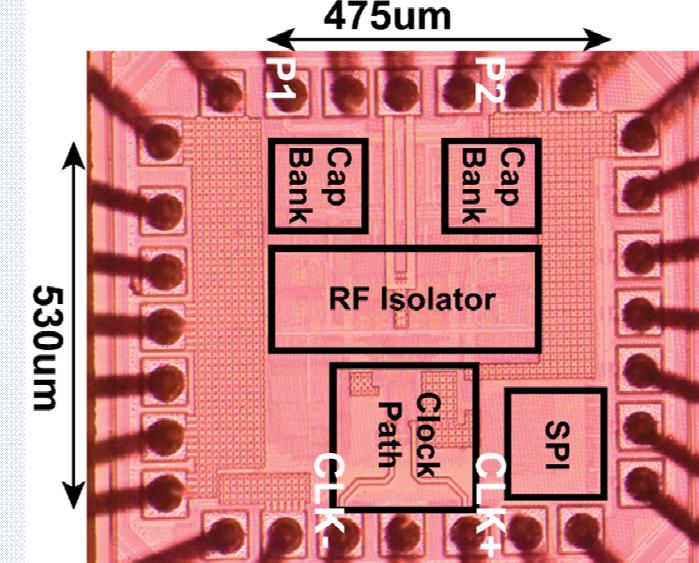


[Sounas, Nat. Elec., 2018]



Spatio-Temporal Modulation-Based

This Work



- ✓ Integrated
- ✓ Small Area
- ✓ Low Loss
- ✓ High Isolation

29.4: High-Performance Isolators and Notch Filters Based on N-Path Negative Transresistance

Presentation Outline

- Introduction
- Negative Transresistance Concept in N-Path Structures
- N-Path Notch Filter and RF Isolator Structures
- Circuit Implementations
- Measurement Results
- Conclusion

Single Path Waveforms (Forward Direction)

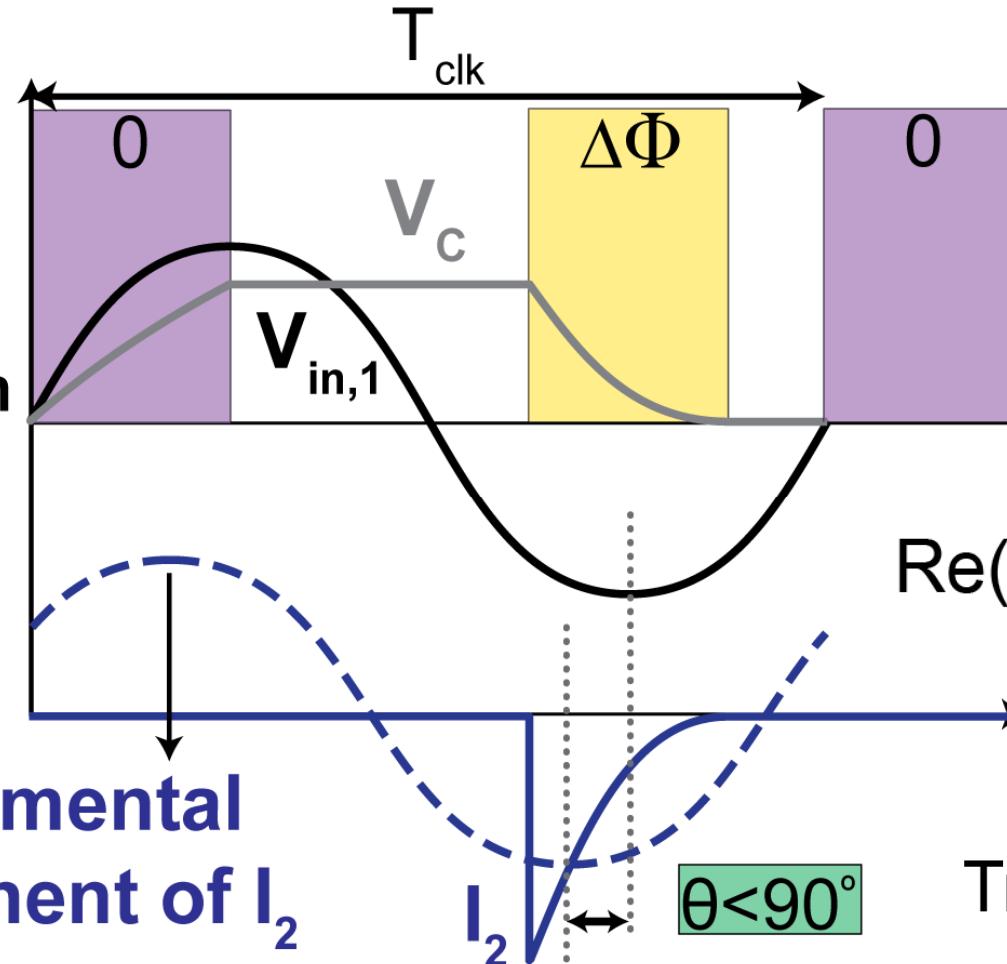
e.g. $\Delta\Phi=5\pi/4$:

$$\begin{aligned}C &= 1\text{pF} \\f_{\text{clk}} &= 1\text{GHz} \\D &= 25\%\end{aligned}$$

Forward Direction

$$V_{\text{in},2}=0$$

Fundamental Component of I_2



$$\text{Re}(-Y_{21}(f_{\text{clk}})) \propto -\left| \frac{I_2(f_{\text{clk}})}{V_{\text{in},1}(f_{\text{clk}})} \right| \cos(\theta) < 0$$

$$\text{Forward Transresistance} = \frac{1}{\text{Re}(-Y_{21}(f_{\text{clk}}))} < 0$$

Negative transresistance can be seen in the forward direction.

Single Path Waveforms (Reverse Direction)

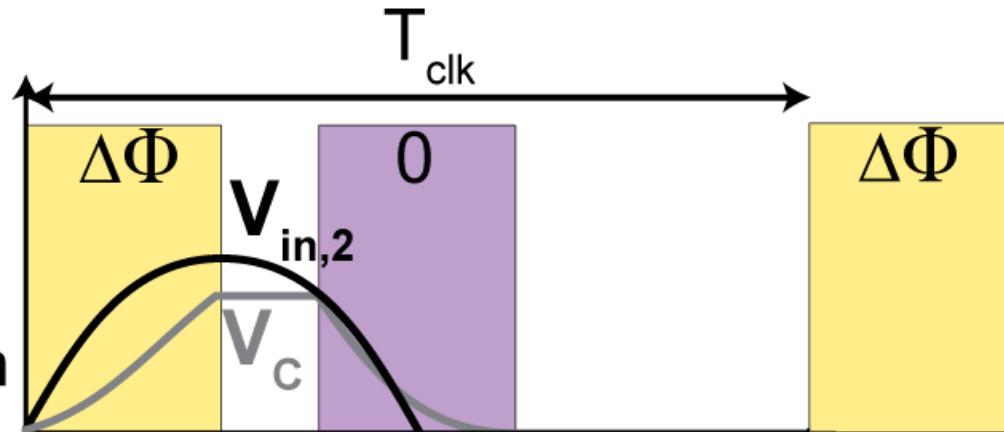
e.g. $\Delta\Phi=5\pi/4$:

$$\begin{aligned}C &= 1\text{pF} \\f_{\text{clk}} &= 1\text{GHz} \\D &= 25\%\end{aligned}$$

Reverse Direction

$$V_{\text{in},1}=0$$

Fundamental Component of I_1



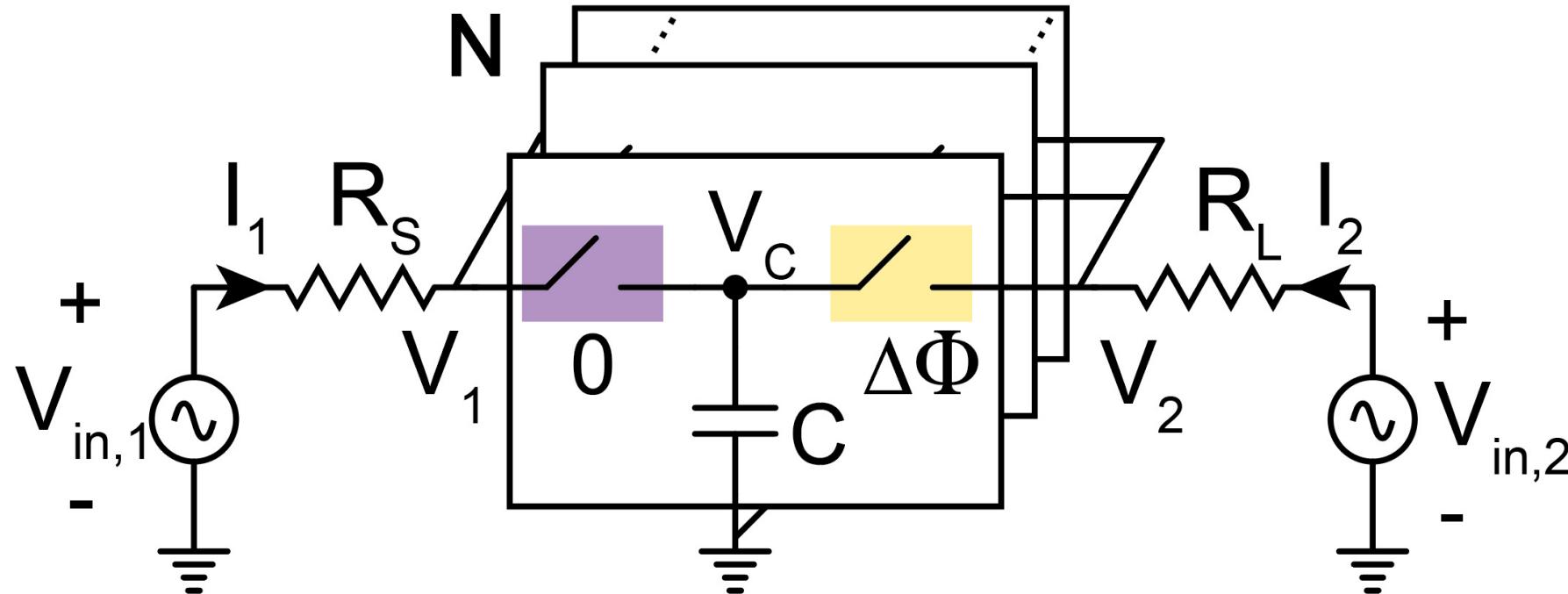
$$\text{Re}(-Y_{12}(f_{\text{clk}})) \propto -\left| \frac{I_1(f_{\text{clk}})}{V_{\text{in},2}(f_{\text{clk}})} \right| \cos(\theta) > 0$$

$$\theta > 90^\circ$$

$$\text{Reverse Transresistance} = \frac{1}{\text{Re}(-Y_{12}(f_{\text{clk}}))} > 0$$

The transresistance is positive in the reverse direction and hence it is nonreciprocal.

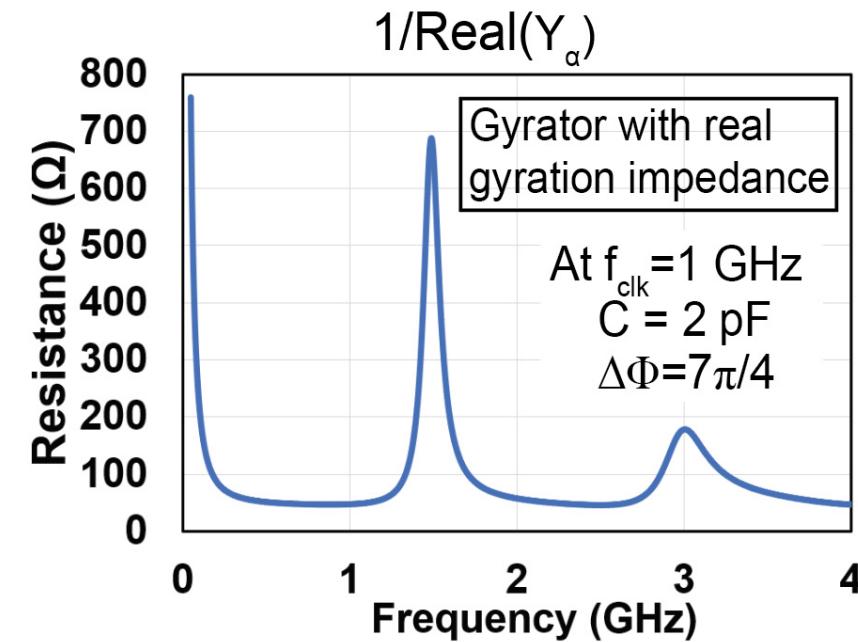
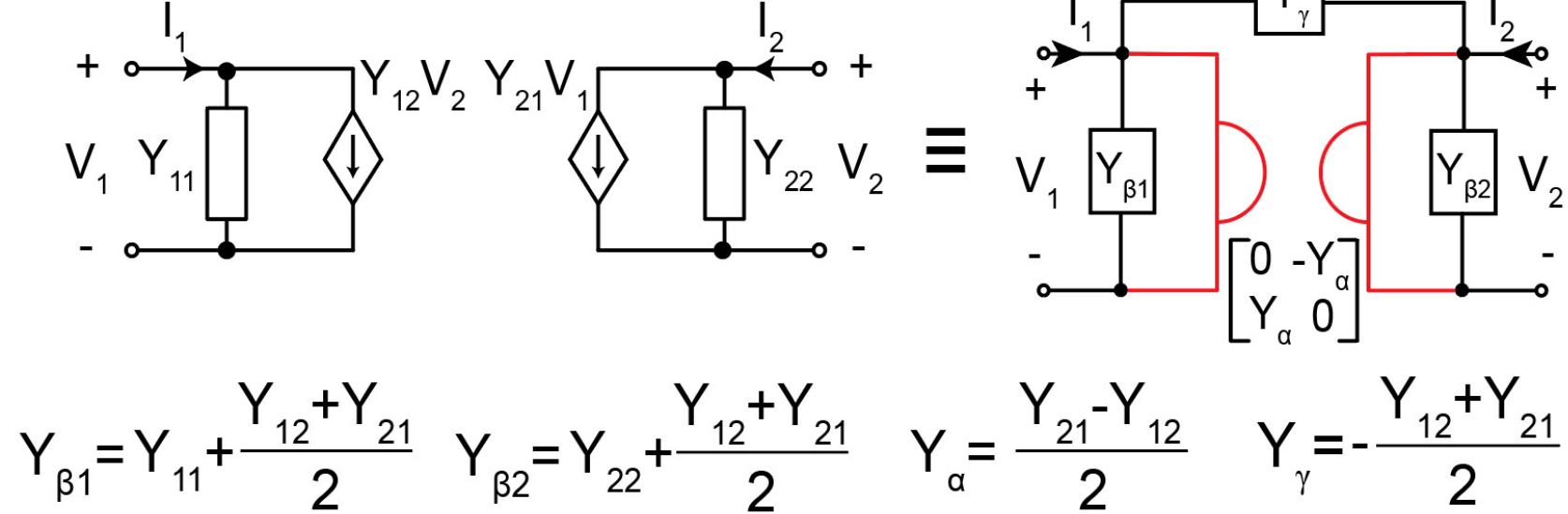
N-Path Phase-Shifted Switched Capacitor



	$0 \leq \Delta\Phi < \pi/2$	$\pi/2 \leq \Delta\Phi < \pi$	$\pi \leq \Delta\Phi < 3\pi/2$	$3\pi/2 \leq \Delta\Phi < 2\pi$
Transresistance in the forward direction, $\text{Re}(-Y_{21})$	Always +	+ / - †	Always -	+ / - †
Transresistance in the reverse direction, $\text{Re}(-Y_{12})$	+ / - †	Always -	+ / - †	Always +

†: Depends on the capacitor value and $\Delta\Phi$

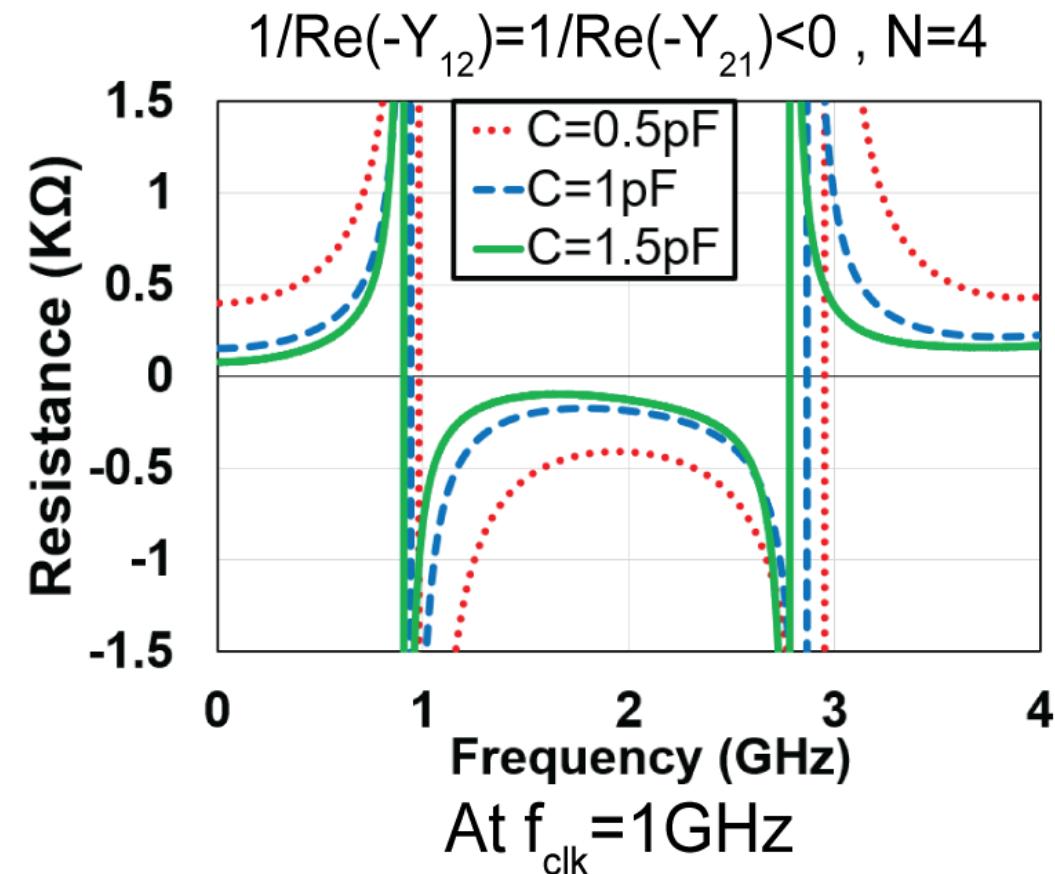
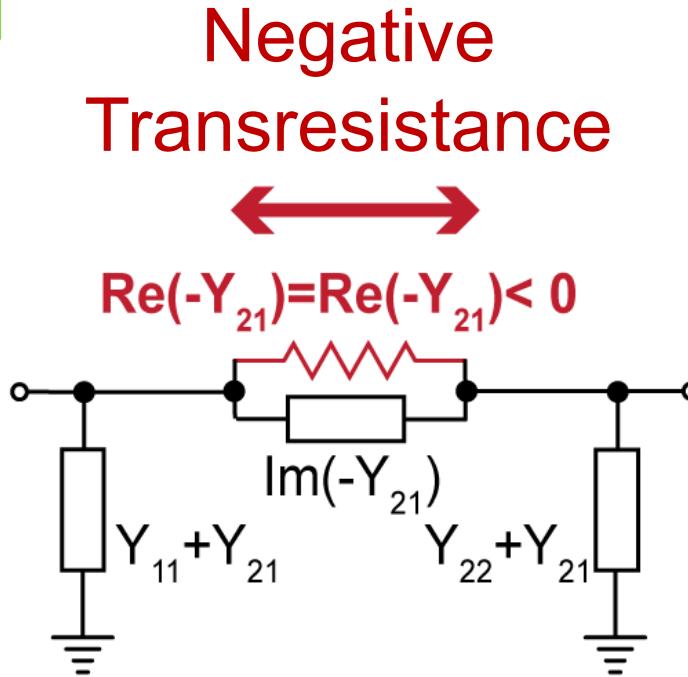
Nonreciprocal Transresistance Model



In this case, the N-path model can include a gyrator with a real gyration impedance.

Reciprocal Negative Transresistance Model

$$\Delta\Phi=\pi$$



For the reciprocal case, the model can be simplified to a π -model.

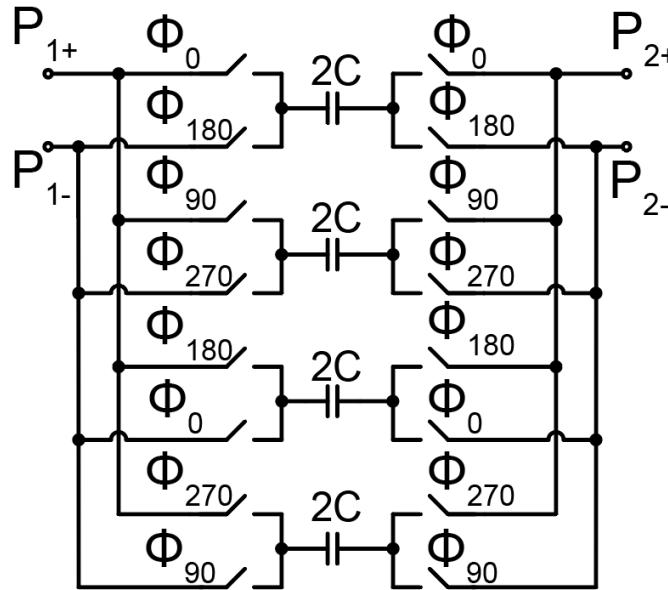
Presentation Outline

- Introduction
- Negative Transresistance Concept in N-Path Structures
- **N-Path Notch Filter and RF Isolator Structures**
- Circuit Implementations
- Measurement Results
- Conclusion

Notch Filter Evolution

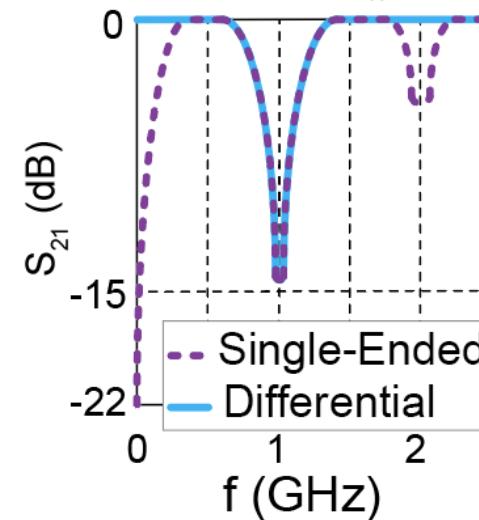
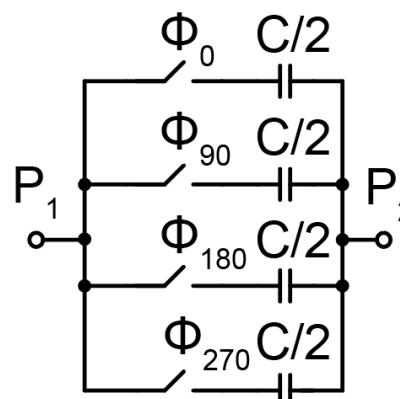
Conventional Notch Filter Structures

Differential

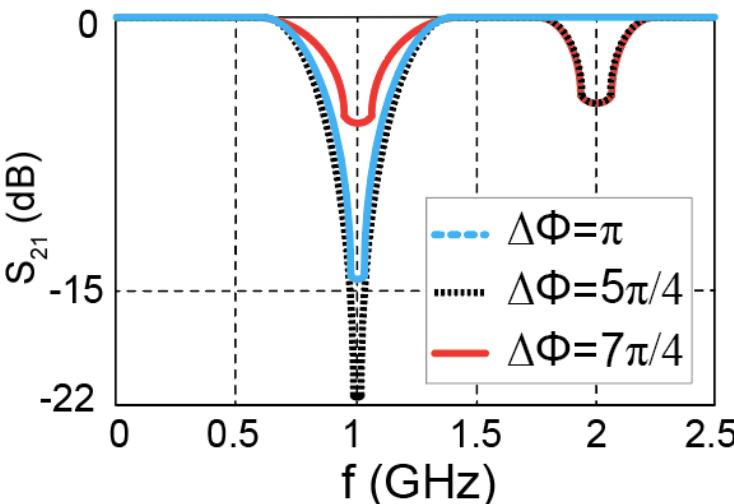
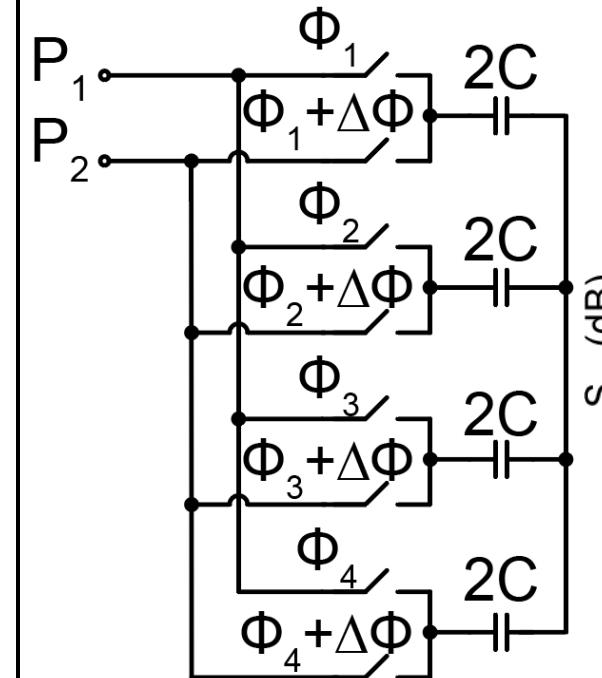


[Ghaffari, JSSC
2013]

Single-Ended



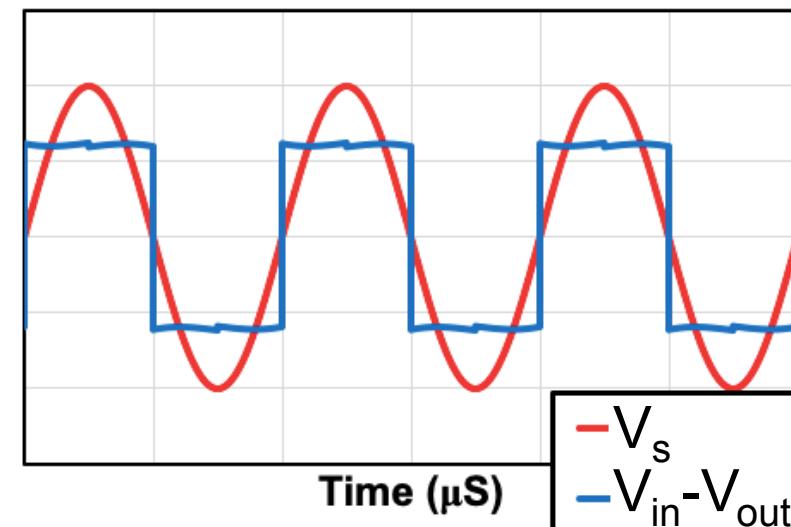
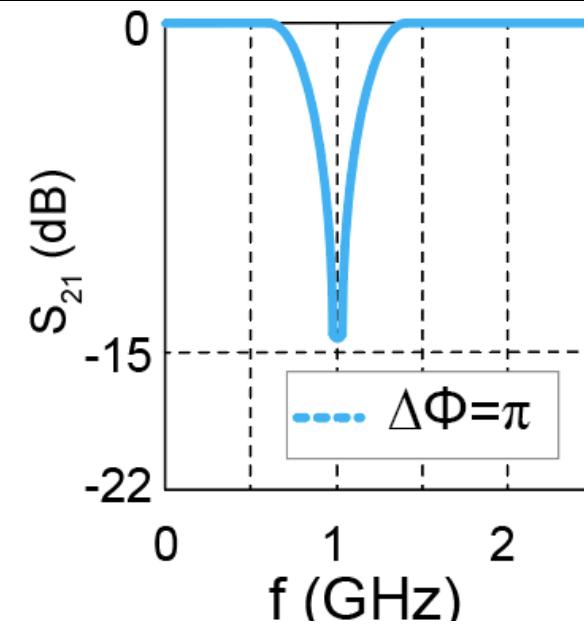
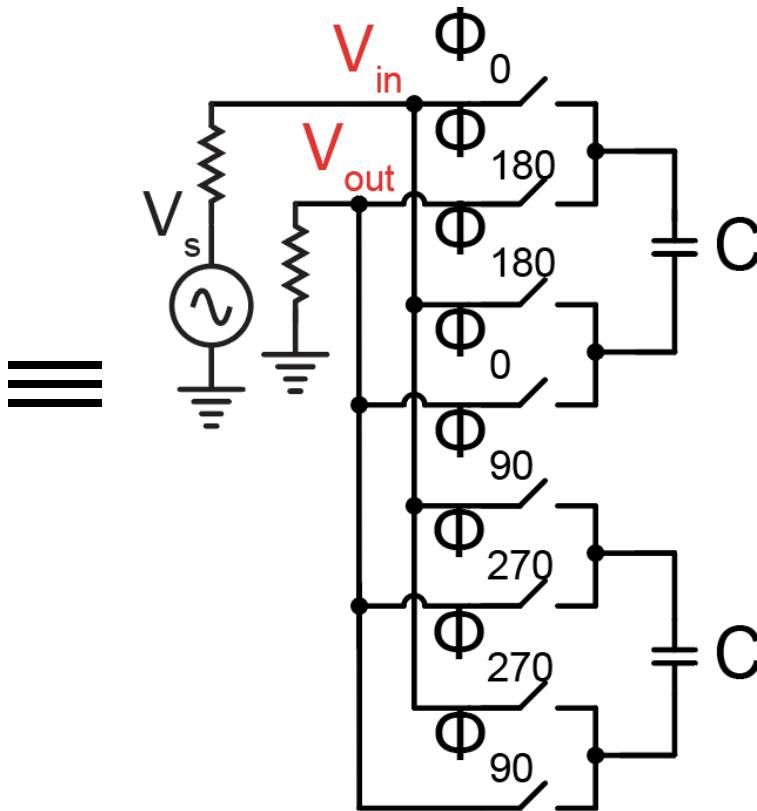
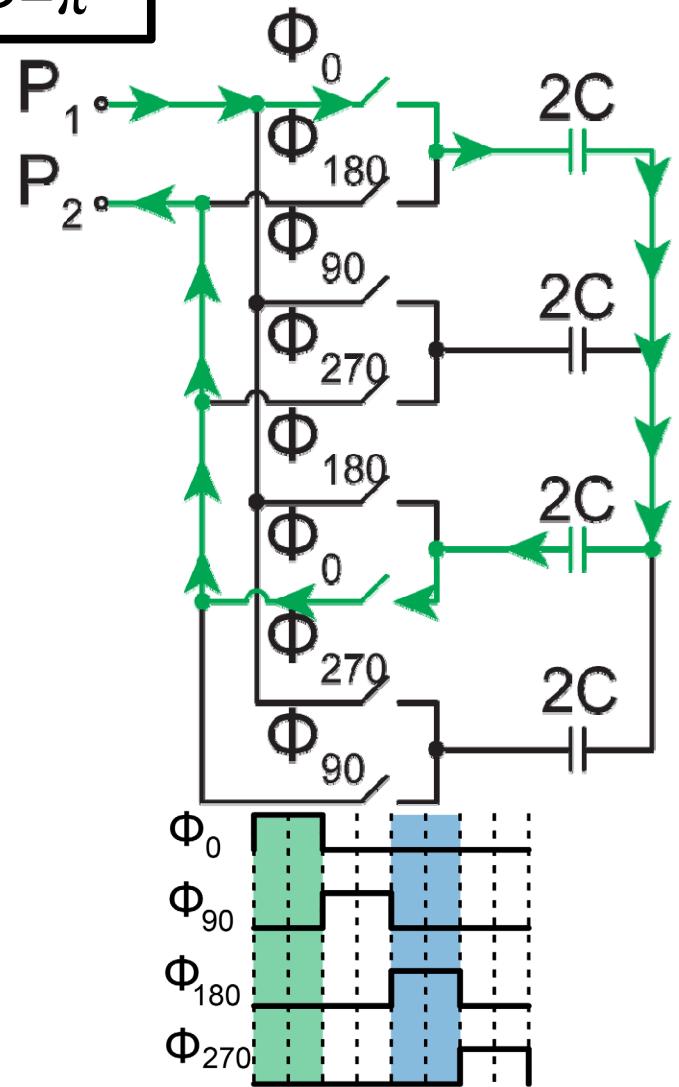
New Multi-Phase Notch Filter Structure



Enables a programmable notch depth by changing $\Delta\Phi$.

Notch Filter Evolution

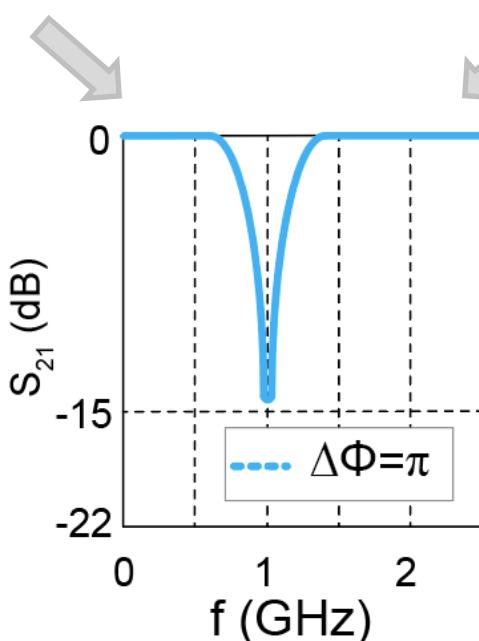
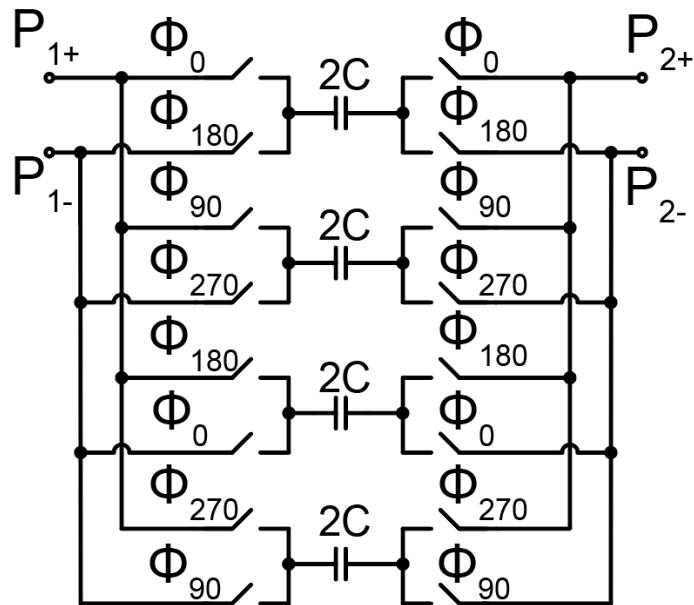
$$\Delta\Phi = \pi$$



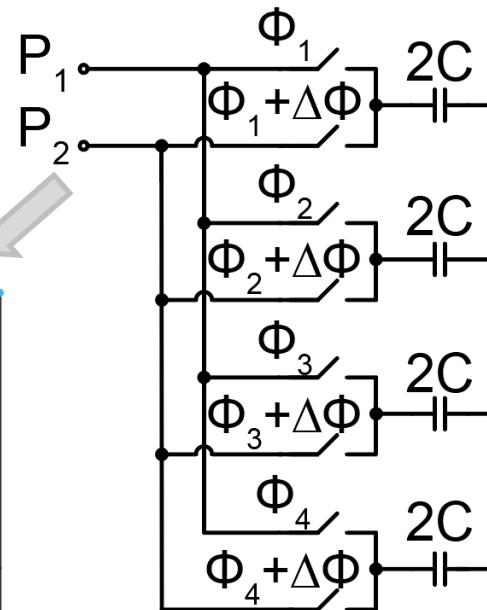
29.4: High-Performance Isolators and Notch Filters Based on N-Path Negative Transresistance

Capacitor-Shared Notch Filter Structure

Conventional Differential Notch Filter

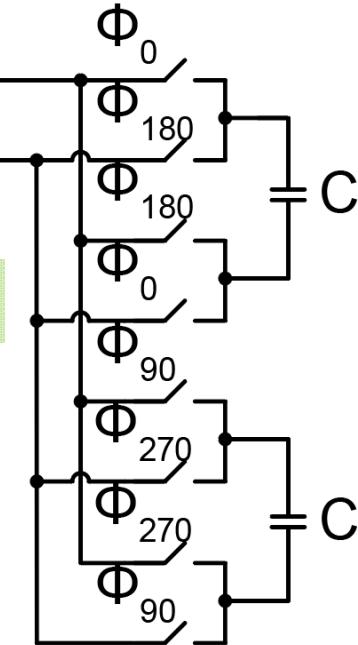


New Multi-Phase Notch Filter



for $\Delta\Phi = \pi$:

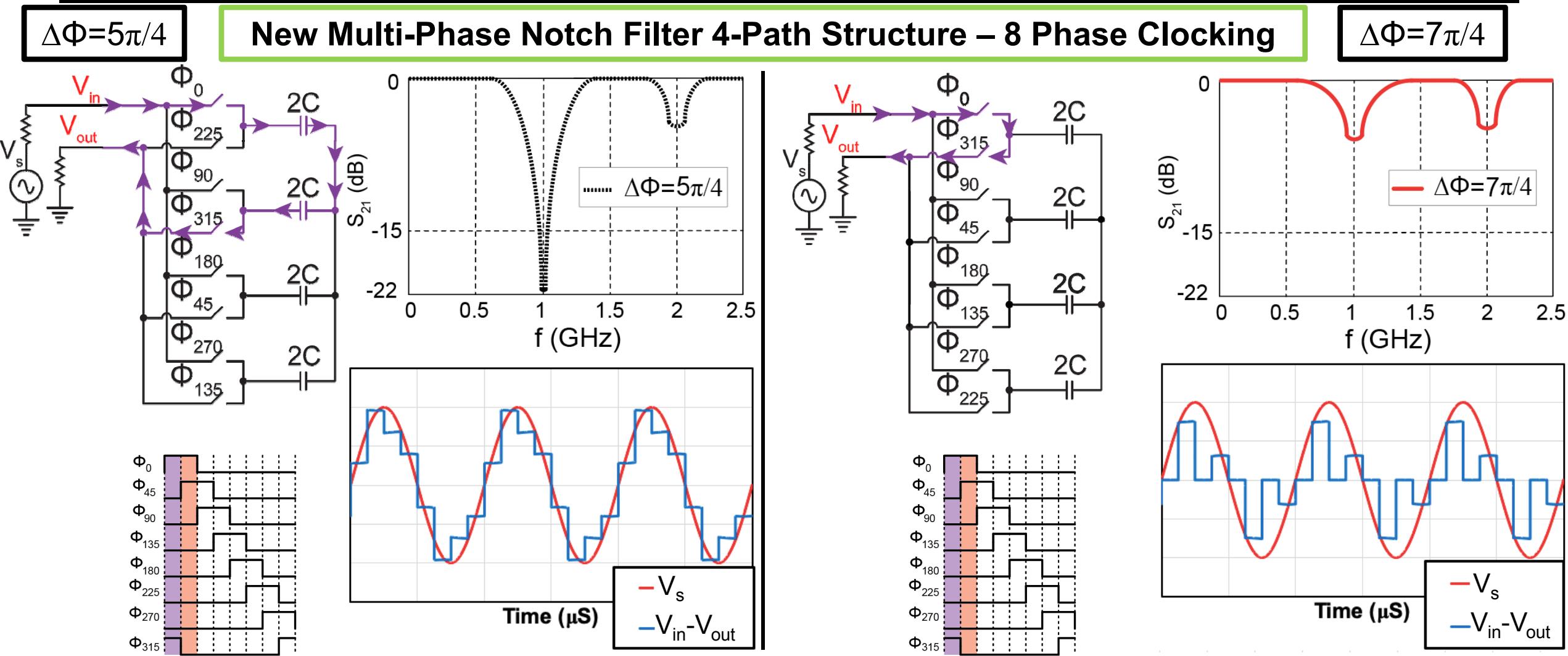
=====



Total capacitance:	8C
No. of switches:	16
Excitation mode:	Differential

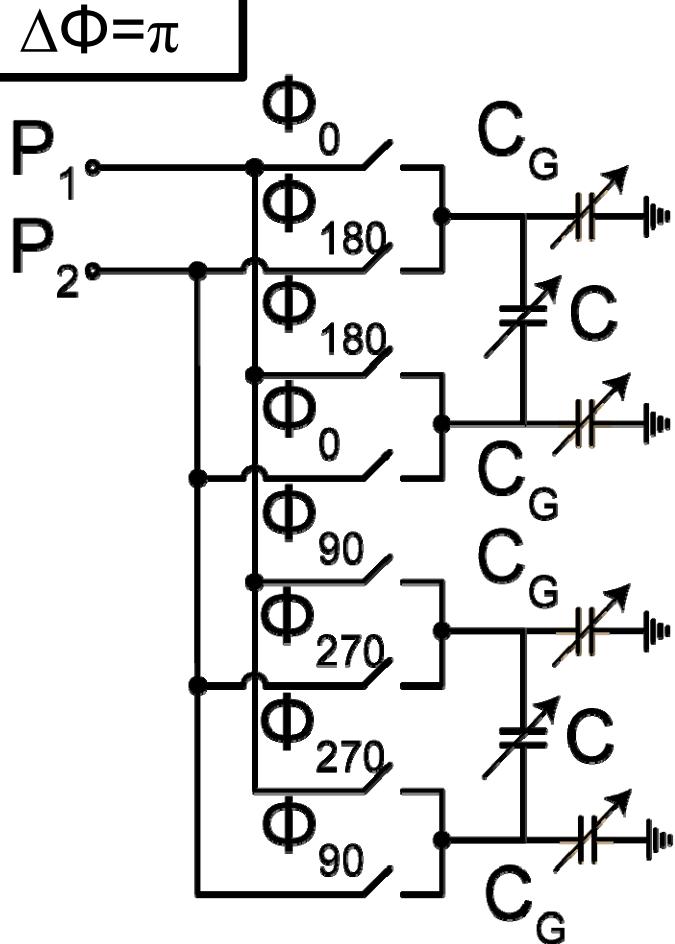
8C	Single-Ended	2C
8		8

Notch Filter Evolution

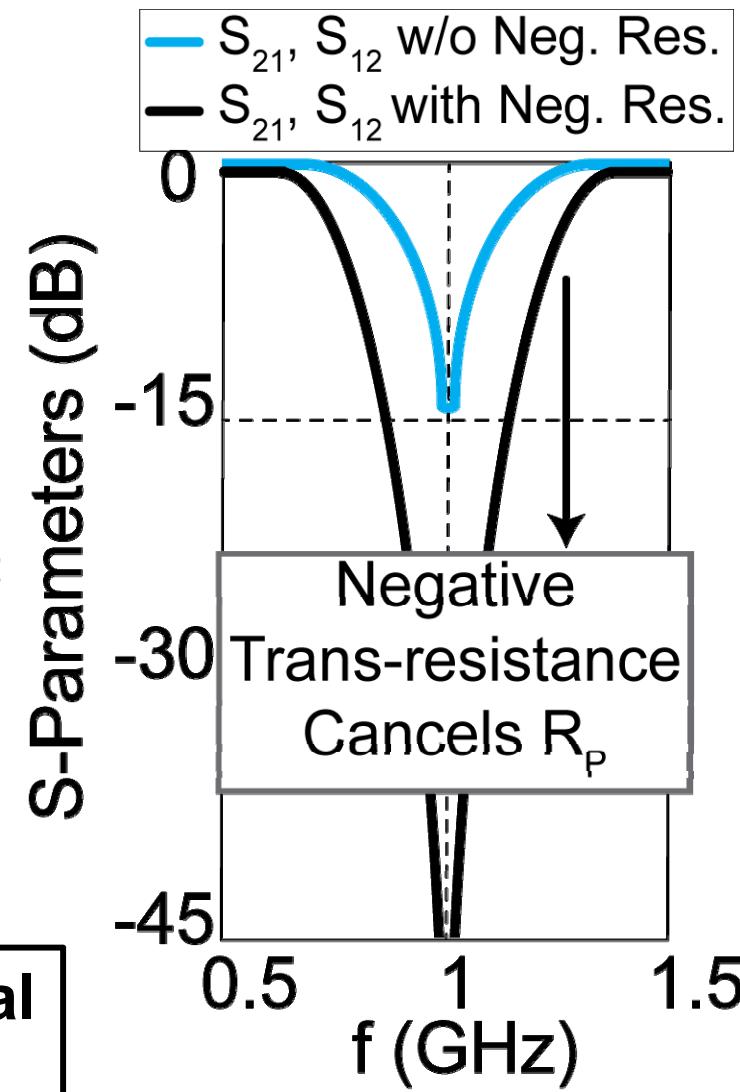
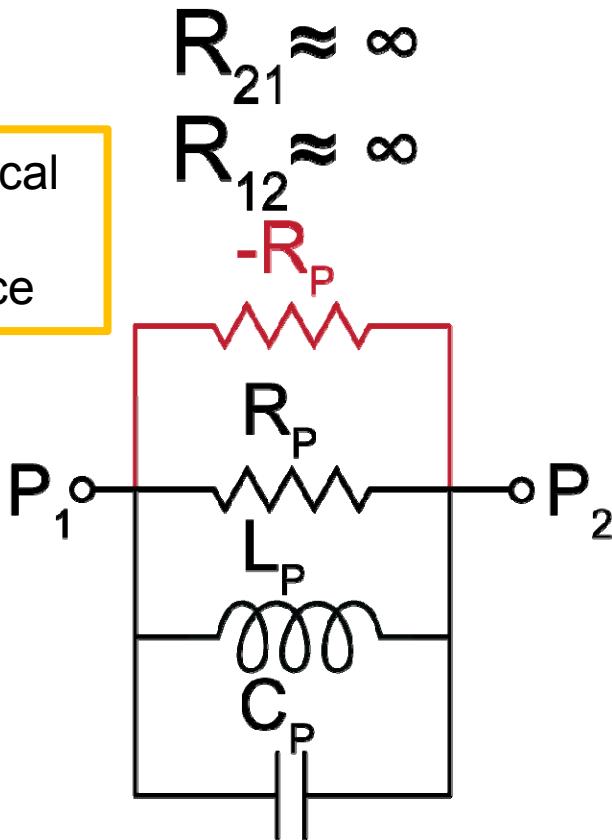


Phase shifting the clocks enable a programmable notch depth by changing $\Delta\Phi$.

Notch Filter with Negative Transresistance



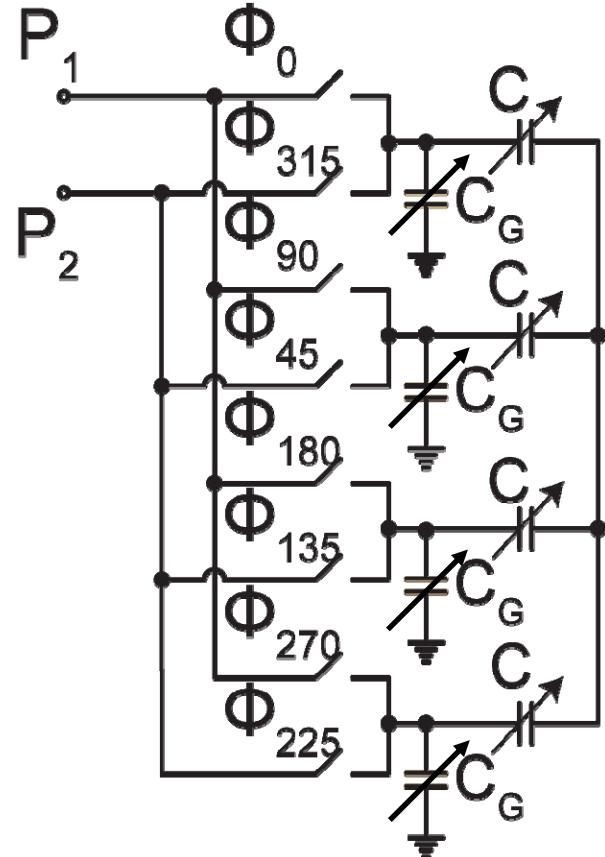
≡



Increased rejection is achieved by adding a reciprocal negative transresistance.

RF Isolator with Nonreciprocal Transresistance

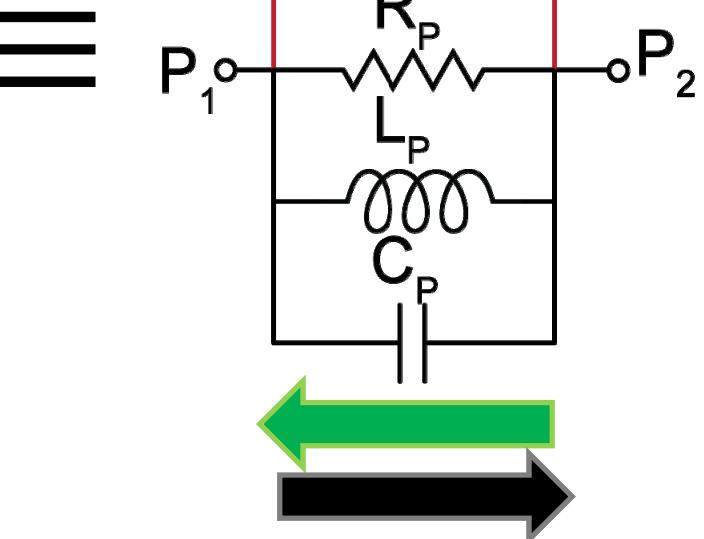
$$\Delta\Phi = 7\pi/4$$



Adding Nonreciprocal Transresistance

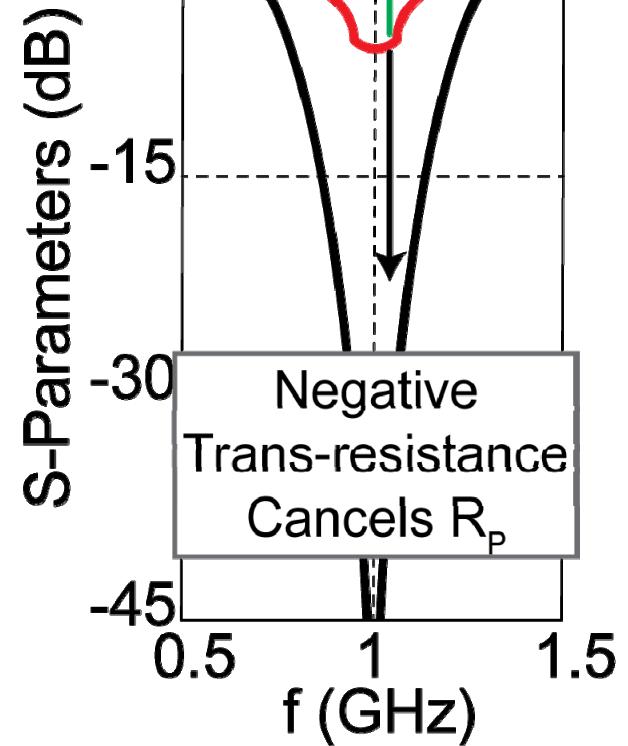
$$R_{21} \approx \infty$$

$$R_{12} \approx R_{\text{small}}$$



Low loss and high rejection is achieved in the opposite direction by using a nonreciprocal transresistance.

Reducing R_p creates a low-loss passband

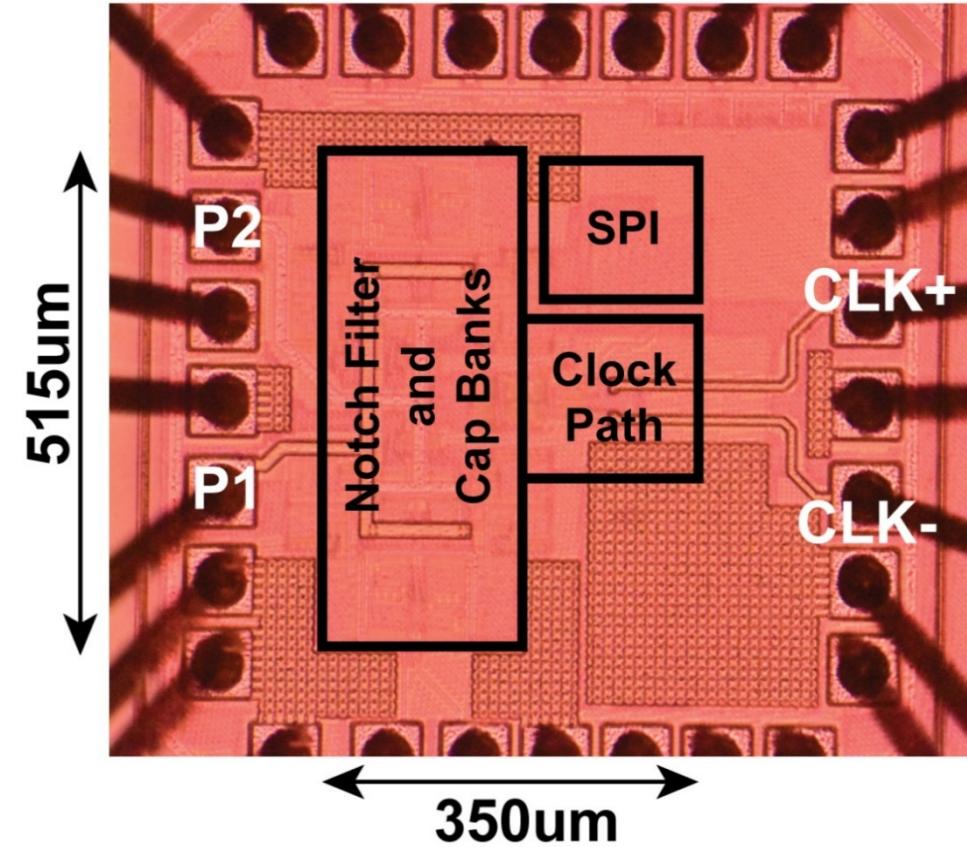
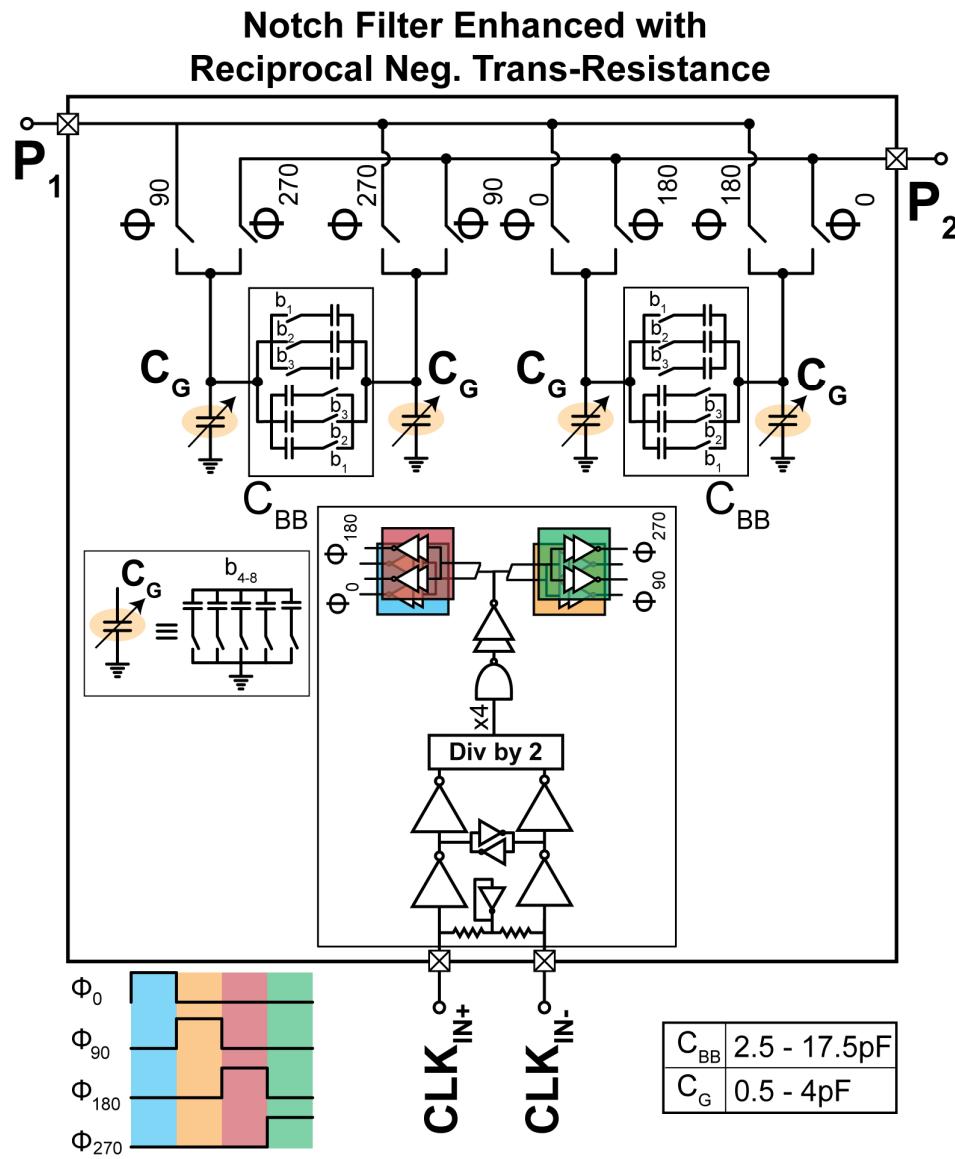


- S_{21}, S_{12} w/o Neg. Trans-Res.
- S_{12} with Neg. Trans-Res.
- S_{21} with Neg. Trans-Res.

Presentation Outline

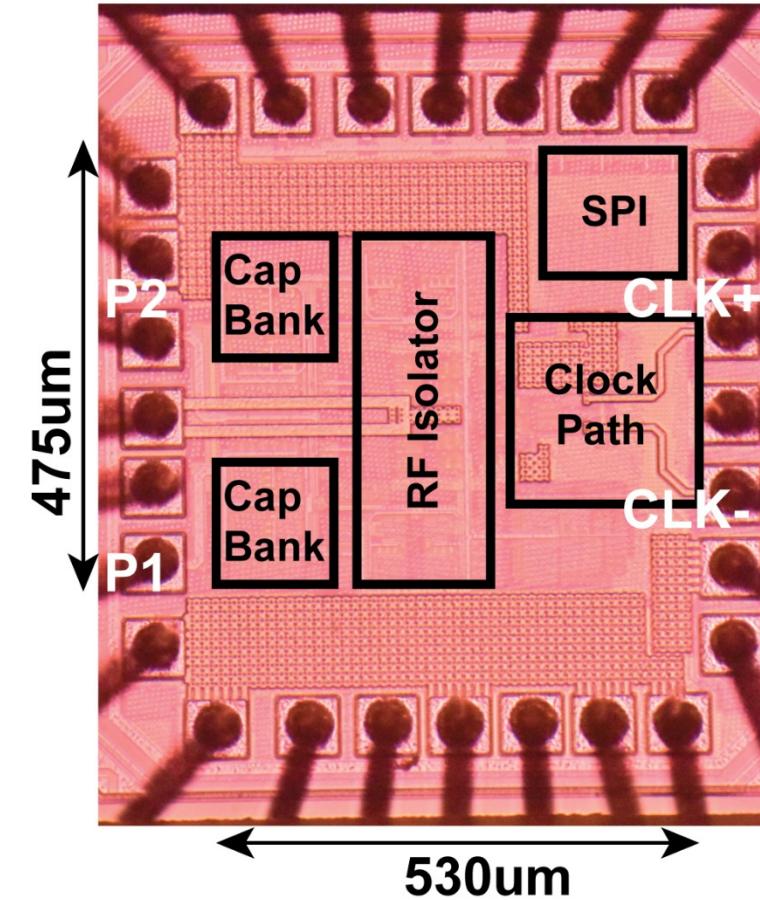
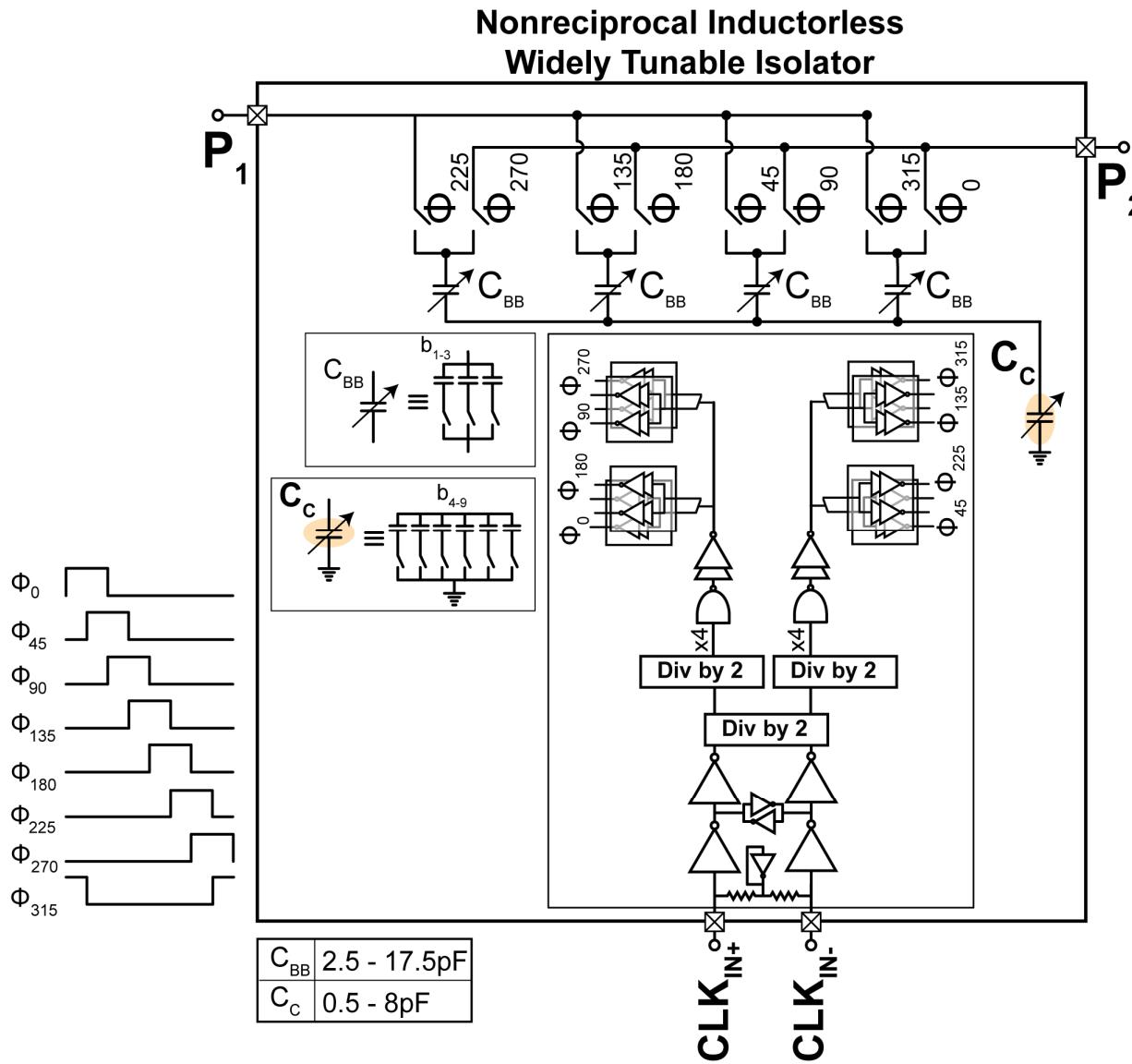
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Circuit Implementation (Notch Filter)



29.4: High-Performance Isolators and Notch Filters Based on N-Path Negative Transresistance

Circuit Implementation (RF Isolator)

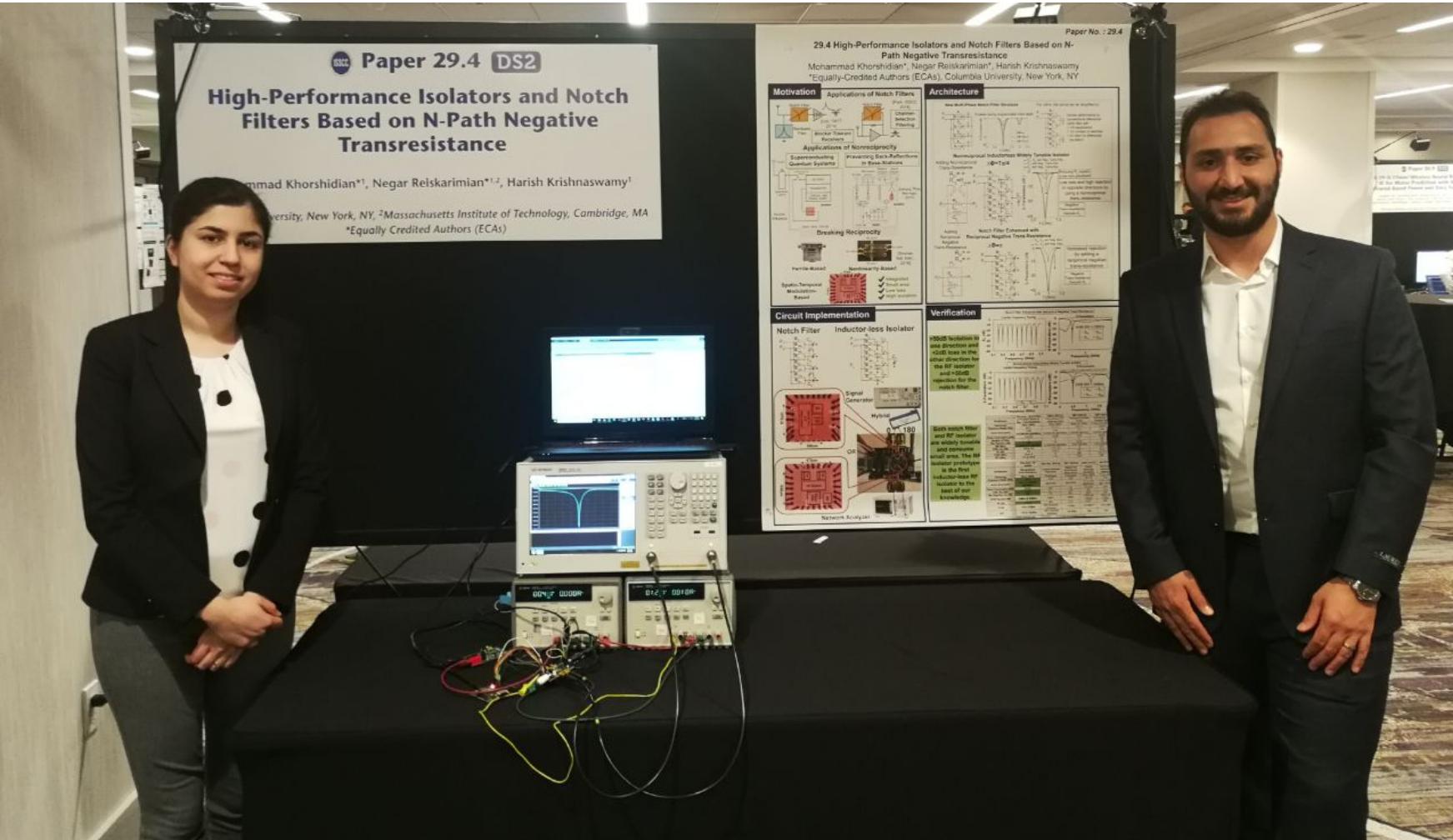


29.4: High-Performance Isolators and Notch Filters Based on N-Path Negative Transresistance

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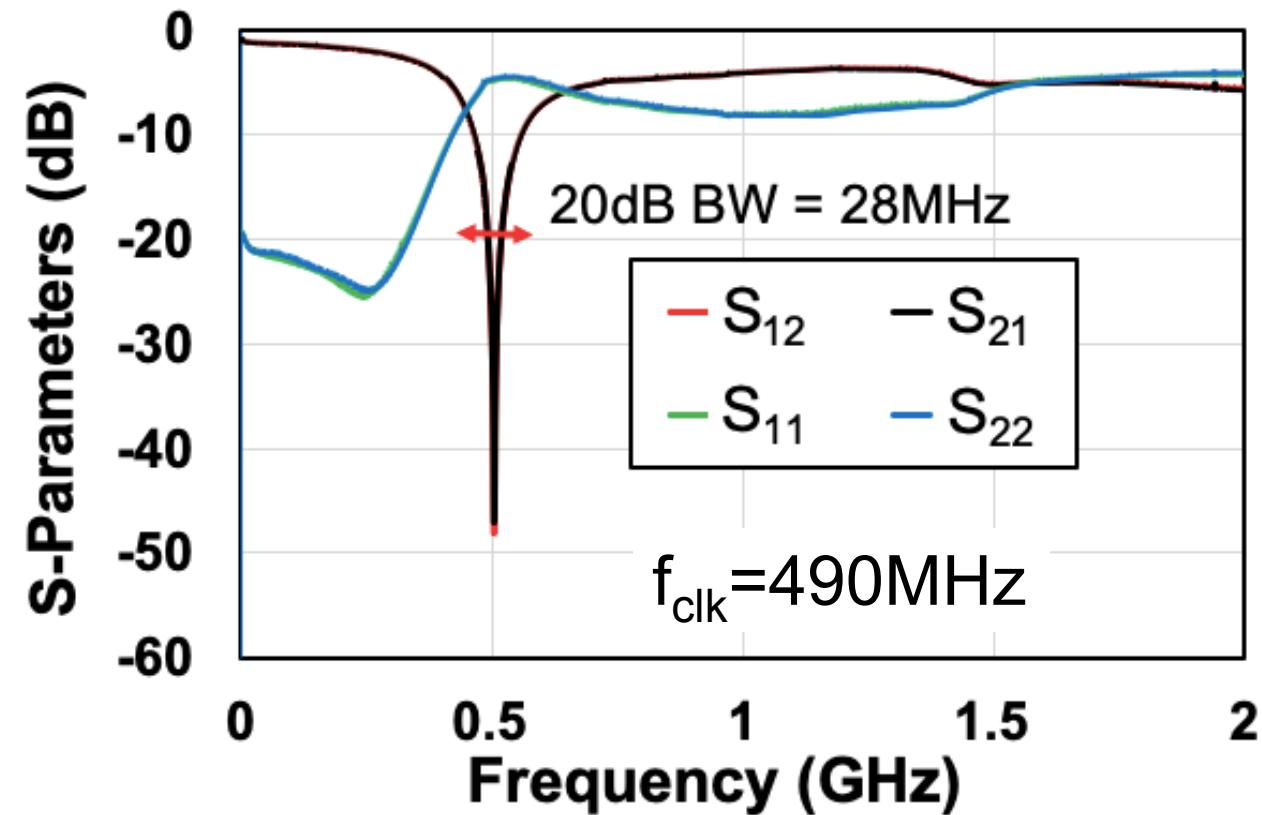
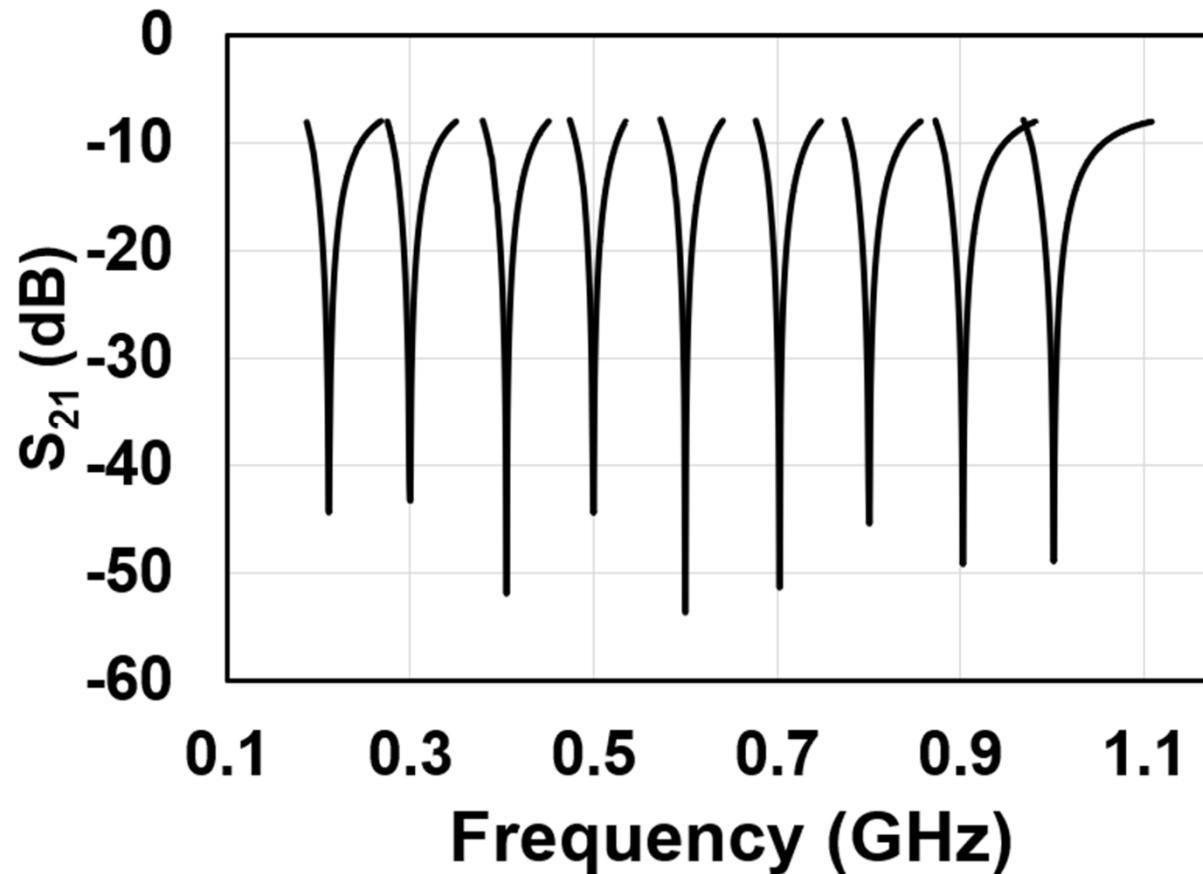
Demonstration



This work was demonstrated in Demo Session 2 on Tuesday.

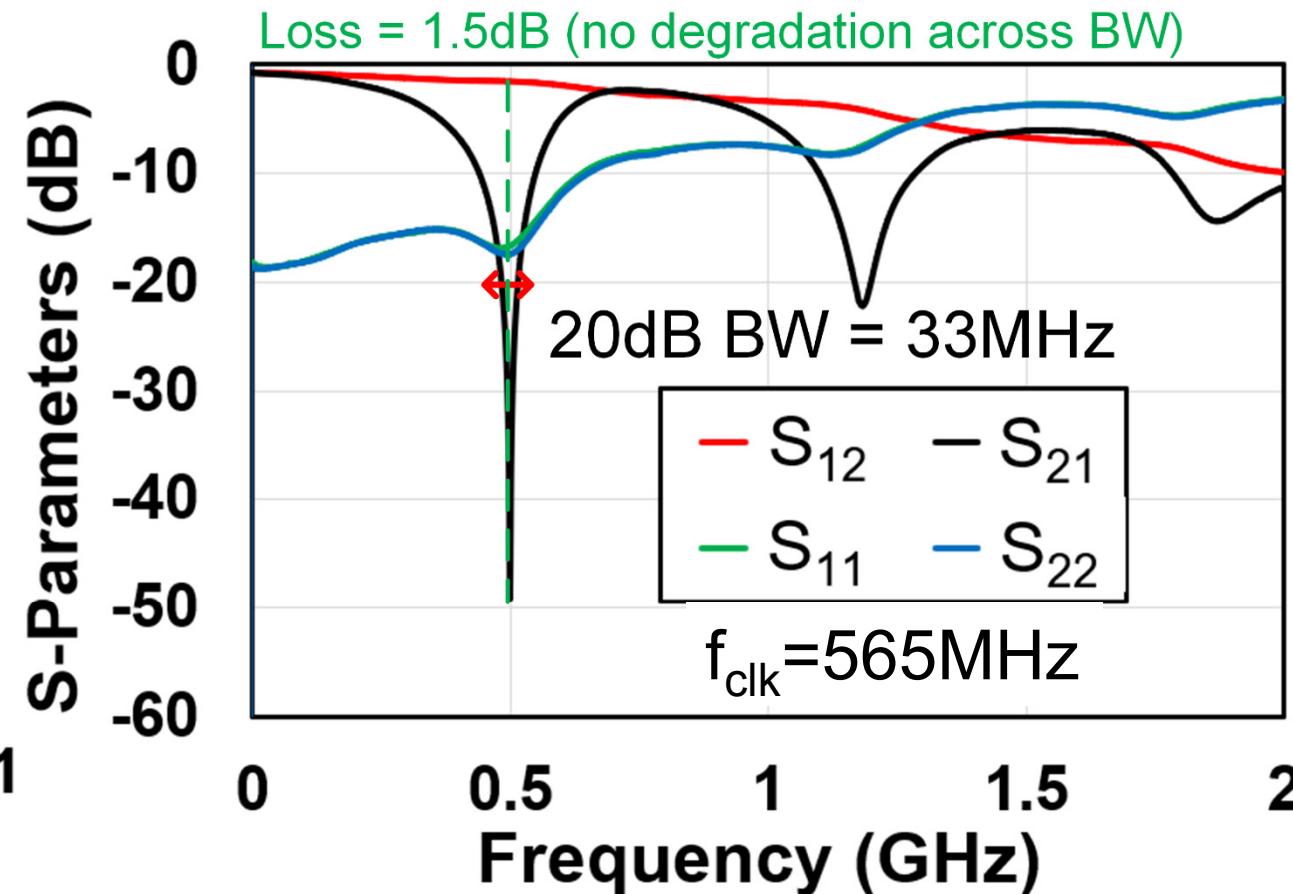
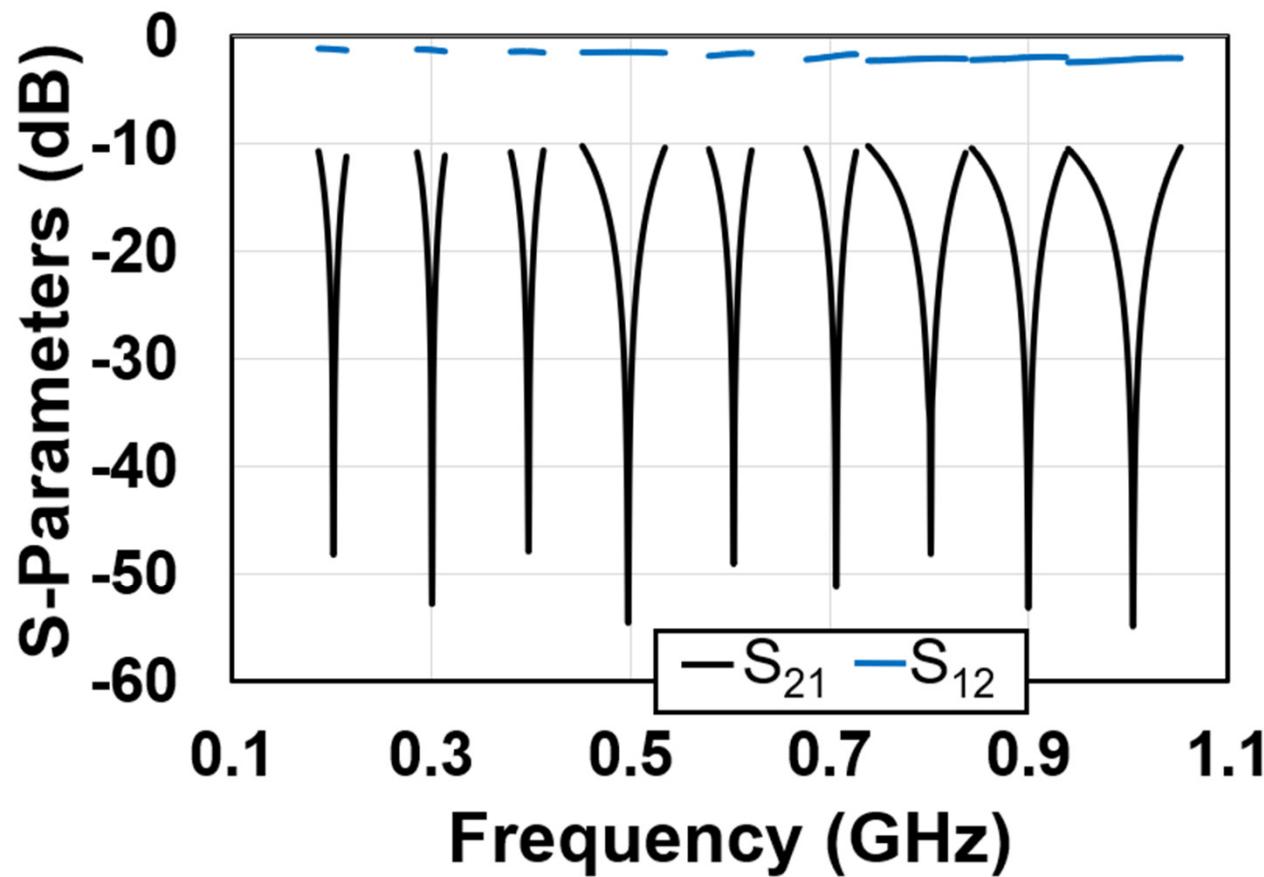
Measurement Results (Notch Filter)

Notch filter enhanced with reciprocal negative transresistance



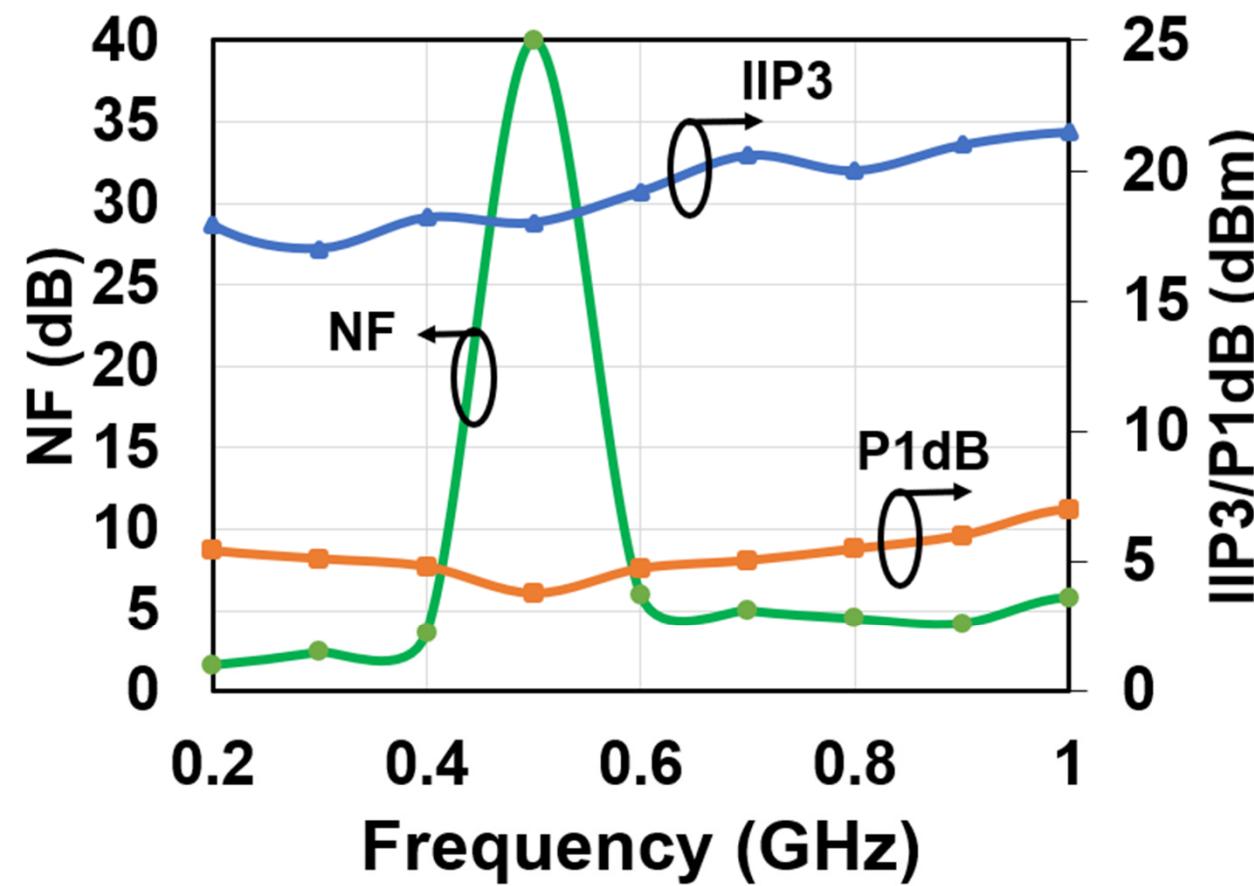
Measurement Results (RF Isolator)

Nonreciprocal inductorless widely tunable isolator

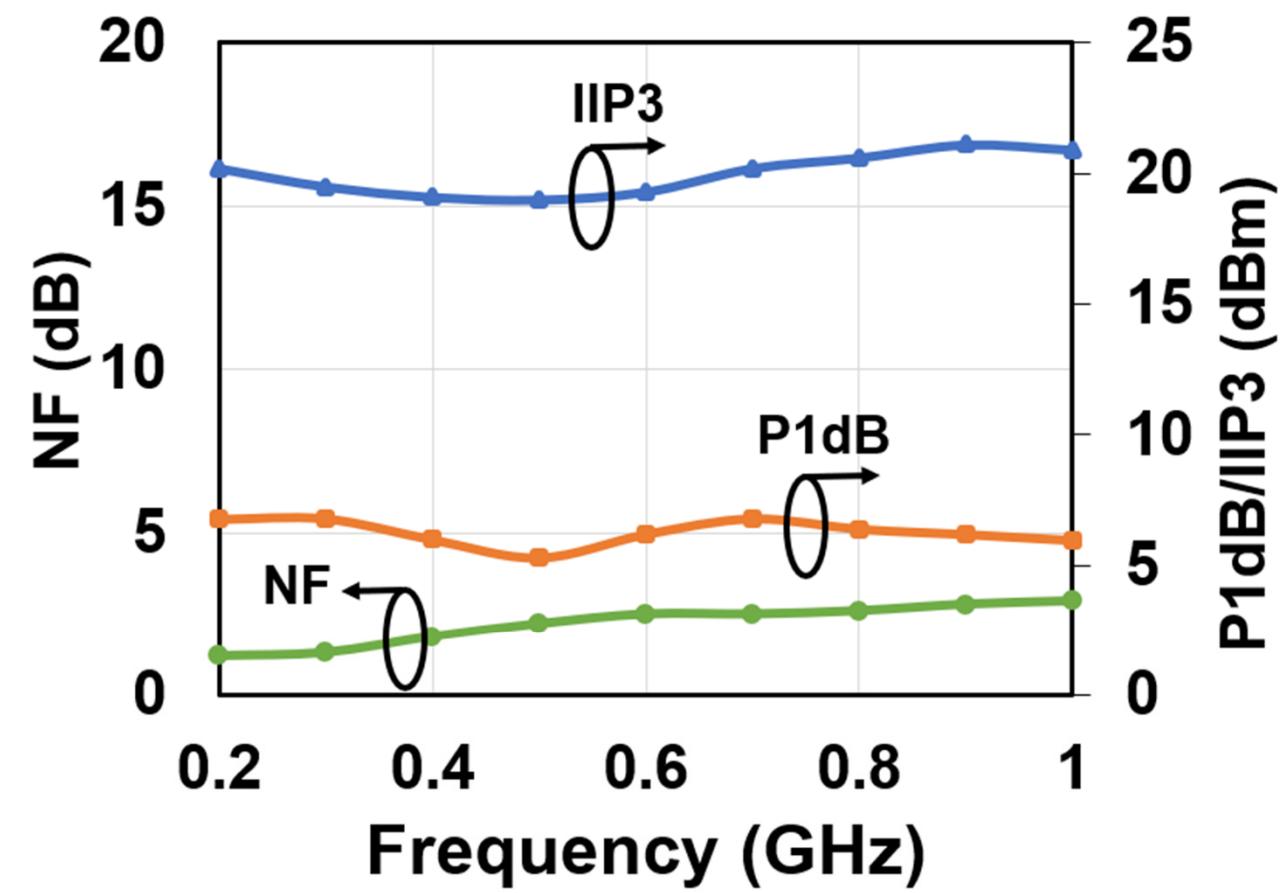


Measurement Results

Notch Filter Enhanced with Reciprocal Negative Trans-Resistance



Nonreciprocal Inductorless Widely Tunable Isolator



Comparison Table (Notch Filter)

	This work – Notch Filter	ISSCC 2012 [1]	TMTT 2019 [3]	TMTT 2016 [5]
Architecture	LPTV Notch Based on Neg. Trans-Resistance	Conventional LPTV Differential Notch	Impedance-Inverted N-Path	Q-Enhanced LC + Synthetic Notch
Technology	65nm CMOS	65nm CMOS	45nm SOI CMOS	0.13um SiGe BiCMOS
Frequency Range (GHz)	0.2 to 1	0.1 to 1.2	0.9 to 1.1	2.25 to 4.5
Active Area (mm ²)	0.18 $\lambda^2/2,000,000$ (@500MHz)	0.14 $\lambda^2/2,600,000$ (@500MHz)	1.77 $\lambda^2/50,000$ (@1GHz)	0.48 $\lambda^2/20,000$ (@3GHz)
Power Consumption (mW)	7.2 to 13.2	3.5 to 30	6.18	66 to 99
Number of Paths	4	8	4	N/A
Max Rejection (dB)	>50	22	20 to 23	70
BW (MHz)	28 (20dB BW) @500MHz	6 (18dB BW) @500MHz	12 to 25 (3dB BW)	4 to 40 (20dB BW)
OOB Loss (dB)	-0.8 to -3.5	-1.4 to -2.5	-3	0 to 1*
NF (dB)	1 to 4	1.6 to 2.5	4 to 5	12 to 13
P1dB (dBm)	+5 to +7	+6	N/R	-2 to -1.5
IIP3 (dBm)	+17 to +21.5	>+17	+22.6	N/R

*: Positive numbers represent gain.

Comparison Table (RF Isolator)

	This work – RF Isolator	Nat. Elec. 2018 [4]	TMTT 2019 [6]	JSSC 2019 [7]	IMS 2016 [8]
Architecture	Nonreciprocal Trans-Resistance	Coupled Nonlinear Resonance	Magnet-less Nonreciprocal Metamaterials	Serially Resonated Modulators	Distributedly Modulated Capacitors
Technology	65nm CMOS	PCB-Based	PCB-Based	65nm CMOS	0.1um GaN
Frequency Range (GHz)	0.2 to 1	0.75	2.05	85 to 110	0.5 to 3
Active Area (mm²)	0.25, $\lambda^2/1,440,000$ (@500MHz)	N/R (PCB)	N/R (PCB)	0.13, $\lambda^2/70$ (@100GHz)	11.76 [†] , $\lambda^2/2500$ (@1.75GHz)
Power Consumption (mW)	9.6 to 24	N/A	15	9.6 to 12.9	5.4 [†]
Loss, S₁₂ (dB)	1.1 to 2	2.1	1.03	5.6	1 to 4
Max Rejection, S₂₁ (dB)	>50	>30	36.2	46.5	>25
20dB Rejection BW	33MHz @ 500MHz	70MHz	13MHz	1.5GHz @ 110GHz	1.8GHz @ 1.6GHz
NF (dB)	1.5 to 2.5	N/R	21.2	4.53**	N/R
P1dB	+5 to +7dBm	N/R (Inherently Nonlinear)	+17dBm	+10.9dBm**	+10.5 dBm
IIP3	+19 to +22dBm	N/R (Inherently Nonlinear)	+34.5dBm	N/R	N/R

**: Simulation. †: LO path not integrated on chip.

Presentation Outline

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Conclusion

- A negative transresistance structure has been introduced.
- The structure can be engineered to provide nonreciprocal transresistance or reciprocal negative transresistance.
- Negative transresistance is employed to build high performance notch filters and isolators.
- Fully integrated 65nm CMOS inductorless passive isolator and notch filter validate the claims.

Acknowledgement

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- Special thanks to:
 - Dr. Tim Hancock, Dr. Troy Olsson, and Dr. Ben Epstein from DARPA,
 - Prof. Andrea Alù from CUNY ASRC, and
 - CoSMIC Lab group members for fruitful discussions.