Thank you for your attention

THzID: A 1.6mm^2 Package-Less Cryptographic Identification Tag at 260GHz

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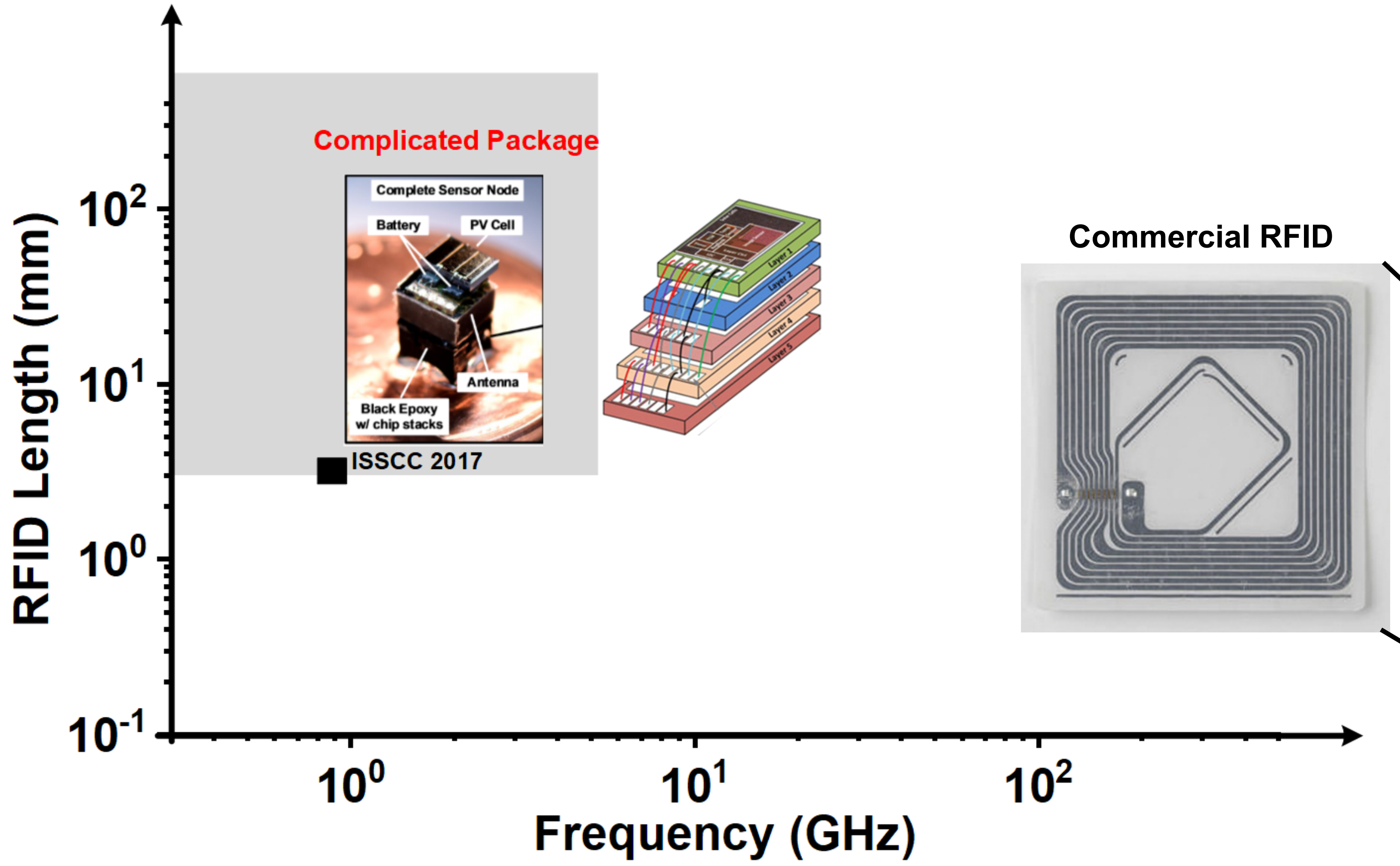
Outline

- Introduction
- 260GHz Package-Less Cryptographic THzID
  - 260GHz Backscattering Module
  - Downlink Circuitry
  - Optical-Power Harvesting
  - Cryptographic Processor
- Measurement Results
- Conclusion

Radio Frequency Identification (RFID) Tags

- RFIDs are used in ID cards, supply chain, authentication and other applications



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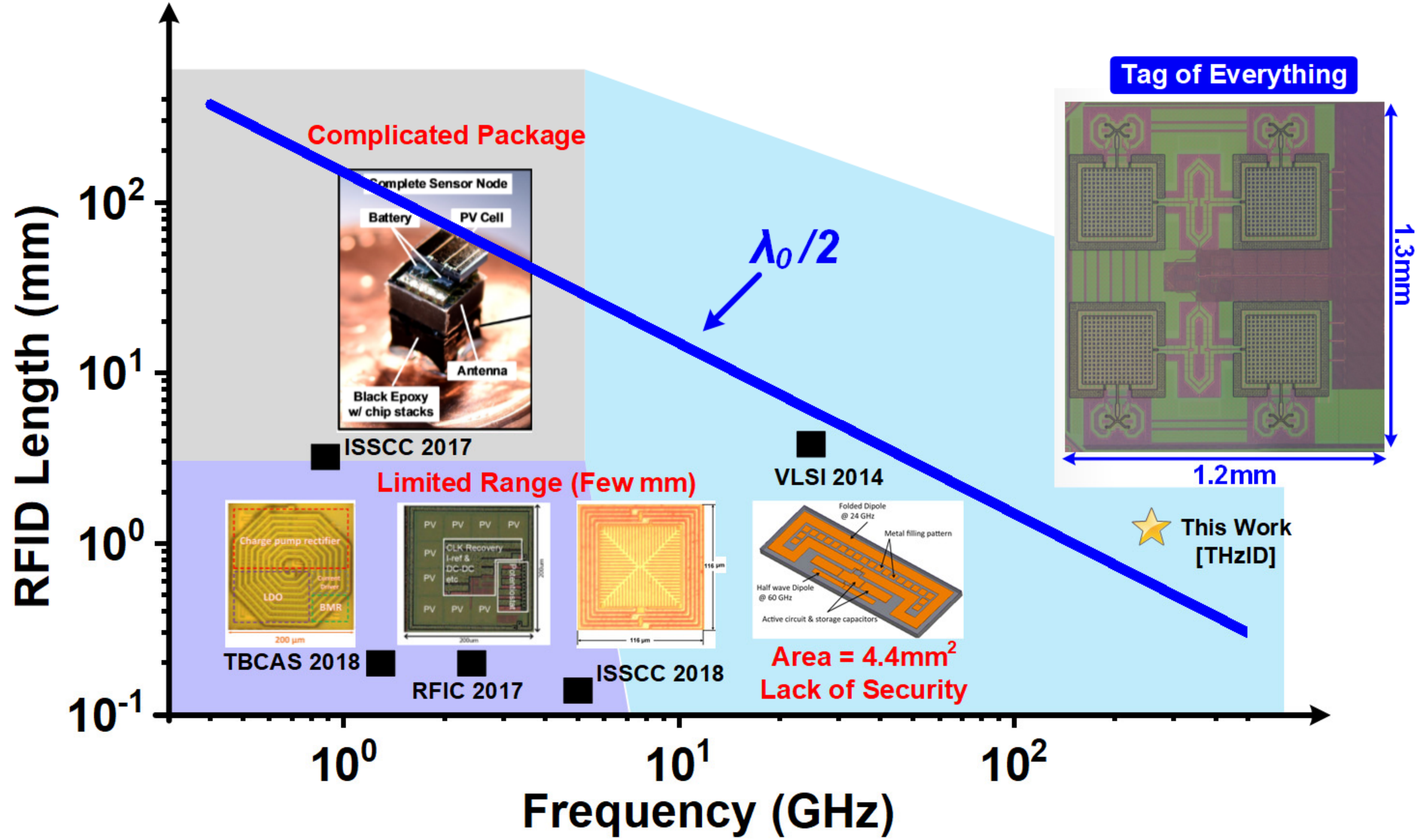
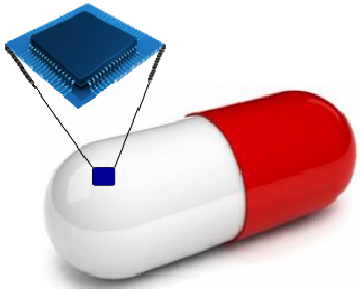
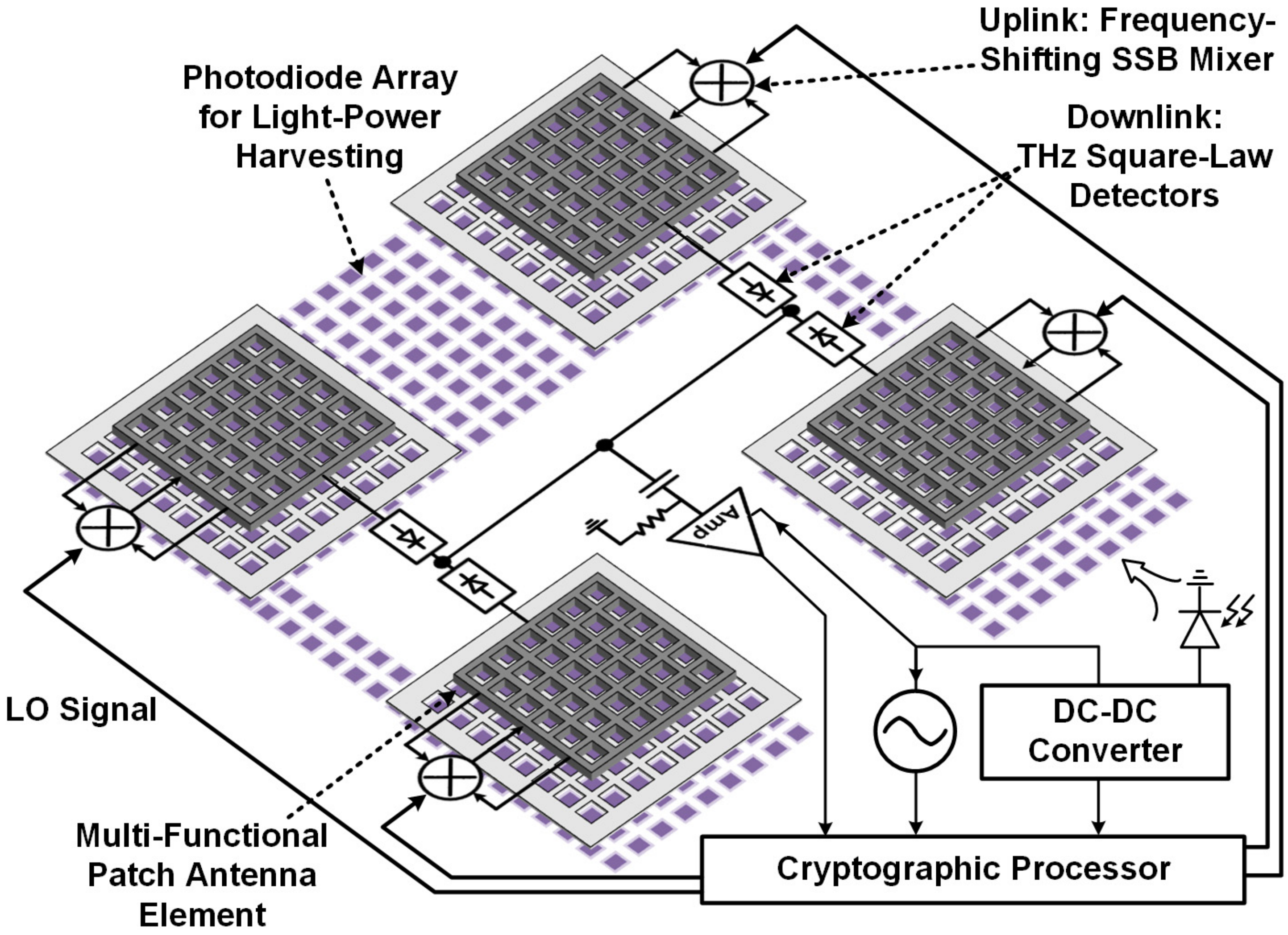




Cryptographic Package-Less THzID



THz frequency → Small antenna size

Antenna array → Increase gain & Beam-steering

Fully passive and compact communication module

Tightly integrated photovoltaic cells for powering

Cryptographic processor for authentication

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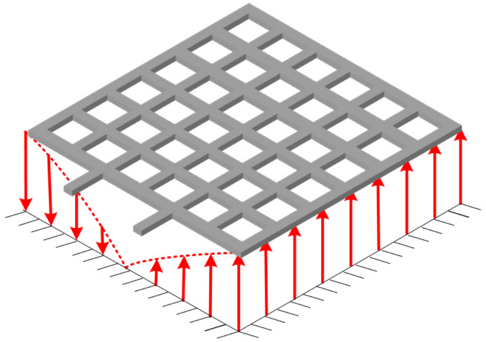
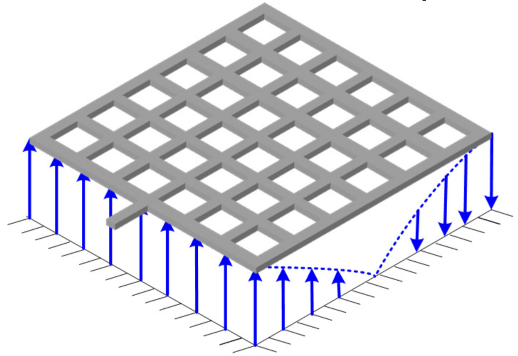
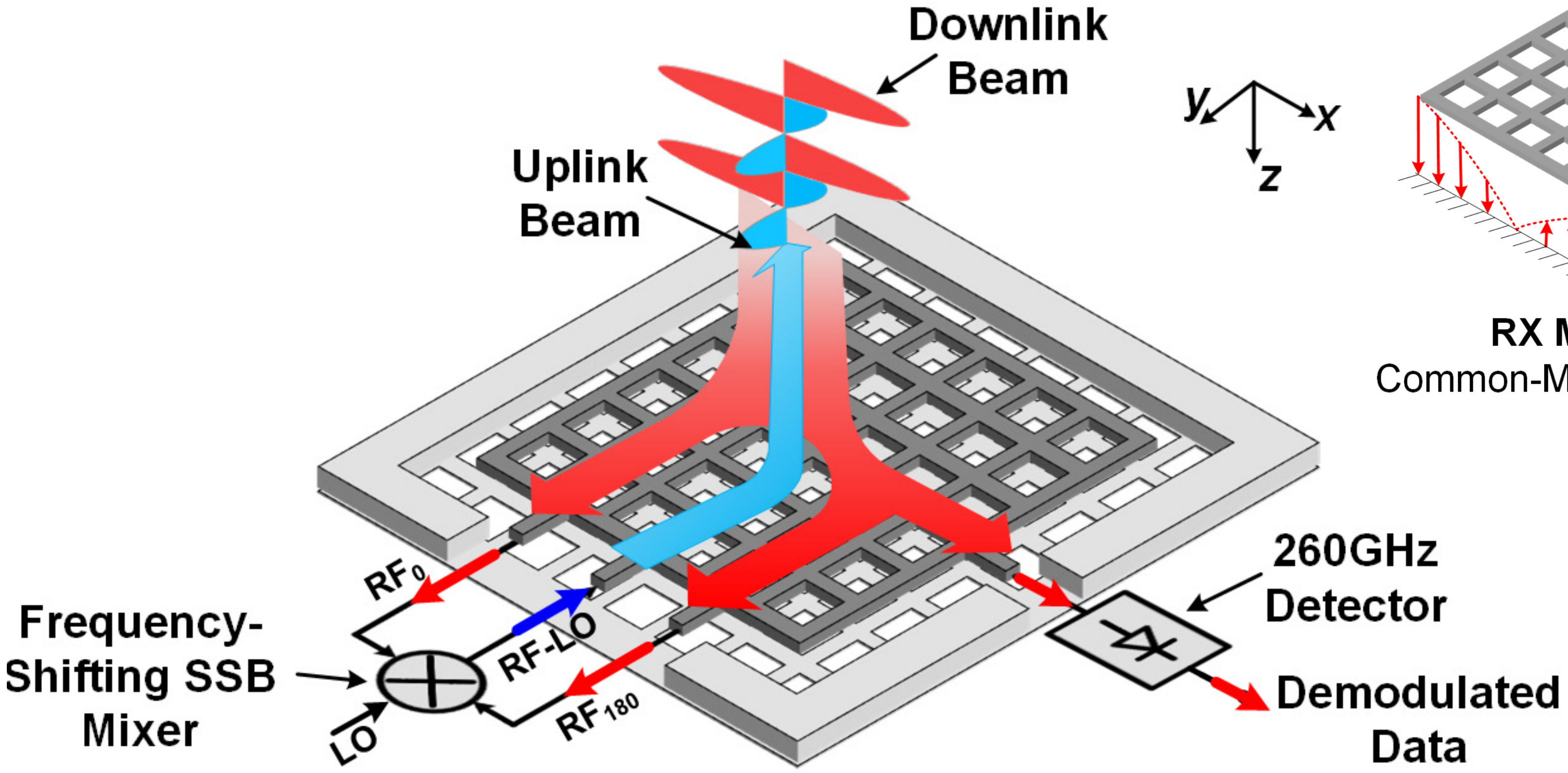
Multi-Functional Patch Antenna

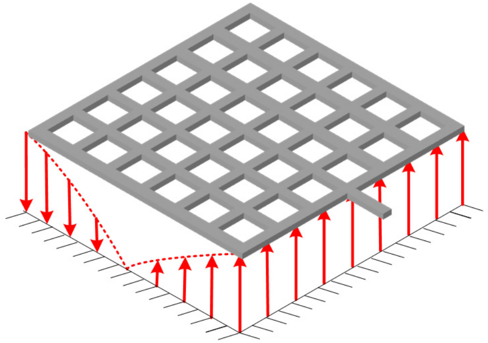


RX Mode (TM_{10})
Differential SSB Mixer Input



TX Mode (TM_{01})
Common-Mode Mixer Output

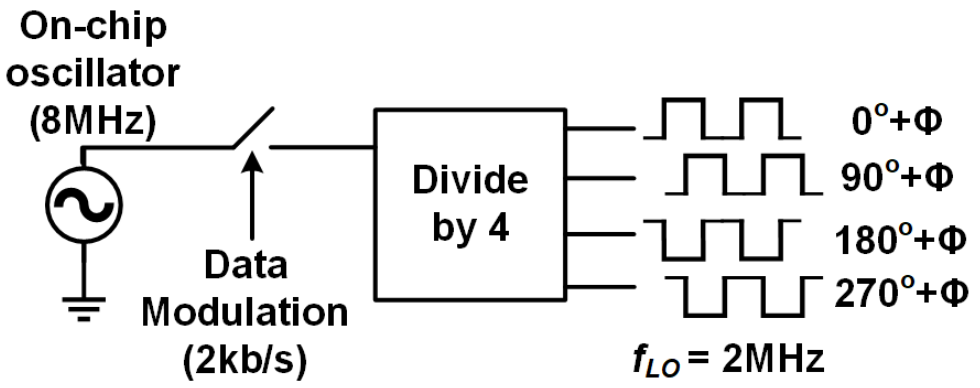


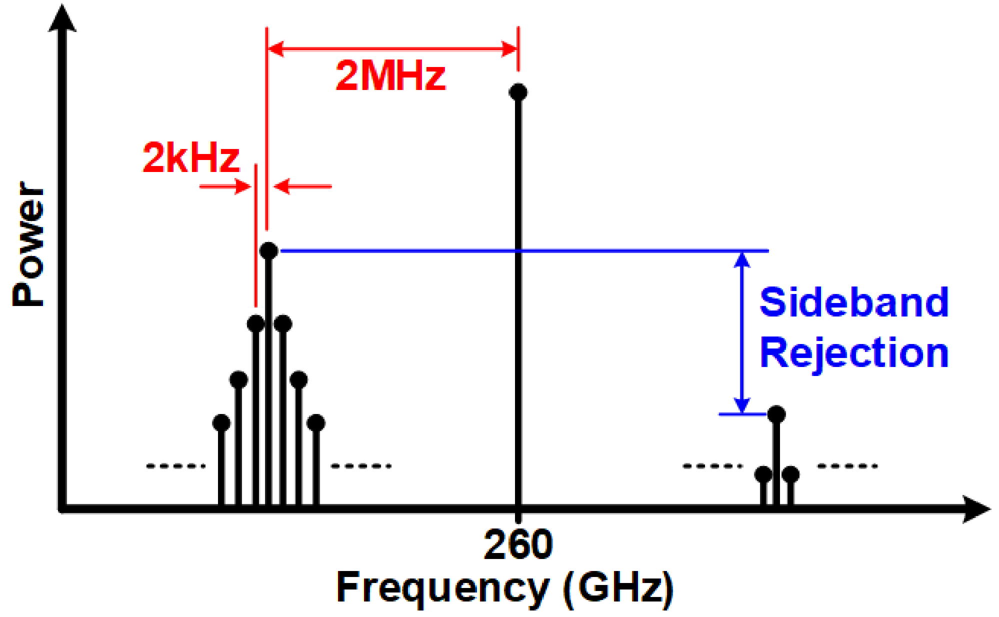


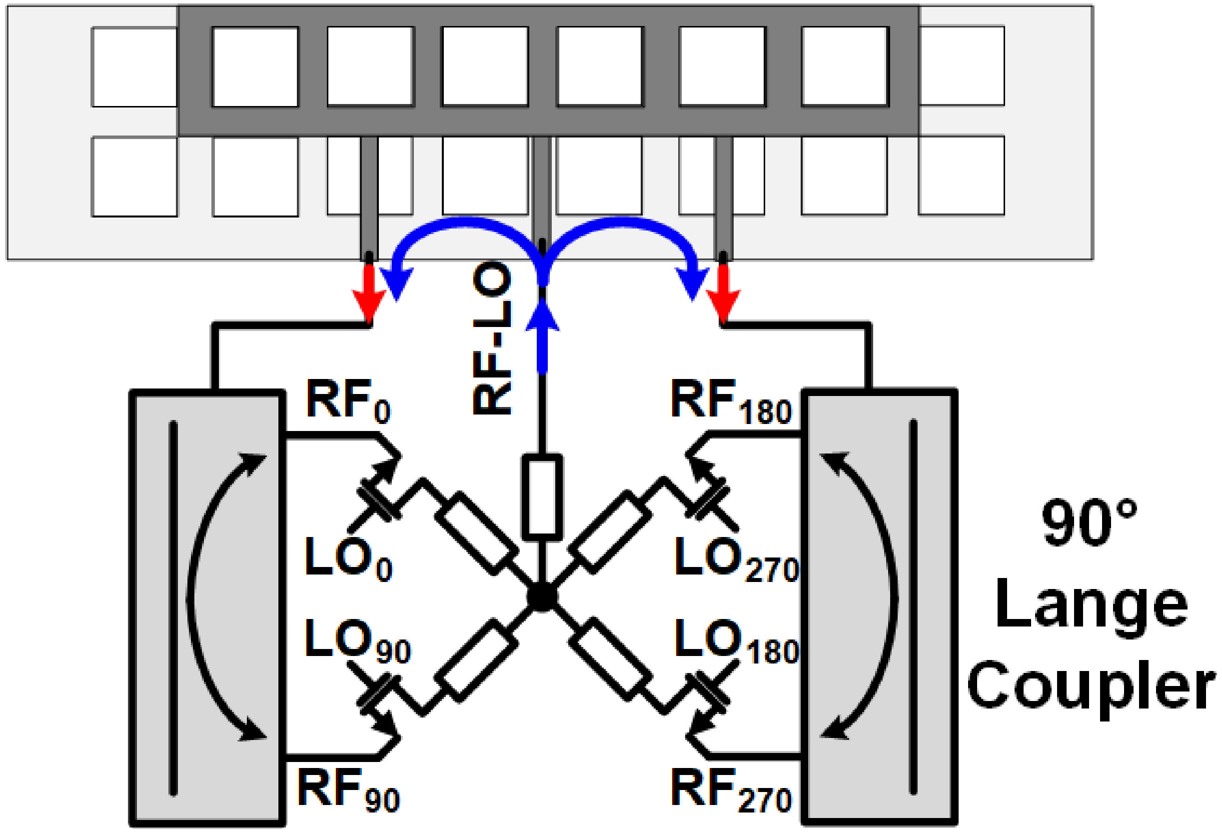
RX Mode (TM_{10})
Common-Mode Detector Input

- **Equal power splitting between mixer and detector**
- **Orthogonal polarization of the RX and TX modes resulting in 25dB rejection for the reflection from the surrounding**

Frequency-Shifting Backscattering Module

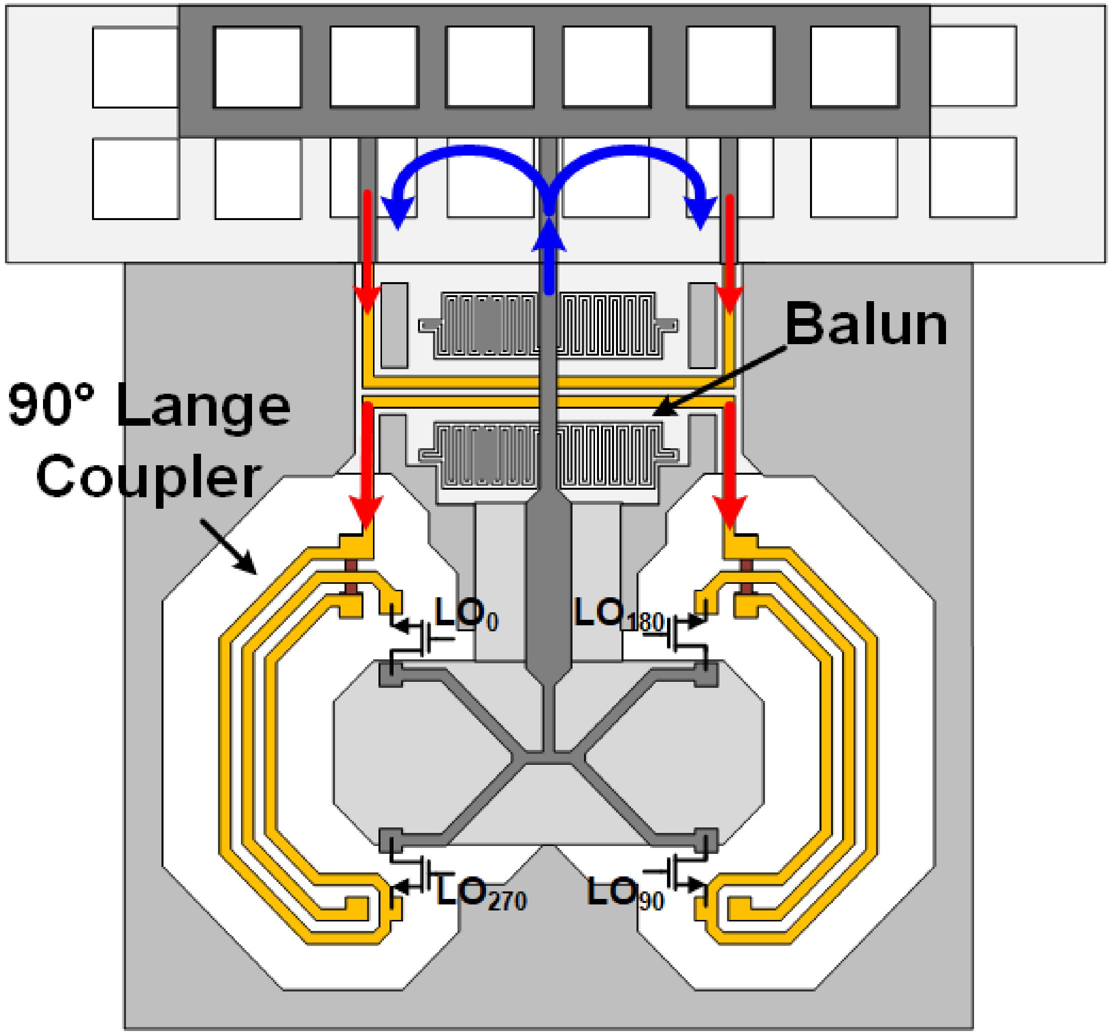


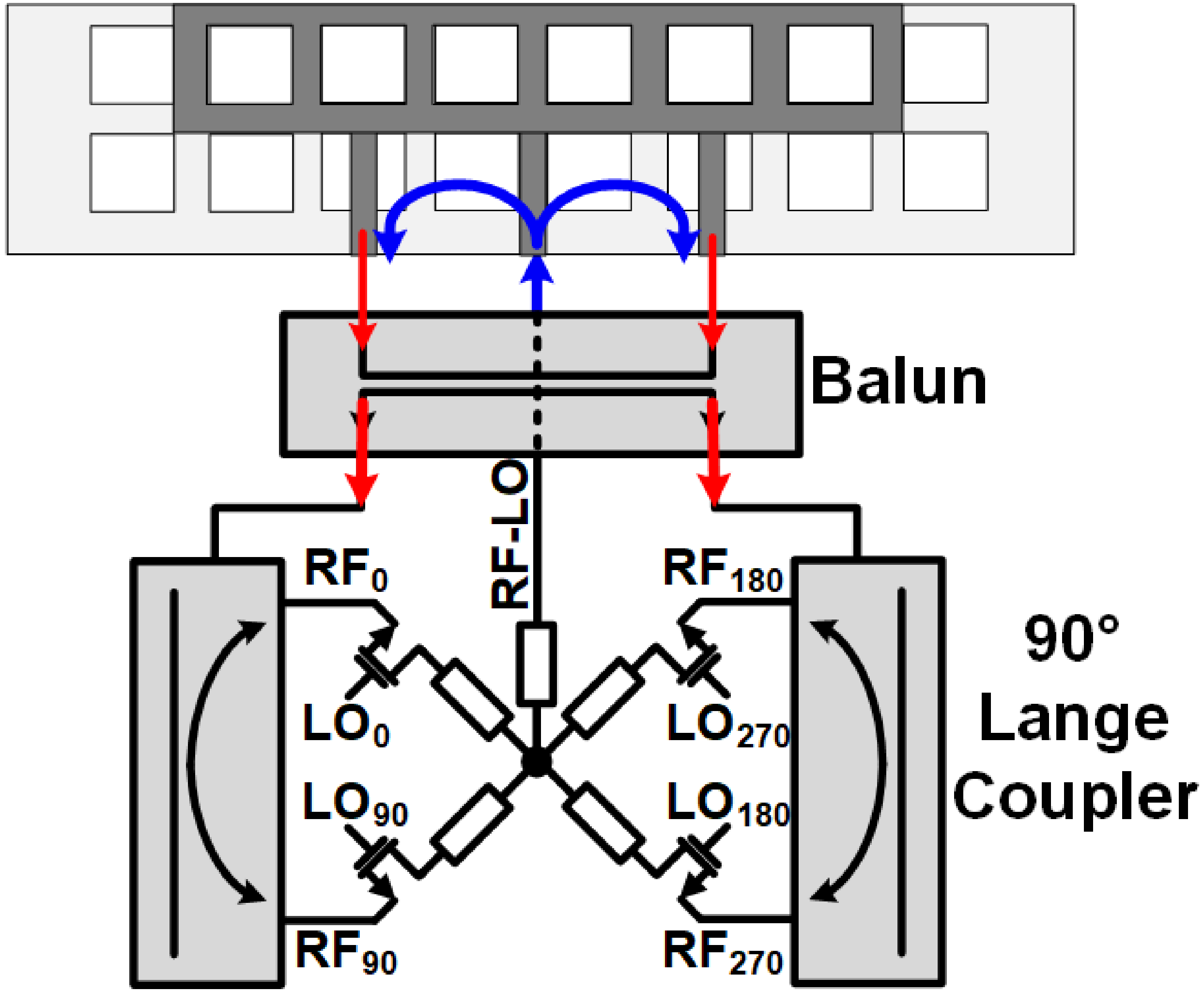




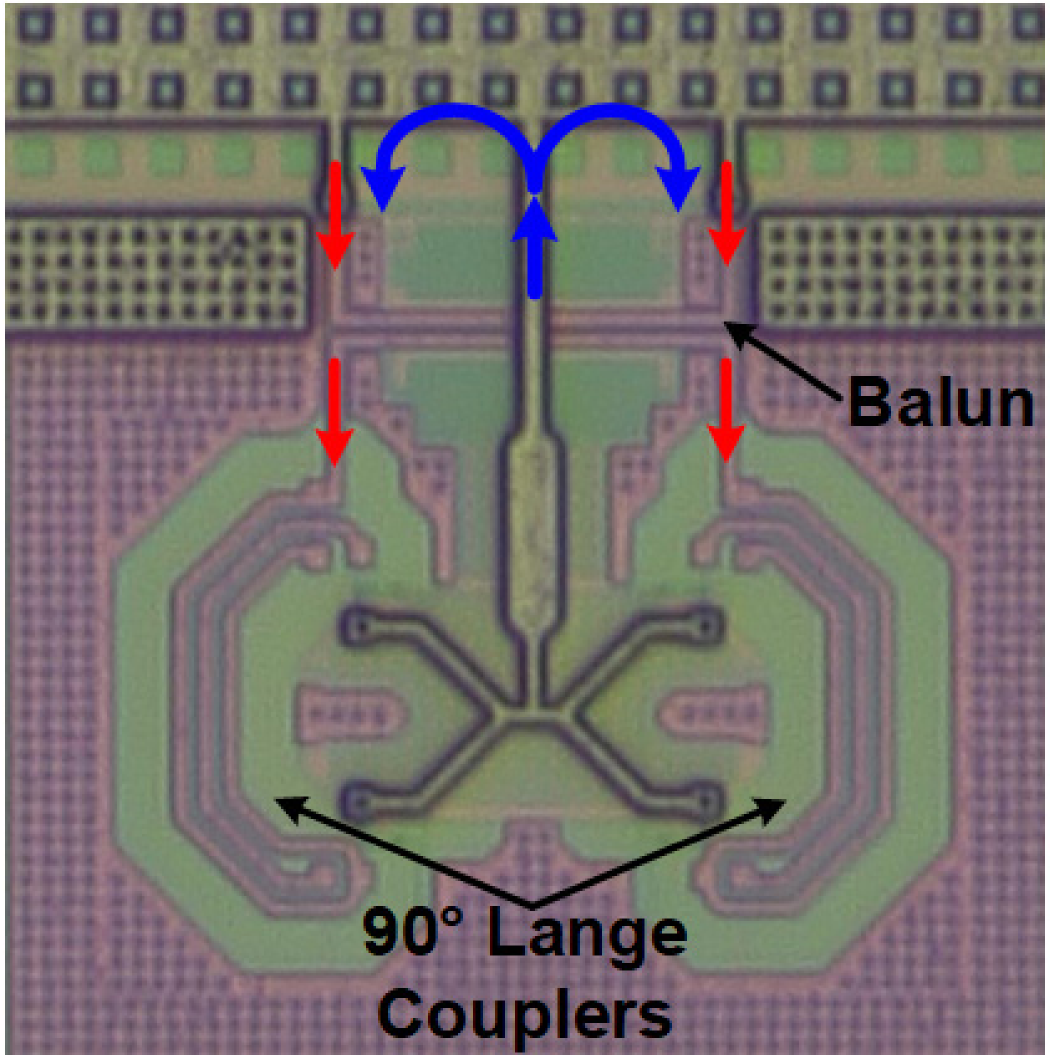
- The uplink data rate is 2kb/s
- Changing the LO phase (Φ) allows for beam-steering

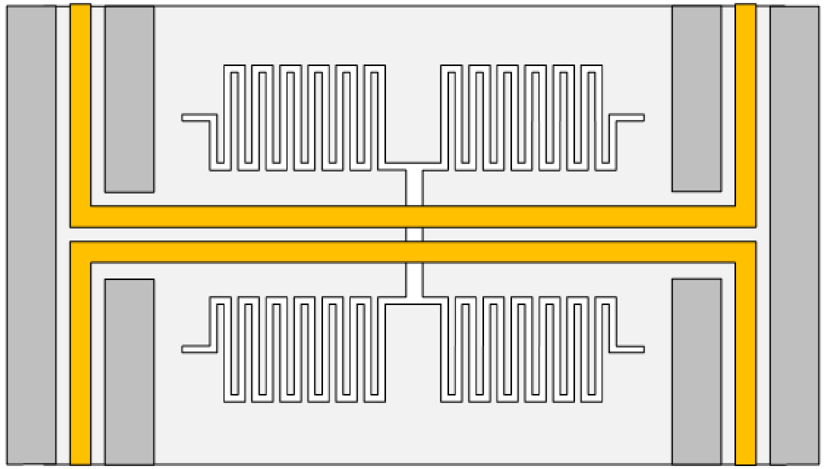
Frequency-Shifting Backscattering Module





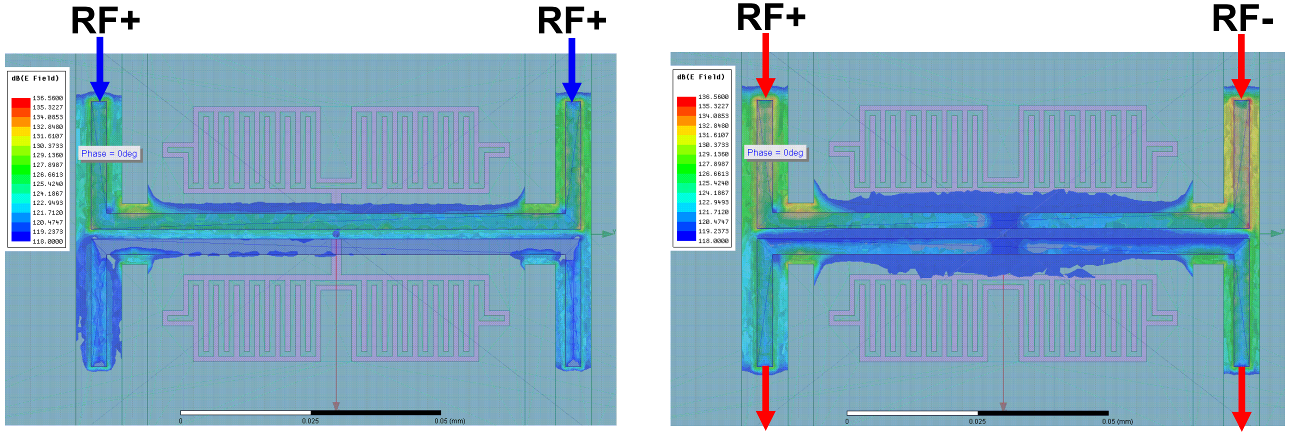
Differential Slot Balun Performance





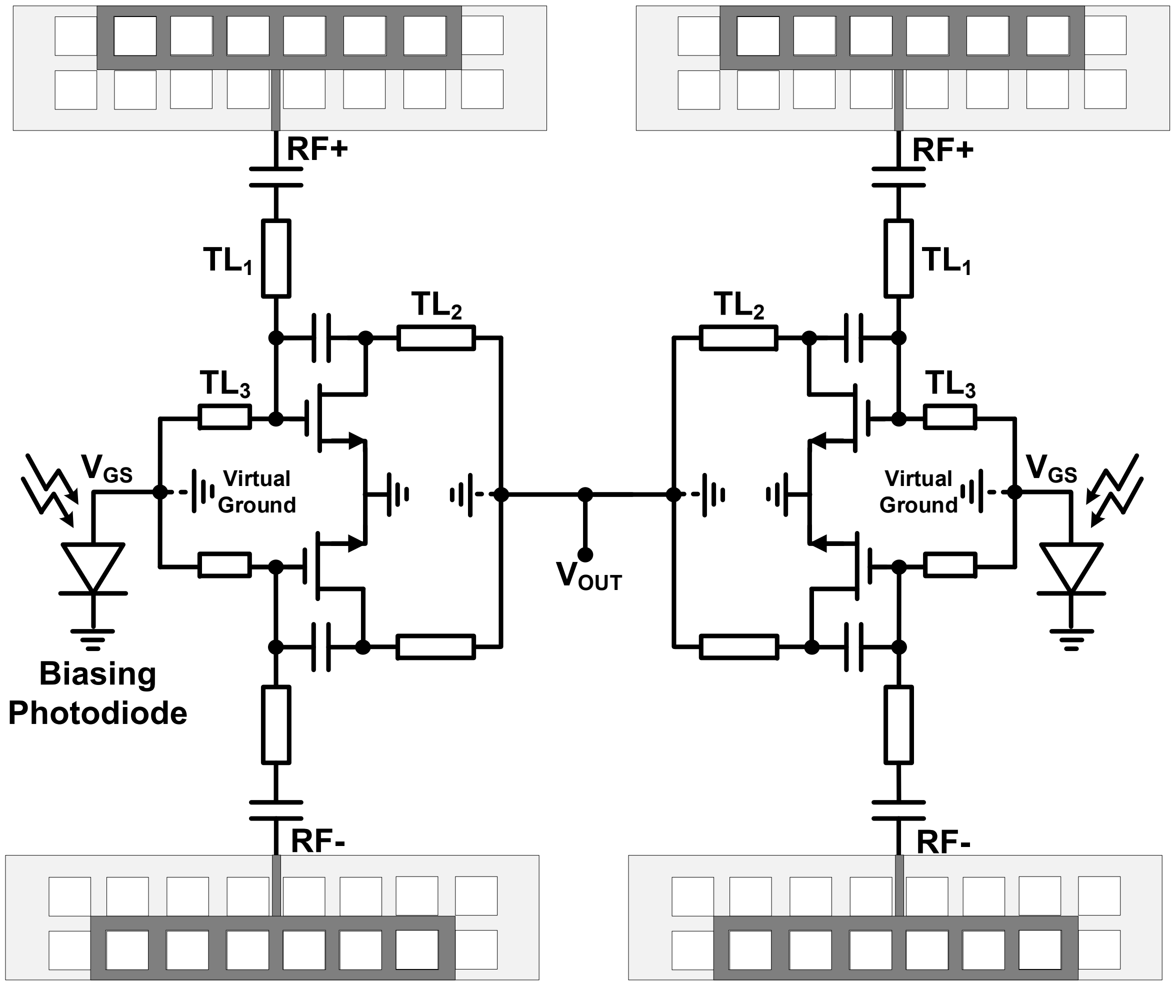
Common Mode

Differential Mode

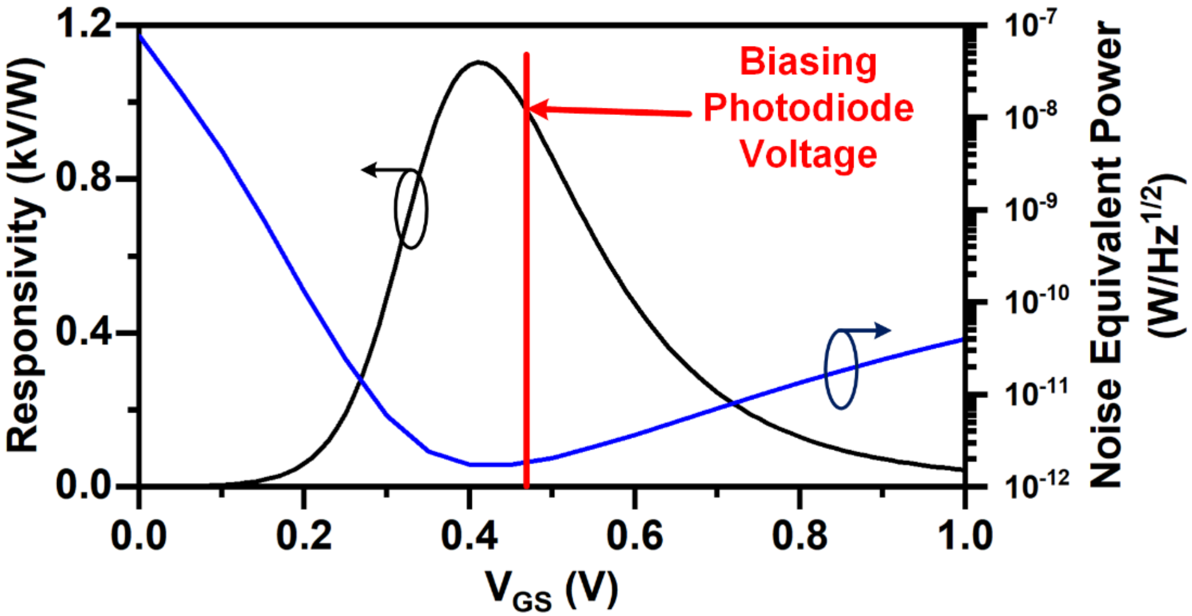


- Diff. to common mode isolation is 10dB

260GHz Square-Law Detector

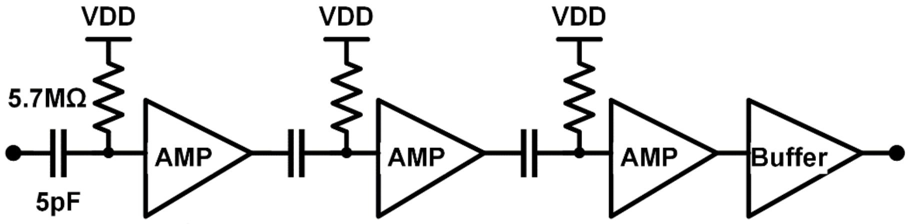


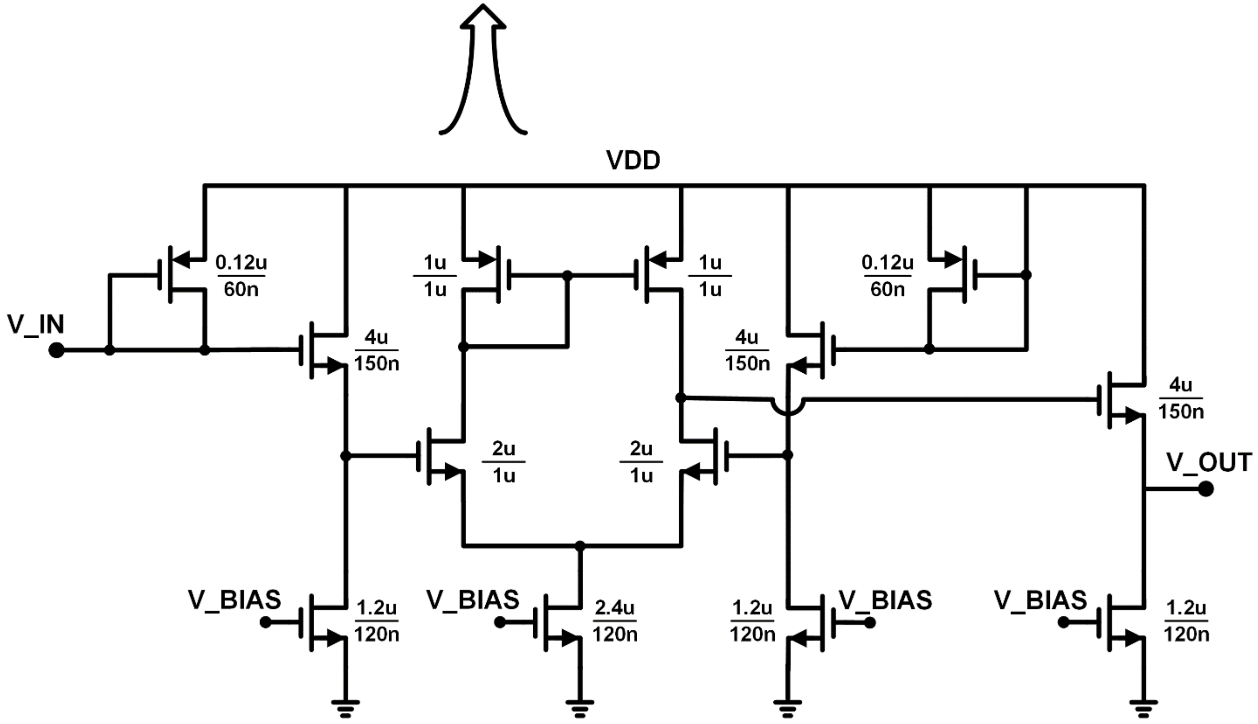
- RF+ and RF- are coming from two antennas facing each other
- Photodiode is used for biasing
- Responsivity ≈ 1kV/W, and NEP ≈ 32pW/√Hz



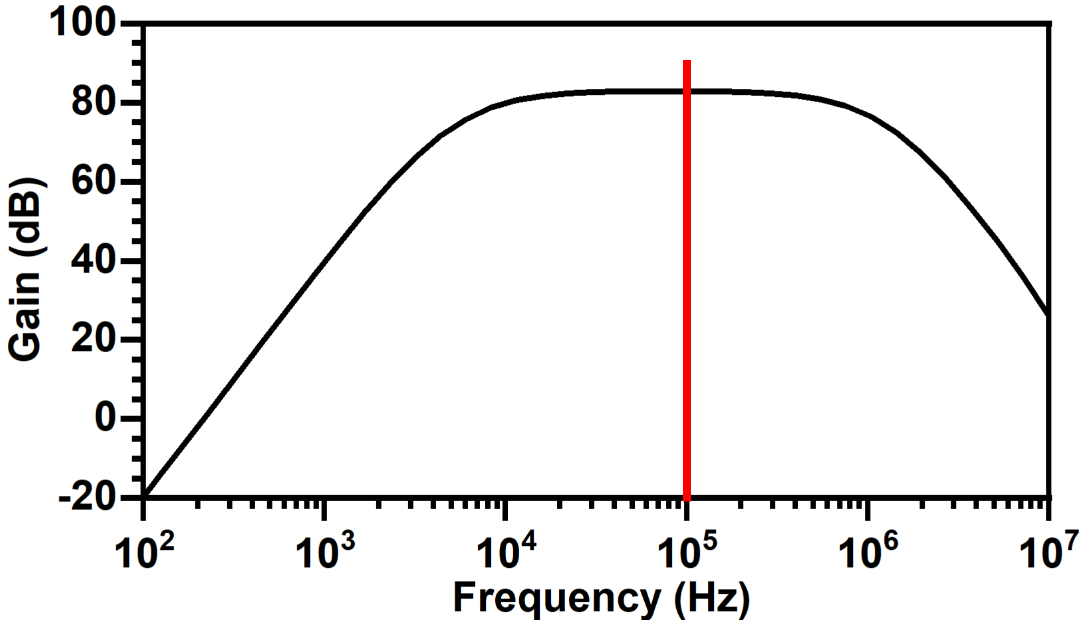
Simulated Detector Responsivity and NEP

Ultra-Low Power Amplifier Chain



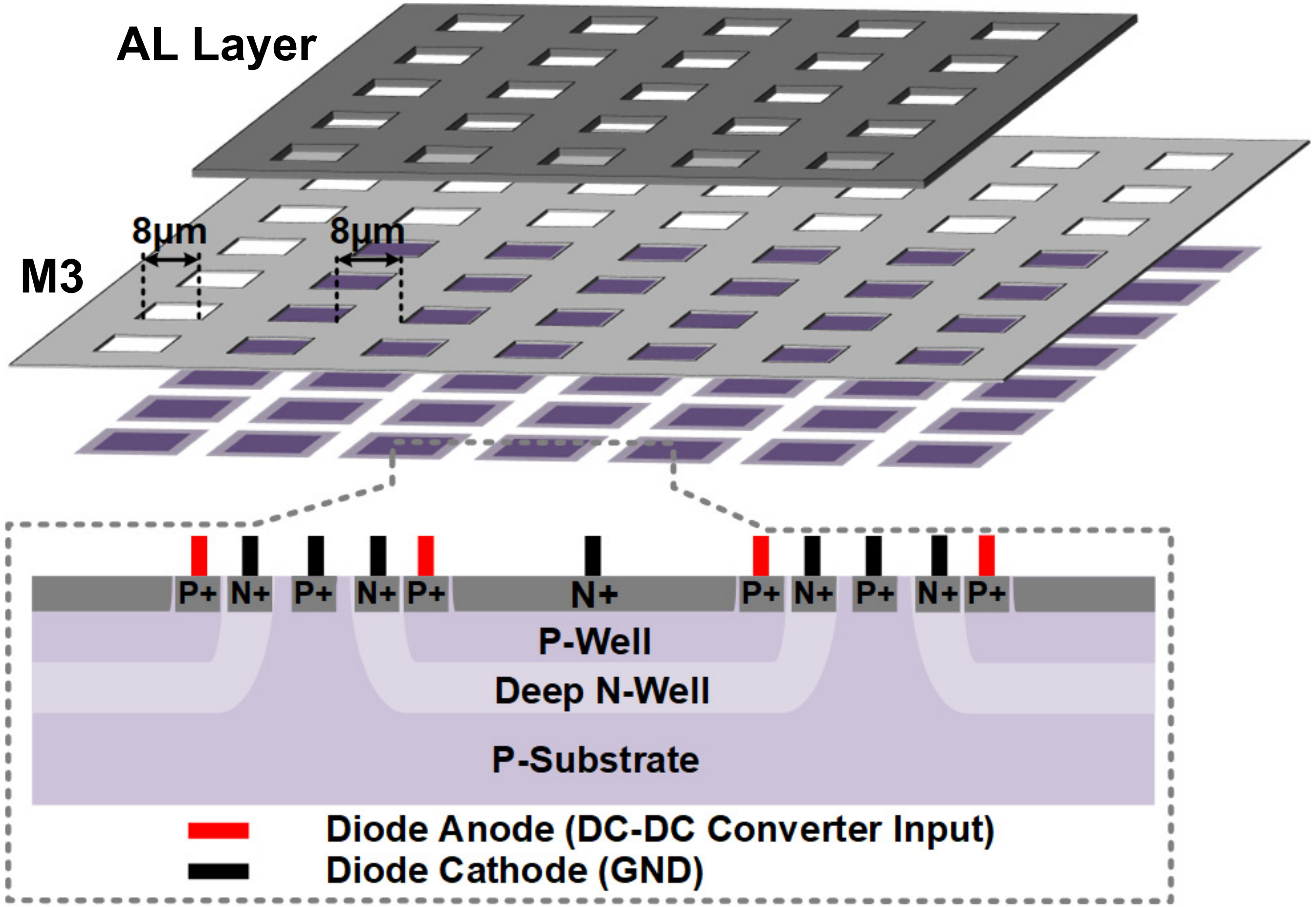


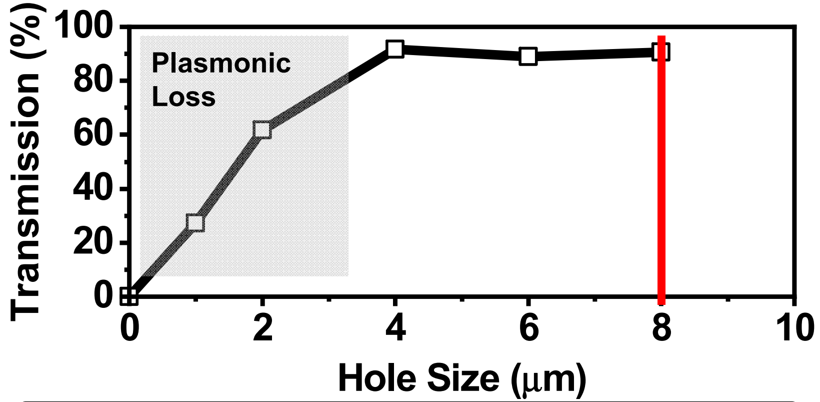
- **Subthreshold low power design**
  - Simulated gain of 80dB
  - Simulated DC power of 1.5μW
- **Downlink data rate is 100kb/s**



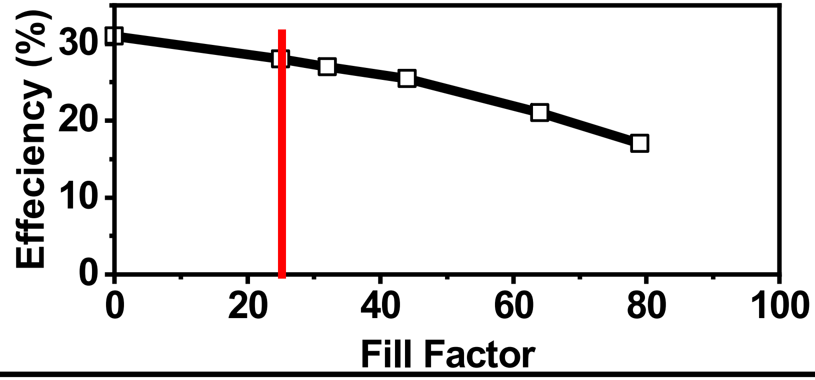
Simulated Amplifier Gain

Optical-Power Harvesting





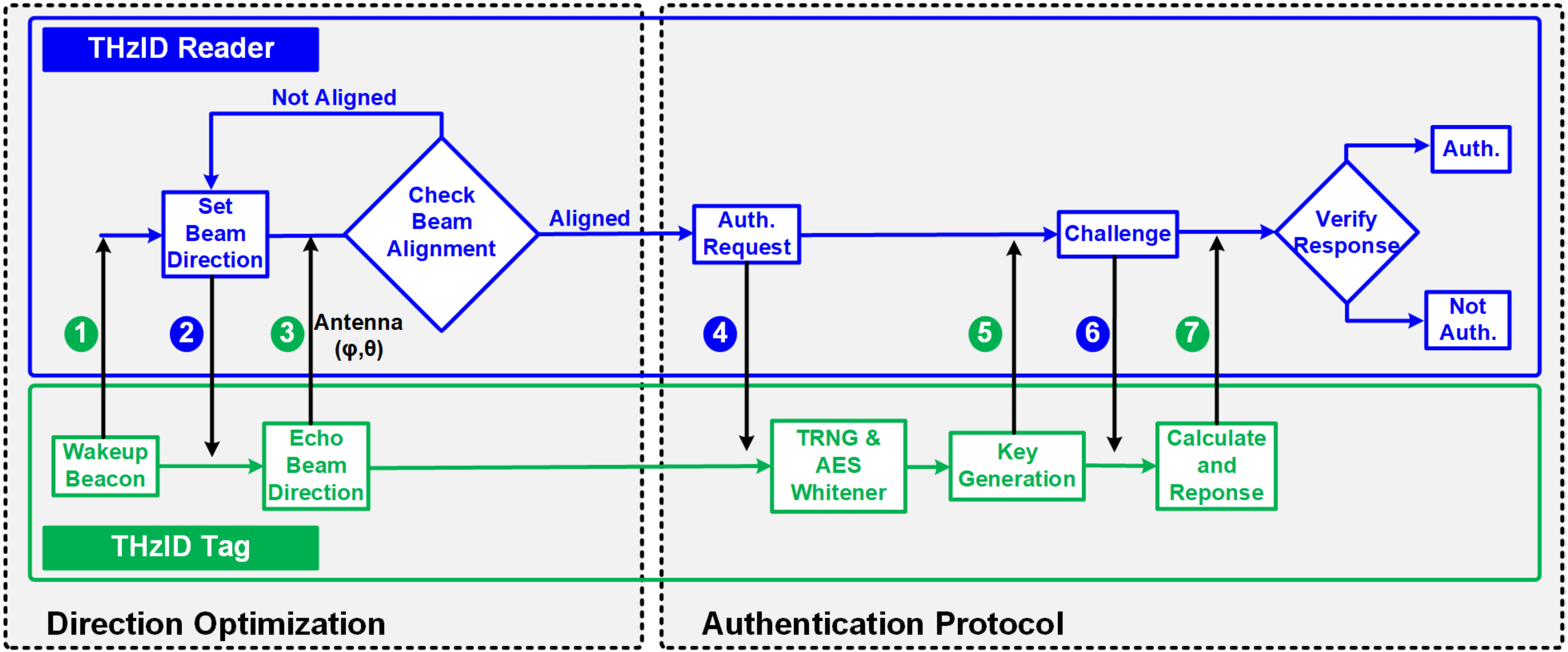
Light Transmission with Hole Size



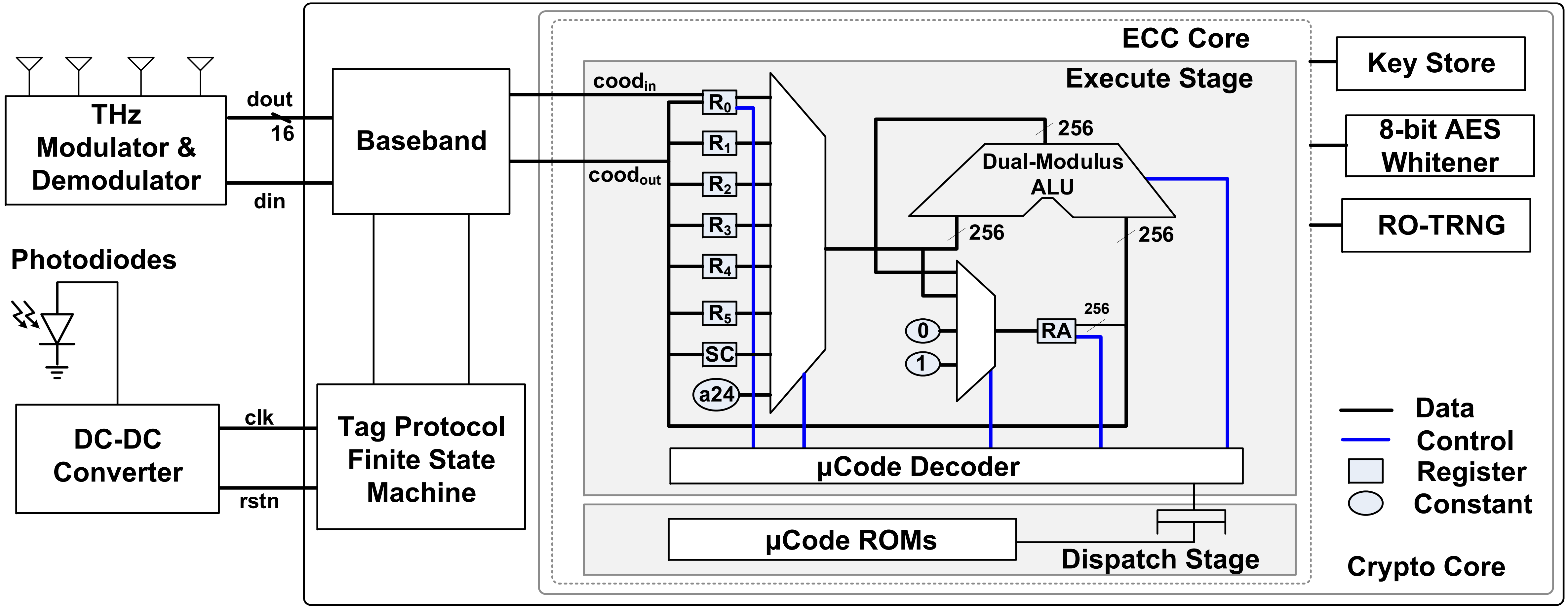
Antenna Efficiency with Fill Factor (8µm Hole Size)

- N+/P-well/Deep-N-well diode is used to create an isolated anode terminal
- The simulated light transmission through the antenna fishnet pattern is 22%

Communication Protocol



Cryptographic Processor



- **Elliptic curve cryptography (ECC) with 22% lower area and 18% lower cycle count compared to state-of-the-art**

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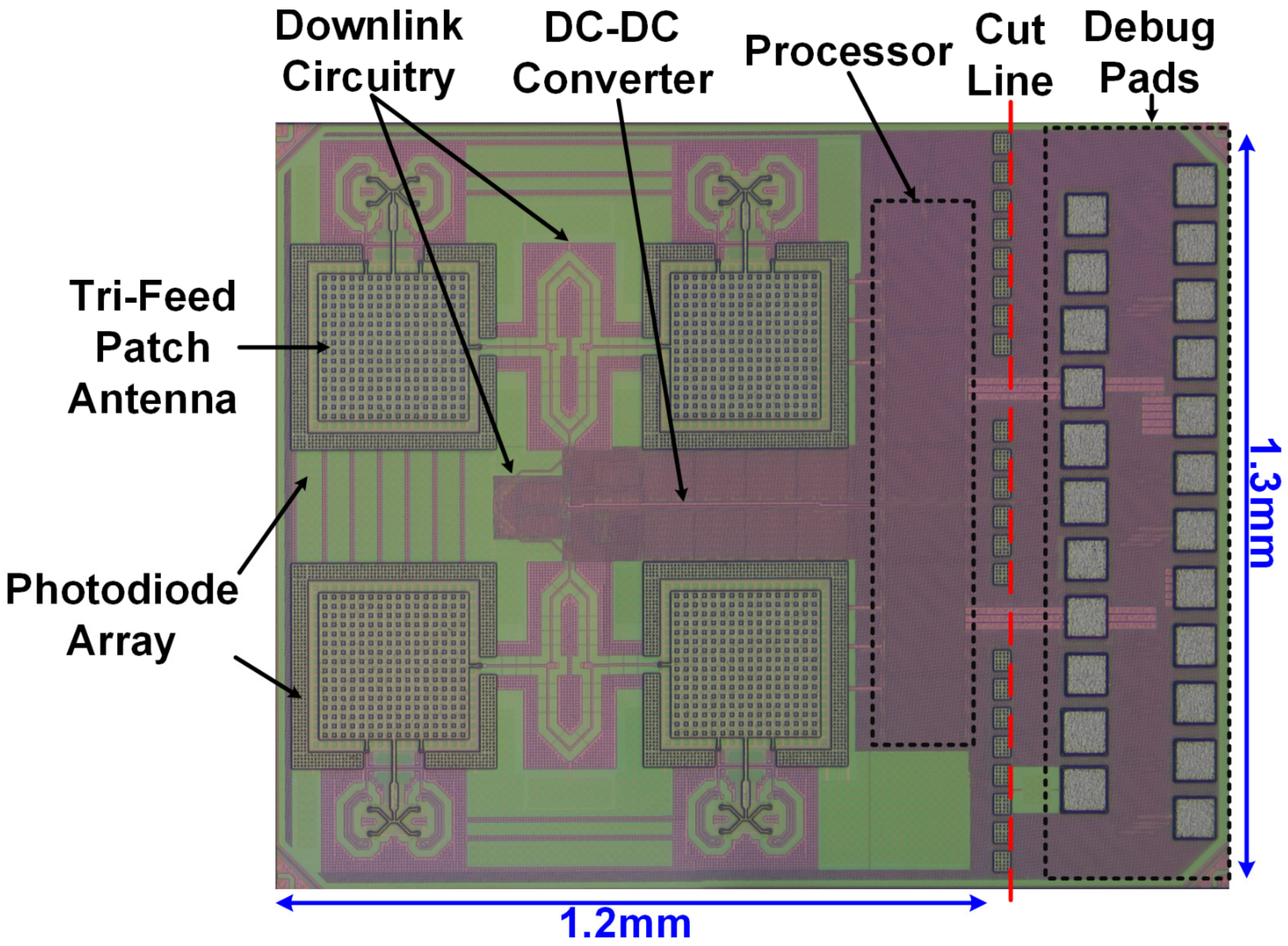
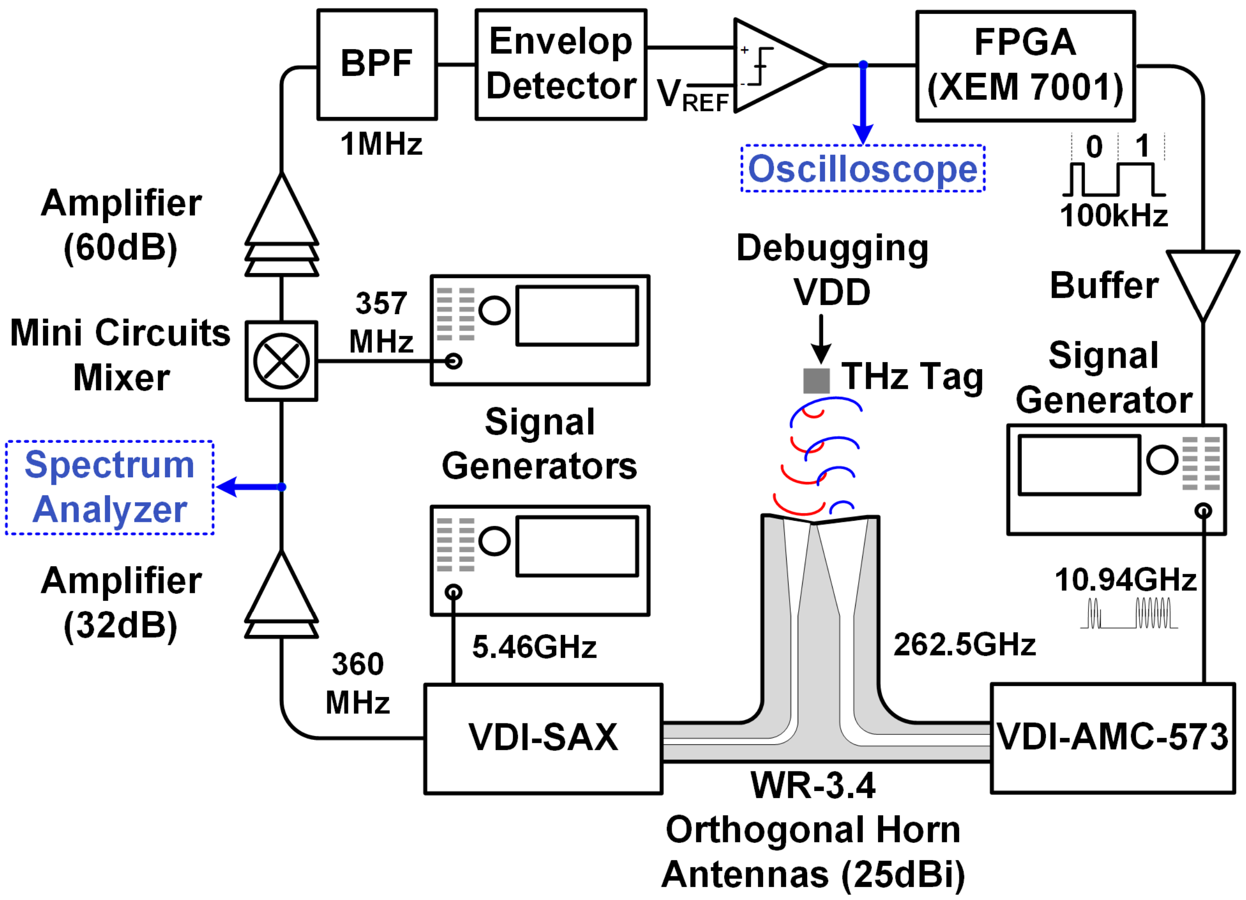
Chip Micrograph

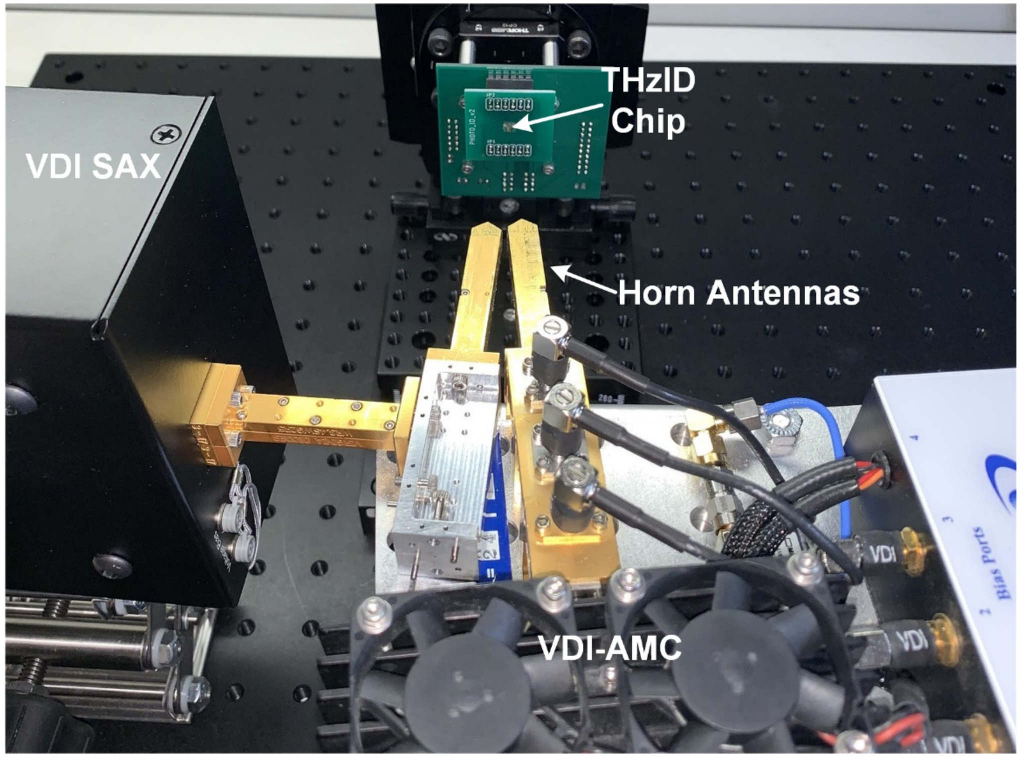
- **TSMC 65nm CMOS process**



Measurement Setup



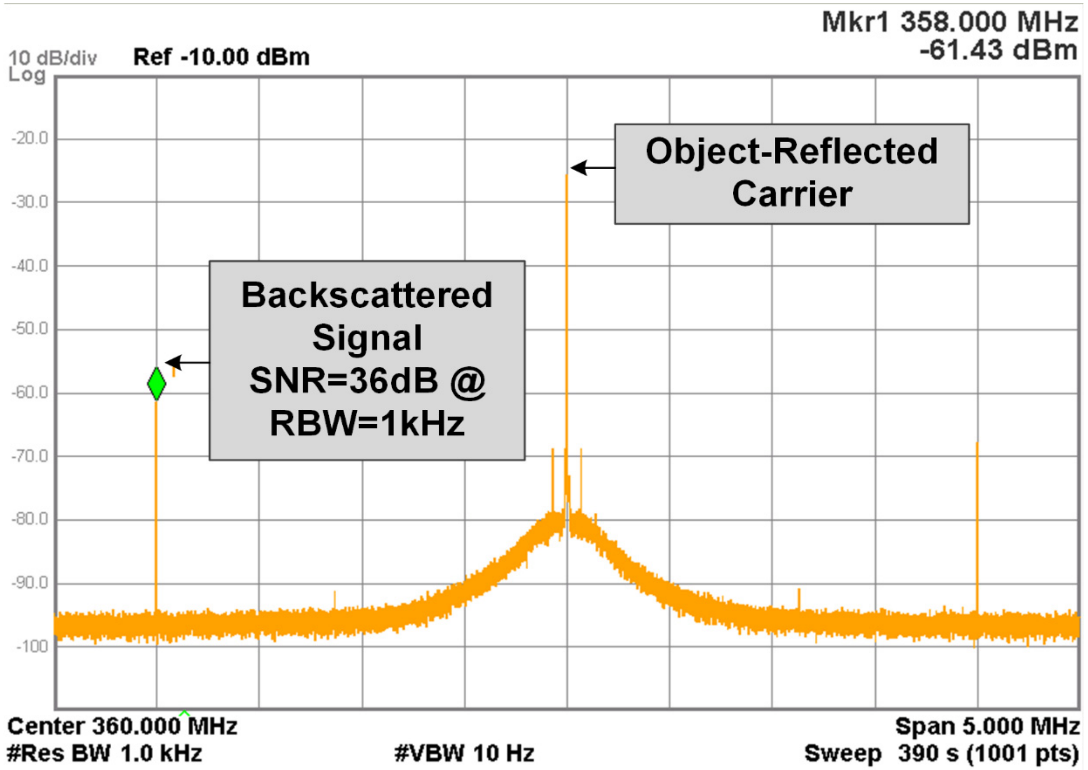
Measurement Setup Schematic



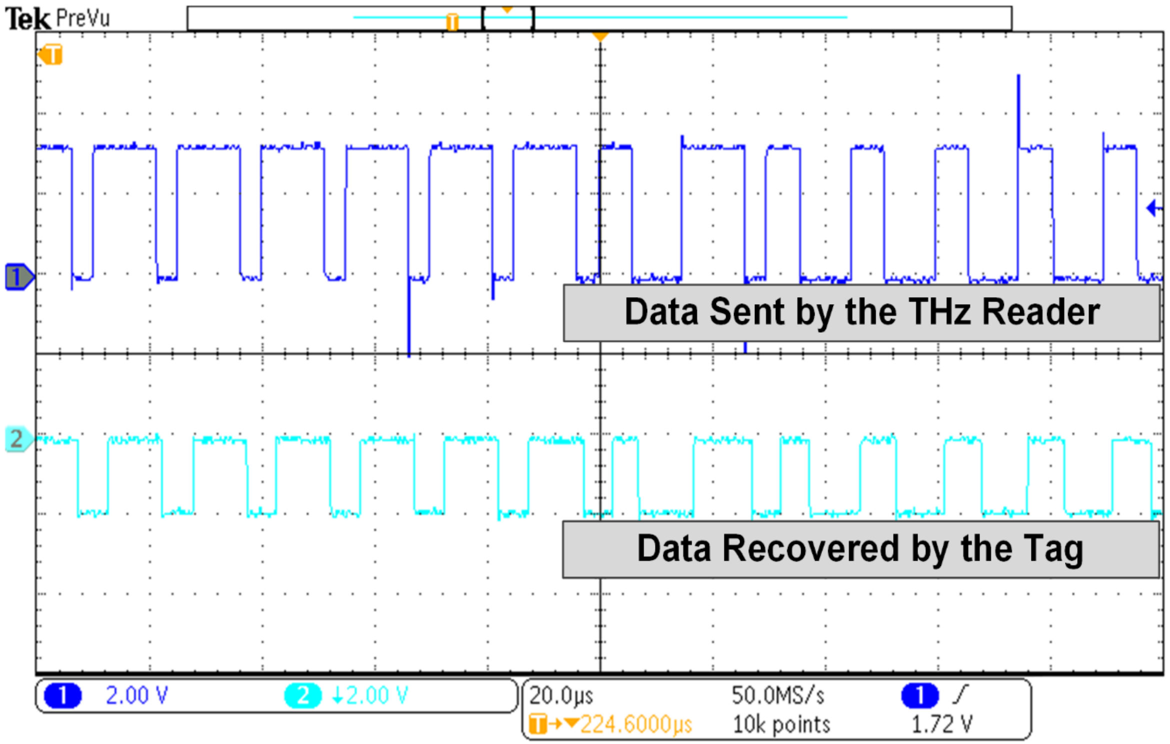
Chip Testing Setup Photograph

260GHz Front-End Performance

Measured Backscattered Spectrum

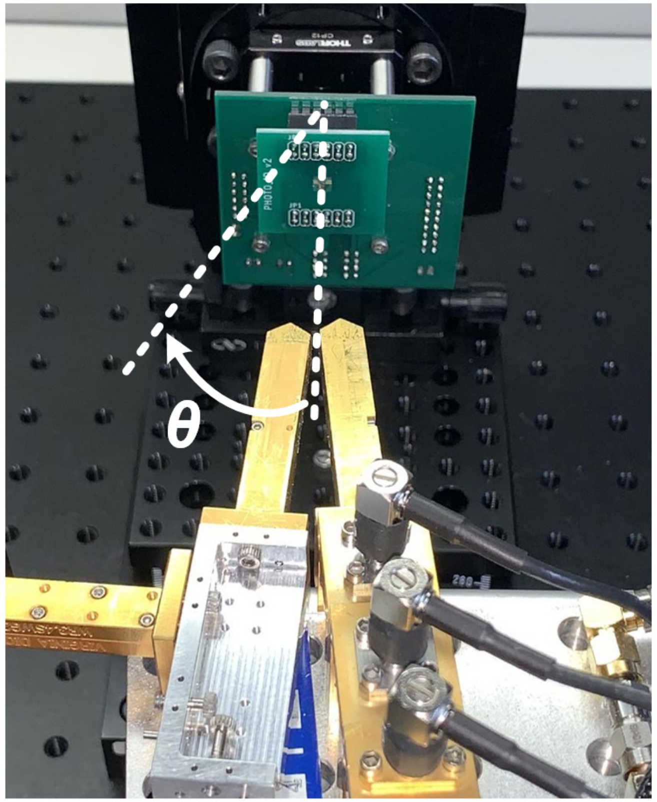


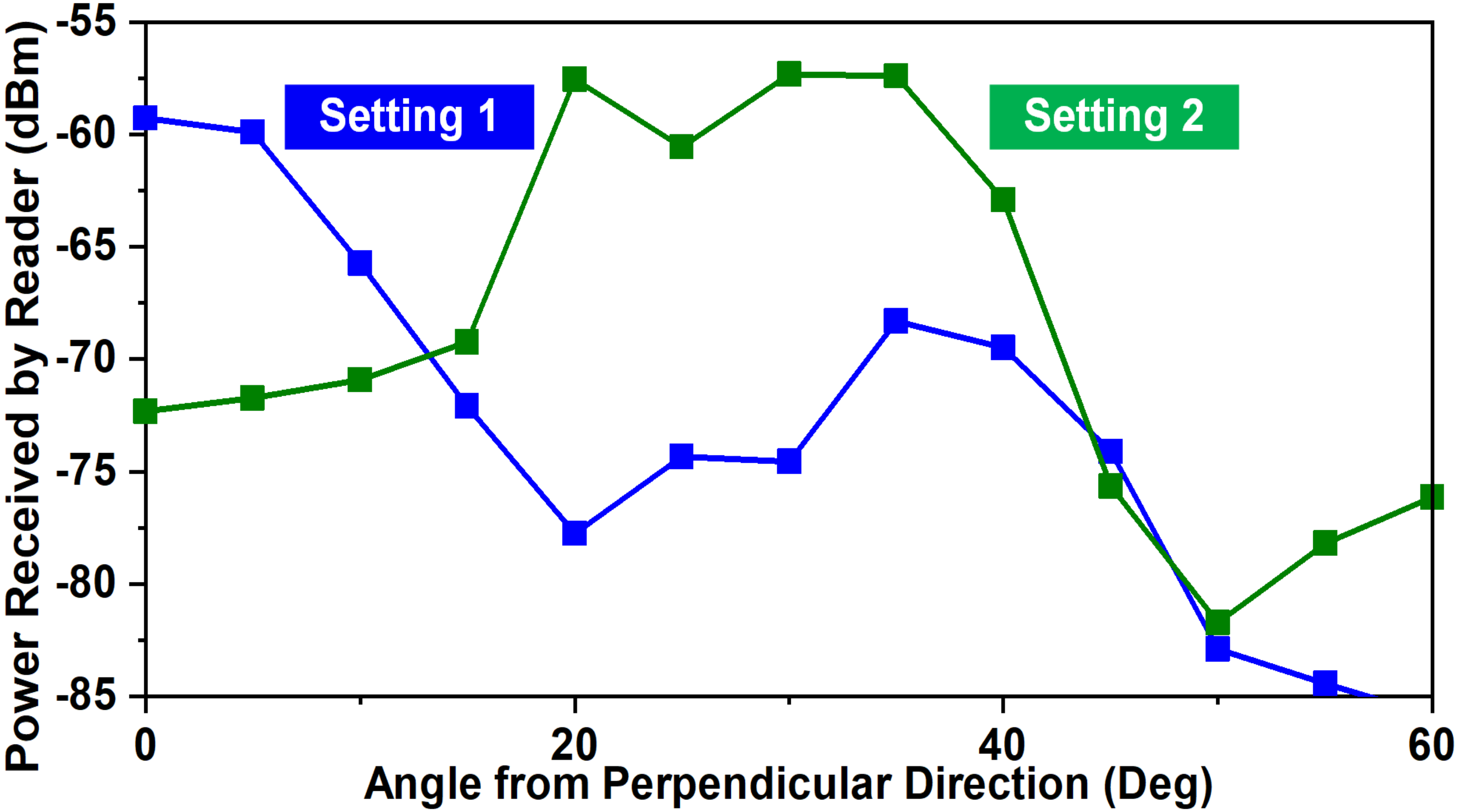
Measured Downlink Data



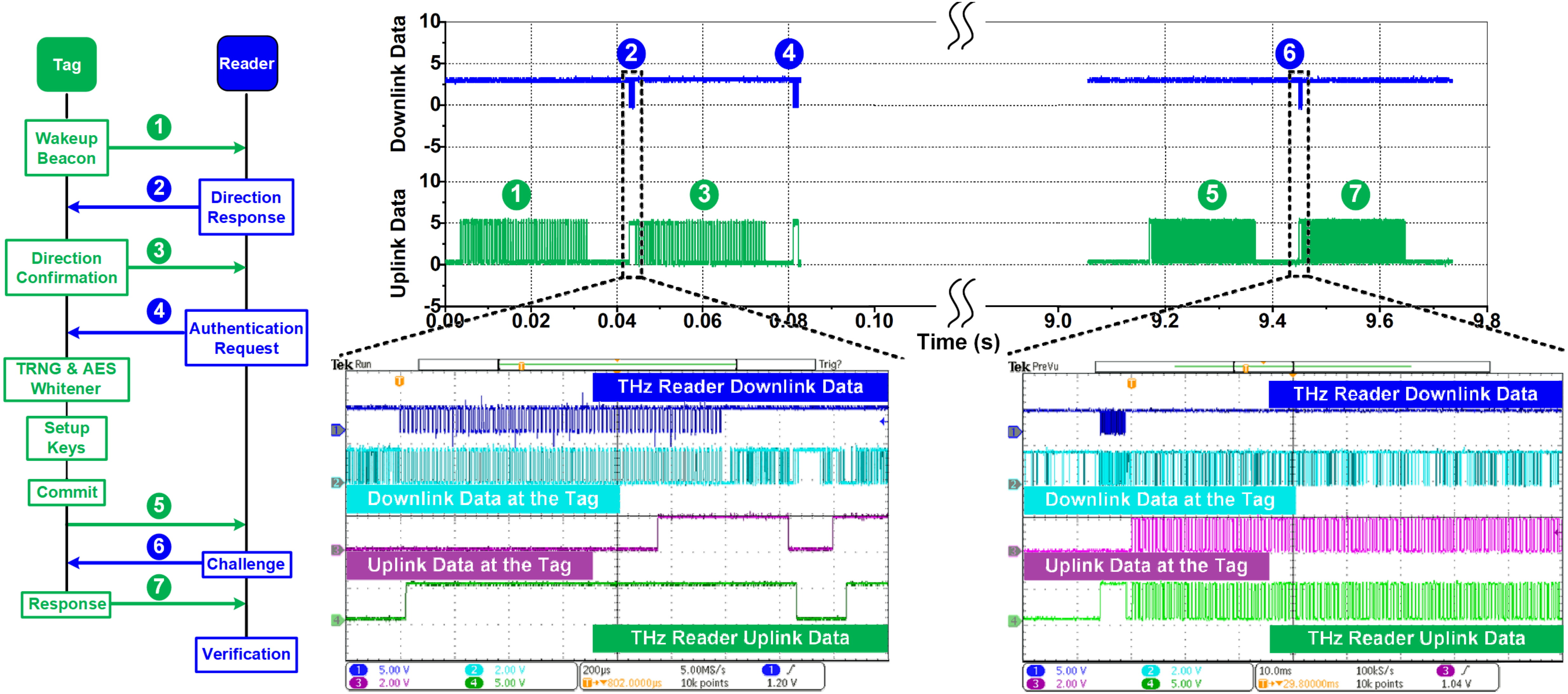
Beam-Steering Measurements

- **Backscattered signal detected by the reader at non-perpendicular positions by sweeping the angle (*θ*)**

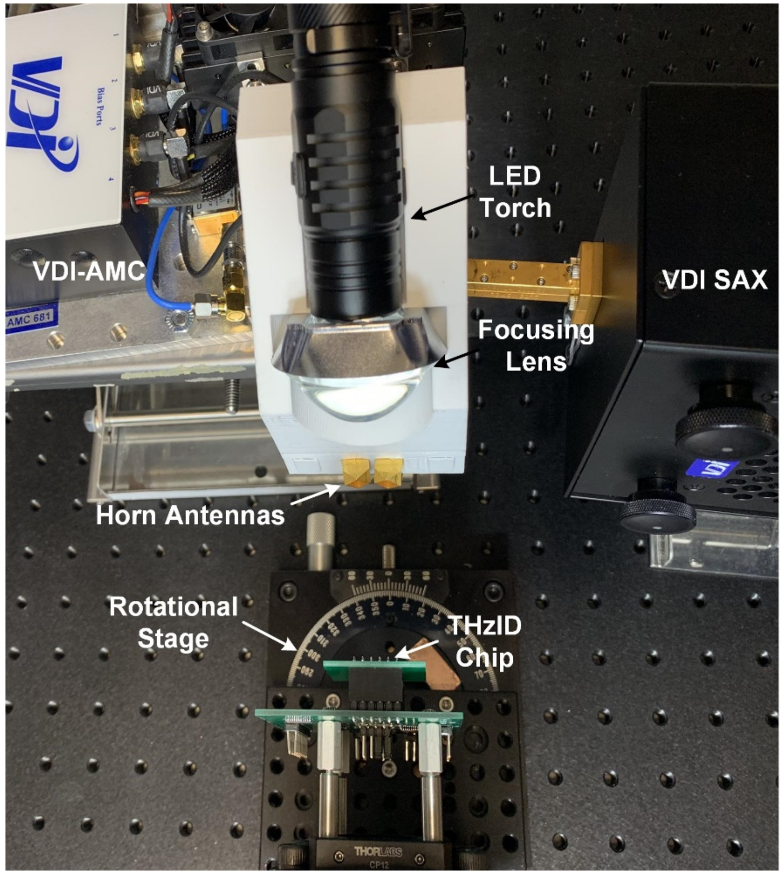




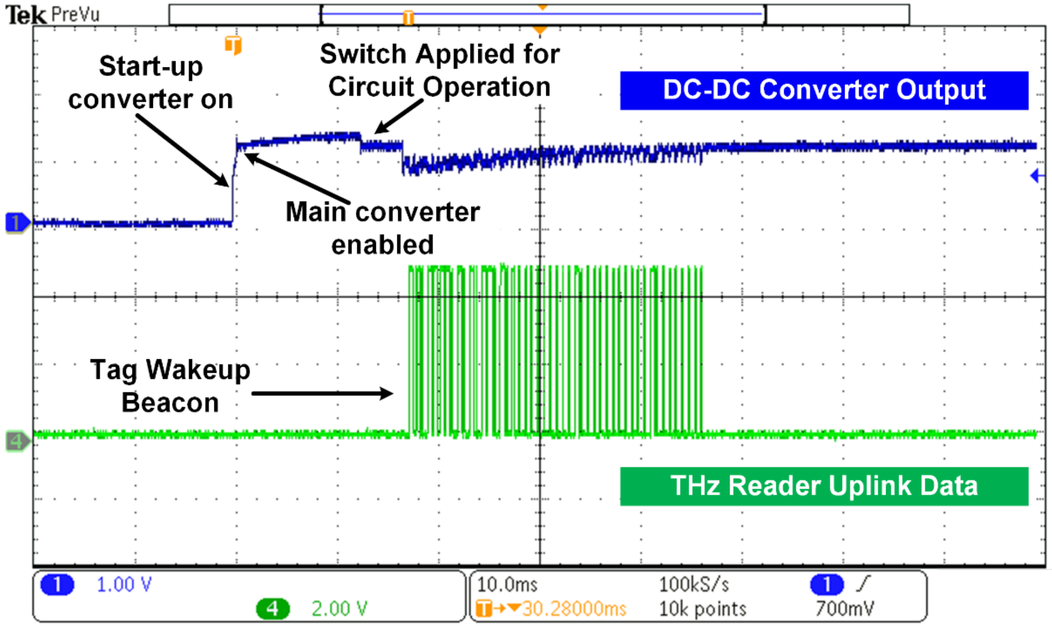
Measured Time Domain Communication



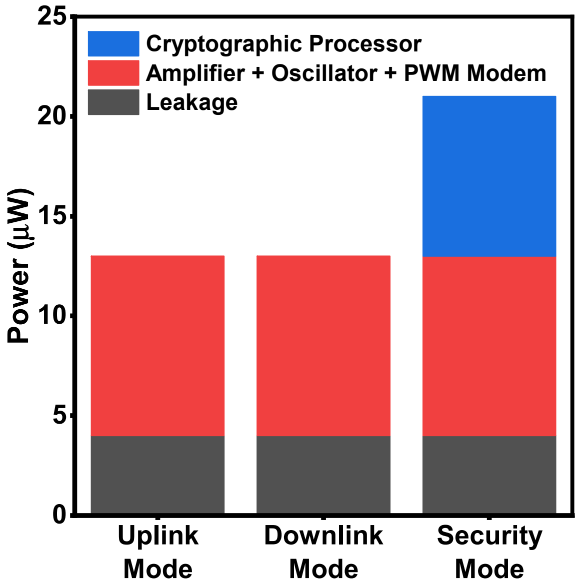
Light Powering Performance



Chip Testing Setup Photograph with LED Torch



Chip Start-up with Light Power



Power Budget Breakdown

Outline

Performance Comparison

References	Process	Carrier Frequency (GHz)	Data Rate	Peak Power	Security	Range	Beam-Steering	Area (mm^2)
This Work	65nm	260	DL:100kbps UL:2kbps	21μW	Yes (Elliptic Curve)	5cm	Yes	1.6
ISSCC'17 [1]	180nm	0.915	DL:62.5kbps UL:30.3kbps	2mW	No	20m	No	9*
ISSCC'18 [2]	65nm	5.8	DL:5Mbps UL:4kbps	10μW		1mm		0.01
VLSI'14 [3]	65nm	DL:24 UL:60	DL:6.5Mbps UL:1.2Mbps	11mW**		50cm		4.4
ISSCC'16 [4]	130nm	0.433	125kbps	16μW	Yes (Symmetric)	5mm		64***

* Volume is $27mm^3$
** Calculated data according to [1]
*** The area includes off-chip antenna (chip area is $0.8x0.8mm^2$)

[1] L. Chuo, et al., *ISSCC*, 2017.
[2] B. Zhao, et al., *ISSCC*, 2018.
[3] M. Tabesh, et al., *VLSI*, 2014.
[4] C. S. Juvekar, et al., *ISSCC*, 2016.

Acknowledgement

- National Science Foundation (SpecEES ECCS-1824360)
- Virginia Diodes Inc. (VDI) for providing testing instruments
- Prof. Donhee Ham and Dr. Houk Jang at Harvard University for their support during the testing
- Prof. Nicholas Fang and Xinhao Li at MIT for their support during the testing

Paper 29.9

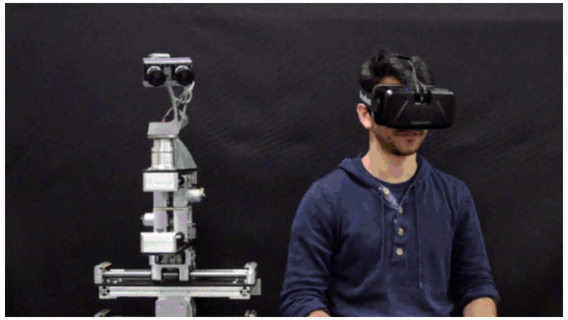
4 x 4 Distributed Multi-Layer Oscillator Network for Harmonic Injection and THz Beamforming with +14dBm EIRP at 416GHz in a Lensless 65nm CMOS IC

Hooman Saeidi, Suresh Venkatesh, Chandrakanth Reddy Chappidi, Tushar Sharma, Chengjie Zhu, Kaushik Sengupta

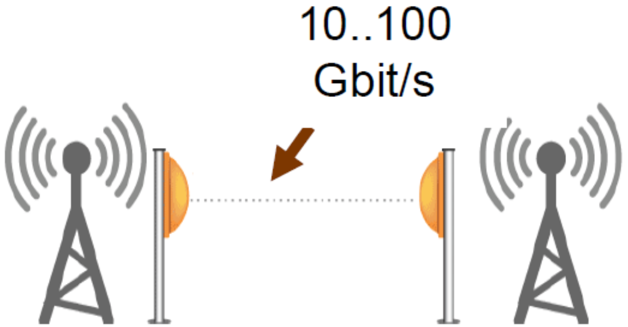
Princeton University, Electrical Engineering, Princeton, NJ

THz Applications

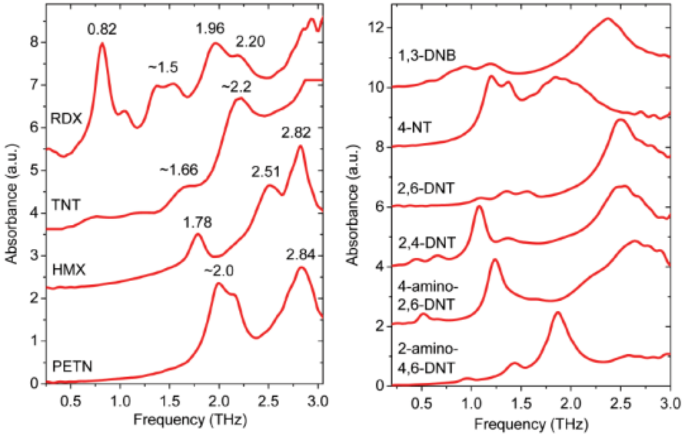
High-resolution Sensing



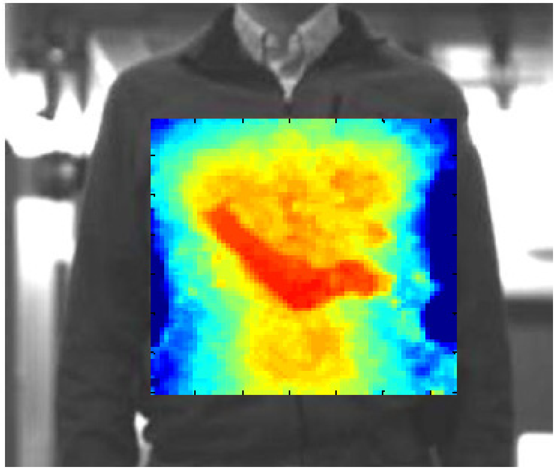
Robotics and AR/VR



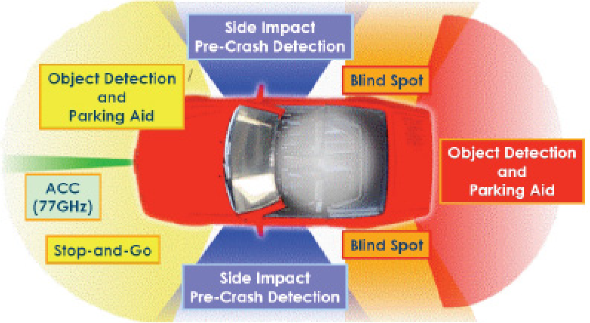
Fronthaul/Backhaul



Spectroscopy



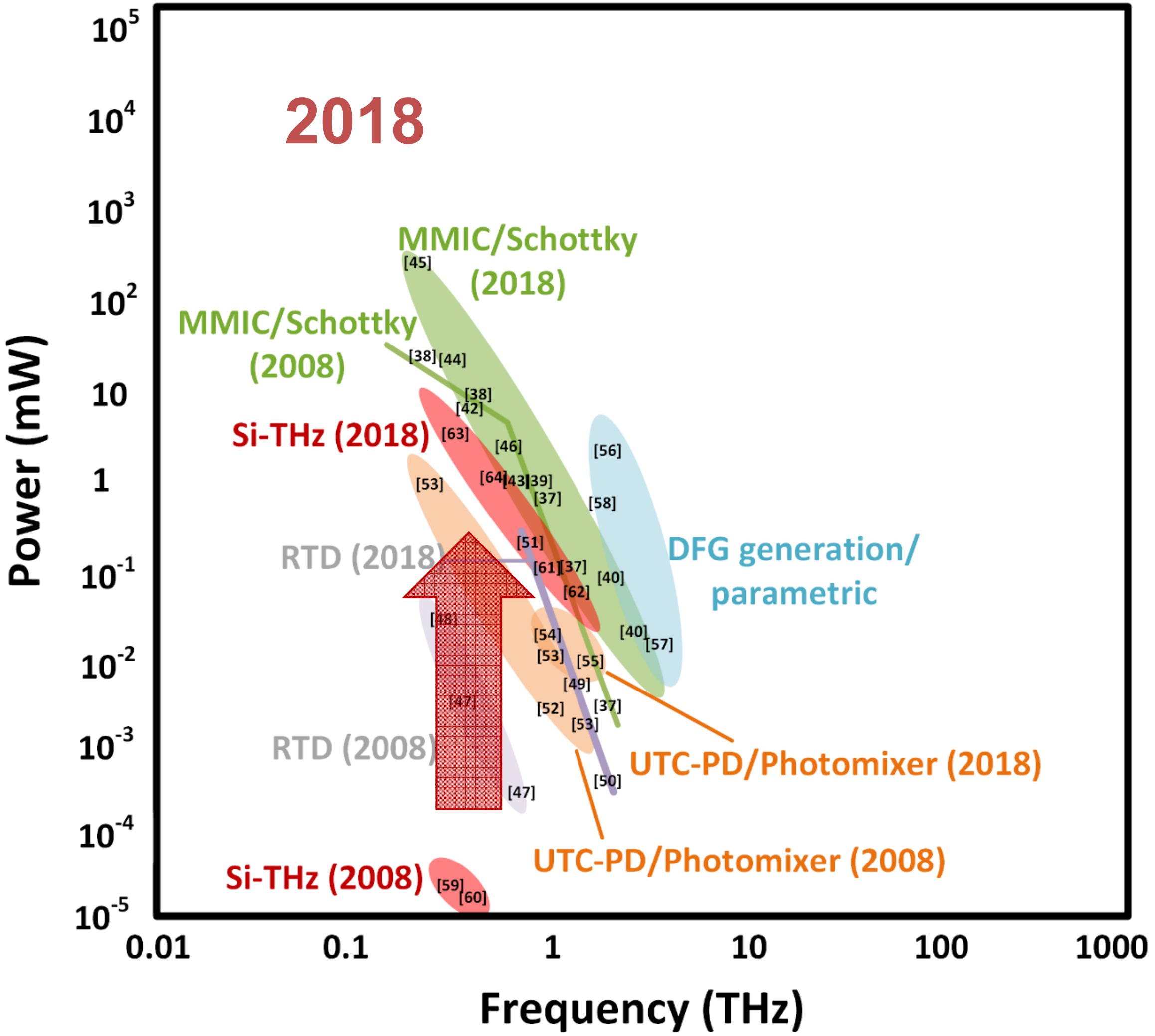
Imaging



Automotive Vision

- ❑ Communication (backhaul), Sensing, Imaging and Spectroscopy

THz Sources

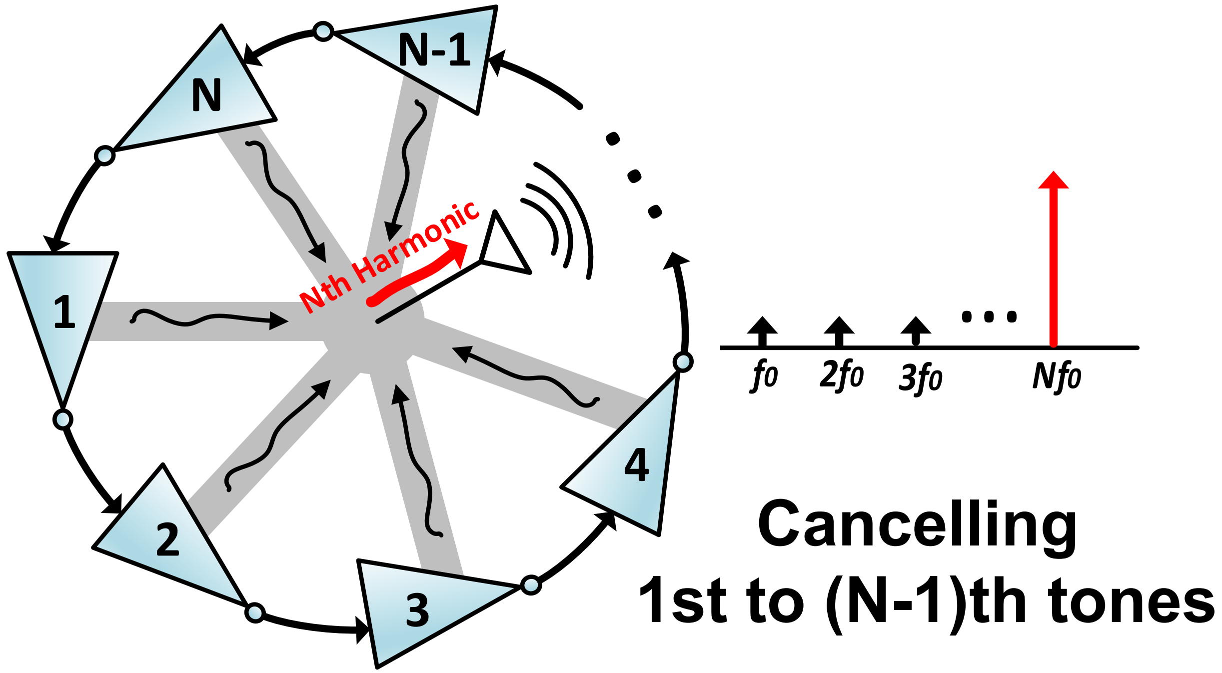


- Tremendous improvement of power generation in silicon at THz in the past decade.
- High efficient, high power generation needed in chip-scale THz systems where cost, size, scalability and room temperature operation are critical.

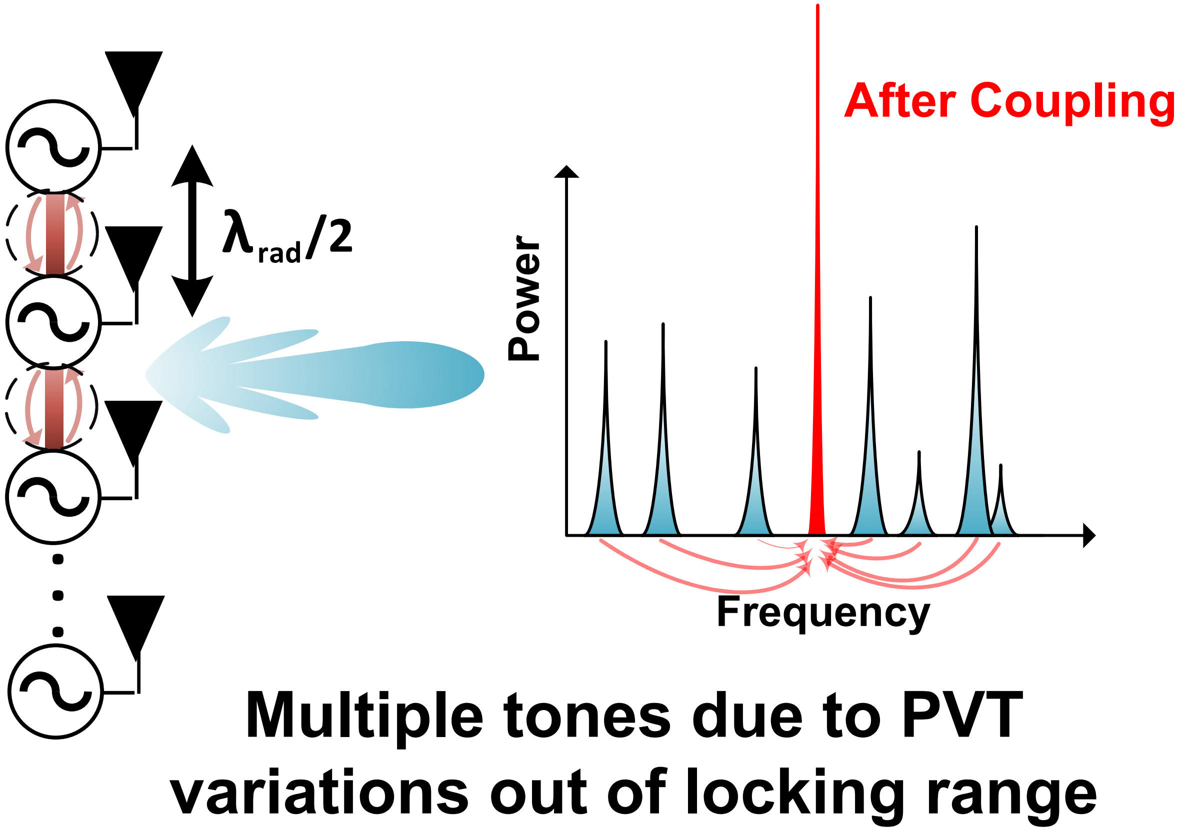
K.Sengupta, T.Nagatsuma and D.Mittleman, ***Nature Electronics, Dec. 2018.***

THz Power Generation

- Due to the limited Device f_{max}, harmonic oscillators used to reach frequencies above f_{max}.

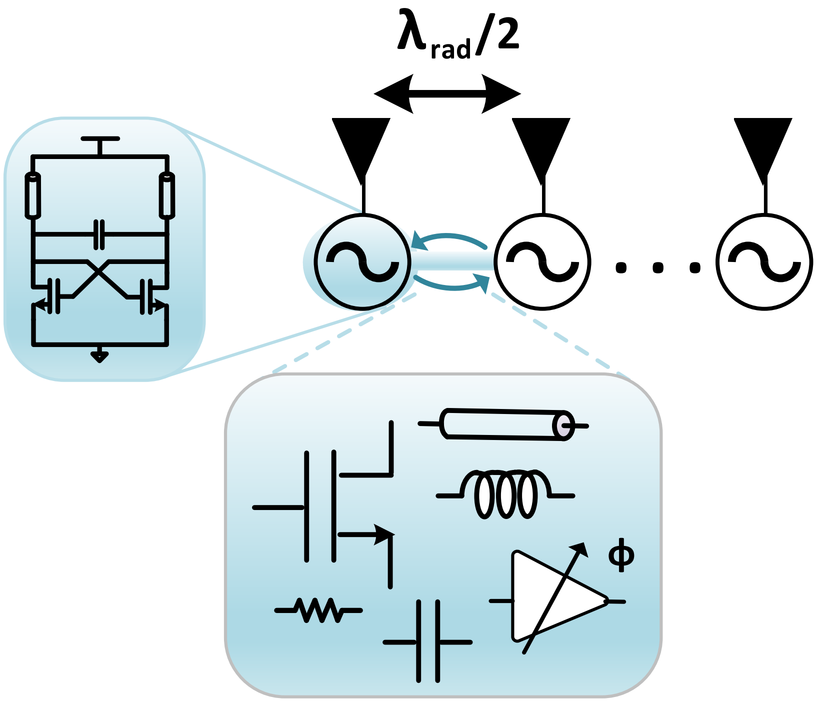


- Multiple coupled sources to boost up the radiated power.



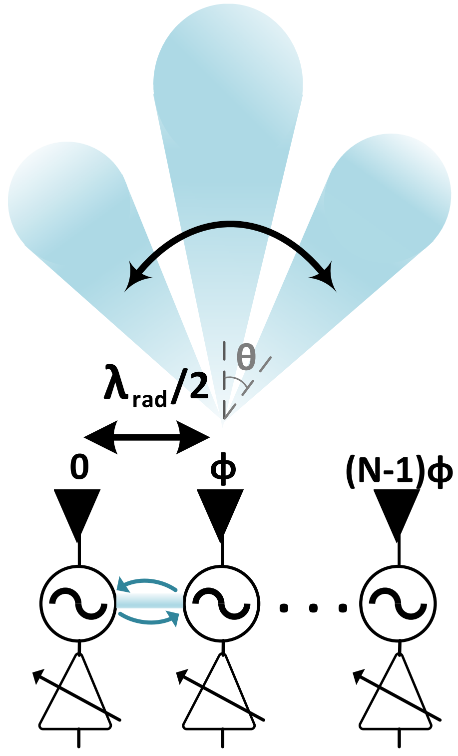
Challenges in THz Sources

1. Locking the spaced sources



Active/ Passive Coupling

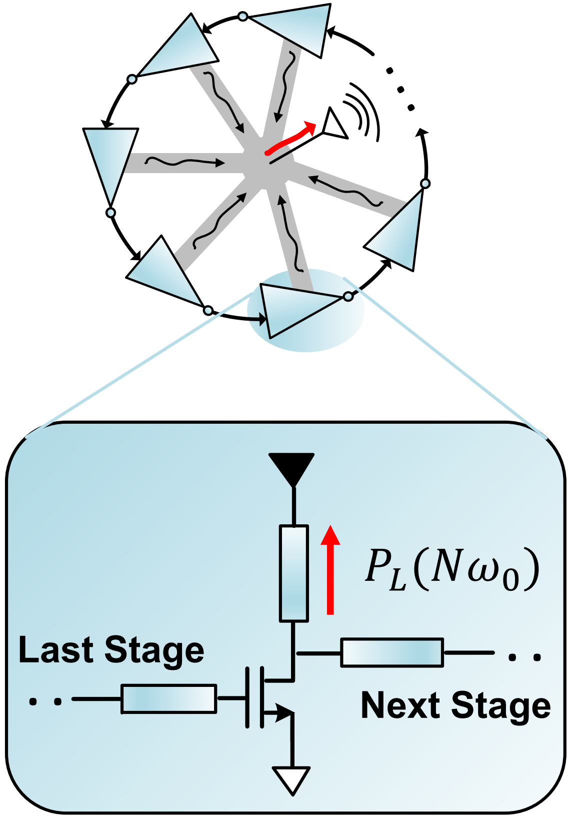
2. Phase difference for beamforming



Phase shifting

$(\beta d \sin\theta = \varphi)$

3. Optimum loading for High power generation



Optimum loading

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- **Large scale and Robust 2D Frequency Reference Network**

- **Multi-layer THz Power Generation and Beamforming Capability**

- **Measurement Results**

- **Conclusion**

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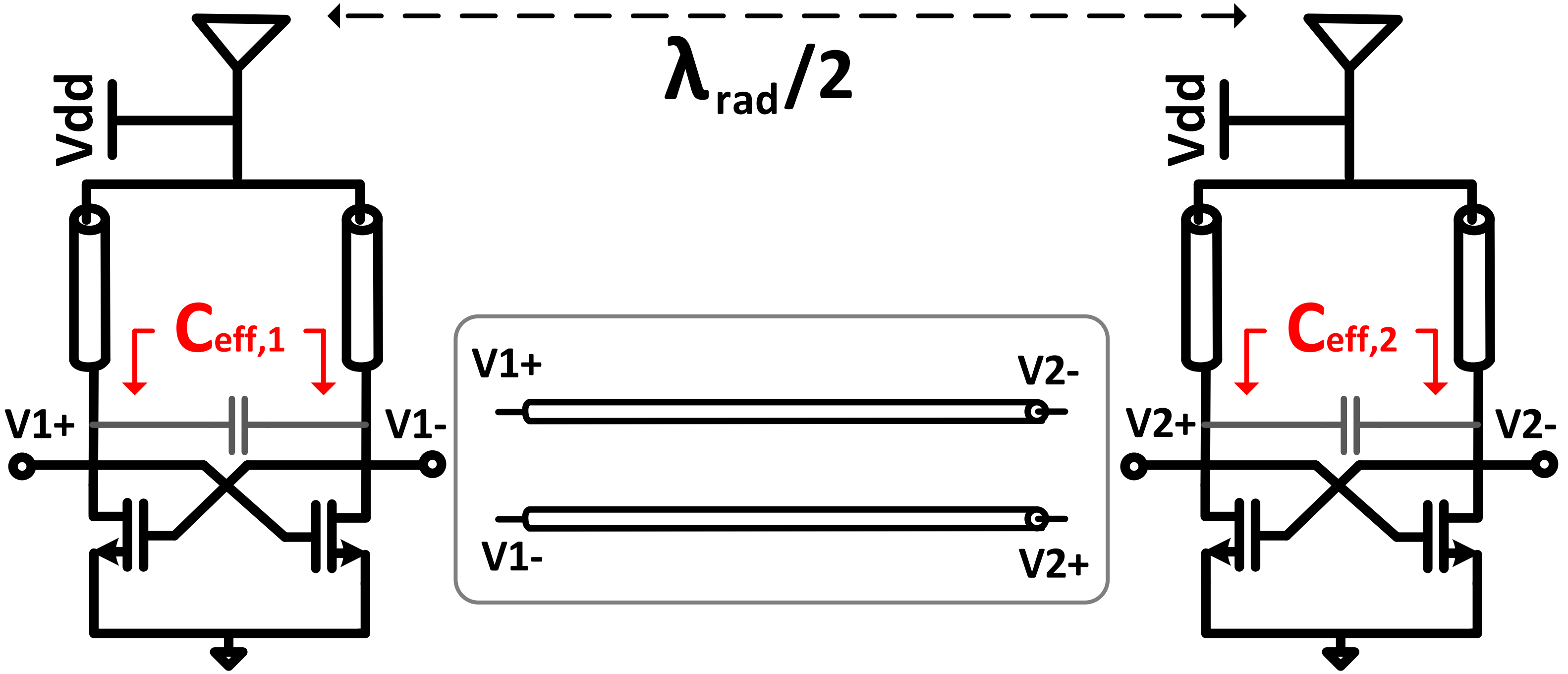
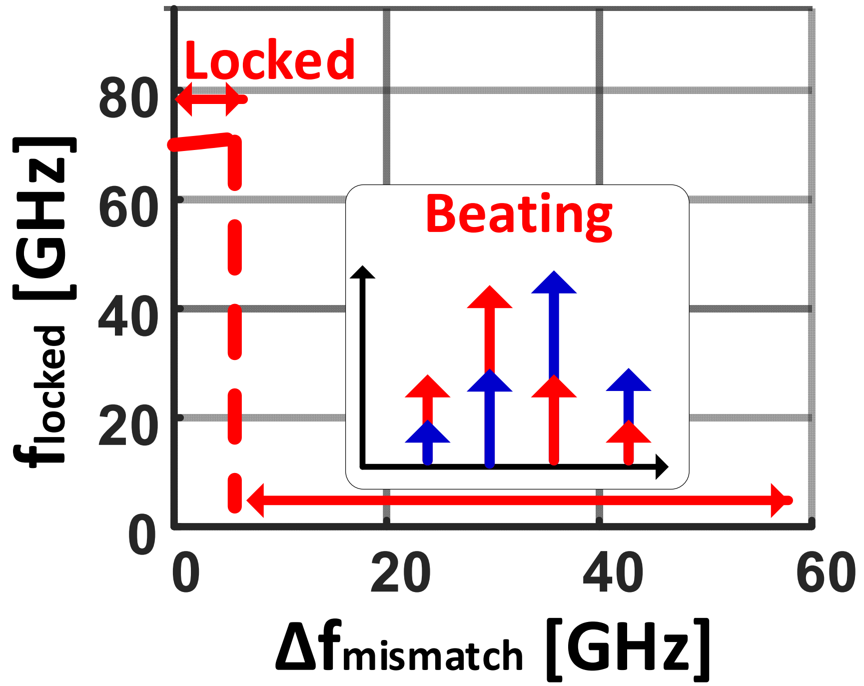
Tline-Coupled Oscillators

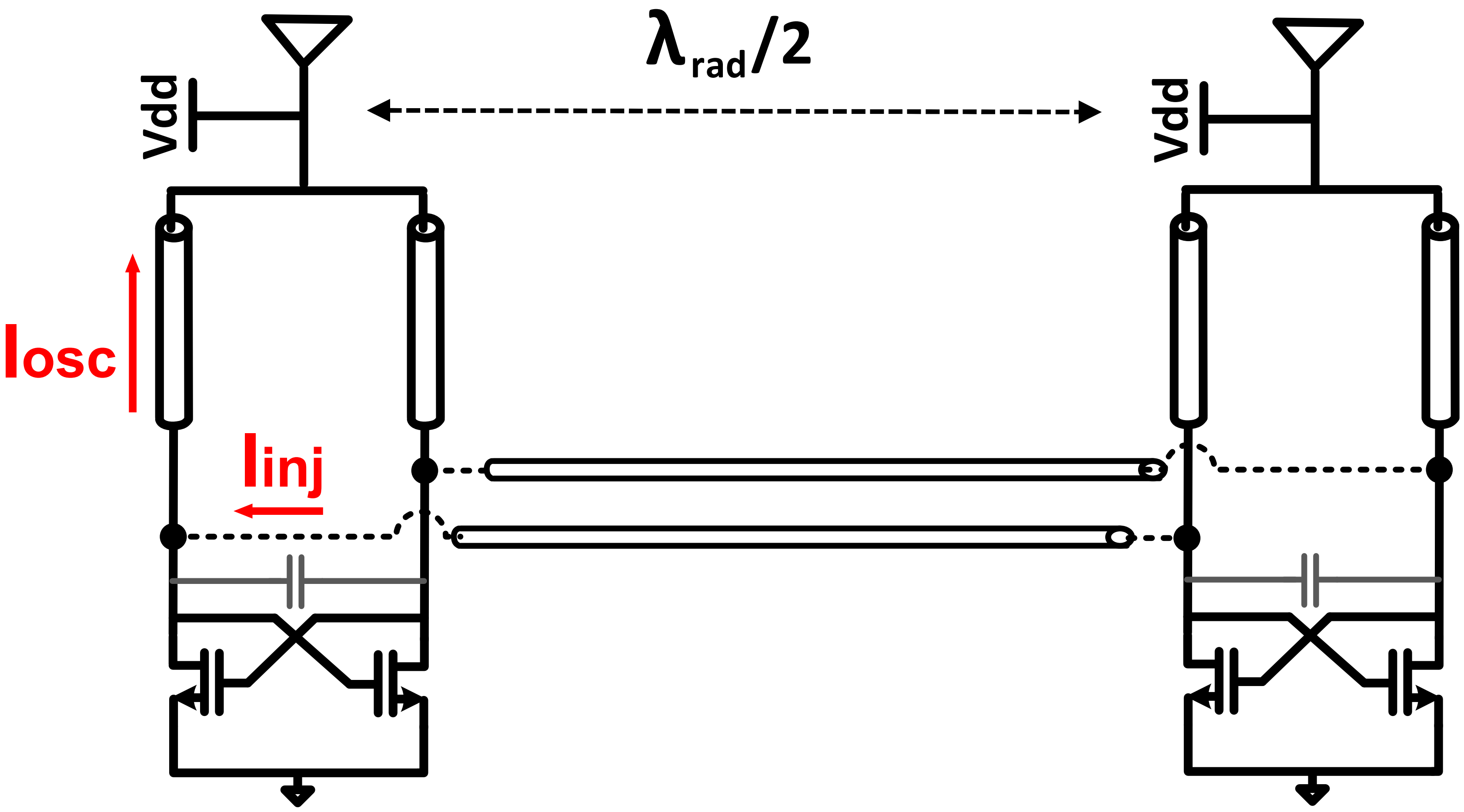




$$\Delta f_{mismatch} = \frac{1}{\sqrt{LC_{eff,1}}}\downarrow - \frac{1}{\sqrt{LC_{eff,2}}}\uparrow$$

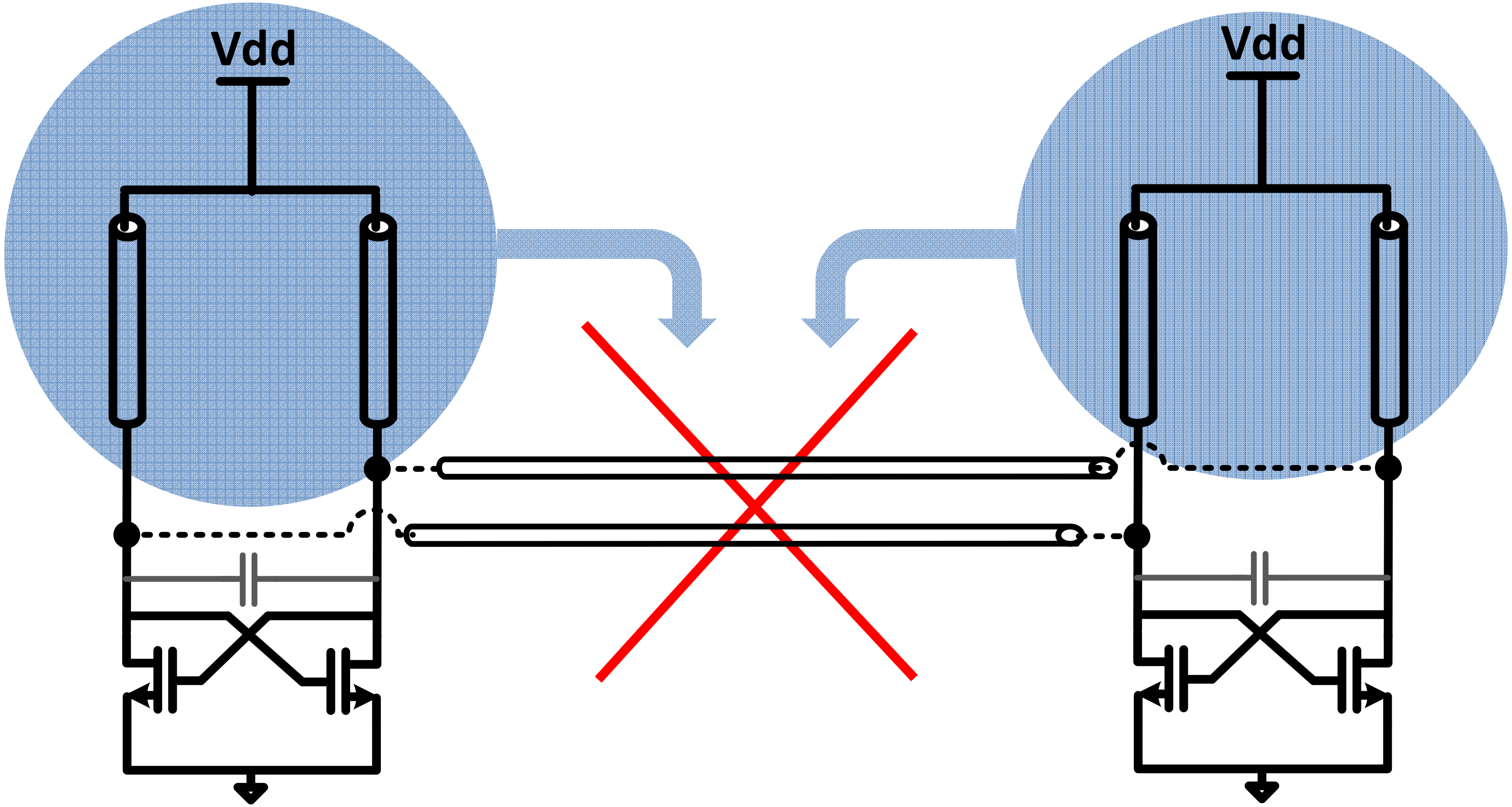
- Tline-based coupled oscillator sources.
- Even small mismatches can force them out of the locking range.

Tline-Coupled Oscillators



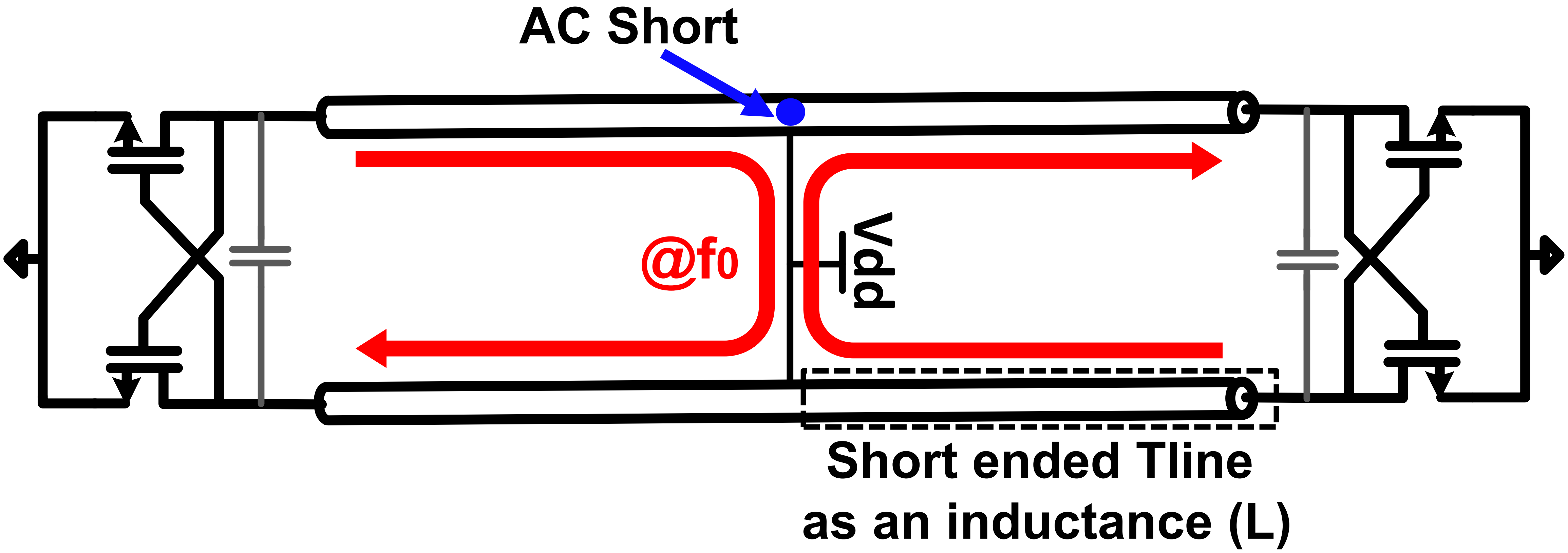
- Under small injection, based on Adler's equation : $\frac{\Delta\omega}{\omega} \propto \frac{I_{Inj}}{I_{osc}}$

Coupling Network = Resonator Network



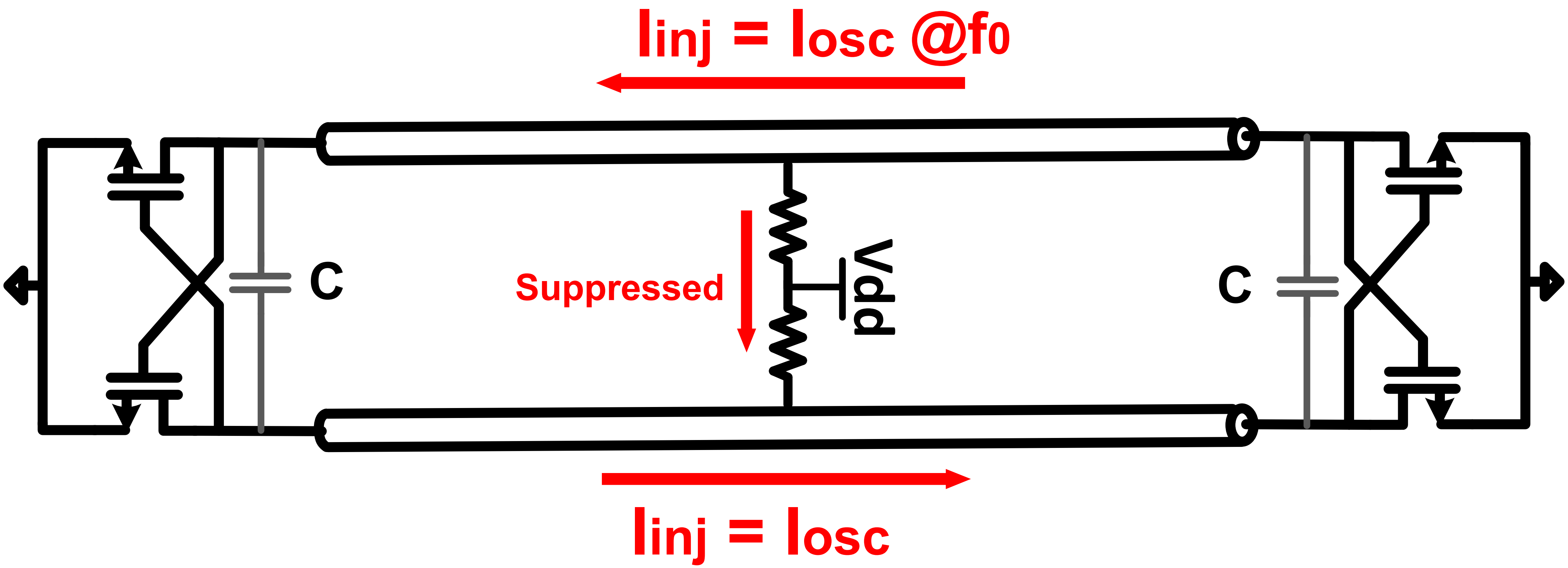
- Removing the coupling network and replacing the coupling network with the resonator network.

Uncoupled System



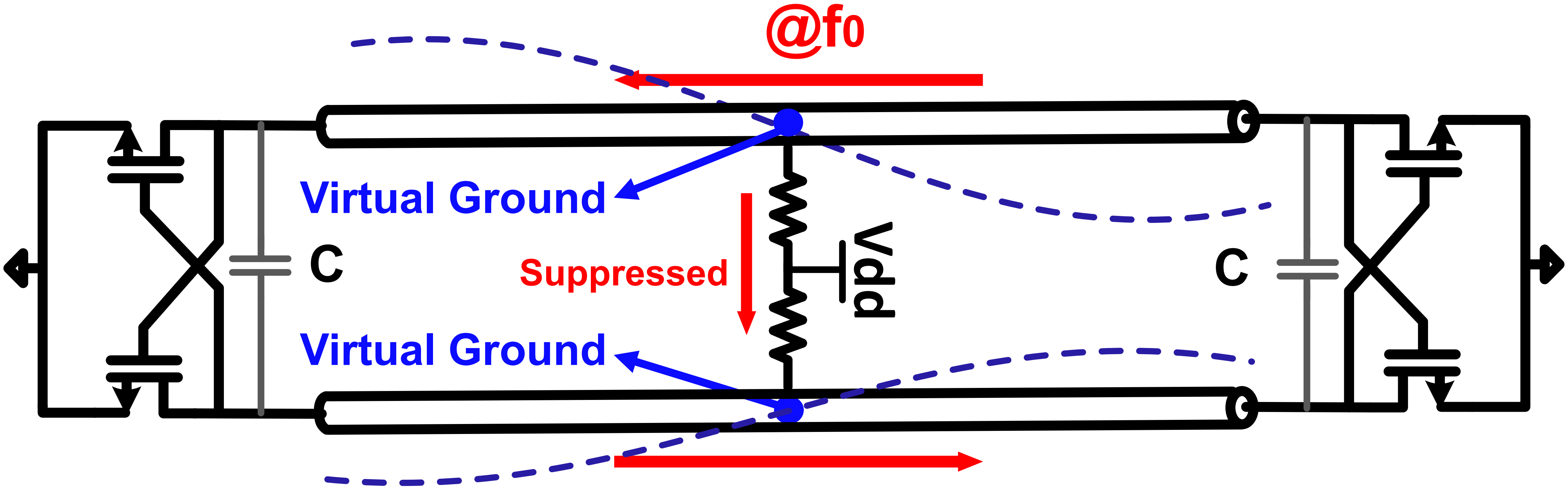
- This results in two uncoupled oscillator.

Dual Core Distributed Oscillator



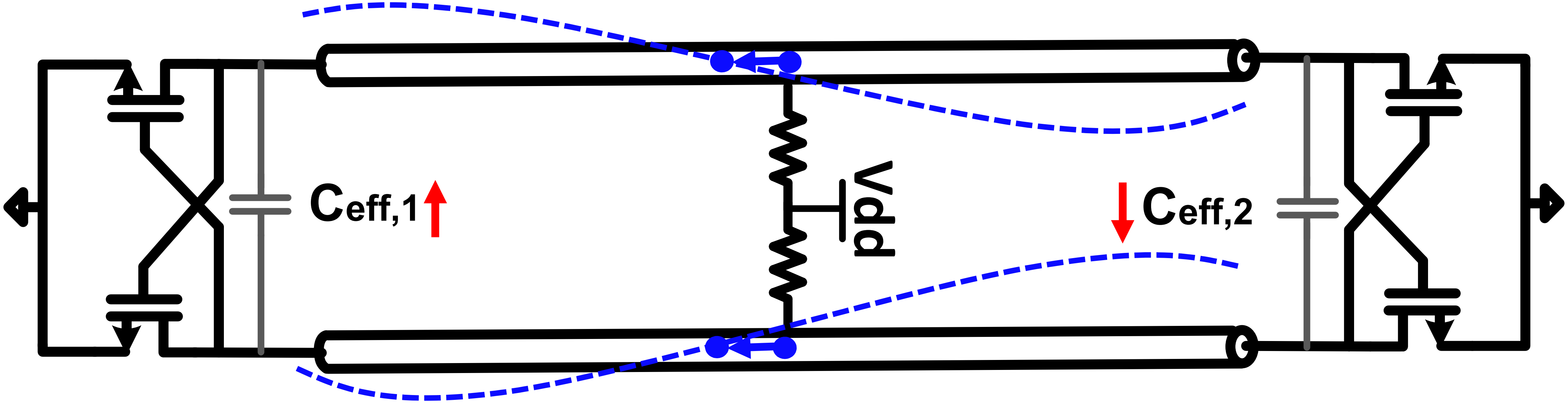
- The resistor suppresses any common mode oscillation
- Transparent to the fundamental oscillation.

Dual Core Distributed Oscillator



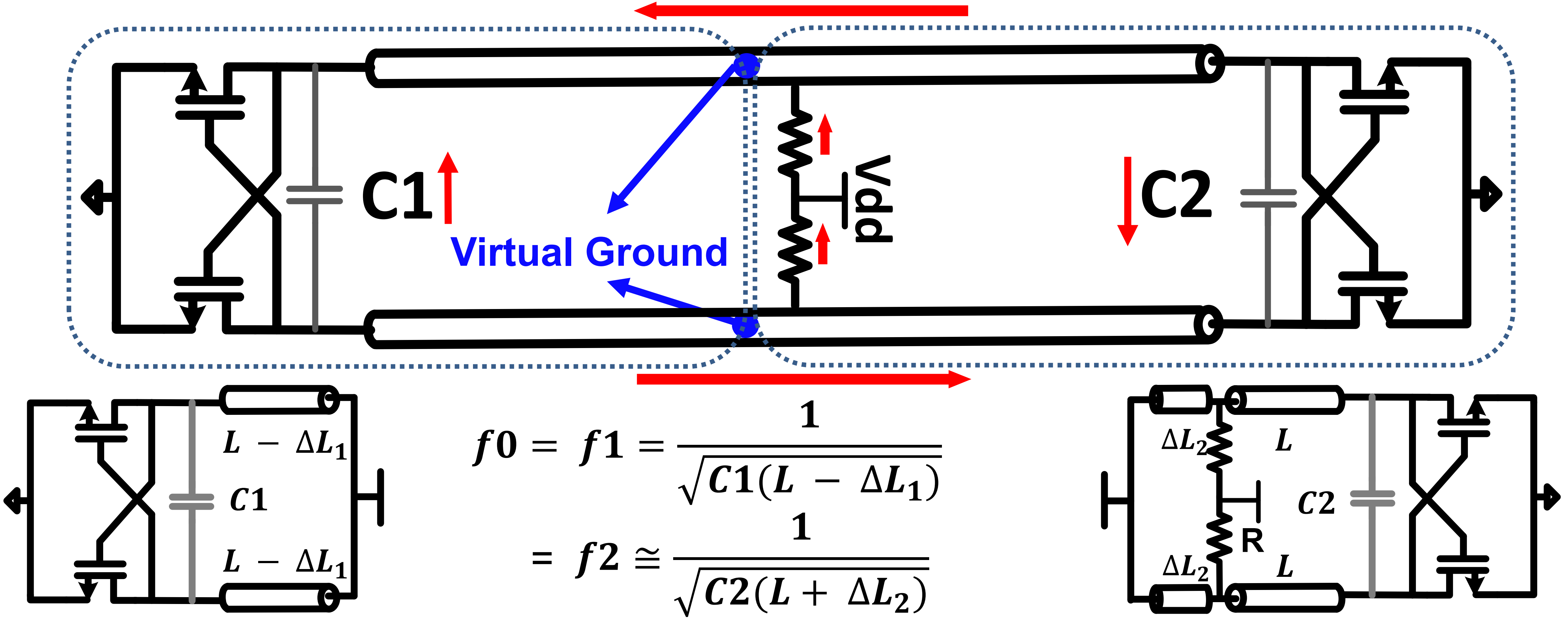
- The midpoint will be seen as a virtual ground.
- That structure will behave as a ***single oscillator*** with two separated – Gm Cells.

Mismatches in the Dual-Core Oscillator



- Virtual ground will move to adjust the effect of mismatch between 2 cells.

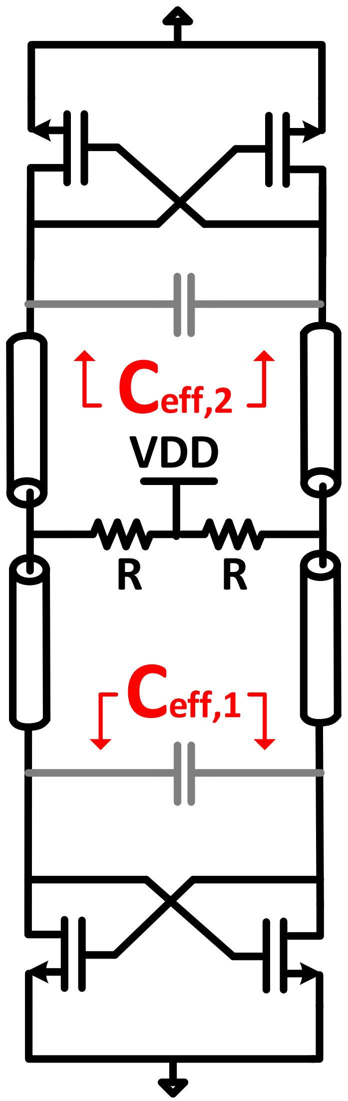
Mismatches in the Dual-Core Oscillator

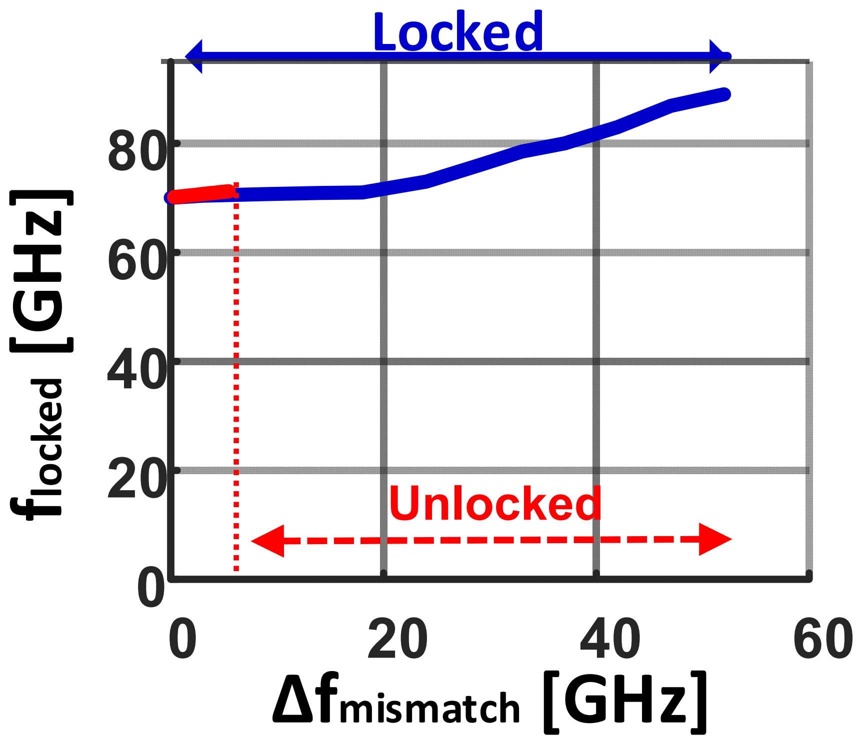


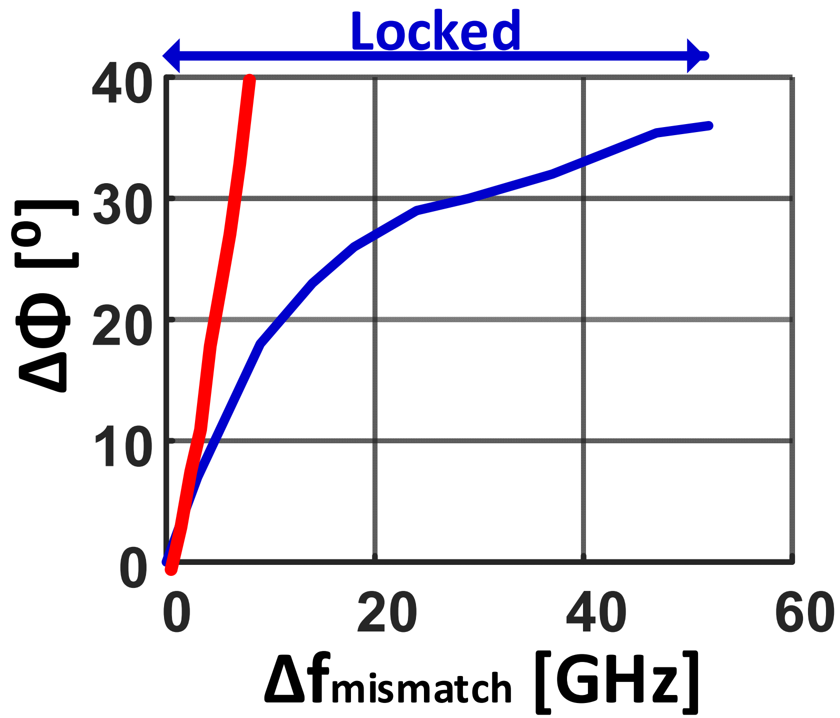
$$f0 = f1 = \frac{1}{\sqrt{C1(L - \Delta L_1)}}$$

$$= f2 \cong \frac{1}{\sqrt{C2(L + \Delta L_2)}}$$

Locking Range = Oscillation Range



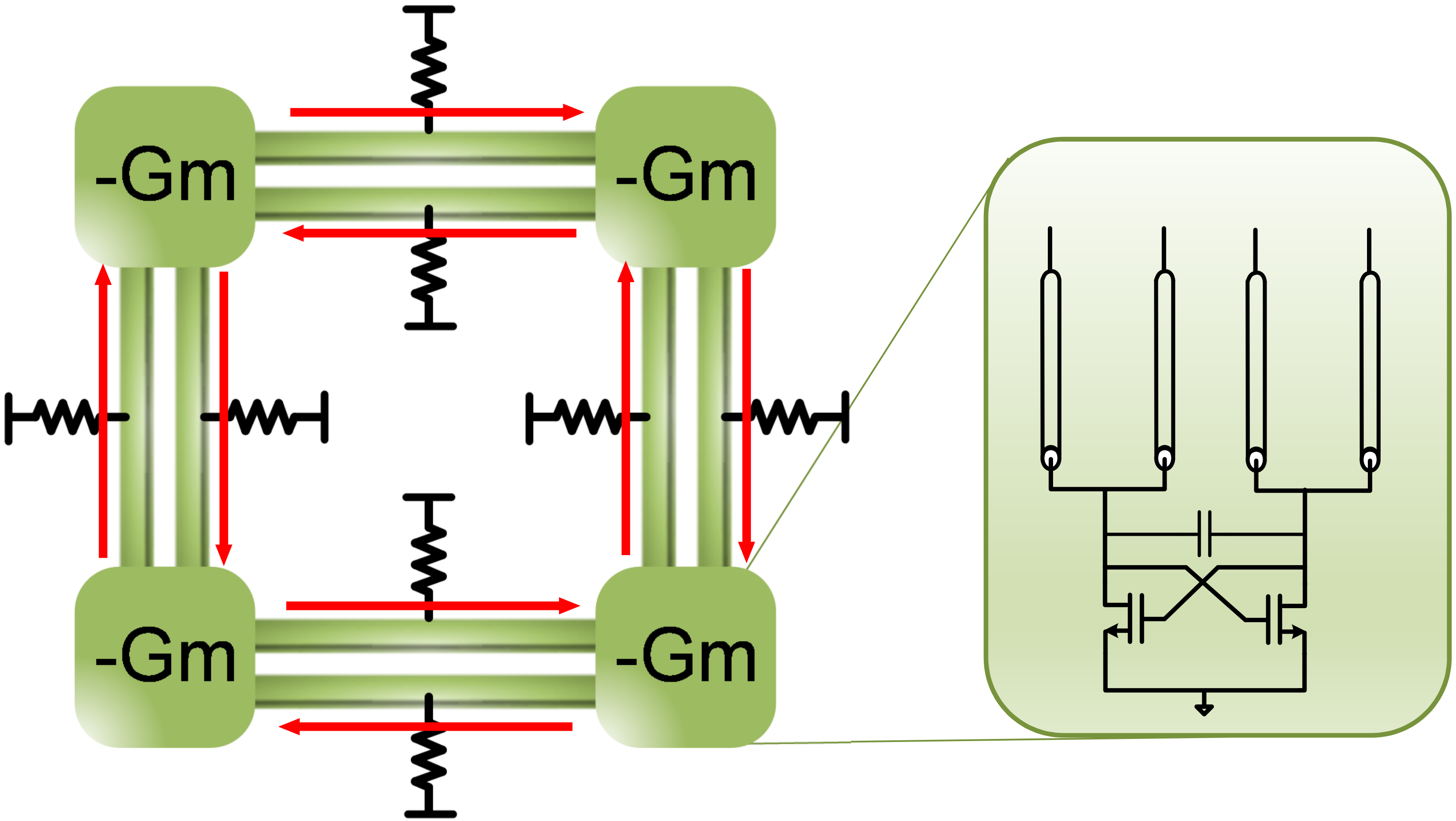




$$\Delta f_{mismatch} = \frac{1}{\sqrt{LC_{eff,1}\downarrow}} - \frac{1}{\sqrt{LC_{eff,2}\uparrow}}$$

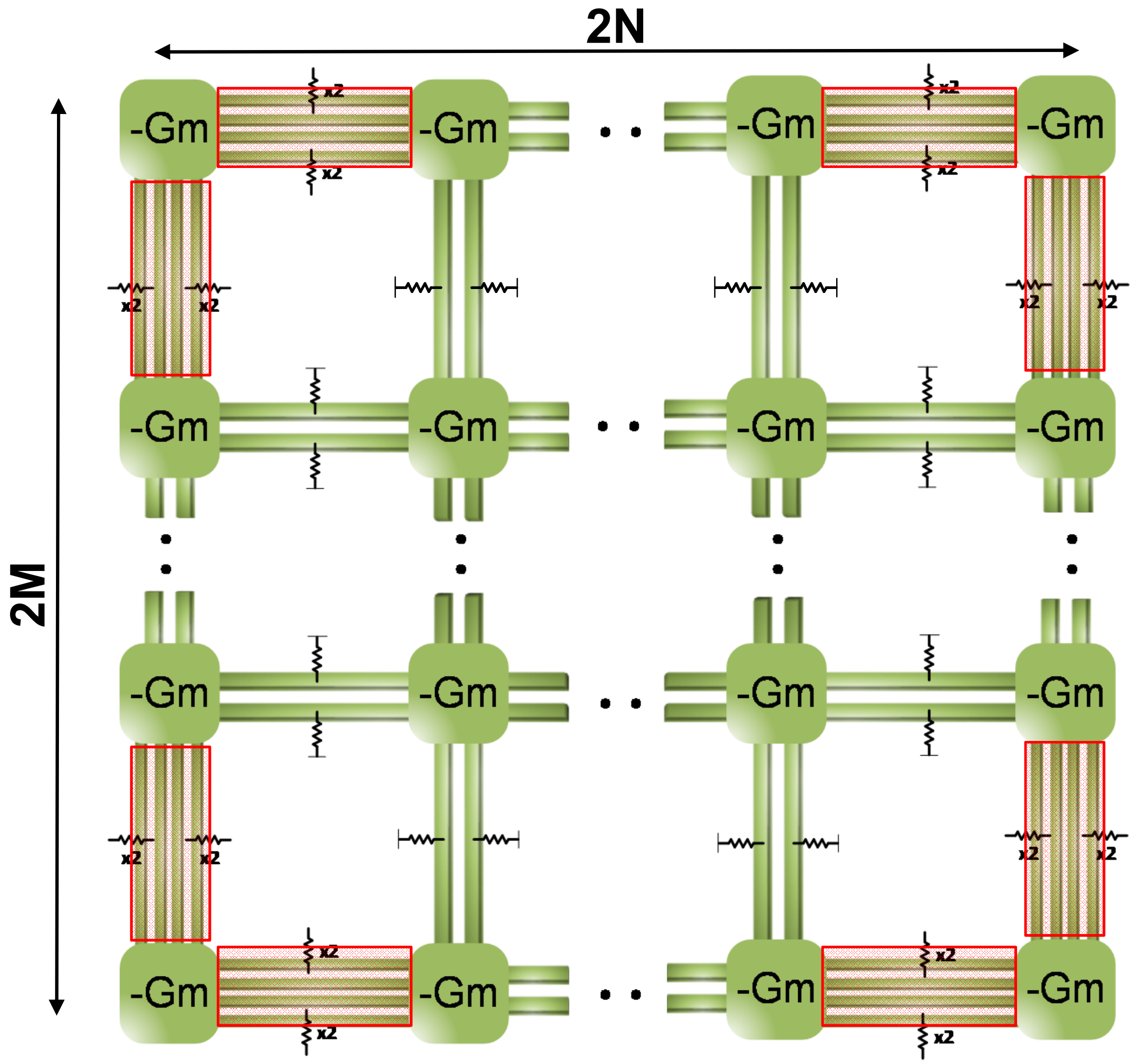
- The pair oscillates synchronously with small phase difference under very large mismatches.

Scaling Up the Synchronous Oscillator Network

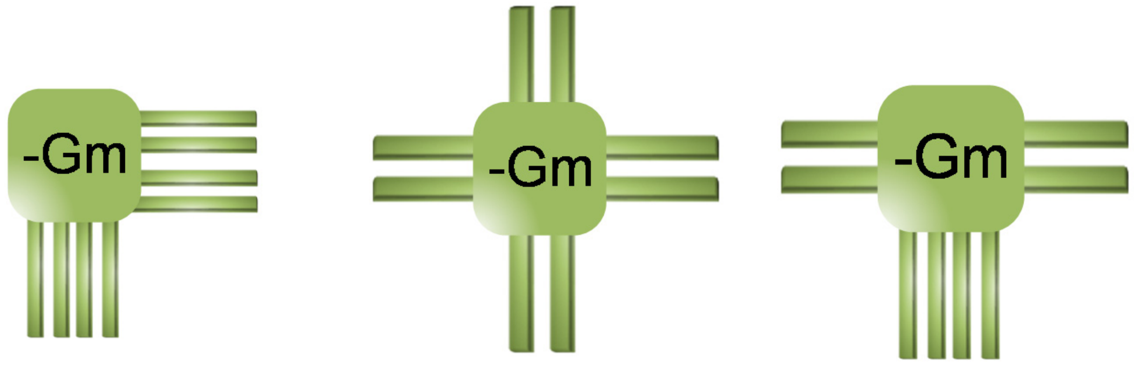


- The network behaves as a single oscillator with 4 spaced –Gm cells.

Scalable Oscillator Network



2N x 2M Core Oscillator



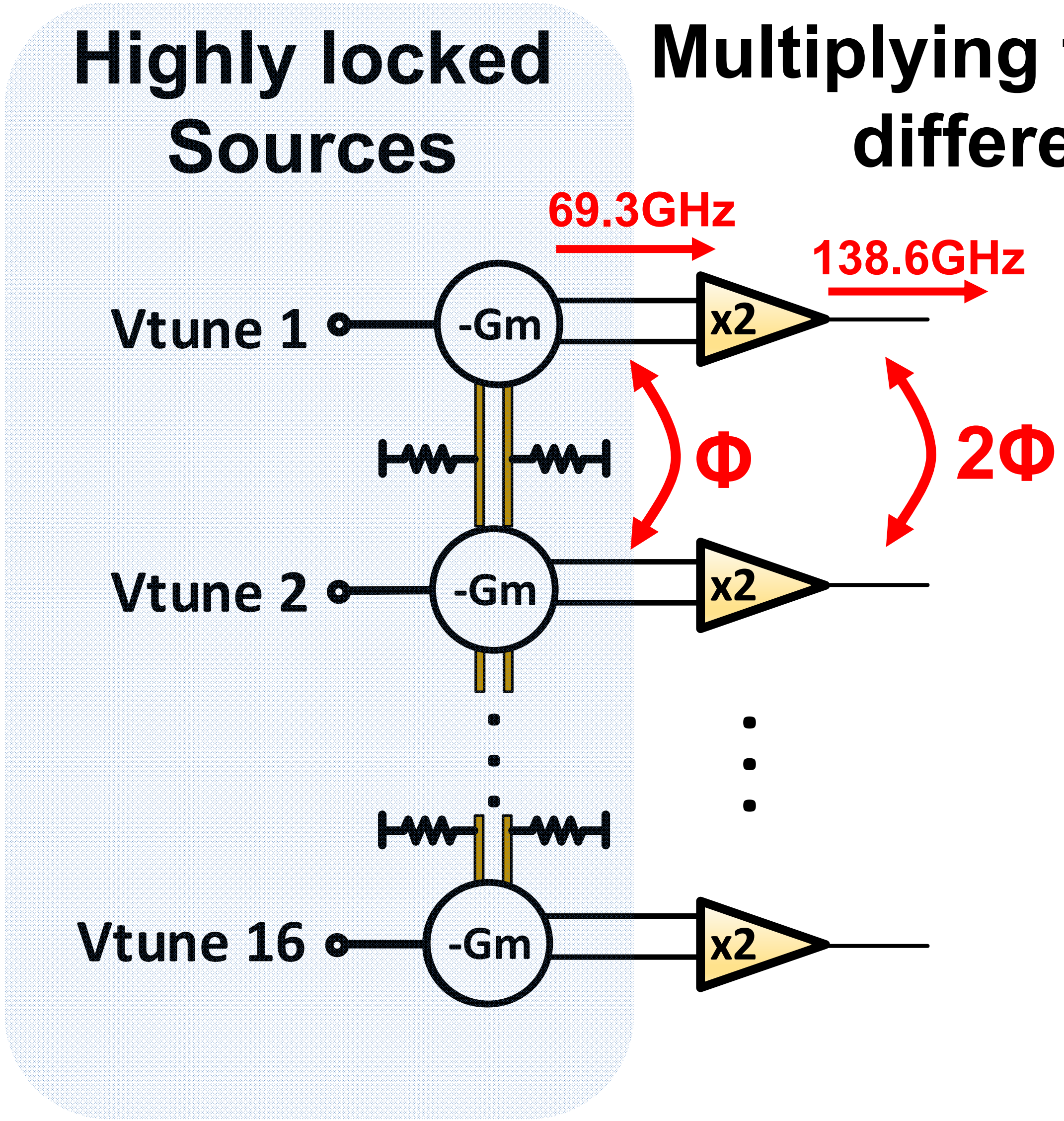
Corner cell Middle cell Side cell

- Corner, side, and middle cells are loaded equally.
- Here we built 4x4 oscillator network around 70 GHz.

Outline

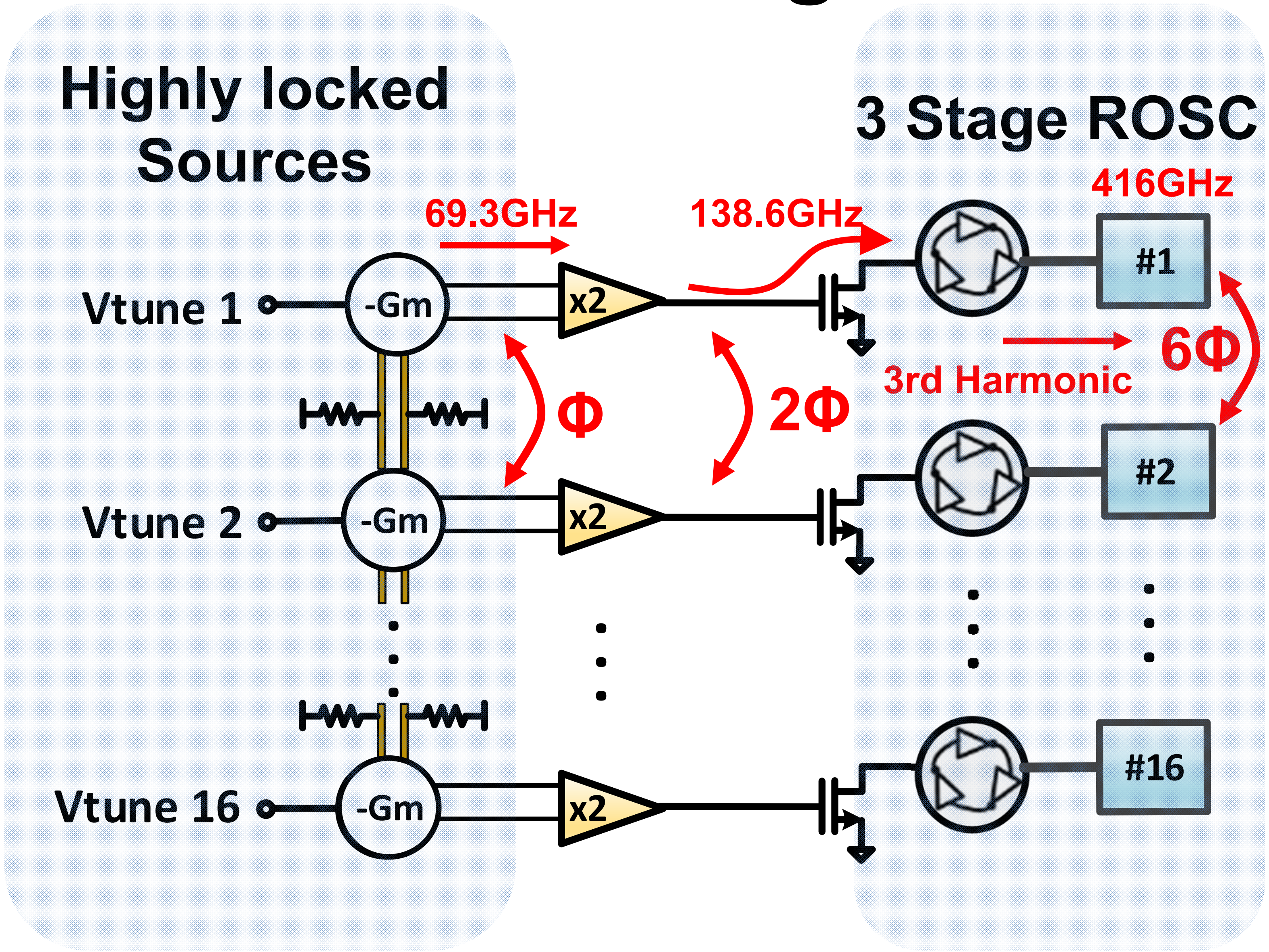
- Large scale and Robust 2D Frequency Reference Network
- **Multi-layer THz Power Generation and Beamforming Capability**
- Measurement Results
- Conclusion

Beamforming and Power Generation



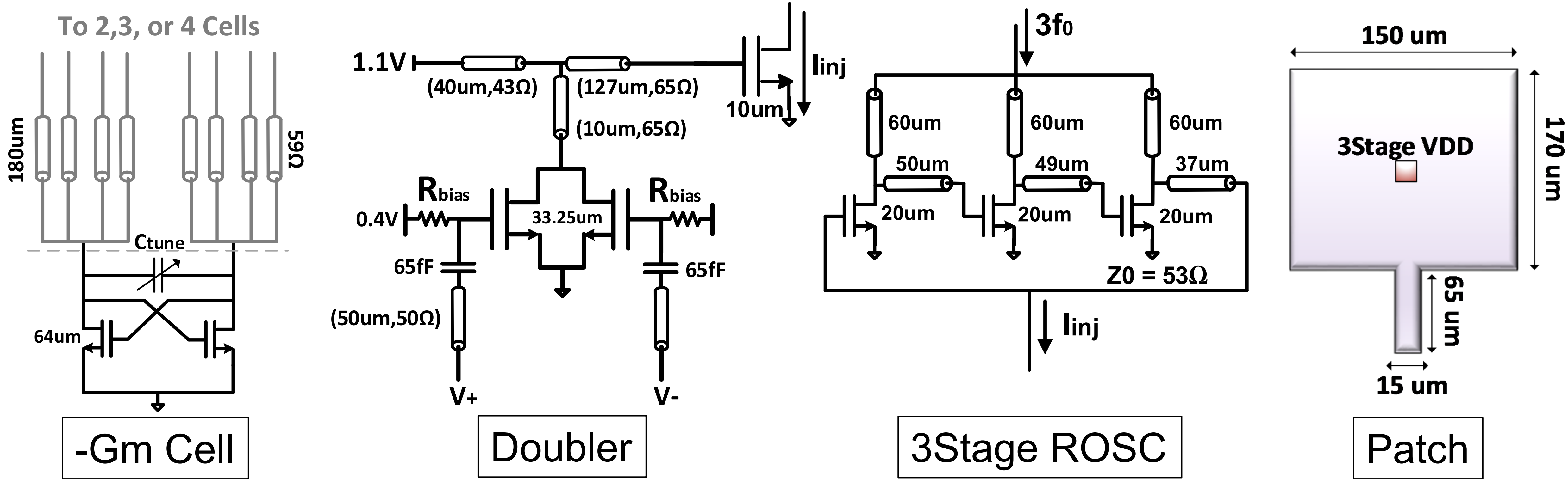
- Adding varactors will enable us to tune the frequency from 68-72GHz
- Doublers are operating at 139 GHz which creates phase difference of 2Φ (required for Beamforming)

Beamforming and Power Generation



- Doubler locked with a 3-stage ring oscillator for output power at 416 GHz.
- Φ variation at 1st layer translates to 6Φ at output under locking condition.
- Simulated EIRP=15 dBm with -2dBm total radiated power

Circuit Blocks



- Varactors will provide frequency tuning range of 68-72GHz.
- Peak simulated radiated power = -2dBm @416GHz.
- Patch antenna efficiency @416GHz = 47%.

Outline

- Large scale and Robust 2D Frequency Reference Network
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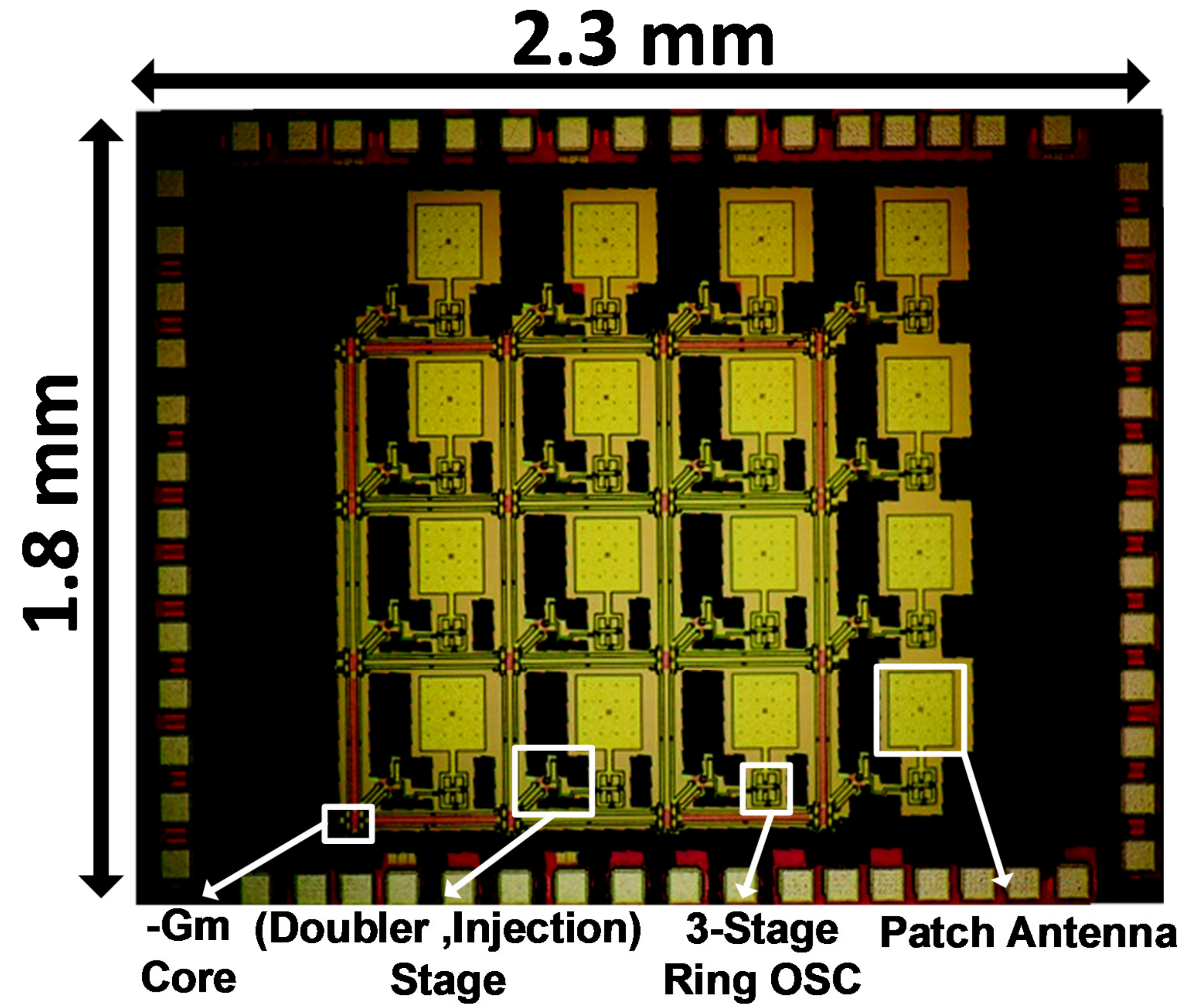
- **Measurement Results**
- Conclusion

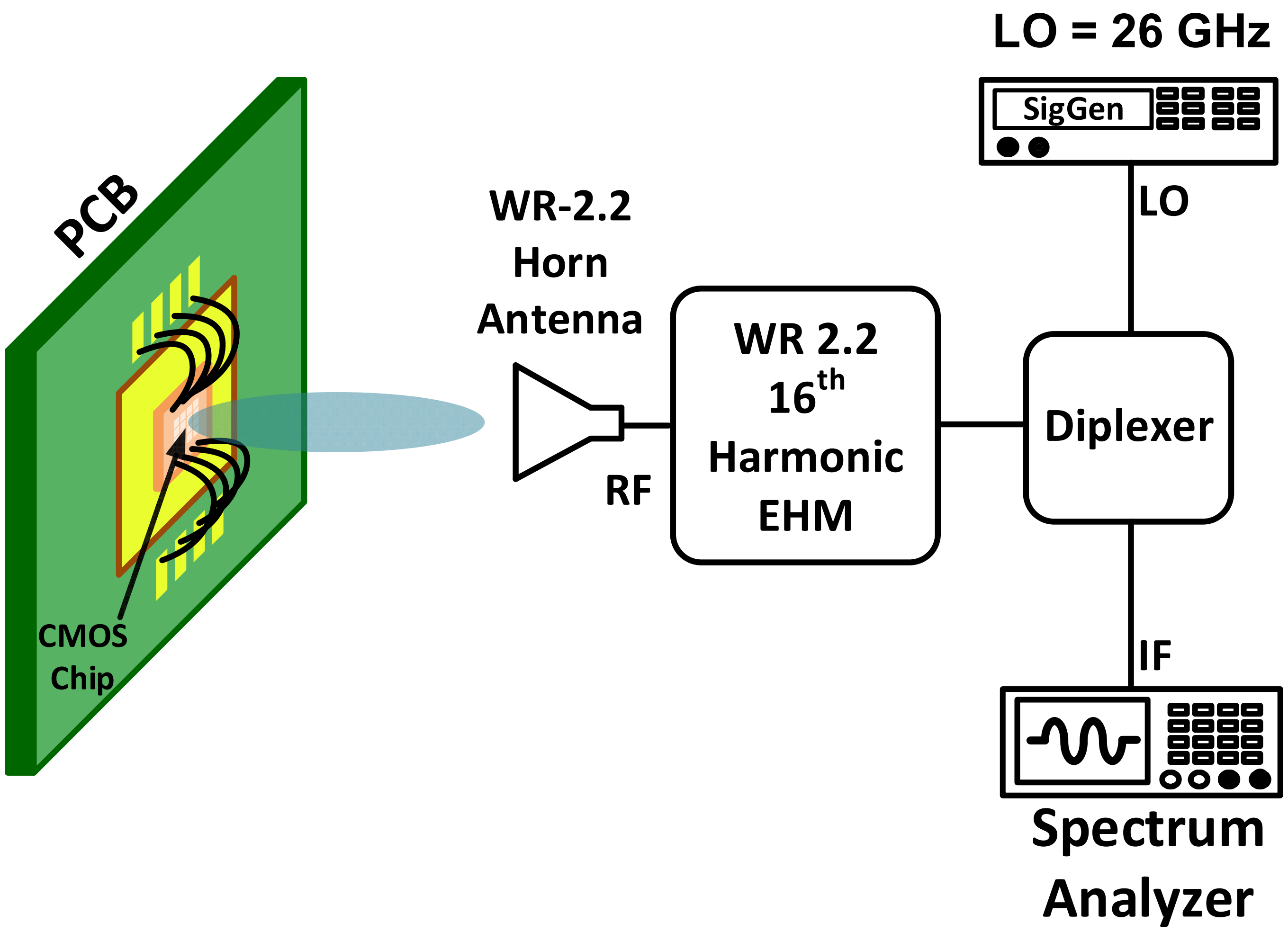
Chip Layout



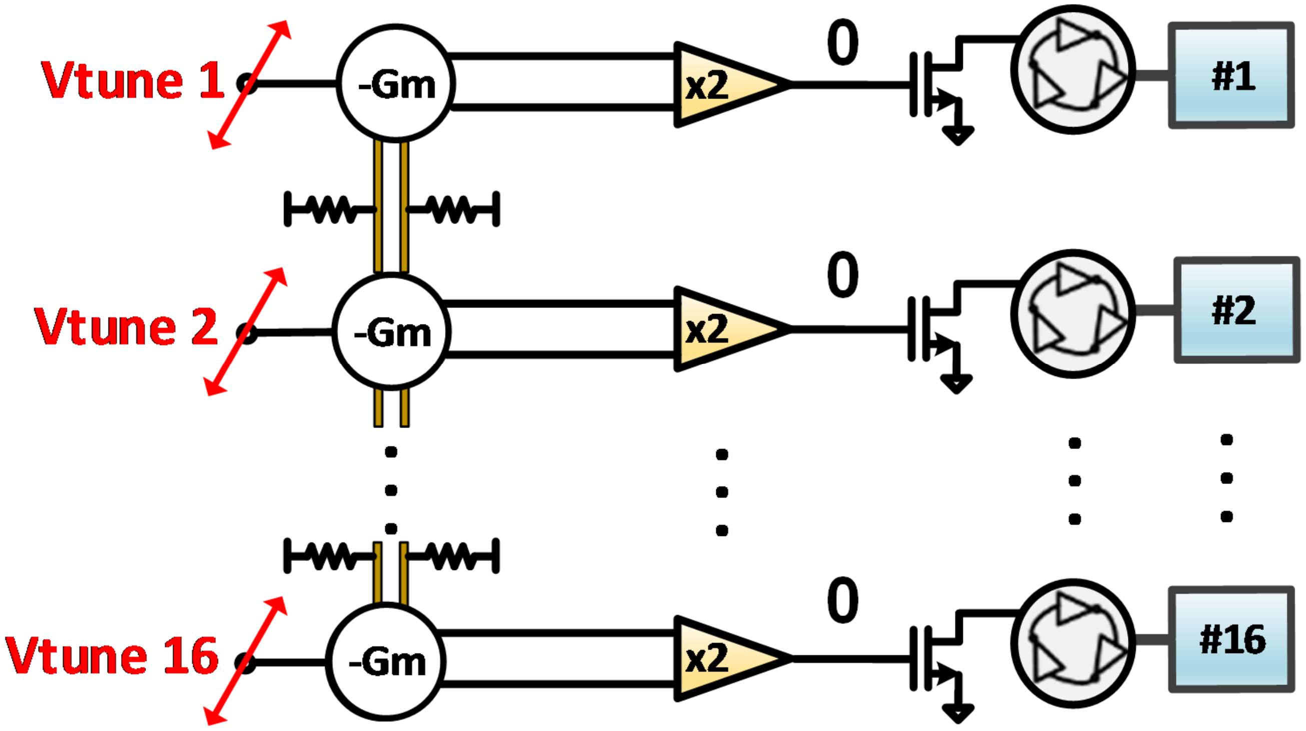
- Chip fabricated in 65 nm CMOS
- Chip area=1.8x2.3 mm^2.

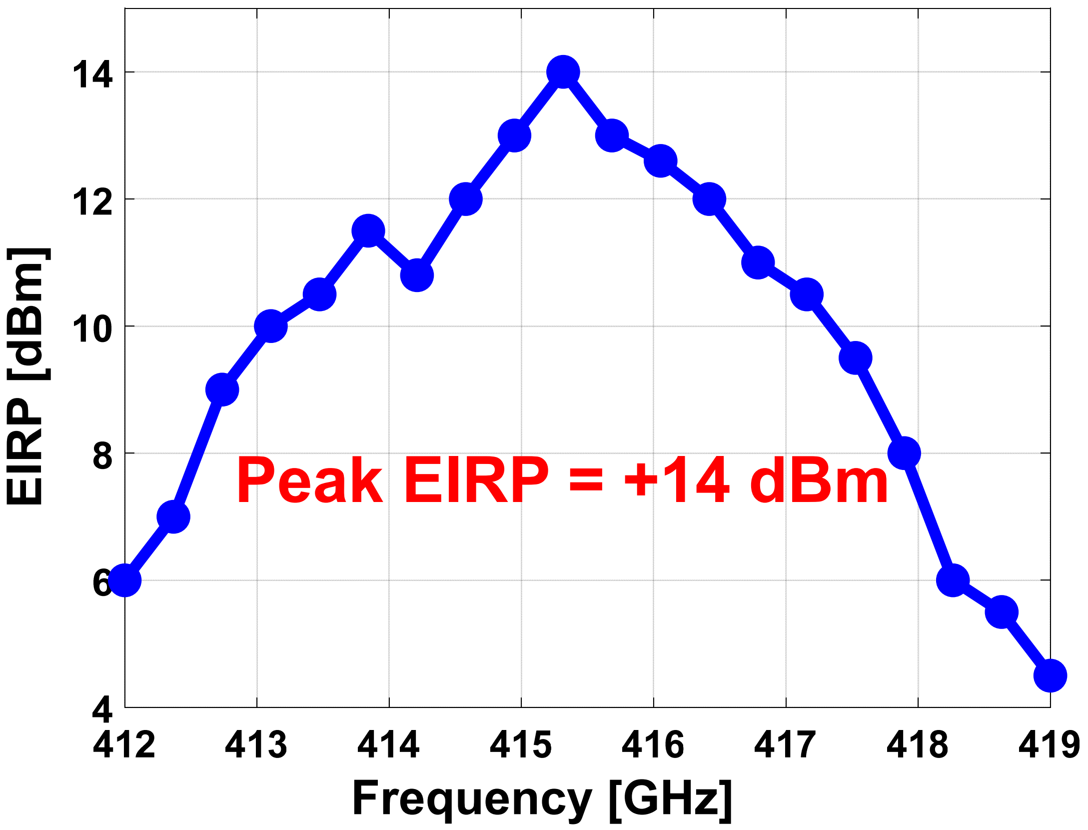
Measurement Setup

- The measurement setup is shown in the following:



EIRP Measurement

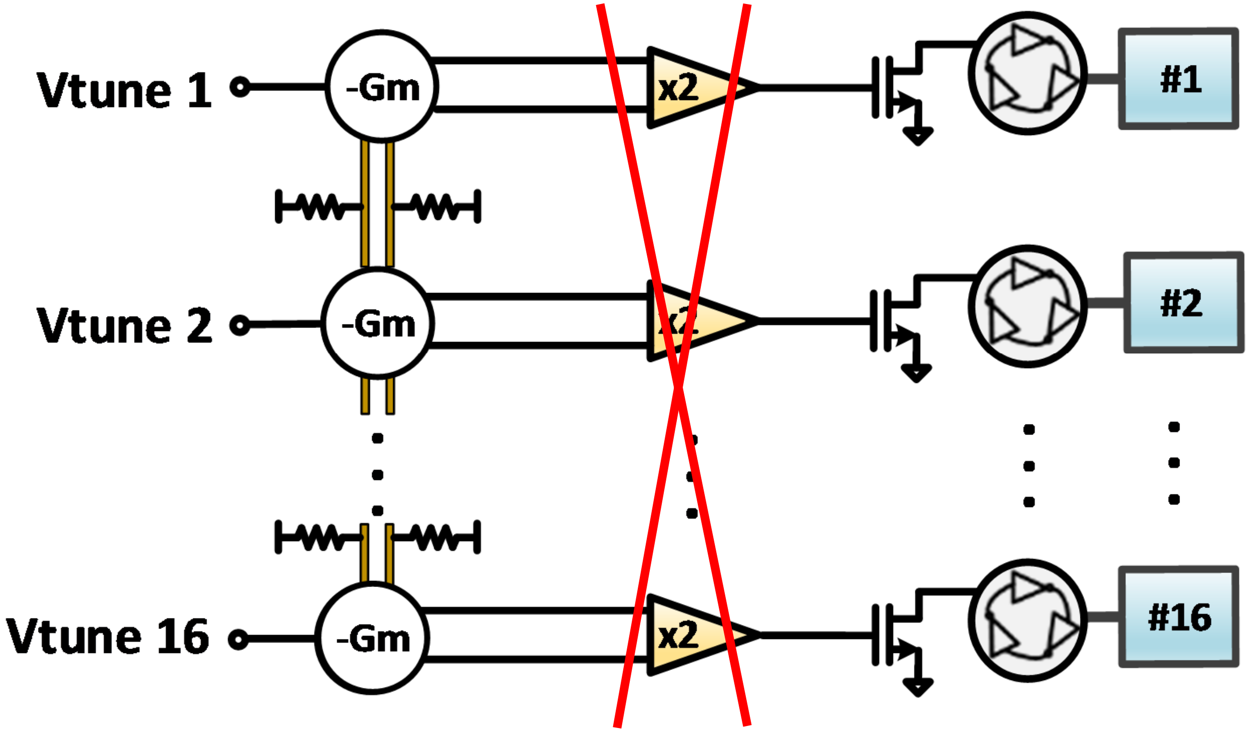


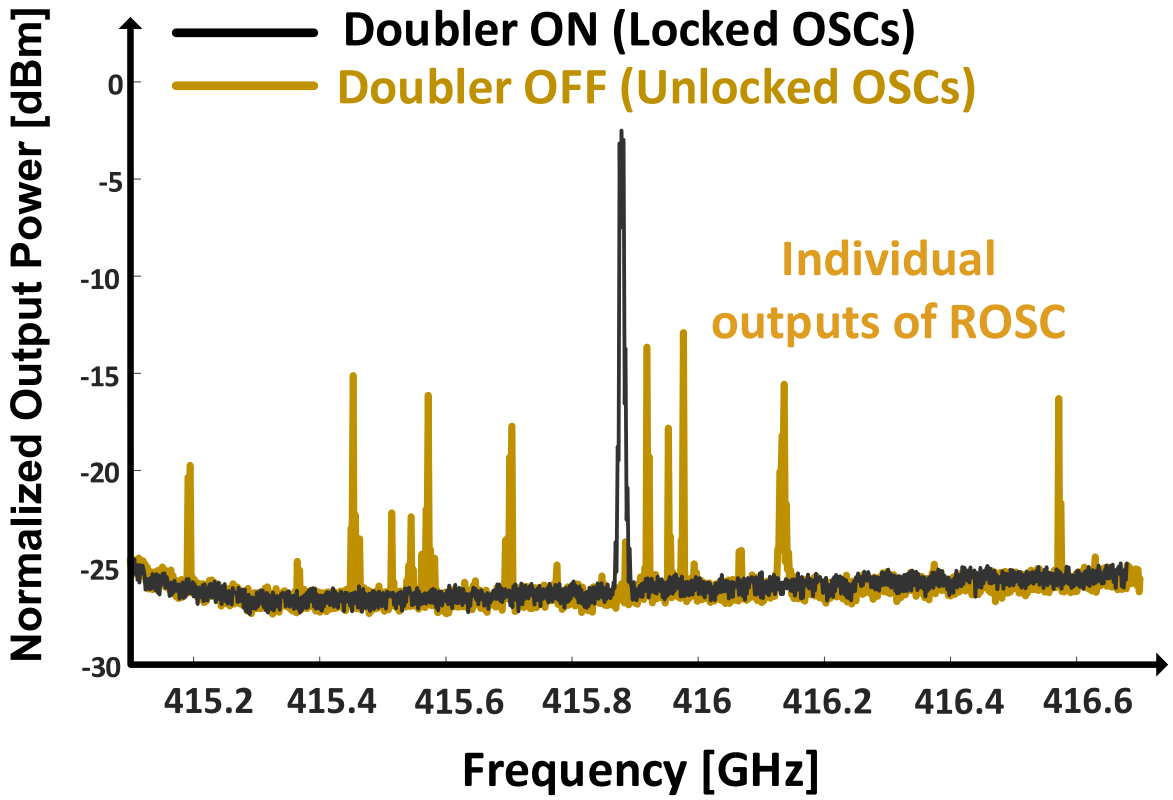


- ❑ Vtune1 =Vtune2= … = Vtune16

- Measured peak EIRP = +14 dBm at 416 GHz.

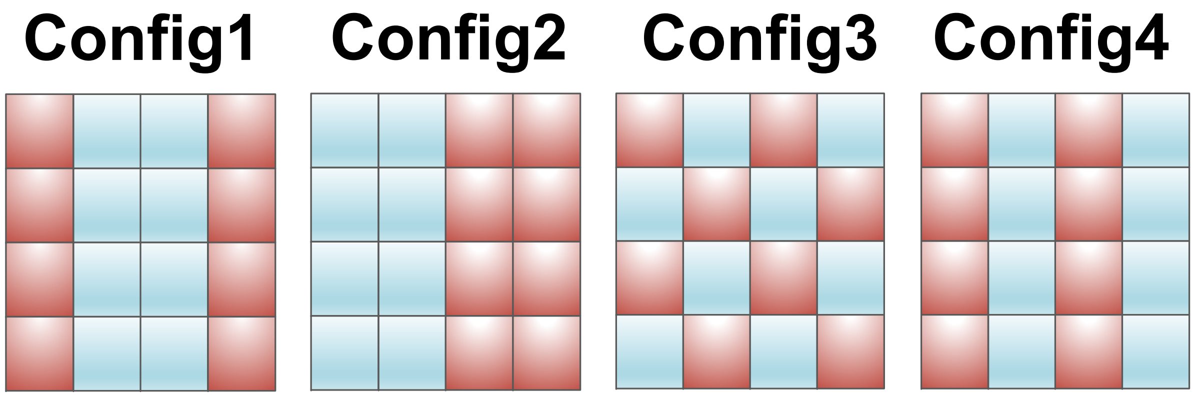
THz Chip Characterization



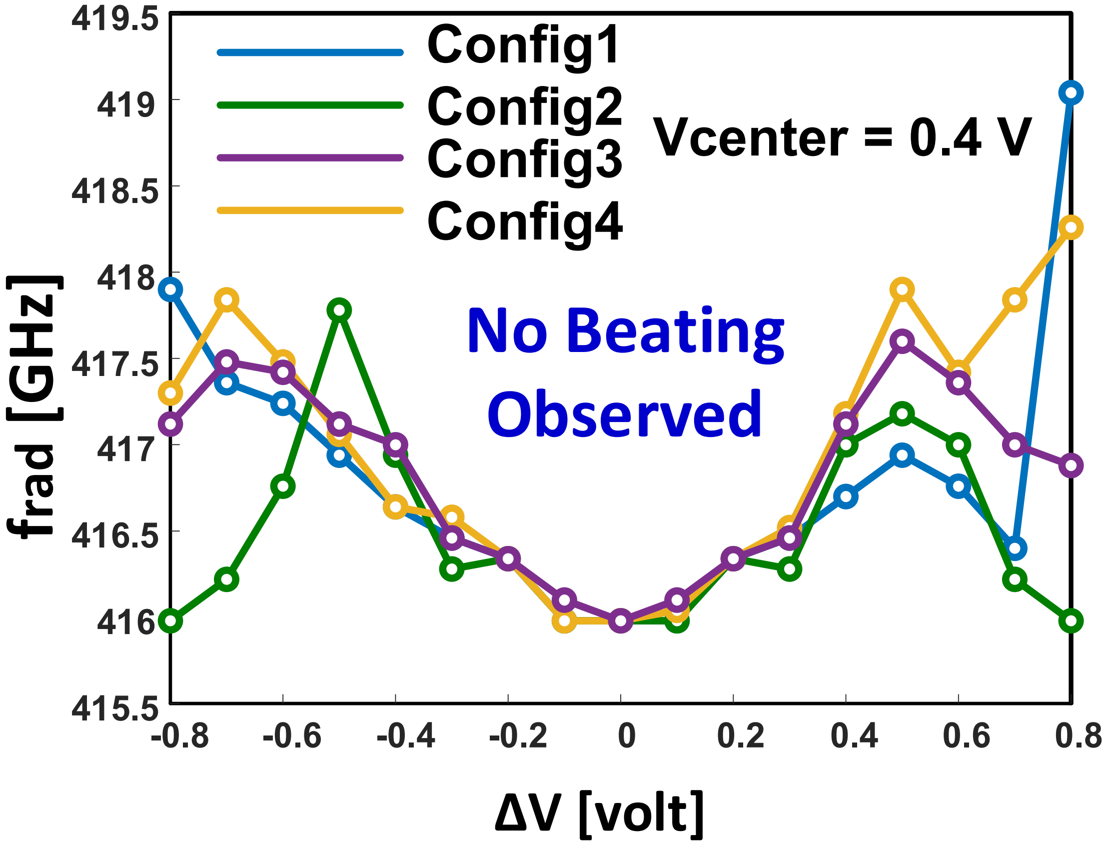


- Turning on the doublers results locks all radiating signals across 415-417 GHz to a single frequency tone.

Robustness Measurement



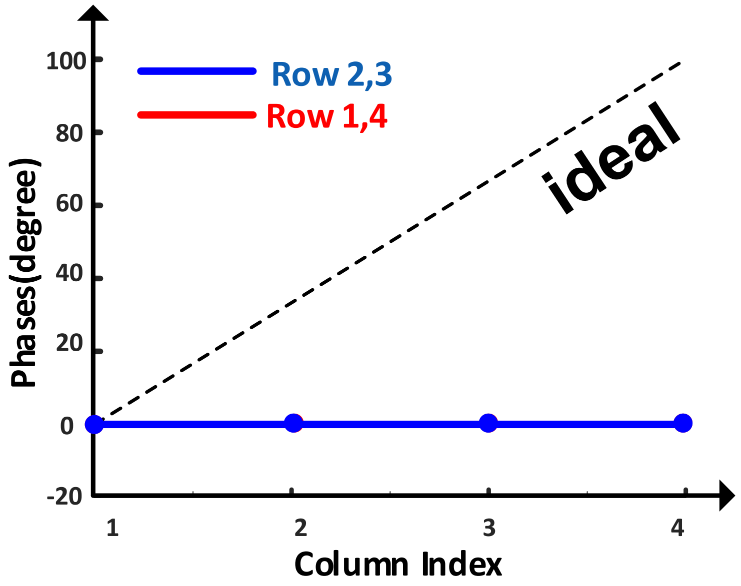
Vtune1 = Vcenter + ΔV/2
Vtune2 = Vcenter – ΔV/2



- Across end-to-end variations of the tuning configurations, the chip radiated synchronously.

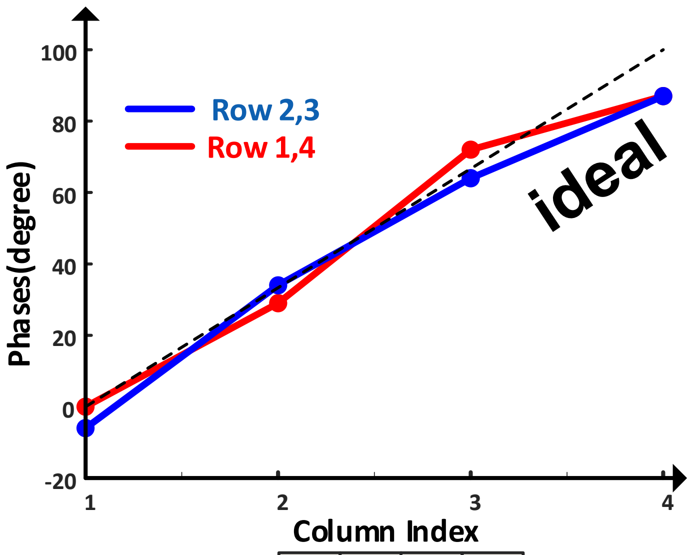
Beamforming Optimization

Initial State



0.4	0.4	0.4	0.4
0.4	0.4	0.4	0.4
0.4	0.4	0.4	0.4
0.4	0.4	0.4	0.4

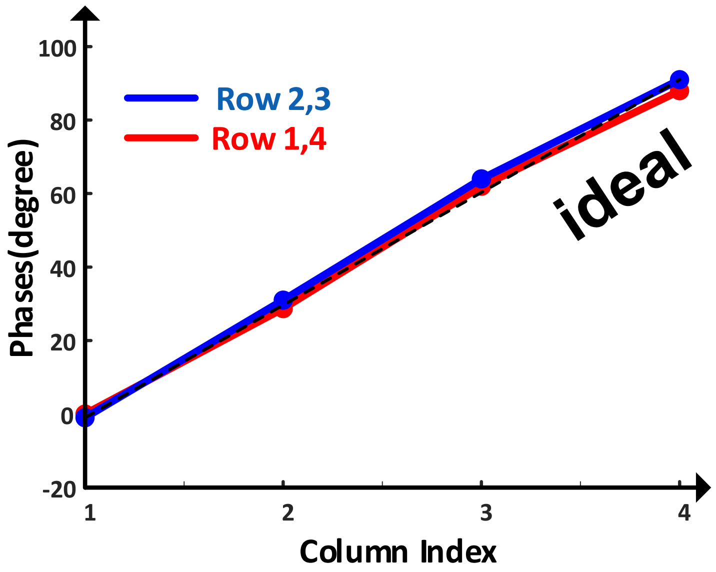
Optimized Step1



1	0.5	0.7	0
1	0.5	0.7	0
1	0.5	0.7	0
1	0.5	0.7	0

optimization

Optimized Step2

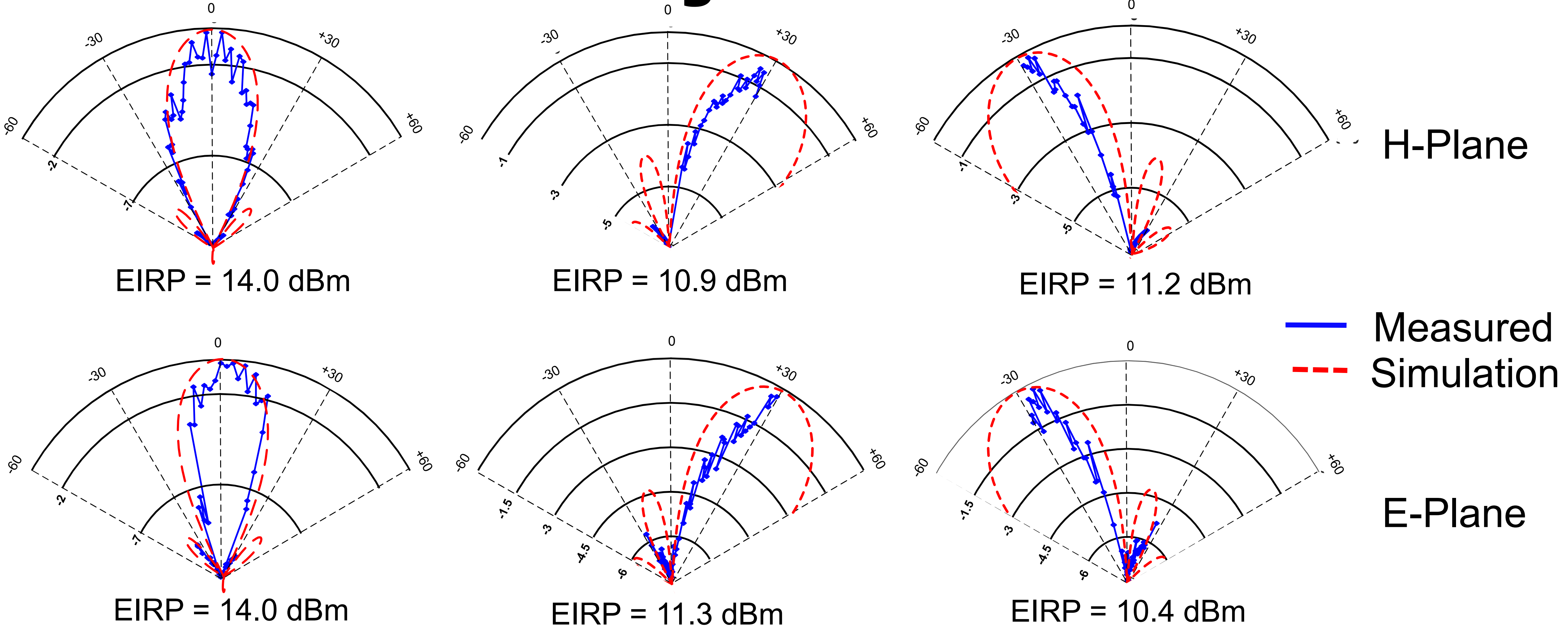


optimization

1	0.55	0.5	0.05
0.95	0.5	0.65	0
0.95	0.5	0.65	0
1	0.55	0.5	0.05

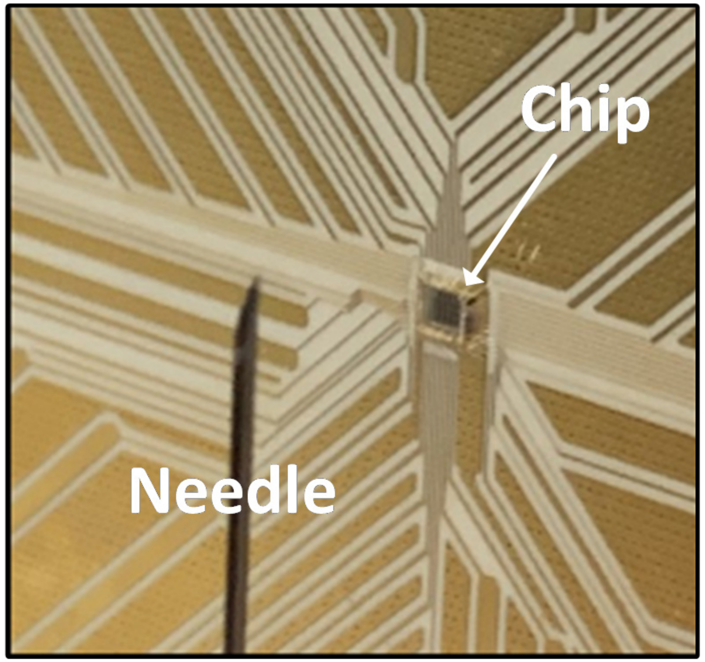
- $15° \times 6 = 90°$ Phase difference at radiation for $30°$ beam steering

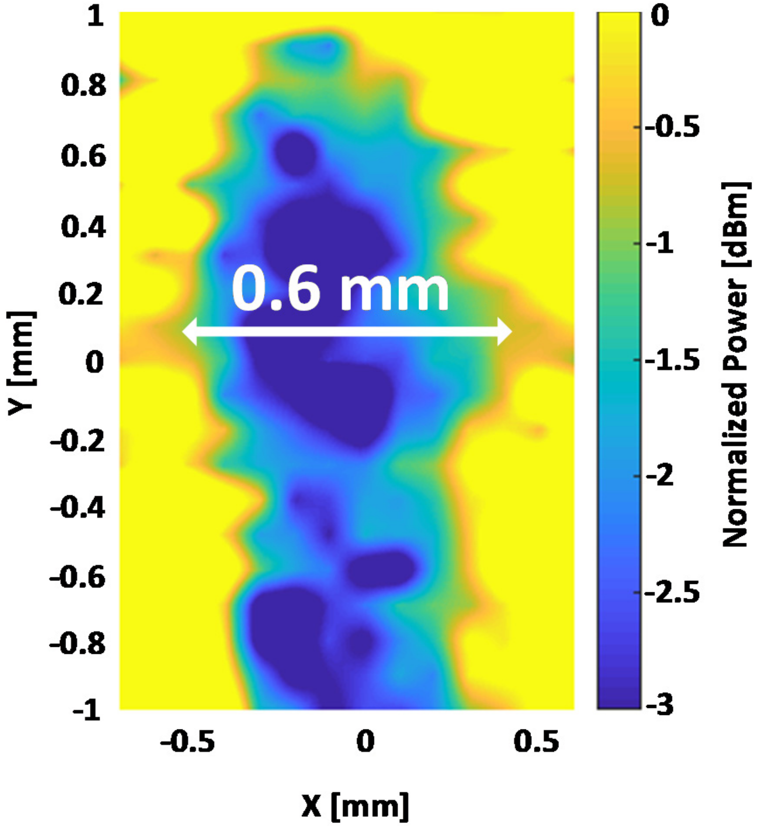
Beamforming Measurement



- Optimal varactor setting obtained for beamforming in the coupled system.

THz Imaging





- The object is placed at 2cm distance from the source with an external receiver.
- THz imaging demonstrated at 416 GHz with the CMOS source.

Comparisons with Recent Works

Metrics	This Work	JSSC 2015 Y.Tousi	ISSCC 2017 H.Jalili	JSSC 2019 K.Guo	JSSC 2014 U. Pfeiffer	RFIC 2017 P. Hilger
Frequency [GHz]	416	338	344	531	530	428
EIRP [dBm]	+14	+17	+4.9	+2.3	+25	+15
Antenna	Patch	Patch	Patch	Patch	Ring antenna + silicon Lens	Ring antenna + silicon Lens
Prad [dBm]	-3	-0.9	-6.8	-12	-12	-12
DC Power [W]	1.45	1.54	0.31 to 0.64	0.26	0.156	0.164
Chip Size [mm2]	4.1	3.9	1.2	2.5	4.2	0.19
Tuning range (%)	1.7	2.1	15.1	0.9	3.2	2.1
Tech.(fmax)	65nm CMOS (250 GHz)	65nm CMOS (250 GHz)	130nm SiGe (215 GHz)	40nm CMOS (300 GHz)	130nm SiGe (500 GHz)	130nm SiGe (450 GHz)
Beam Steering [º]	60/60	45/50	128/53	60	0	0

Conclusions

- We demonstrated a scalable 2D frequency reference network robust to mismatches and process variations, where locking range = oscillation range.
- A multi-layer harmonic generation network for THz power generation, radiation and beamforming was demonstrated.
- Measured EIRP at 416 GHz is +14 dBm with ±30^{O} of beam-scanning in space.

Thank you!

All members of the IMRL!

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