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SESSION 13
Cryo-CMOS
for Quantum Computing

A Fully Integrated Cryo-CMOS SoC for Qubit Control in Quantum Computers Capable of State Manipulation, Readout and High-Speed Gate Pulsing of Spin Qubits in Intel 22nm FFL FinFET Technology

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Self Introduction



- B.S. degree from Yonsei Univ., Seoul, Korea, 2012
- Ph.D. degree from Georgia Tech, GA, USA, 2017
- Have been with Intel Labs, Hillsboro, OR, since 2018
- My research interests include
 - Analog/RF/mm-wave integrated circuits and systems for
 - Quantum computers
 - Wireless communications

Outline

- Motivation
- System Specifications and Cryo-CMOS SoC Design
 - Microwave Drive
 - Gate pulsing
 - Readout
- Measurement Results
- Conclusions

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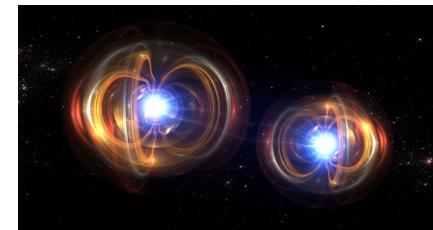
Motivation

Exponential speed-up in solving certain complex problems

- Security
→ Shor's algorithm, RSA encryption



- Solving naturally quantum mechanical problems
→ quantum chemistry

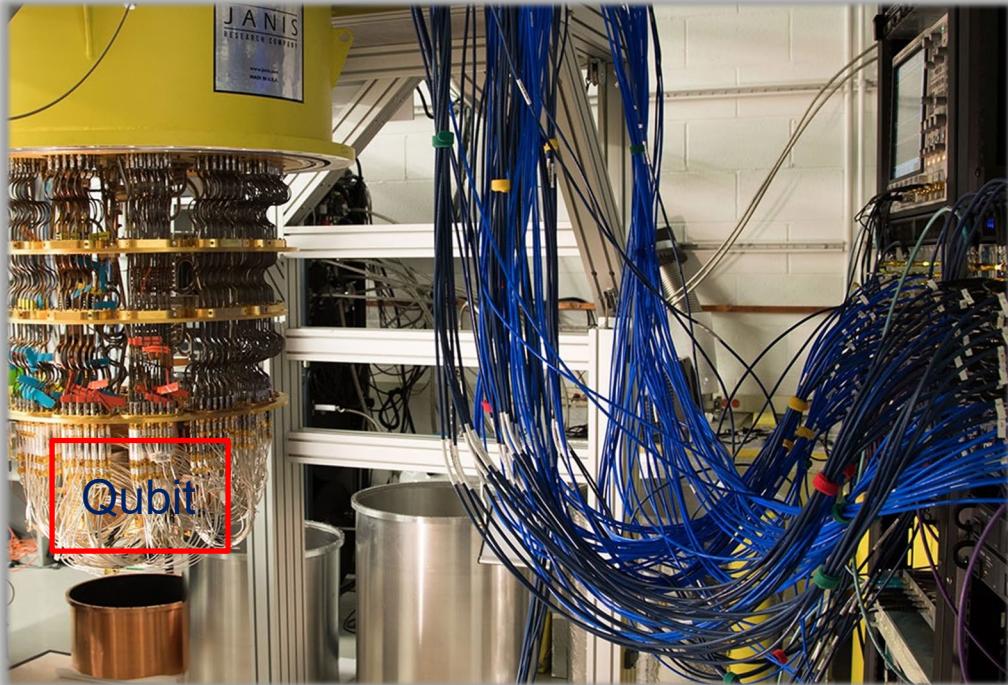


- Optimization
→ optimizing traffic routing



>1000 qubits quantum computer is required to solve useful problems

Scaling to Many Qubits



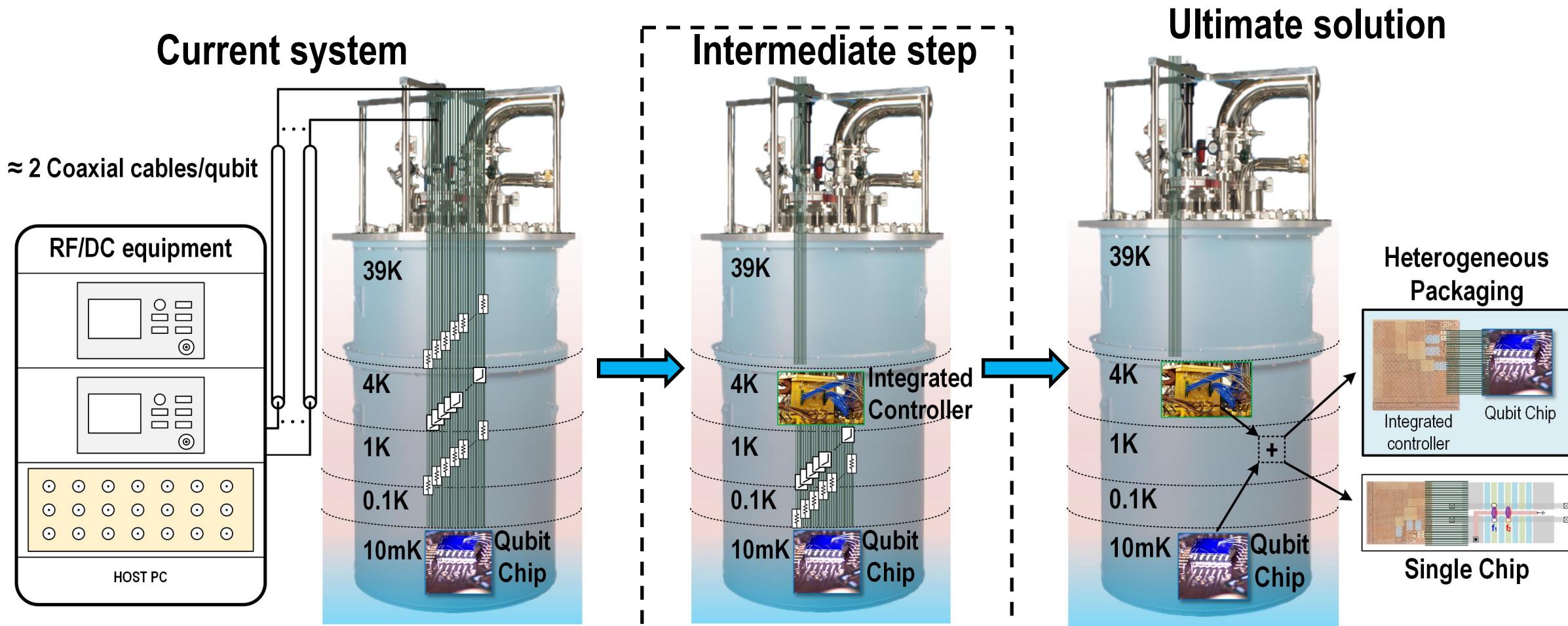
[Bardin, ISSCC 2019]

- Room temperature electronics controlling qubits in dilution refrigerator → ≈ 2 coax cables/qubit
 - Current approach does not scale
 - Form factor
 - Thermal load on fridge
 - Power consumption and cost
- Largest quantum computer < 100 qubits

Integrated SoC controller placed at 4K to address current scalability challenges

Path to Scalable Quantum Computer

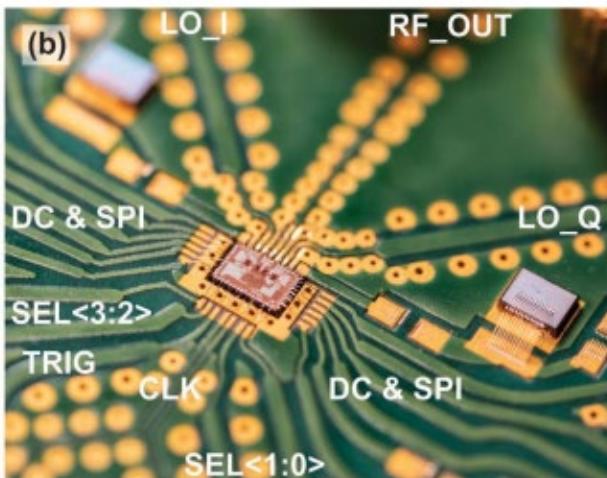
Cryo-CMOS integrated SoC intermediate and ultimate goals



13.1: A Fully Integrated Cryo-CMOS SoC for Qubit Control in Quantum Computers Capable of State Manipulation, Readout and High-Speed Gate Pulsing of Spin Qubits in Intel 22nm FFL FinFET Technology

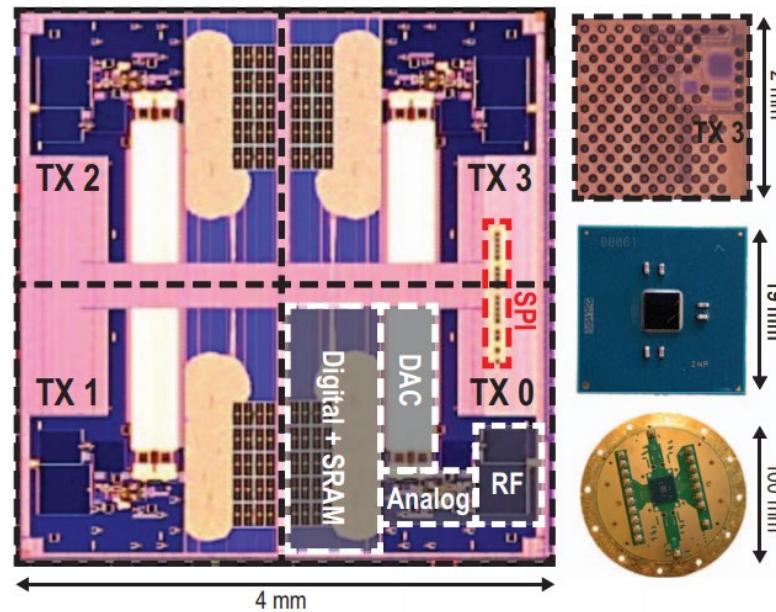
Prior Art

[J. Bardin et al ISSCC 2019]



- Qubit state manipulation

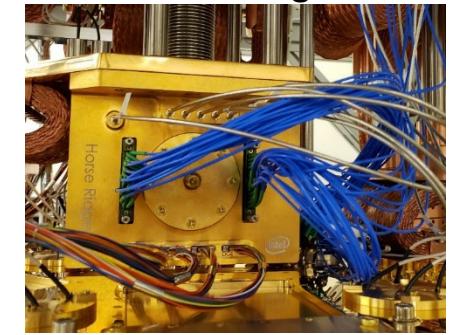
[B. Patra et al ISSCC 2020]



- Qubit state manipulation

- Frequency-multiplexing
- Arbitrary I/Q pulse generation
- Digitally-intensive architecture

Horse Ridge II



- Qubit state manipulation
 - Digital FIR filter
- High-speed gate pulsing
- Qubit state readout
 - TX/RX for RF reflectometry
 - On-chip demodulator
- Microprocessor
 - Integrated instruction sets

Outline

■ Motivation

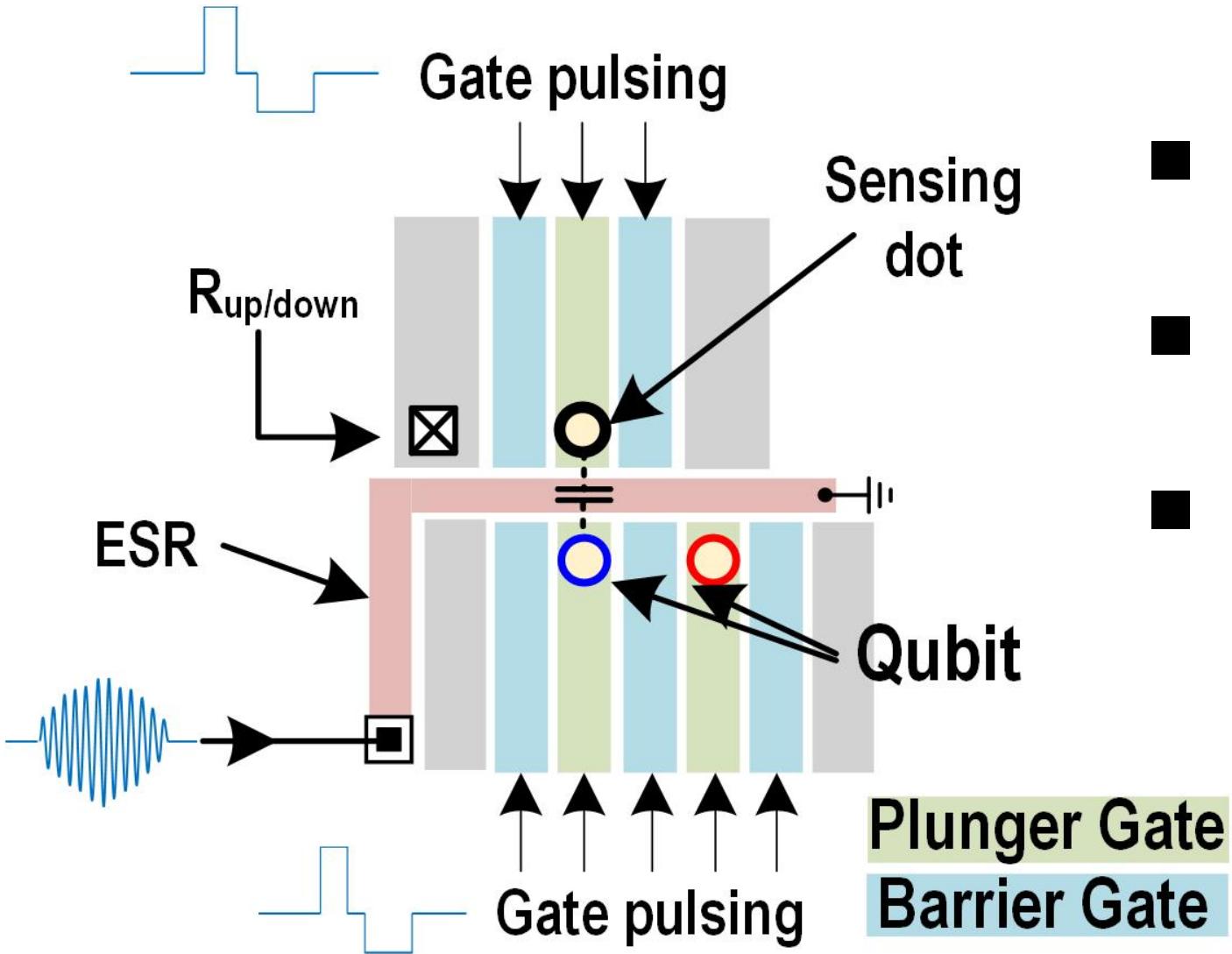
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- Microwave Drive
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- Readout

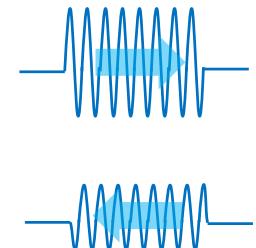
■ Measurement Results

■ Conclusions

Control Signals for Qubits

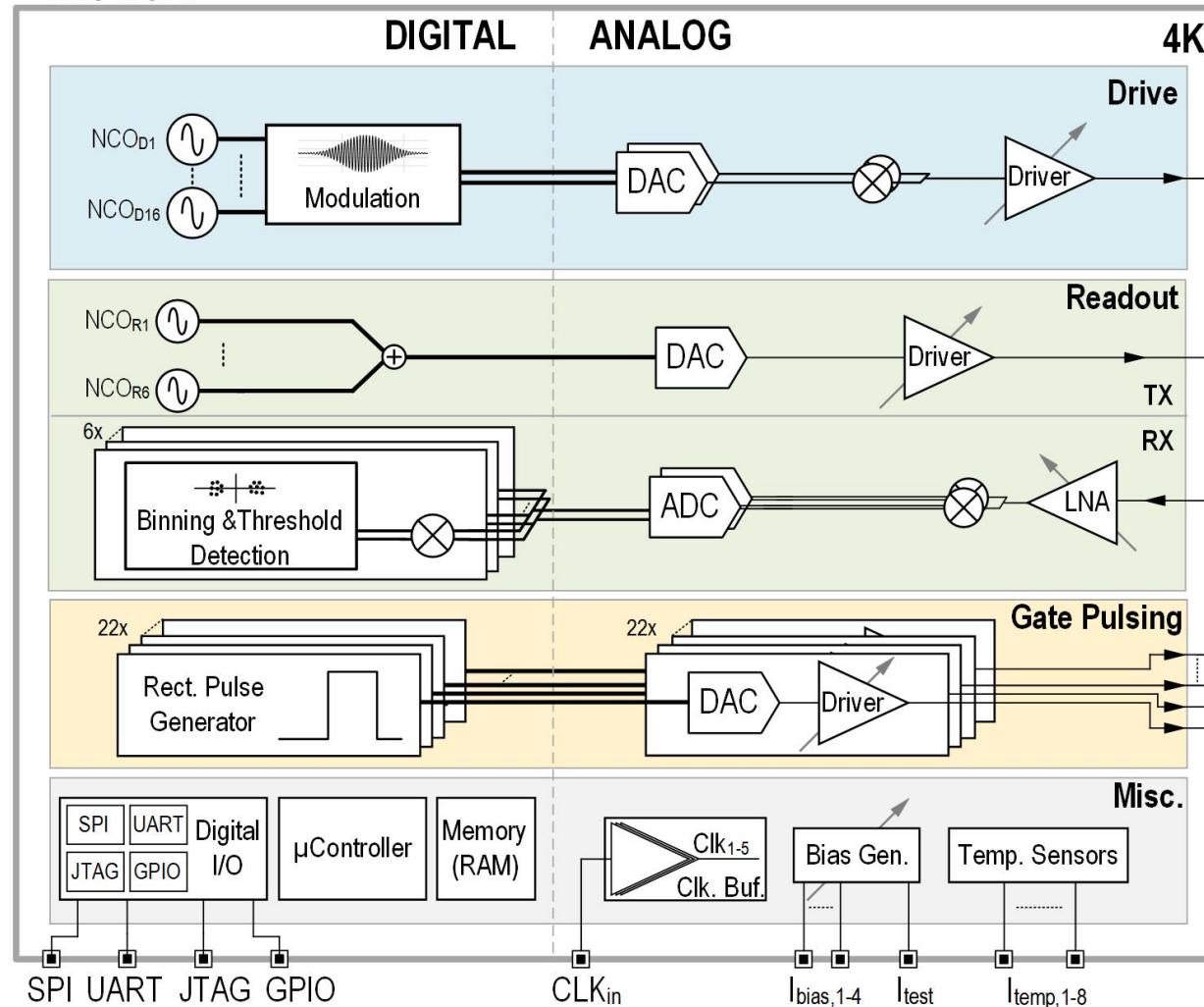


- Manipulate qubit states (drive)
 - RF pulses
- Qubit biasing and entanglement
 - Square pulses
- Read qubit state ($R_{\text{up/down}}$)
 - Generate stimulus
 - Detect amplitude and phase response in reflected pulse



The Proposed SoC

This work



- Drive: microwave pulse generation
- RF reflectometry readout: multitone signal generation and detection of reflected signal
- Gate pulsing: square pulse generation
- Quantum instruction set architecture (QISA) with integrated microcontroller
- Integrated temperature sensing

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Bloch Sphere

- North pole
 - Ground state $|0\rangle$

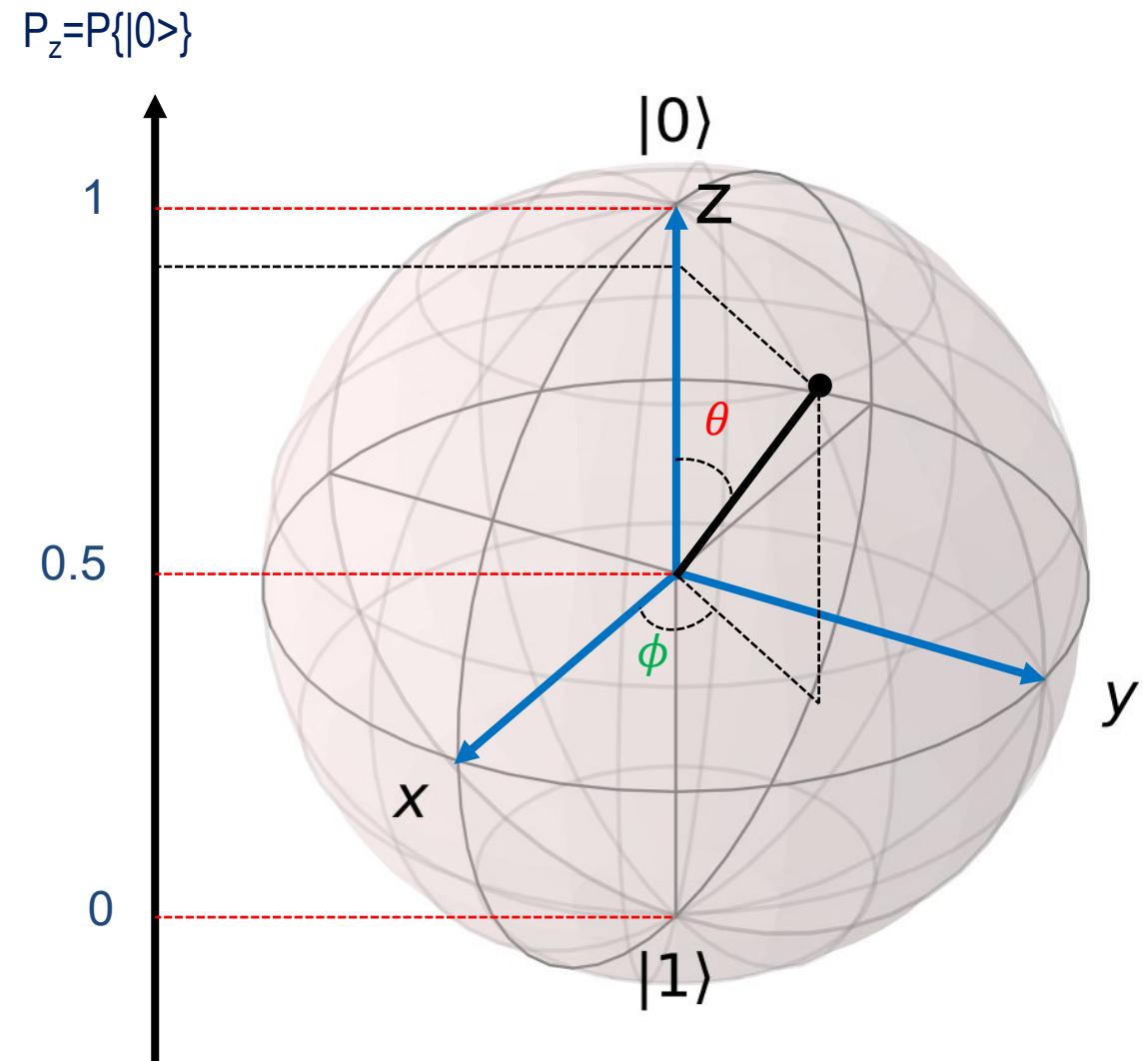
- South pole
 - Excited state $|1\rangle$

- Any point on the sphere
 - Pure state

$$\psi = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{i\phi}\sin\left(\frac{\theta}{2}\right)|1\rangle$$

- Projection on z-axis
 - Qubit state probability

$$P\{|0\rangle\} = \cos^2\left(\frac{\theta}{2}\right)$$



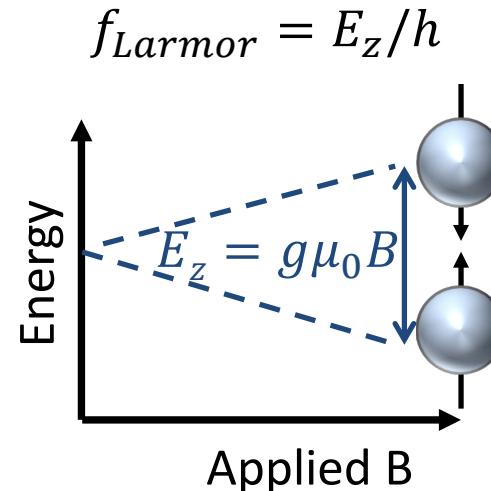
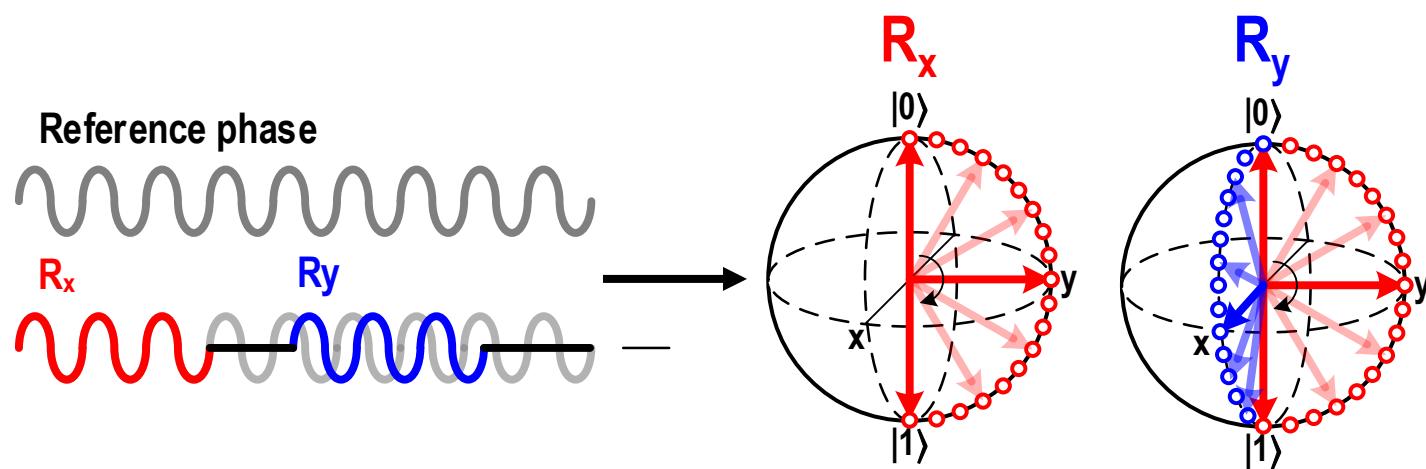
Qubit Drive: System Specifications

- **Qubit state manipulation (R_x , R_y)**

Microwave freq. → matching with qubit Larmor freq.

Qubit rotation angle \propto pulse energy (amplitude × duration)

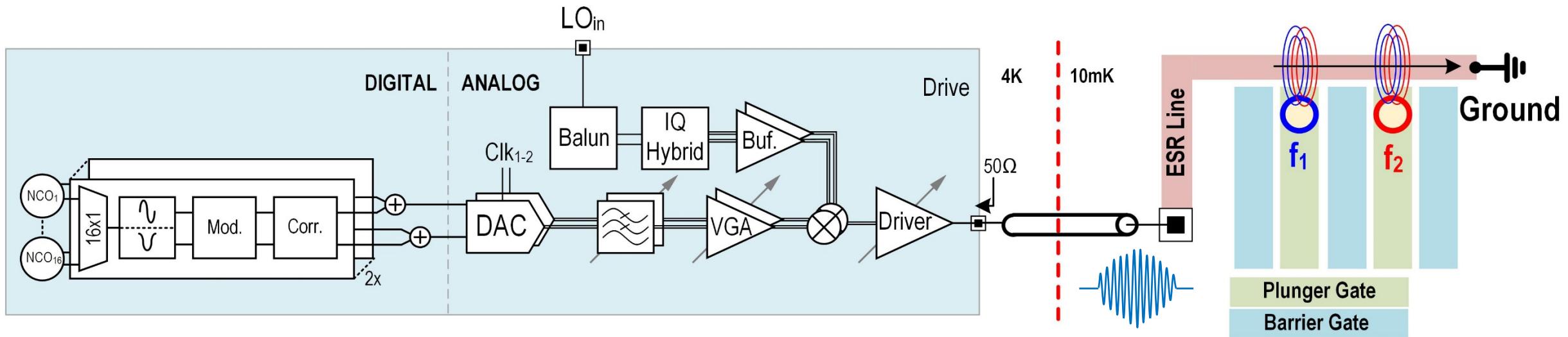
Qubit rotation axis → pulse phase



| | |
|----------------------|-------------------------|
| Frequency | 10-18GHz |
| Power | -35dBm at the qubit |
| IMD3 | -50dBc |
| SNR over 25MHz | >44dB (99.99% fidelity) |
| Output impedance | 50Ω |
| Pulse duration | 16ns to 5000ns |
| Amplitude resolution | 8.5bit |

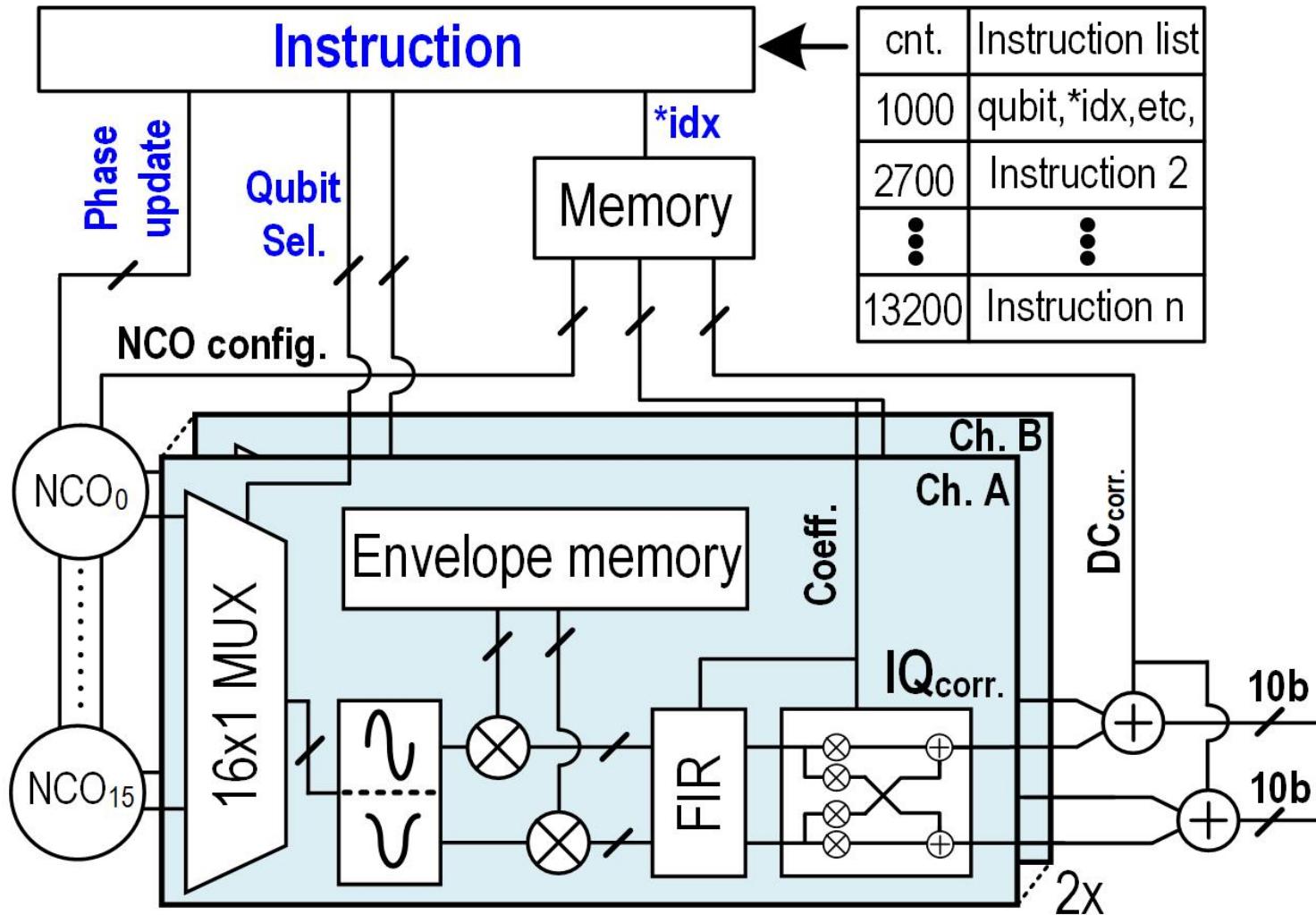
[J. Dijk et al, Physical Review Applied, 2019]

Qubit Drive: System Block Diagram



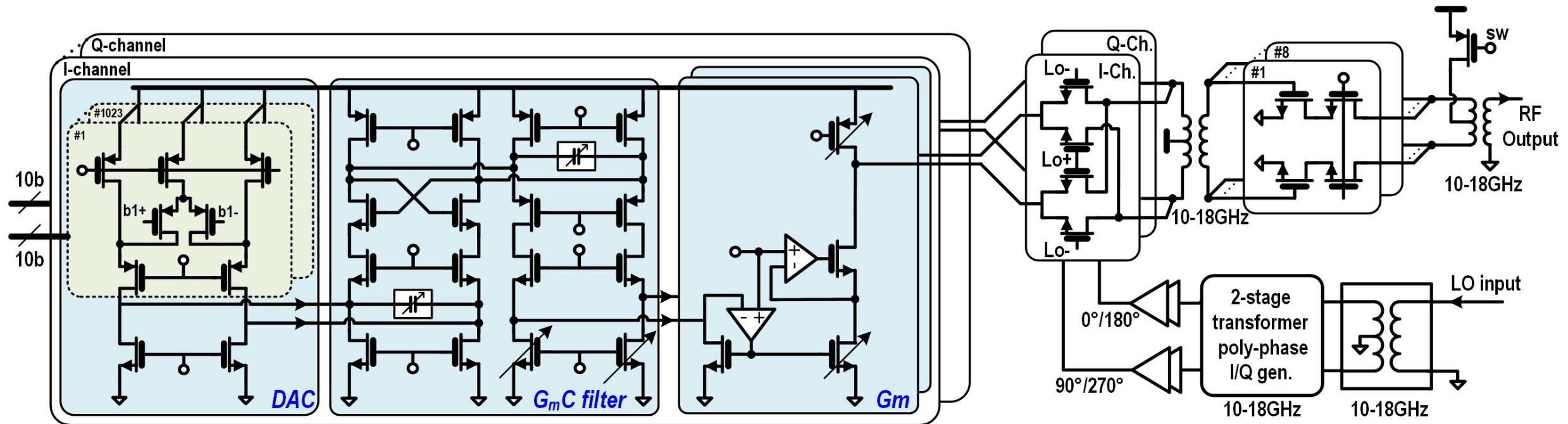
- Chip output at 4K is connected to the grounded Electron Spin Resonance (ESR) line of the qubit chip at 10mK
- Direct digital synthesis (DDS) and low-IF scheme
- Support up to 16 qubits with 1 ESR line by frequency multiplexing
- Wideband 50Ω output impedance to absorb reflected signal

Qubit Drive: Digital Design



- Simultaneous 2-qubit manipulation
- 16 NCOs track the phase of 16 qubits
- Instantaneous phase update for Z-correction
- FIR filter for qubit cross-talk mitigation
- Envelope template shared across all instructions to save memory

Qubit Drive: Analog/RF Design



- 40dB amplitude control
- Integrated wideband 2-stage transformer-based hybrid for IQ generation
- Wideband transformer matching for 10-18GHz RF bandwidth
- Integrated PA shunt switch to suppress LO leakage and noise during readout

Outline

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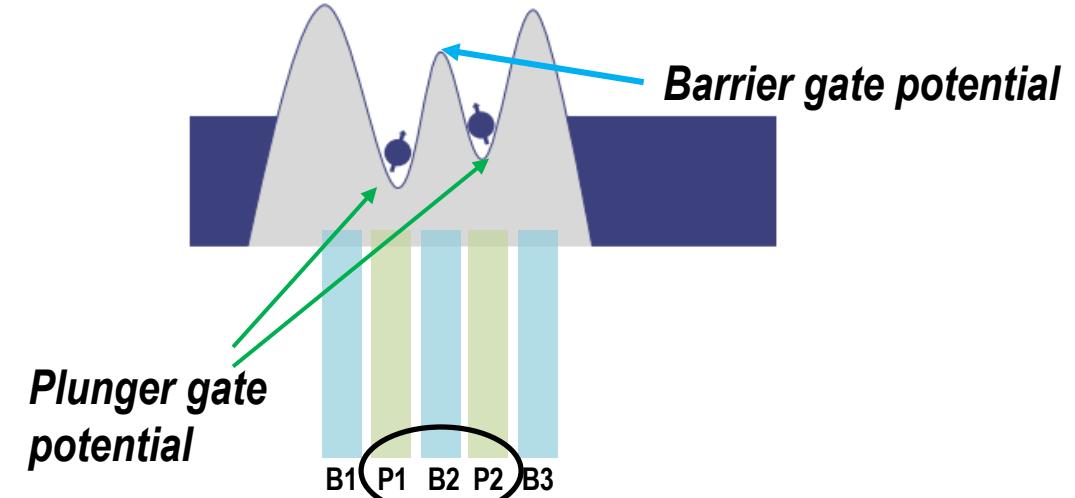
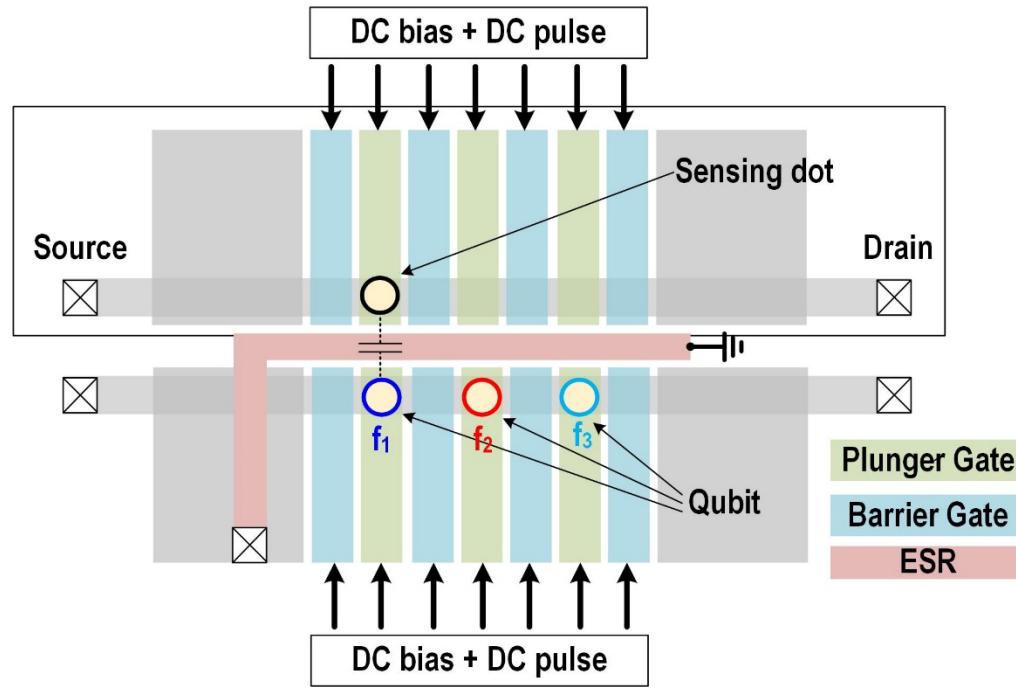
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Gate Pulsing: System Specifications

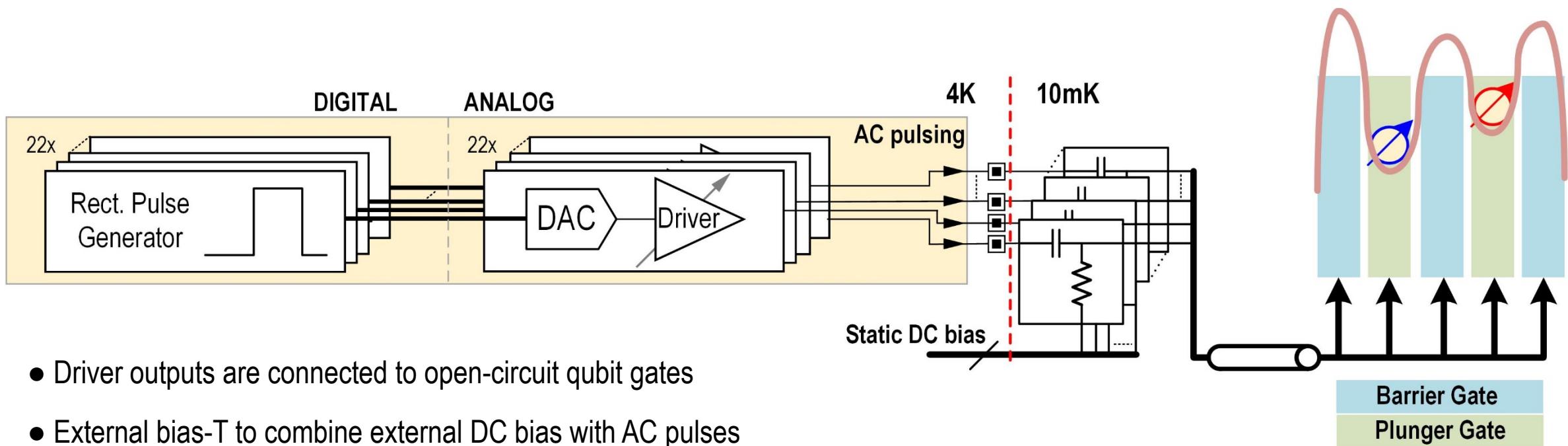


[C. Volk et al, *npj Quantum Information* 2019]

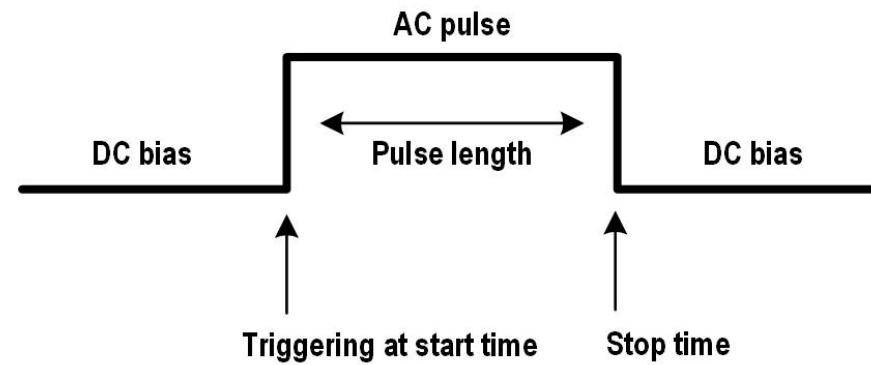
- Plunger gate sets quantum dot electrochemical potential
- Barrier gate controls qubit-to-qubit interaction (entanglement)
- Each qubit has 1 plunger gate and 1 barrier gate \rightarrow 2 gates/qubit
- **Both DC bias and AC pulses are required for initialization, manipulation, entanglement, and readout**

| | |
|----------------------|--------------------|
| Amplitude resolution | 11bit, 300 μ V |
| Integrated noise | <1LSB |
| Output impedance | 50 Ω |
| Rising/fall time | 10ns |
| Pulse duration | 100ns to 1ms |

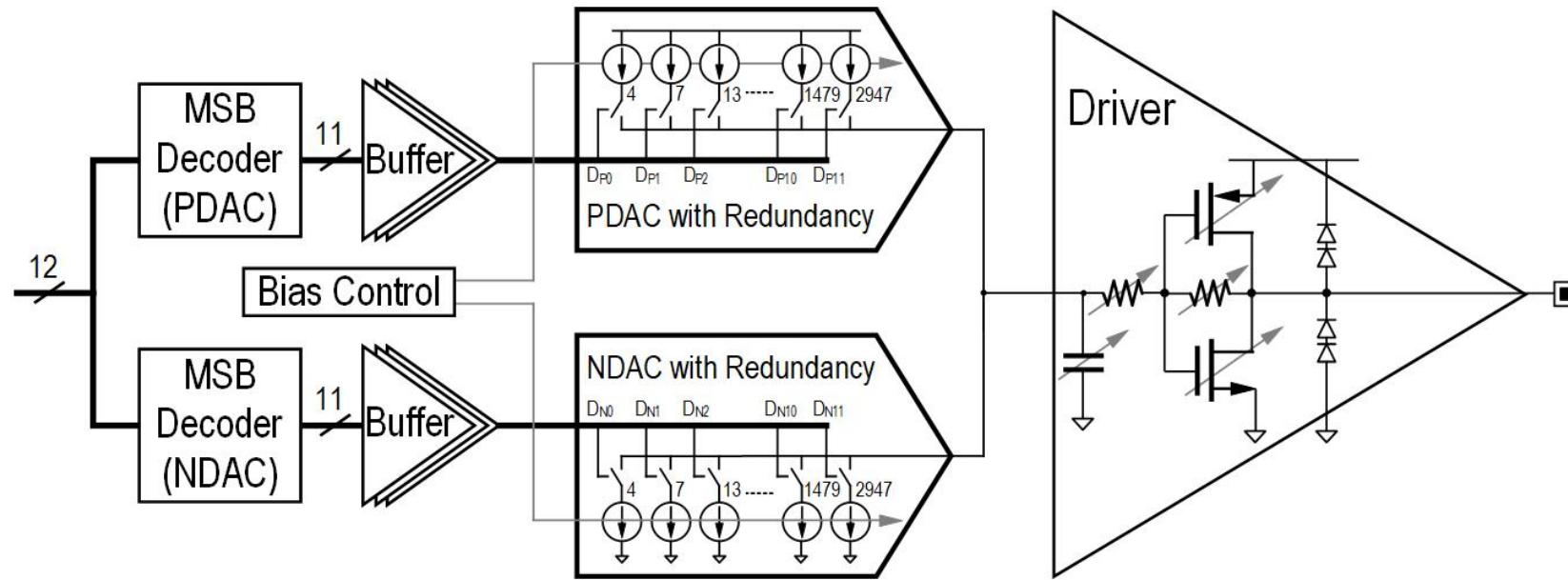
Gate Pulsing: System Block Diagram



- Driver outputs are connected to open-circuit qubit gates
- External bias-T to combine external DC bias with AC pulses
- 22 DACs to support up to 7-qubit chip
- DAC clocked at pulse start and stop time only to save power
- 22 DACs pulse simultaneously to cancel crosstalk



Gate Pulsing: Analog/RF Design



- 11-bit nMOS + pMOS class-B current DACs → support positive/negative pulses and save power in idle mode
- Redundancy with <2 radix to save area
- LUT to map the linear 11-bit ideal code to the 12-bit raw DAC code
- Tunable driver with 50Ω output impedance to absorb reflections from open-circuit qubit gates

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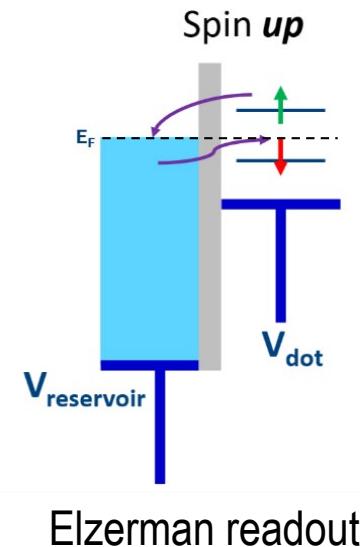
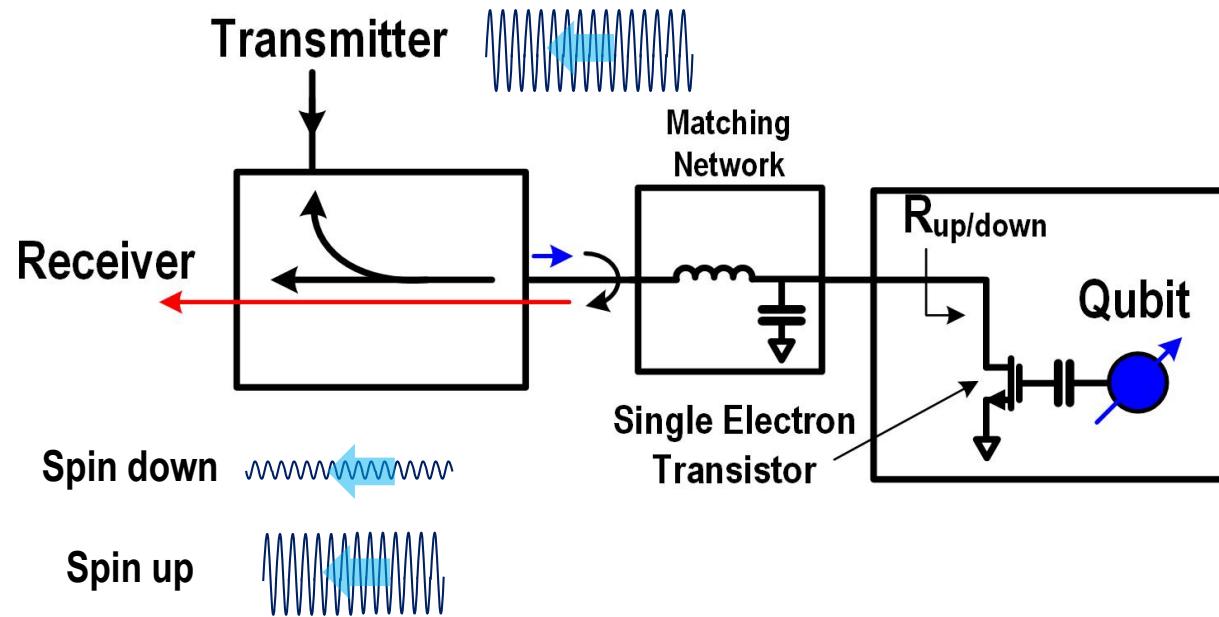
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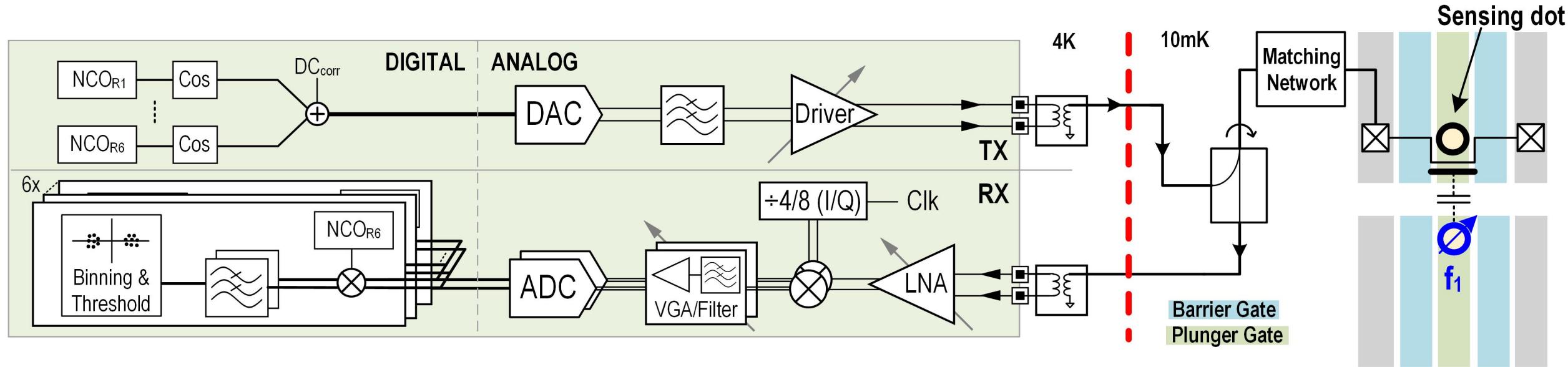
Qubit Readout: System Specifications



- RF reflectometry with directional coupler, matching network, and SET
- Qubit is capacitively coupled to the gate of SET → channel impedance is modulated depending on qubit state → reflected signal is monitored.

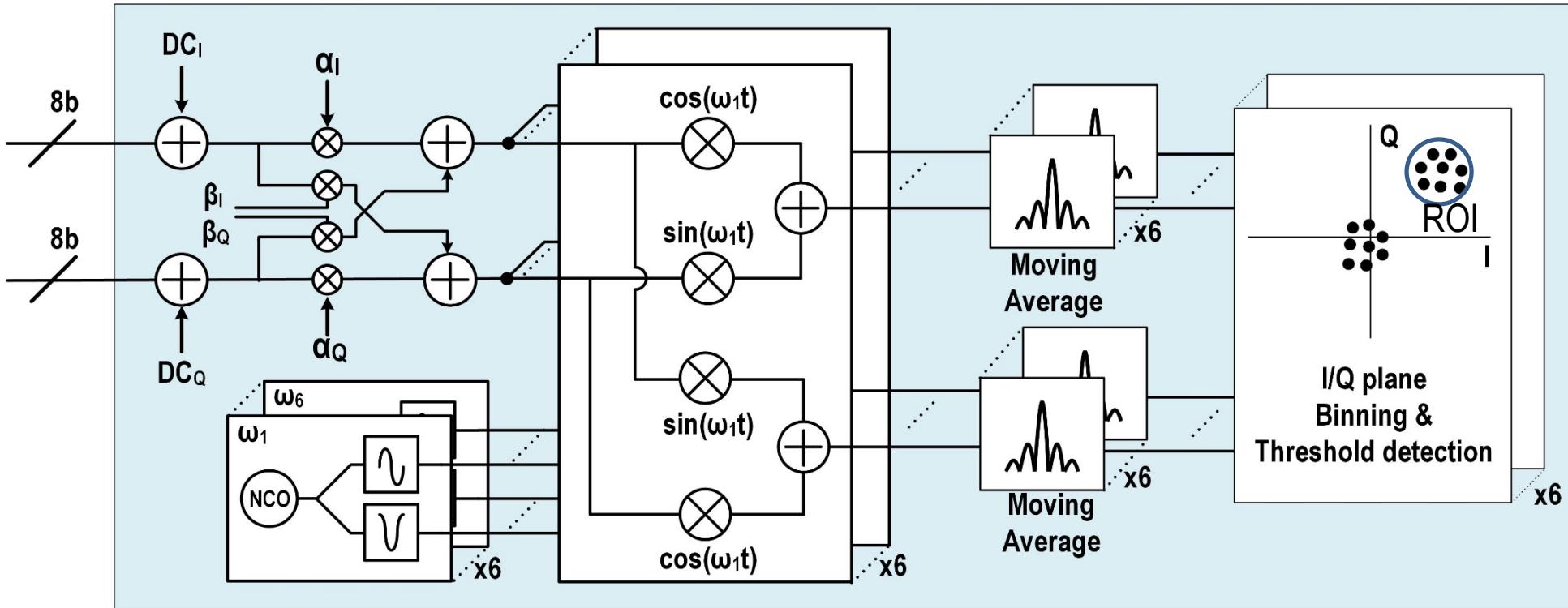
| | |
|--------------------|----------------------------|
| RF Frequency | 200-to-600MHz |
| TX Power Min./max. | -100/-70 dBm at the sample |
| Thermal noise | 100mK at the sample |
| Pulse duration | 100ns to 1ms |
| RX Gain | >90dB |
| TX/RX Isolation | >50dB |

Qubit Readout: System Block Diagram



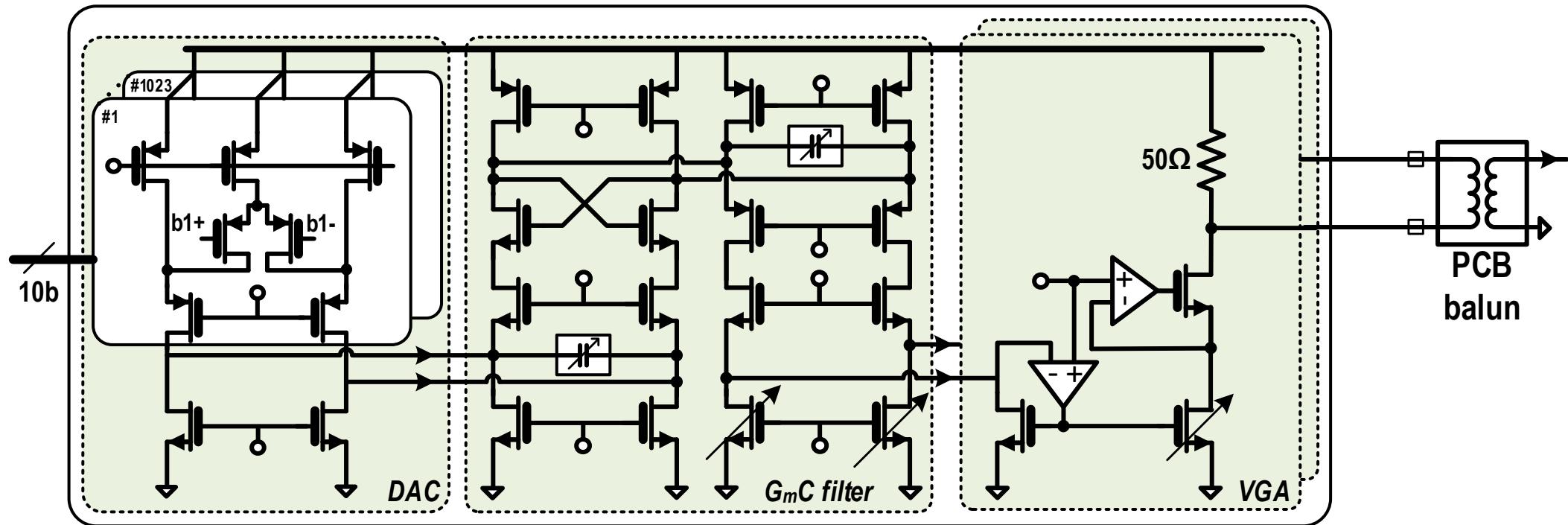
- Direct digital-to-RF Tx to avoid up-conversion mixer spurious tones and LO leakage
- RX I/Q mixer to partition the 90dB gain between RF and baseband and prevent instability
- Rx LO generated by integer division of system clock to suppress spurs by AC coupling and low-pass filtering
- The constant phase relation among TX digital, RX demodulator, and I/Q LO
- Support up to 6 simultaneous qubit-state readout.

Qubit Readout: Digital Design



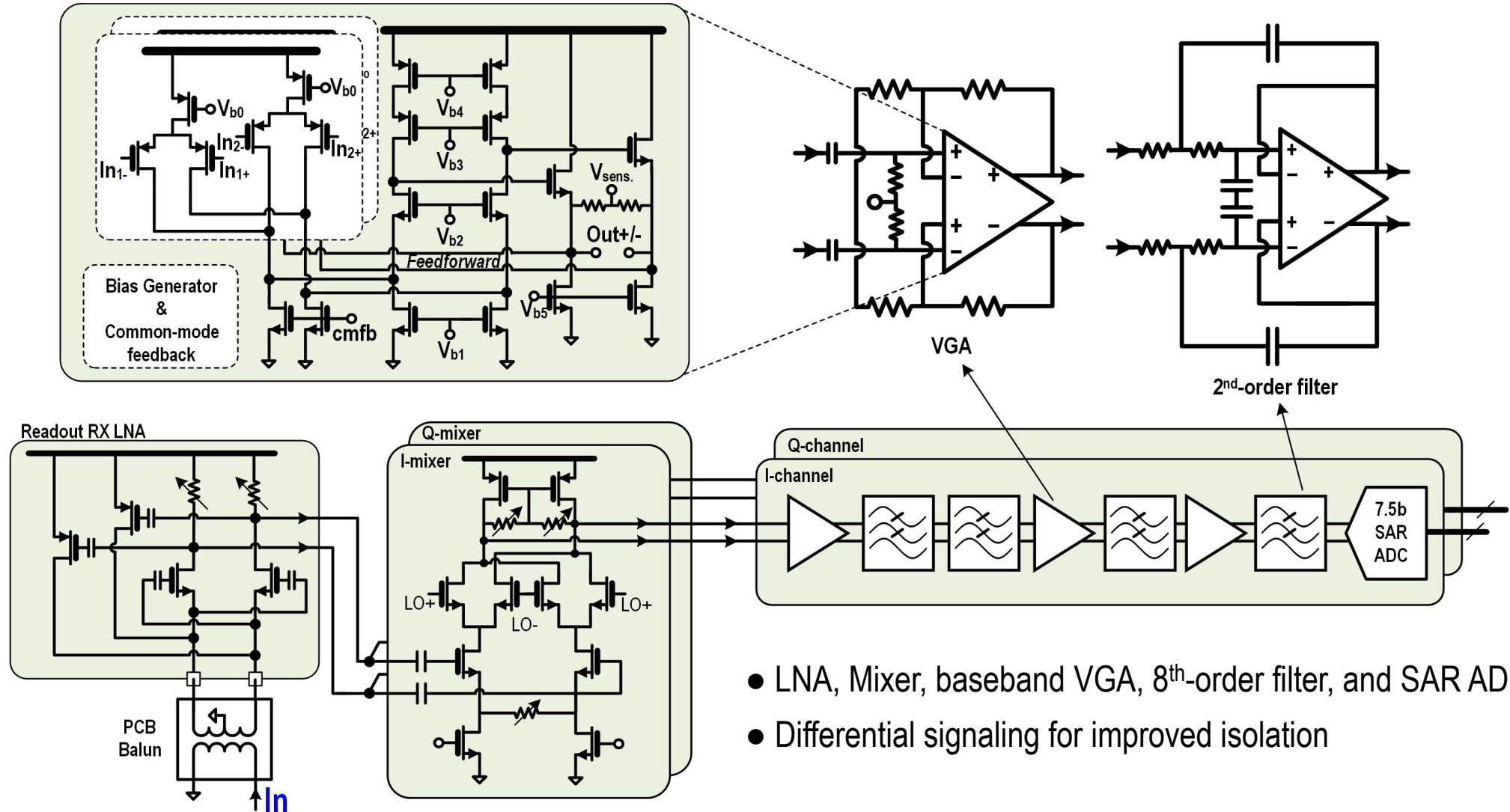
- Each tone down converted to DC and filtered to suppress adjacent tones and noise
- On-chip qubit-state detection by I/Q plane binning and thresholding
 - Minimize memory size, data transfer, and allow for low-latency qubit state detection
 - Essential for branching algorithm

Qubit Readout TX: Analog/RF Design



- 10-bit 2.5GS/s current steering DAC
- 2nd order gmC current-mode reconstruction filter
- Programmable attenuator (VGA) for -70dBm to -40dBm output power (additional external 20-30dB attenuator used)

Qubit Readout Rx: Analog/RF Design



- LNA, Mixer, baseband VGA, 8th-order filter, and SAR ADC
- Differential signaling for improved isolation

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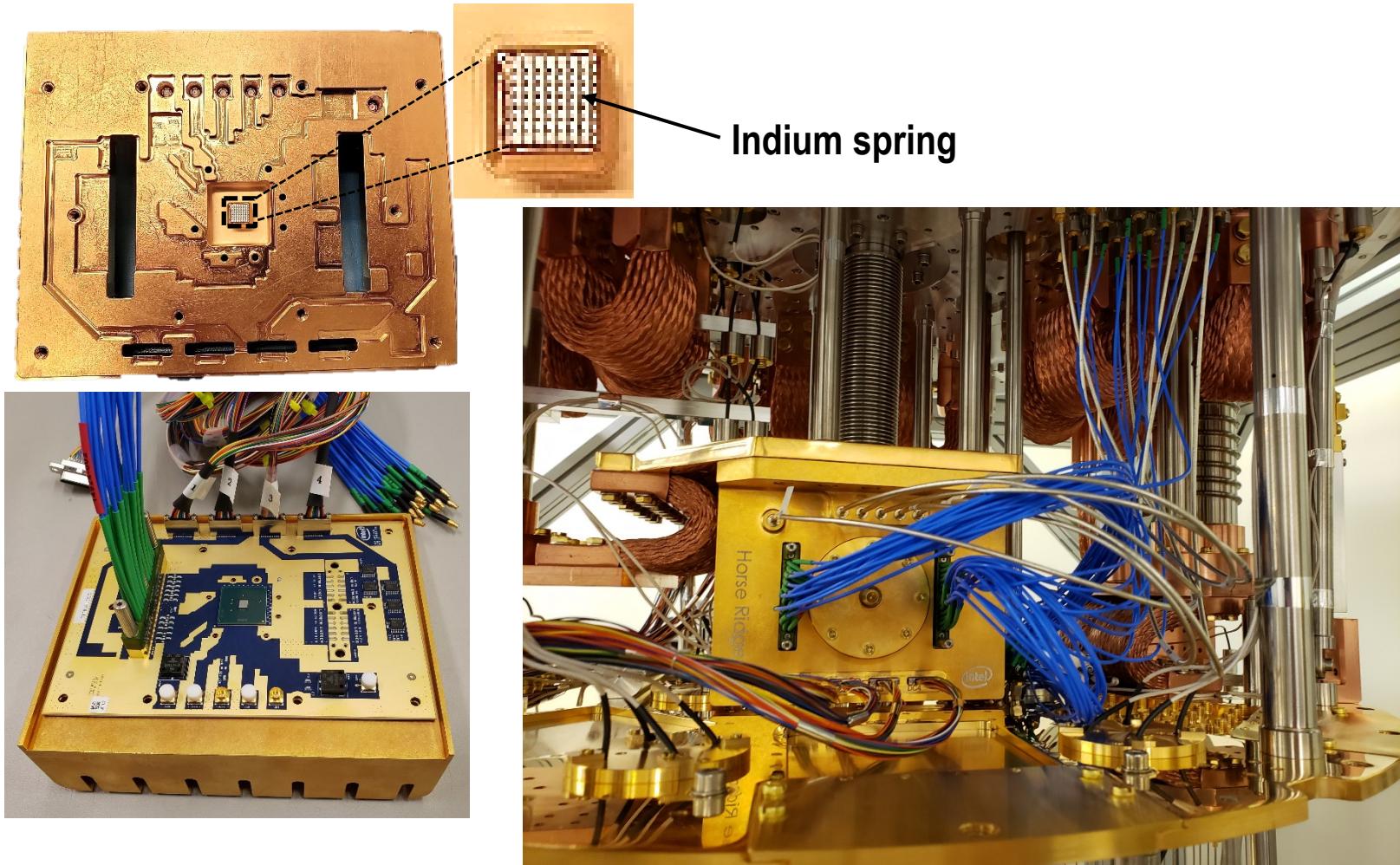
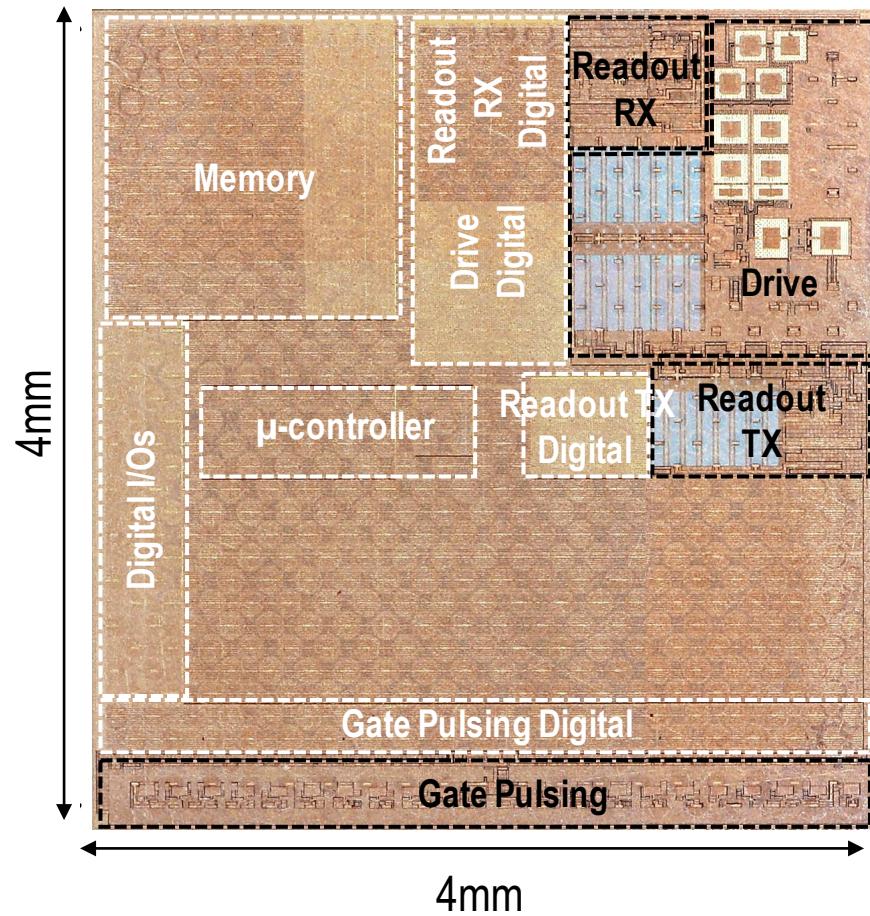
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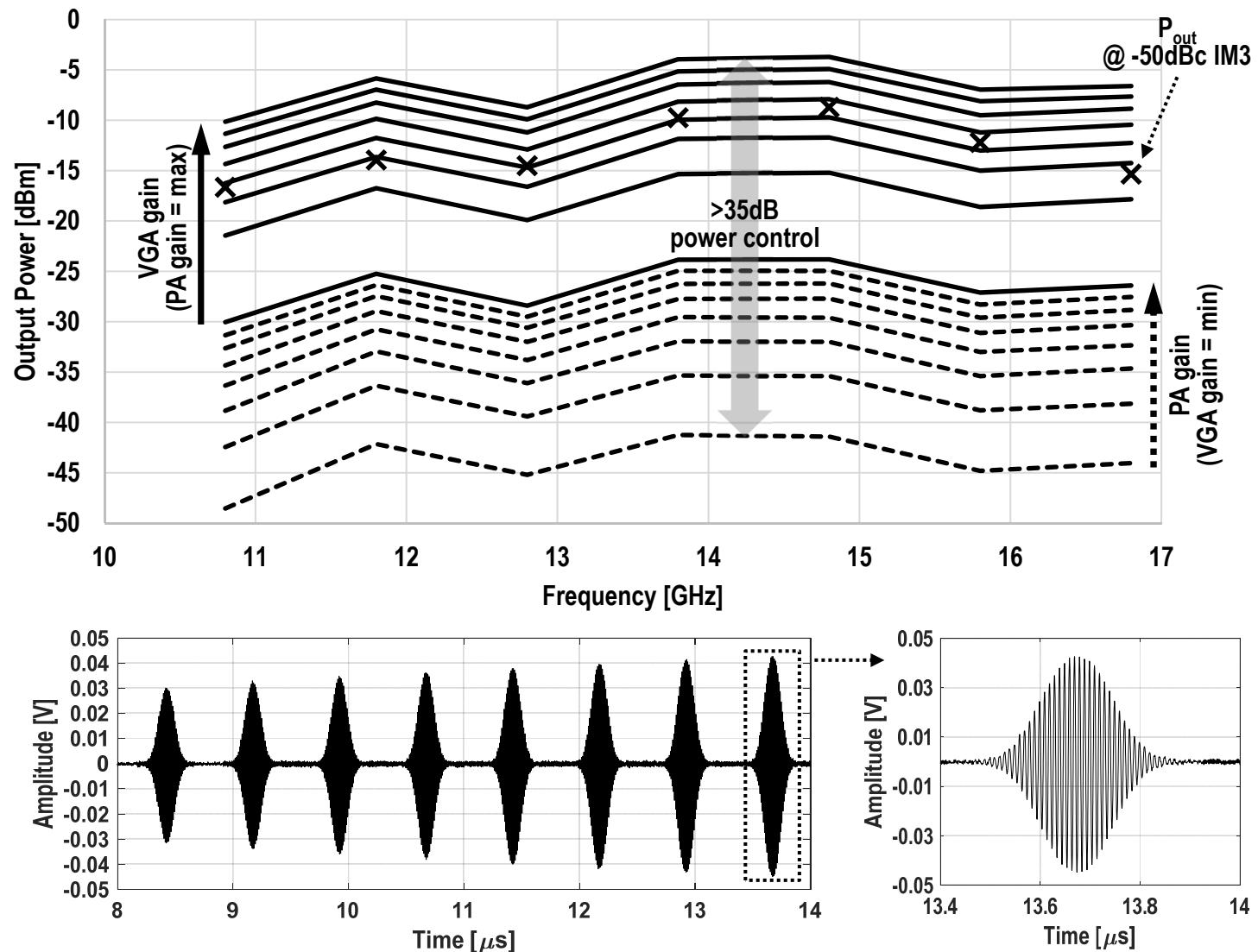
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SoC Photo and Cryogenic Measurement Setup



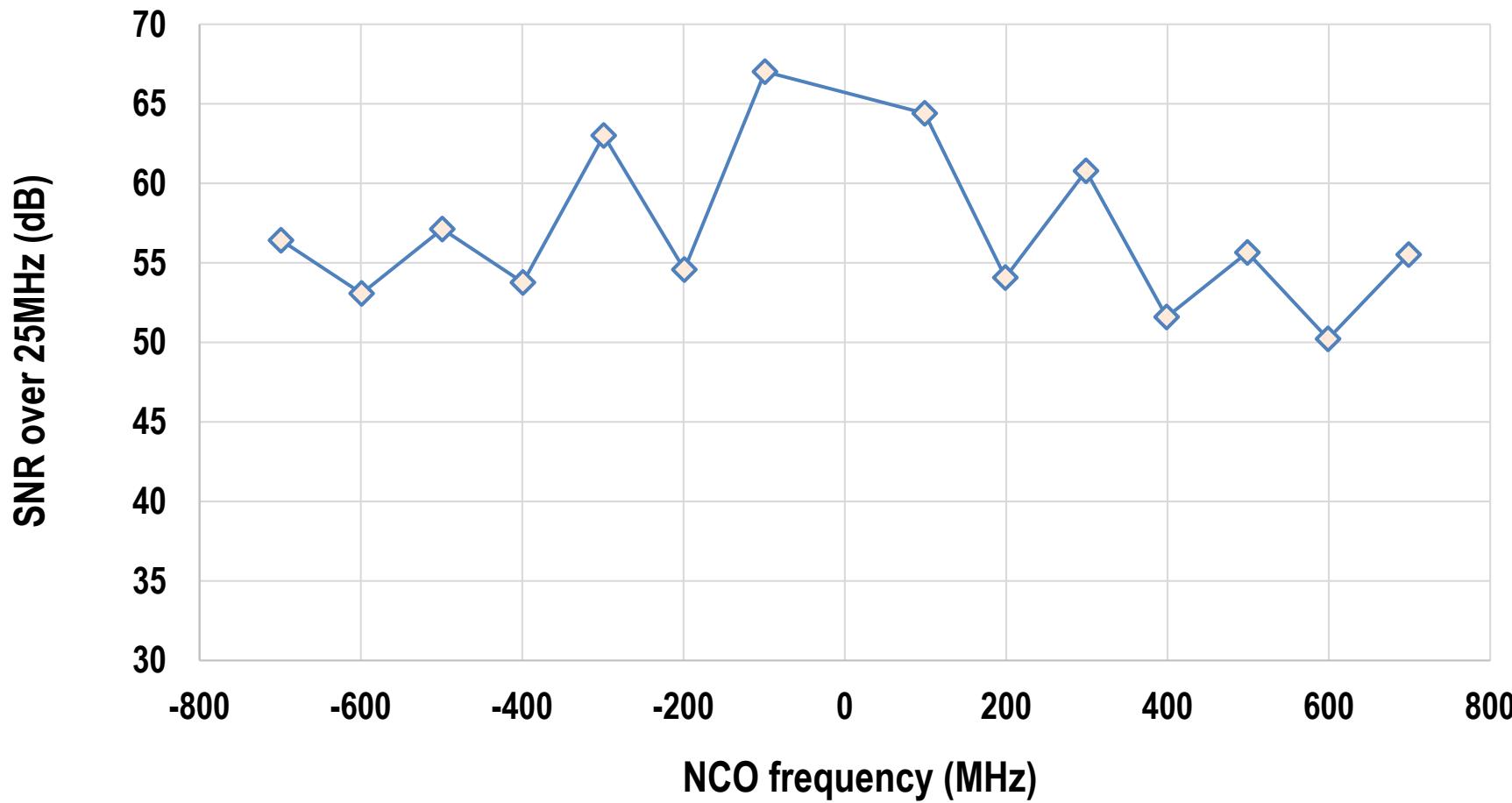
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Qubit Drive



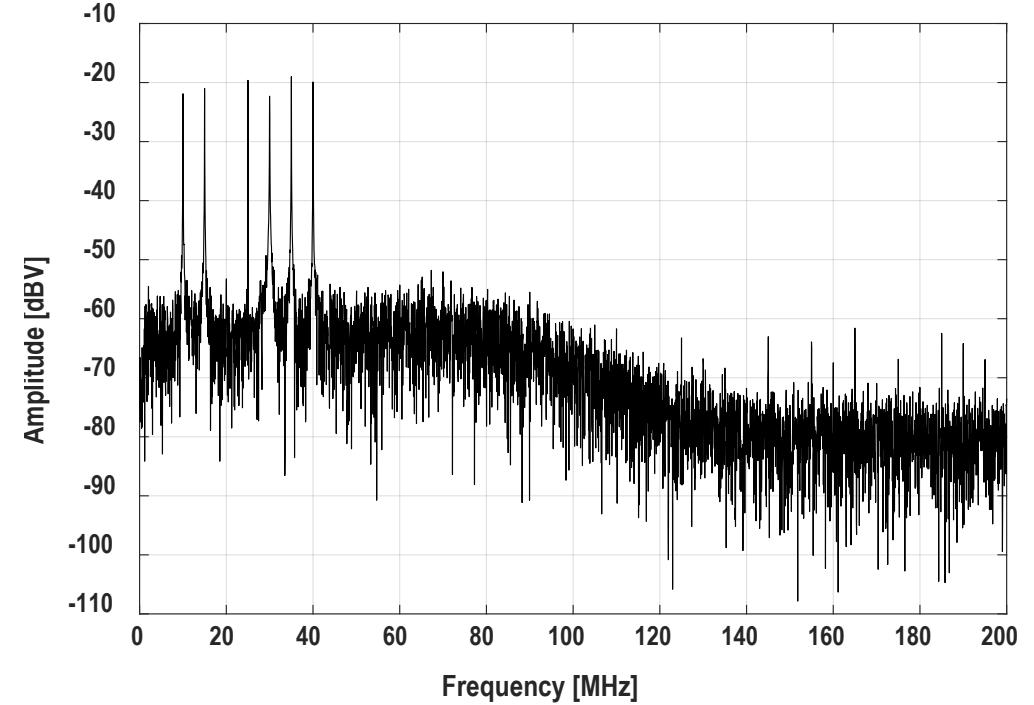
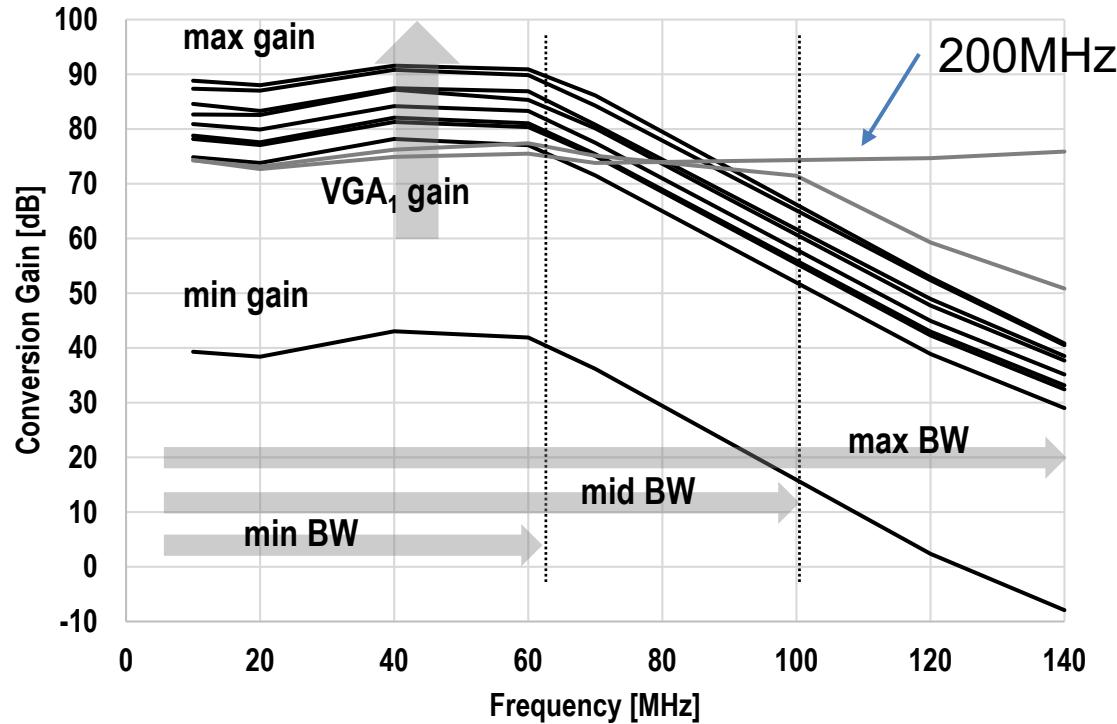
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Drive Signal SNR



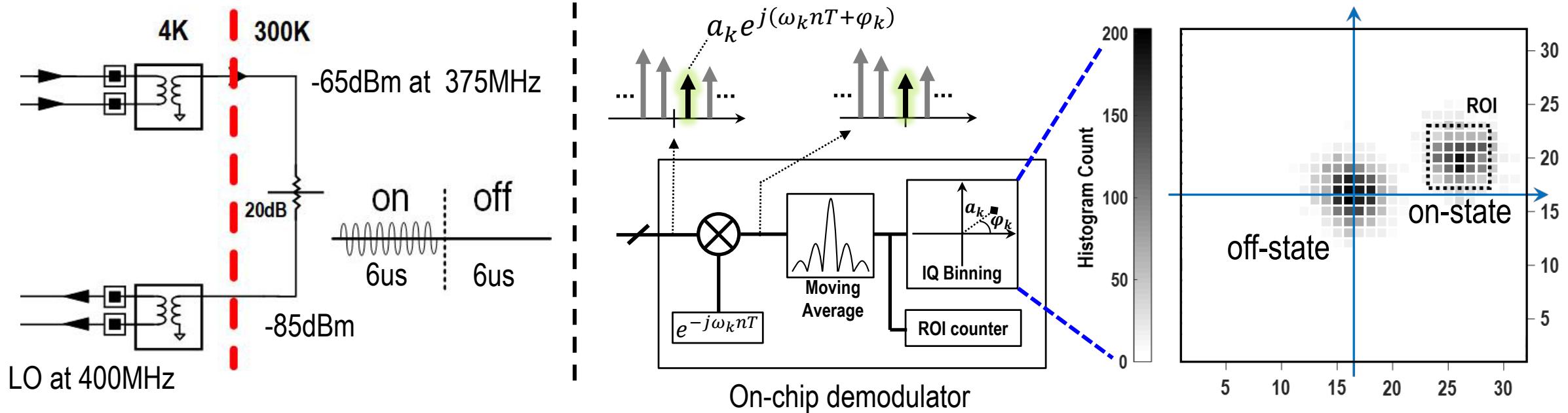
SNR over 25MHz > 50dB for a target fidelity of 99.99%

Qubit Readout RX



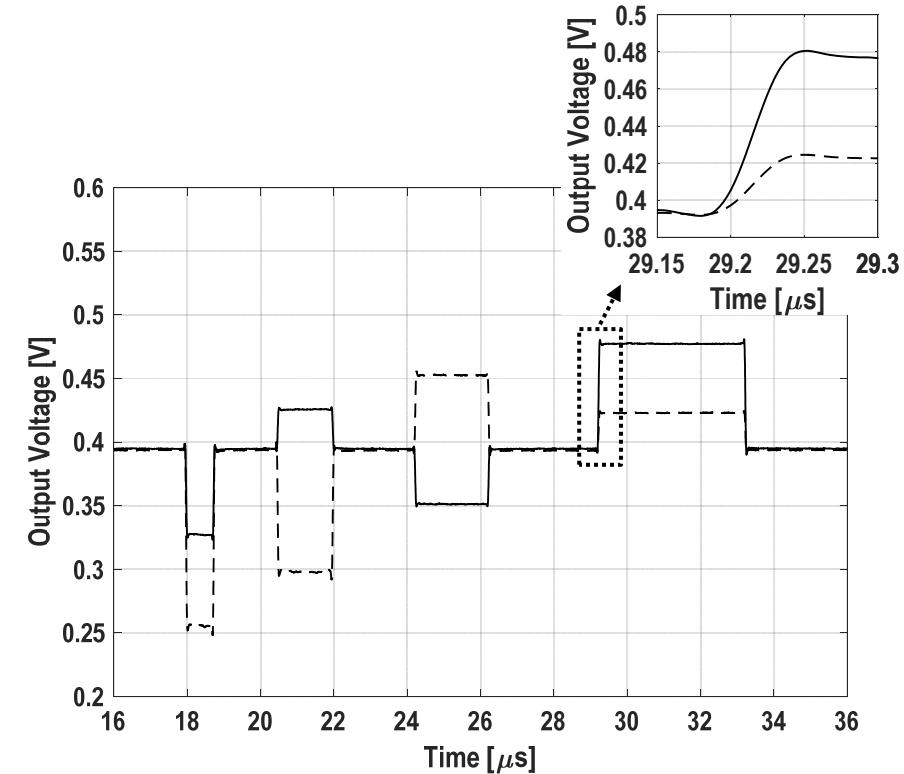
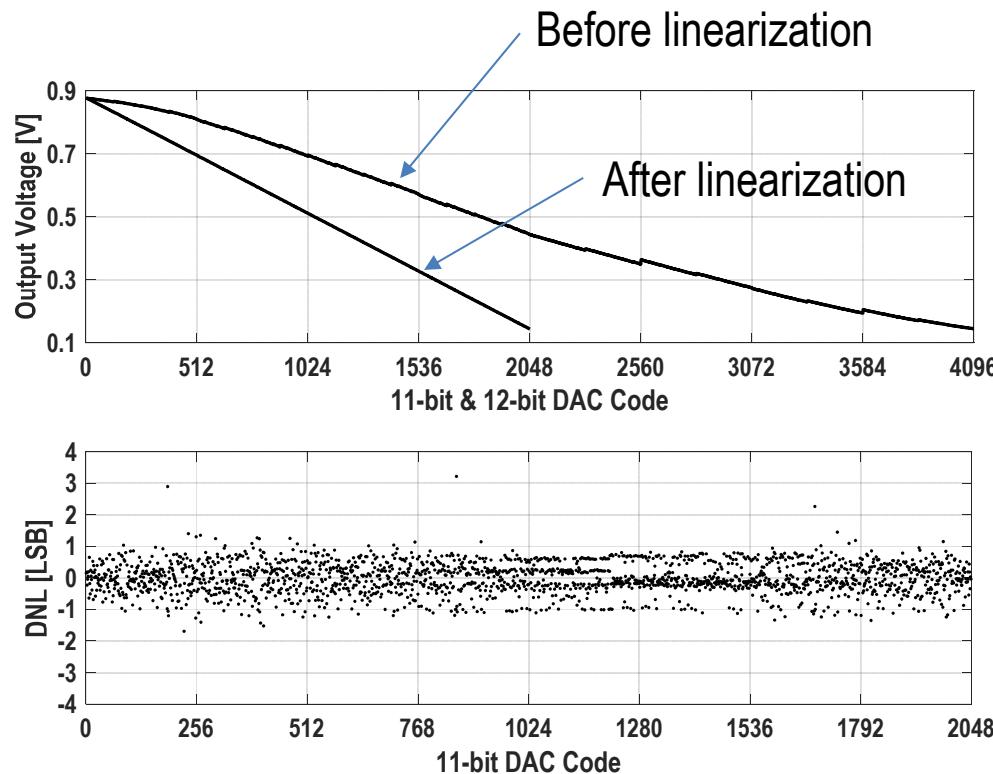
44K overall receiver noise temperature
(NF~0.6dB when referred to 300K)

Qubit Readout Loop-Back Experiment



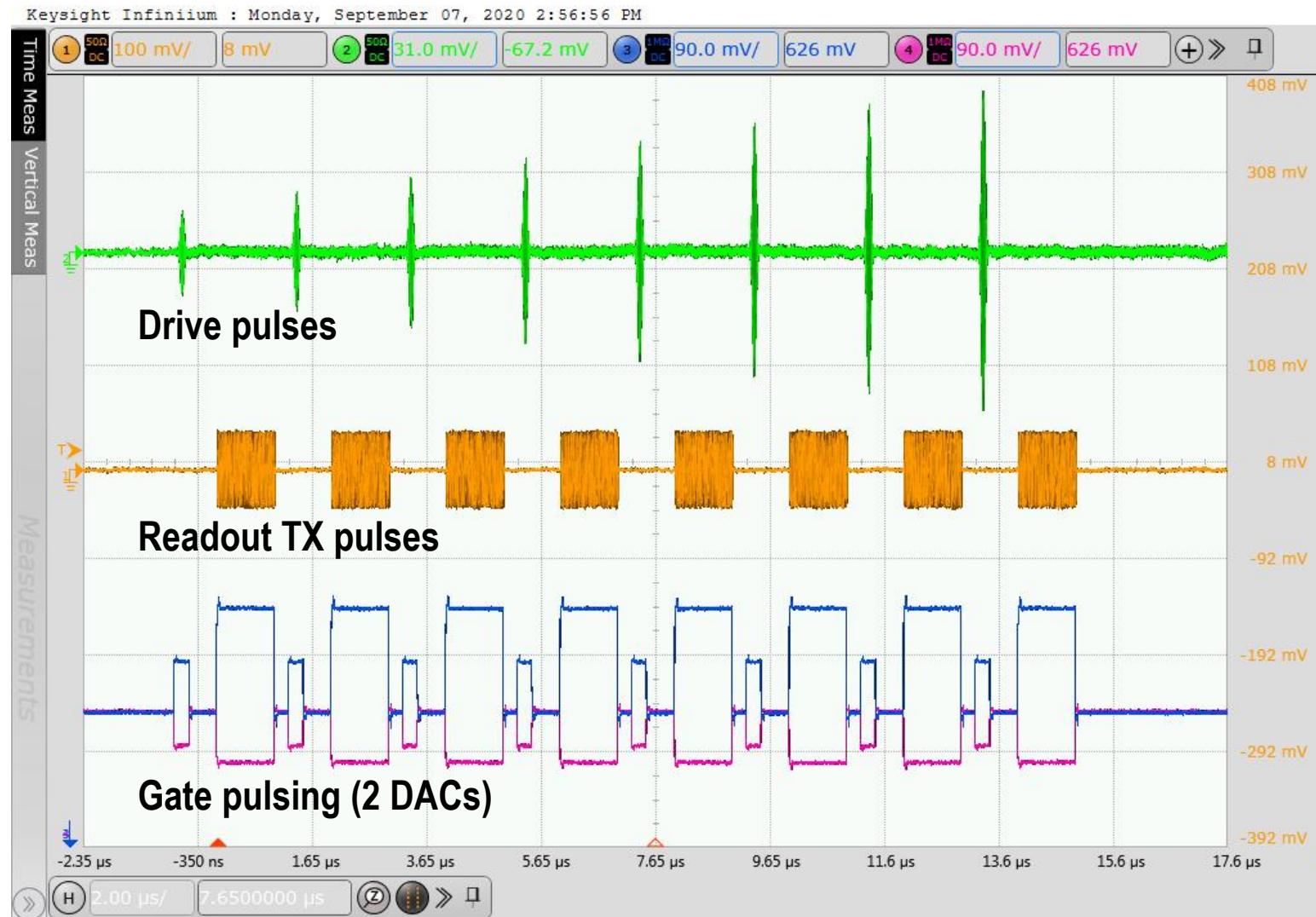
- Tx loopback to Rx with 20dB attenuation
- The receiver successfully demodulates two different states in I/Q plane
- Measured Tx/Rx isolation > 80dB

Gate Pulsing



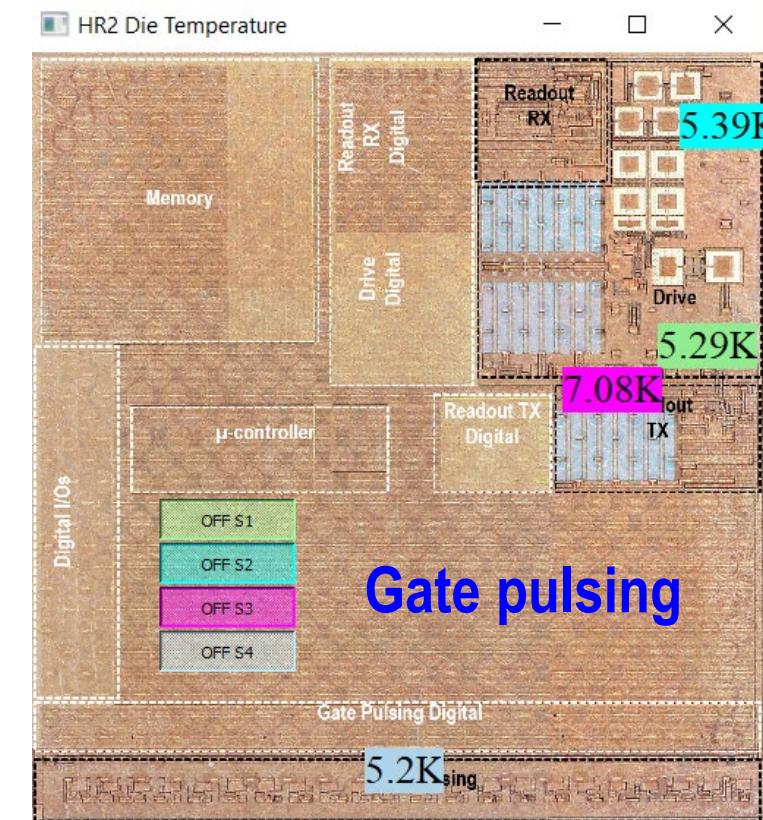
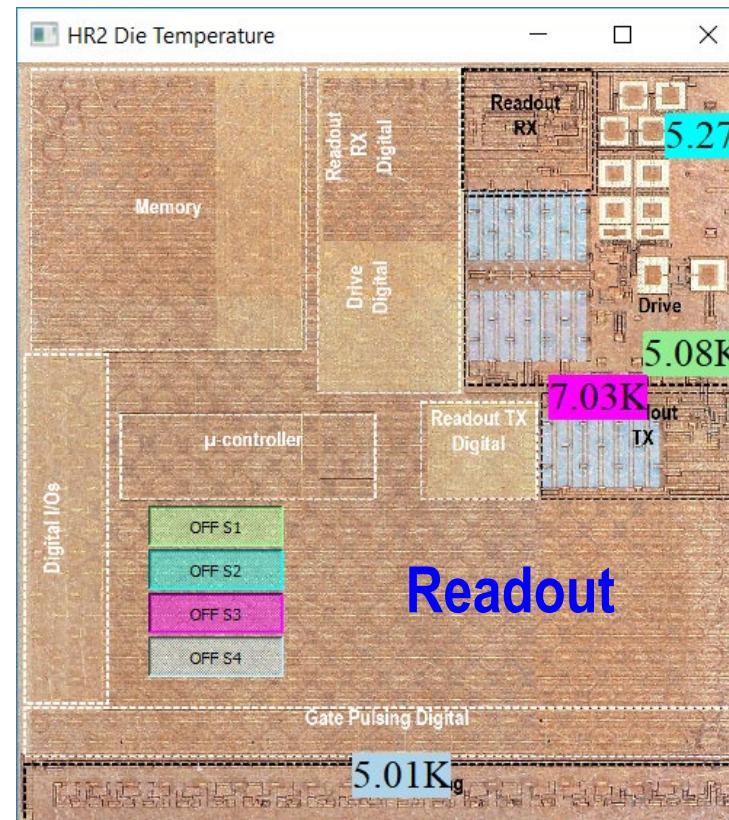
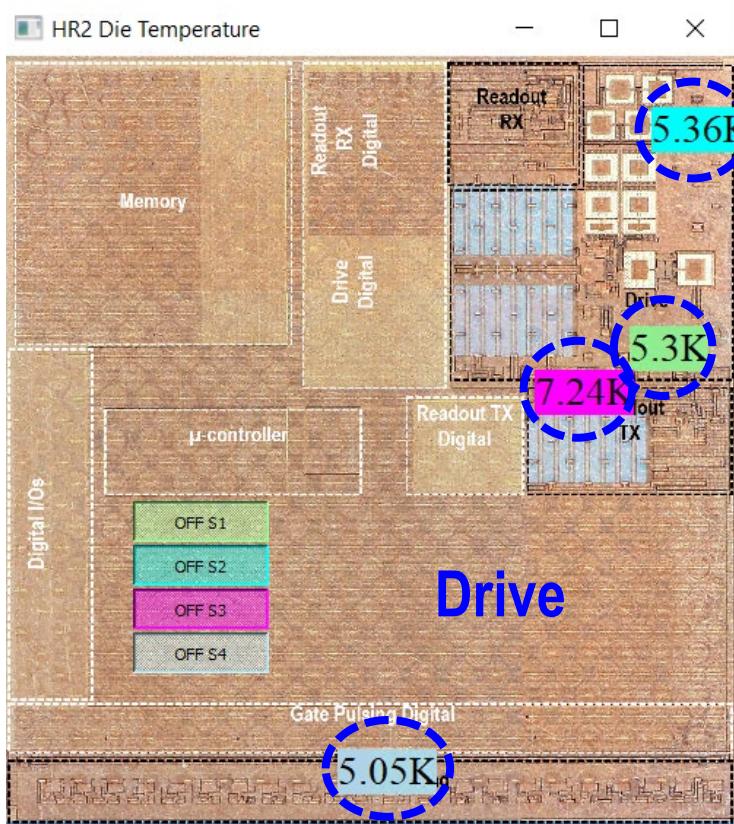
- LUT-based linearization → 12-bit input code is mapped to 11-bit code with the output voltage range from -0.4V to 0.4V
- The output integrated noise $\approx 200\mu\text{V}_{\text{rms}} < \text{LSB}$ ($390\mu\text{V}$)

Rabi Oscillation Signaling Experiment



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On-Die Temperature Sensing



- 4 temperature sensors at analog/RF blocks
- Inject reference current and measure diode voltage for temperature sensing
- Silicon temperature < 8 K with the base temperature of 3K.

Performance Summary and Comparison

| | | This Work | [B. Patra, 2020 ISSCC] | [J. Bardin, 2019 ISSCC] |
|------------------------------|---------|--|--------------------------------------|---------------------------|
| Qubit platform | | Spin qubits | Transmons + spin qubits | Transmons |
| Controller capability | | Drive, Readout with Digital Detector, Gate Pulsing, μ-Controller | Drive | Drive |
| Power | Analog | Drive: 5.2mW/qubit ^a Readout TX/RX: 1.3/9.3mW/qubit Gate pulsing: 2.9mW/channel | 1.7mW/qubit | <2mW/qubit |
| | Digital | 10 – 140mW ^b @ 1.6GHz clock | Digital: 330mW @ 1GHz clock | N/A |
| Chip area | | 16mm ² | 4mm ² | 1.6mm ² |
| Technology | | 22nm FinFET CMOS | 22nm FinFET CMOS | 28nm bulk CMOS |
| Drive | | | | |
| Freq. range | | 11 – 17GHz @ >-10dBm | 2 – 20GHz @ >-45dBm | 4 – 8GHz |
| Freq. multiplexing | | Yes, 16 qubits | Yes, 32 qubits | No |
| Sampling rate | | up to 2.5GS/s | 1GS/s | 1GS/s |
| IM3 | | <-50dBc @ >-17dBm (11 to 17GHz) | <-50dBc @ -18dBm (6.25GHz) | N/A |
| Data bandwidth | | up to 2GHz | 1GHz | 400MHz |
| Digital FIR | | Yes, 2 notches per qubit | No | No |
| Envelope size | | 16,384 points AWG ^c | Up to 40,960 points AWG ^d | Fixed 22 points symmetric |
| Instruction set | | 2 ¹⁹ codewords per qubit | 2 ³ codewords per qubit | 2 ⁴ codewords |
| Output impedance | | 50Ω | N/A | N/A |
| LO IQ generation | | Integrated on-chip hybrid | External off-chip hybrid (PCB) | External off-chip hybrid |

| This Work – Readout | | This Work – Gate Pulsing | |
|---|------------------------|-------------------------------|----------------------|
| Freq. multiplexing | Yes, 6 qubits | # Channels | 22 (simultaneous) |
| TX output freq. | DC – 0.6GHz | Amplitude range | ±0.4V ^f |
| TX output power | -70 to -40dBm | Amplitude res. | 11 bits |
| RX RF freq. | 200 – 600MHz | Pulse width | 10ns – 2.6ms |
| RX gain | 40 – 90dB | Pulse width resolution | 2.5ns |
| RX noise temperature^e | 44K | Rise/fall time | ~50ns ^g |
| RX baseband BW | 60 – 200MHz | Output rms noise | 200μV _{rms} |
| Filter order | 8 th | Output impedance | 50Ω |
| ADC | SAR, 7.5 bits, 400MS/s | | |
| Qubit state detector | Integrated | | |

^aFor max P_{out}

^bDepending on activity

^cPer codeword, per qubit

^dShared for 8 codewords and 16 qubits

^eIntegrated over 60MHz BW

^fAround DC output voltage

^gWith 14pF load

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| Power | Analog | Drive: 5.2mW/qubit ^a Readout TX/RX: 1.3/9.3mW/qubit Gate pulsing: 2.9mW/channel | 1.7mW/qubit | <2mW/qubit |
| | Digital | 10 – 140mW ^b @ 1.6GHz clock | Digital: 330mW @ 1GHz clock | N/A |
| Chip area | | 16mm ² | 4mm ² | 1.6mm ² |
| Technology | | 22nm FinFET CMOS | 22nm FinFET CMOS | 28nm bulk CMOS |
| Drive | | | | |
| Freq. range | | 11 – 17GHz @ >-10dBm | 2 – 20GHz @ >-45dBm | 4 – 8GHz |
| Freq. multiplexing | | Yes, 16 qubits | Yes, 32 qubits | No |
| Sampling rate | | up to 2.5GS/s | 1GS/s | 1GS/s |
| IM3 | | <-50dBc @ >-17dBm (11 to 17GHz) | <-50dBc @ -18dBm (6.25GHz) | N/A |
| Data bandwidth | | up to 2GHz | 1GHz | 400MHz |
| Digital FIR | | Yes, 2 notches per qubit | No | No |
| Envelope size | | 16,384 points AWG ^c | Up to 40,960 points AWG ^d | Fixed 22 points symmetric |
| Instruction set | | 2 ¹⁹ codewords per qubit | 2 ³ codewords per qubit | 2 ⁴ codewords |
| Output impedance | | 50Ω | N/A | N/A |
| LO IQ generation | | Integrated on-chip hybrid | External off-chip hybrid (PCB) | External off-chip hybrid |

| This Work – Readout | | This Work – Gate Pulsing | |
|---|------------------------|-------------------------------|----------------------|
| Freq. multiplexing | Yes, 6 qubits | # Channels | 22 (simultaneous) |
| TX output freq. | DC – 0.6GHz | Amplitude range | ±0.4V ^f |
| TX output power | -70 to -40dBm | Amplitude res. | 11 bits |
| RX RF freq. | 200 – 600MHz | Pulse width | 10ns – 2.6ms |
| RX gain | 40 – 90dB | Pulse width resolution | 2.5ns |
| RX noise temperature^e | 44K | Rise/fall time | ~50ns ^g |
| RX baseband BW | 60 – 200MHz | Output rms noise | 200μV _{rms} |
| Filter order | 8 th | Output impedance | 50Ω |
| ADC | SAR, 7.5 bits, 400MS/s | | |
| Qubit state detector | Integrated | | |

^aFor max P_{out}

^bDepending on activity

^cPer codeword, per qubit

^dShared for 8 codewords and 16 qubits

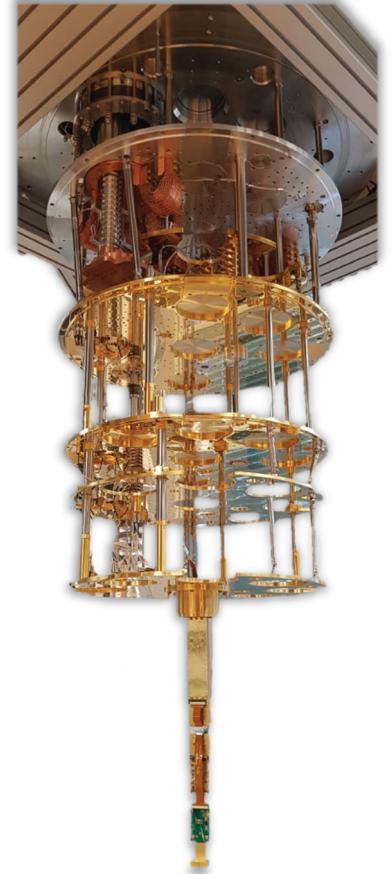
^eIntegrated over 60MHz BW

^fAround DC output voltage

^gWith 14pF load

Conclusions

- Qubit control requires high-precision RF/analog signals
- Current approach with external control electronics does not scale
- Proposed solution enables qubit drive, readout and gate-pulsing in one cryogenic SoC to replace external control electronics
- Demonstrated target performance at 4K for all 3 main functions
- Integrated quantum instruction set architecture (QISA)



This work paves the way to scalable quantum computers

Acknowledgments

The Authors would like to thank the Quantum Computing team at Intel Labs and Component Research and our collaborators at Delft University of Technology

A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

Andrea Ruffino^{*1}, Yatao Peng^{*1}, Tsung-Yeh Yang², John Michniewicz³,
Miguel Fernando Gonzalez-Zalba^{2,4}, and Edoardo Charbon¹

^{*}Equally-Credited Authors (ECAs)

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²Hitachi Cambridge Laboratory, Cambridge, United Kingdom

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⁴Quantum Motion Technologies, Leeds, United Kingdom

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Self Introduction

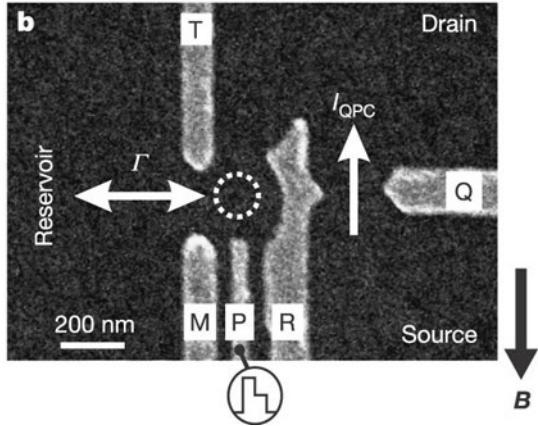
- B.Sc. degree (*cum laude*) in Engineering Physics from Politecnico di Torino in 2013
- M.Sc. triple joint degree (*cum laude*) in Micro and Nanotechnologies from Politecnico di Torino, INP Grenoble and EPFL in 2015
- Currently Ph.D. in Microelectronics at EPFL since 2016
- IEEE SSCS Predoctoral Achievement Award 2020-2021 recipient
- My interests are analog, RF integrated circuit design and cryogenic CMOS electronics for quantum computing



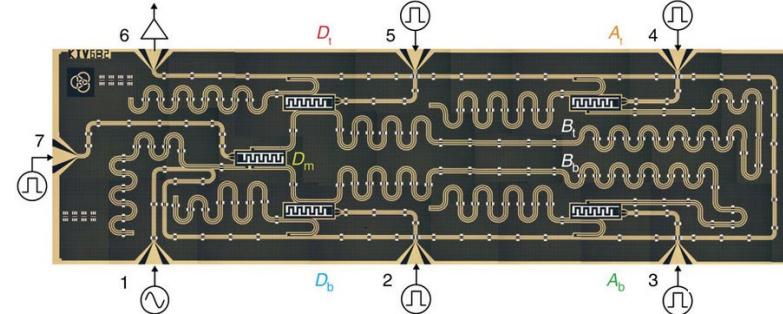
Presentation Outline

- Introduction
- System-on-Chip architecture and circuits
- Measurements
- Conclusion

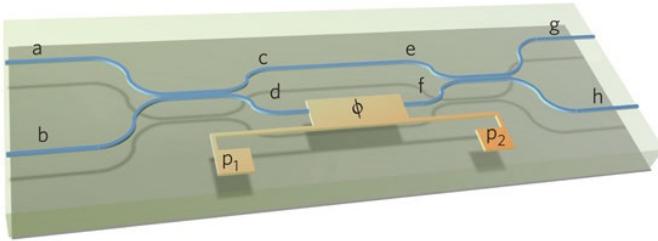
Quantum computing and qubits



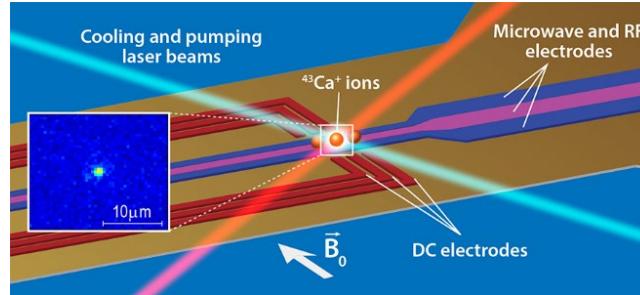
[1] Elzerman et al., Nature 430, 431-435 (2004)



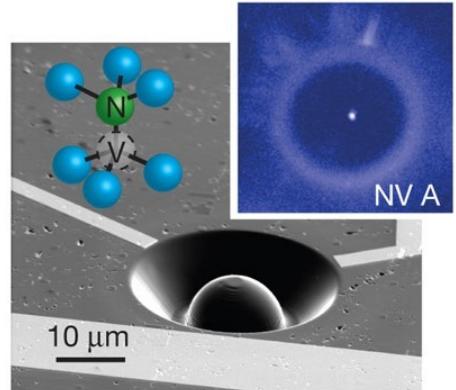
[2] Ristè et al., Nature Communications 6, 6983 (2015)



[3] Matthews et al., Nature Photonics 3, 346-350 (2009)

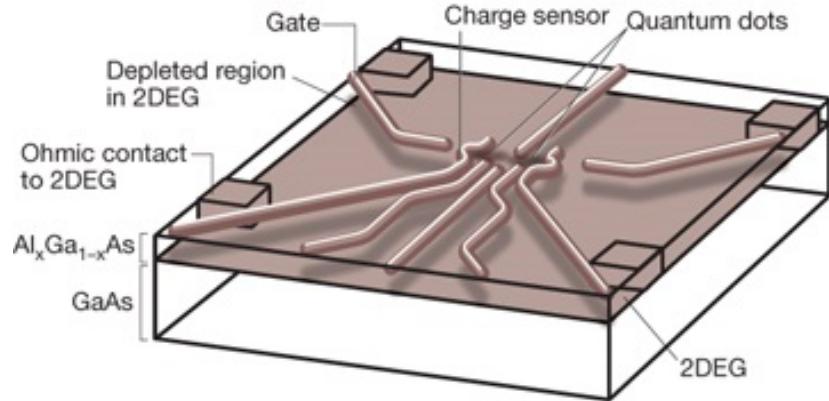


[4] Kim, Physics 7, 119 (2014)

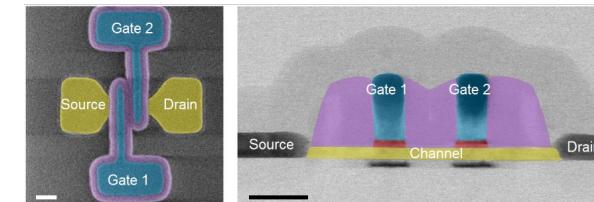
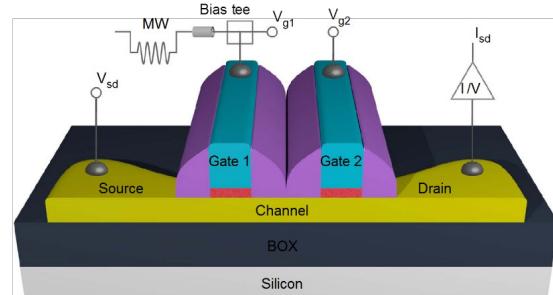


[5] Robledo et al., Nature 477, 574-578 (2011)

Silicon qubits



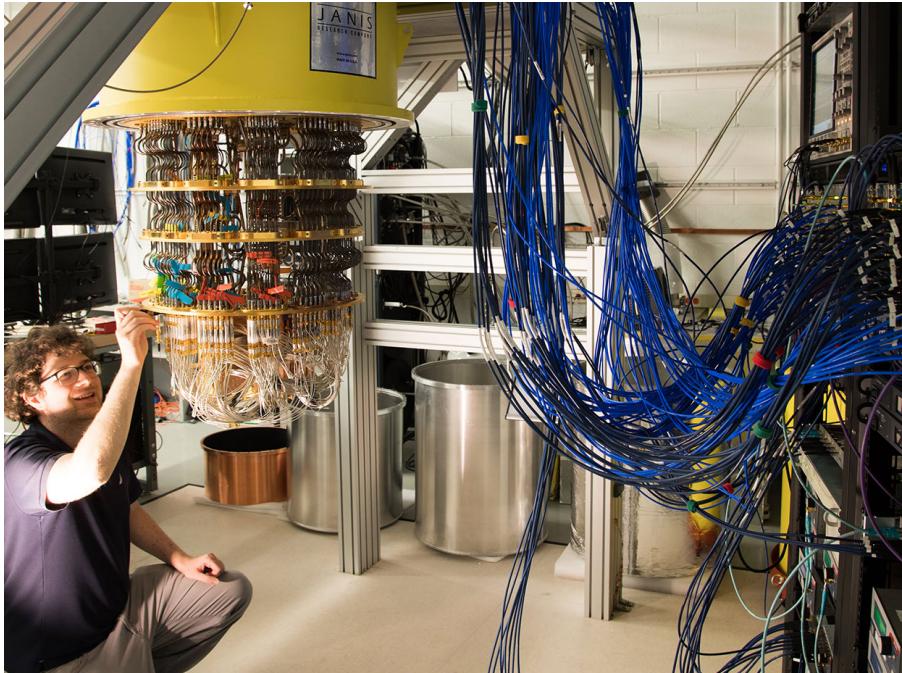
[6] Ladd et al., Nature 464, 45-53 (2010)



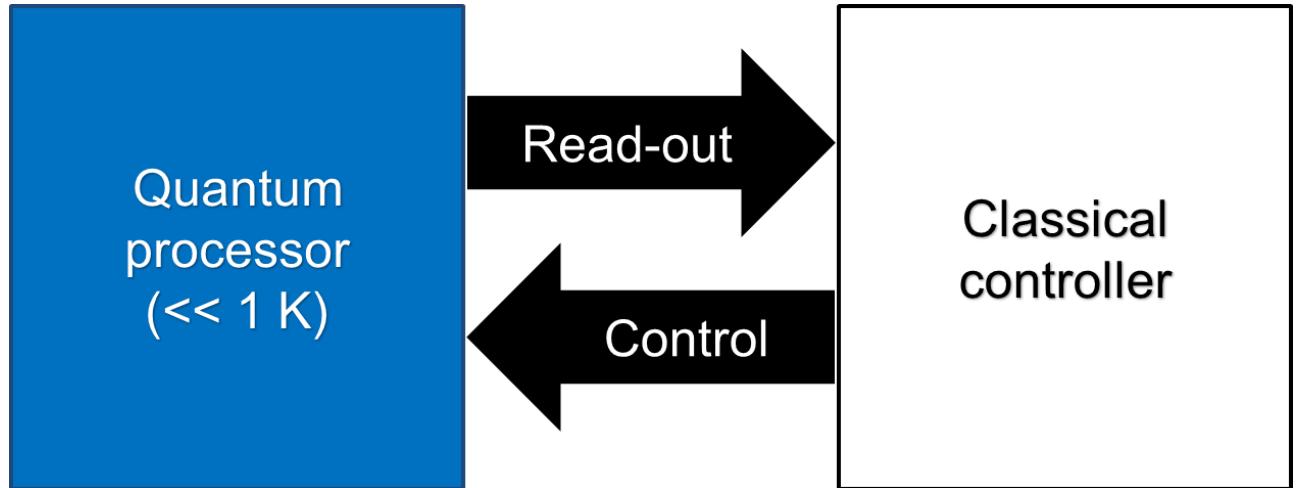
[7] Maurand et al., Nature Communications 7, 13575 (2016)

- Electrostatically defined quantum dots in a 2D electron gas
- Transistor-like structures

Interfacing qubits

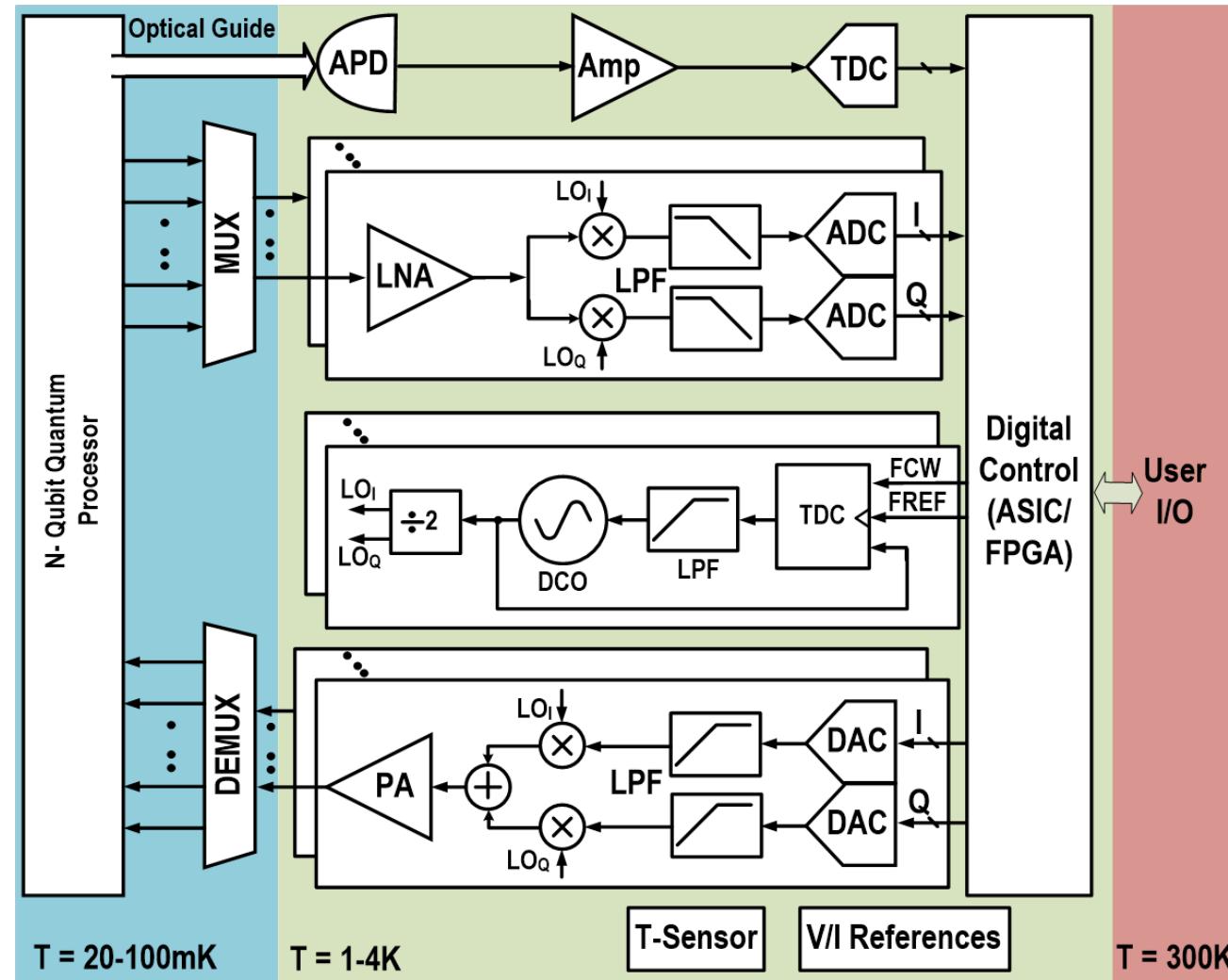


[8] Bardin et al., ISSCC 2019



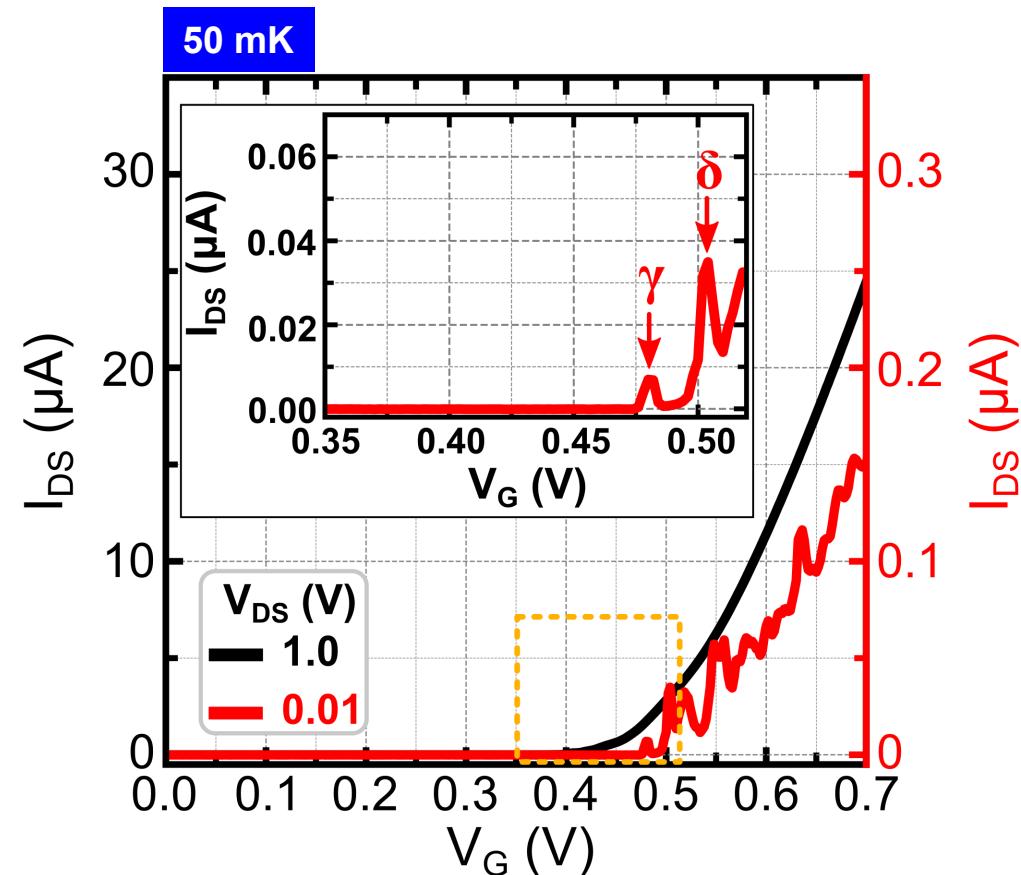
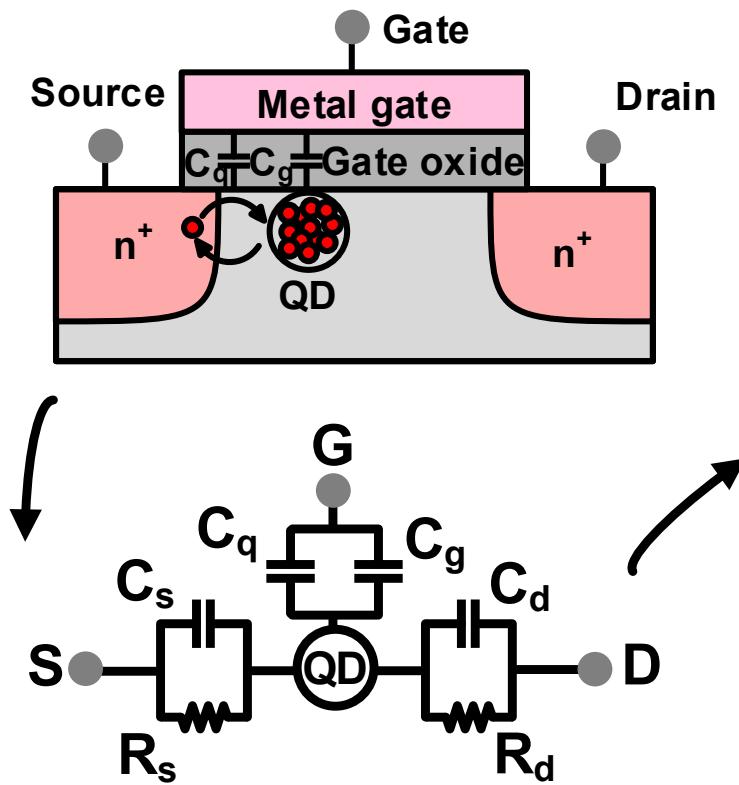
- Minimized wiring
- (Co-)integration for millions of qubits

Cryo-CMOS electronics



[9] Charbon et al., ISSCC 2017

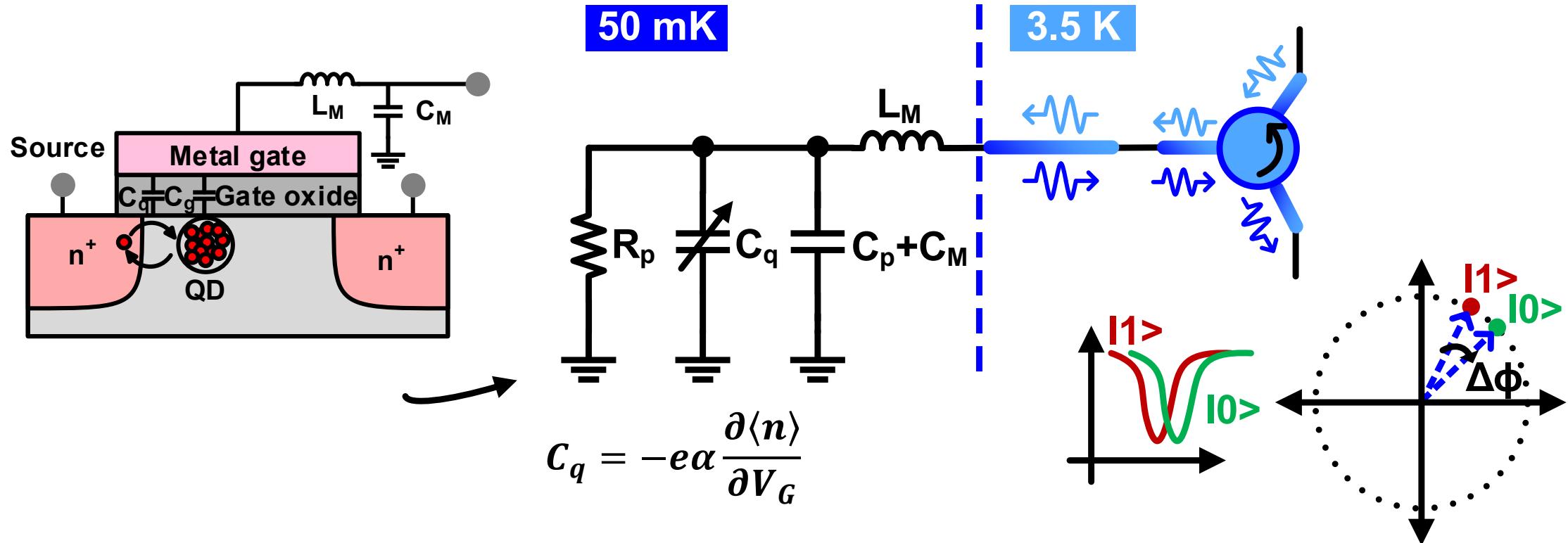
CMOS quantum dots



[10] Yang et al., EDL 2020

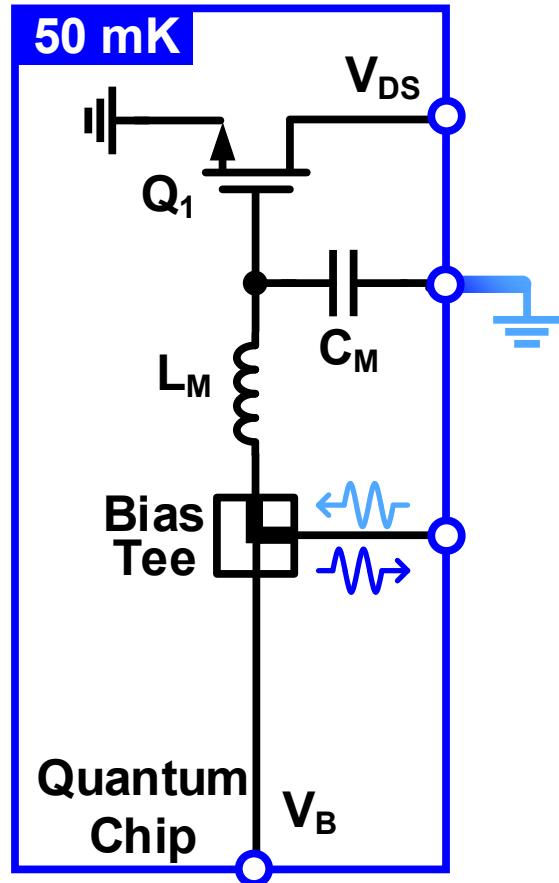
- At 50 mK, CMOS transistors create few electron quantum dots

Gate-based reflectometry readout



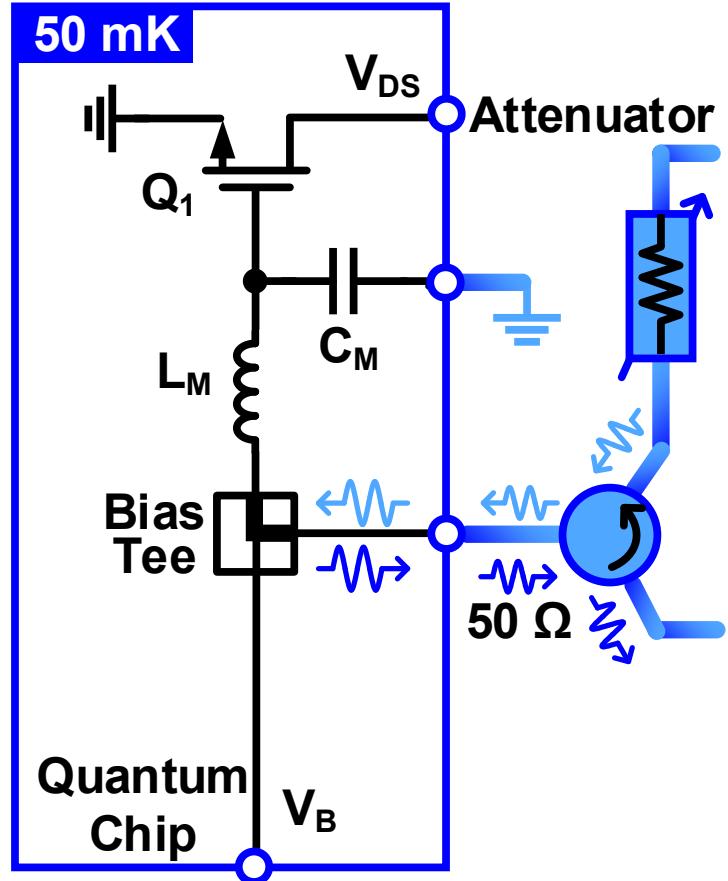
- Gate-based reflectometry reads the dispersive phase shift of the quantum state

Cryogenic CMOS platform



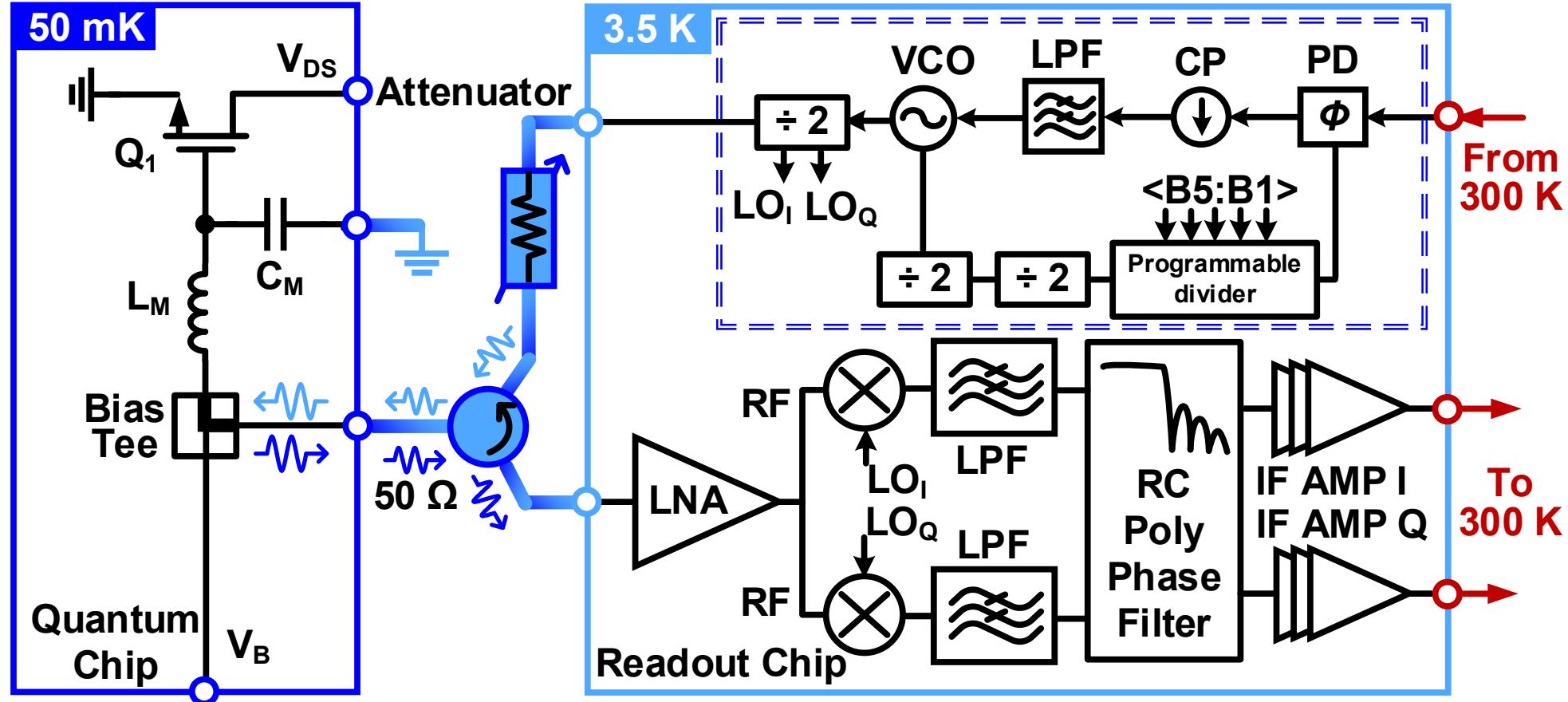
13.2: A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

Cryogenic CMOS platform

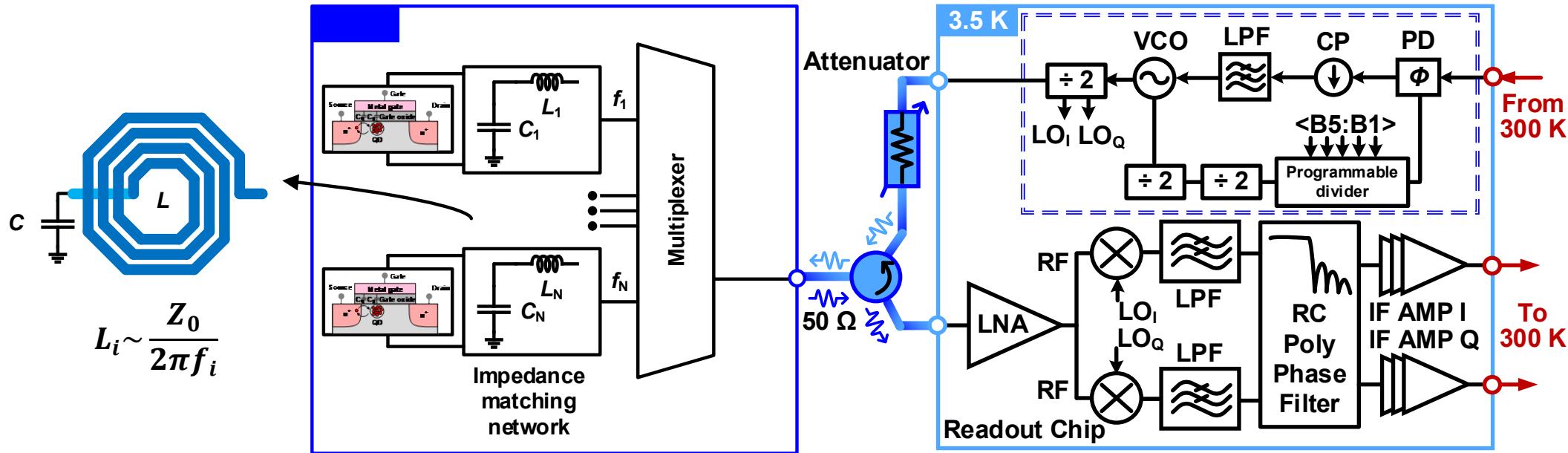


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Cryogenic CMOS platform



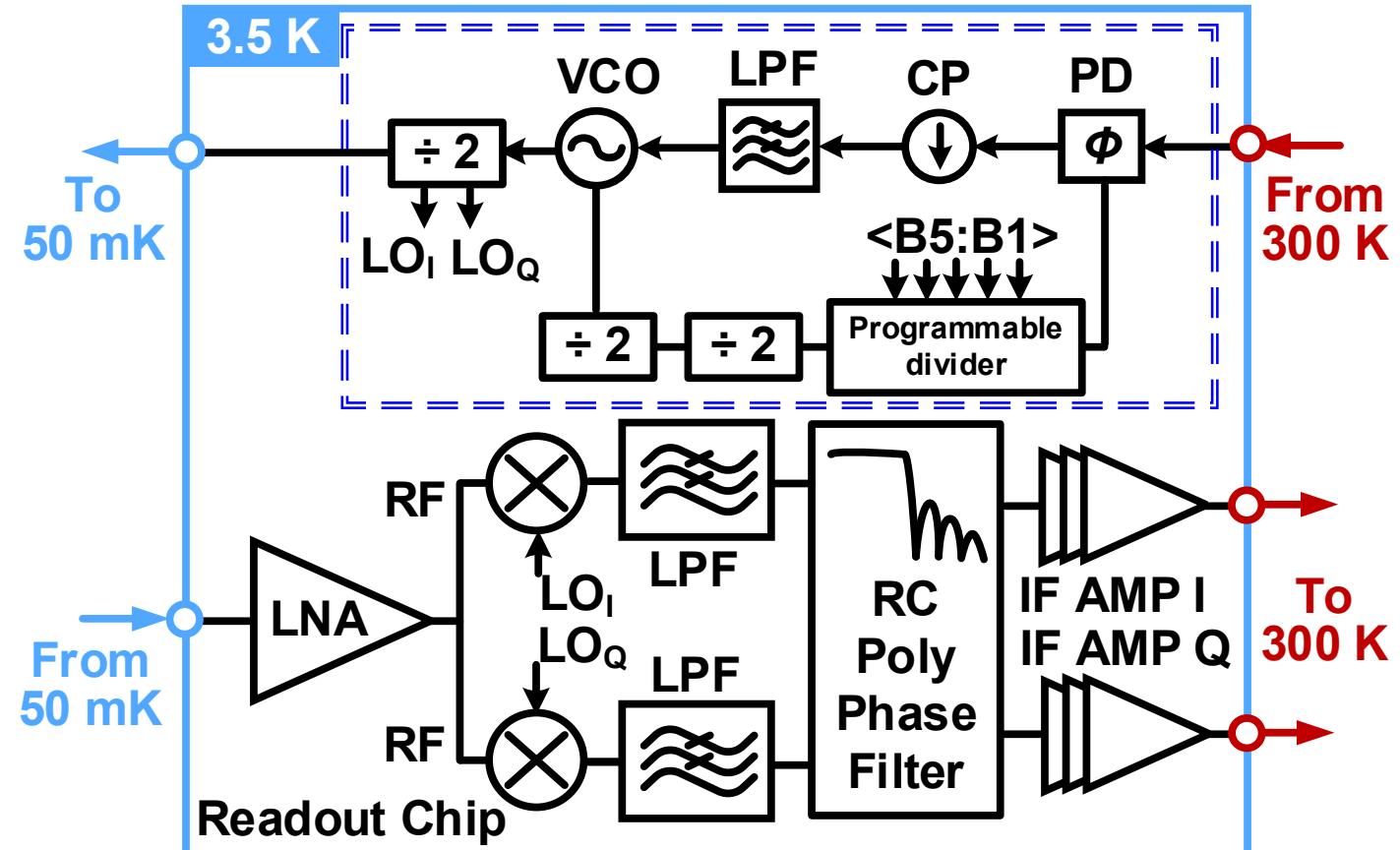
A scalable approach



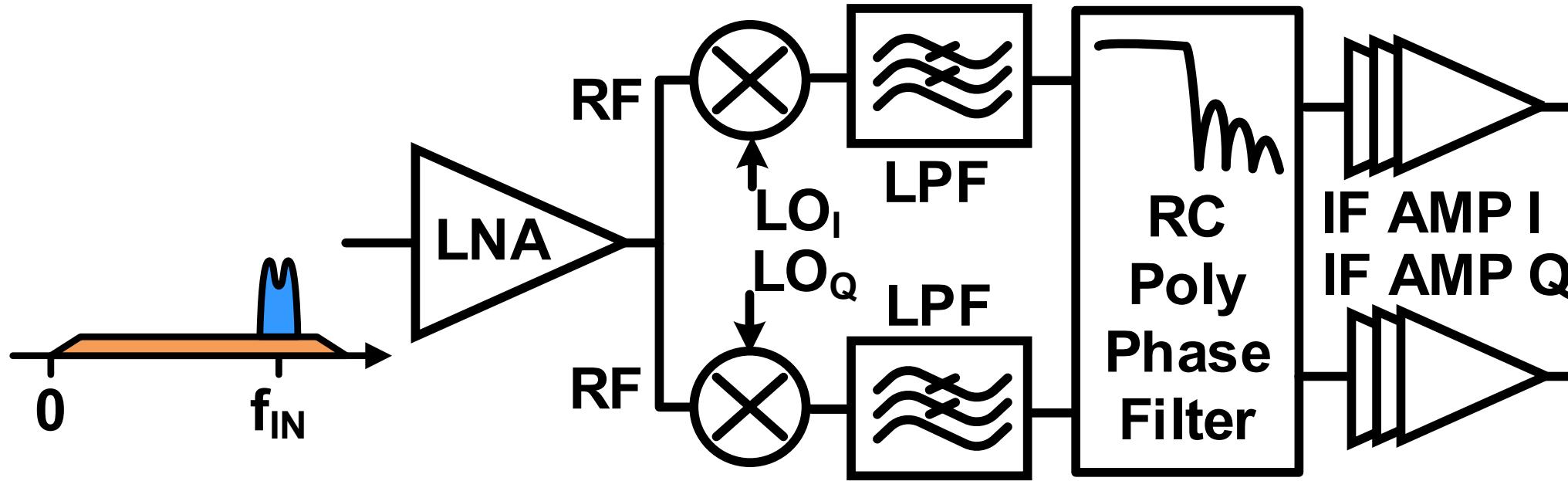
- Scalability is addressed by targeting:
 - ✓ Wide bandwidth for frequency multiplexing
 - ✓ Readout frequency ~6 GHz instead of sub-1 GHz for smaller inductors and higher Q factors

Cryogenic SoC architecture

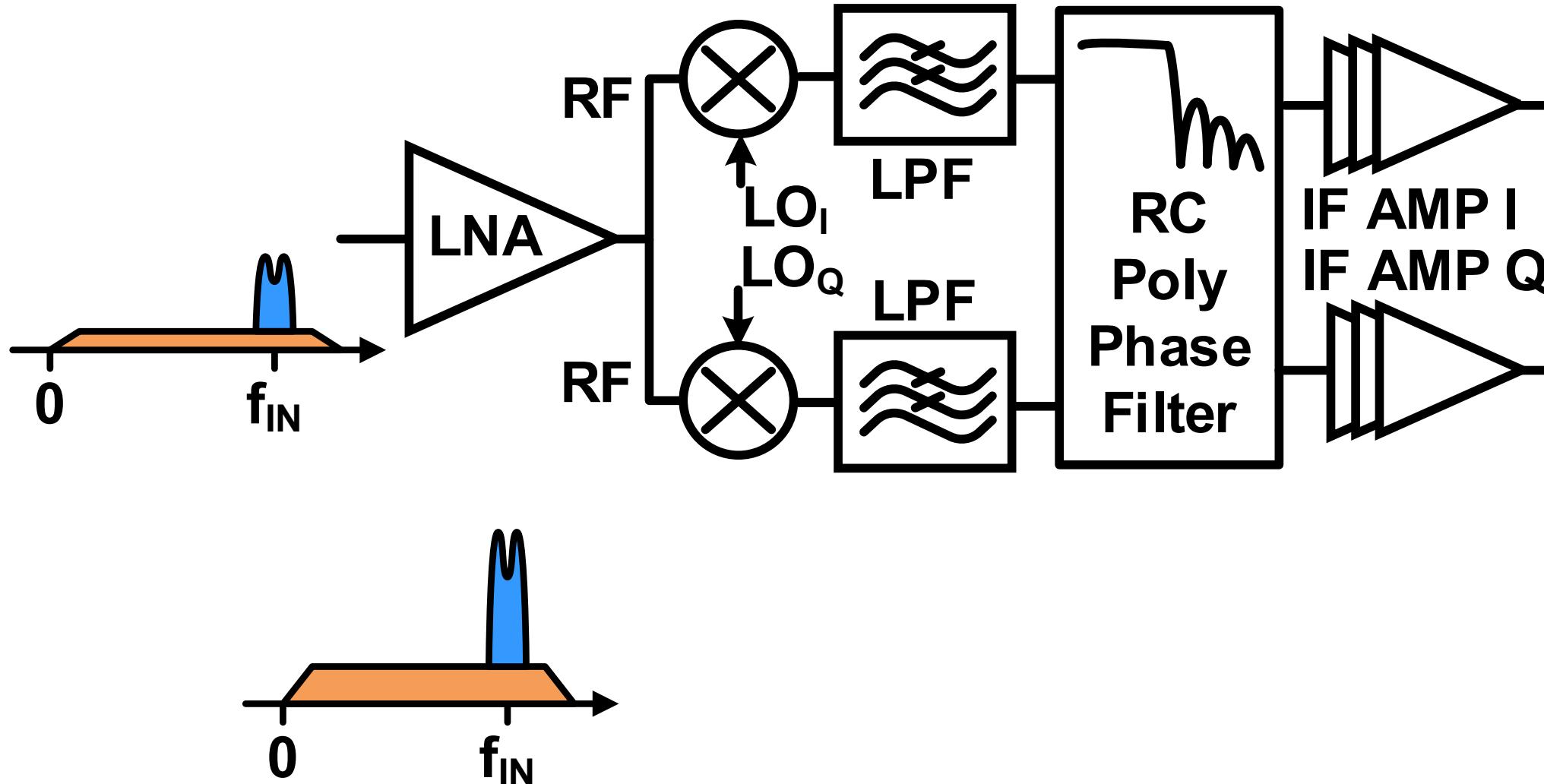
- Wideband 5-6.5 GHz receiver architecture for multiplexed readout
- Non-zero 0.1-1.5 GHz IF to suppress effects of flicker noise at low temperature
- Image-reject architecture for in-band noise suppression
- Frequency synthesizer on-chip for compactness



I/Q Low-noise receiver

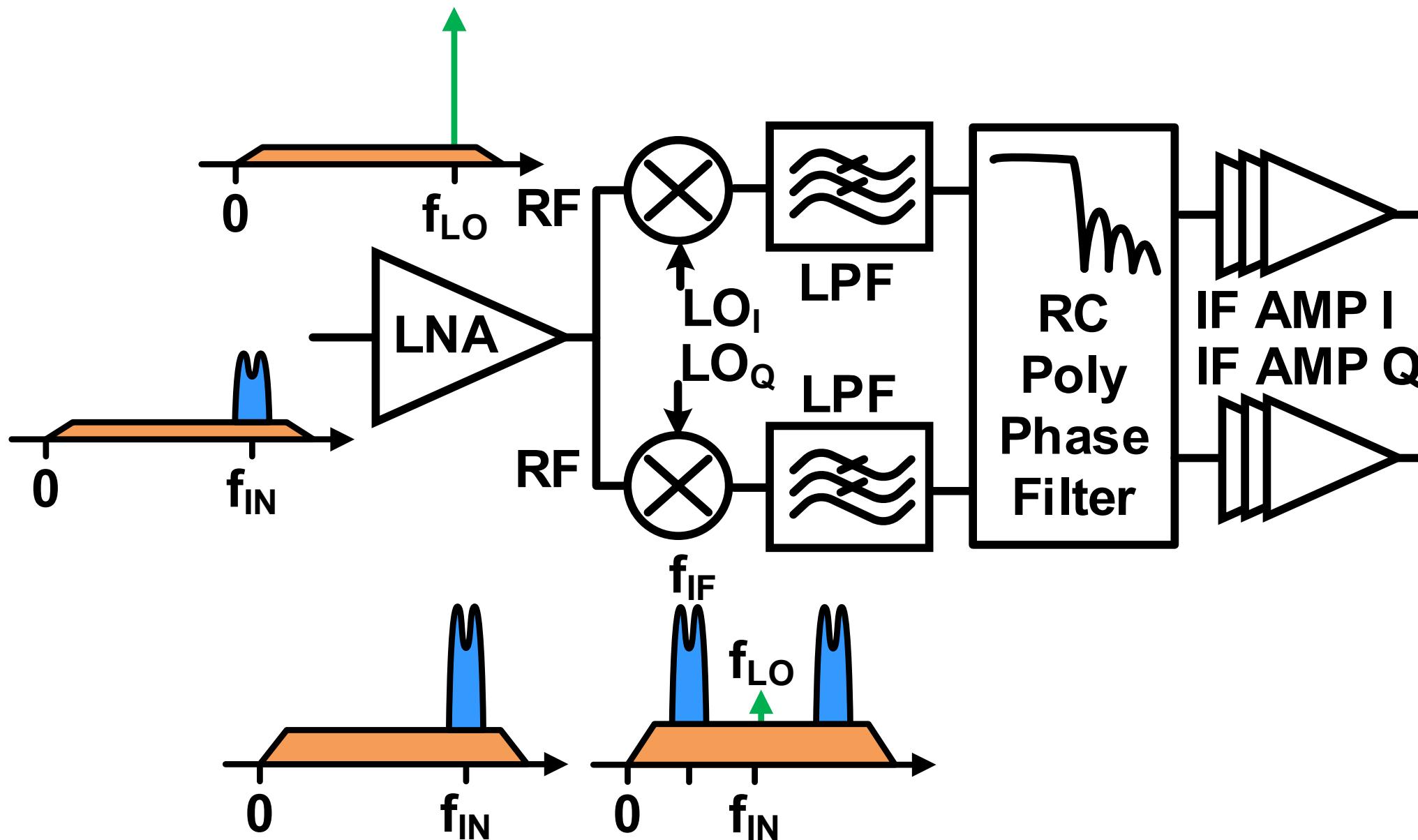


I/Q Low-noise receiver



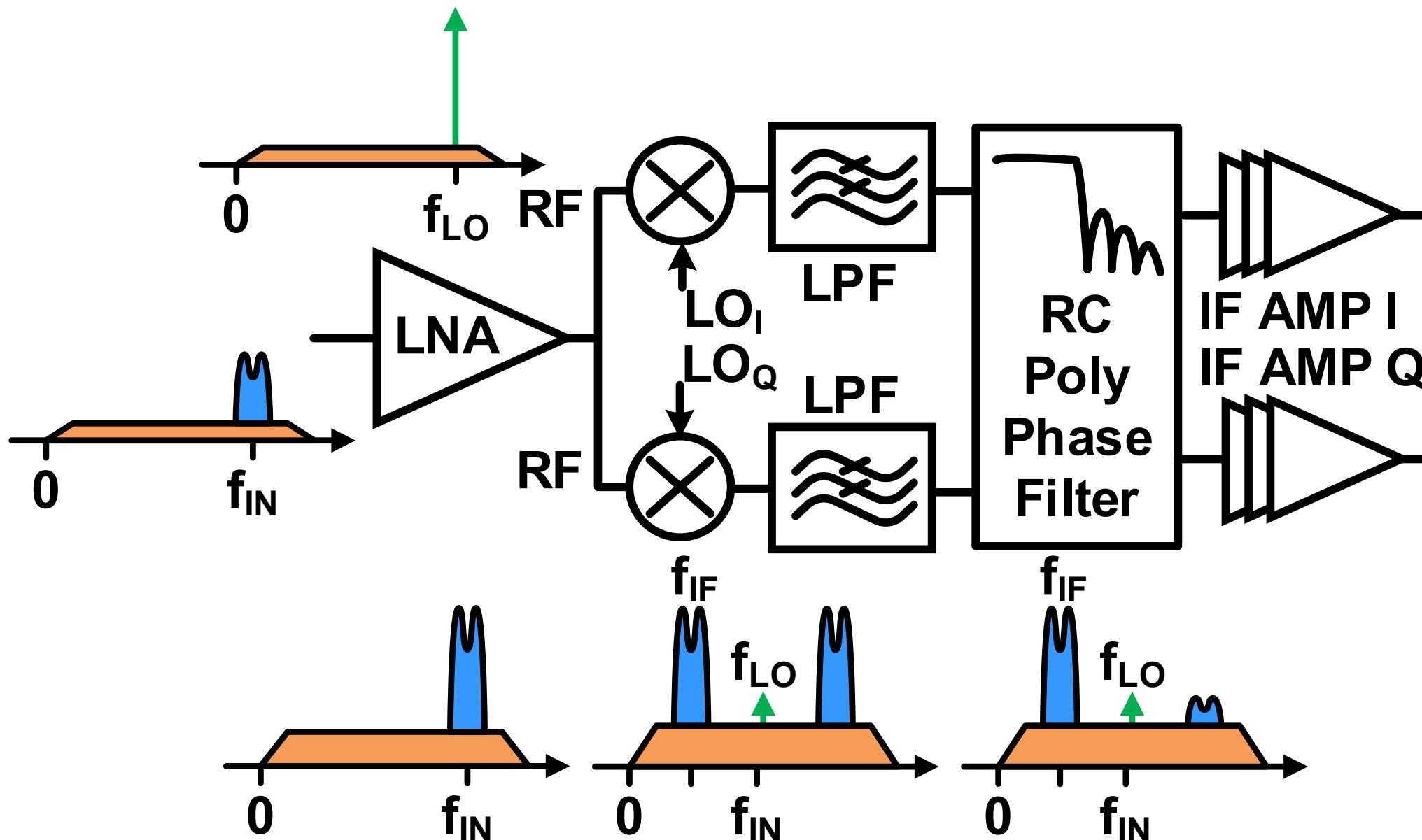
13.2: A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

I/Q Low-noise receiver



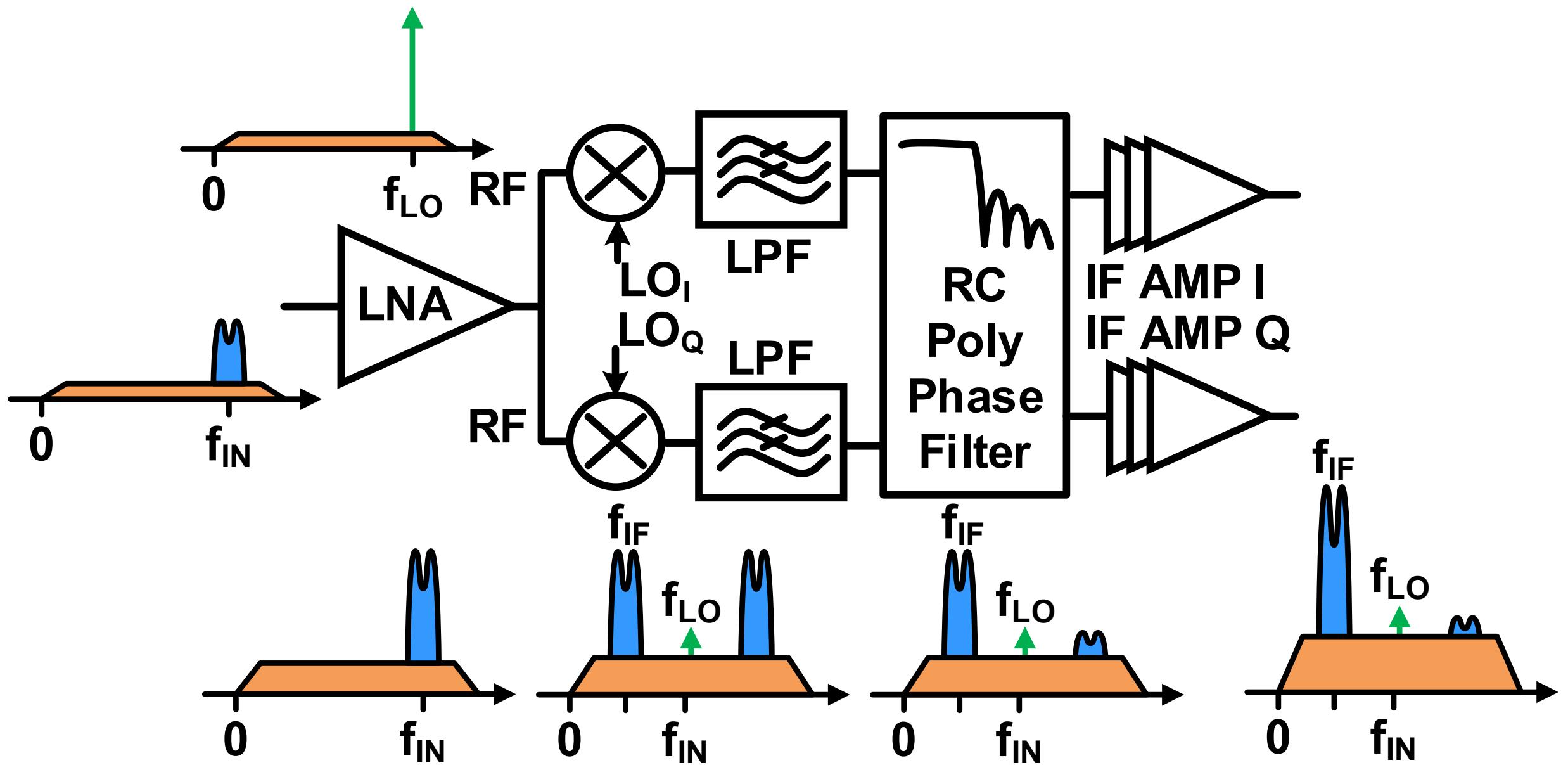
13.2: A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

I/Q Low-noise receiver



13.2: A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

I/Q Low-noise receiver

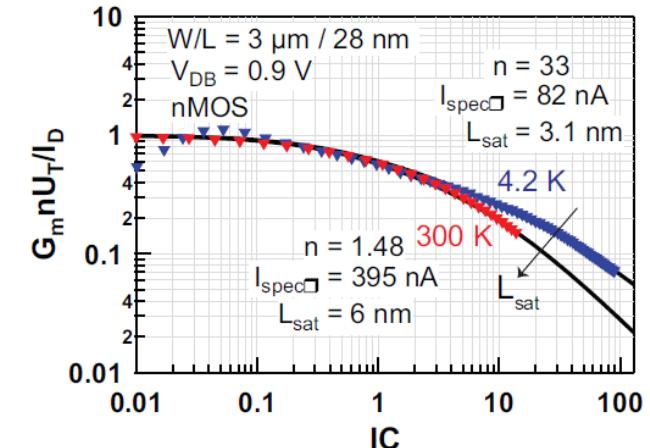
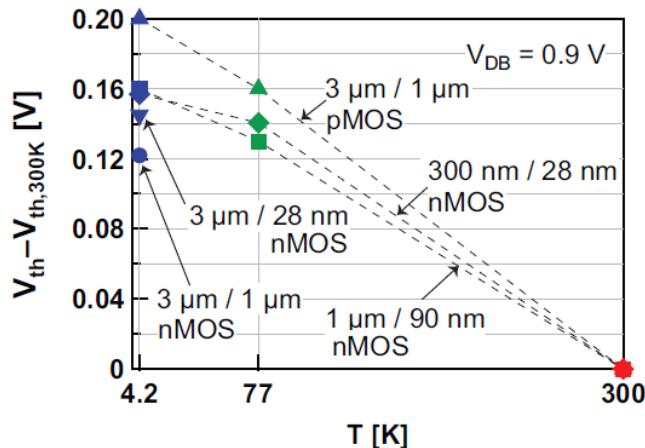


13.2: A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

Cryogenic CMOS circuit design

Transistors

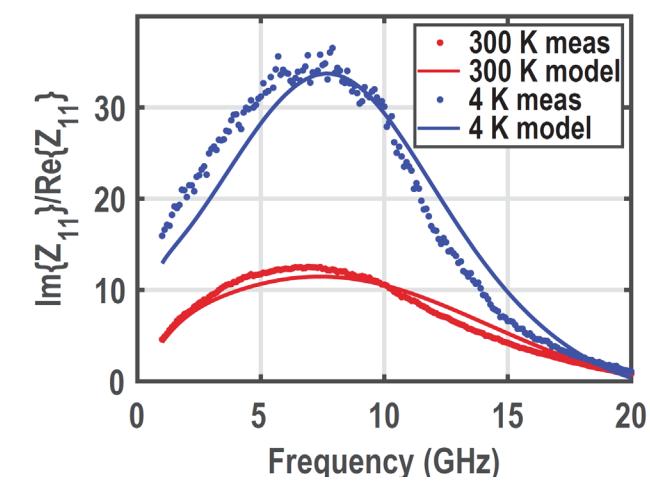
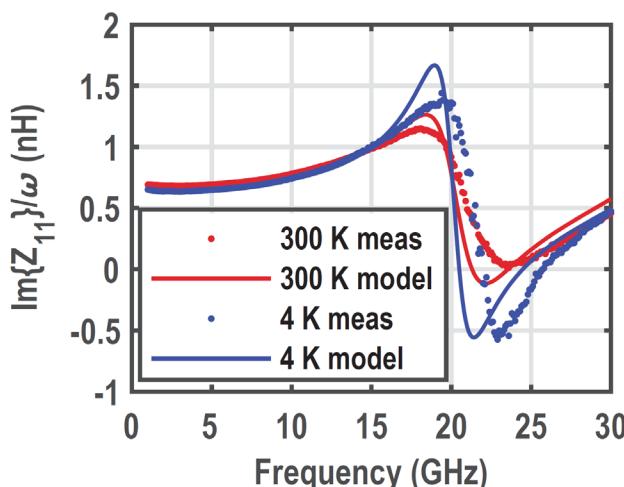
- Threshold voltage $V_{th} \uparrow$, voltage headroom \downarrow
- Transconductance efficiency $G_m/I_D \uparrow$, gain for same current \uparrow , lower power



[11] Beckers et al., ESSDERC 2017

Passives

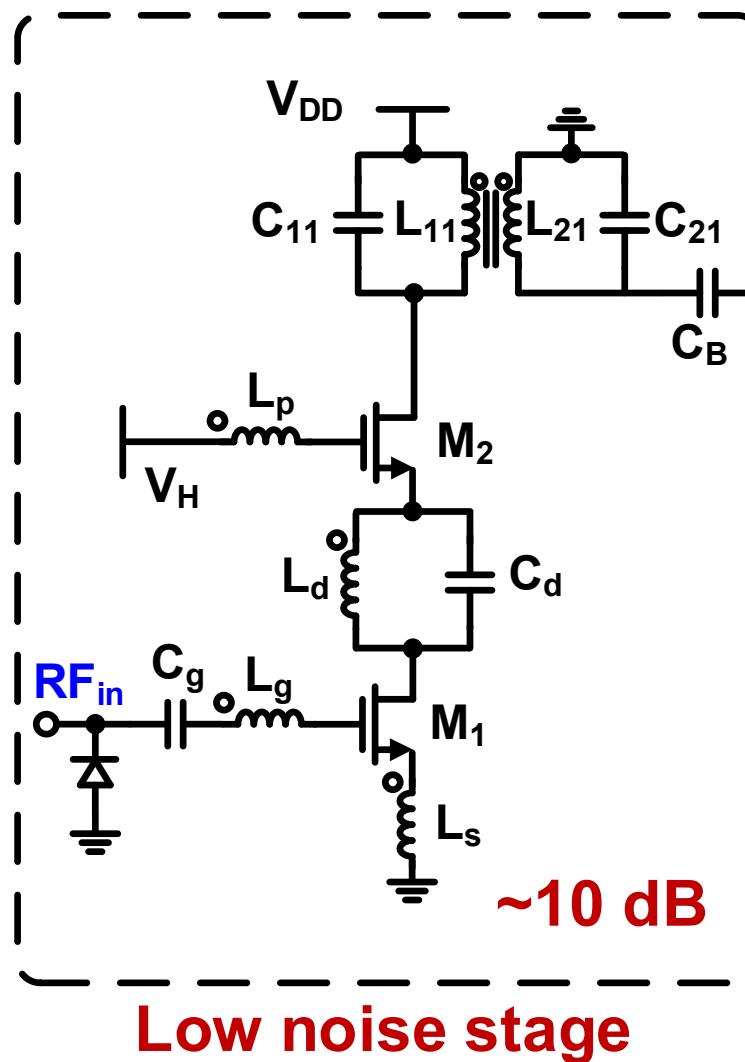
- Capacitance $C \uparrow$, inductance $L \downarrow$
- Quality factor $Q \uparrow$



[12] Patra et al., JEDS 2020

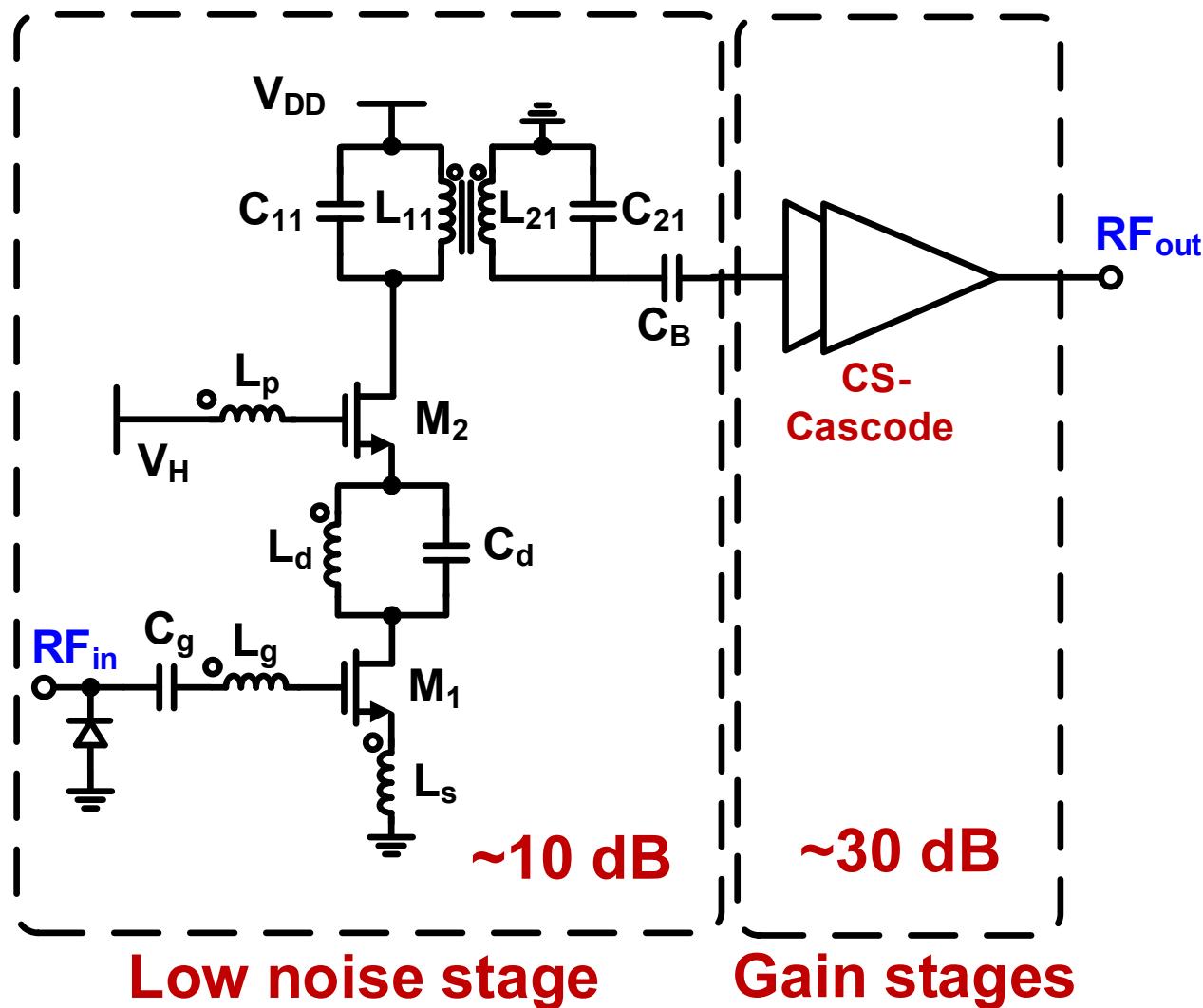
Low-noise amplifier

- Single-ended inductively degenerated common source LNA
- LC tank load for optimal noise impedance
- Transformer-coupled cascaded gain stages
- Optimal current biasing for low power
- 40 dB gain



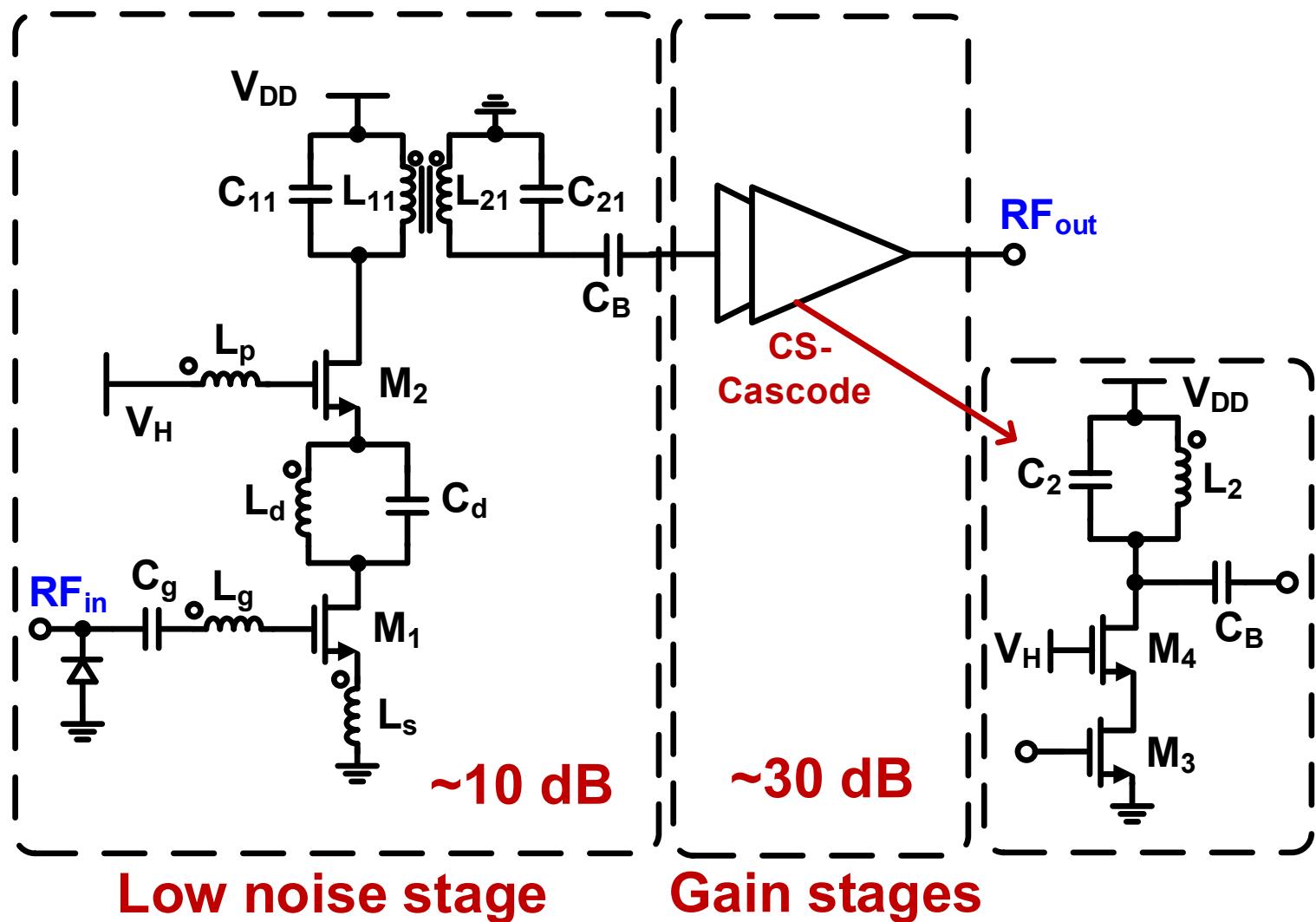
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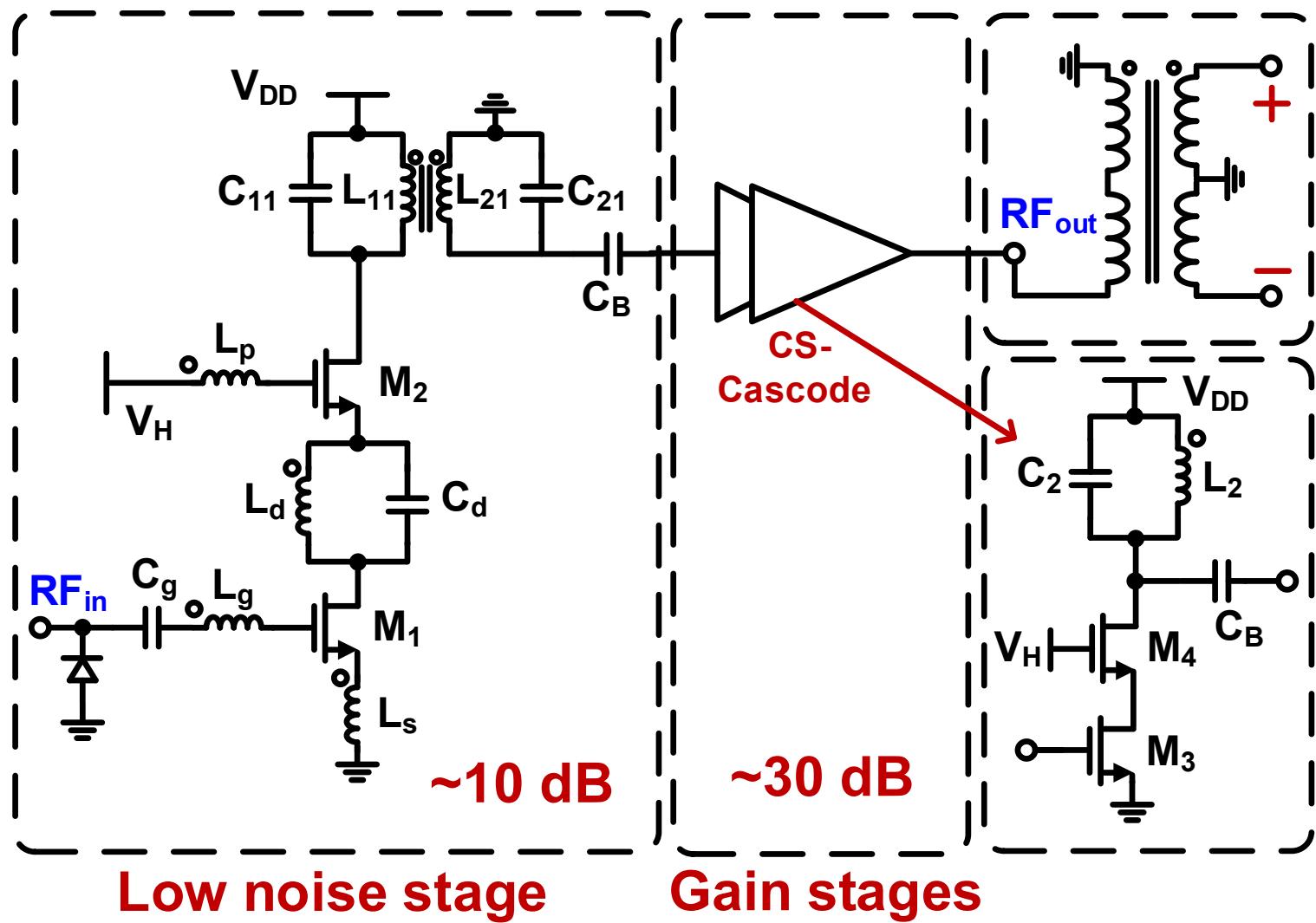
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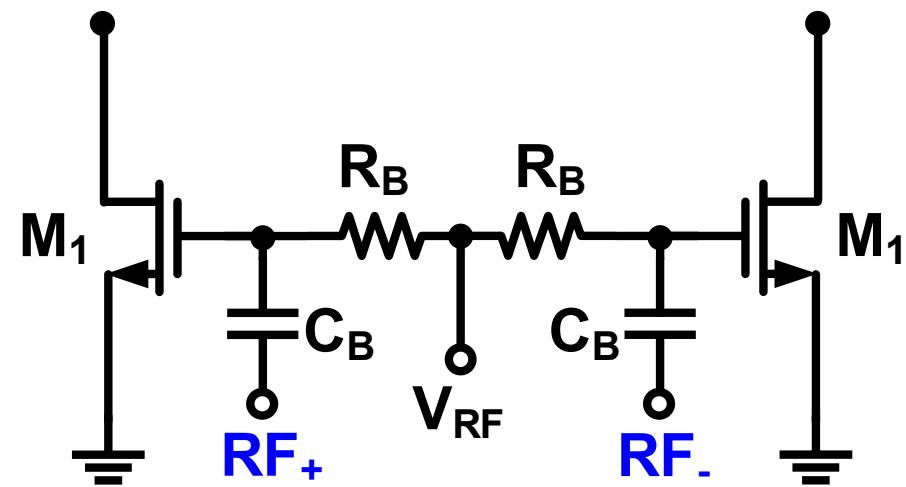
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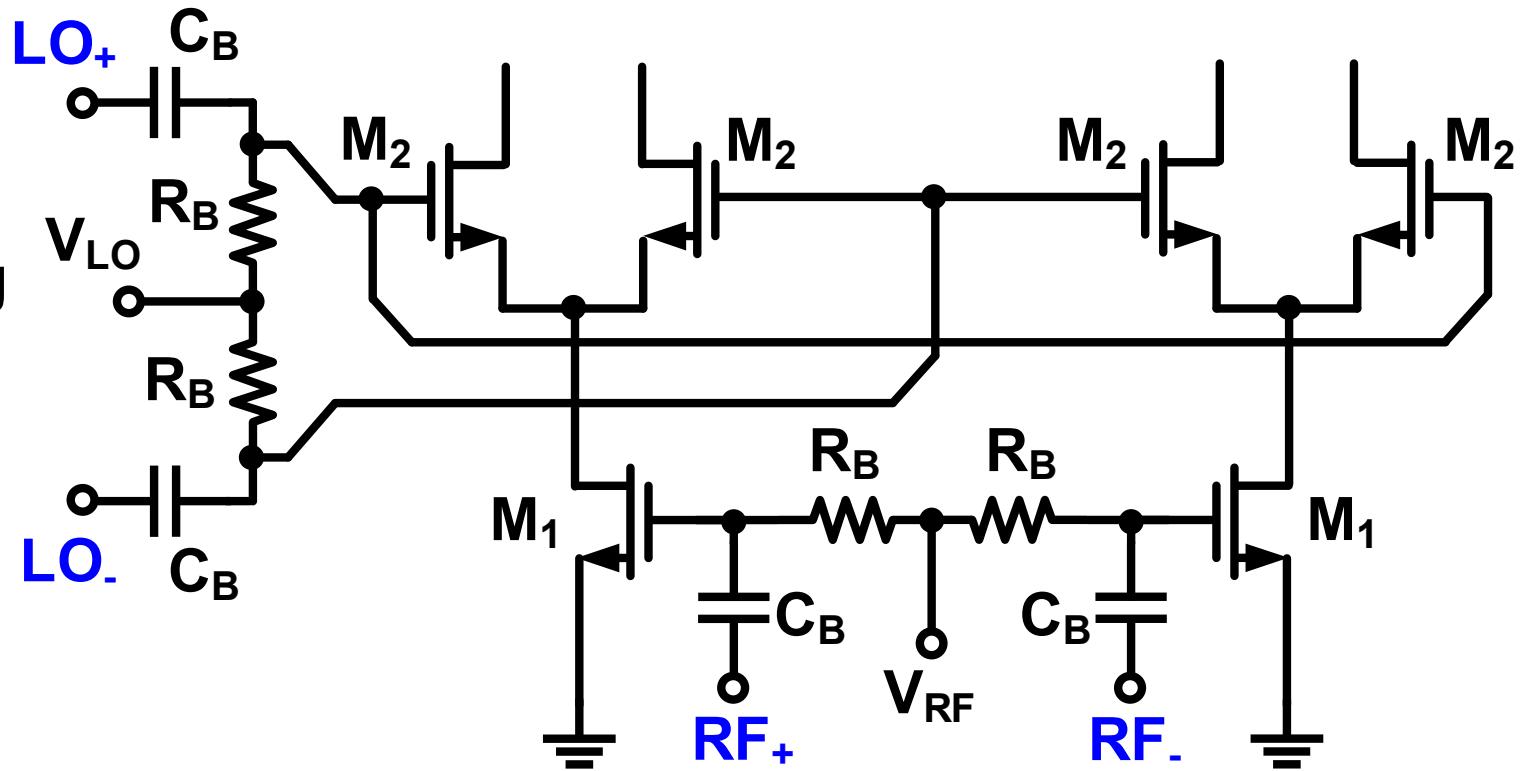
Mixer

- Single quadrature I/Q differential mixer for single-sideband (SSB) down-conversion
- Gilbert cell active mixer
- Resistor current bleeding for increased voltage headroom at low temperature
- 0.1-1.5 GHz IF with 4.9 GHz-6.3 GHz RF



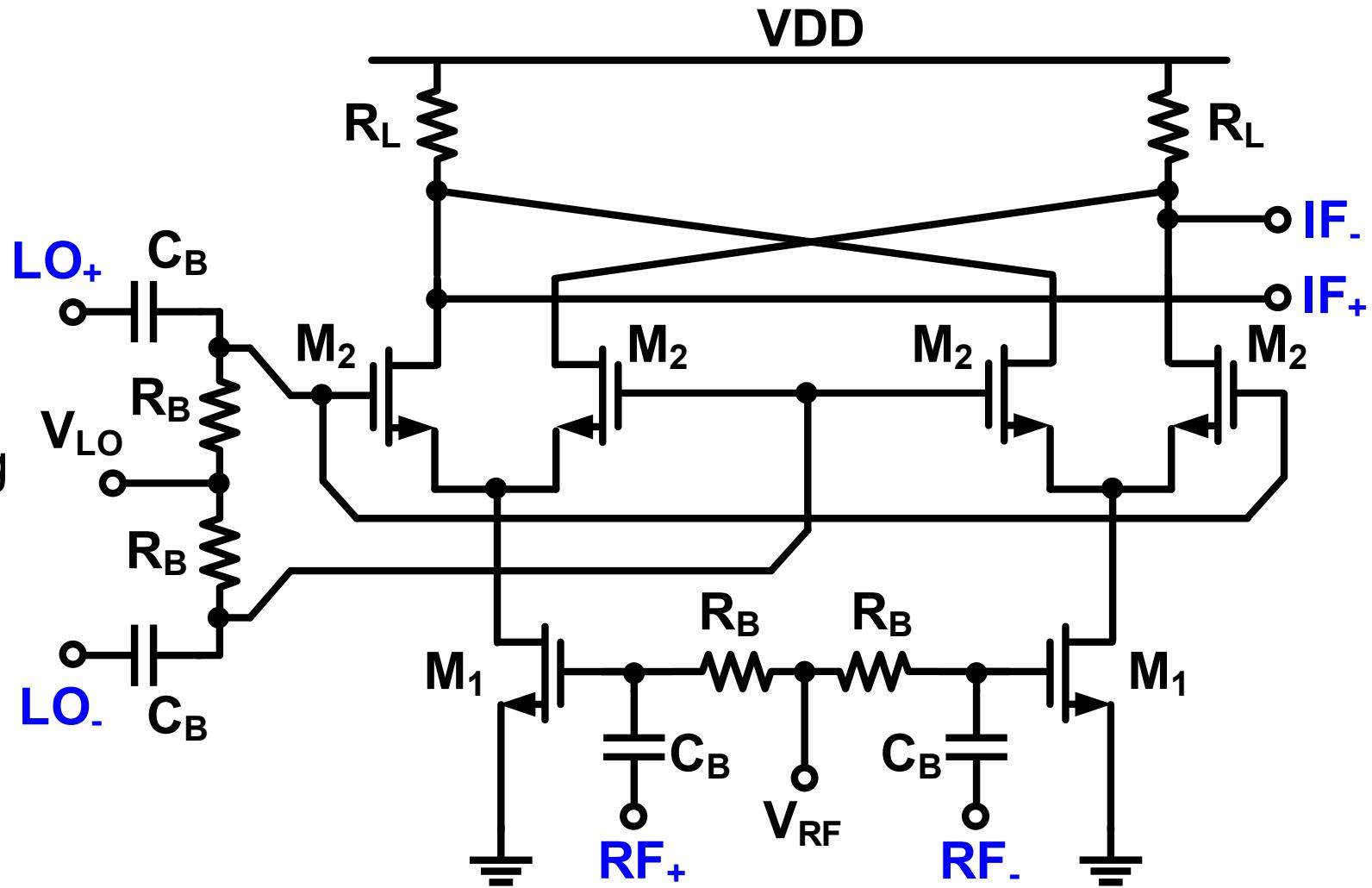
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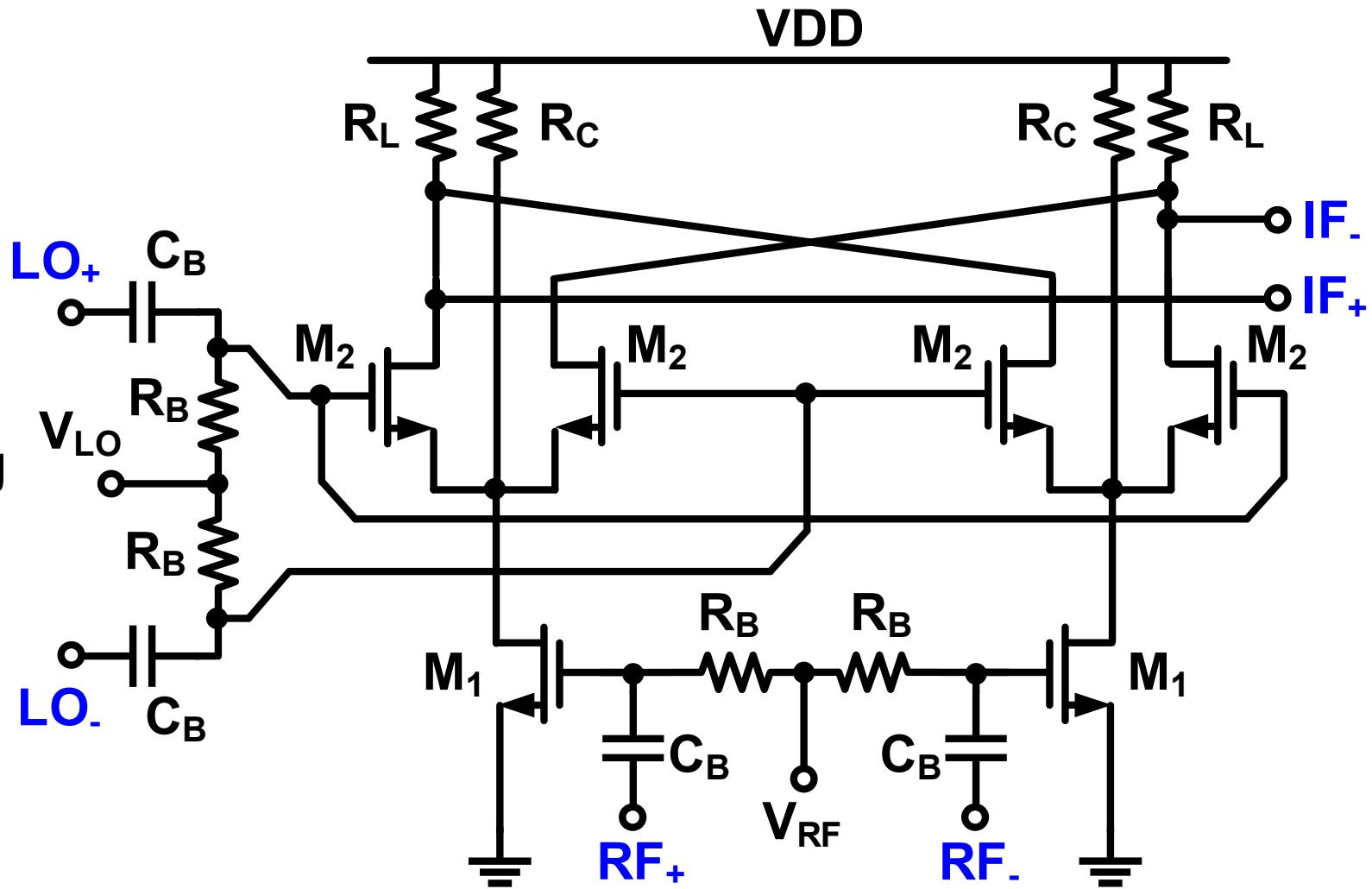
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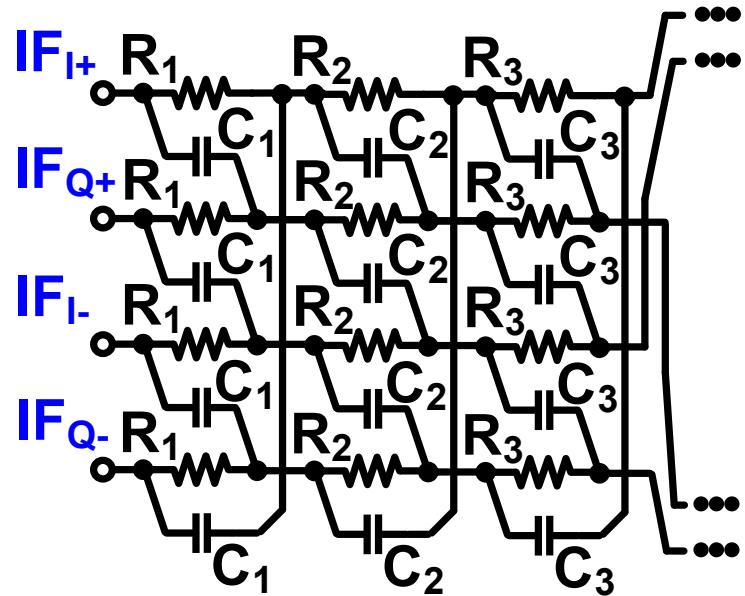


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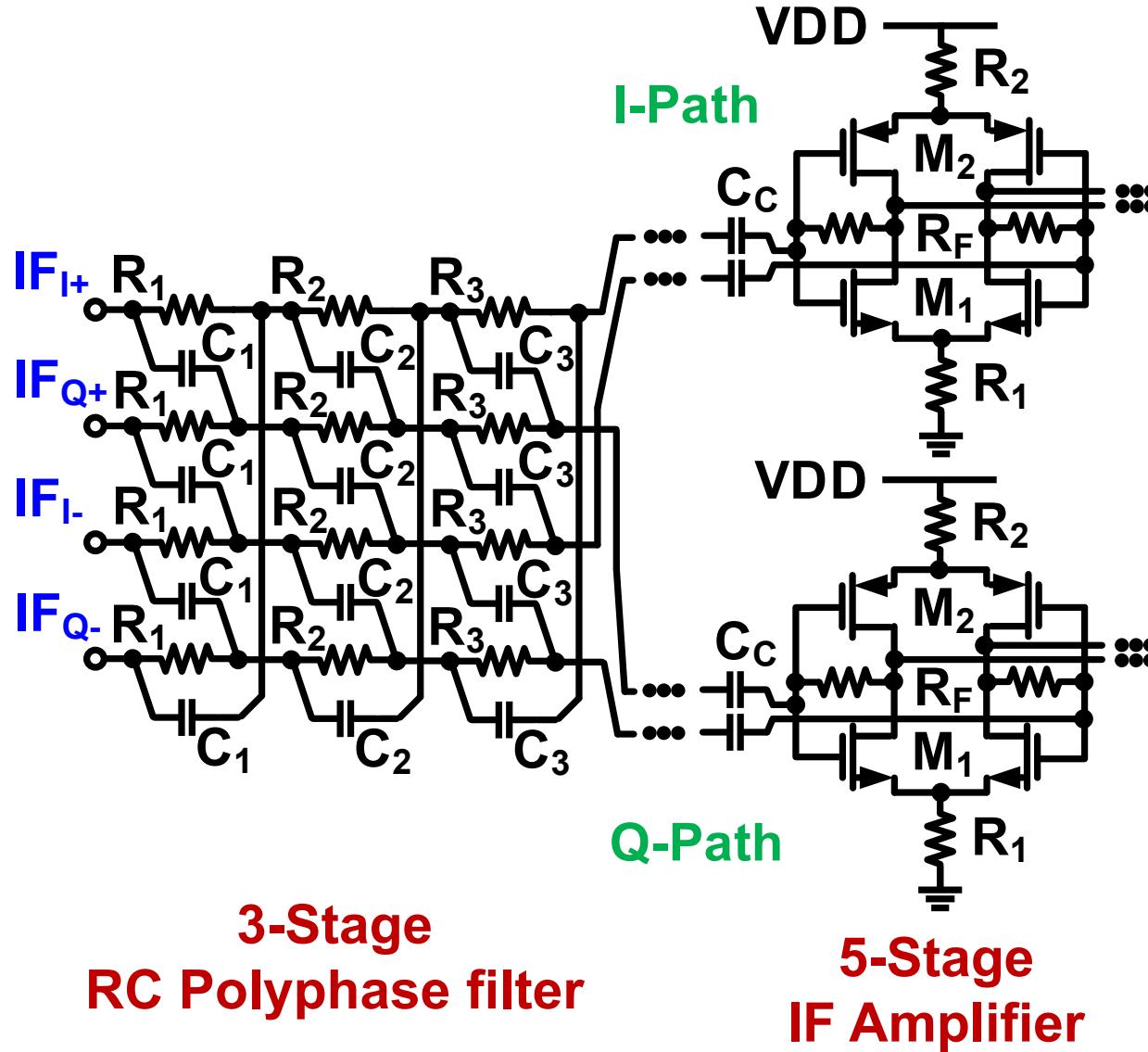


Intermediate Frequency chain

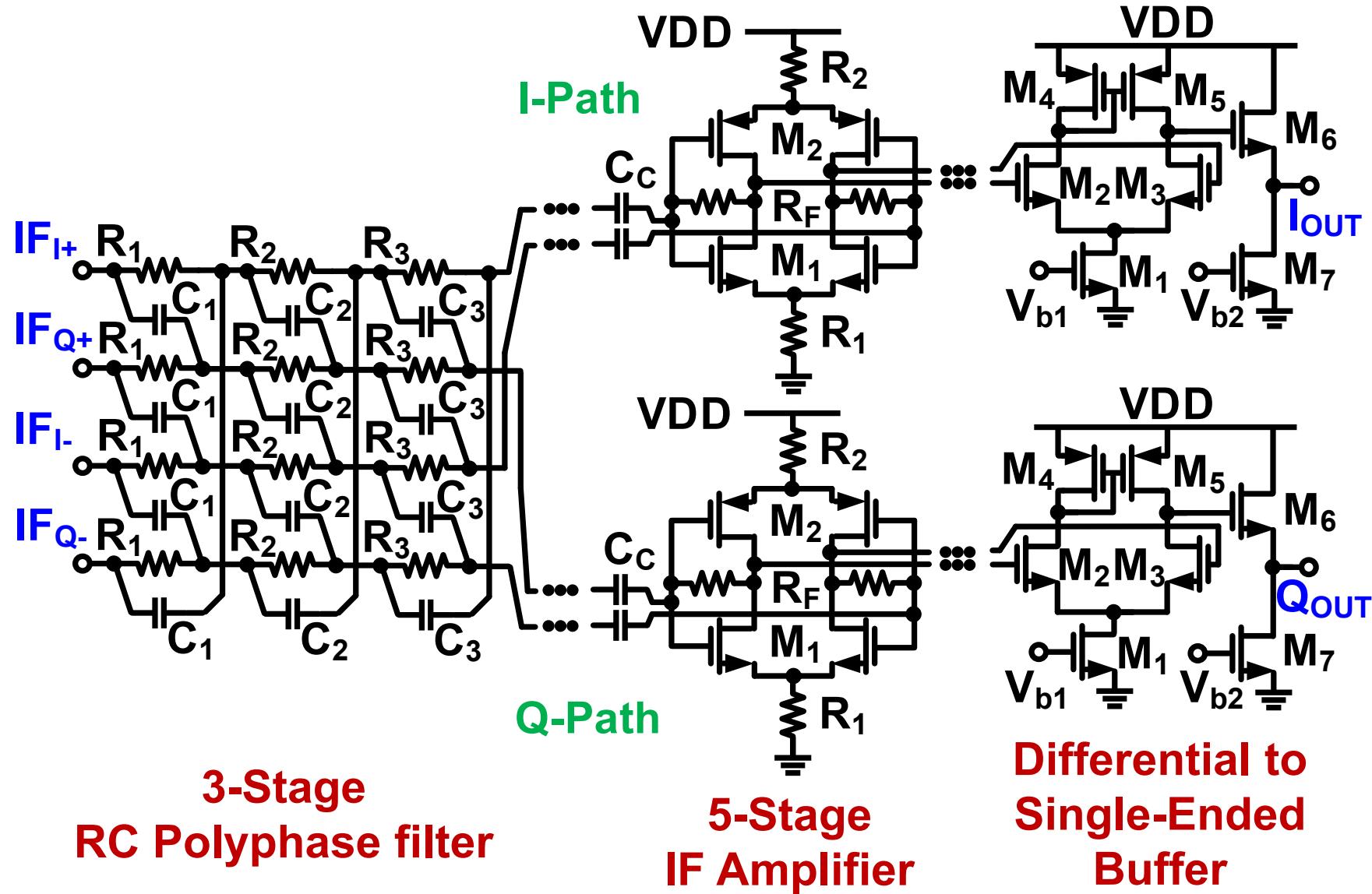


**3-Stage
RC Polyphase filter**

Intermediate Frequency chain

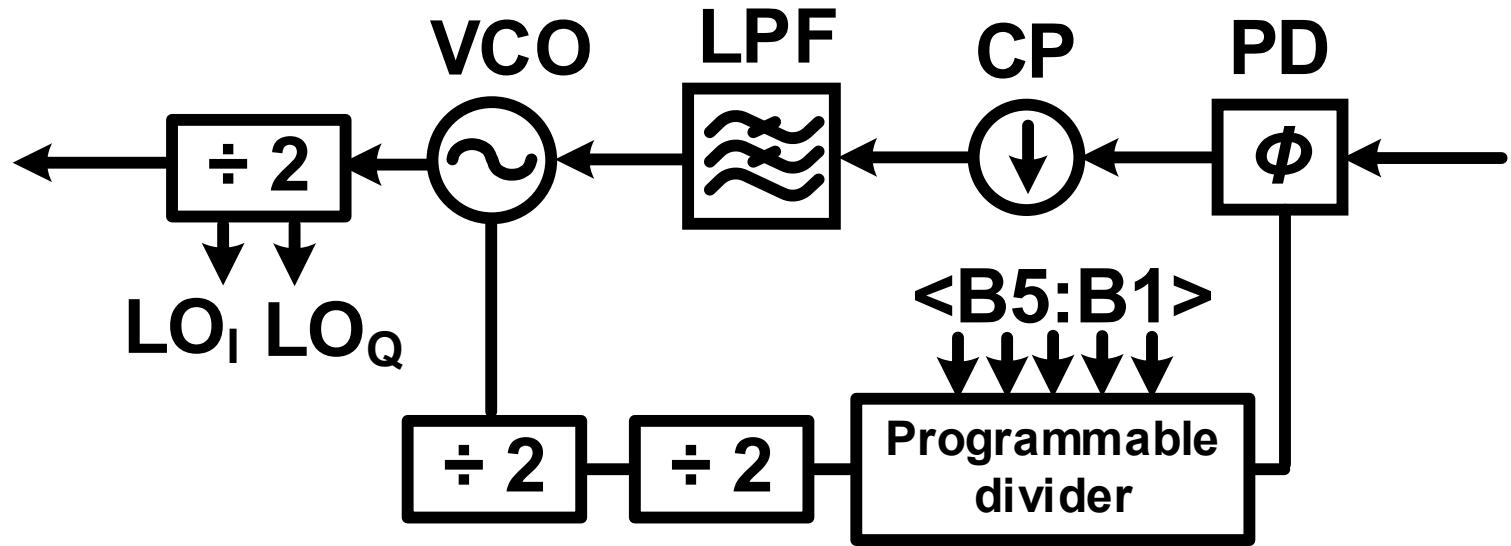


Intermediate Frequency chain

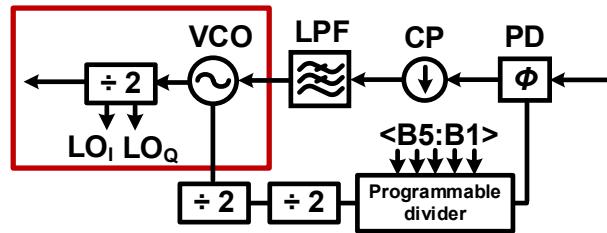


Frequency synthesizer architecture

- Analog charge-pump integer-N phase-locked loop
- Programmable divider to ensure locking range to the reference clock

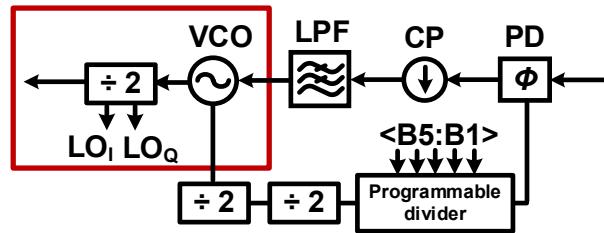


LC VCO and CML divider

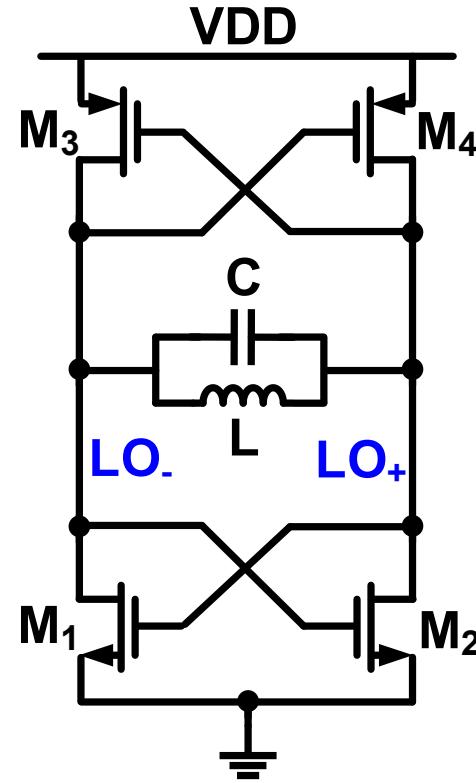


- 12.8 GHz VCO with divider by 2 to generate quadrature 6.4 GHz
- Push-pull LC VCO for low power
- 1.25 V supply voltage for 3.5 mA current
- CML latch with inductive-resistive load for wider bandwidth locking range
- VCO driving FD directly to save power

LC VCO and CML divider

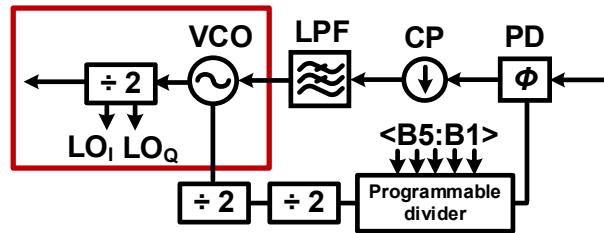


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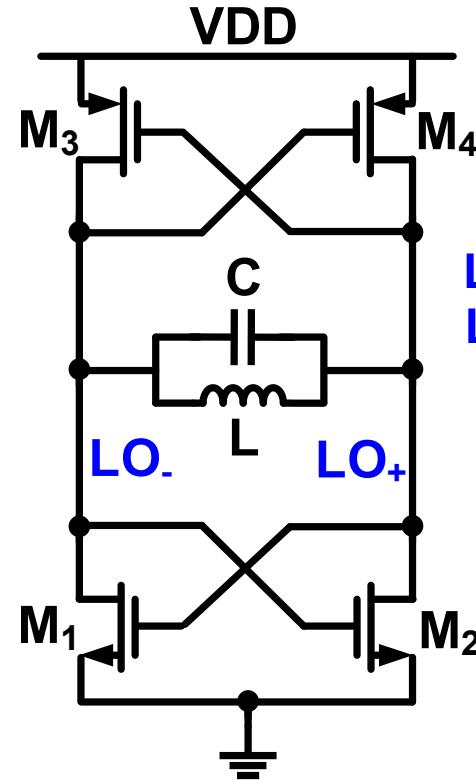


**Push-Pull
LC-Tank VCO**

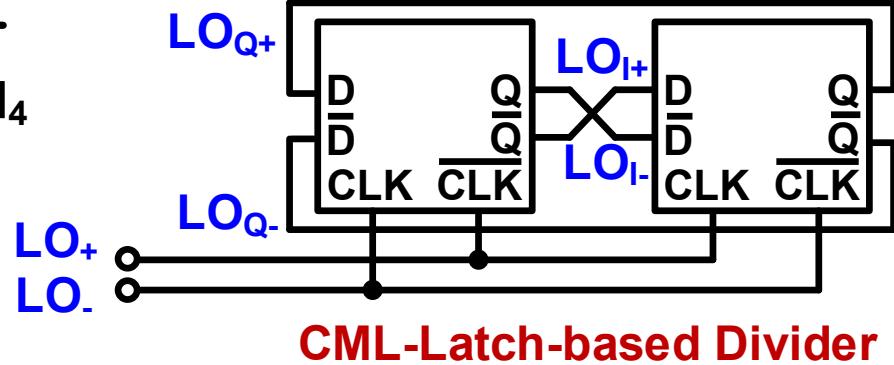
LC VCO and CML divider



- 12.8 GHz VCO with divider by 2 to generate quadrature 6.4 GHz
- Push-pull LC VCO for low power
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- CML latch with inductive-resistive load for wider bandwidth locking range
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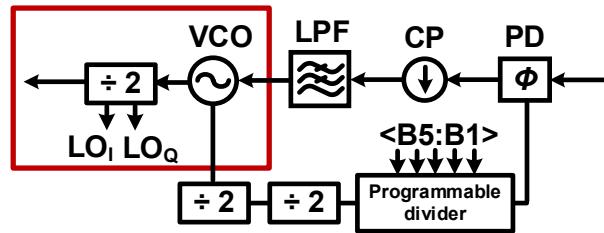


Push-Pull
LC-Tank VCO

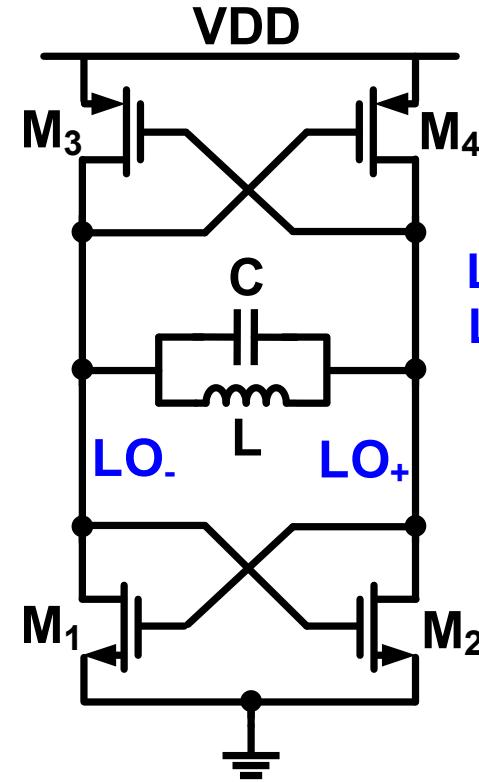


CML-Latch-based Divider

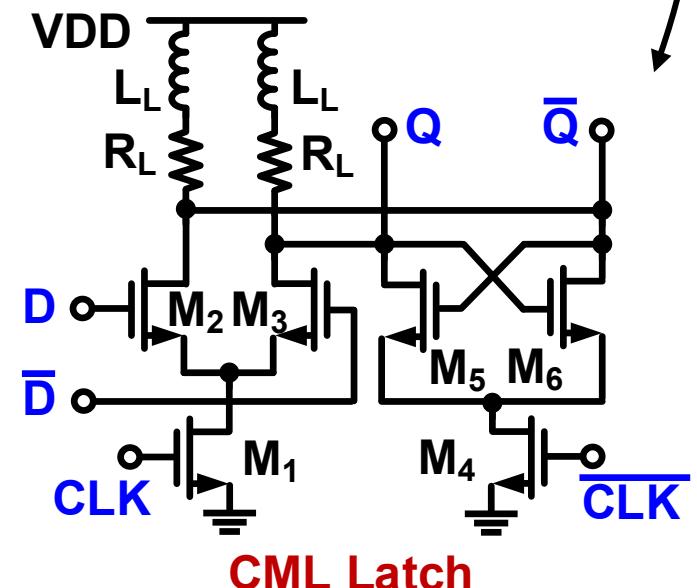
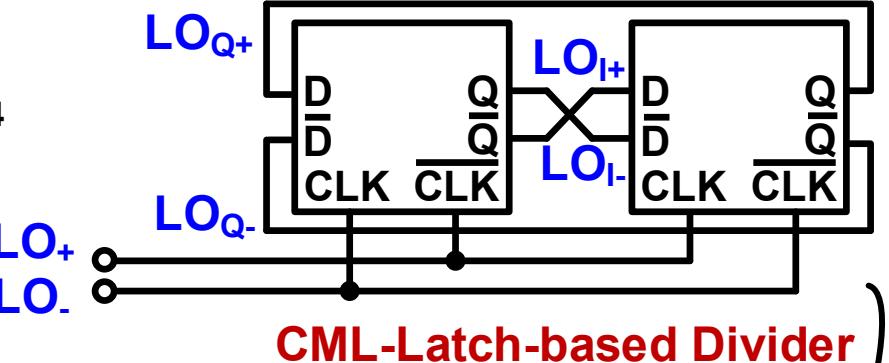
LC VCO and CML divider



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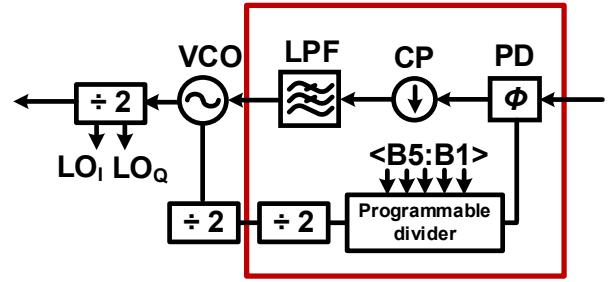


Push-Pull
LC-Tank VCO



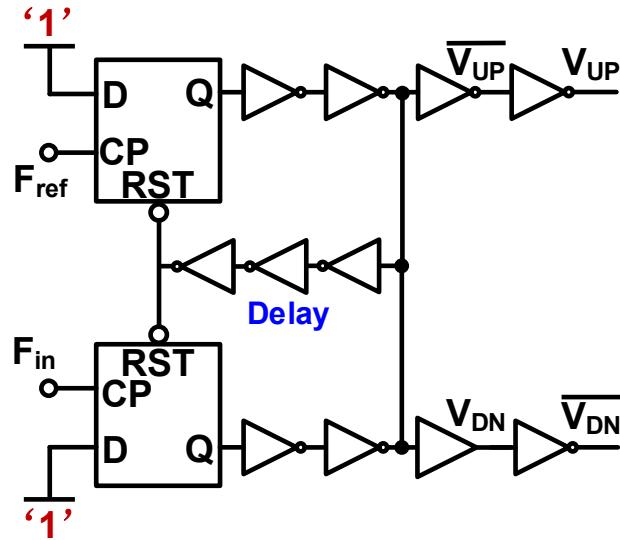
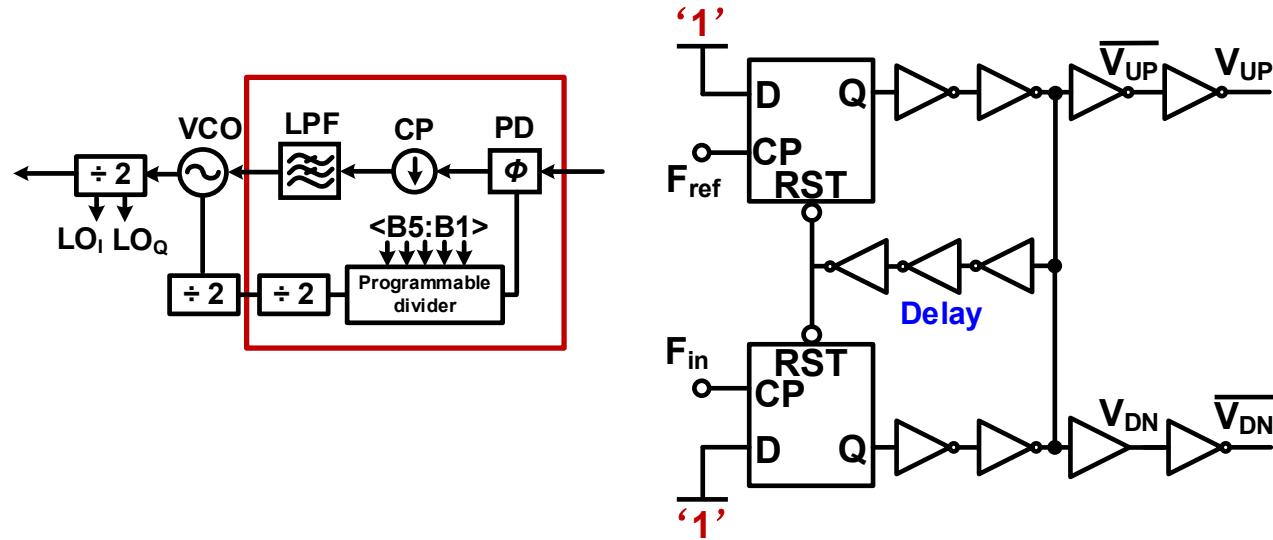
CML Latch

PLL internal blocks



13.2: A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

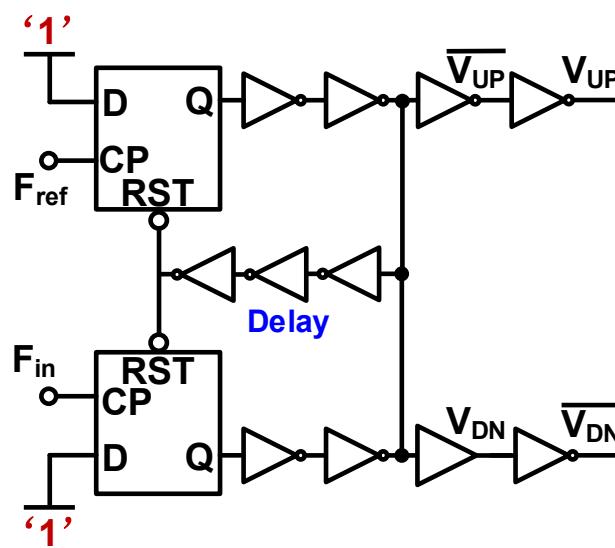
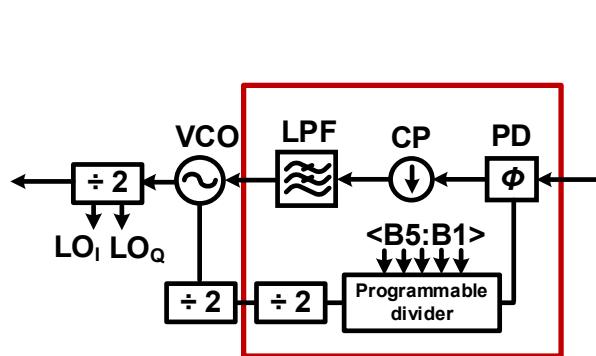
PLL internal blocks



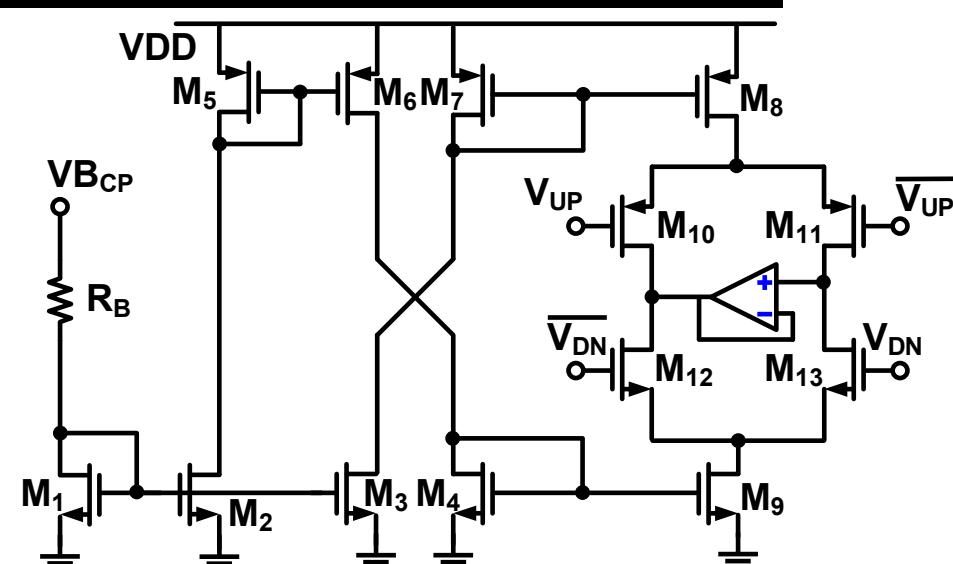
Phase Frequency Detector

- PFD with two edge-triggered, resettable D Flip-Flops

PLL internal blocks



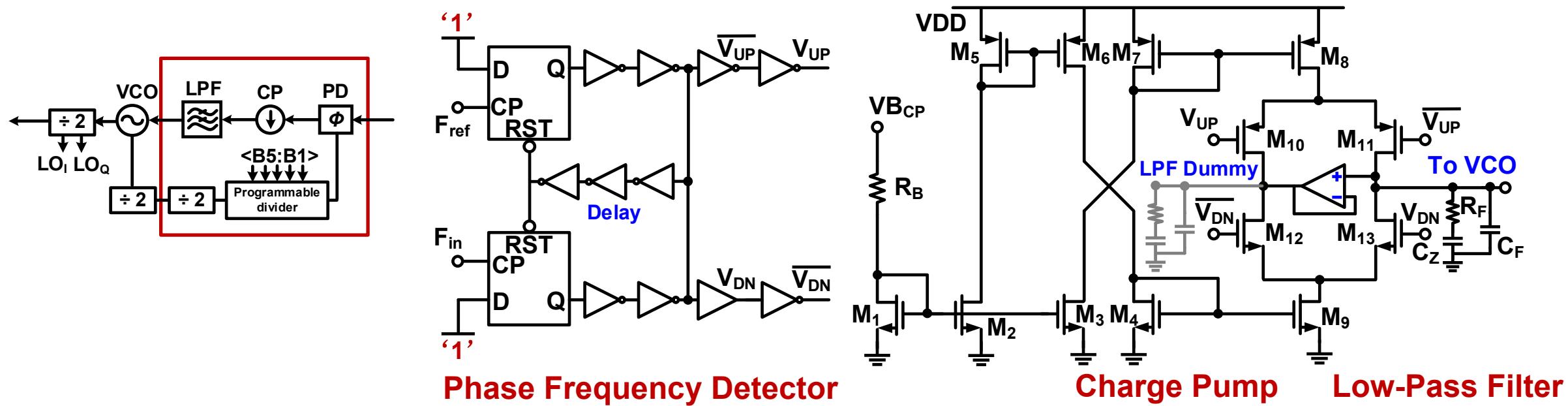
Phase Frequency Detector



Charge Pump

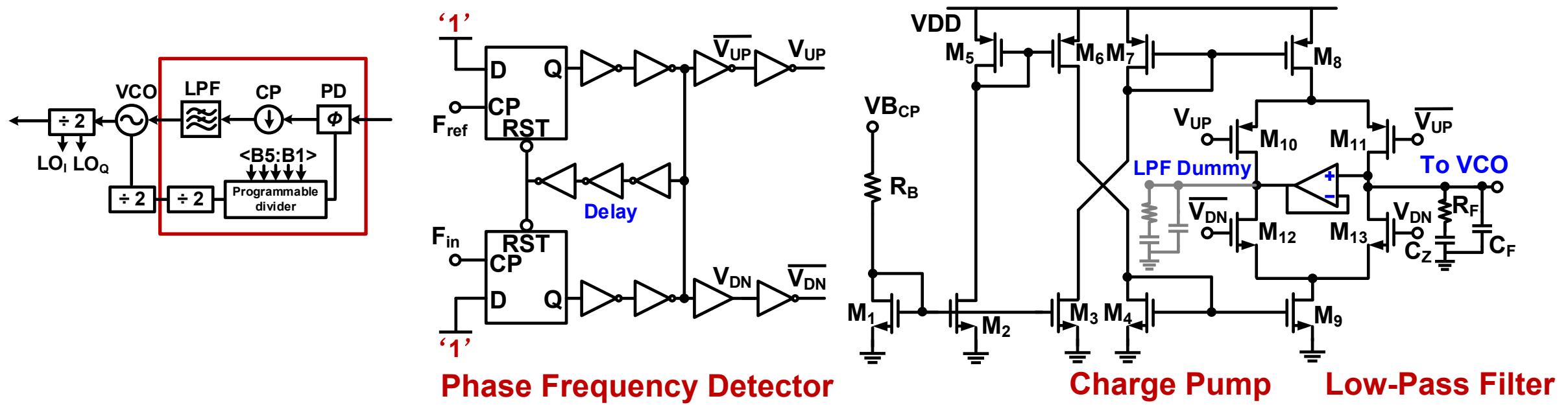
- PFD with two edge-triggered, resettable D Flip-Flops
- Balanced charge pump to reduce mismatch and charge injections

PLL internal blocks



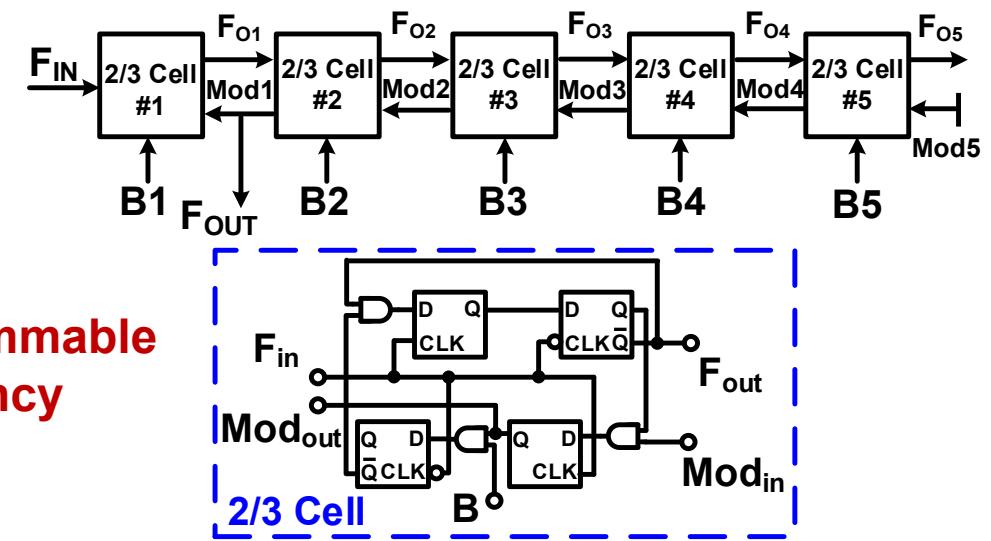
- PFD with two edge-triggered, resettable D Flip-Flops
- Balanced charge pump to reduce mismatch and charge injections
- Second order LPF with large 1.5 MHz bandwidth
- Dummy LPF to balance the two paths

PLL internal blocks

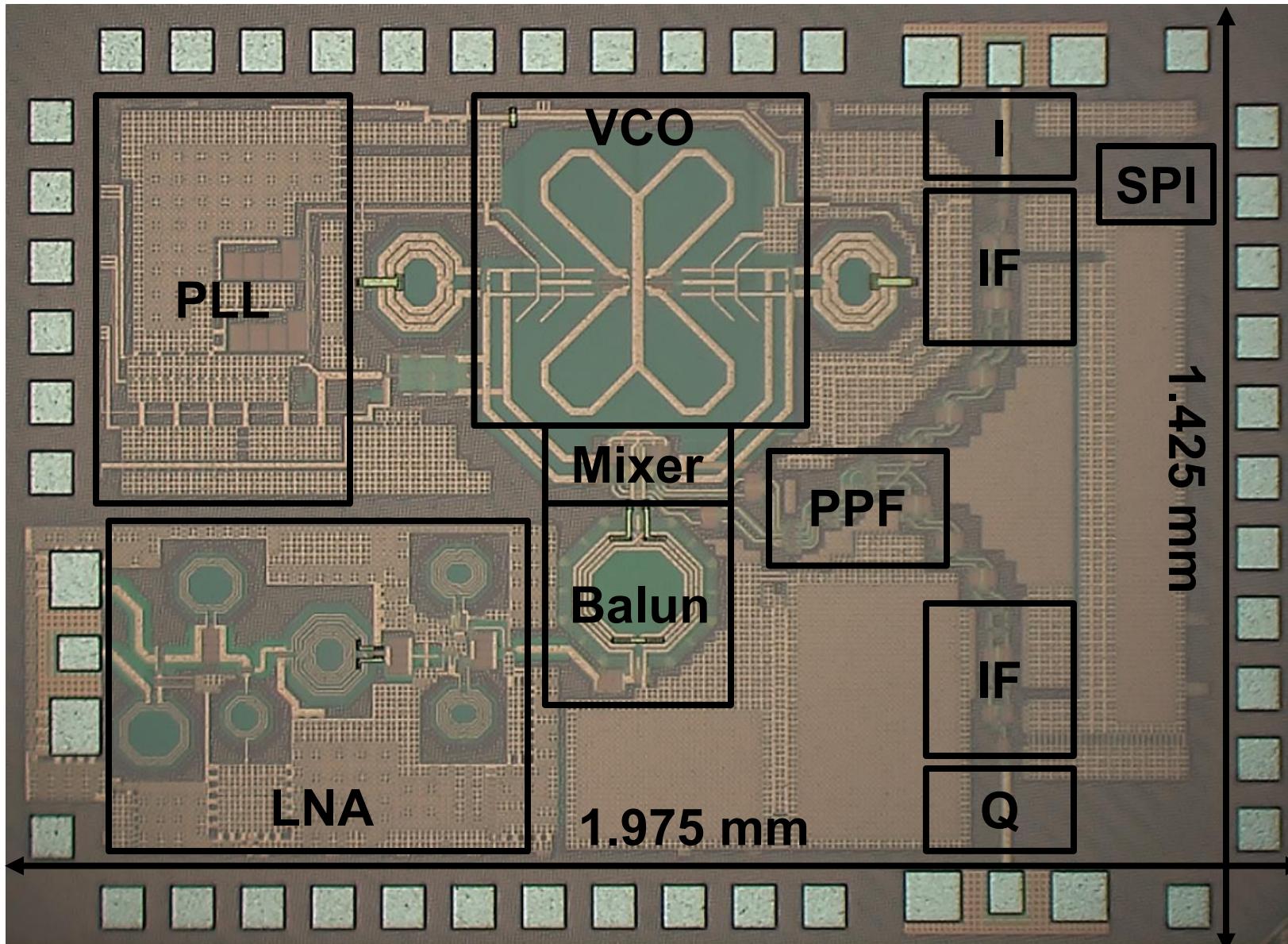


- PFD with two edge-triggered, resettable D Flip-Flops
- Balanced charge pump to reduce mismatch and charge injections
- Second order LPF with large 1.5 MHz bandwidth
- Dummy LPF to balance the two paths

Programmable Frequency Divider

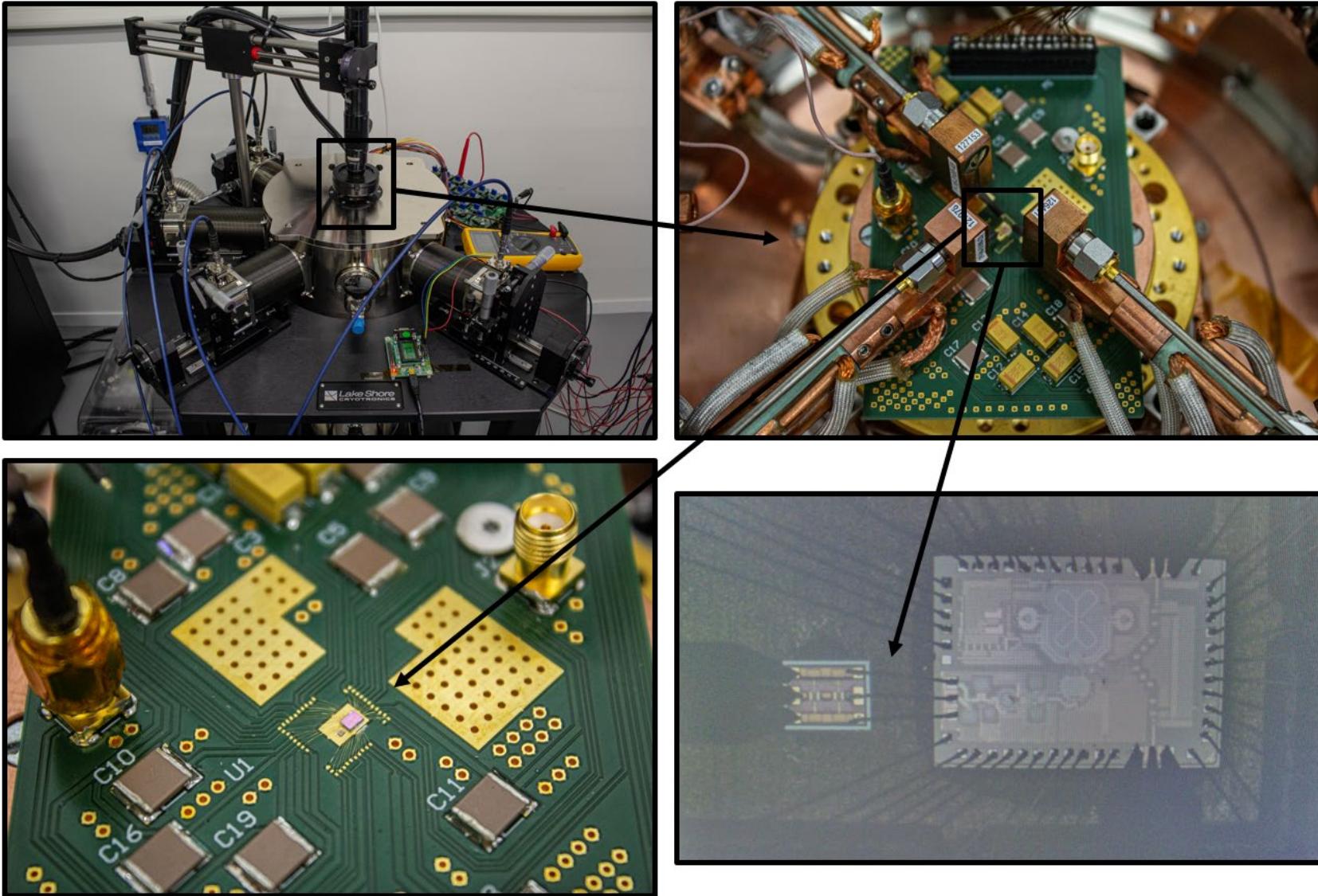


40-nm CMOS SoC prototype



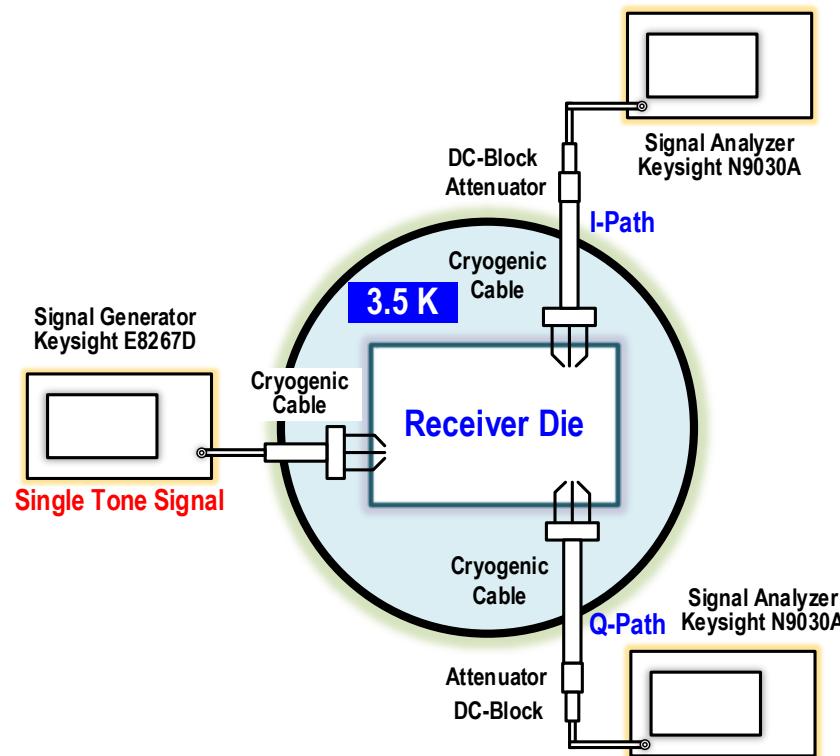
13.2: A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

Measurement setup

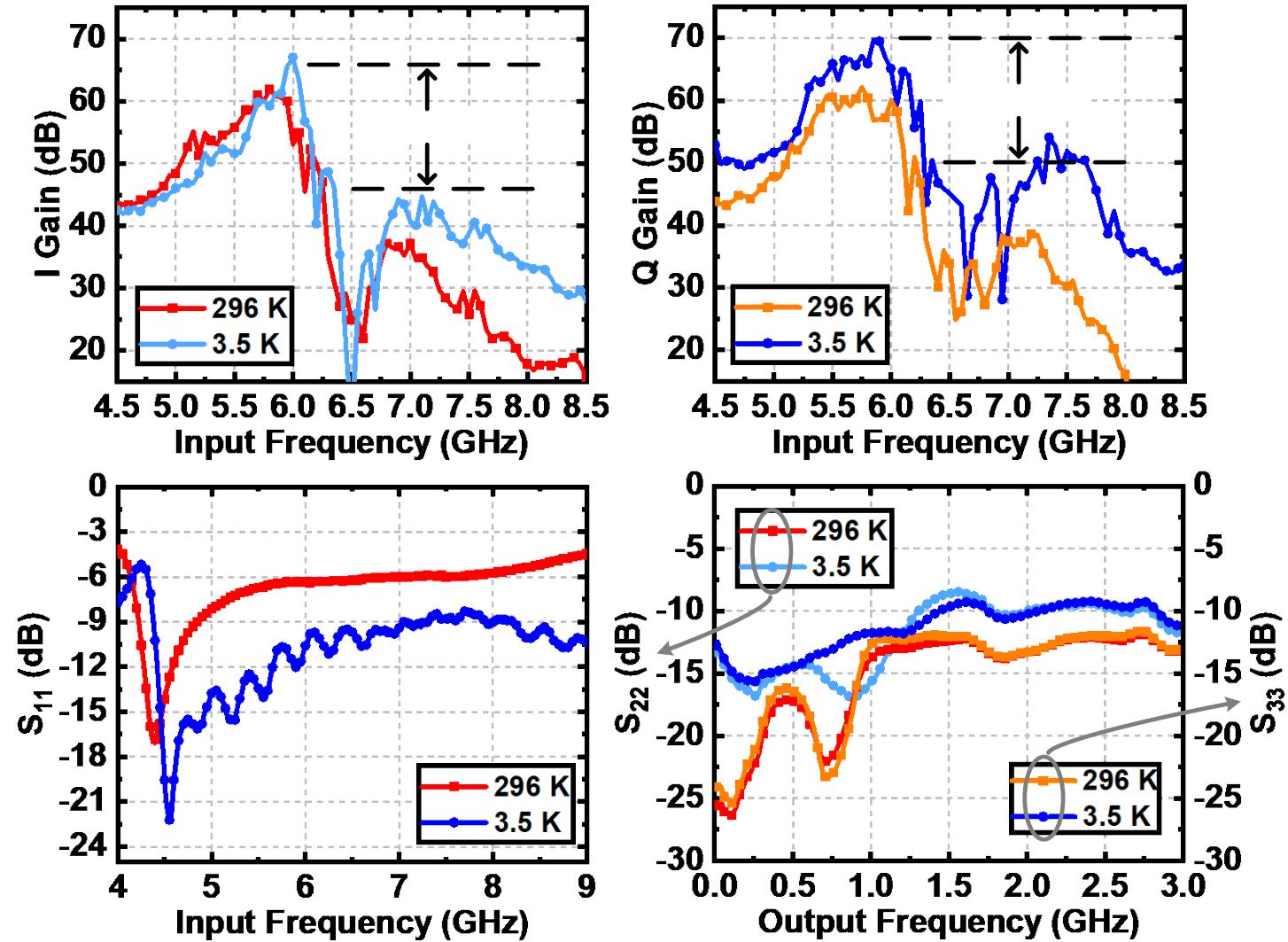


13.2: A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

Receiver gain and matching

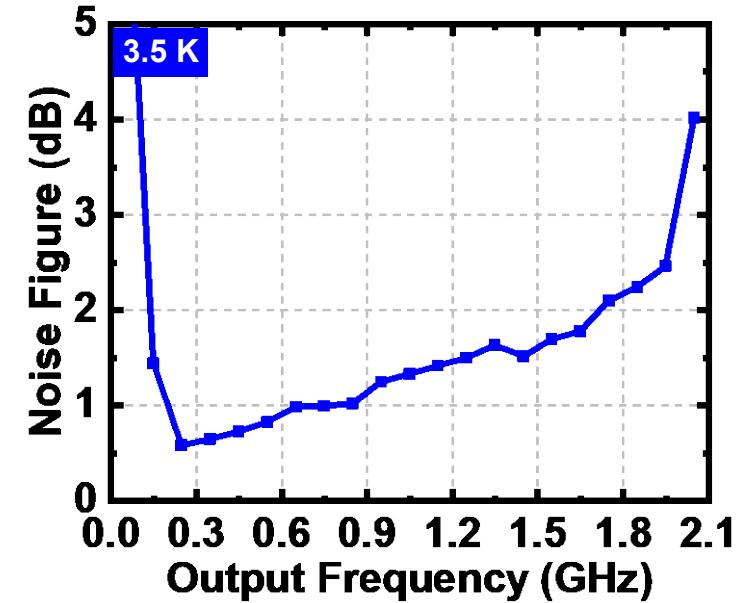
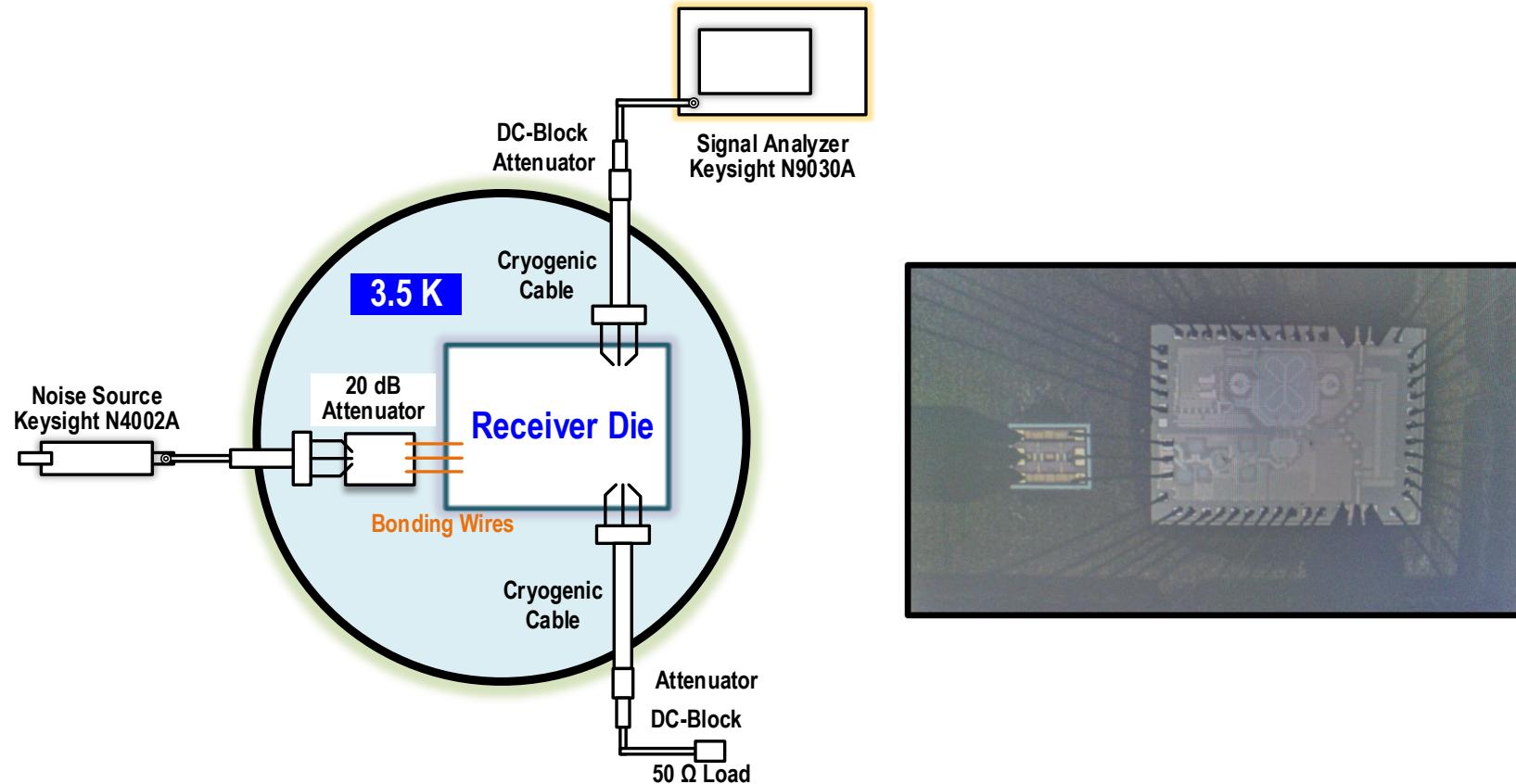


- 70-dB maximum conversion gain
- 1.4 GHz bandwidth
- Average 20-dB image-rejection ratio



13.2: A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

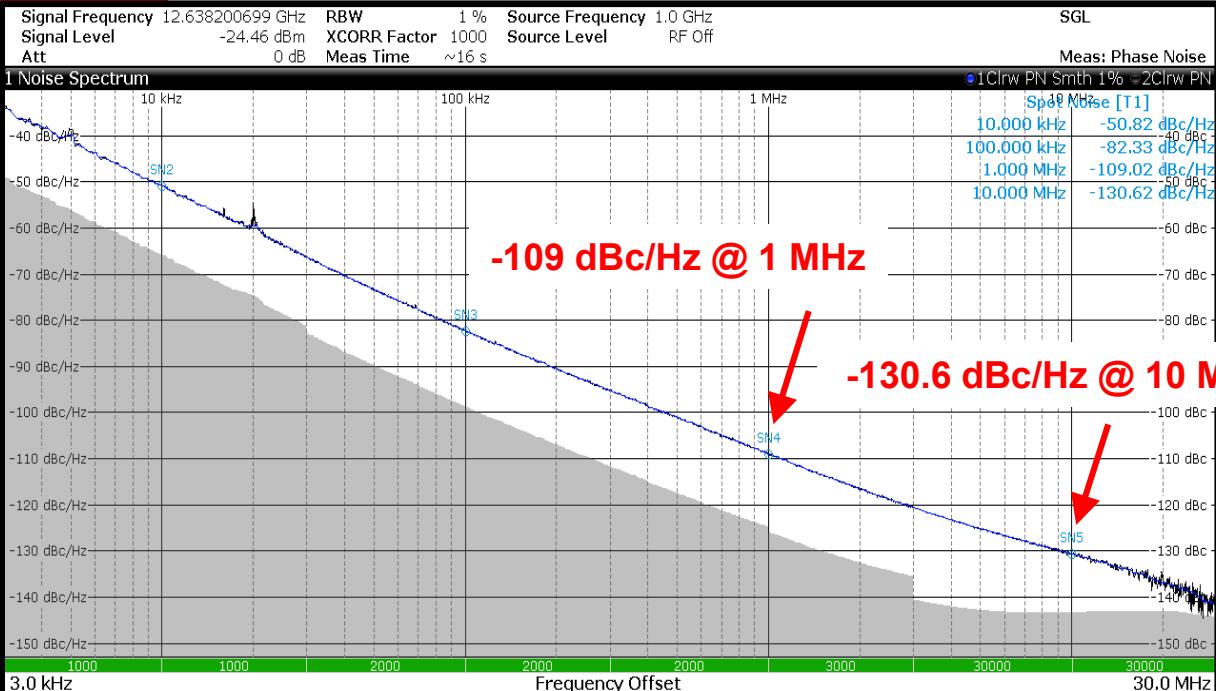
Receiver noise figure



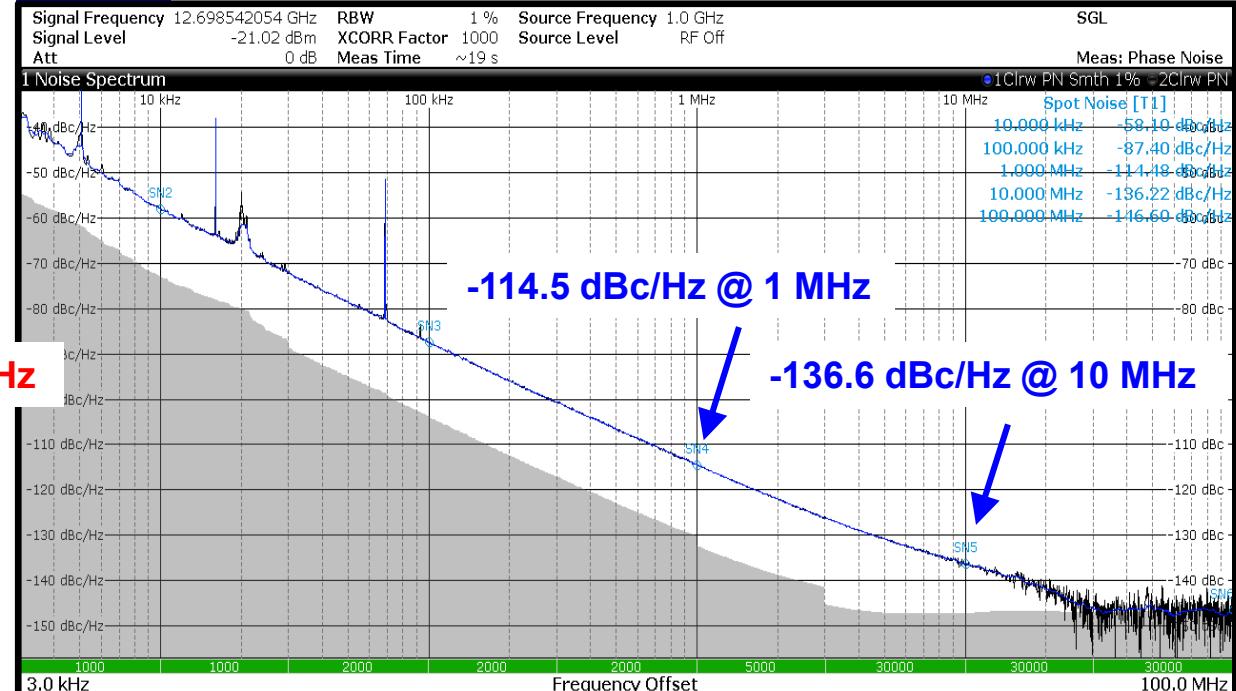
- De-embedded cold attenuator scalar SSB NF measurements
- 0.55 dB minimum noise figure
- Additional cryogenic LNA might be required for direct qubit readout

VCO phase noise

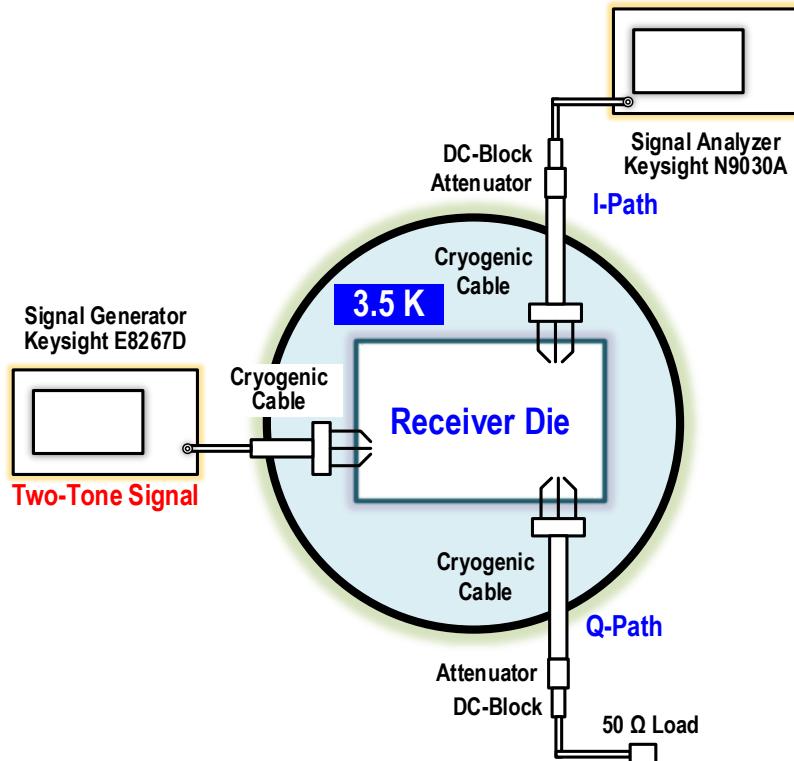
296 K



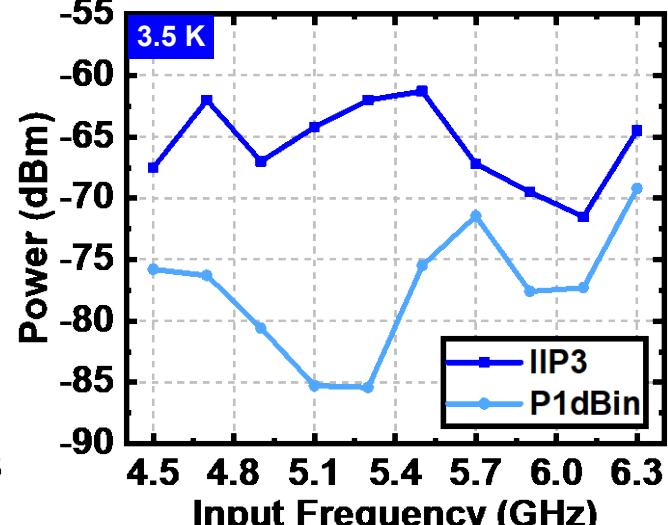
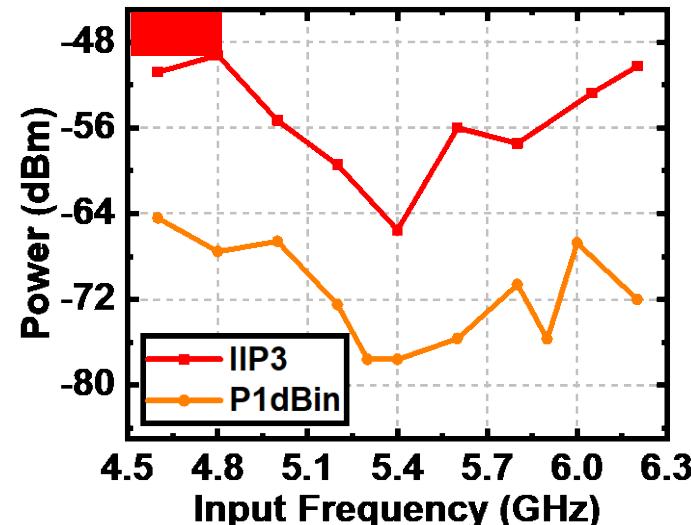
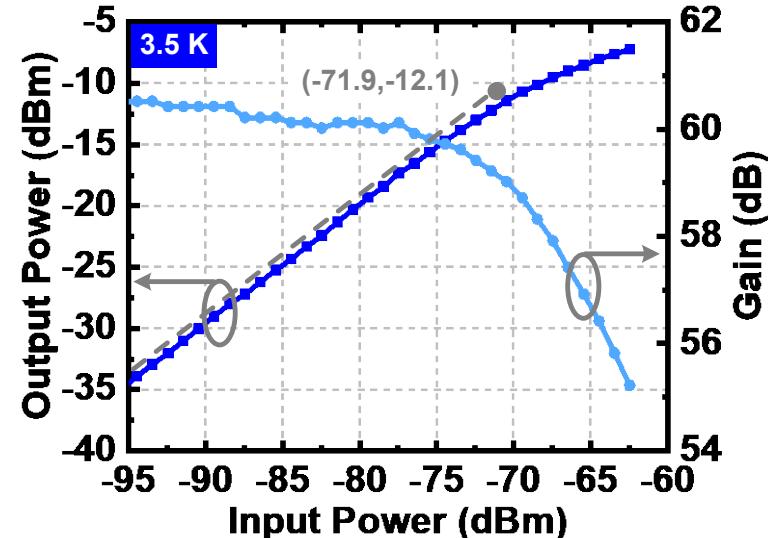
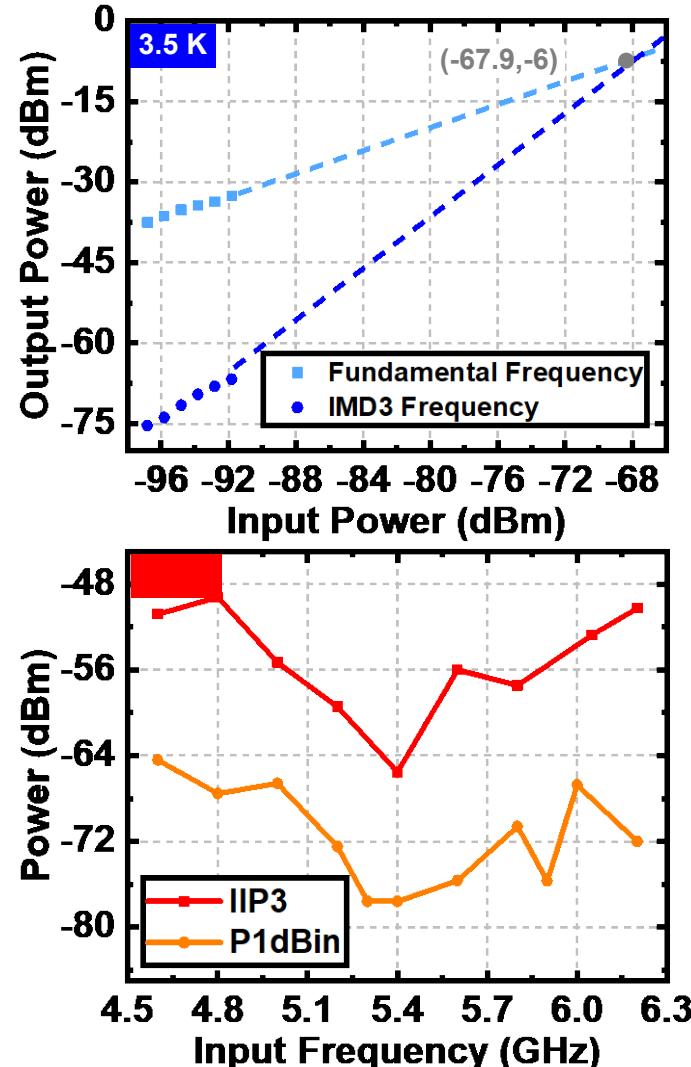
3.5 K



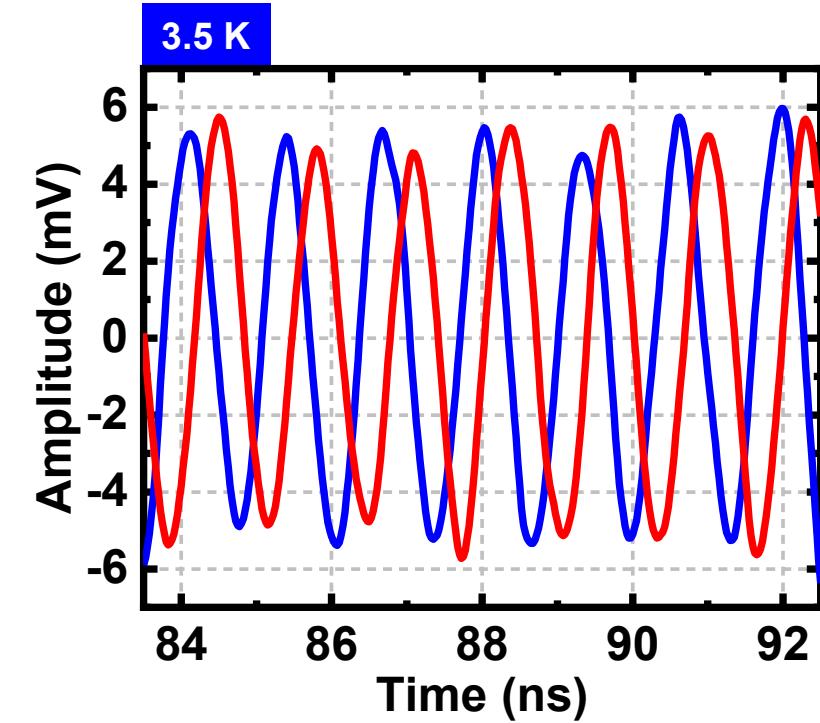
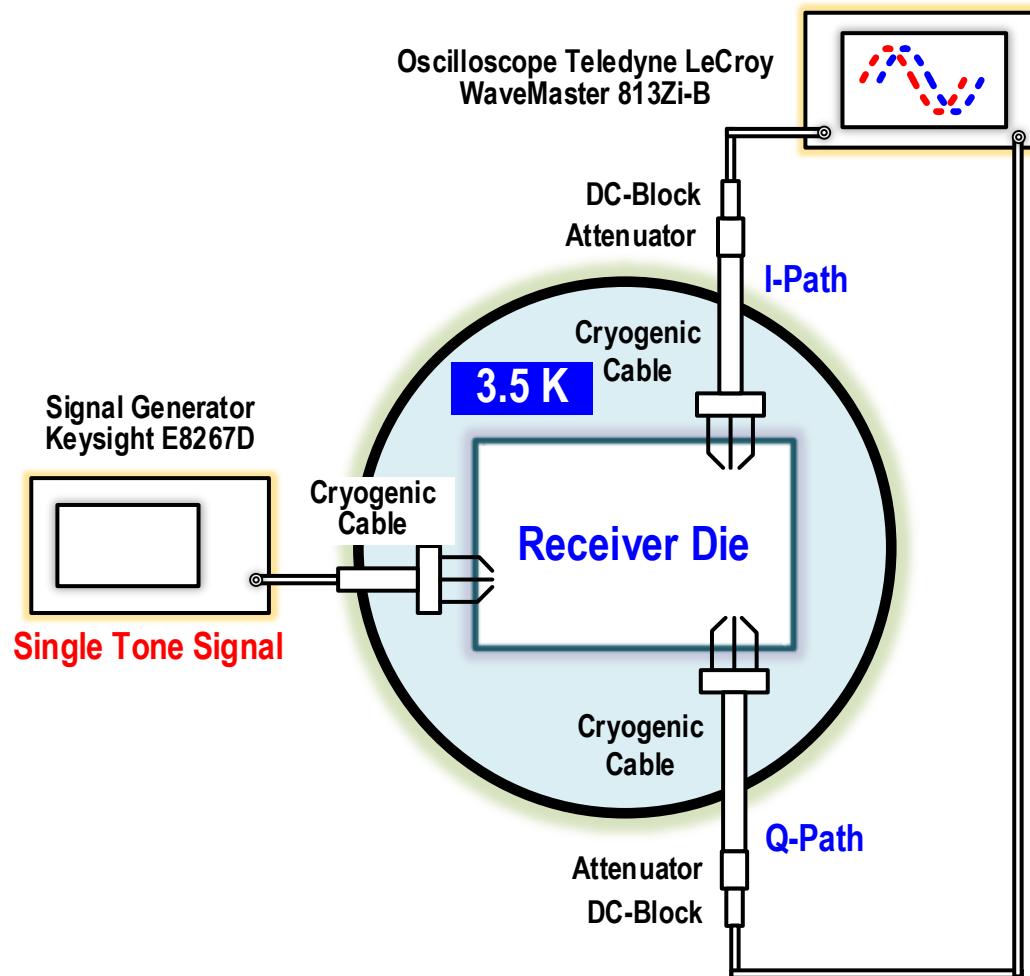
Receiver linearity and compression



- >-72 dBm IIP3 over the bandwidth at 3.5 K
- >-85 dBm P1dB in over the bandwidth at 3.5 K
- Limited by output non-linearity

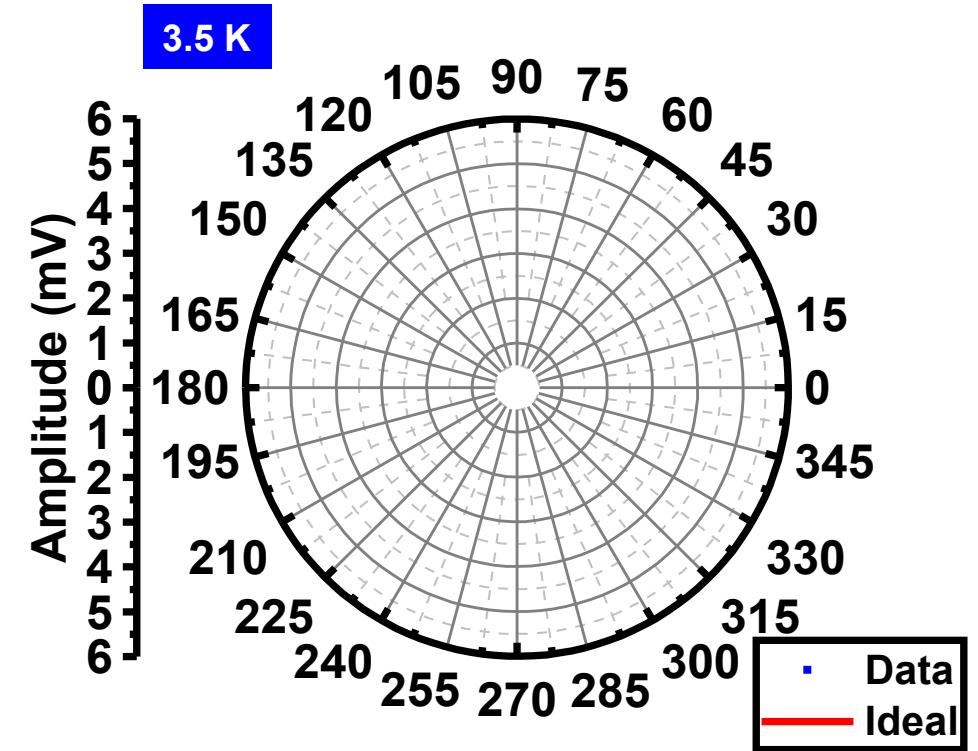
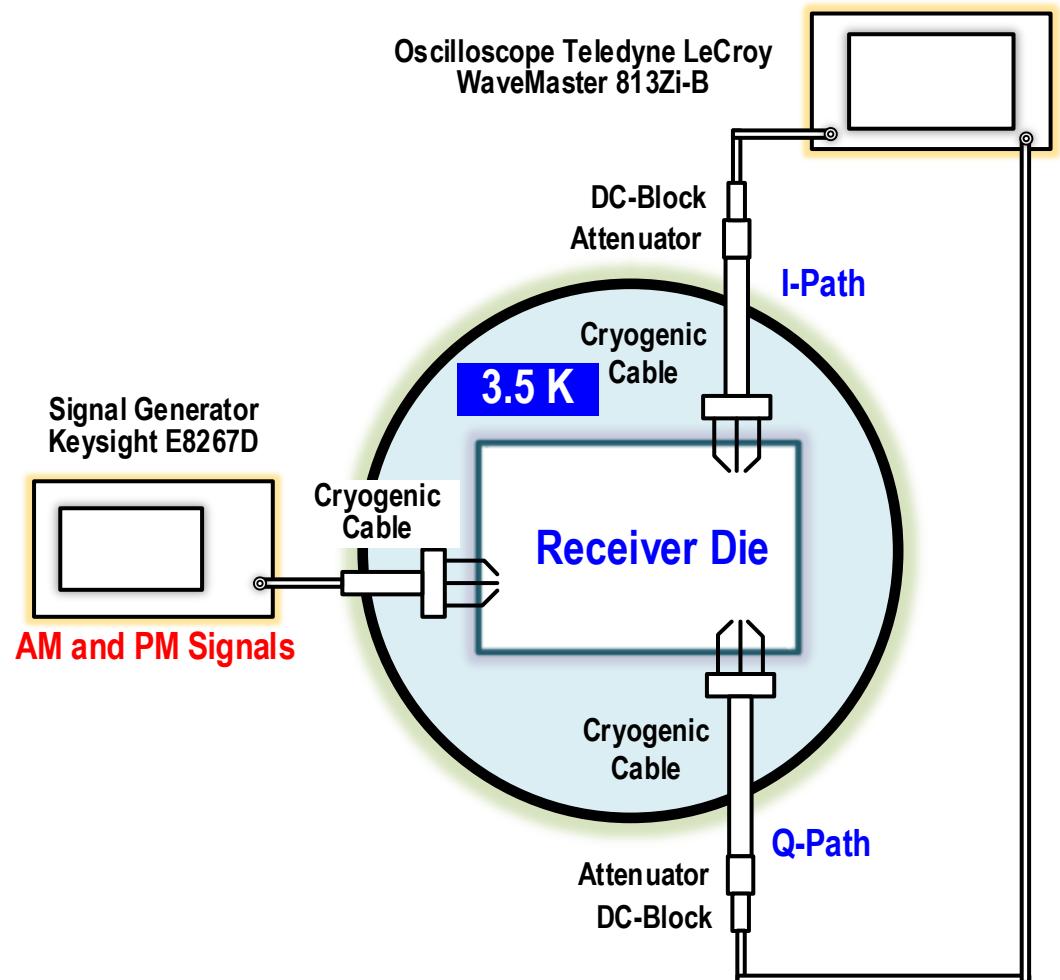


Time-domain I/Q measurements



- 6° phase imbalance at 680 MHz IF frequency from real-time I/Q output waveforms at 3.5 K

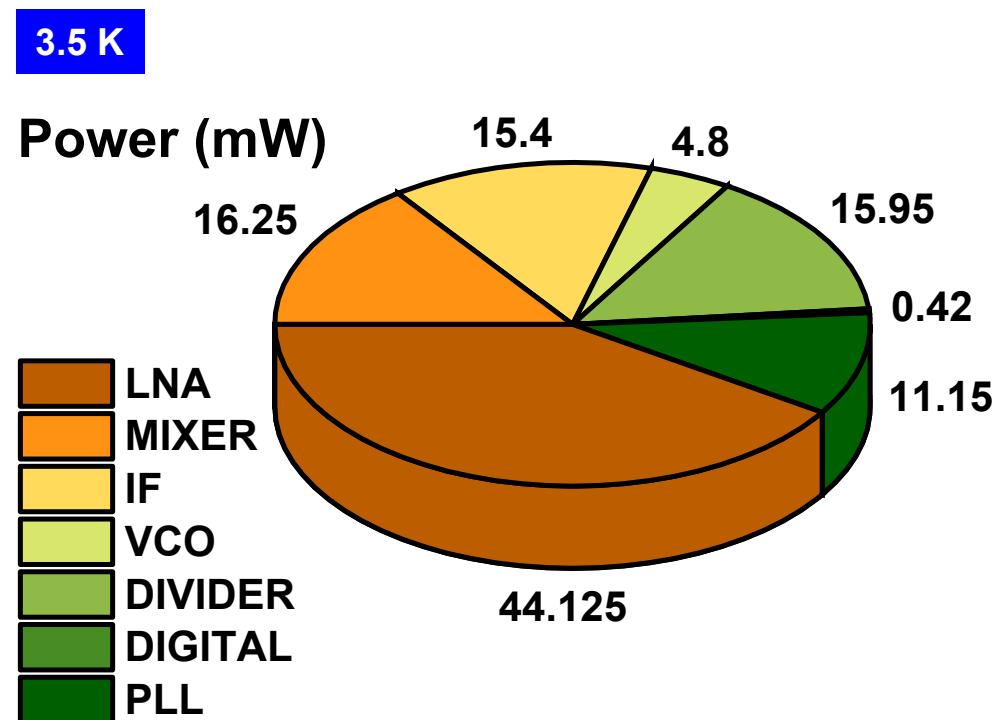
Receiver polar constellation diagram



- The I/Q receiver tracks the linear AM and PM input signal in the output polar constellation plot

Power consumption

- The chip consumes 108 mW at 3.5 K
- With 1.4 GHz bandwidth, 10 MHz qubit bandwidth, 10 MHz spacing, one can read 70 qubits with 1.5 mW/qubit

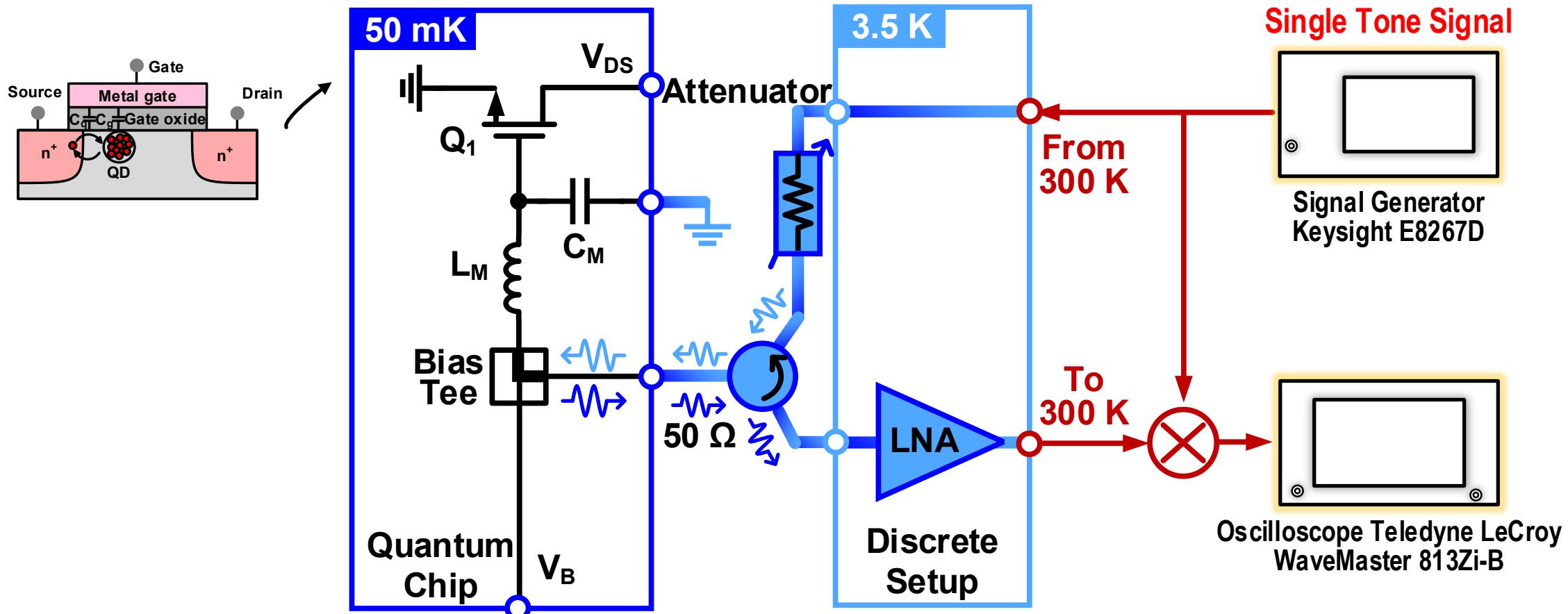


Comparison table

| | This work | [13] ISSCC 2020 | [14] MWCL 2020 | [15] RSI 2014 |
|------------------------------------|------------------------------|----------------------------------|------------------------------------|----------------------------|
| Operating temperature | 3.5 K | 0.11 K | 300 K | 100 K |
| Qubit platform | Spin qubits, transmons | Silicon quantum dots | Si/SiGe spin qubits | N.A. (Radio astronomy) |
| Architecture | Intermediate IF I/Q receiver | DC TIA readout | Intermediate IF I/Q down-converter | Discrete receiver |
| System | Full receiver, PLL | Double quantum dot, VCO, TIA | Down-converter, VCO, divider | Antenna, LNA, feedthroughs |
| RF Frequency | 5-6.5 GHz | DC | 240 GHz | 0.4-3 GHz |
| Bandwidth | 1.4 GHz | 1.1 kHz | 59 GHz | 2.6 GHz |
| Gain | 70 dB | ¹ 11.3 MΩ | 23 dB | 34 dB |
| Input/output match | < -10 dB | N.A. | < -5 dB | N. R. |
| Noise figure | 0.55 dB | ² 300 fA/√Hz | 24.5 dB | 0.5 dB |
| IIP3 | > -72 dBm | N.R. | N.R. | N. R. |
| P1dBin | > -85 dBm | N.R. | -27.3 dBm | N. R. |
| Phase noise at 1 MHz offset | -115 dBc/Hz | N.R. | -82 dBc/Hz | N.A. |
| VCO tuning range | 6 GHz | 4 GHz | 27 GHz | N.A. |
| Technology | 40-nm CMOS | 28-nm FDSOI | 55-nm SiGe | GaAs HEMT, discrete |
| Area | 2.8 mm ² | ³ 1.4 mm ² | 1.8 mm ² | > 1 m ² |
| Power consumption | 108 mW | 295 μW | 859 mW | N. R. |

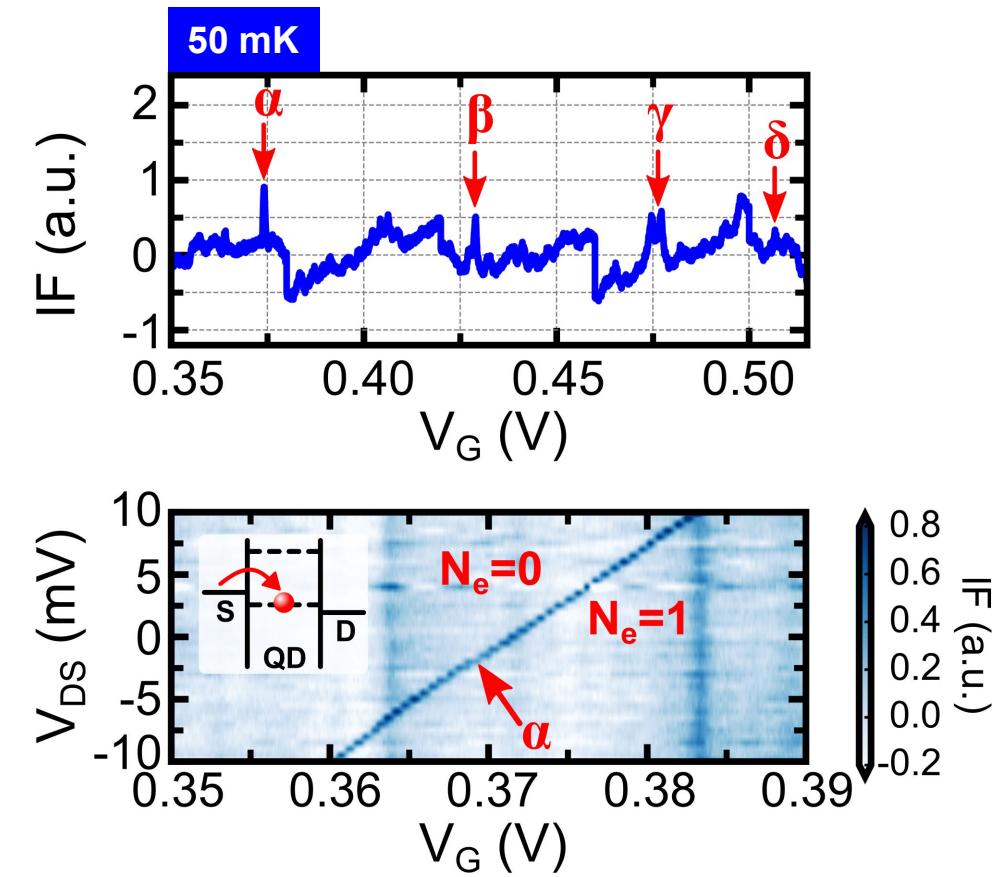
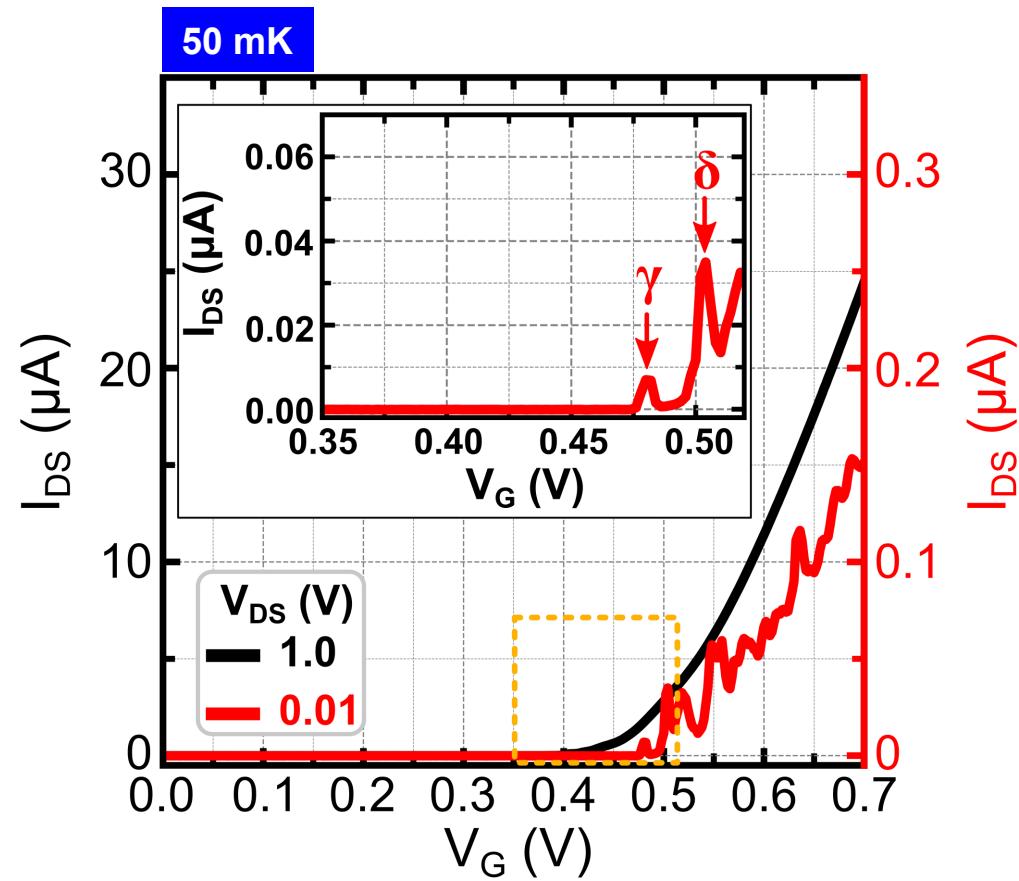
¹Transimpedance amplifier gain, ²Input referred noise, ³Estimated from chip micrograph

RF reflectometry of quantum dots



- As an application of the receiver, quantum dots co-integrated with a lumped LC resonator in standard 40-nm CMOS have been measured in RF reflectometry by a discrete setup

Discrete RF reflectometry results



- At 50 mK, the 40-nm CMOS quantum dots show regular Coulomb oscillations in DC, which can also be resolved in RF reflectometry

Conclusion

- First cryogenic CMOS system-on-chip with receiver and frequency synthesizer for scalable gate-based reflectometry of silicon quantum dots
- Wideband 5-6.5 GHz architecture for multiplexed readout
- 70 dB maximum gain, 0.55 dB noise figure, 108 mW power

Acknowledgements

The authors would like to acknowledge the EUROPRACTICE MPW and design tool support.

The authors would like to thank Adrien Toros from EPFL for his help with chip bonding and packaging.

Thank you for your attention!

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- [2] Ristè et al., Nature Communications 6, 6983 (2015)
- [3] Matthews et al., Nature Photonics 3, 346-350 (2009)
- [4] Kim, Physics 7, 119 (2014)
- [5] Robledo et al., Nature 477, 574-578 (2011)
- [6] Ladd et al., Nature 464, 45-53 (2010)
- [7] Maurand et al., Nature Communications 7, 13575 (2016)
- [8] Bardin et al., ISSCC 2019
- [9] Charbon et al., ISSCC 2017
- [10] Yang et al., EDL 2020
- [11] Beckers et al., ESSDERC 2017
- [12] Patra et al., JEDS 2020
- [13] Le Guevel et al., ISSCC 2020
- [14] Alakusu et al., MWCL 2020
- [15] Gawande et al., RSI 2014

A 6-to-8GHz 0.17mW/Qubit Cryo-CMOS Receiver for Multiple Spin Qubit Readout in 40nm CMOS Technology

Bagas Prabowo^{1,2}, Guoji Zheng^{1,2}, Mohammadreza Mehrpoo^{1,3},
Bishnu Patra^{1,2}, Patrick Harvey-Collard^{1,2}, Jurgen Dijkema^{1,2},
Amir Sammak⁴, Giordano Scappucci^{1,2}, Edoardo Charbon^{1,2,5},
Fabio Sebastiano^{1,2}, Lieven M. K. Vandersypen^{1,2}, Masoud Babaie^{1,2}

¹Delft University of Technology, Delft, The Netherlands,

²QuTech, Delft, The Netherlands, ³Now with Broadcom Netherlands, Bunnik, The Netherlands, ⁴TNO, Delft, The Netherlands, ⁵EPFL, Neuchatel, Switzerland



Self Introduction

- Bachelor in Electrical Engineering from University of Twente, in 2018.
- Master in Electrical Engineering from TU Delft, in 2020.
- Currently pursuing PhD at TU Delft focusing on cryogenic electronics for Quantum Computers.



Outline

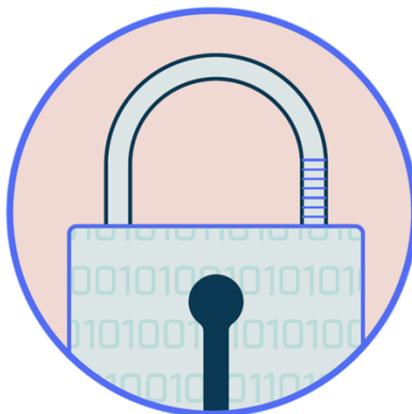
- Introduction
- Spin-Qubit Readout
- System Architecture
- Electrical Performance
- Spin-Qubit Readout Experiment
- Conclusions

Outline

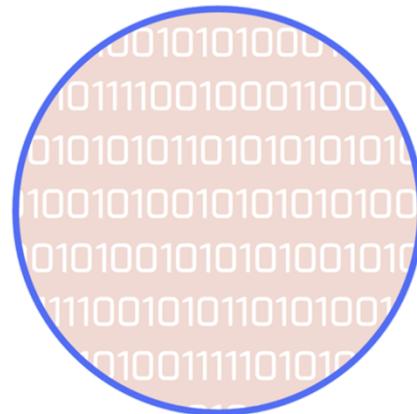
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Why Quantum Computing?

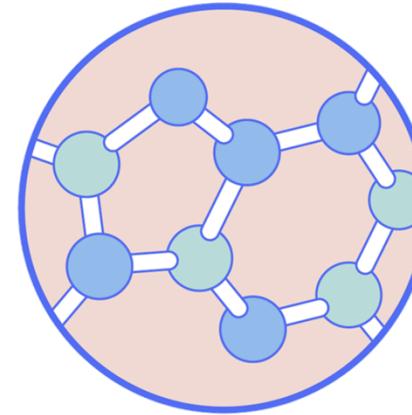
Encryption



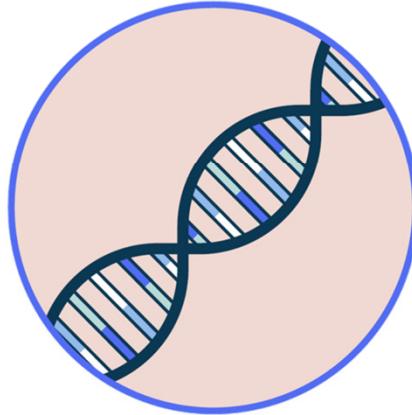
Big Data



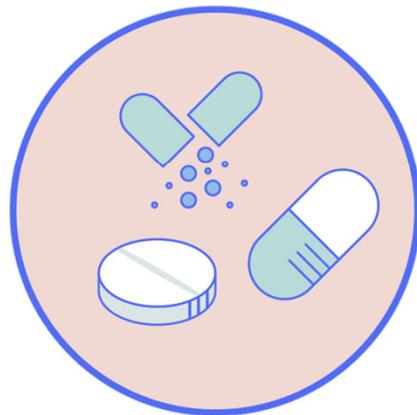
Molecule Simulation



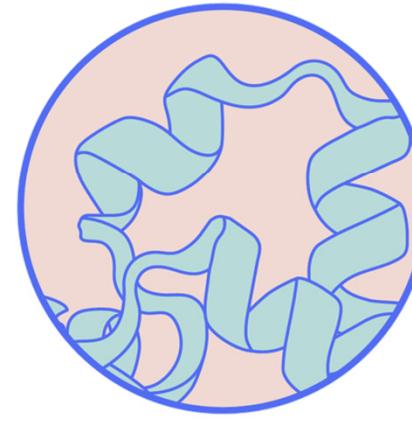
DNA Analysis



Drug Synthesis

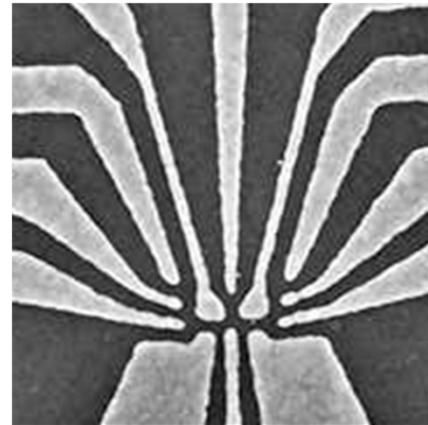


Protein Folding



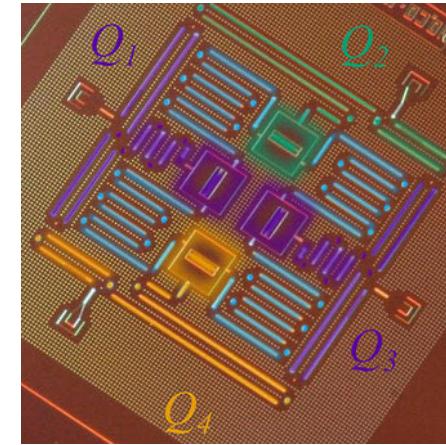
The Solid-State Qubits

Semiconductor
Qubits



[L.M.K. Vandersypen, M. Eriksson,
Physics Today'19]

Superconducting
Qubits

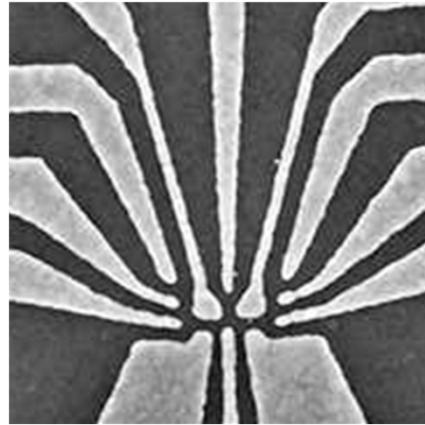


[M. Kjaergaard, arxiv'19]

| | | |
|-------------------------------|-----------------------|-----------------------|
| Temperature | 0.01-1K | 0.01K |
| Qubit Pitch | ~ 100 nm | ~ 100 μm |
| # Qubit/mm² | 10⁸ | 10² |

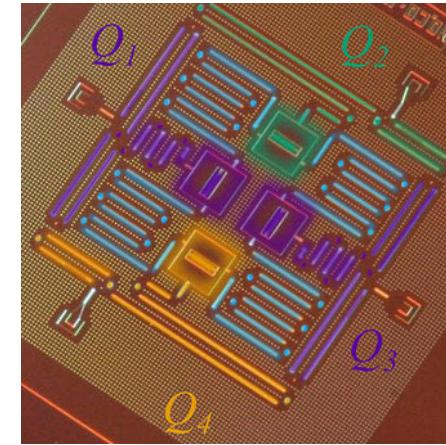
The Solid-State Qubits

Semiconductor
Qubits



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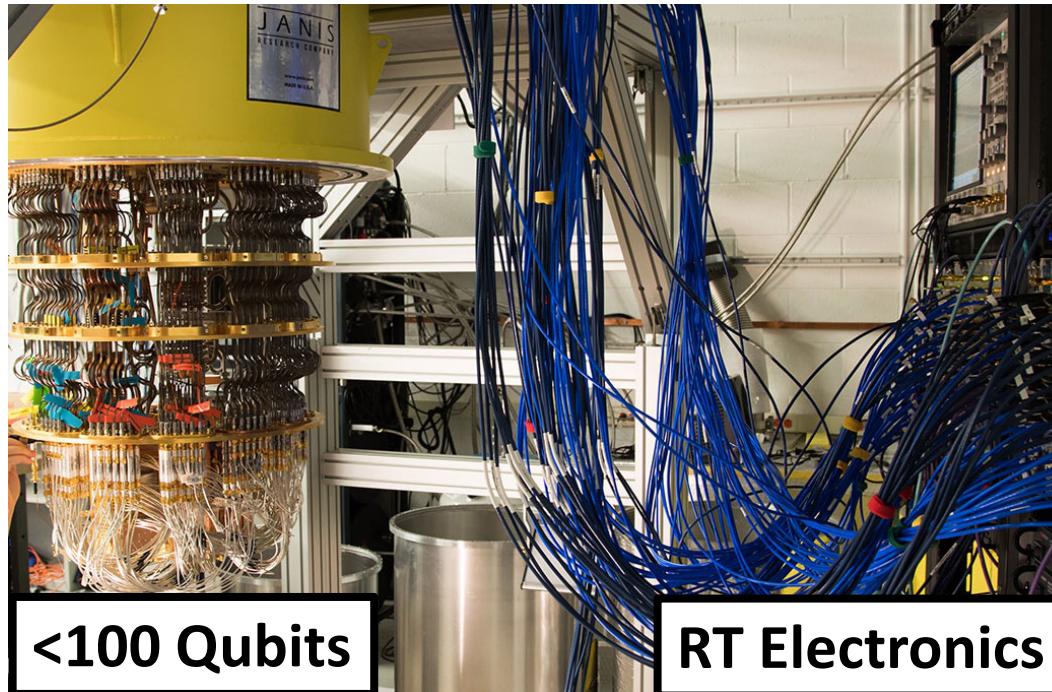


[M. Kjaergaard, arxiv'19]

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|-------------------------|-----------------------|-----------------------|
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State-of-the-art Solution

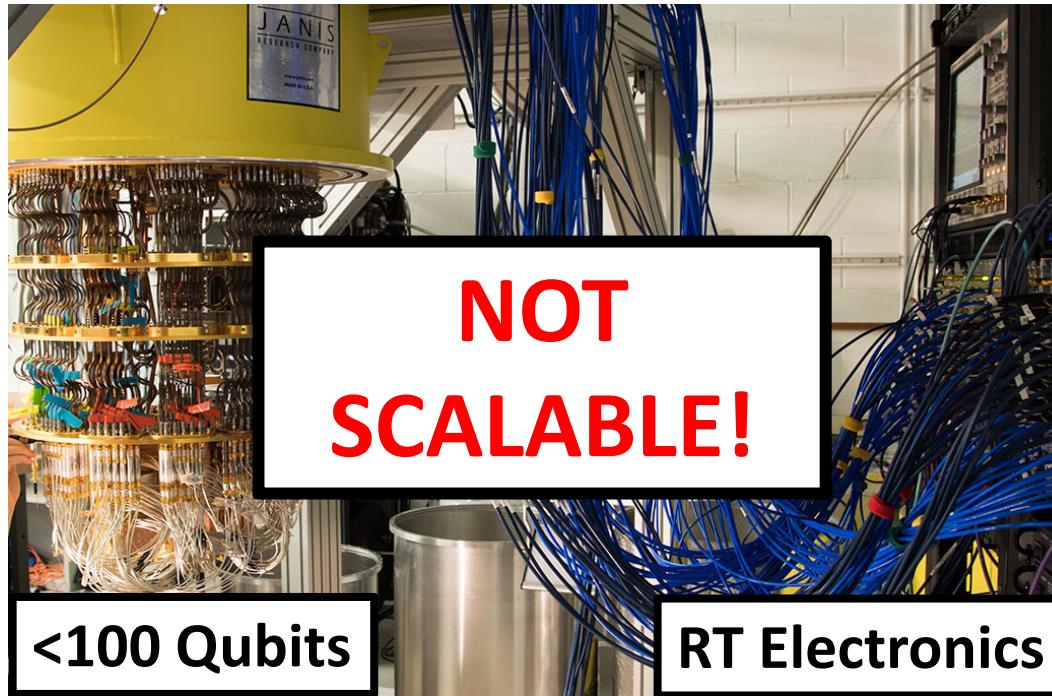
- Scalability issues to large scale QC
 - # Interconnects
 - Control/readout latency



[F. Arute, Nature'19]

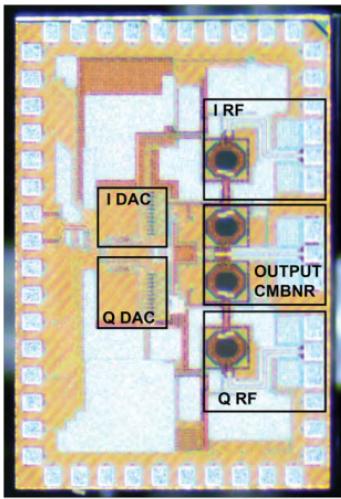
State-of-the-art Solution

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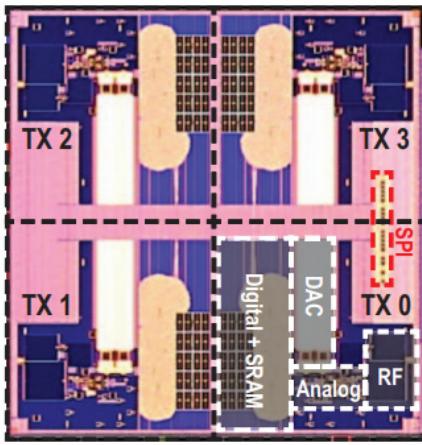


Towards Large Scale QC

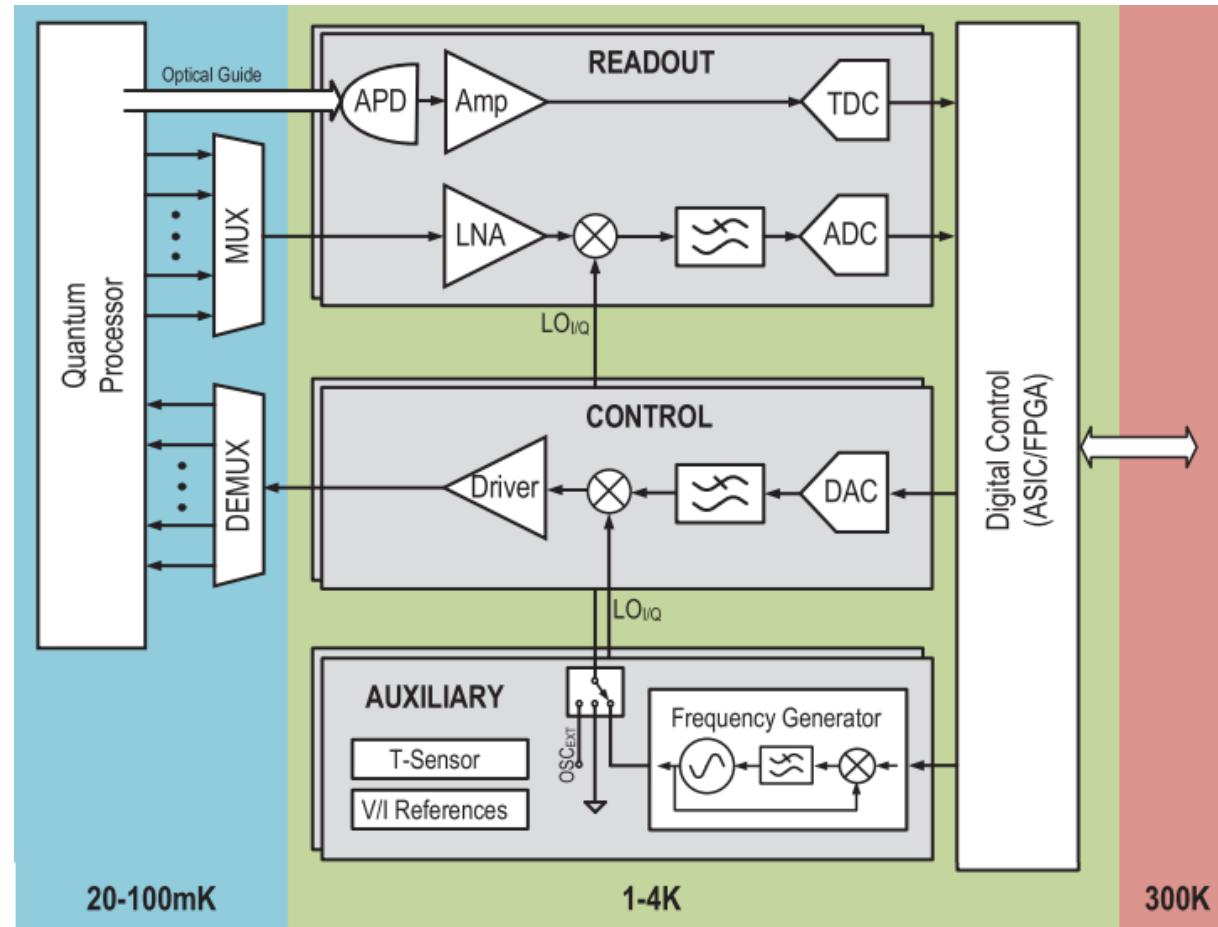
Cryogenic Qubit Control



[J. Bardin, ISSCC'19]

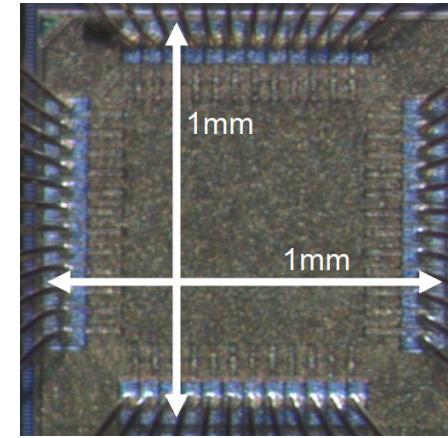


[B. Patra, ISSCC'20]



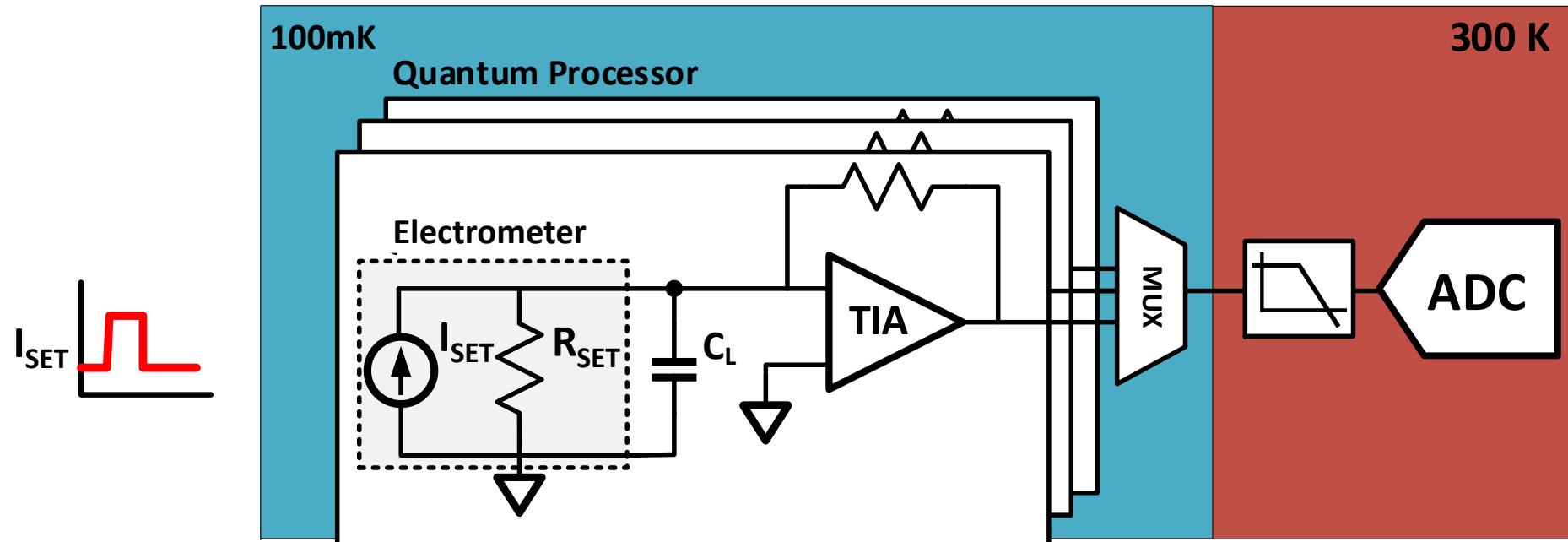
[E. Charbon, ISSCC'17]

DC Qubit Readout



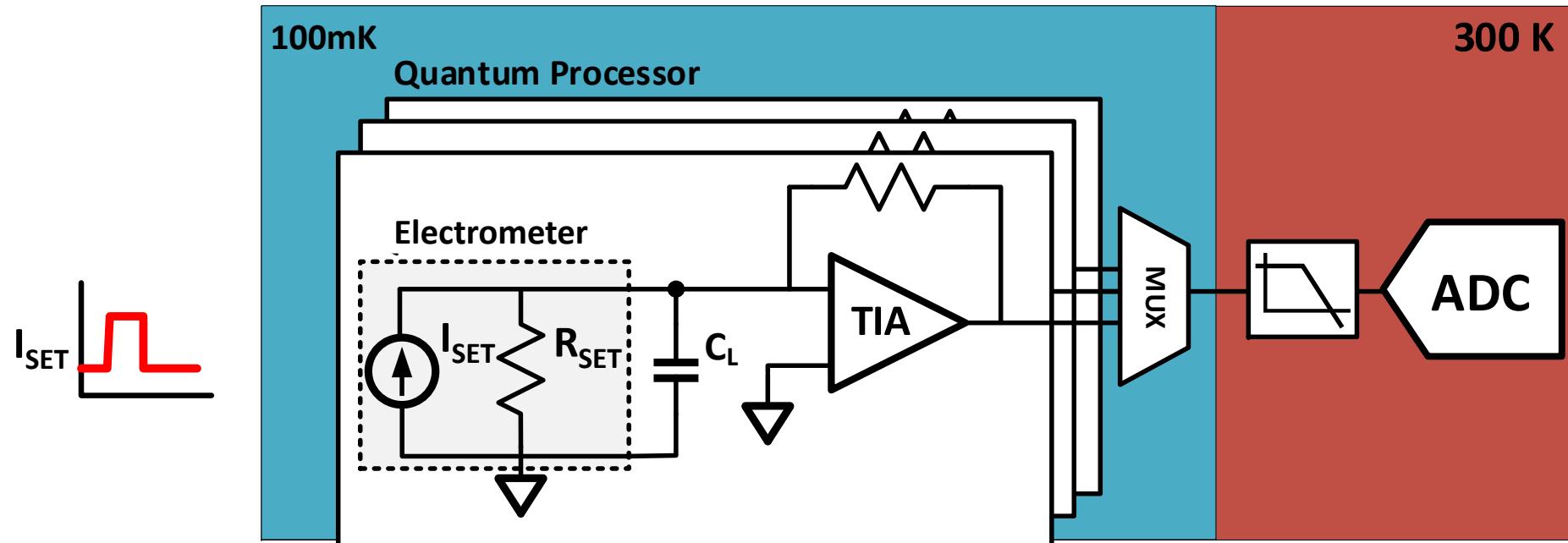
[L. Le Guevel, ISSCC'20]

DC Readout – State-of-the-Art



- Integration at 100 mK stage [L. Le Guevel, ISSCC'20]
- Small area (0.01 mm^2)
- Low power ($1\mu\text{W/qubit}$)
- Sensitive to $1/f$ noise
- Slow readout time $\rightarrow 1 \text{ ms}$
- 1mW cooling power at mK stage

DC Readout – State-of-the-Art



- Integration at 100 mK stage [L. Le Guevel, ISSCC'20]

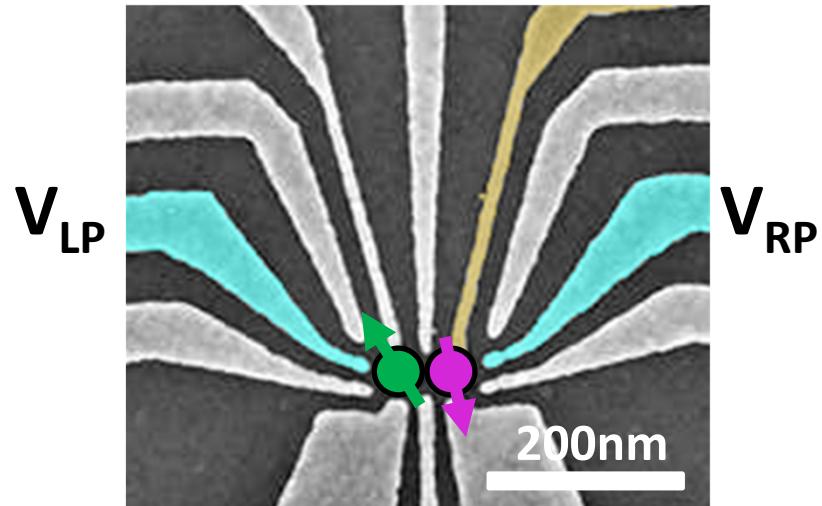
RF Gate-based readout with FDMA

Outline

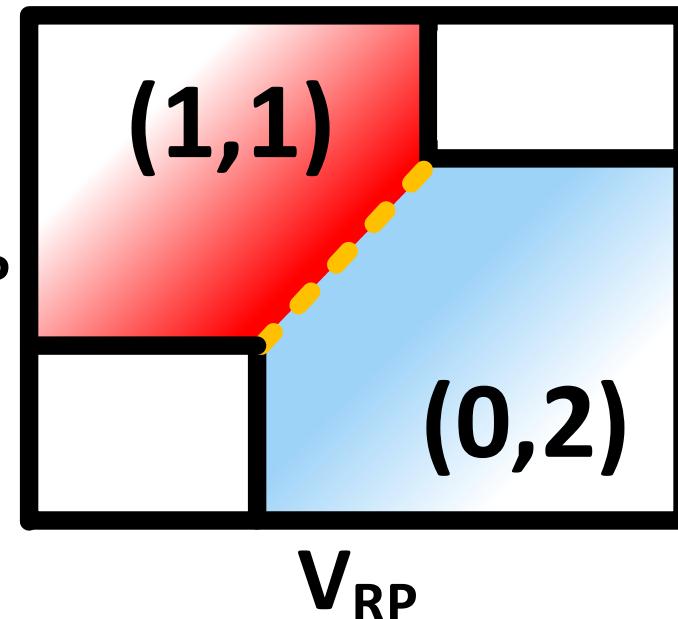
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Gate-based Readout – Physics

Double Quantum Dot
(DQD)

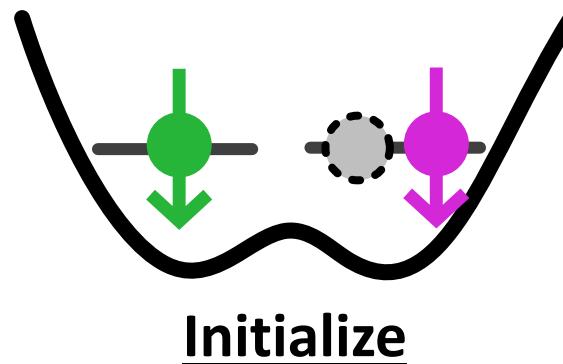
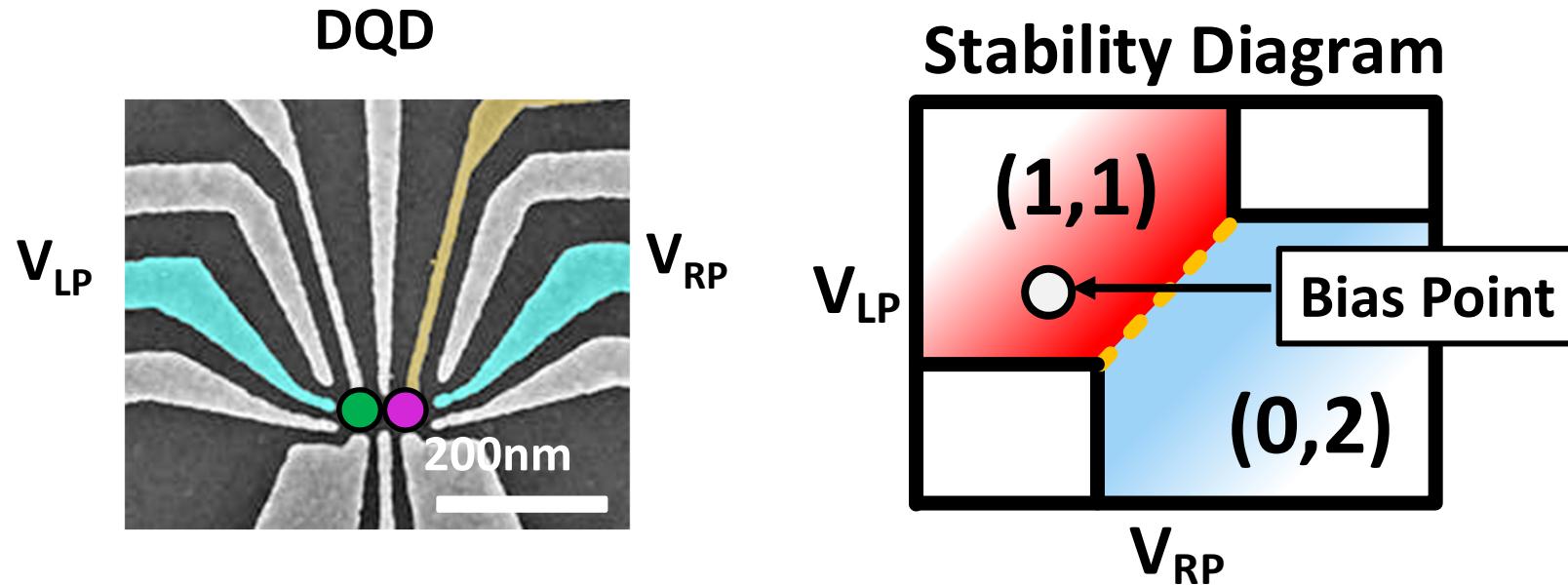


Stability Diagram

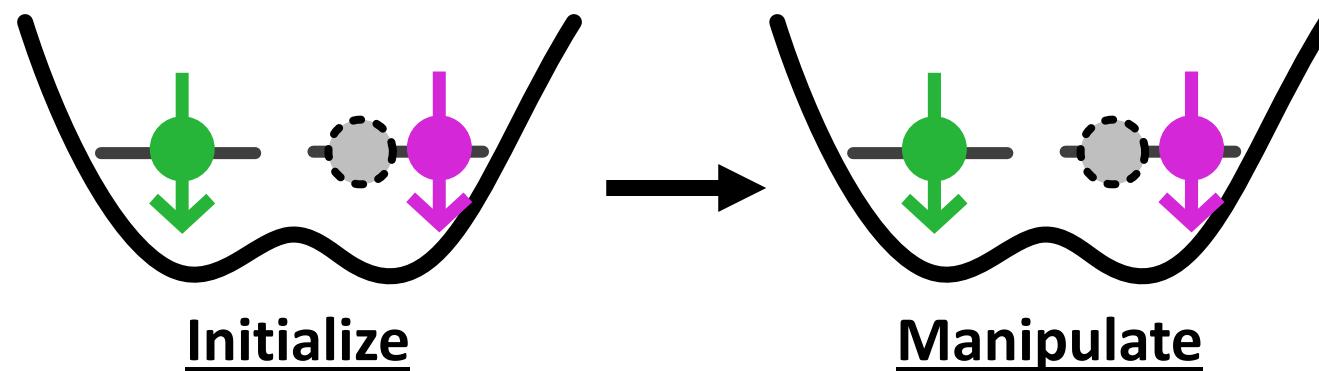
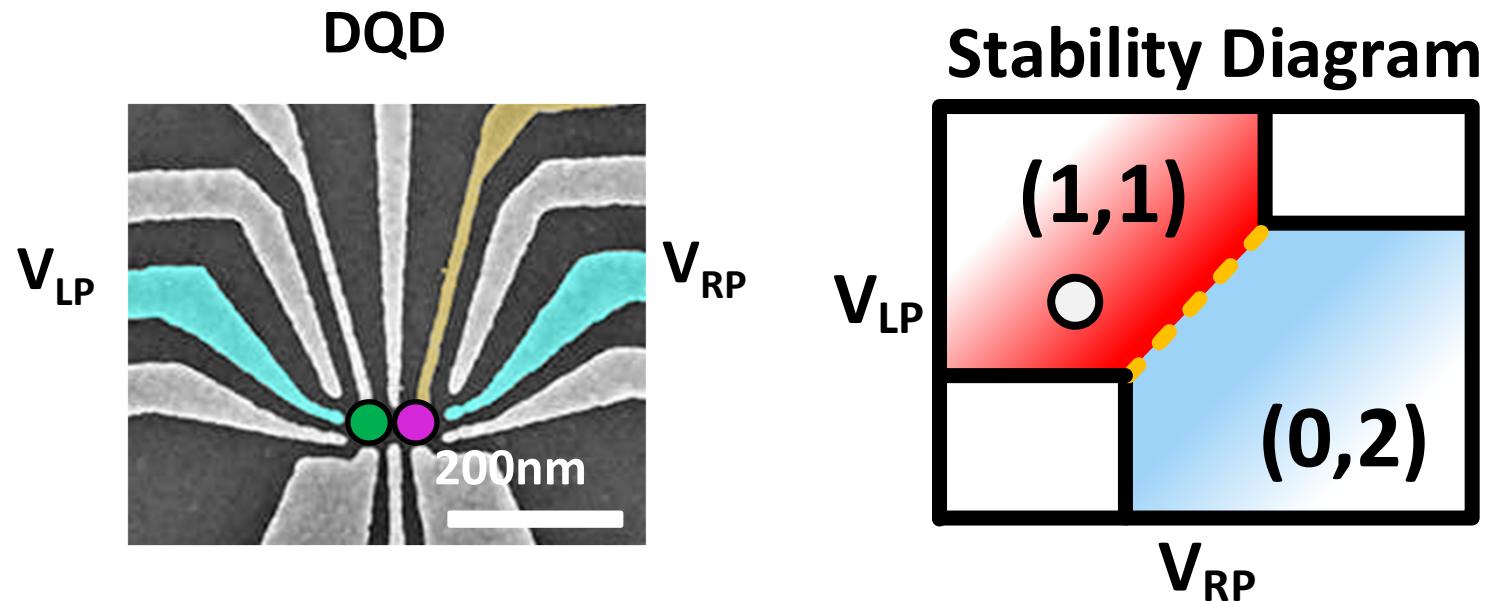


- Behavior of double quantum dot → dependent on biasing
- (N_L, N_R) → Electron population
- Spin qubit → Biased at $(1,1)$ - $(0,2)$ charge regime

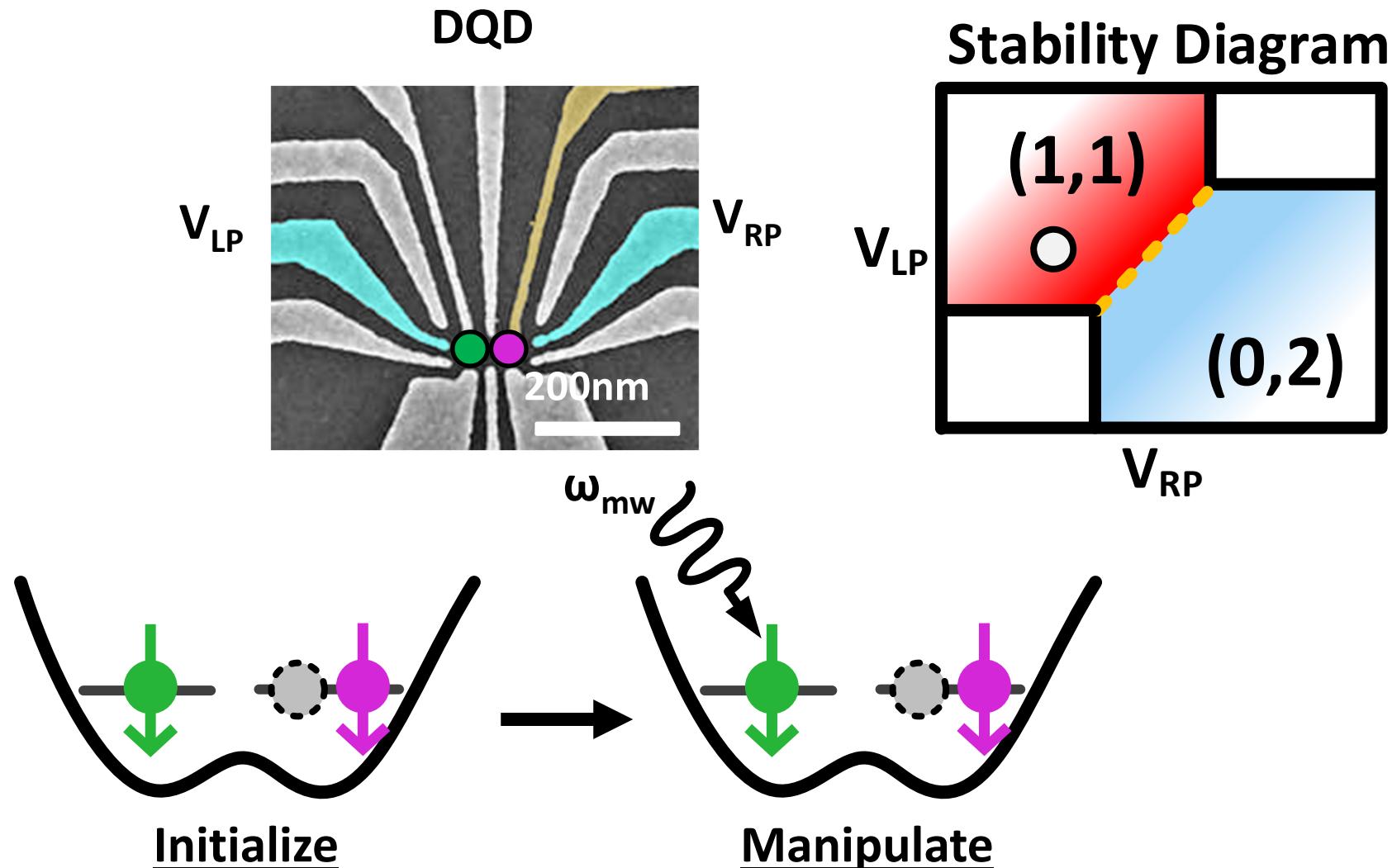
Gate-based Readout – Physics



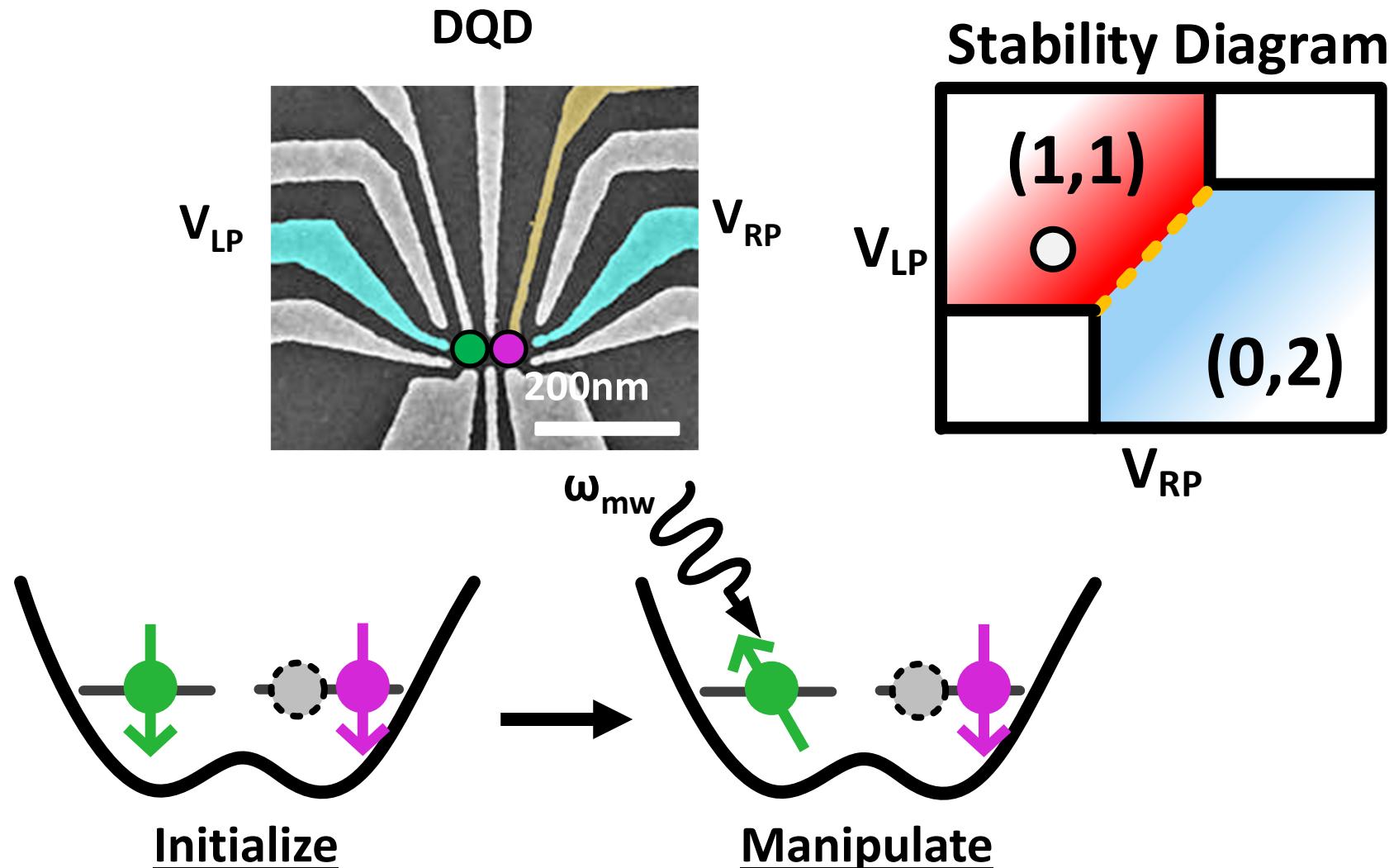
Gate-based Readout – Physics



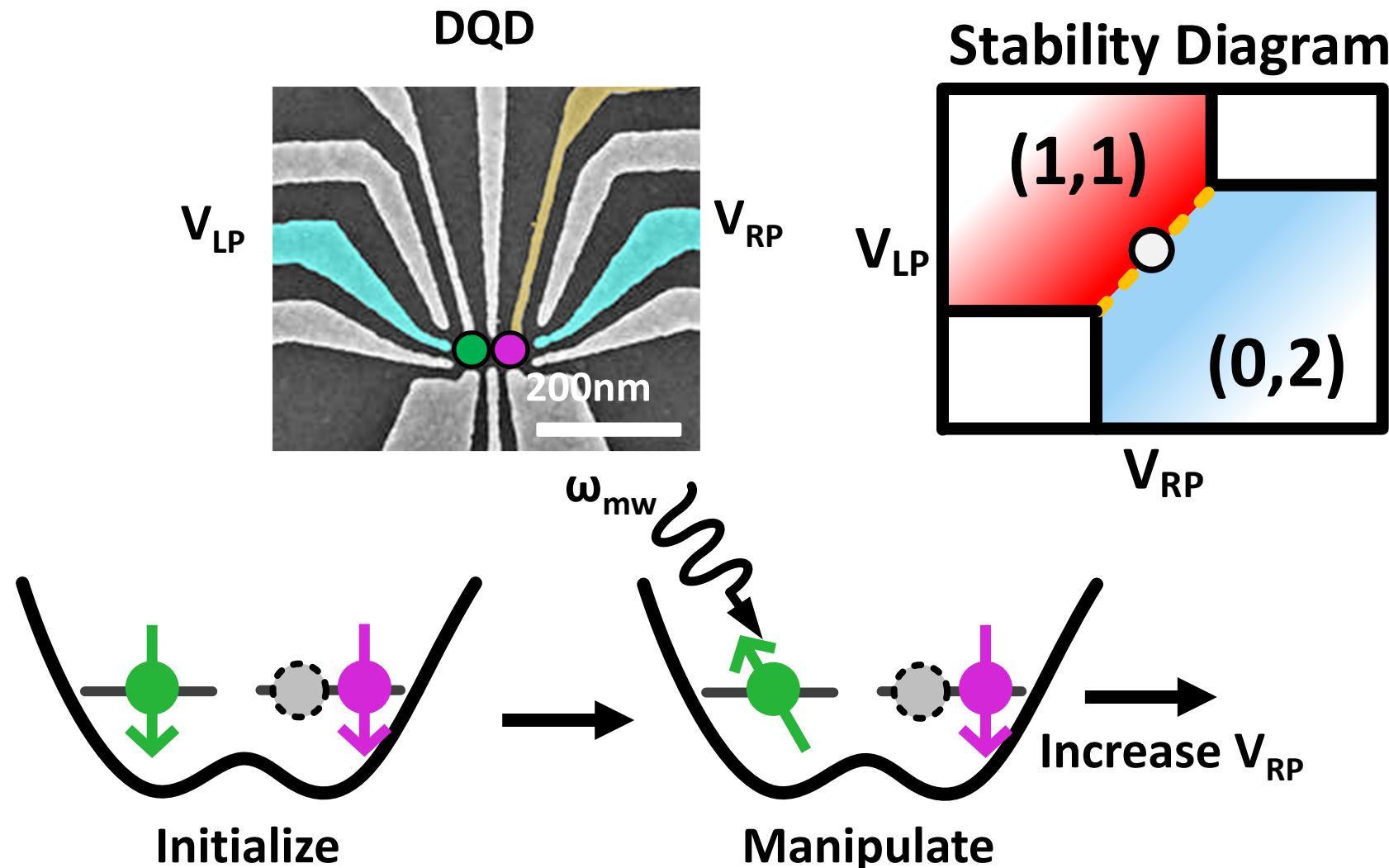
Gate-based Readout – Physics



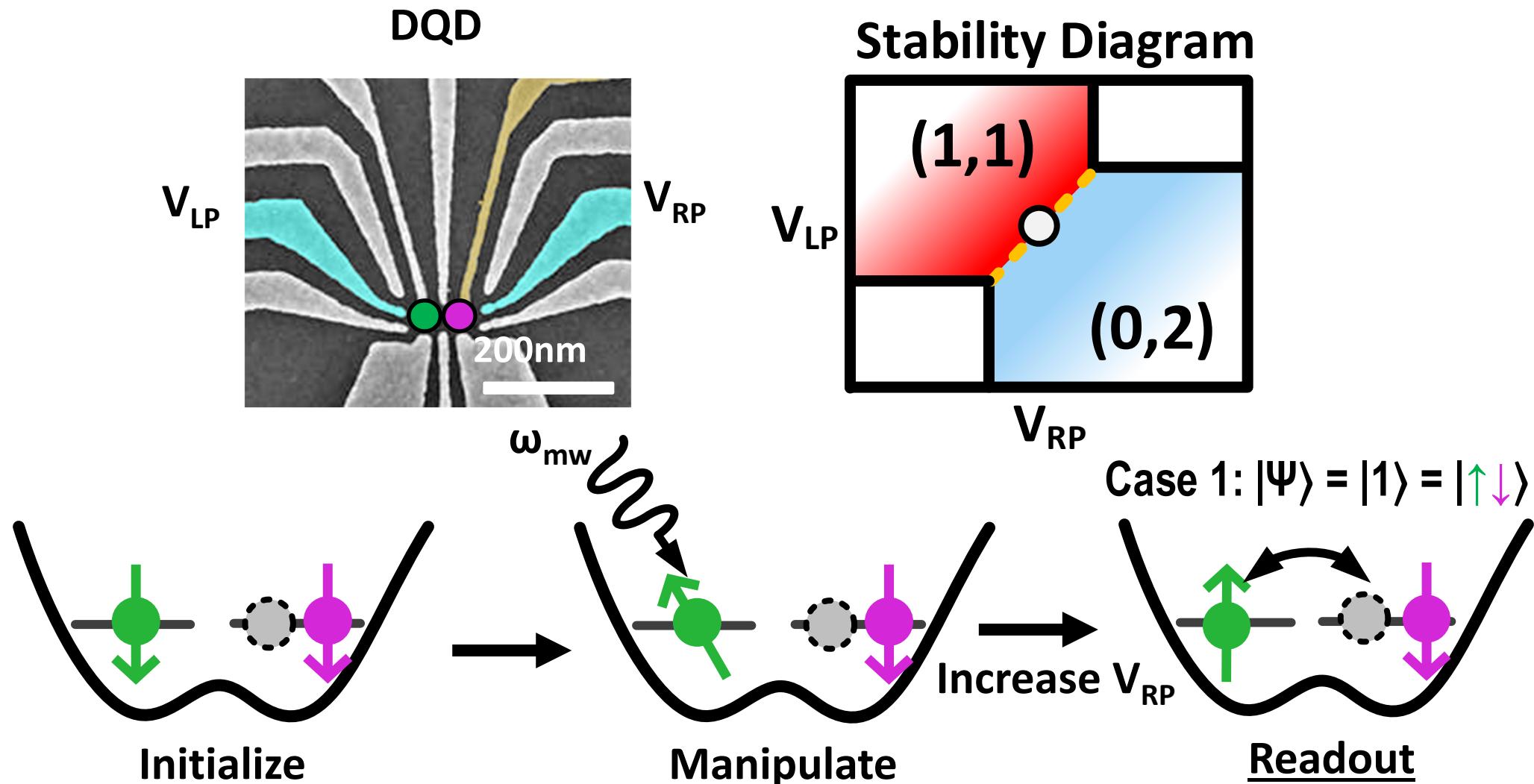
Gate-based Readout – Physics



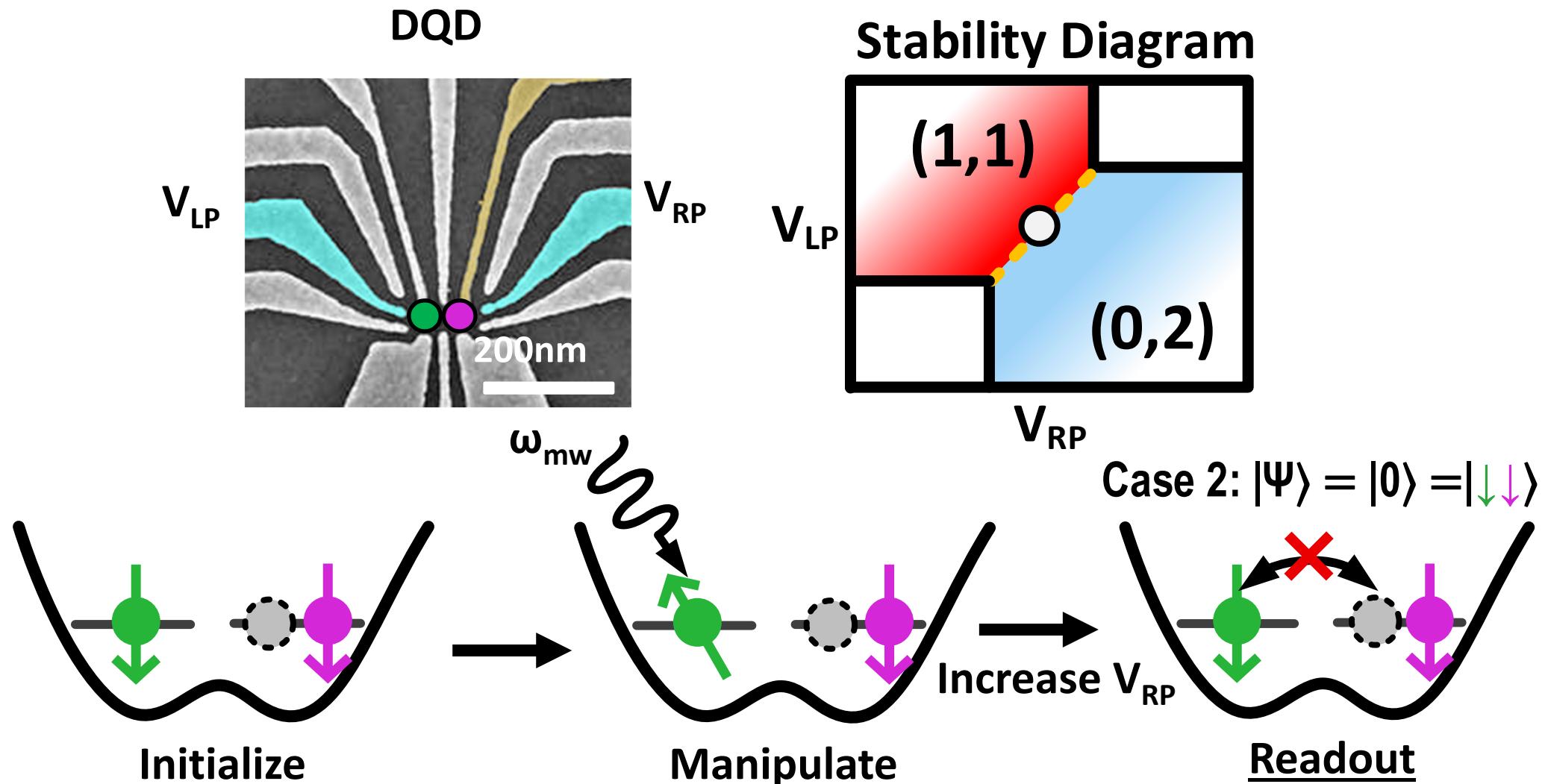
Gate-based Readout – Physics



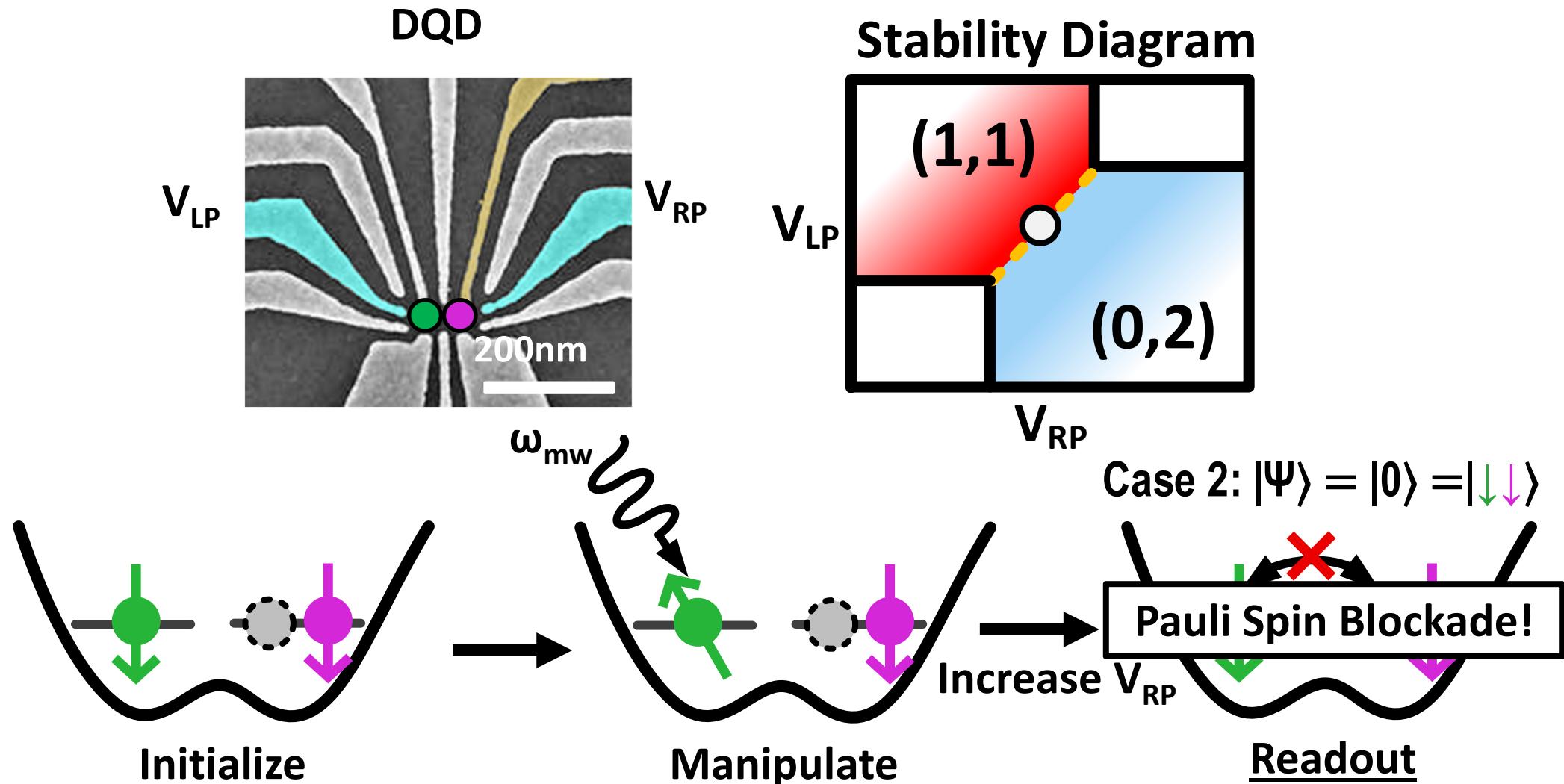
Gate-based Readout – Physics



Gate-based Readout – Physics



Gate-based Readout – Physics

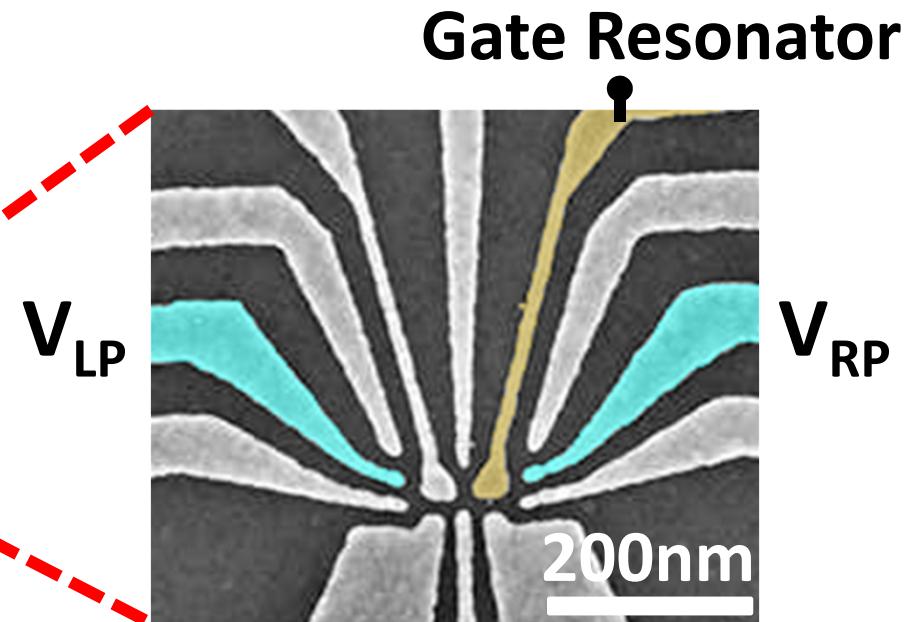
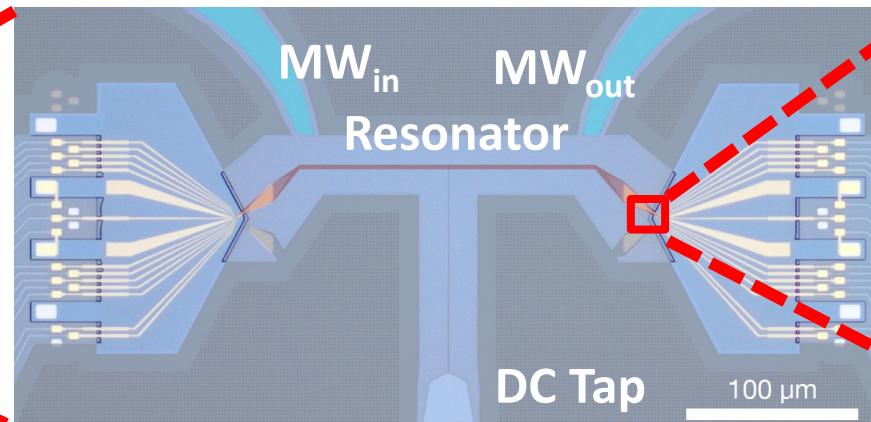
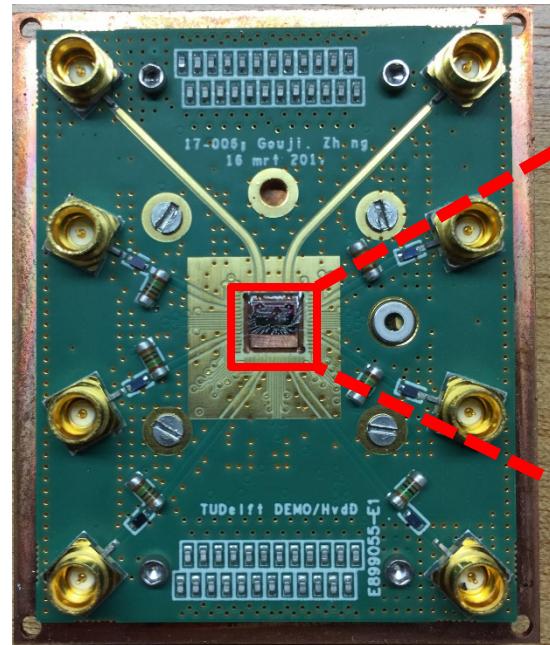


Gate-based Readout – Realization

- How to detect the state-dependent electron tunneling?

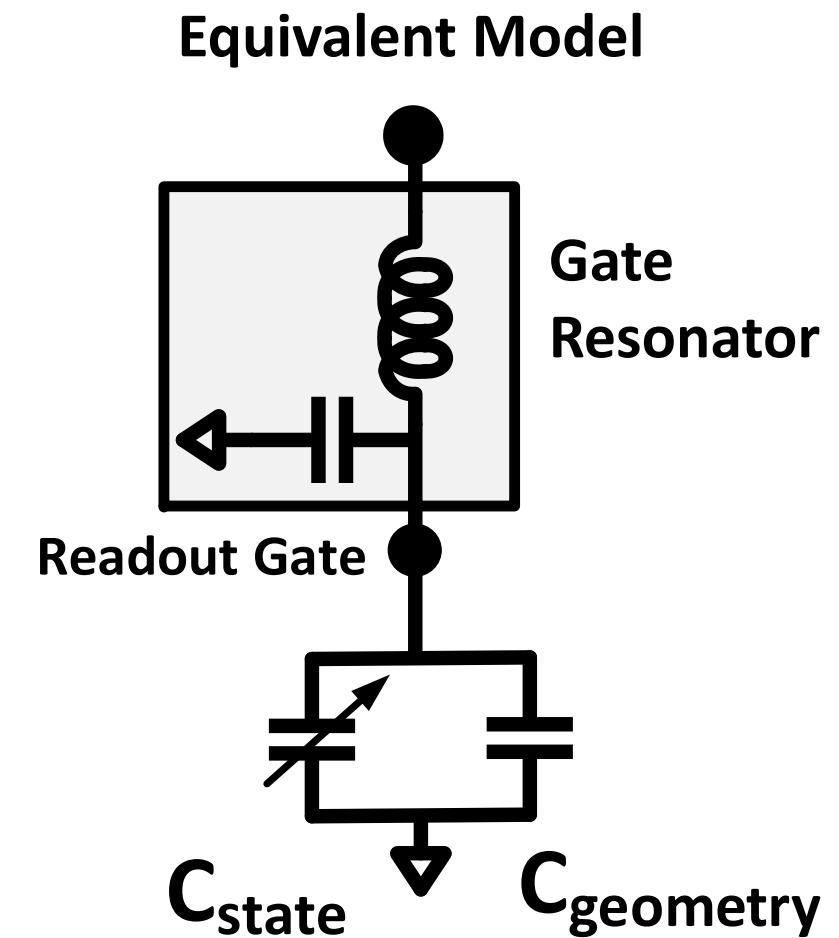
Gate-based Readout – Realization

- How to detect the state-dependent electron tunneling?
 - Couple quantum dot's gate to a resonator



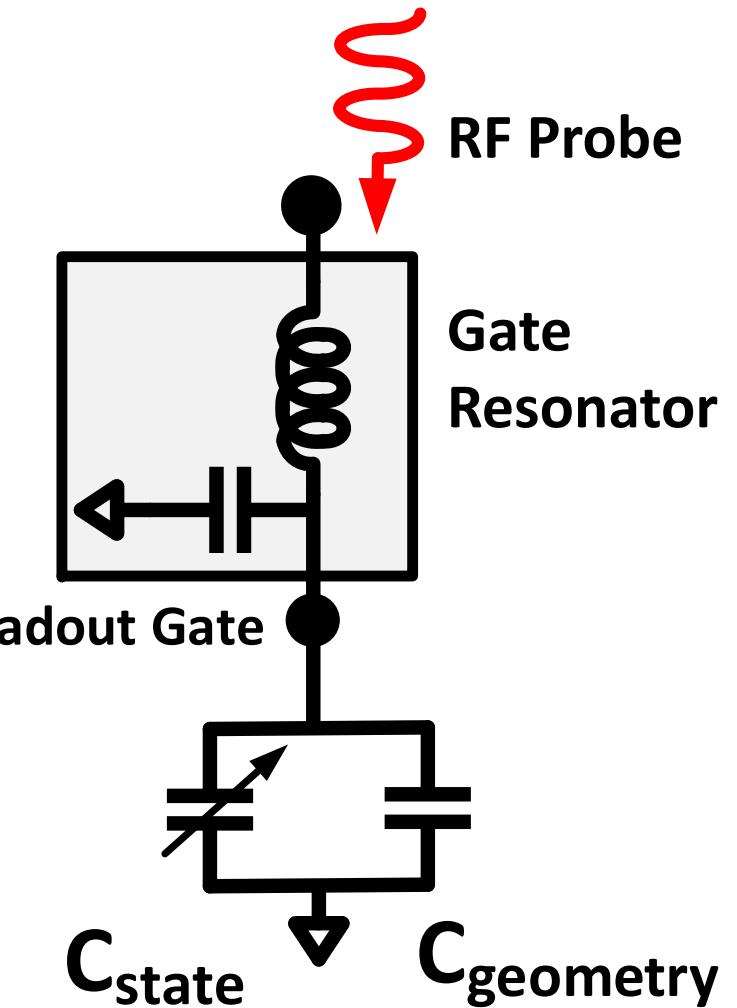
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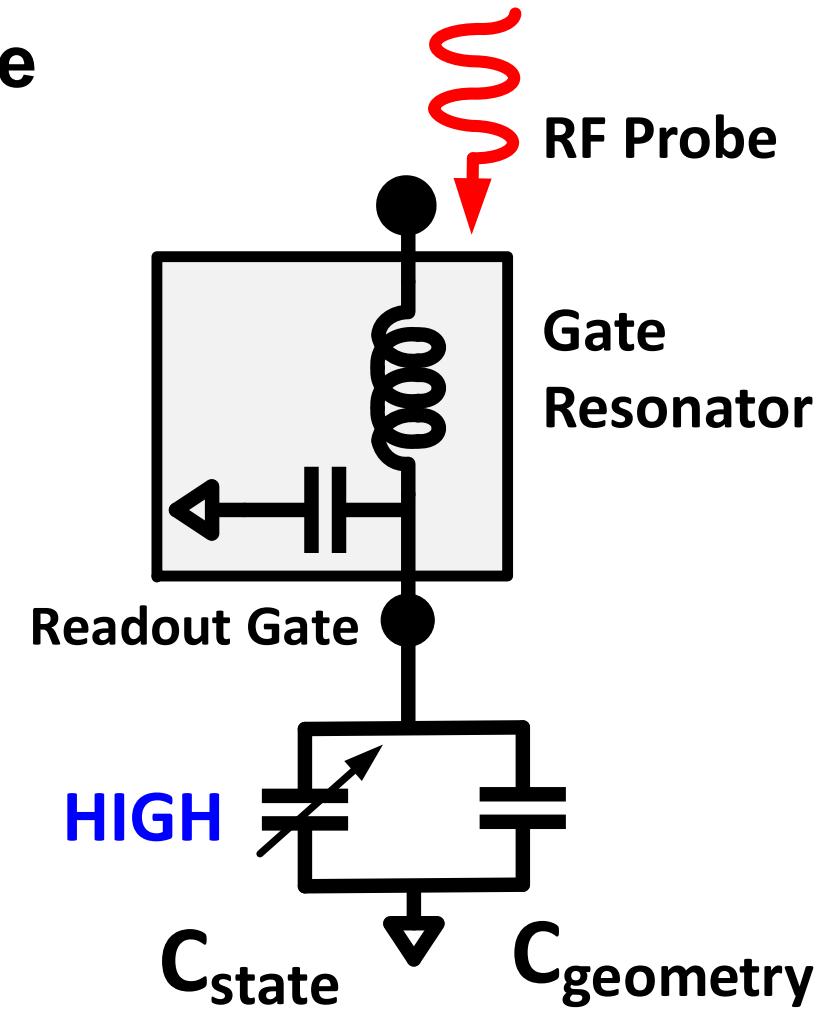
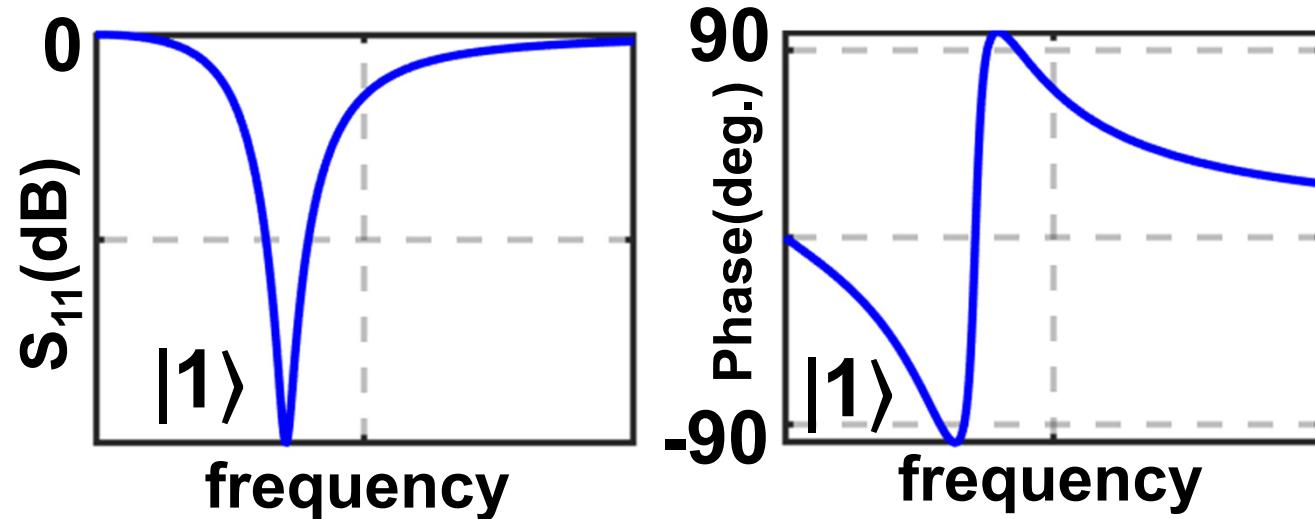
Gate-based Readout – Detection

- Probe with -110 dBm, 6-8 GHz microwave signal



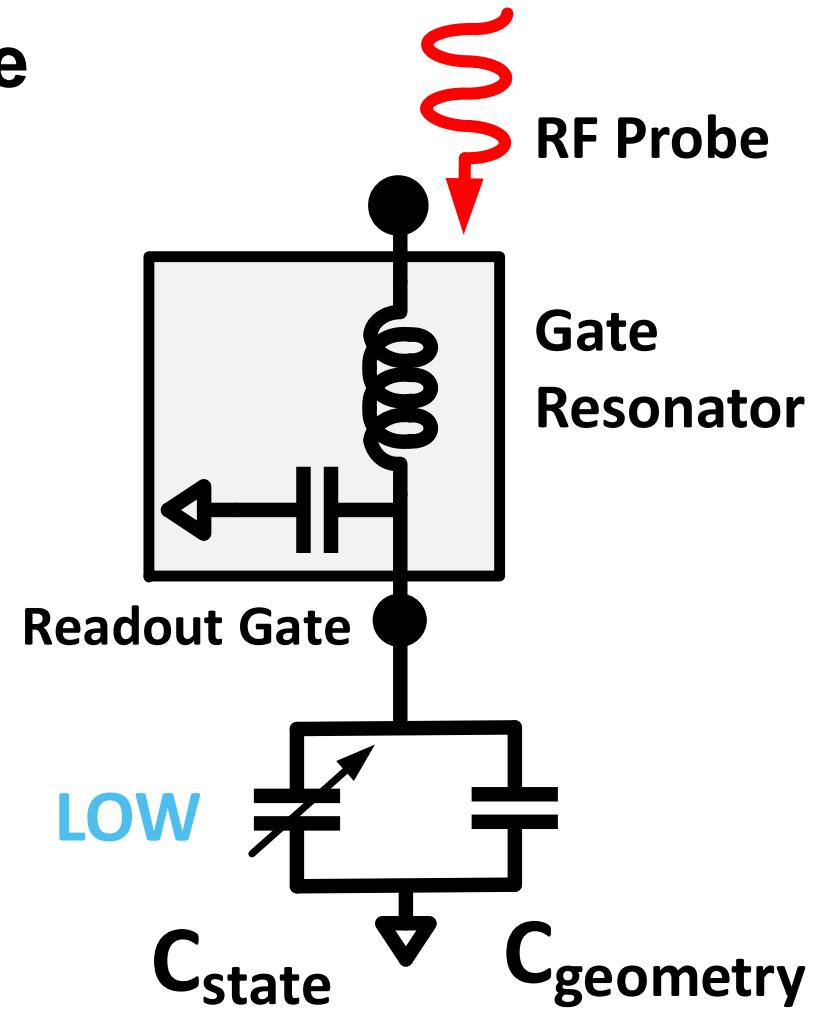
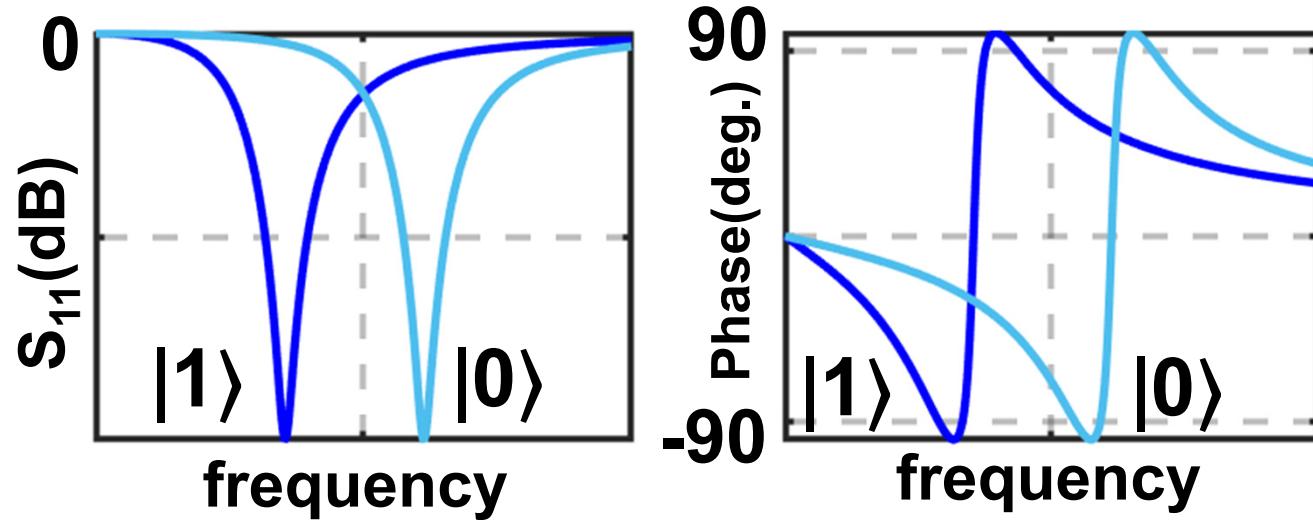
Gate-based Readout – Detection

- Probe with -110 dBm, 6-8 GHz microwave signal
- State-dependent tunneling capacitance



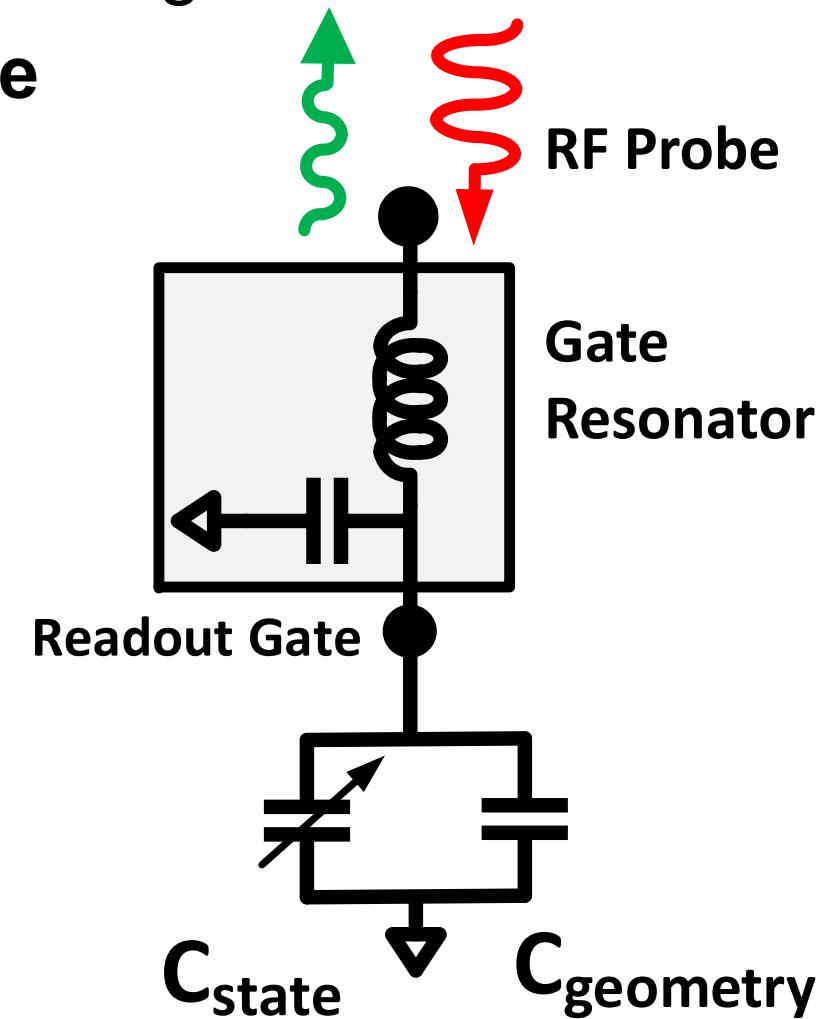
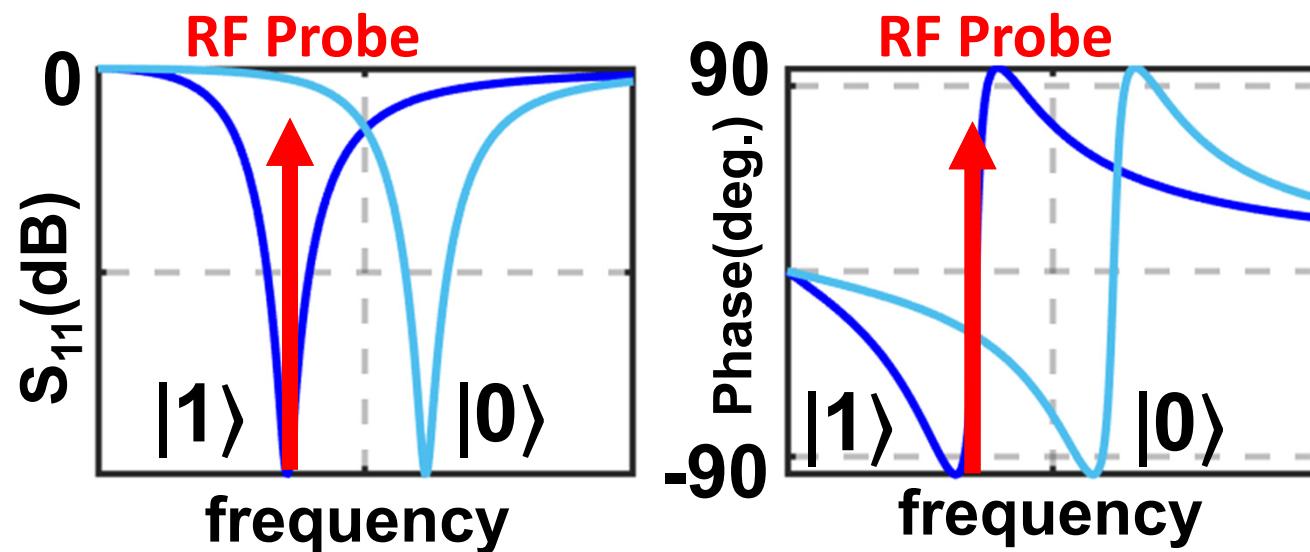
Gate-based Readout – Detection

- Probe with -110 dBm, 6-8 GHz microwave signal
- State-dependent tunneling capacitance



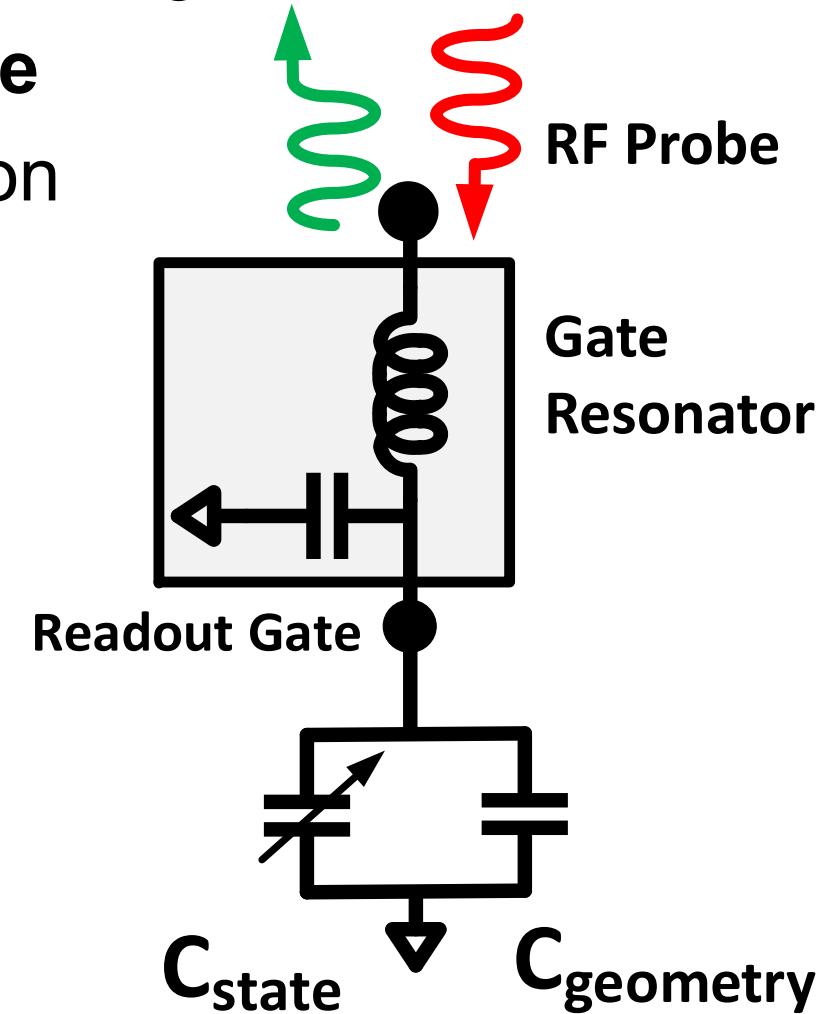
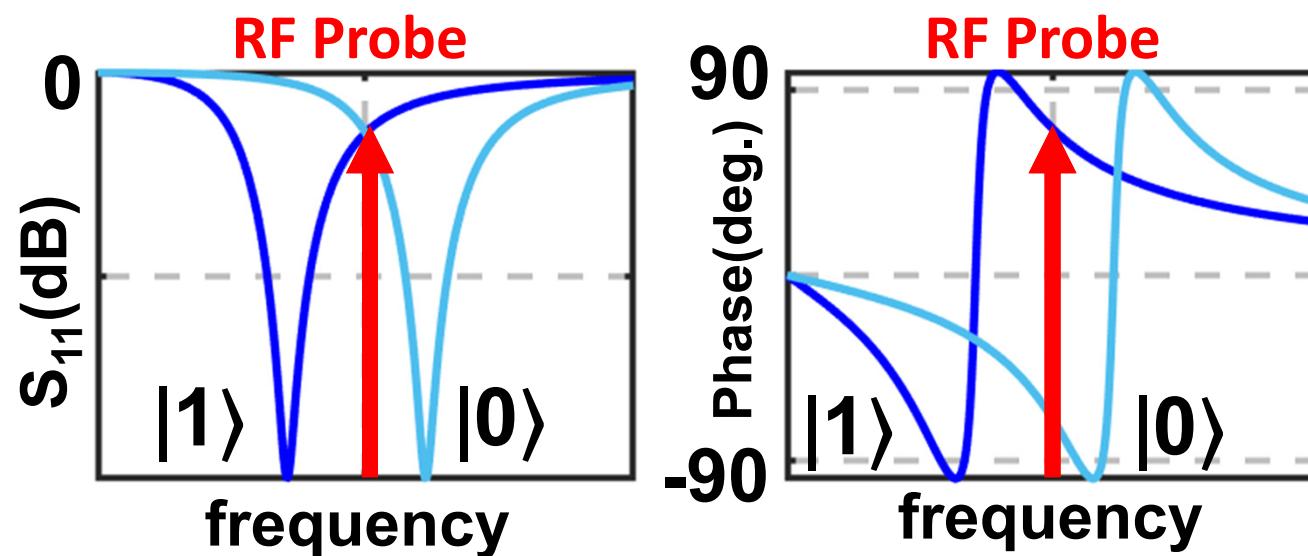
Gate-based Readout – Detection

- Probe with -110 dBm, 6-8 GHz microwave signal
- State-dependent **tunneling capacitance**
- Amplitude Modulation



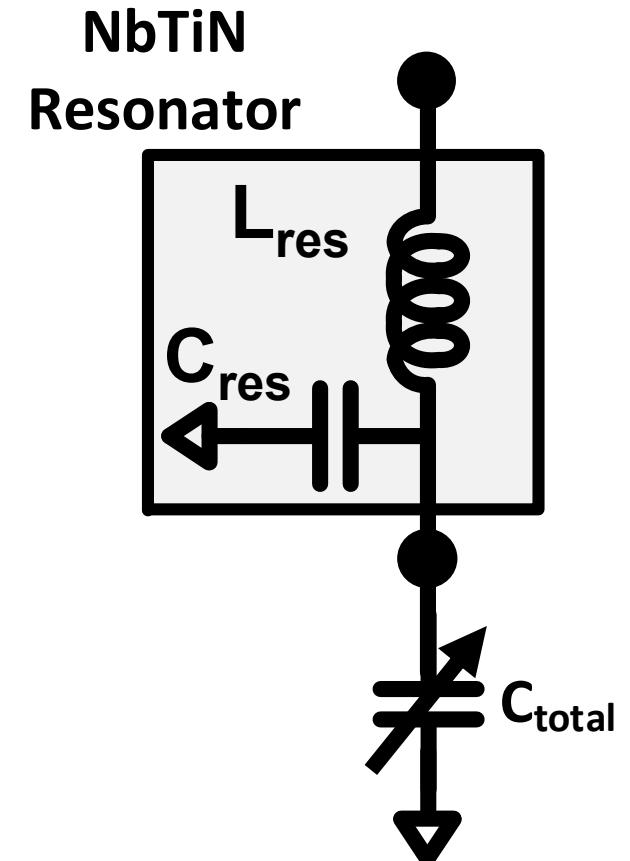
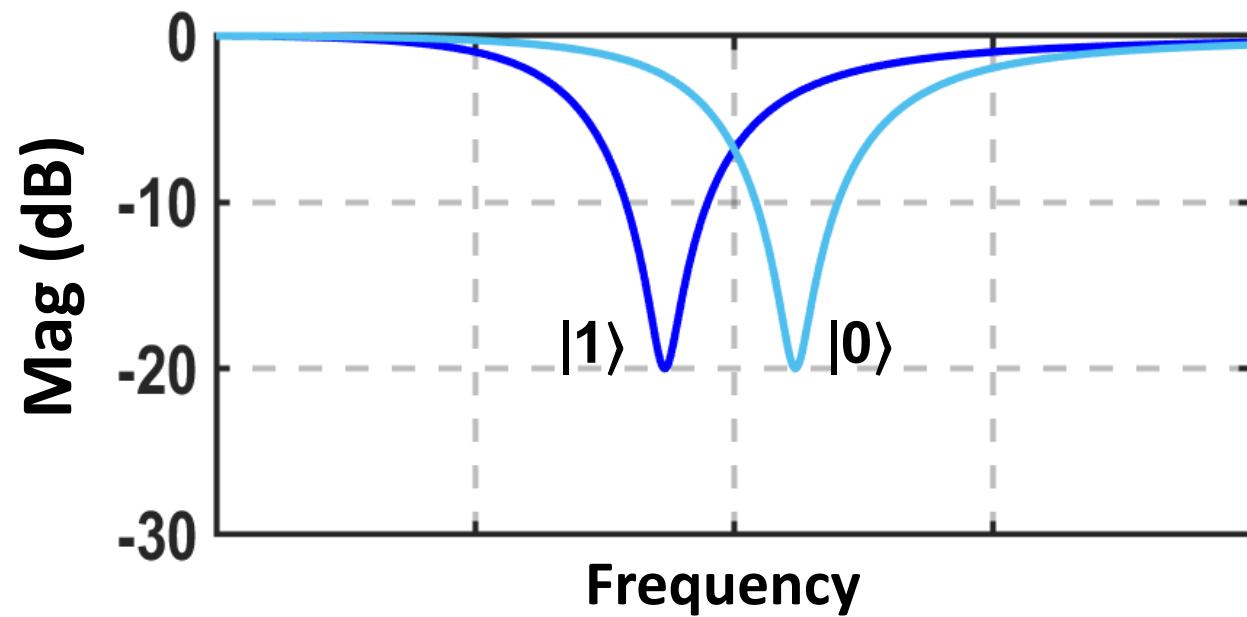
Gate-based Readout – Detection

- Probe with -110 dBm, 6-8 GHz microwave signal
- State-dependent **tunneling capacitance**
- Amplitude Modulation / Phase Modulation



Gate-based Readout – Resonator

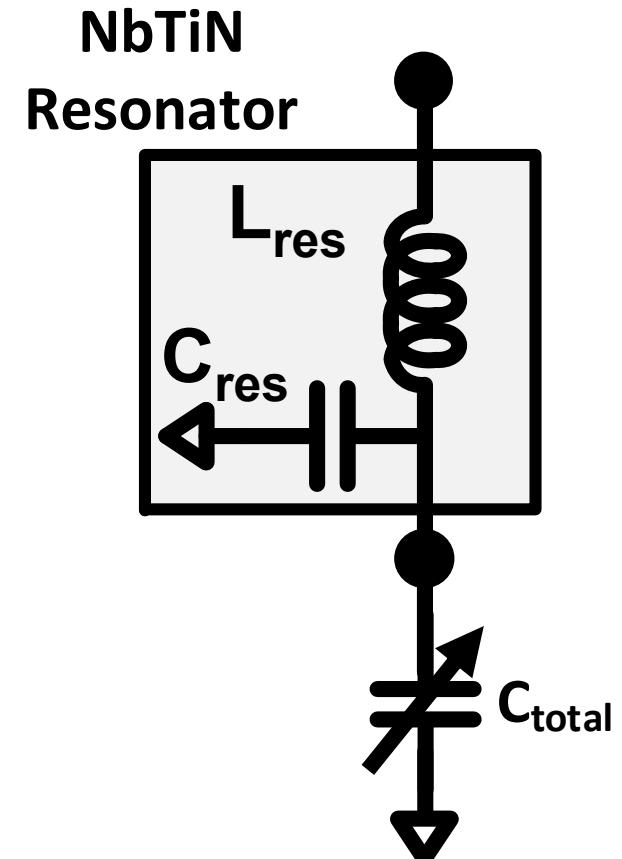
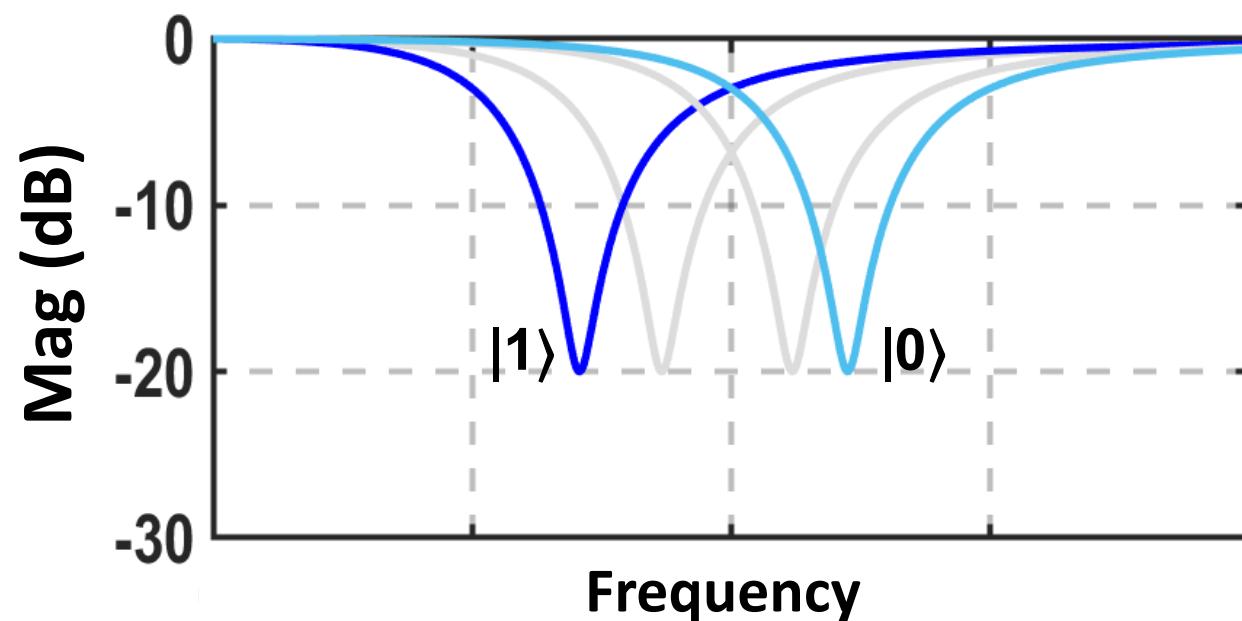
- NbTiN high impedance resonator ($\sim 1\text{K}\Omega$)



Gate-based Readout – Resonator

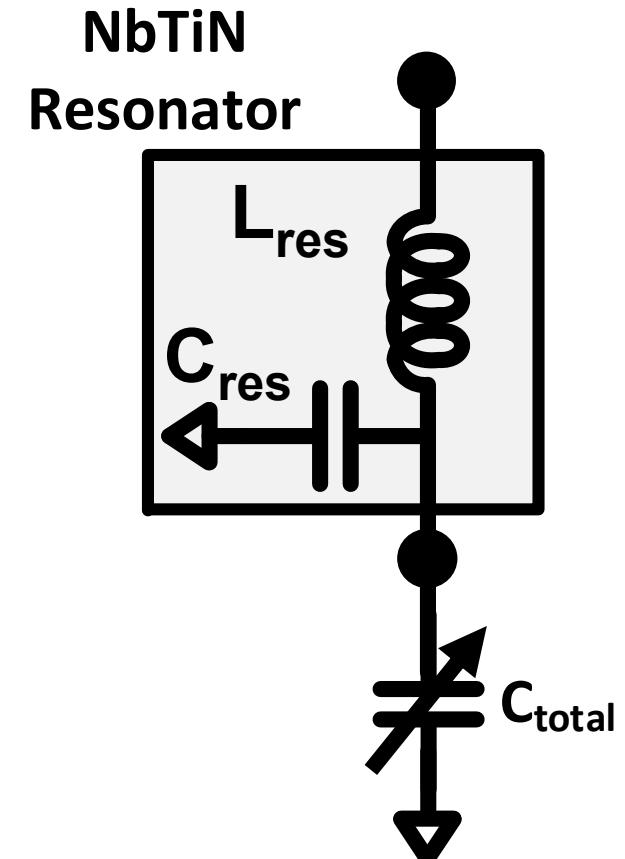
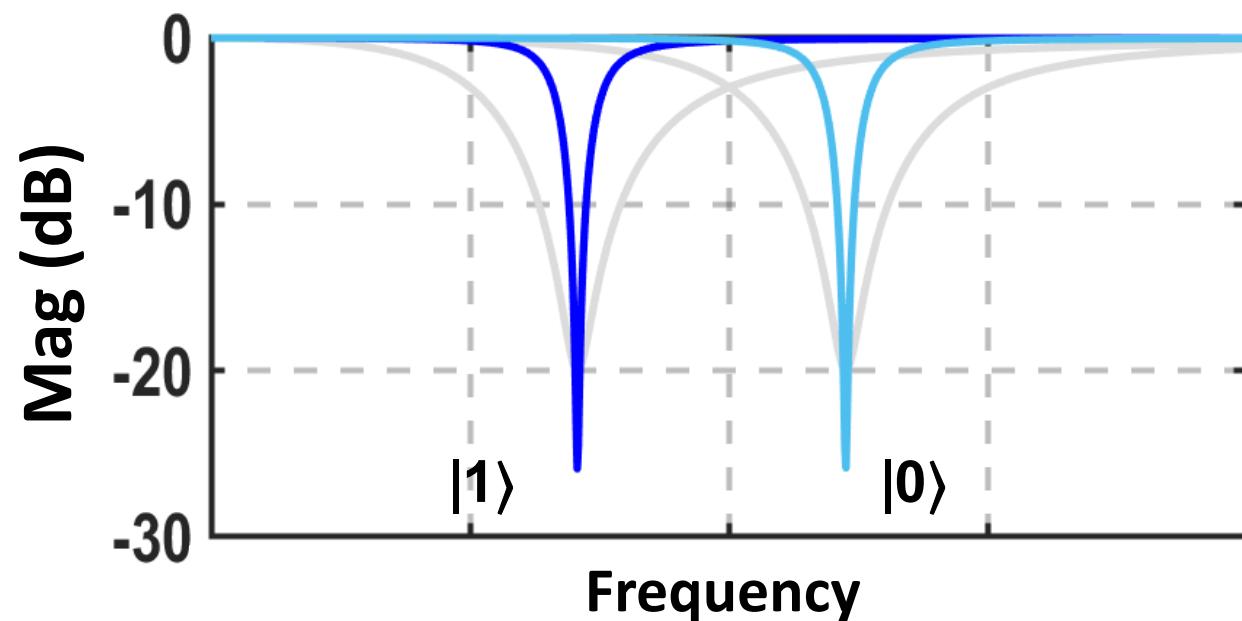
- NbTiN high impedance resonator ($\sim 1\text{K}\Omega$)
 - Improve capacitance variation sensitivity

$$\omega_{res} = \frac{1}{\sqrt{L_{res}(C_{res} + C_{total})}}$$



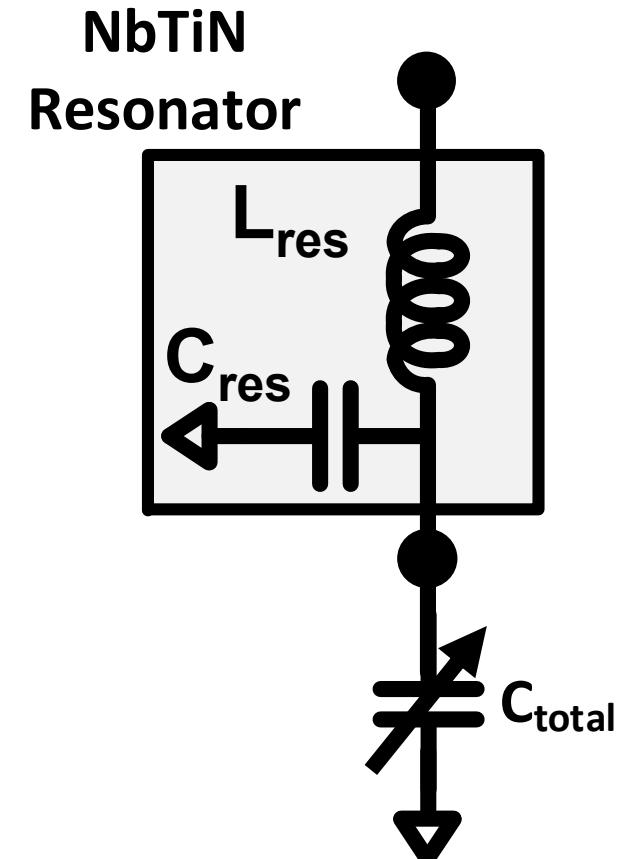
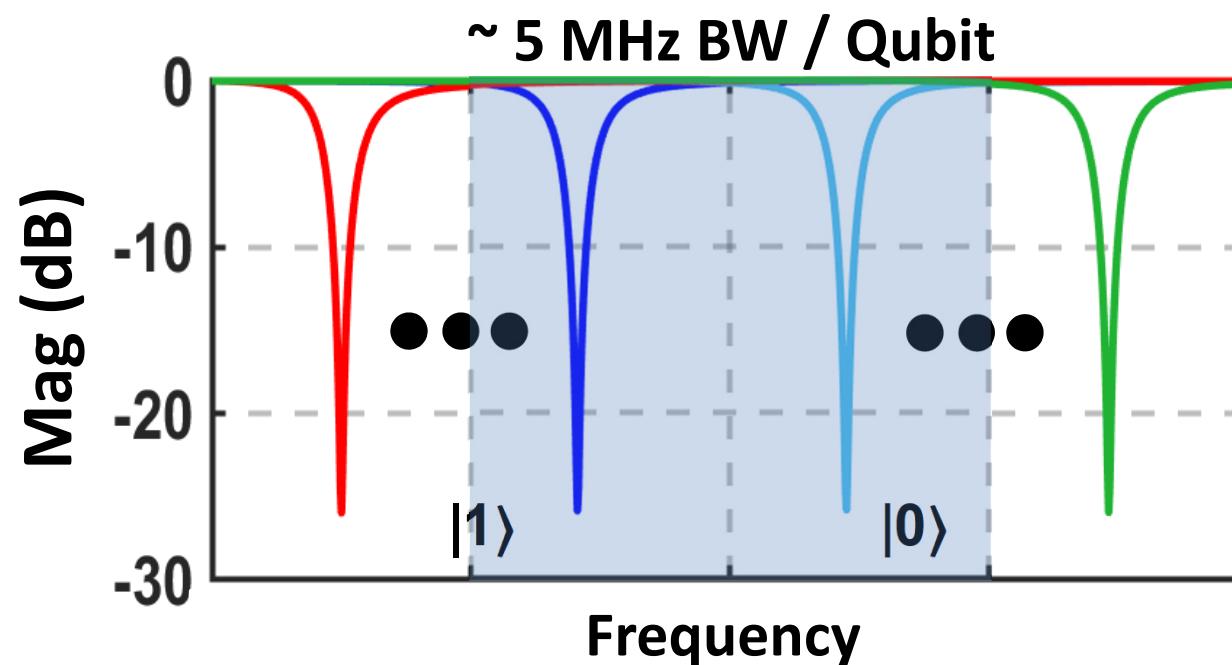
Gate-based Readout – Resonator

- NbTiN high impedance resonator ($\sim 1\text{K}\Omega$)
 - Improve capacitance variation sensitivity
 - High Q-factor (>2500)



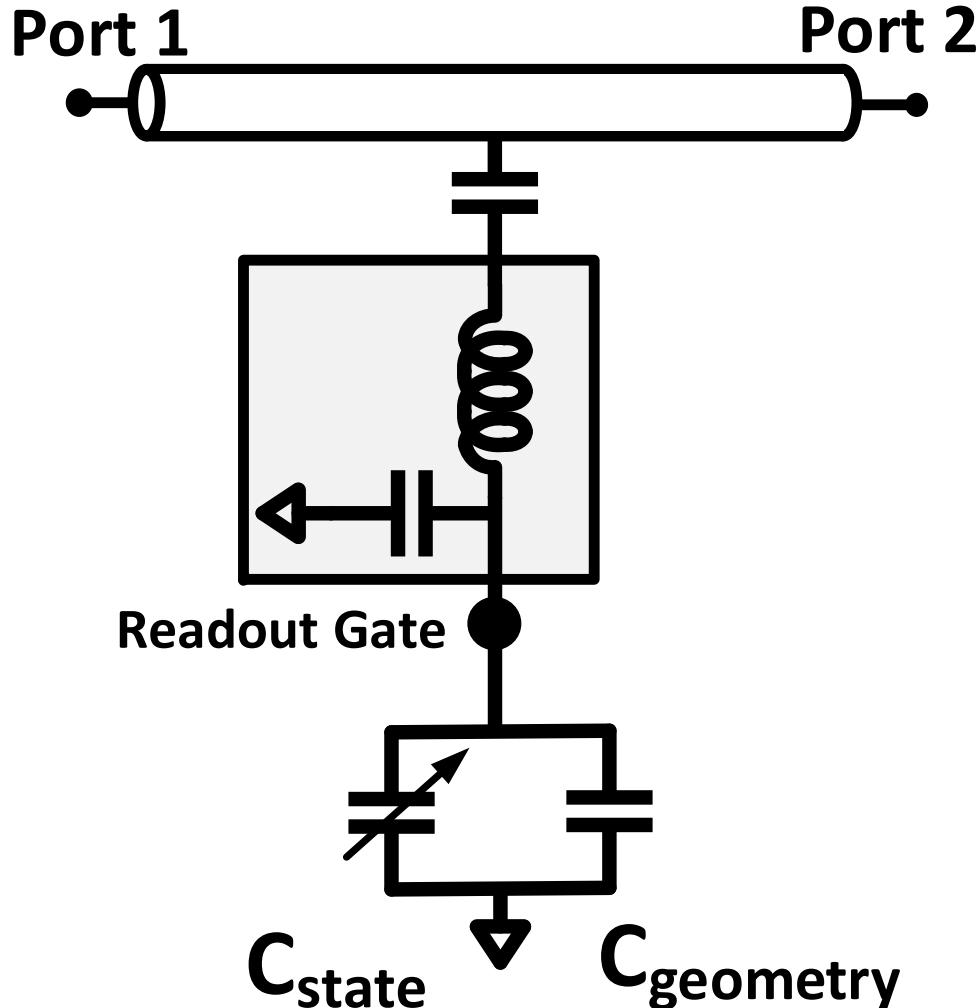
Gate-based Readout – Resonator

- NbTiN high impedance resonator ($\sim 1\text{K}\Omega$)
 - Improve capacitance variation sensitivity
 - High Q-factor (>2500)
 - # Qubits/bandwidth efficiency



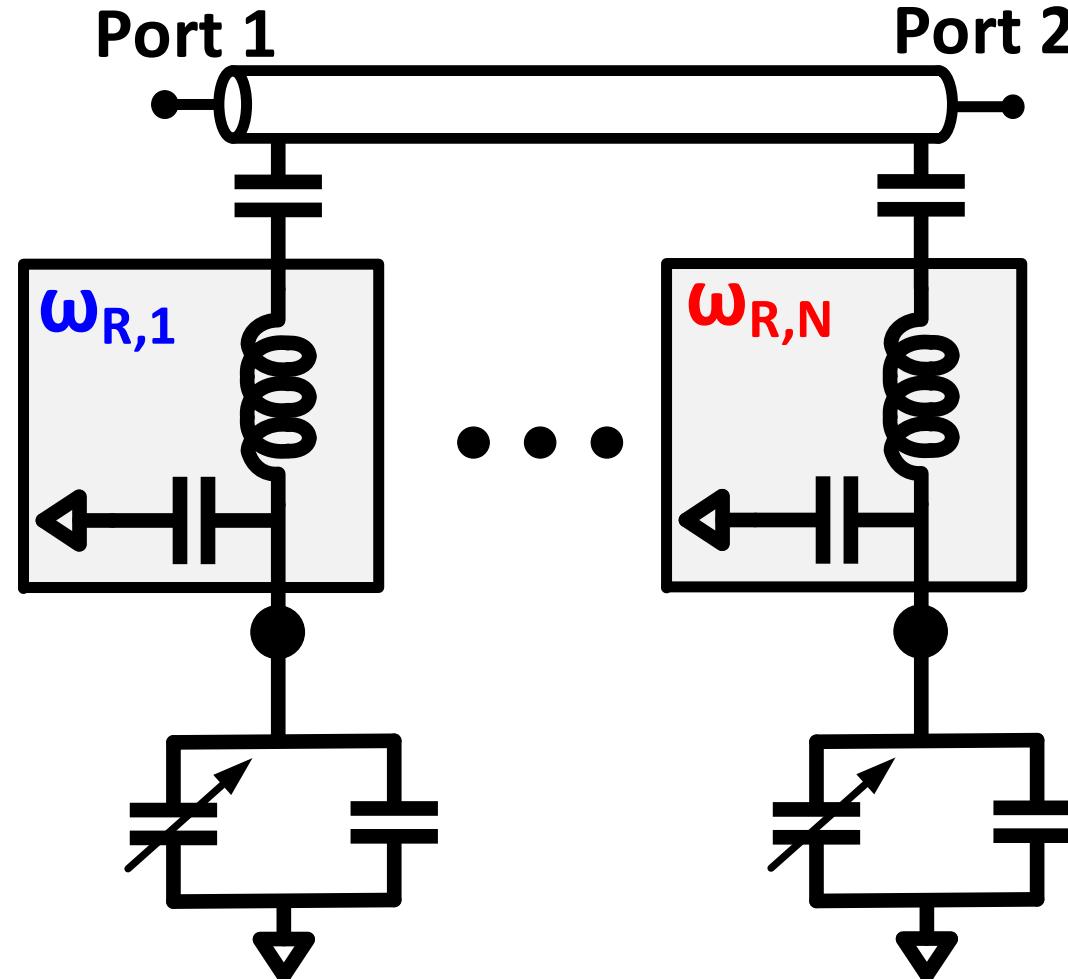
Gate-based Readout – Scalability

- Frequency division multiplexing (FDMA)



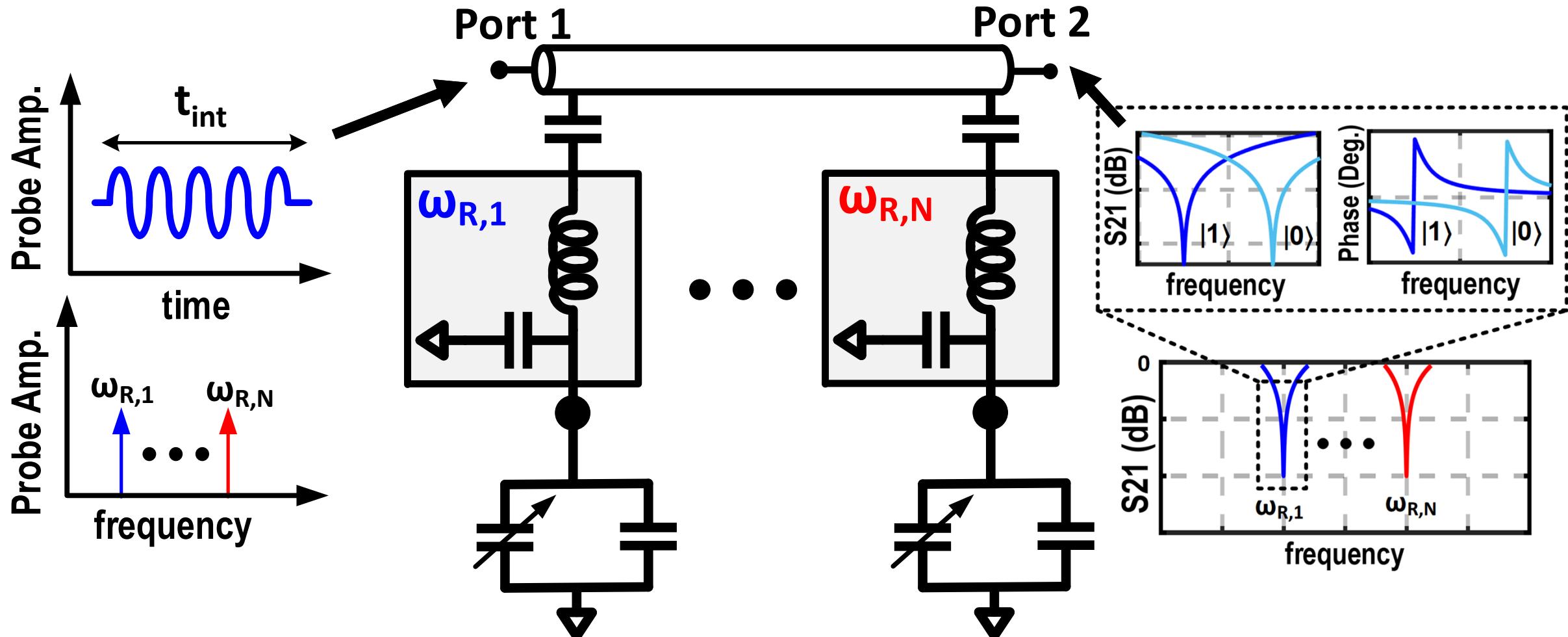
Gate-based Readout – Scalability

- Frequency division multiplexing (FDMA)



Gate-based Readout – Scalability

- Frequency division multiplexing (FDMA)

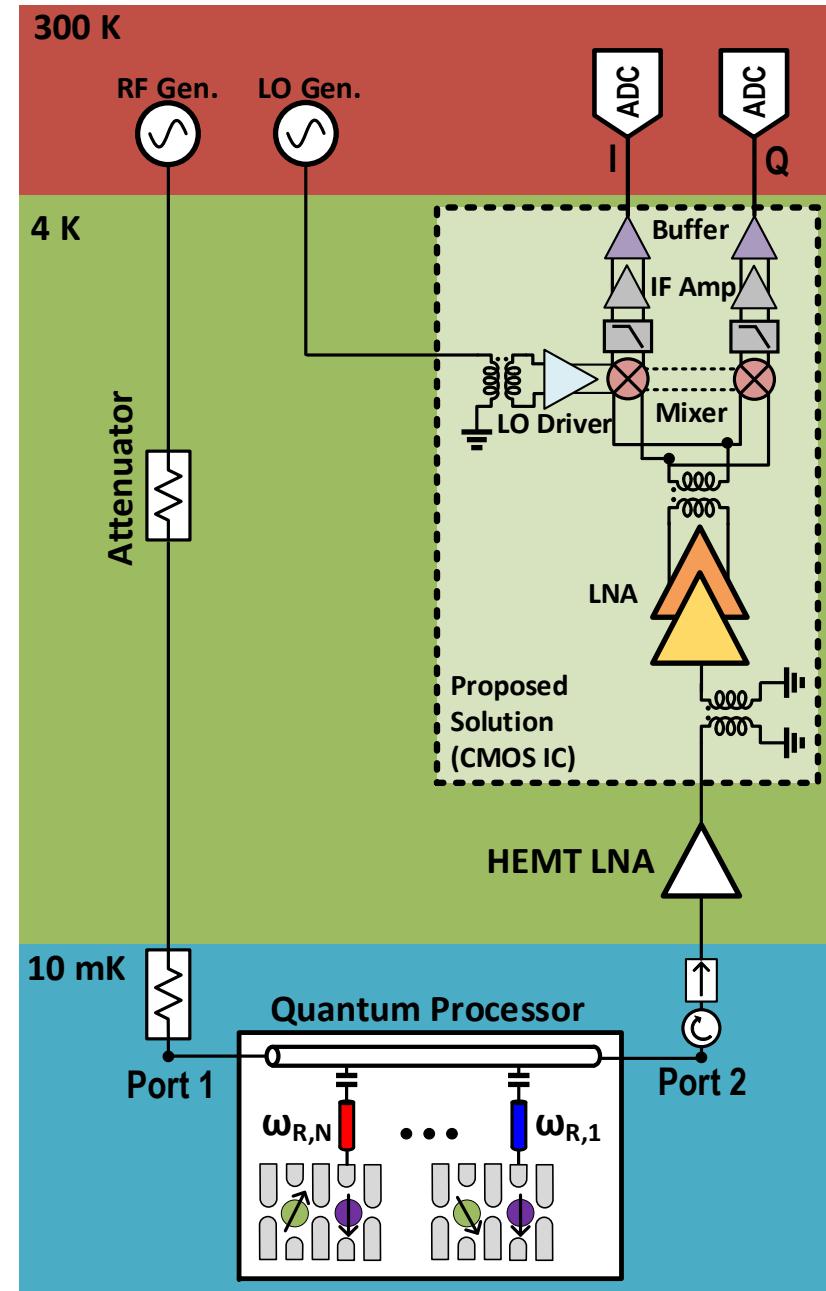


Outline

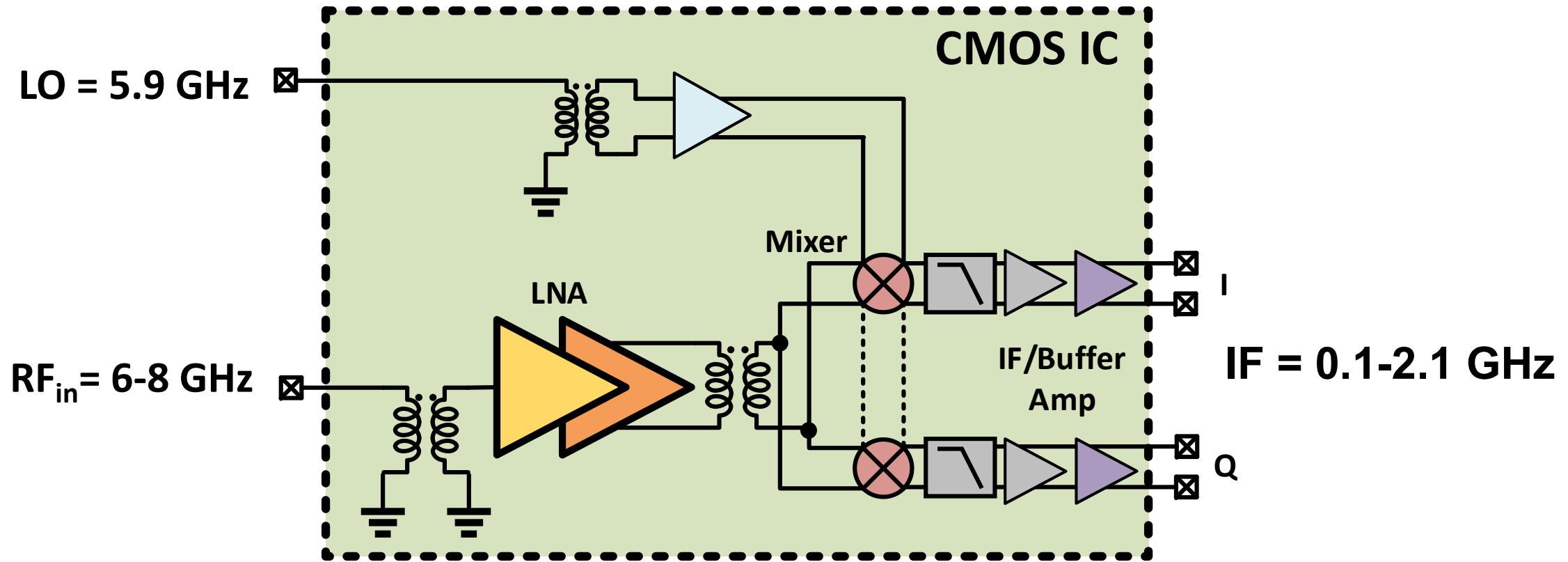
- Introduction
- Spin-Qubit Readout
- System Architecture
- Electrical Performance
- Spin-Qubit Readout Experiment
- Conclusions

Proposed Solution

- **CMOS IC solution at 4K**
 - Reduced complexity
 - Latency
 - Smaller form factor
- **HEMT LNA at 4K**
 - $T_n \sim 5 \text{ K}$
 - Gain = 40 dB
 - BW = 4-8 GHz



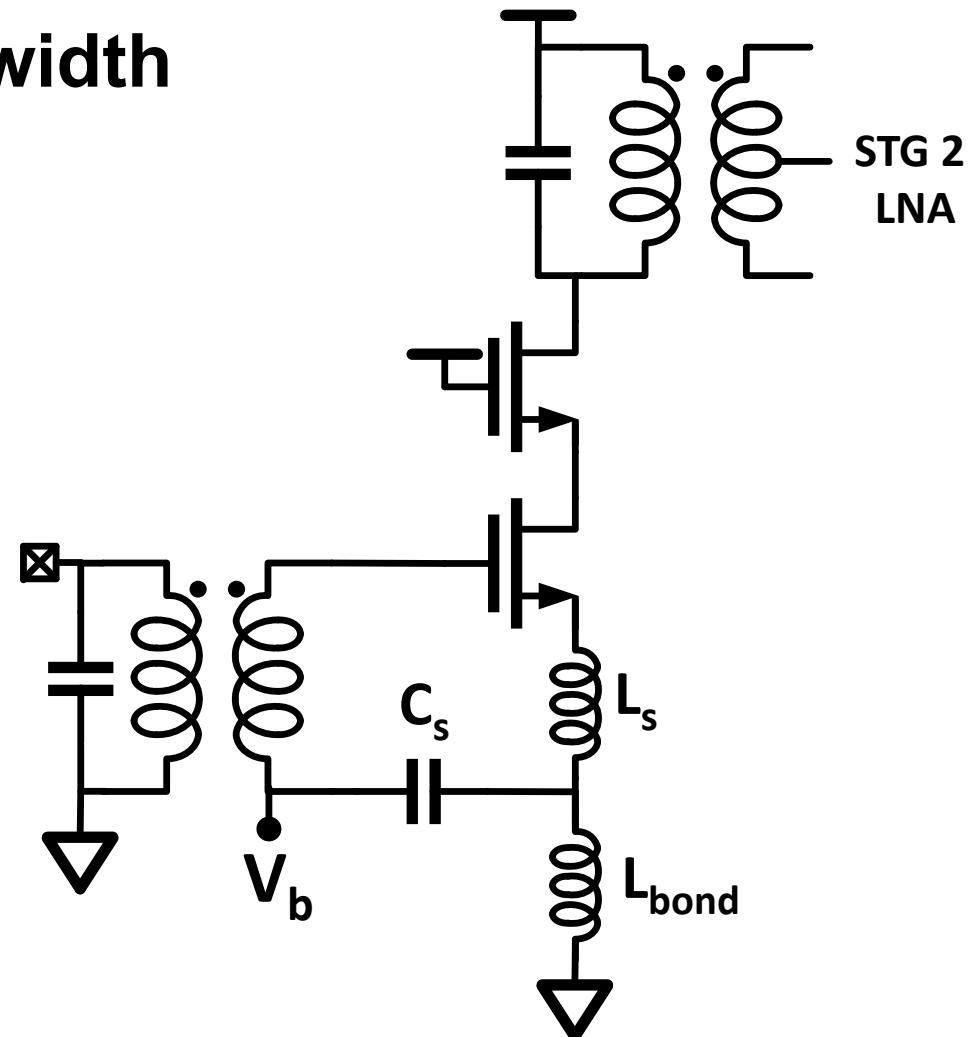
Proposed RX Architecture



- IF RX architecture → Avoid higher 1/f noise at cryogenic temperatures

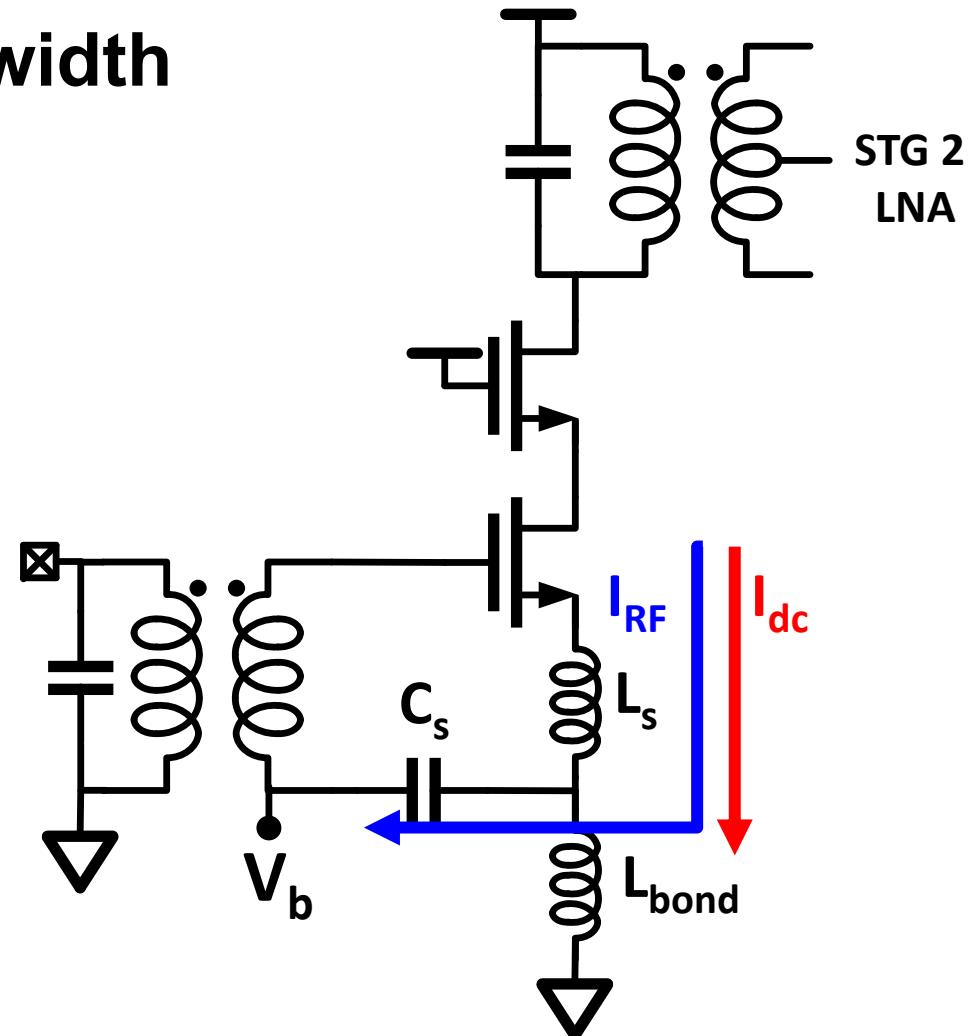
First Stage LNA Design

- **CS Degenerated LNA → Narrow bandwidth**
 - Doubly tuned resonator input matching
- **Bond wire parasitics**
 - Low impedance RF path through C_s
- **Transformer interstage matching**

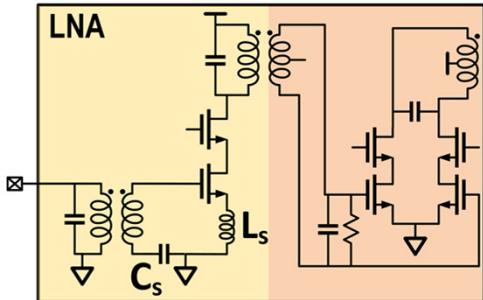
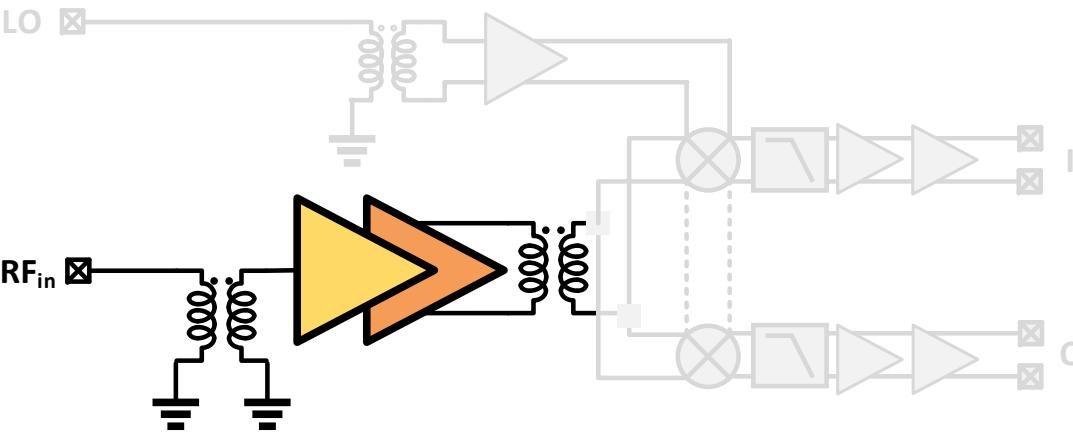


First Stage LNA Design

- **CS Degenerated LNA → Narrow bandwidth**
 - Doubly tuned resonator input matching
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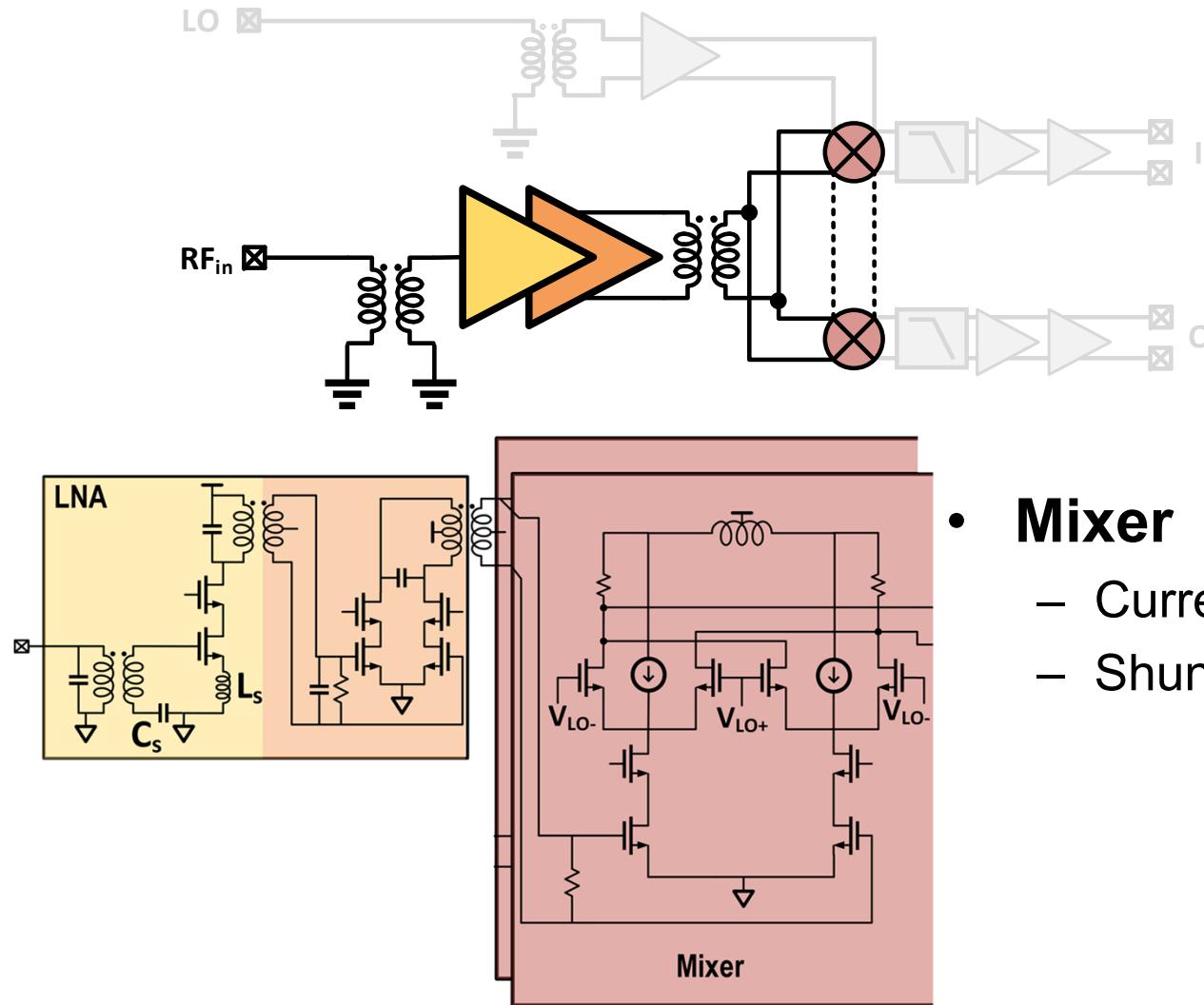


RX Schematic

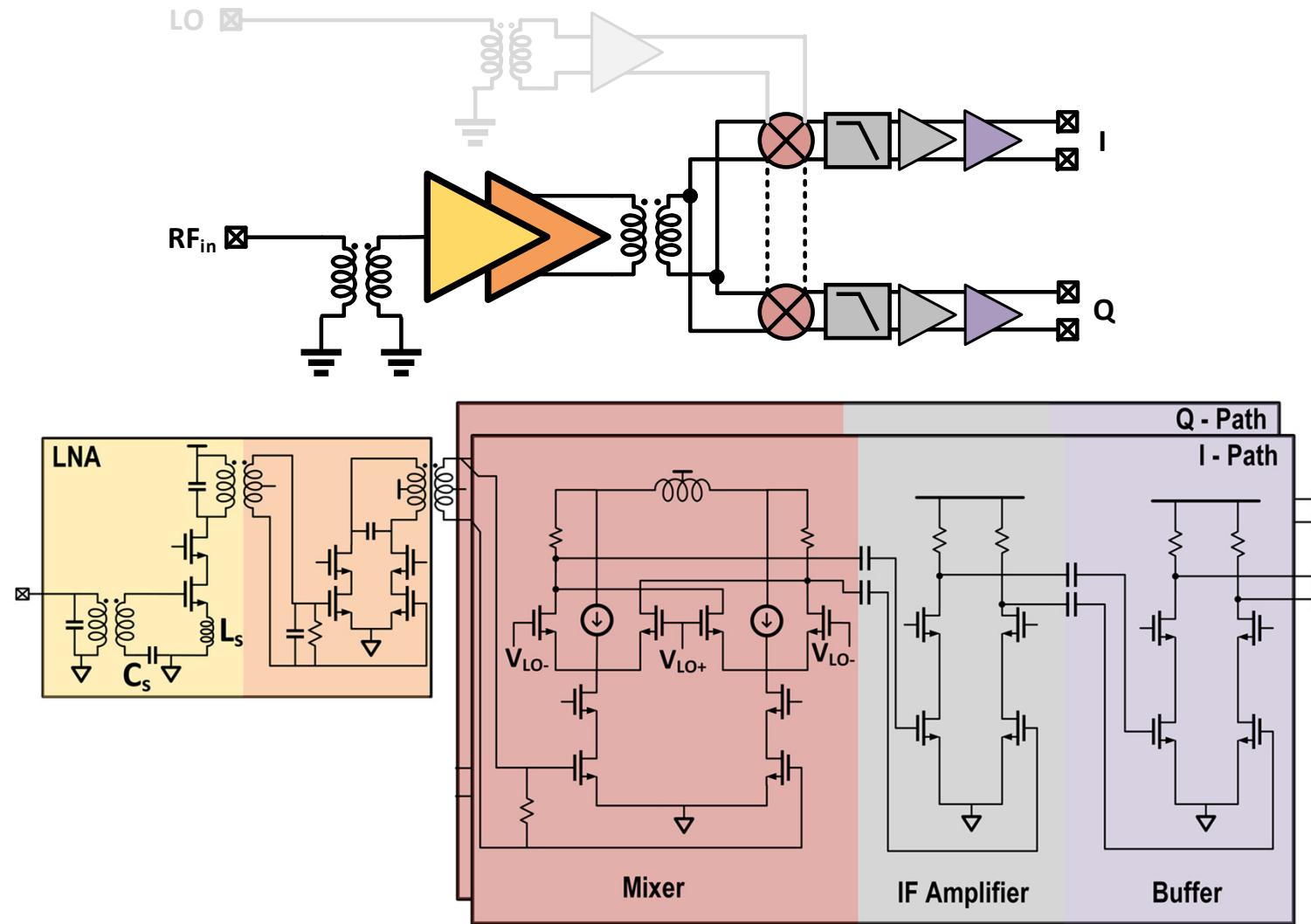


- **2 Stage LNA**
 - Pseudo-differential → Flexibility, V_t increase at 4K
 - 30 dB of gain → NF performance

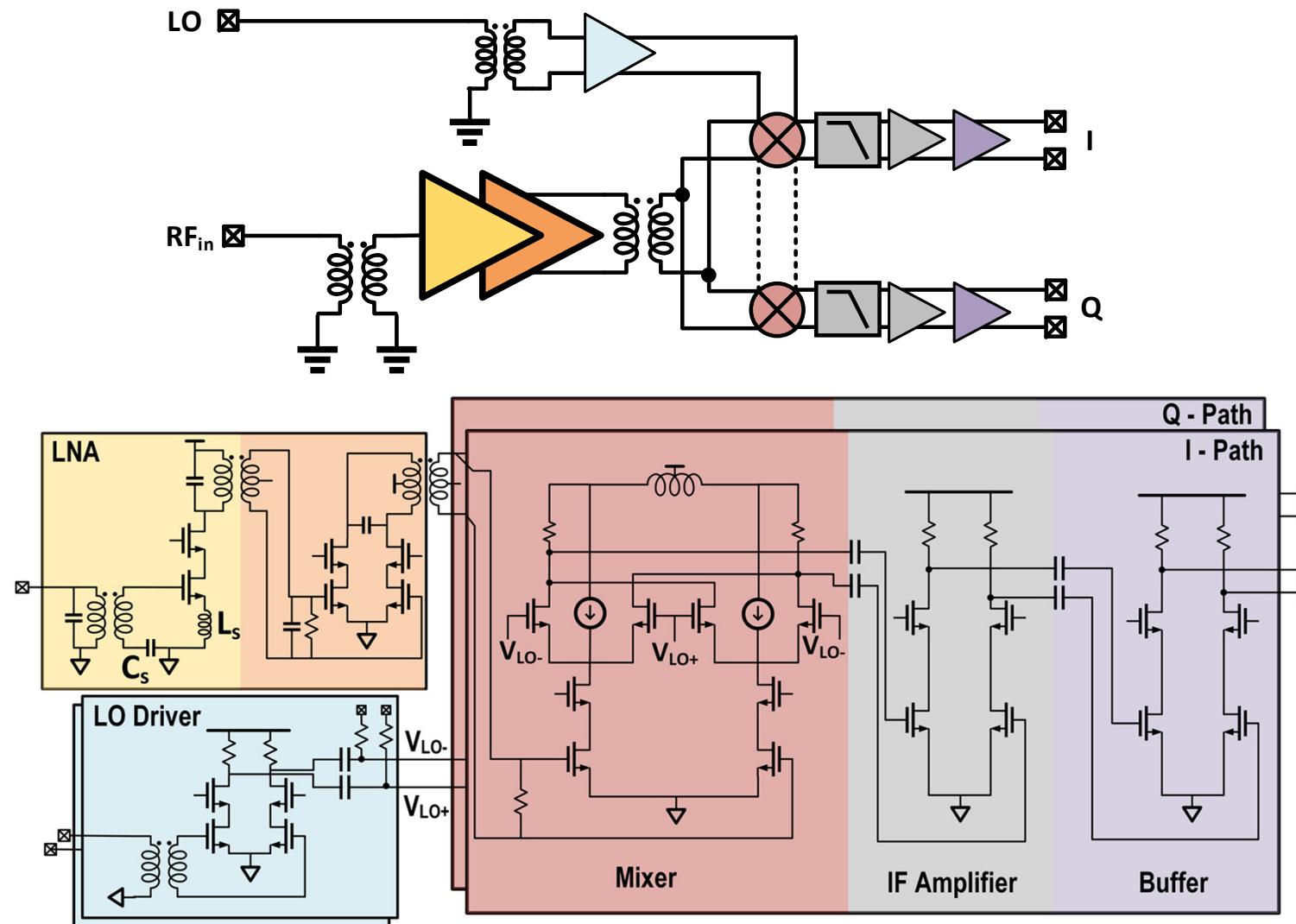
RX Schematic



RX Schematic



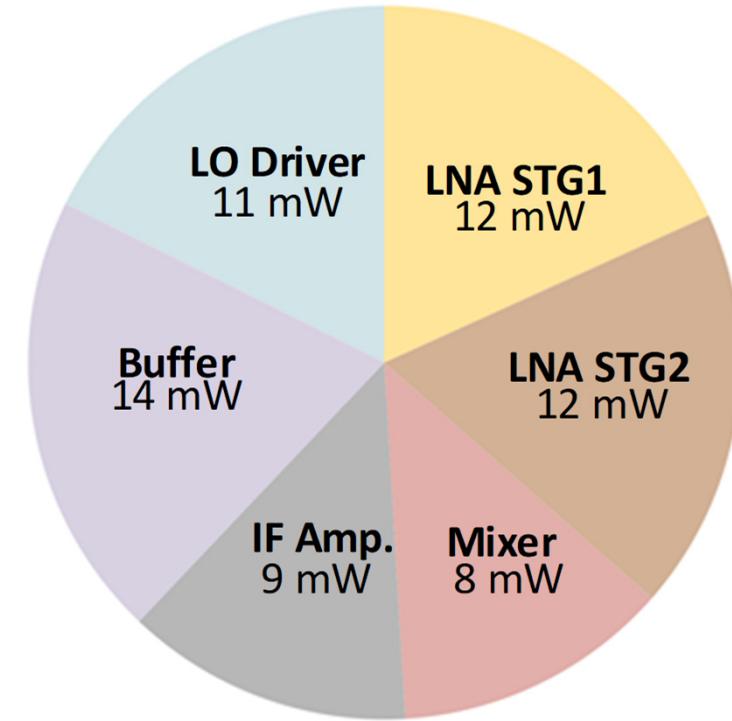
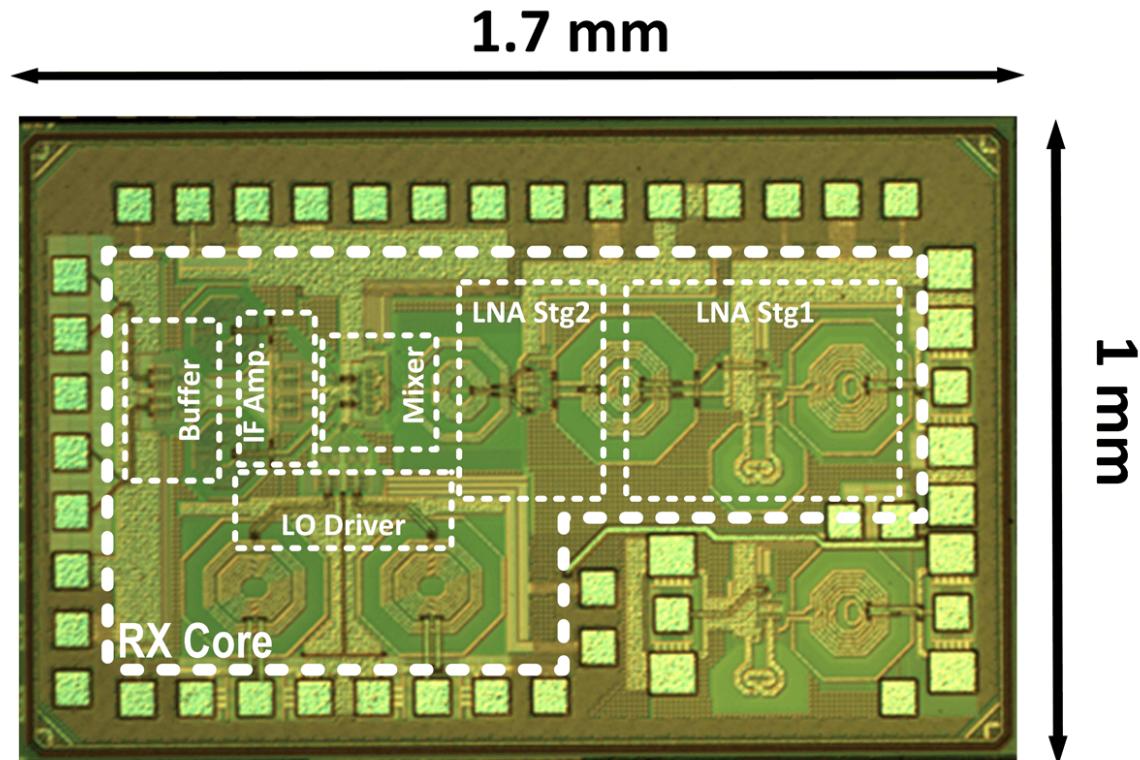
RX Schematic



Outline

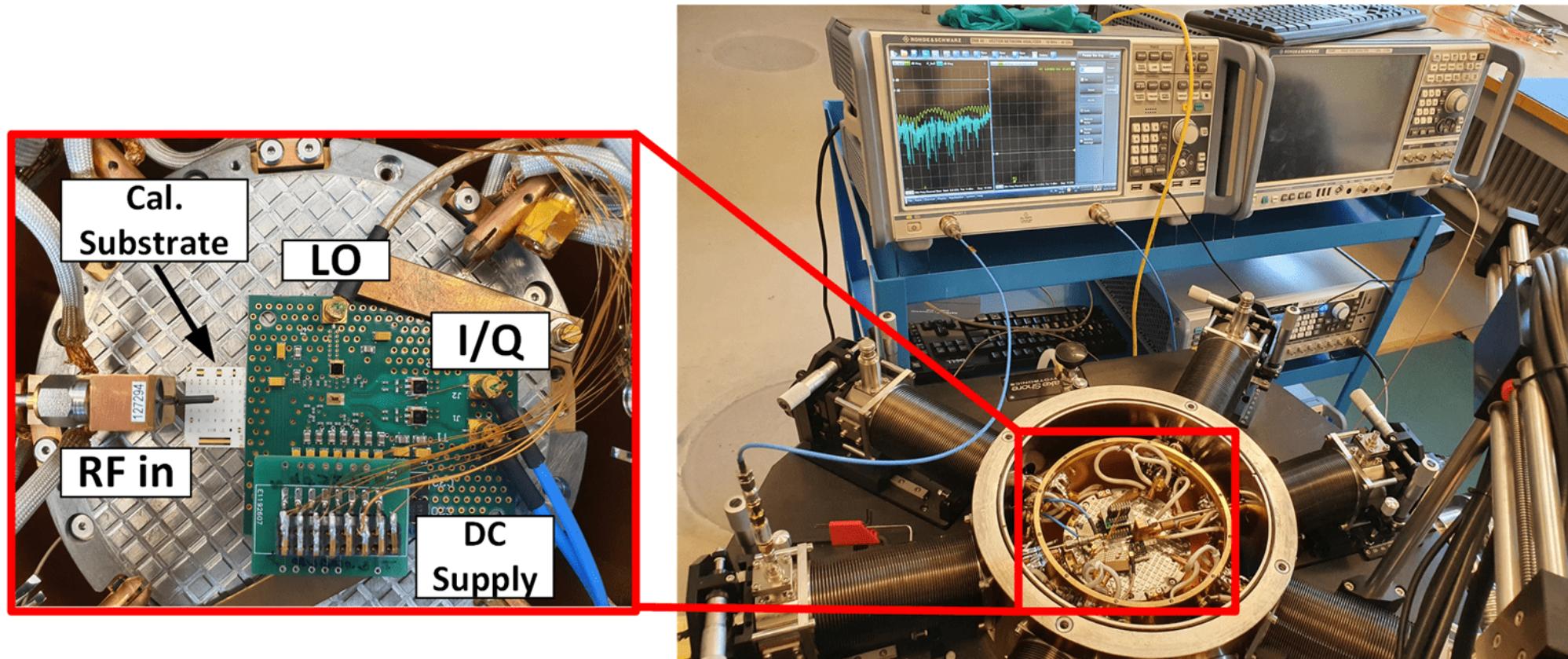
- Introduction
- Spin-Qubit Readout
- System Architecture
- **Electrical Performance**
- Spin-Qubit Readout Experiment
- Conclusions

RX Chip



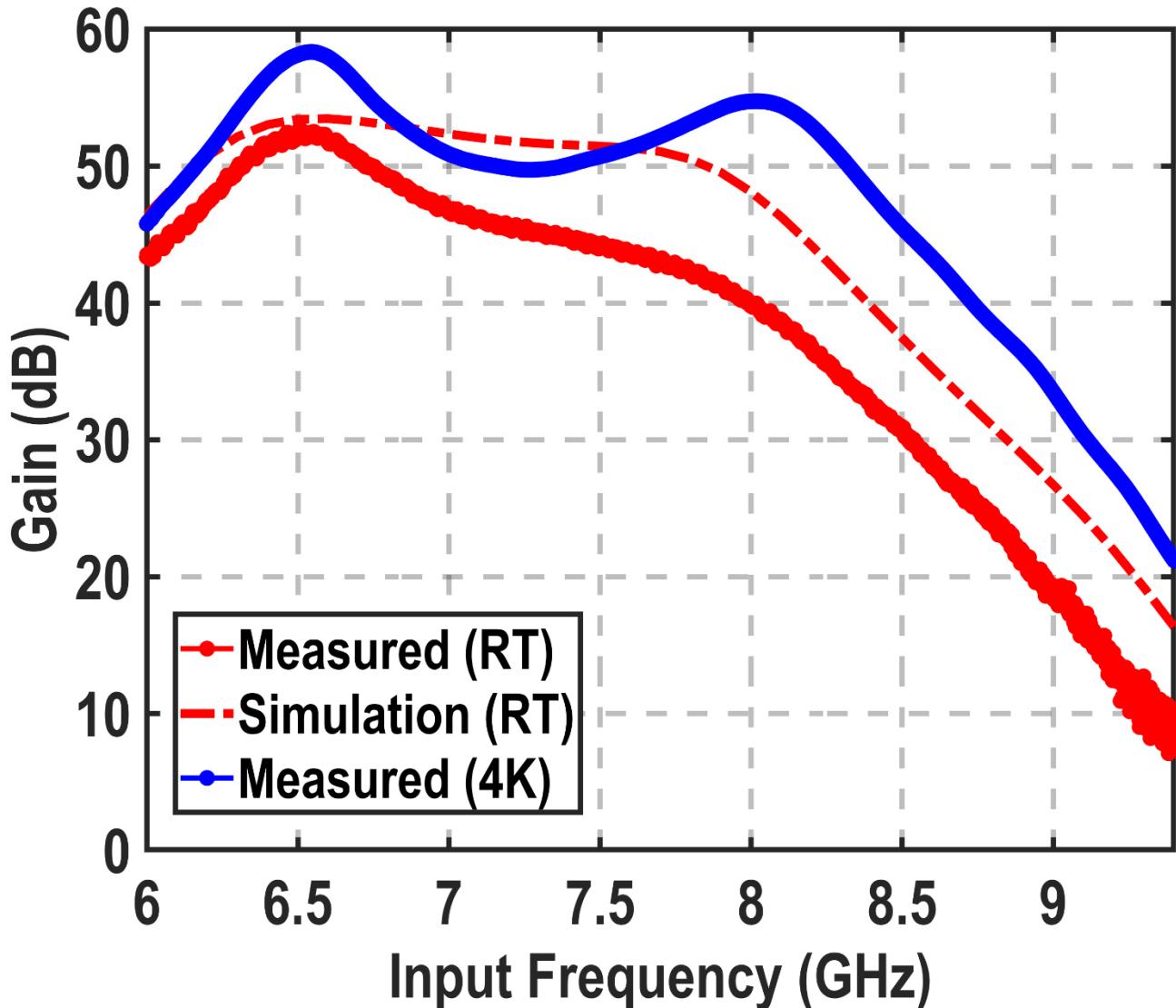
- 40nm Bulk CMOS
- Core area 0.68 mm²
- Total power of 66mW at 4K

Probe Station Measurement Setup



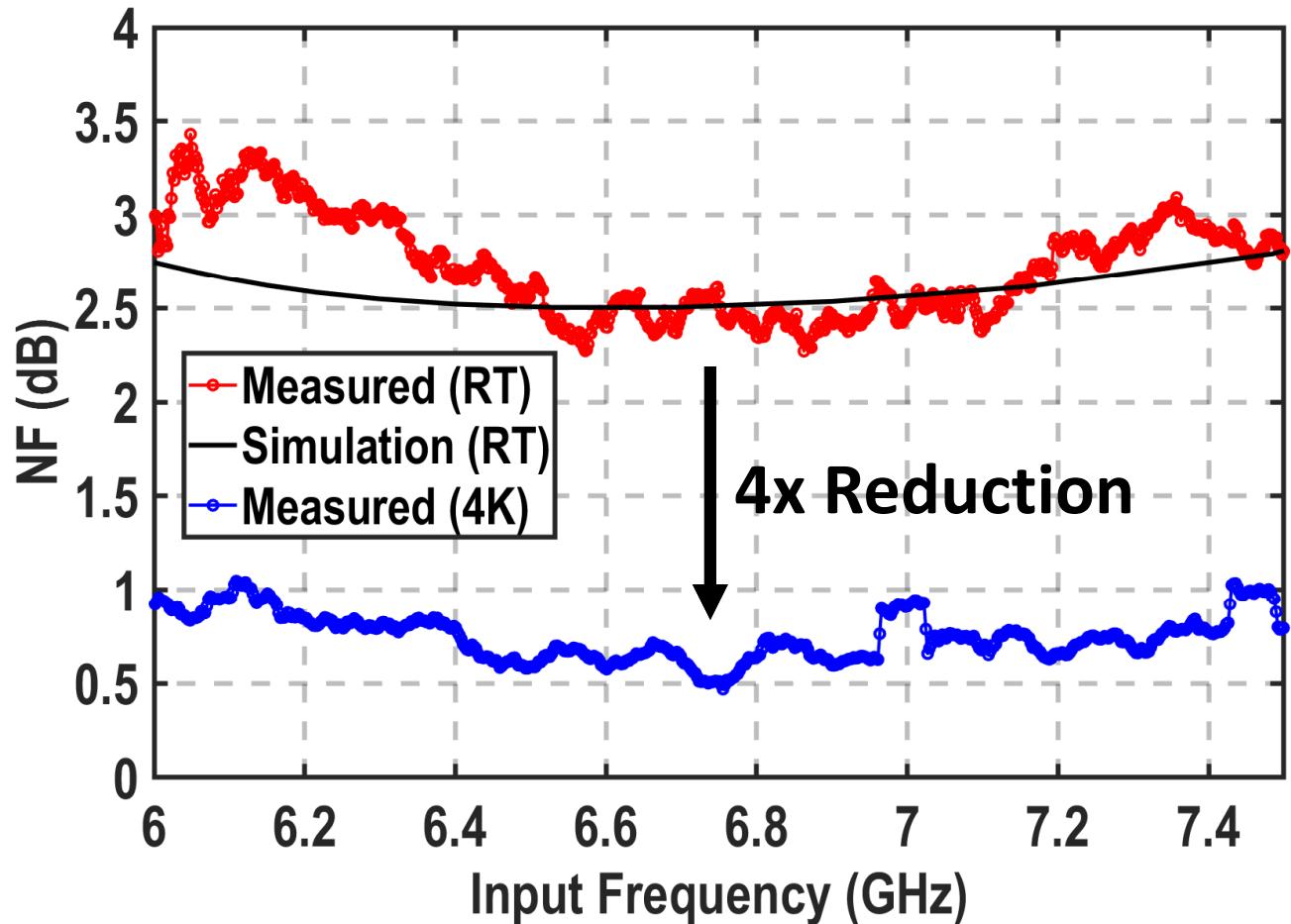
RX Gain

- **~5 dB increase in gain at 4K**
 - Increase in mobility
 - Increase in Q factor



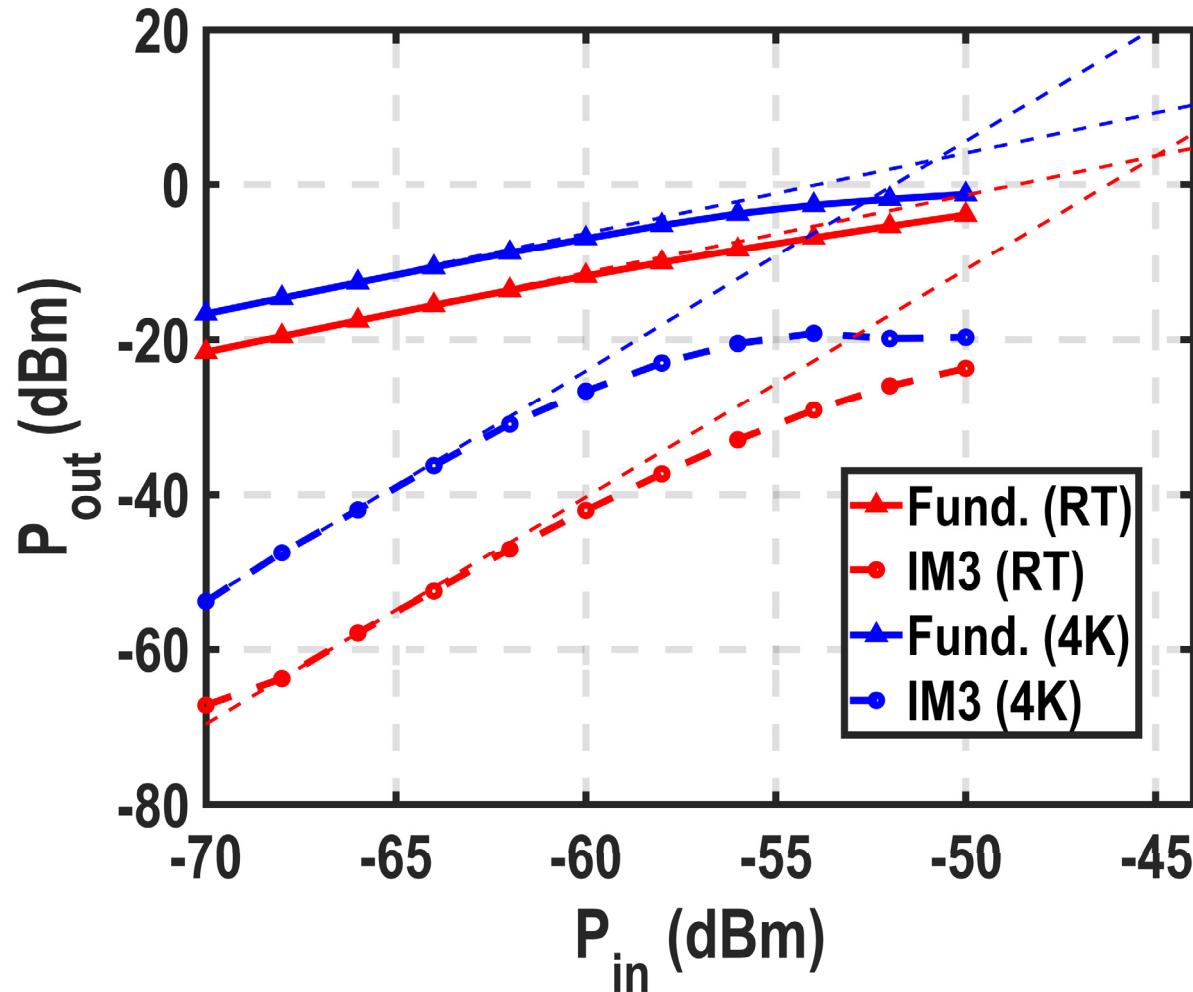
Noise Figure (DSB)

- **~4x NF reduction**
 - Shot noise
 - Self-heating effect



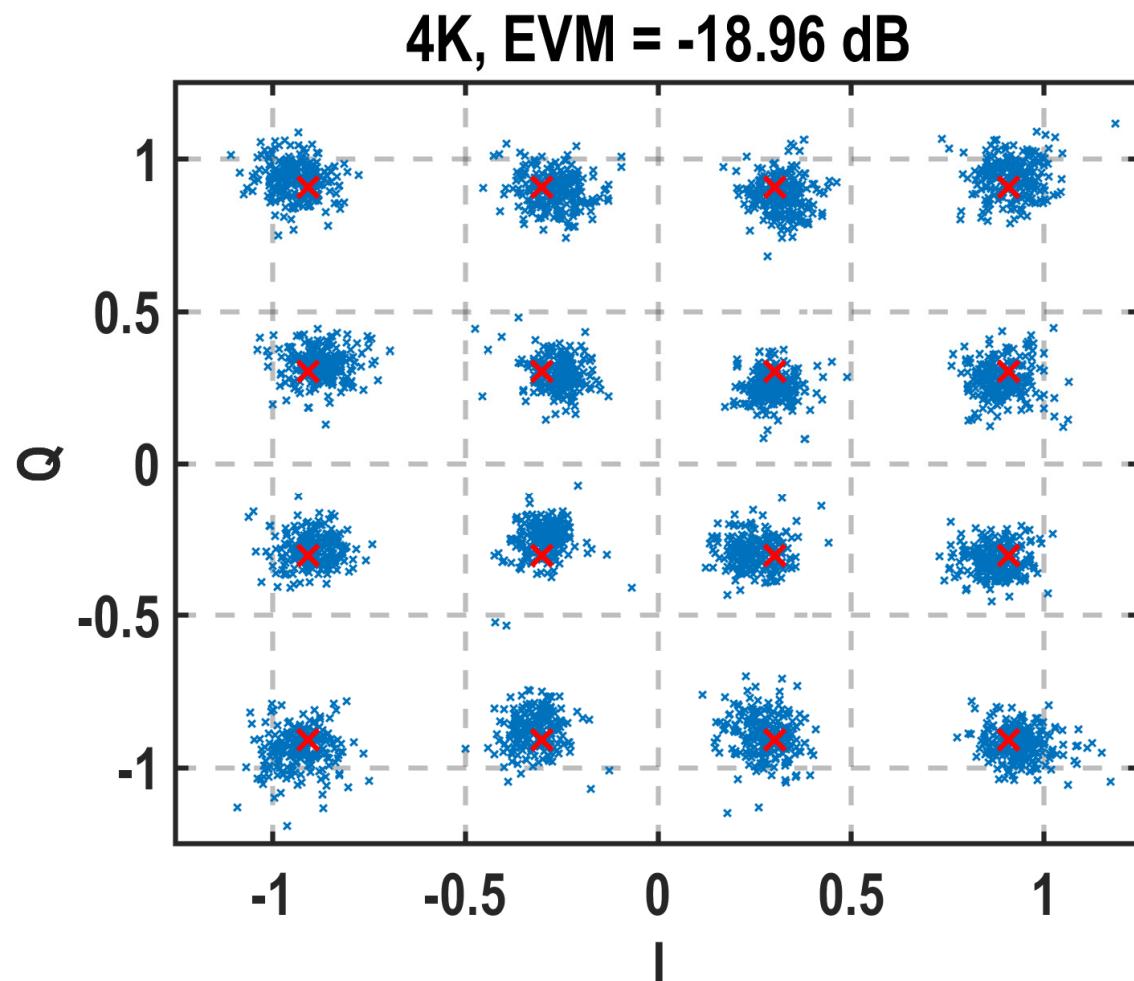
Linearity

- $\Delta f = 50$ MHz
- **IIP3:**
 - 44.9 dBm (RT)
 - 50.8 dBm (4K)
- **IP1dB:**
 - 55 dBm (RT)
 - 58.4 dBm (4K)



EVM

- 16-QAM -70 dBm input
- 200 MHz Baseband LPF



Comparison Table

| | This work | | RT Rack mount |
|-------------------|---------------------------------|---------------------------------|------------------|
| Operating Temp. | 300 K | 4 K | 300 K |
| Technology | Bulk CMOS 40nm | | - |
| Operating Freq. | 6 - 8 GHz | | 4 - 8 GHz |
| Gain | 52 dB | 58 dB | 36.5 dB |
| NF (DSB) | 2.5 dB | 0.6 dB | 1.9 dB |
| IIP3 | -44.9 dBm ($\Delta=50$ MHz) | -50.8 dBm ($\Delta=50$ MHz) | -9.2 dBm* |
| IP1dB | -55 dBm | -58.4 dBm | -19.2 dBm* |
| Power Dissipation | 70 mW | 66 mW | 3 W [#] |
| Area | 0.68 mm ² | | Rack mount |

* Linearity performance only considering the commercial LNA and Mixer from the datasheet

Power excluding the SR445 Preamplifier

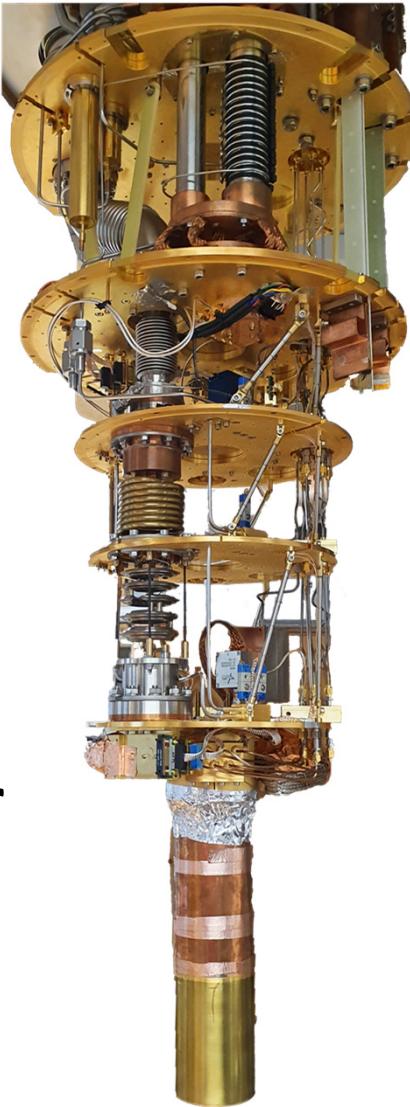
Outline

- Introduction
- Spin-Qubit Readout
- System Architecture
- Electrical Performance
- **Spin-Qubit Readout Experiment**
- Conclusions

Readout Setup

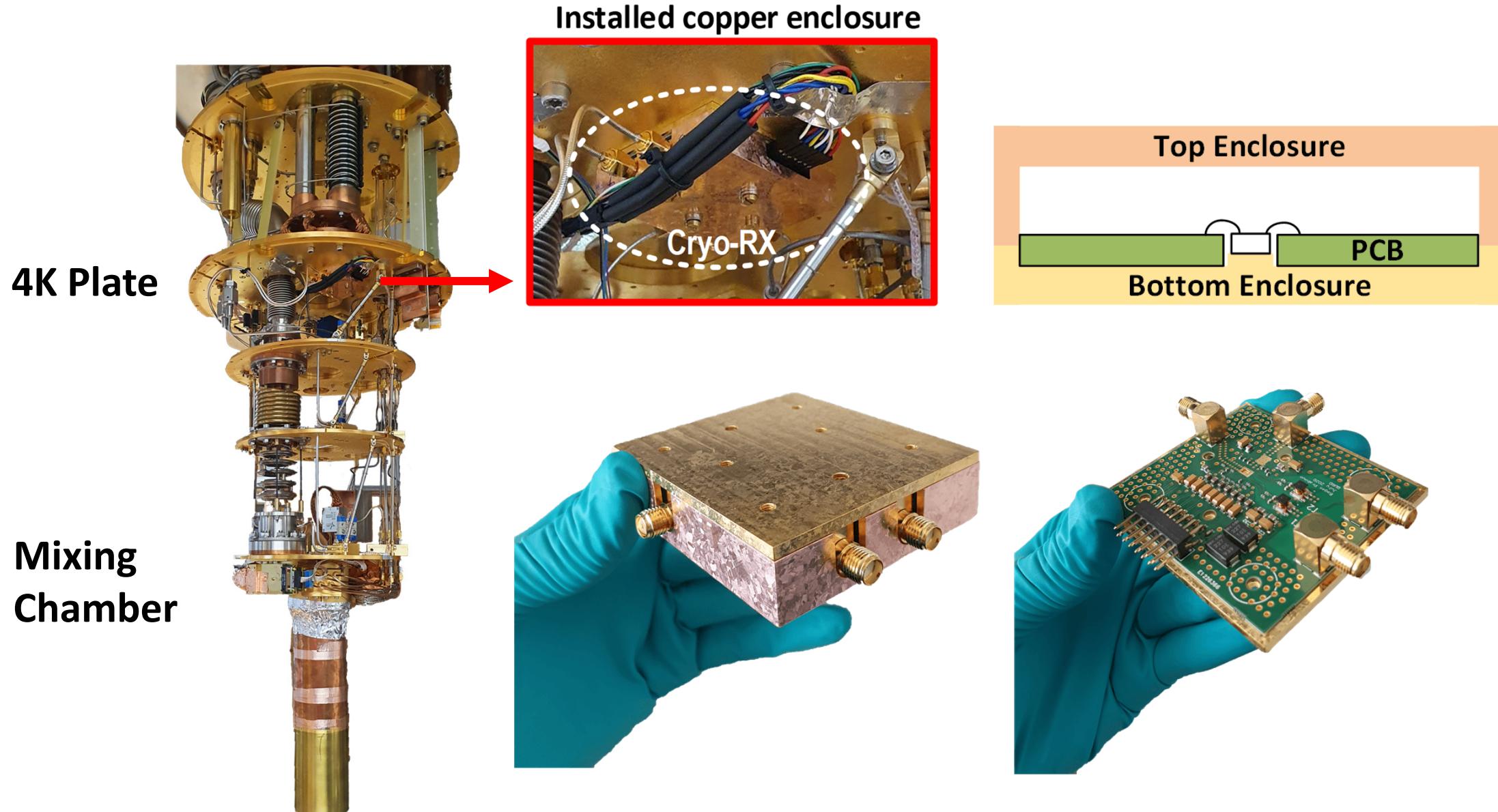
4K Plate

Mixing
Chamber



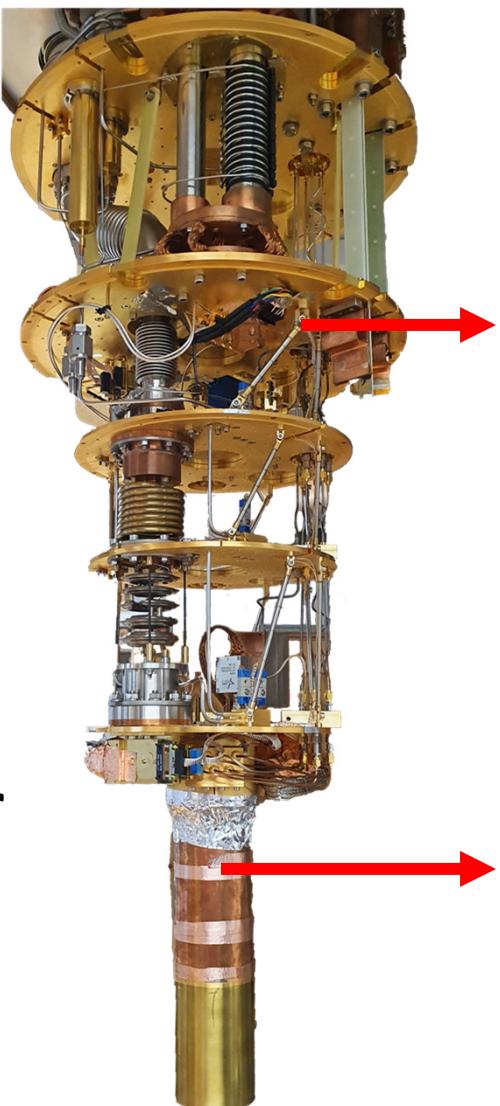
13.3: A 6-to-8GHz 0.17mW/Qubit Cryo-CMOS Receiver for Multiple Spin Qubit Readout in 40nm CMOS Technology

Readout Setup

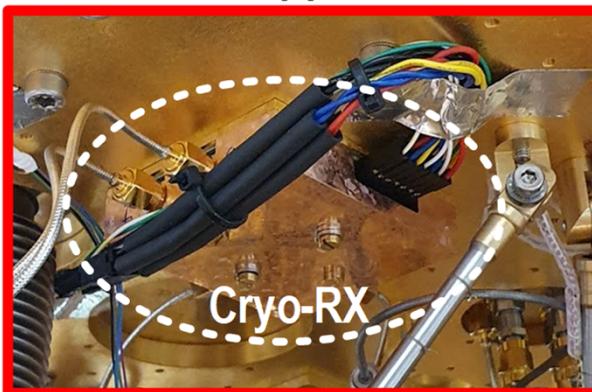


Readout Setup

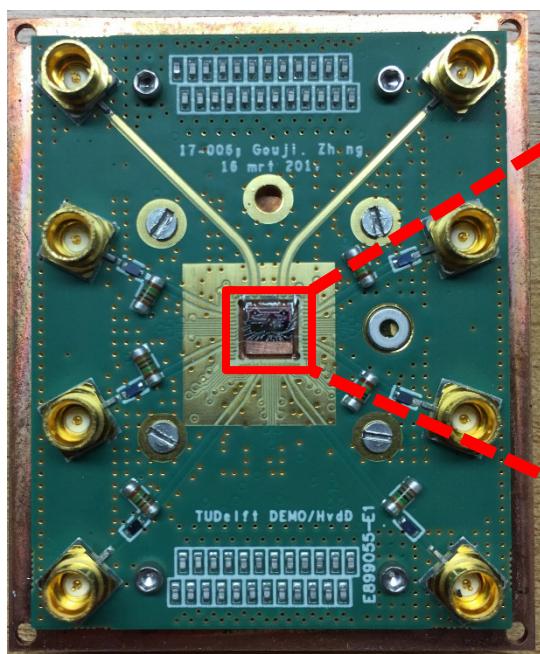
4K Plate



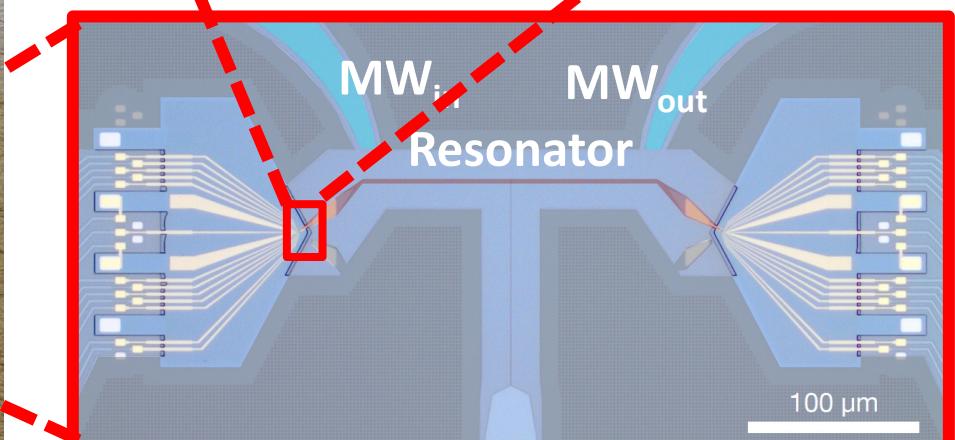
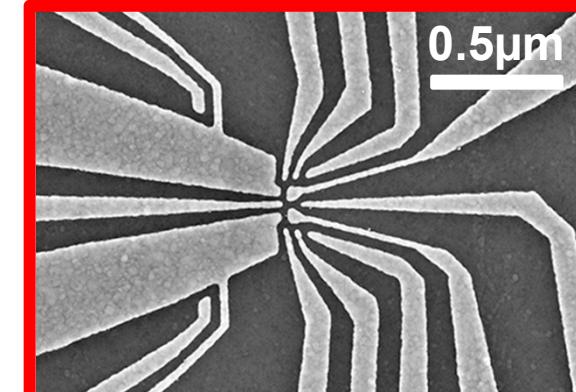
Installed copper enclosure



Mixing Chamber

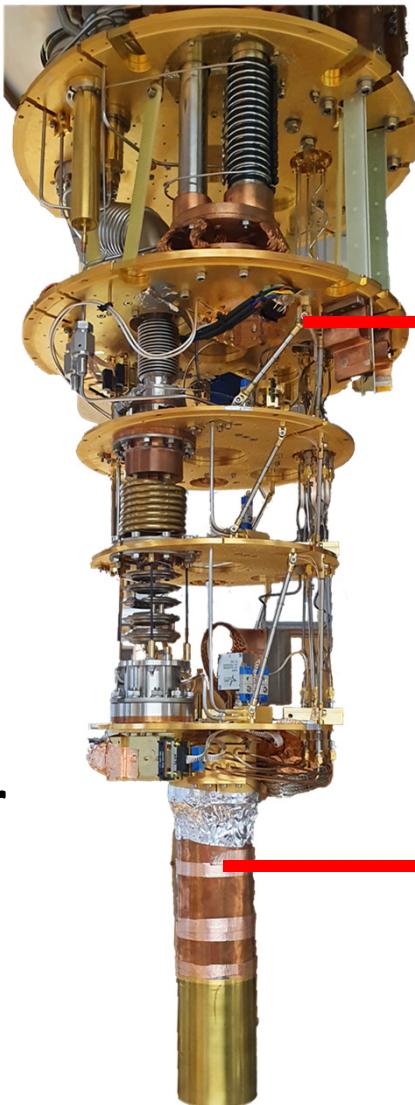


Qubit sample

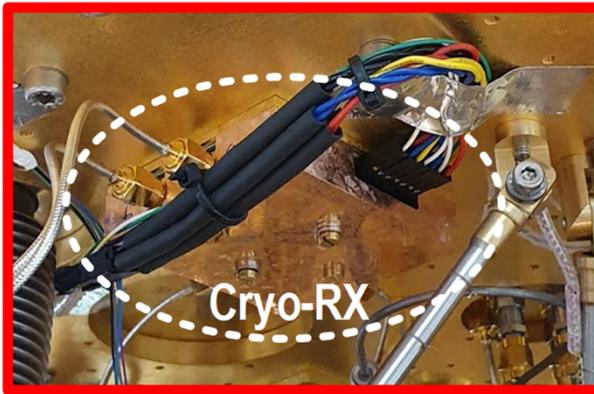


Readout Setup

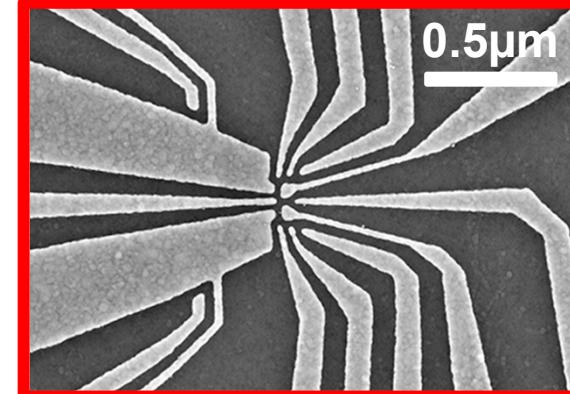
4K Plate



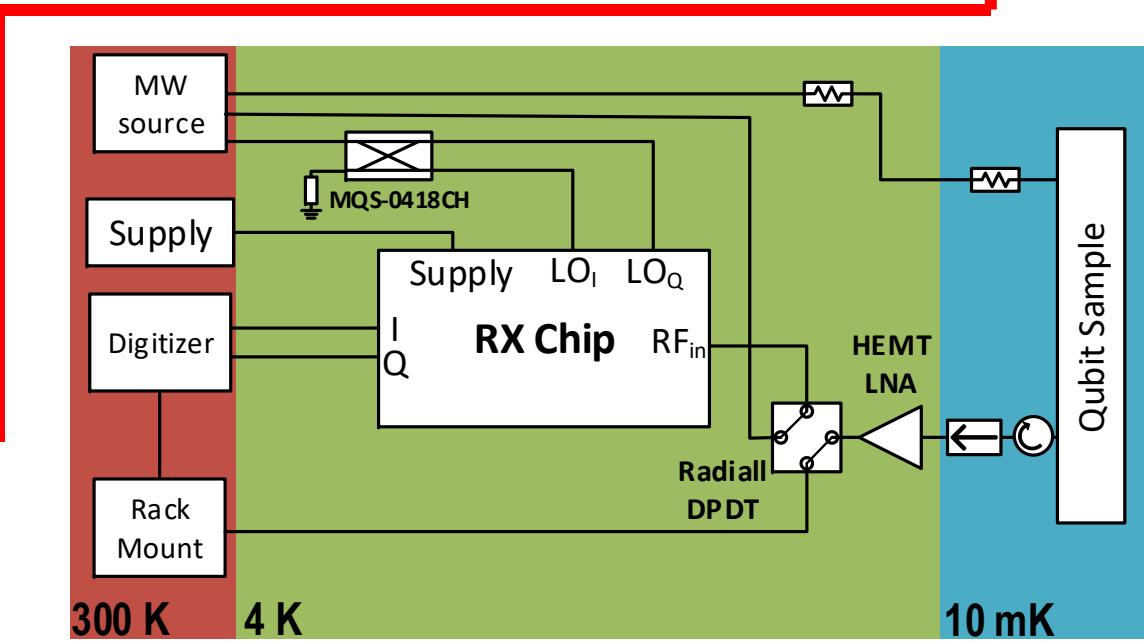
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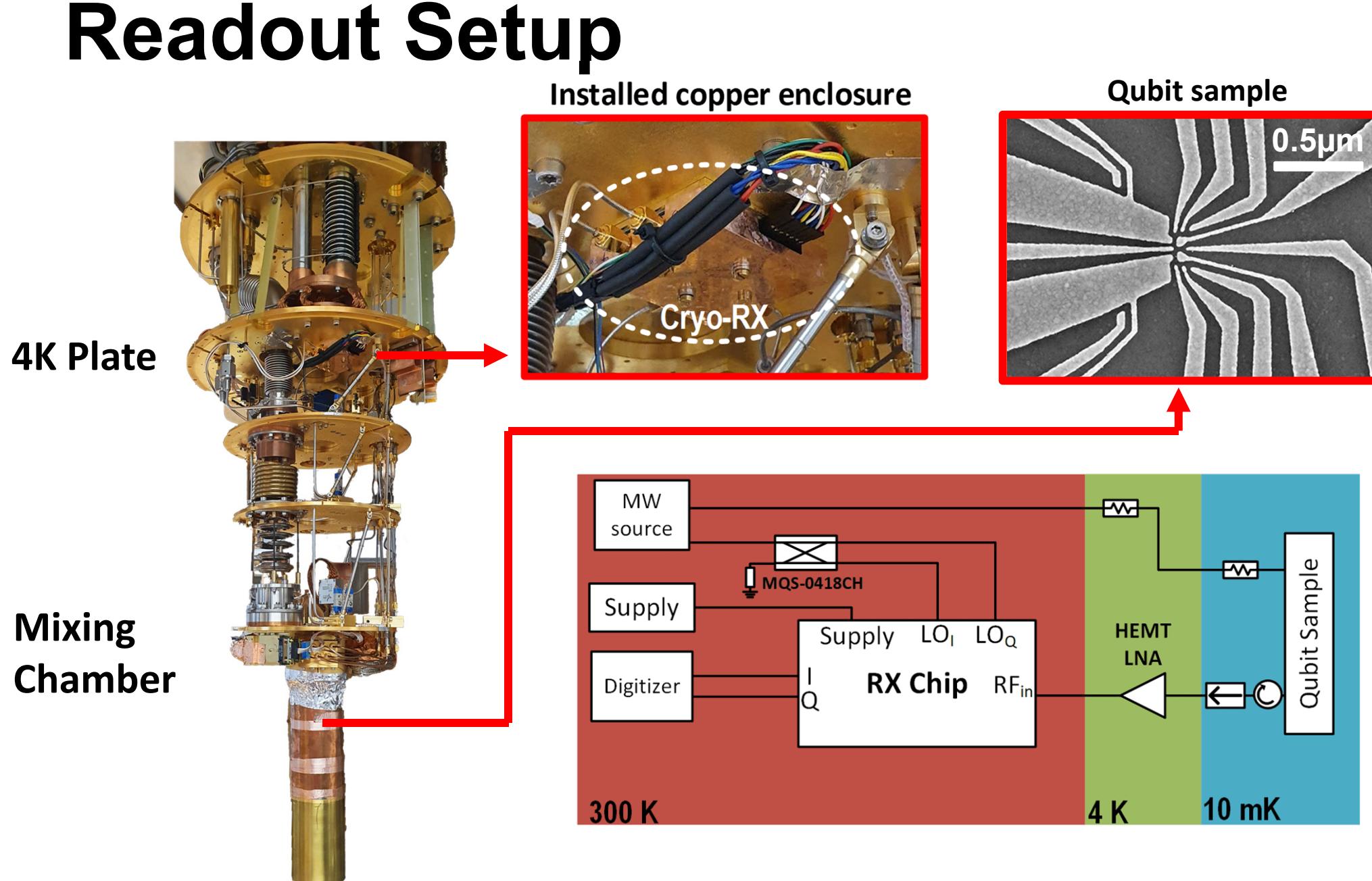
Qubit sample



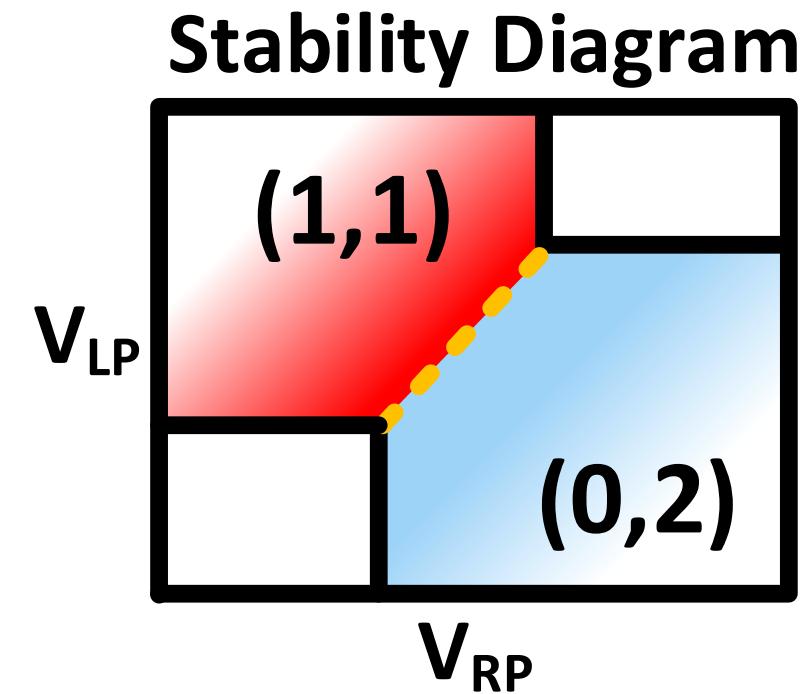
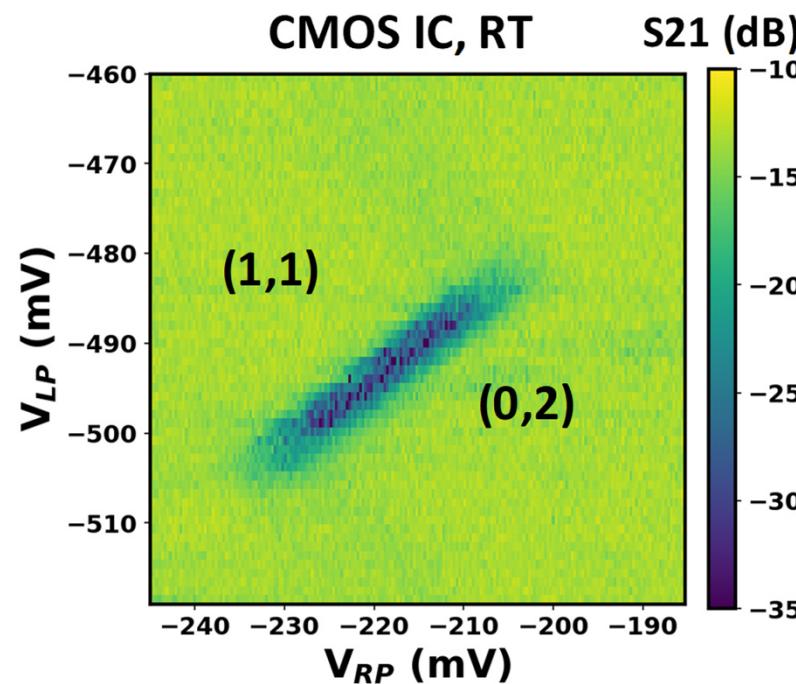
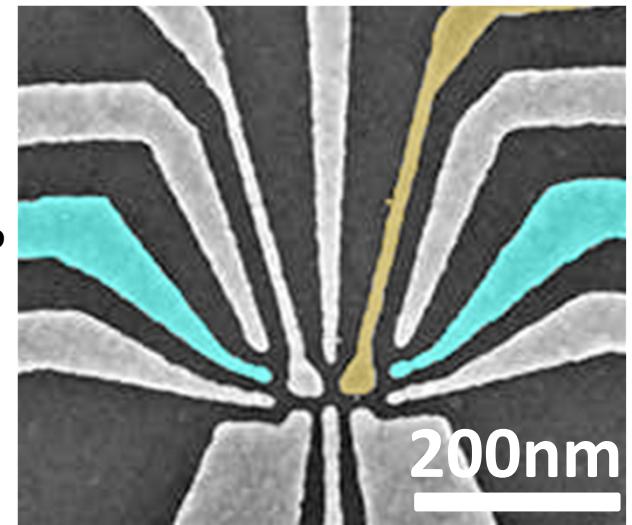
Mixing Chamber



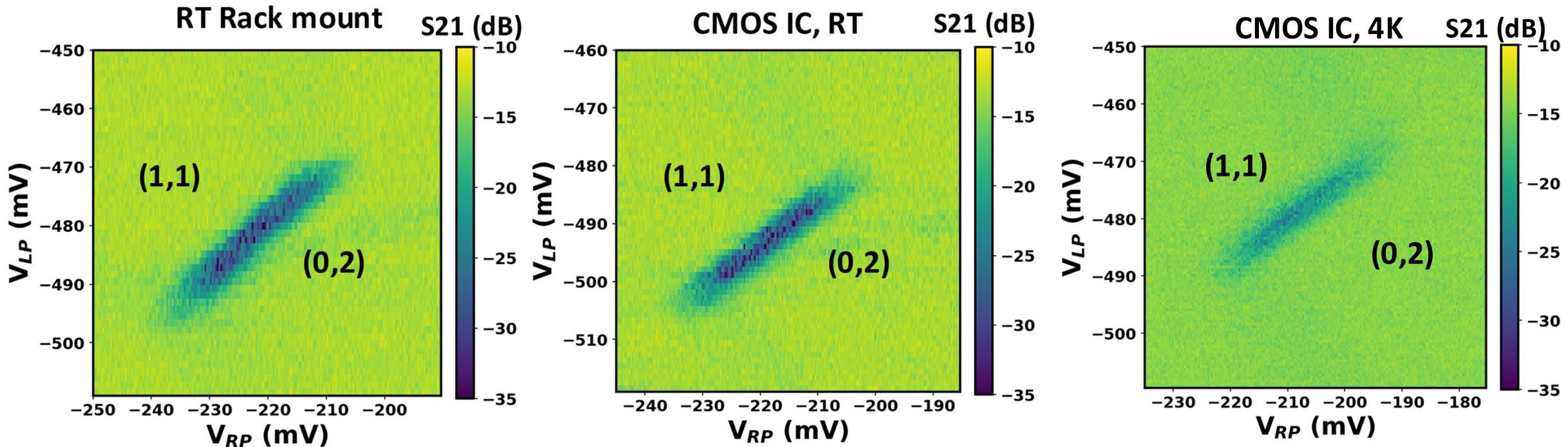
Readout Setup



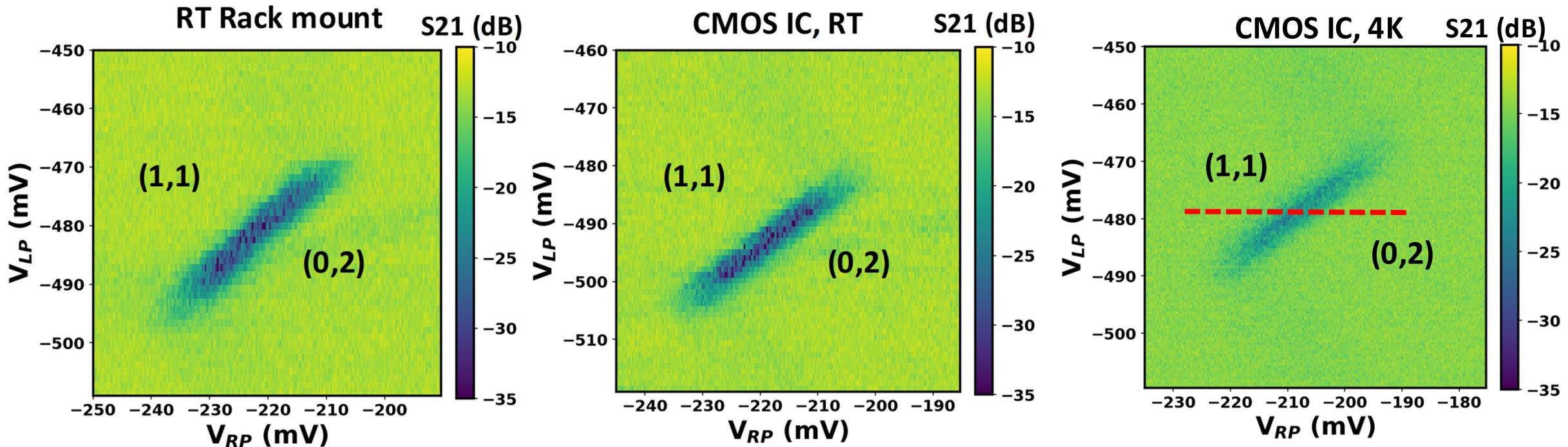
Readout Results—Stability Diagram



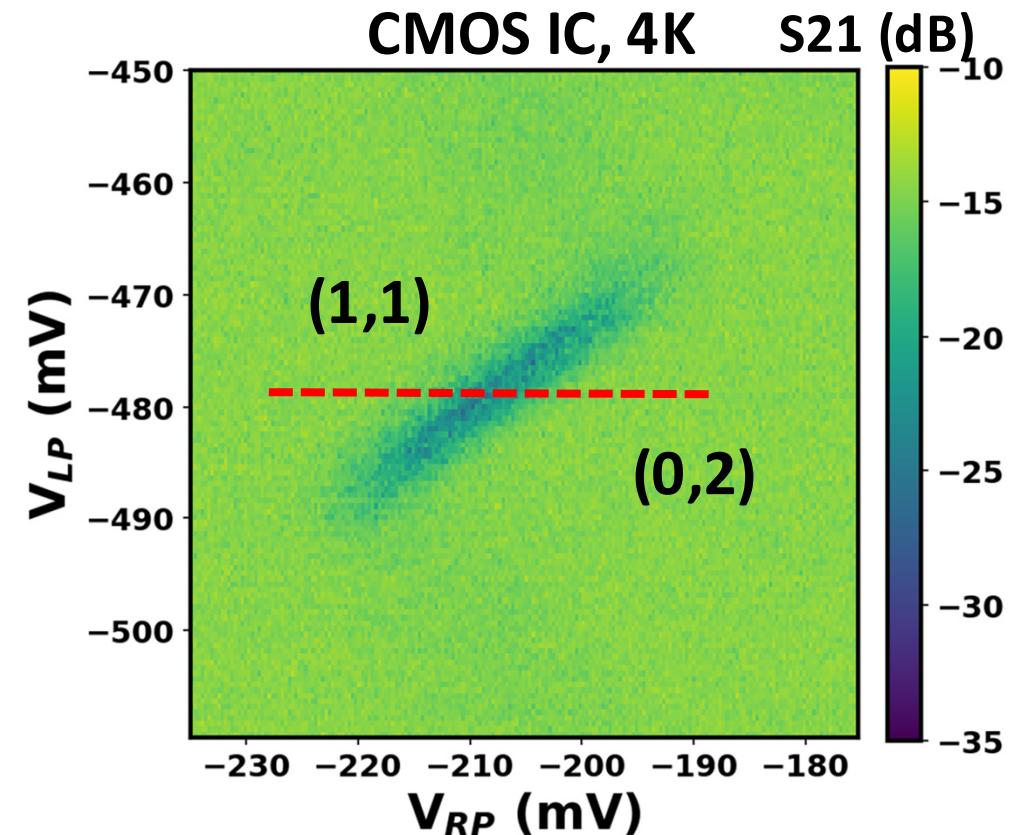
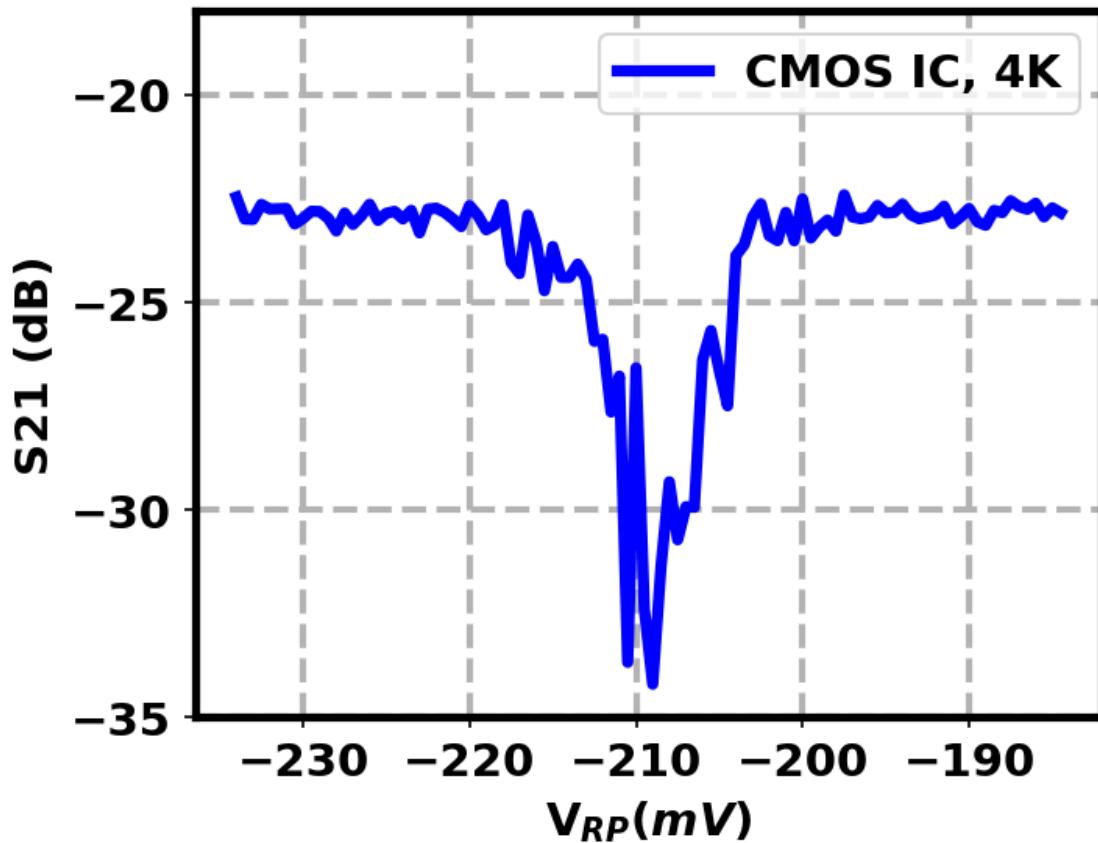
Readout Results—Stability Diagram



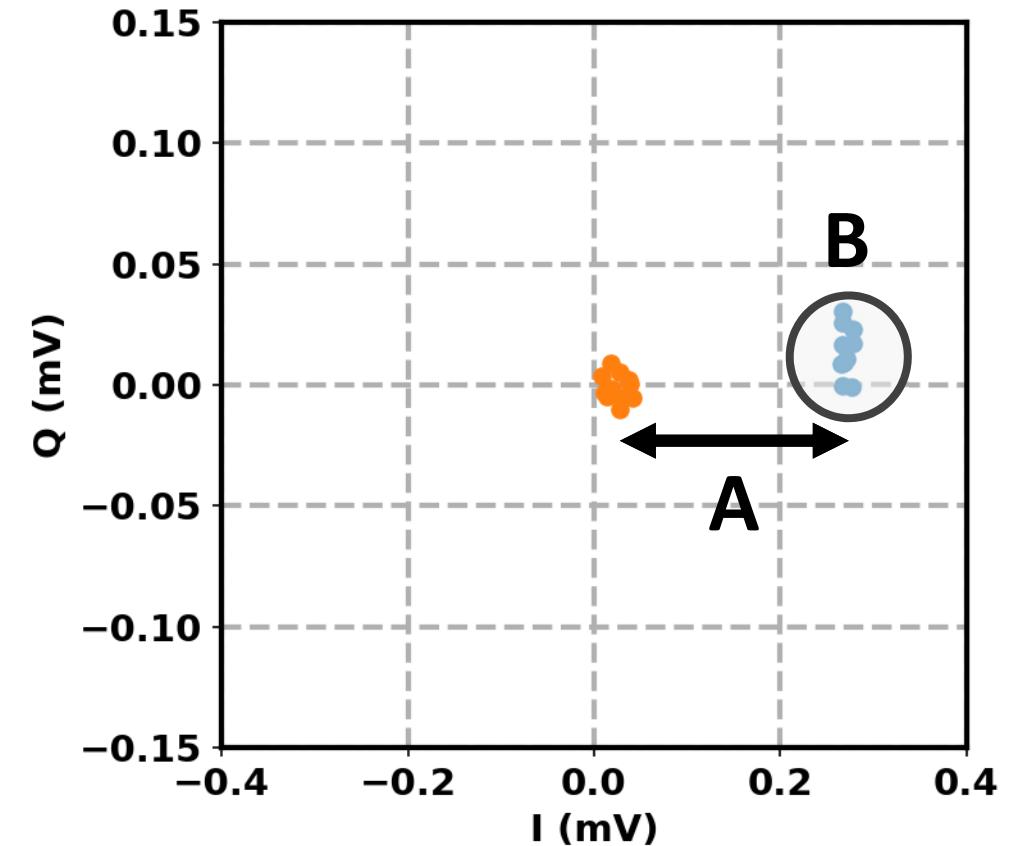
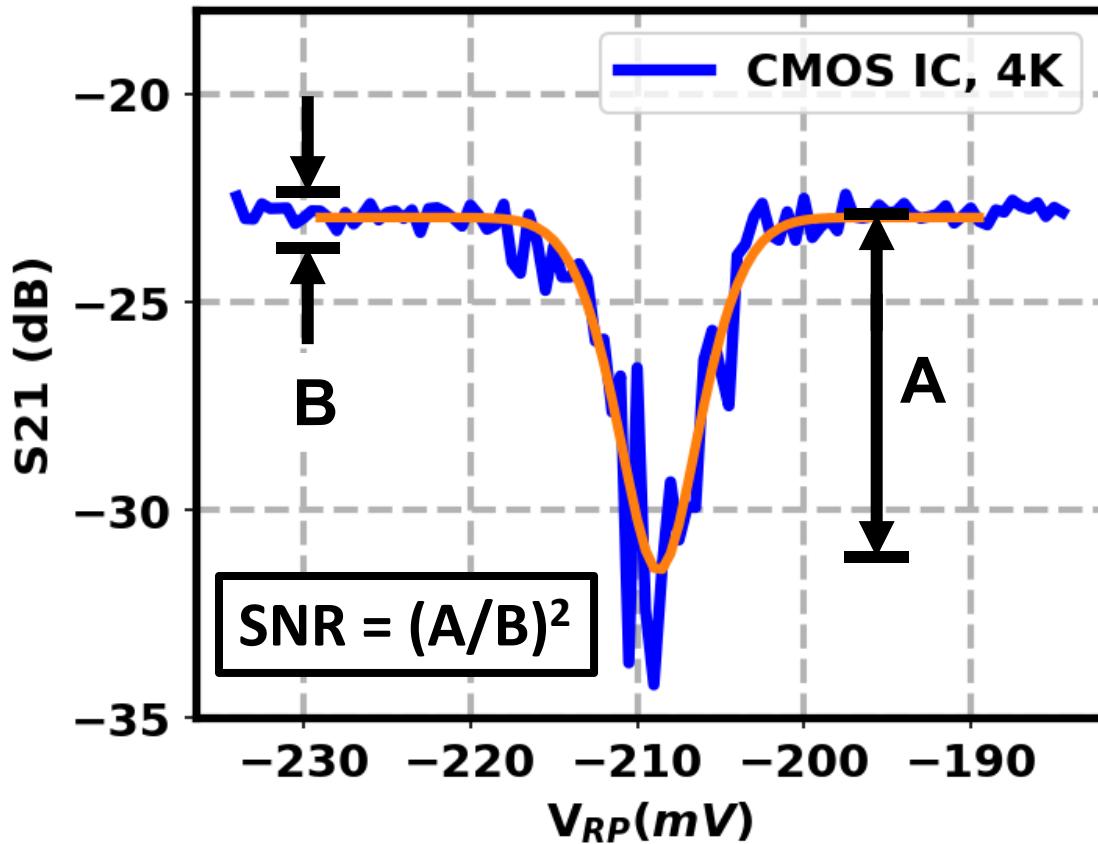
Readout Results—Stability Diagram



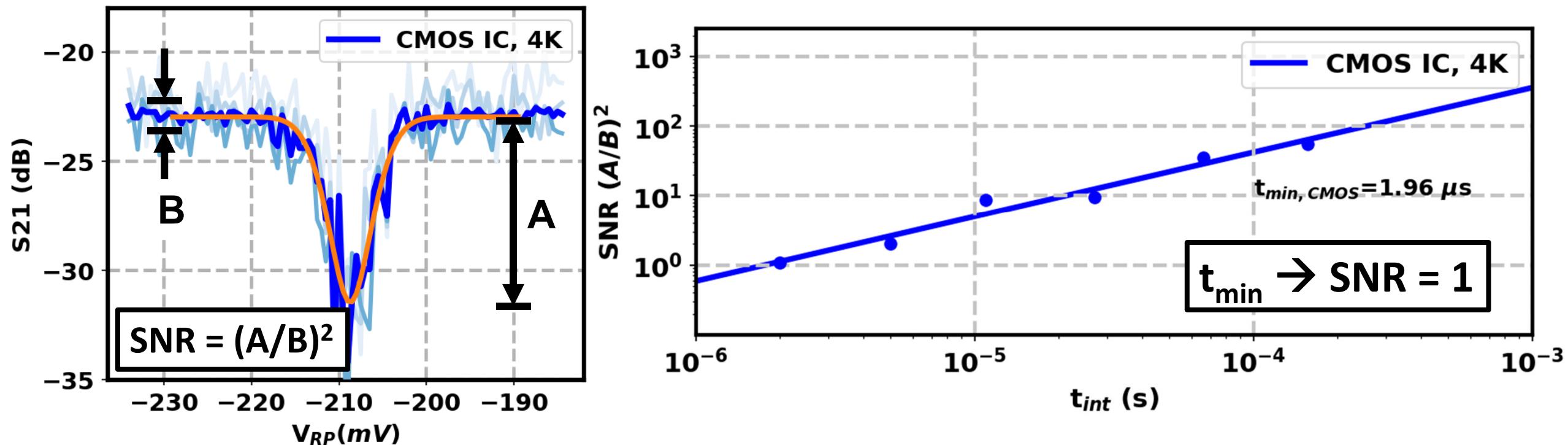
Readout Results – SNR



Readout Results – SNR



Readout Results – SNR



- SNR performance with different integration times

Comparison Table

| | This work | L. Le Guevel, ISSCC'20 |
|--|--------------------------------------|---------------------------|
| Readout scheme | Gate-based RF readout | DC readout |
| FDMA | Yes (5 MHz / qubit) | No |
| Components | LNA, Mixer, baseband amplifier | TIA |
| Operating temperature | 4.2 K | 110 mK |
| P_{DC}/qubit | 170 μ W* | 1 μ W |
| Readout BW | 2 MHz | 1.1 kHz |
| Min. readout time (t_{min}) | 1.96 μ s | 1 ms |
| Energy/Qubit⁺ | 333 pJ | 1 nJ |

* Across 2 GHz BW of RX Chip

+ Energy/qubit = (P_{DC} / qubit) x t_{min}

Conclusions

- ✓ **Scalable readout electronics for large scale quantum computer**
 - Supports FDMA
 - Operates at cryogenic temperature
- ✓ **Demonstrating the first gate-based spin qubit readout with an integrated Cryo-CMOS receiver.**
- ✓ **Achieves 0.17mW/qubit power efficiency with 2 μ s readout time**

A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS

Gerd Kiene^{1,2}, Alessandro Catania³, Ramon Overwater^{1,2}, Paolo Bruschi³,
Edoardo Charbon^{1,2,4}, Masoud Babaie^{1,2}, Fabio Sebastiani^{1,2}

¹Delft University of Technology, Delft, The Netherlands,

²QuTech, Delft, The Netherlands, ³University of

Pisa, Pisa, Italy, ⁴EPFL, Neuchatel, Switzerland



QuTech

Speaker information: Gerd Kiene



- MSc in physics from Heidelberg University
- PhD candidate in electrical engineering at TU Delft
- Research interests:
 - Cryogenic electronics
 - Novel computing paradigms (Quantum, Neuromorphic)
 - Data converters and wireline links

Outline

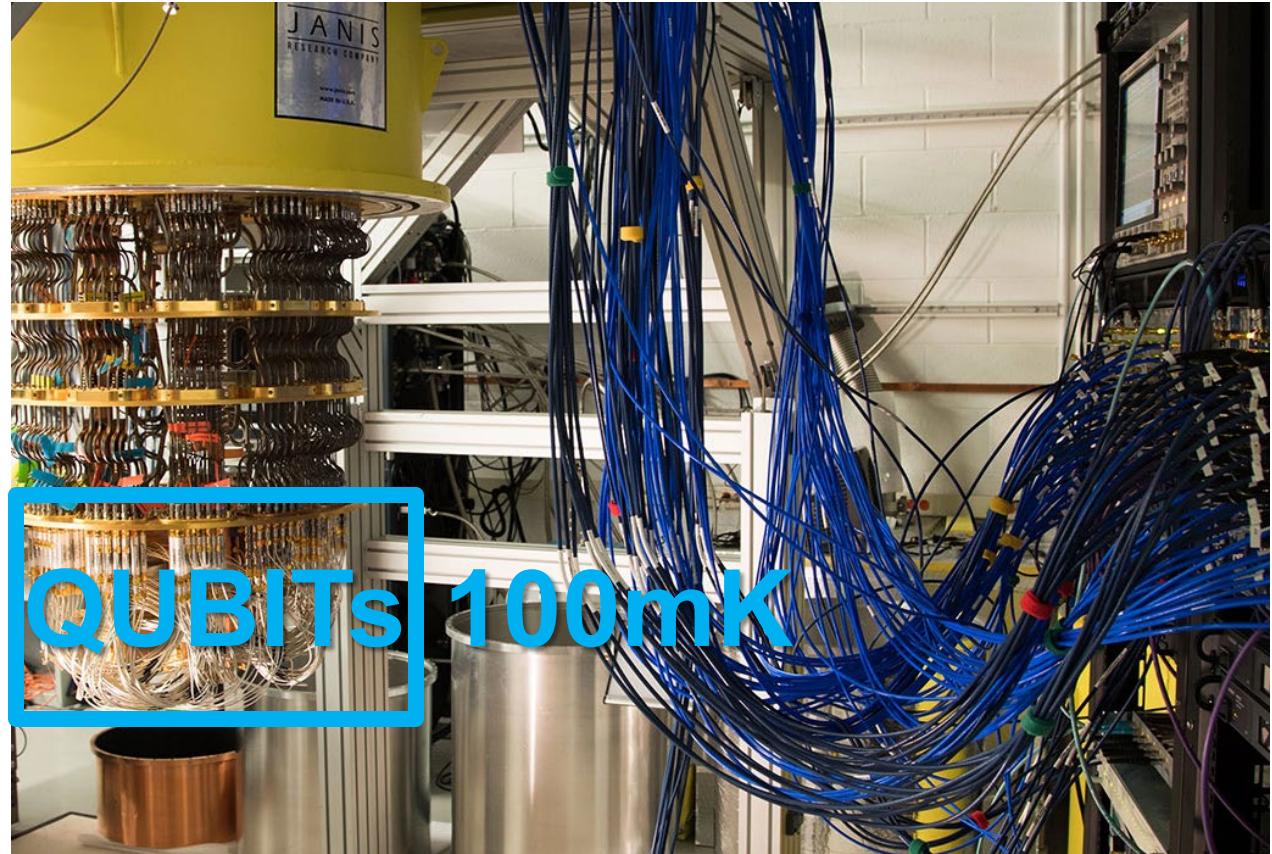
- Introduction
- Application
- Circuit implementation
- Experimental characterization
- Conclusion

Outline

- Introduction
- Application
- Circuit implementation
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Quantum computers

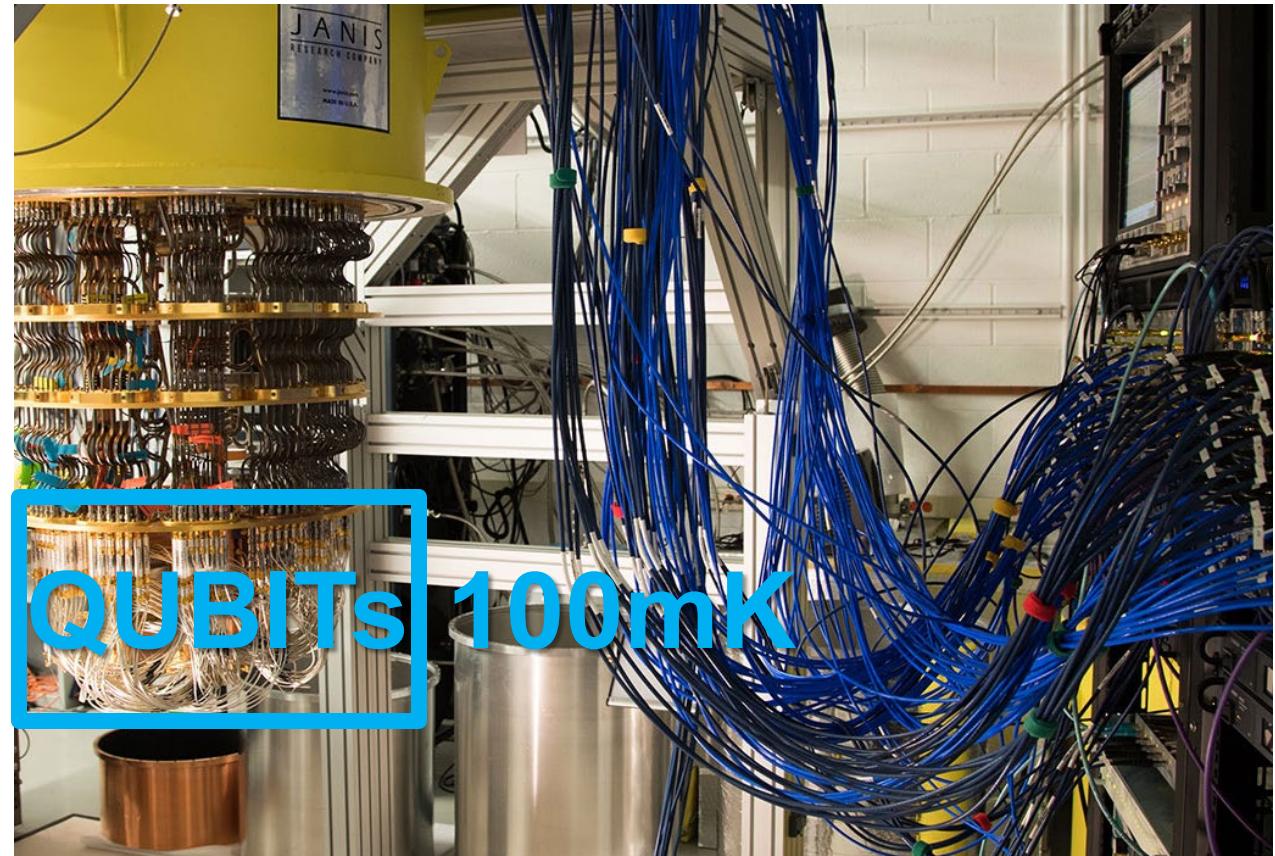
- Current: <100 qubits



[Bardin, 2019]

Quantum computers

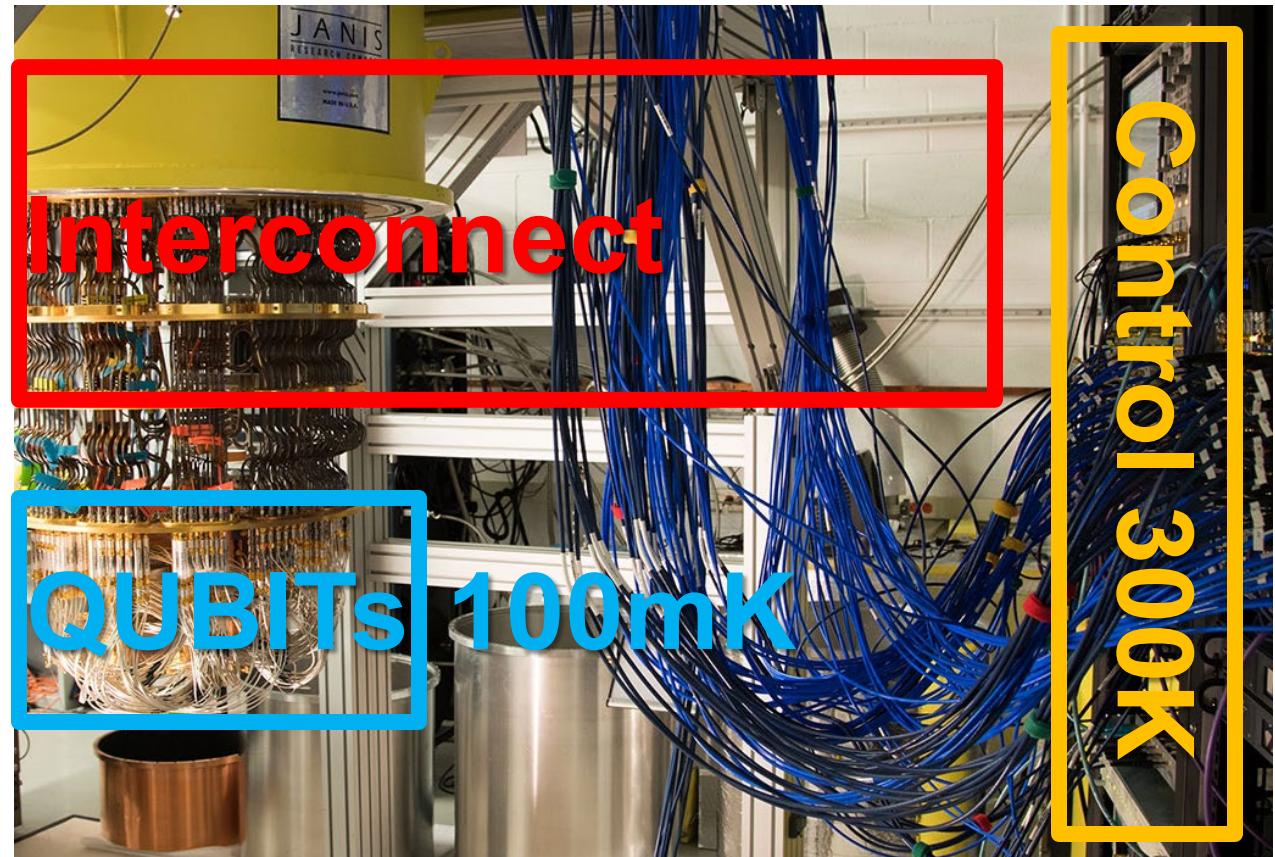
- Current: <100 qubits
- Needed:
 - ~1 Million for quantum chemistry [Reiher, 2017]



[Bardin, 2019]

Quantum computers

- Current: <100 qubits
- Needed:
 - ~1 Million for quantum chemistry [Reiher, 2017]
- Scaling problem of control:
 - Reliability
 - Physical constraints



[Bardin, 2019]

Quantum computers

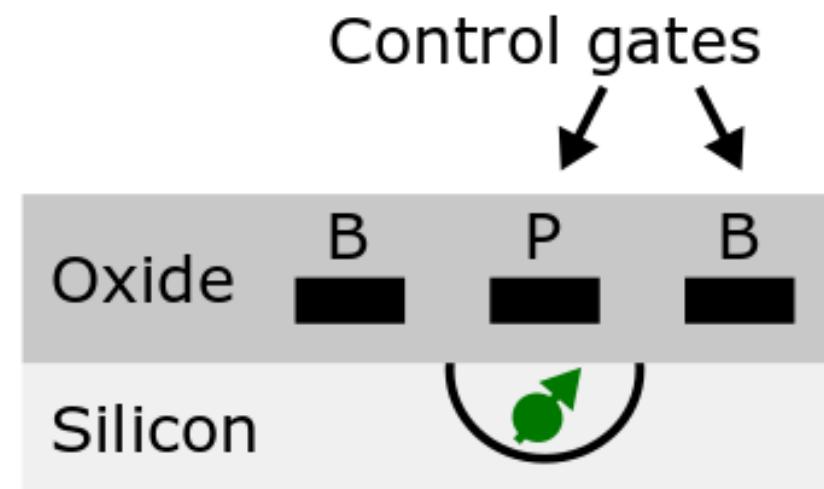
- Current: <100 qubits
- Needed:
 - ~1 Million for quantum chemistry [Reiher, 2017]
- Scaling problem of control:
 - Reliability
 - Physical constraints
- Integrated cryogenic interface needed



[Bardin, 2019]

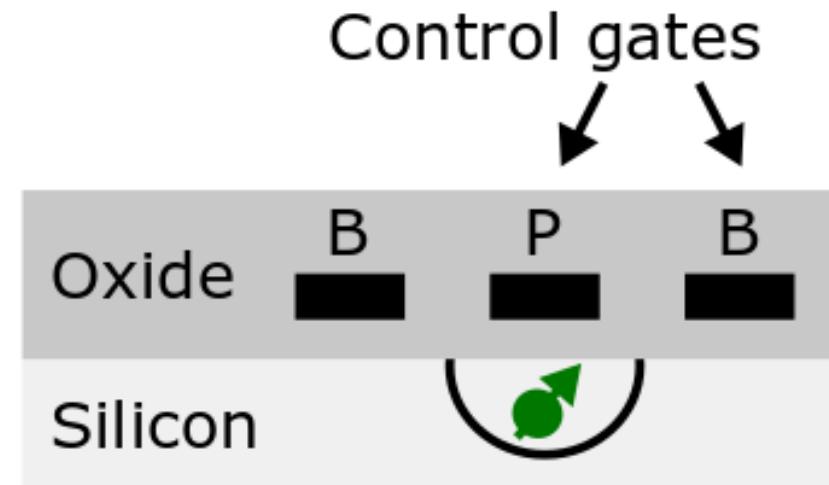
Spin qubits

- Advantages
 - MOS compatible



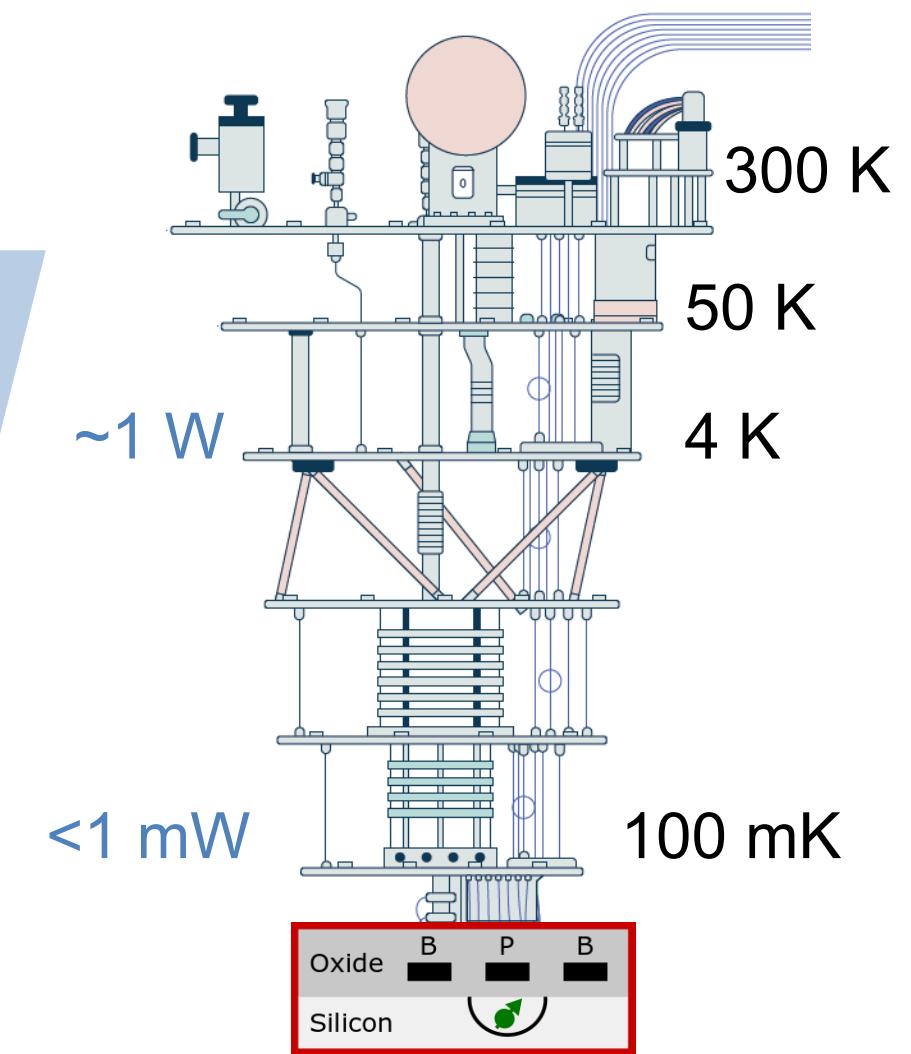
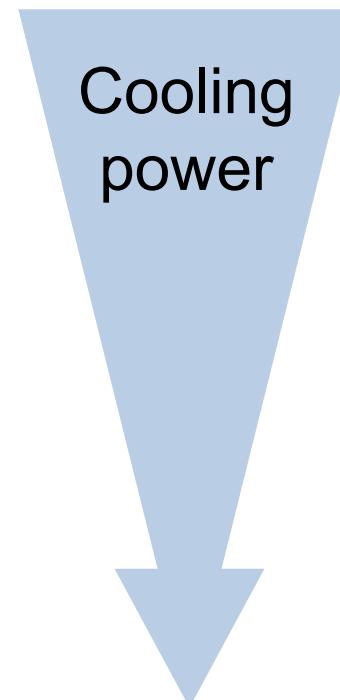
Spin qubits

- Advantages
 - MOS compatible
 - Operational to $T > 1\text{K}$
- [Yang, 2019; Petit, 2020]



Spin qubits

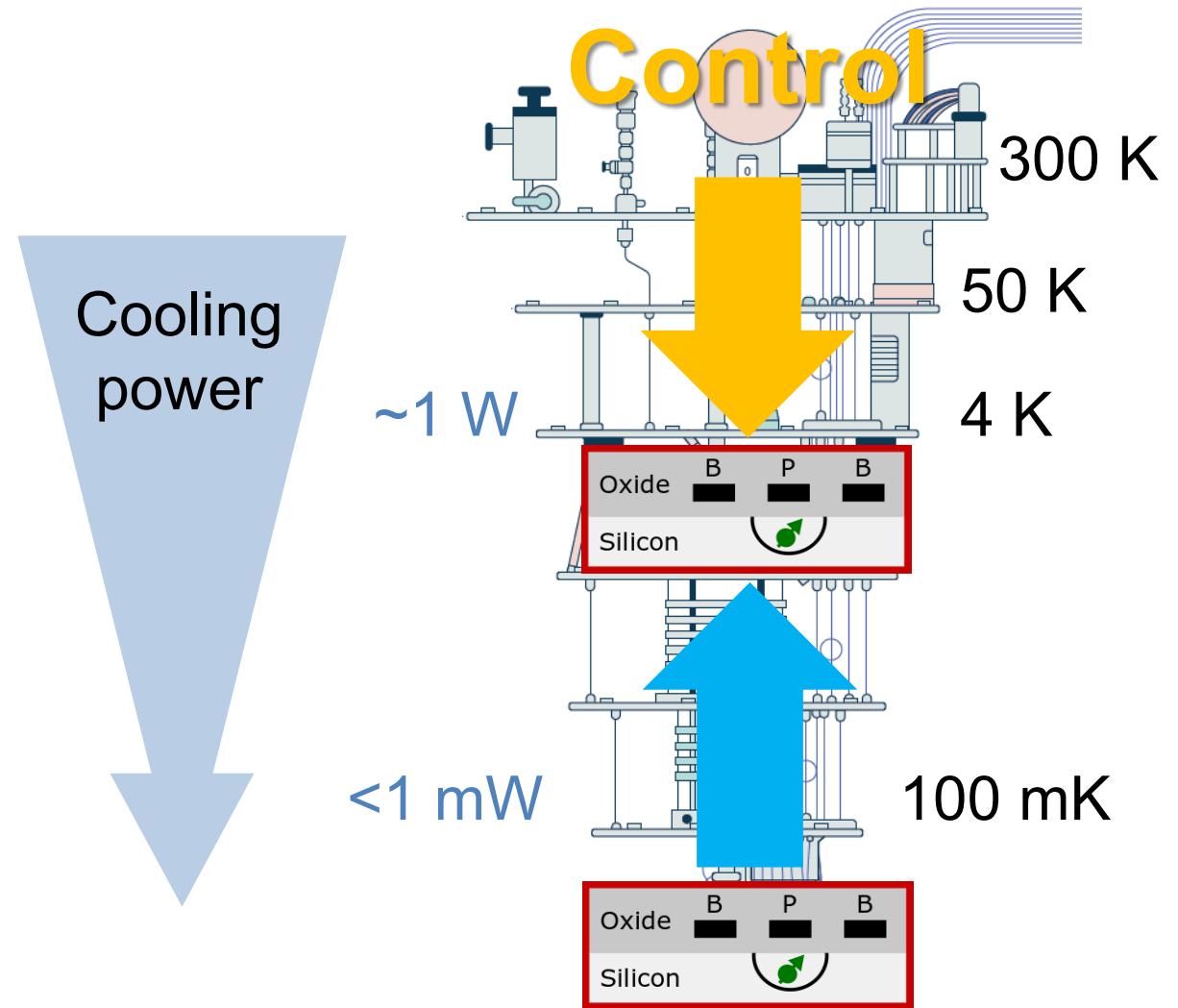
- Advantages
 - MOS compatible
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[Yang, 2019; Petit, 2020]



13.4: A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS

Spin qubits

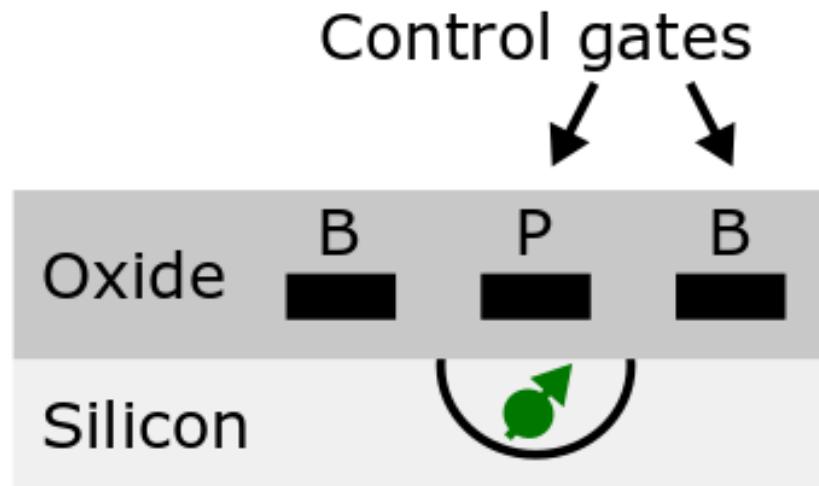
- Advantages
 - MOS compatible
 - Operational to $T > 1\text{K}$
[Yang, 2019; Petit, 2020]
- Vision:
 - Integrate qubits and control



13.4: A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS

Spin qubits

- Advantages
 - MOS compatible
 - Operational to $T > 1\text{K}$
[Yang, 2019; Petit, 2020]
- Vision:
 - Integrate qubits and control
- Here: readout of spin qubits



Outline

- Introduction
- Application
- Circuit implementation
- Experimental characterization
- Conclusion

Readout of spin qubits

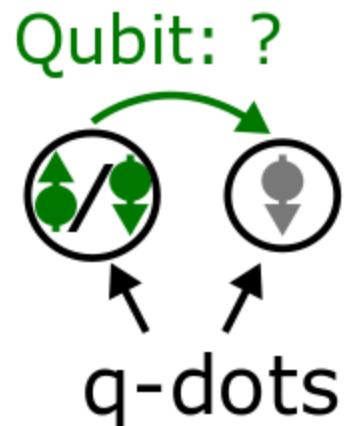
Qubit: ?



q-dot

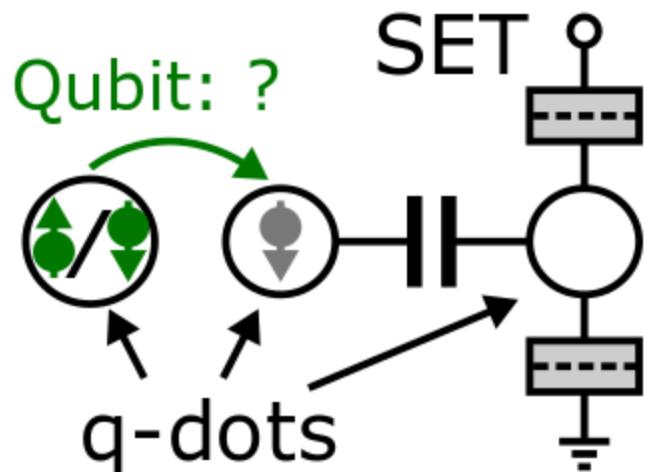
Readout of spin qubits

- Resistive readout
 - Spin-to-charge conversion with Pauli exclusion principle



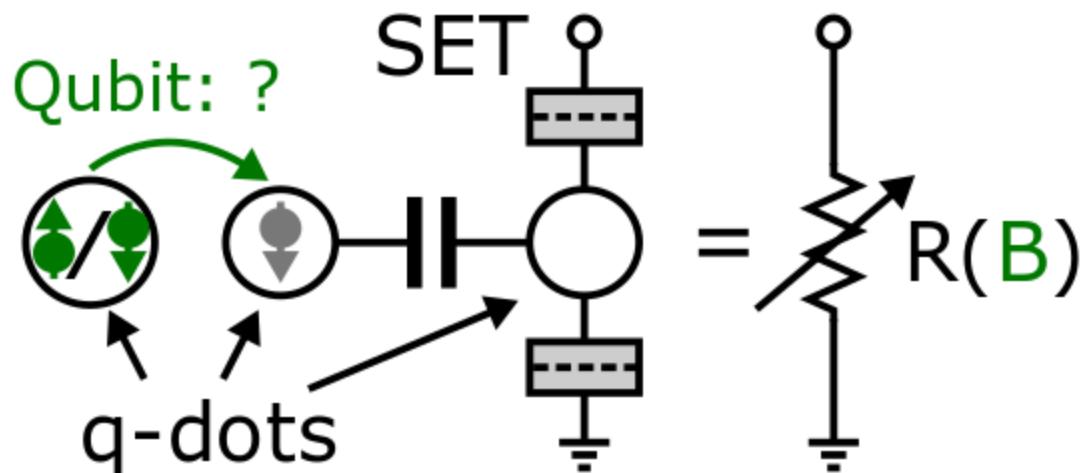
Readout of spin qubits

- Resistive readout
 - Spin-to-charge conversion with Pauli exclusion principle
 - Charge sensing with single electron transistor (SET)



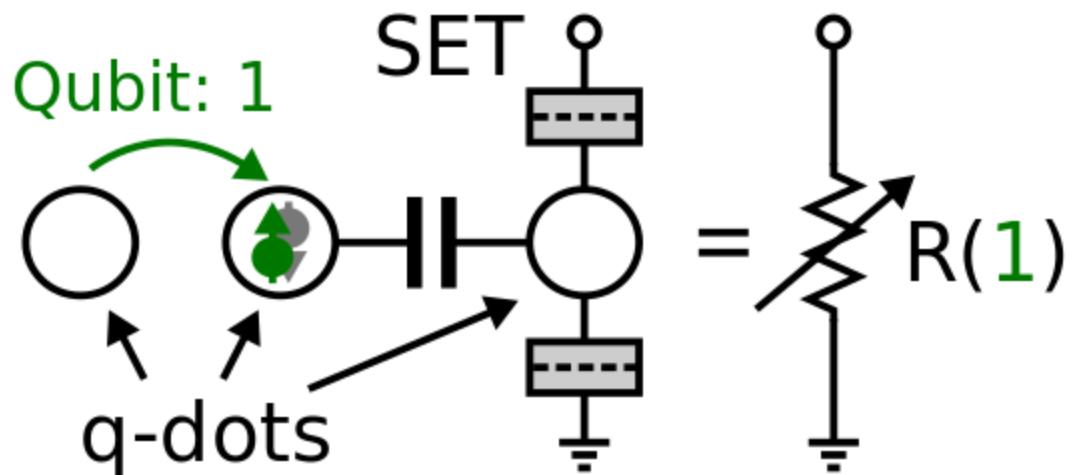
Readout of spin qubits

- Resistive readout
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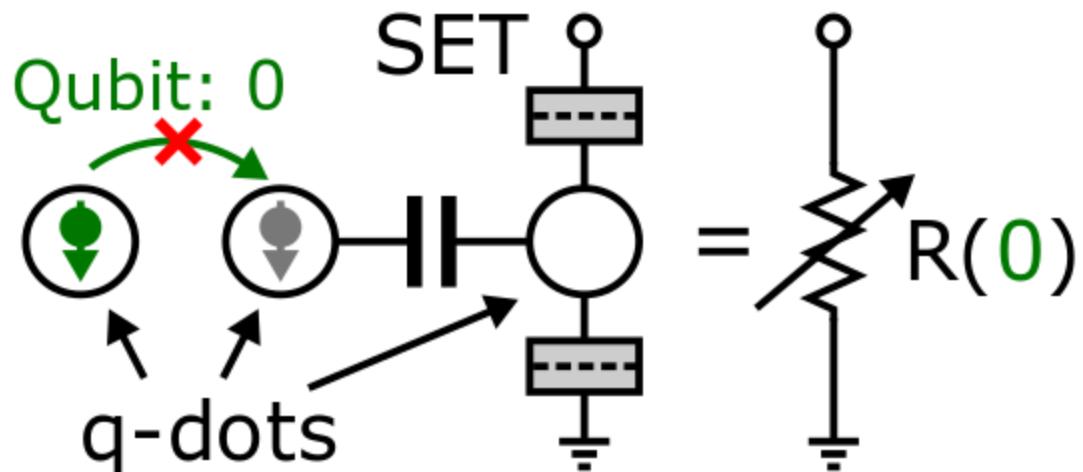
Readout of spin qubits

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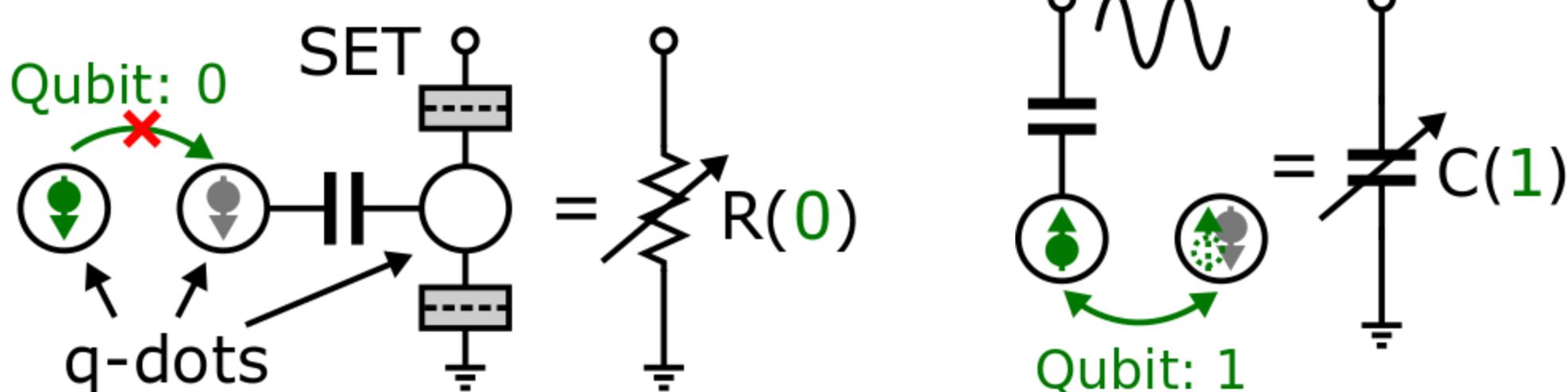
Readout of spin qubits

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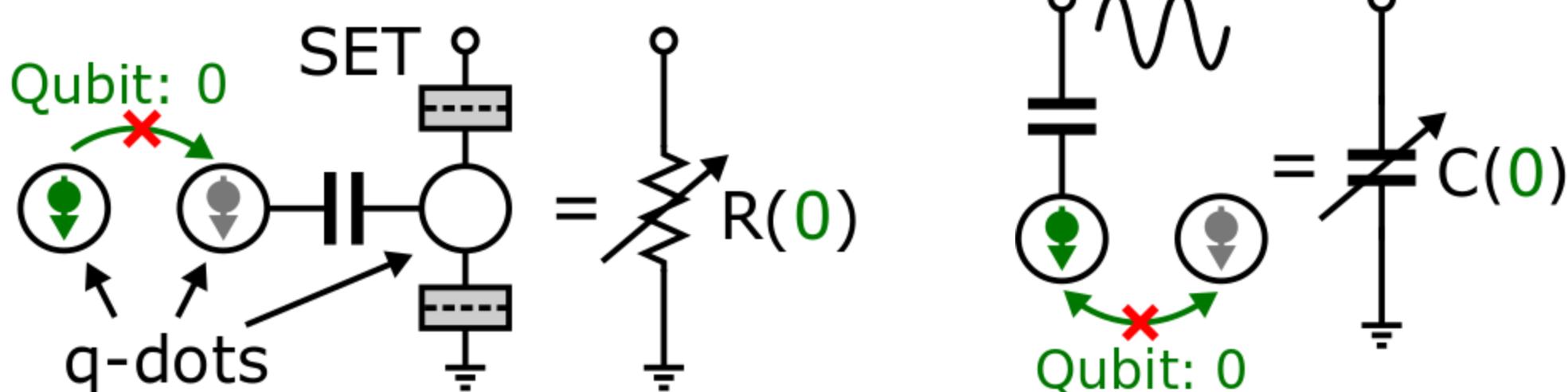
Readout of spin qubits

- Resistive readout
 - Spin-to-charge conversion with Pauli exclusion principle
 - Charge sensing with single electron transistor (SET)
- Gate-based
 - Quantum capacitance as function of qubit state



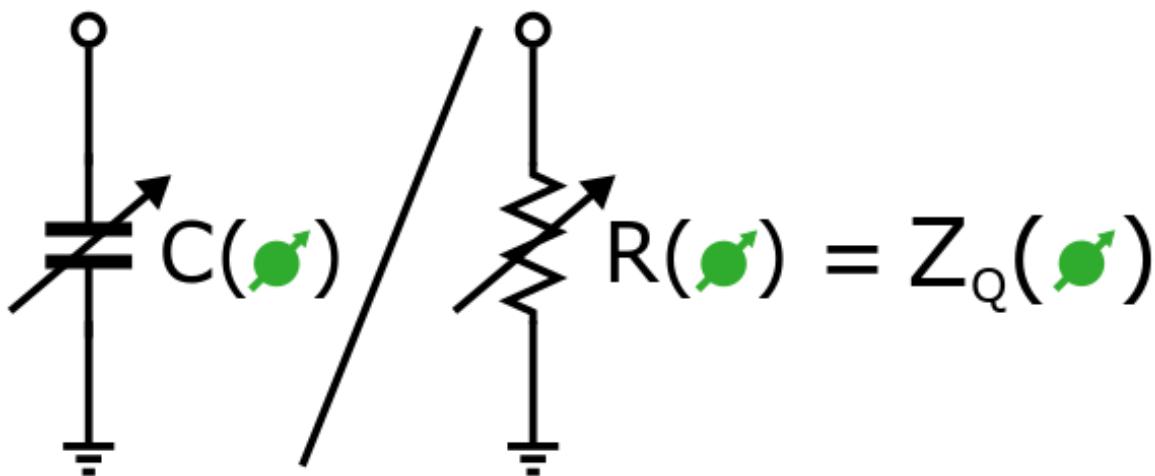
Readout of spin qubits

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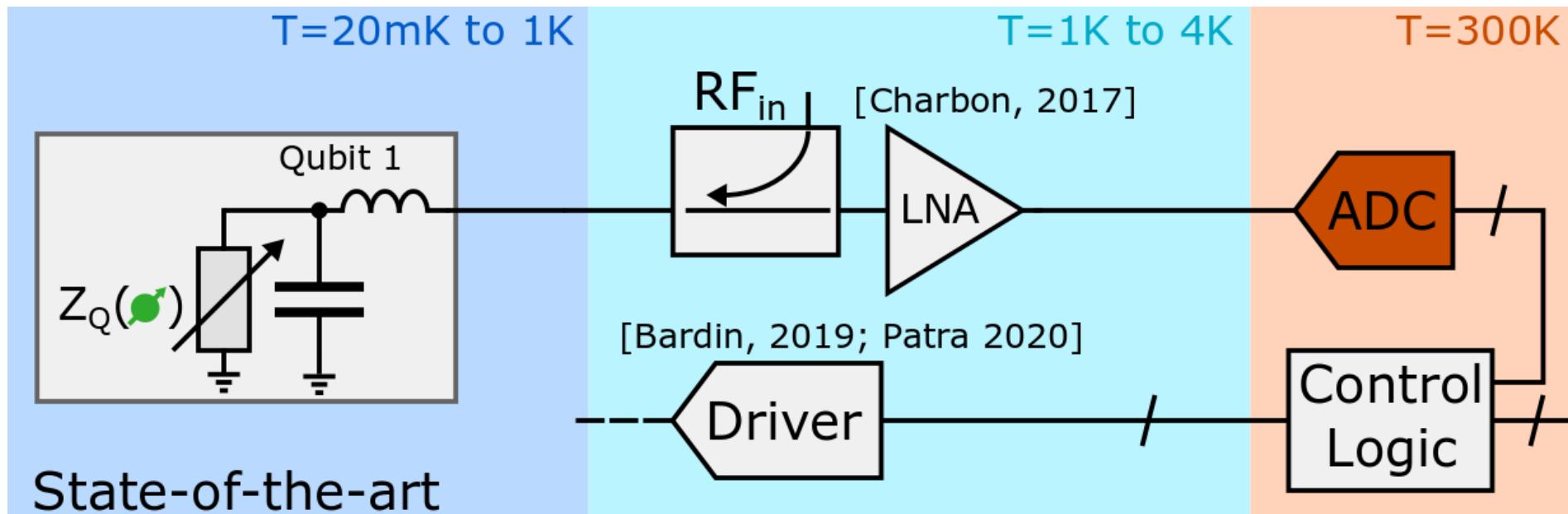
Readout of spin qubits

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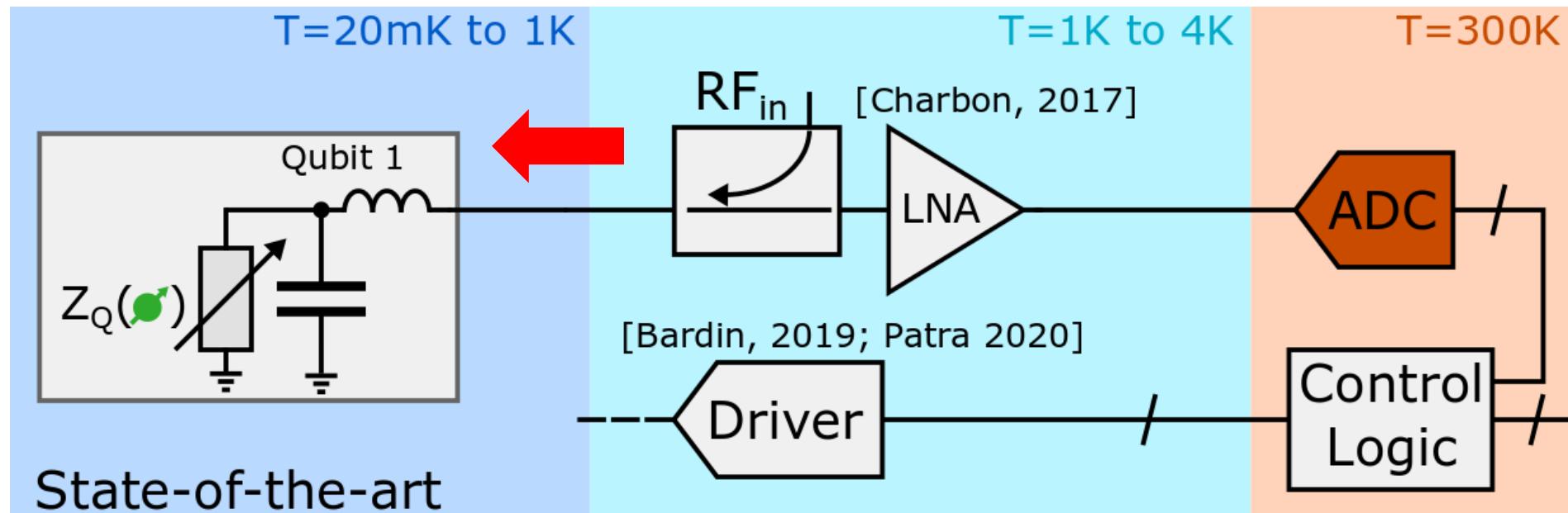
Generic RF readout chain

- Reflectometry setup to read the Z_Q quantum impedance
 - Excite matching network with RF_{in}
 - Amplify with LNA
 - Digitize with ADC



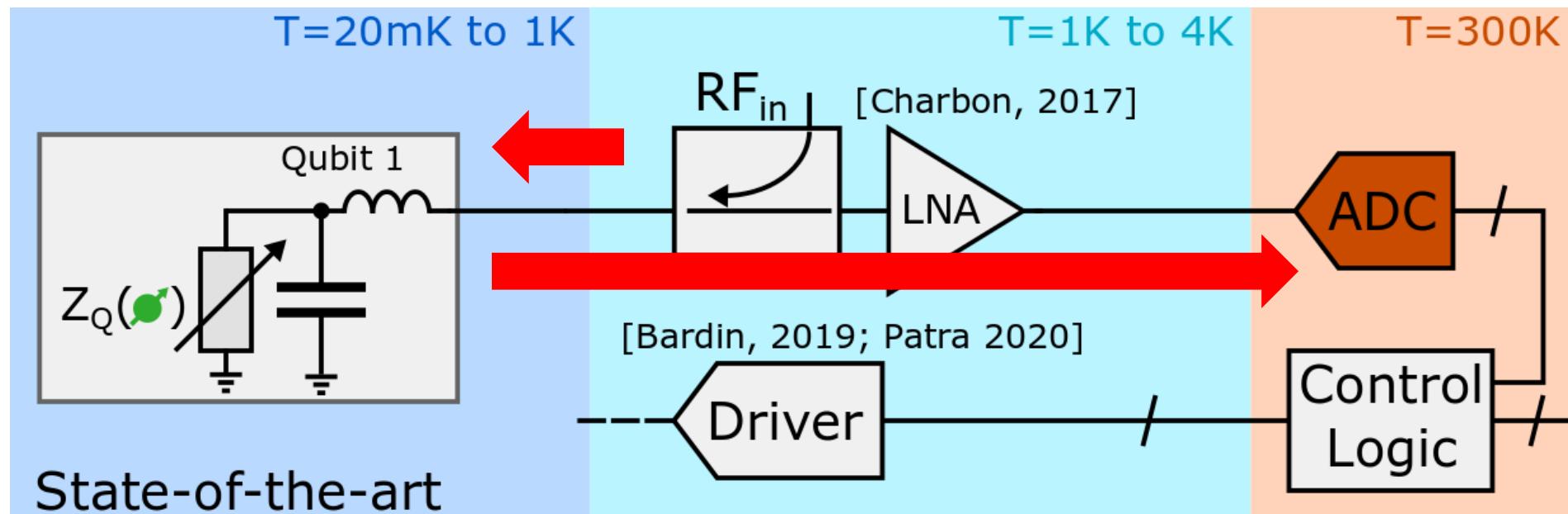
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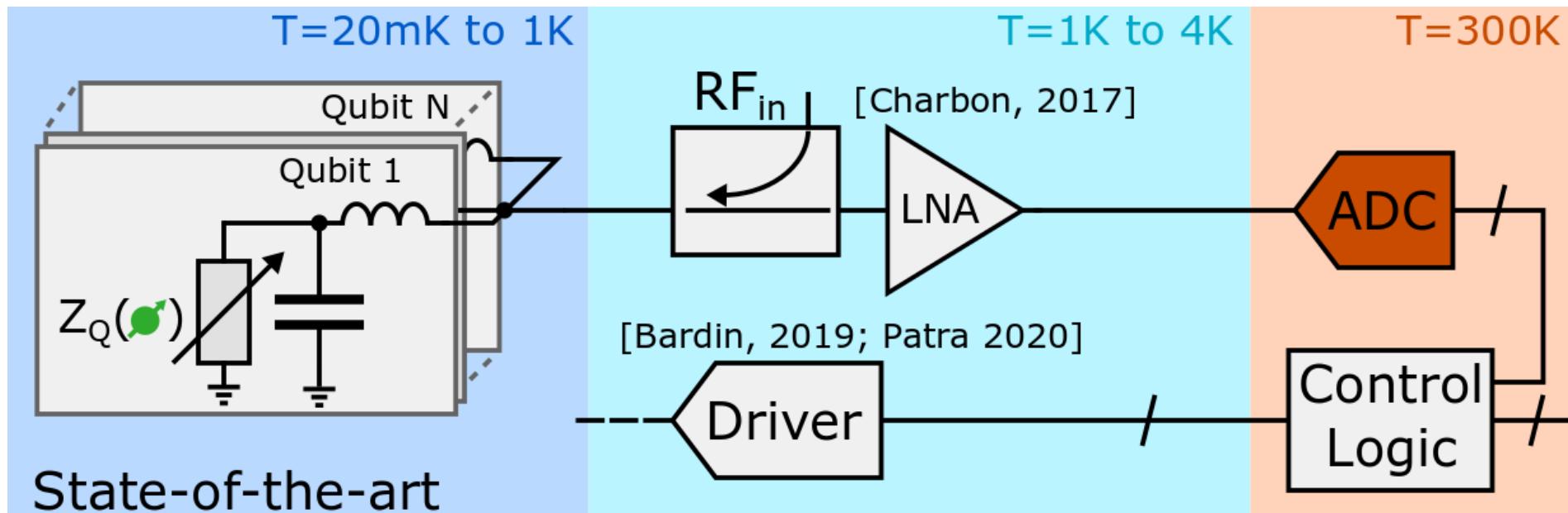
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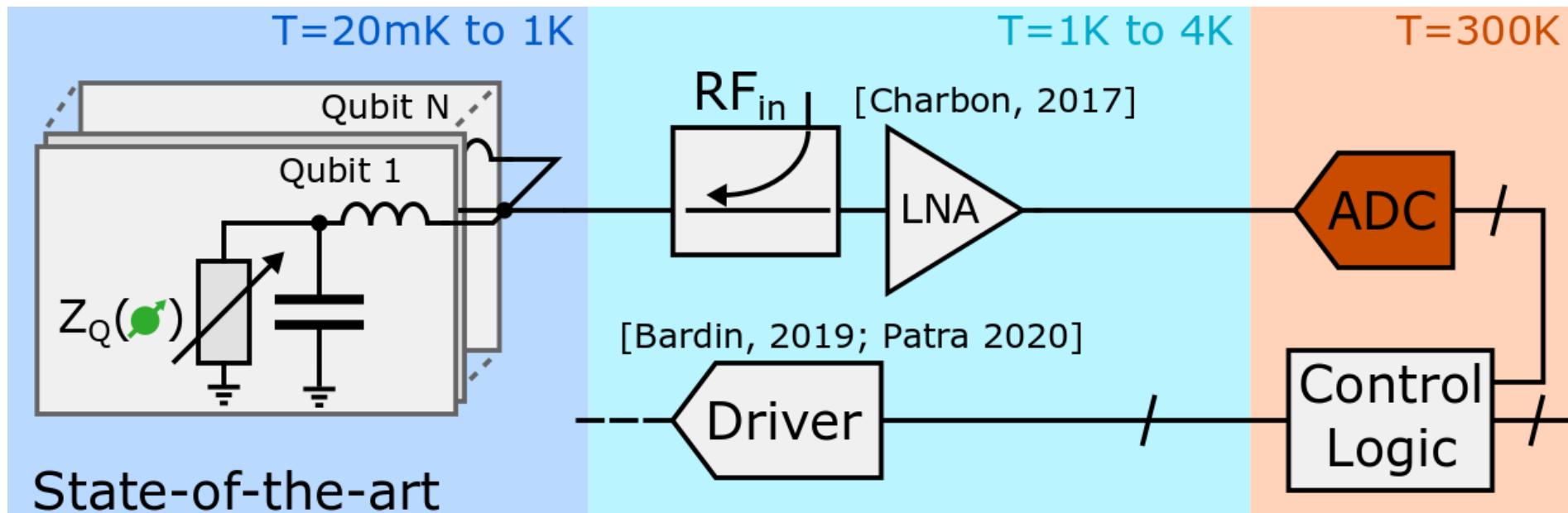
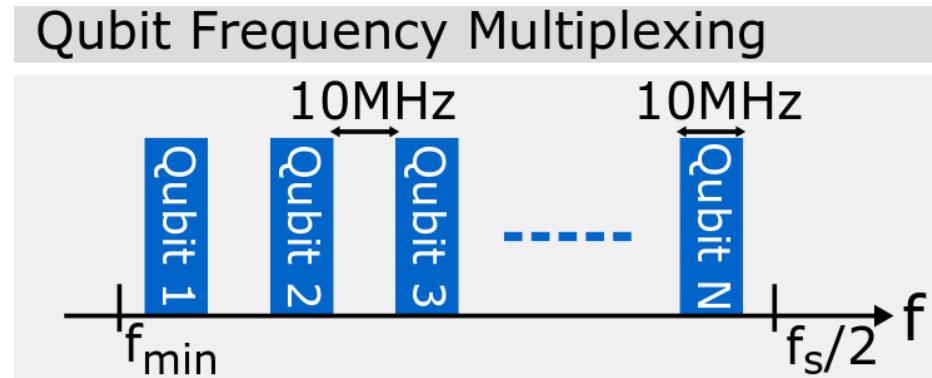
Generic RF readout chain

- Frequency multiplexing
 - More power efficient per qubit
 - Saves coaxial connections in present setups



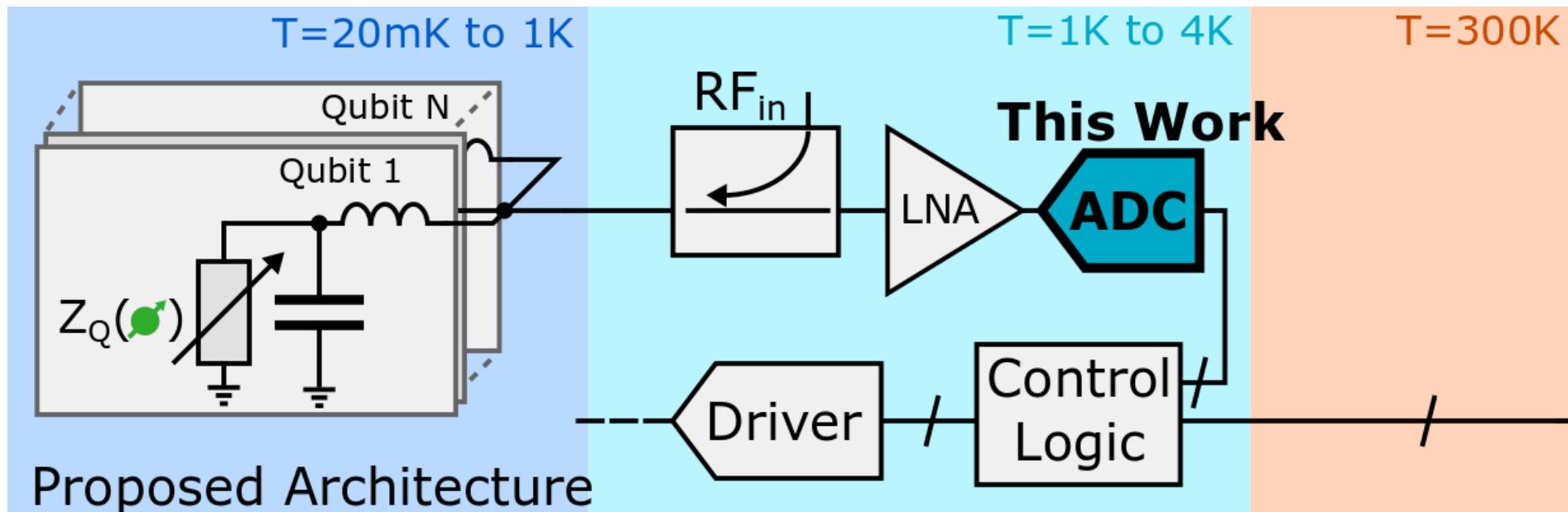
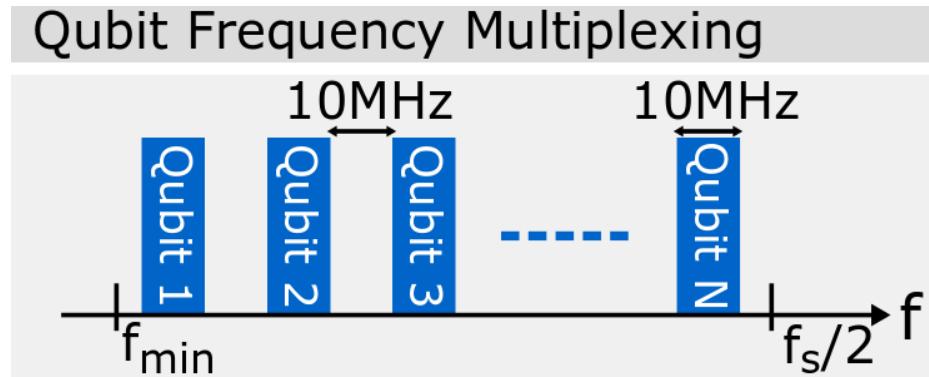
Generic RF readout chain

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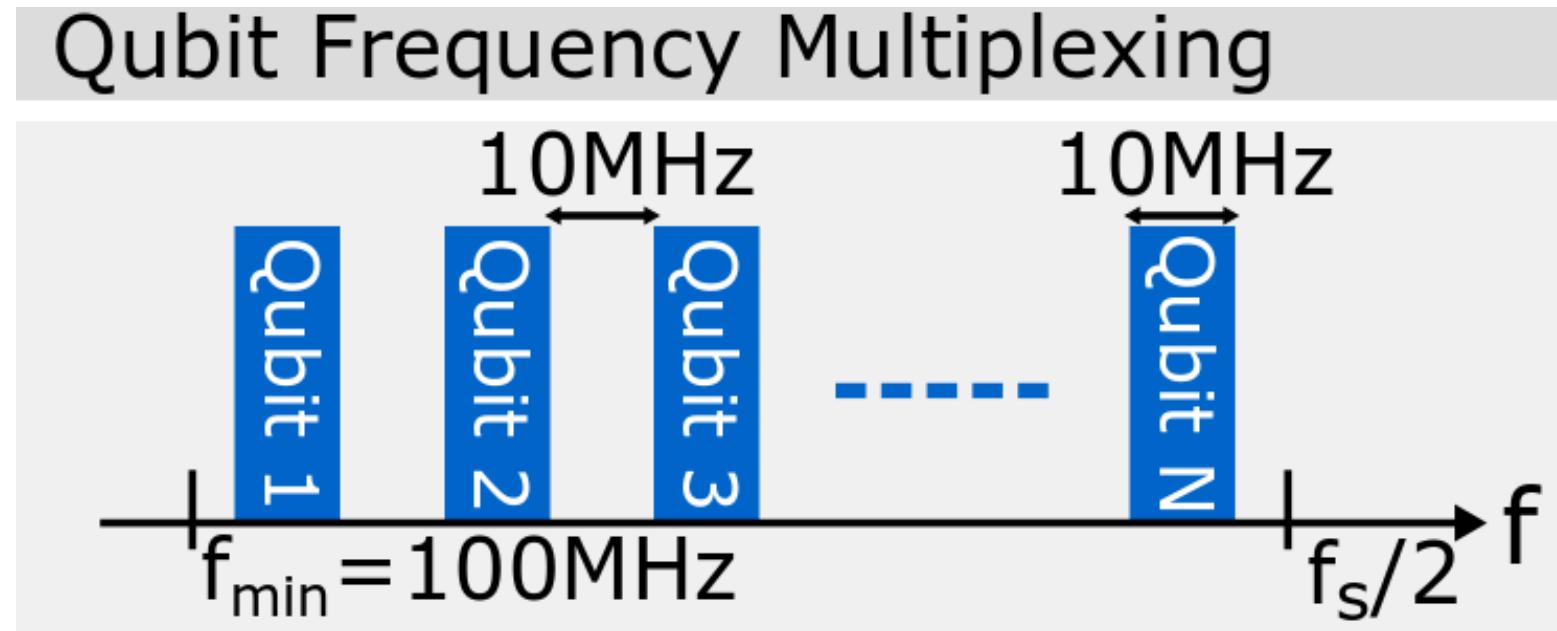


Generic RF readout chain

- Here:
 - Integrate wideband ADC to enable closing the control loop



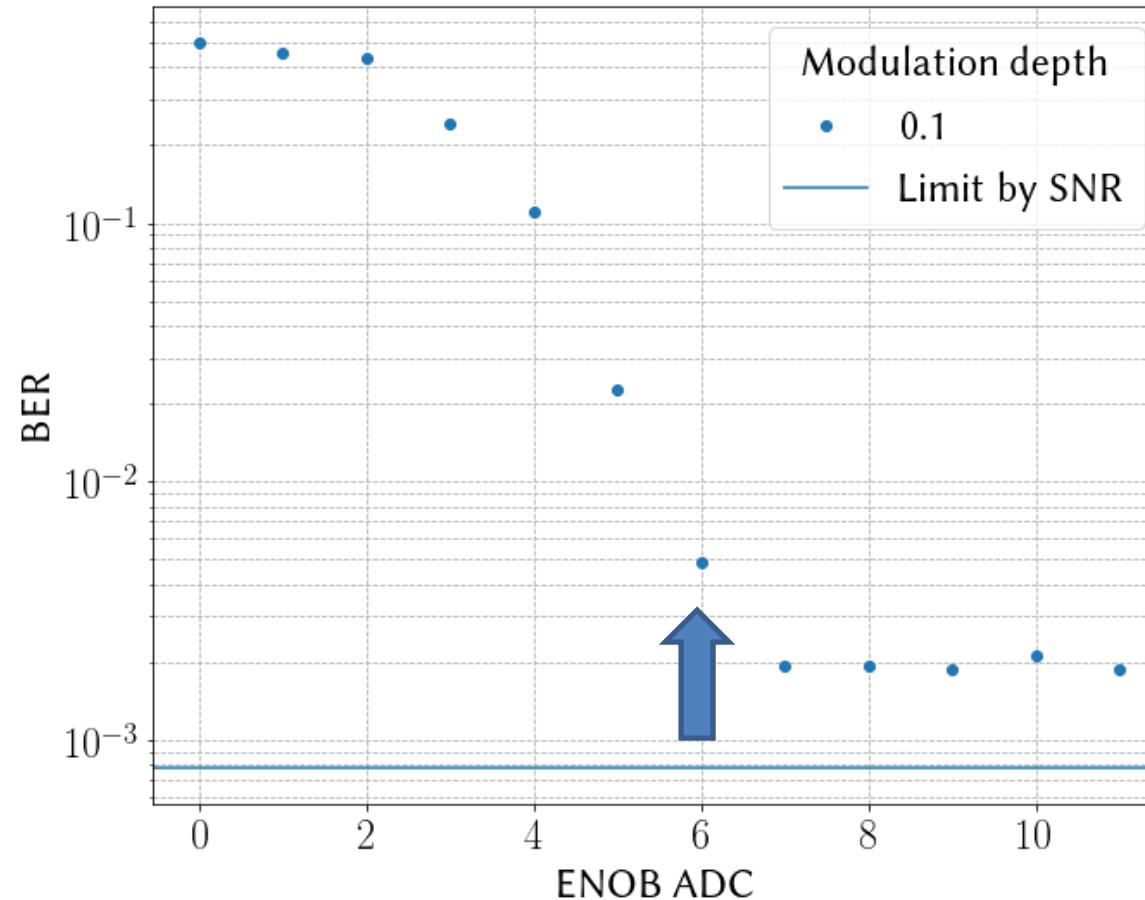
Cryo ADC specifications: BW



- 20 qubit channels require 1GS/s ADC

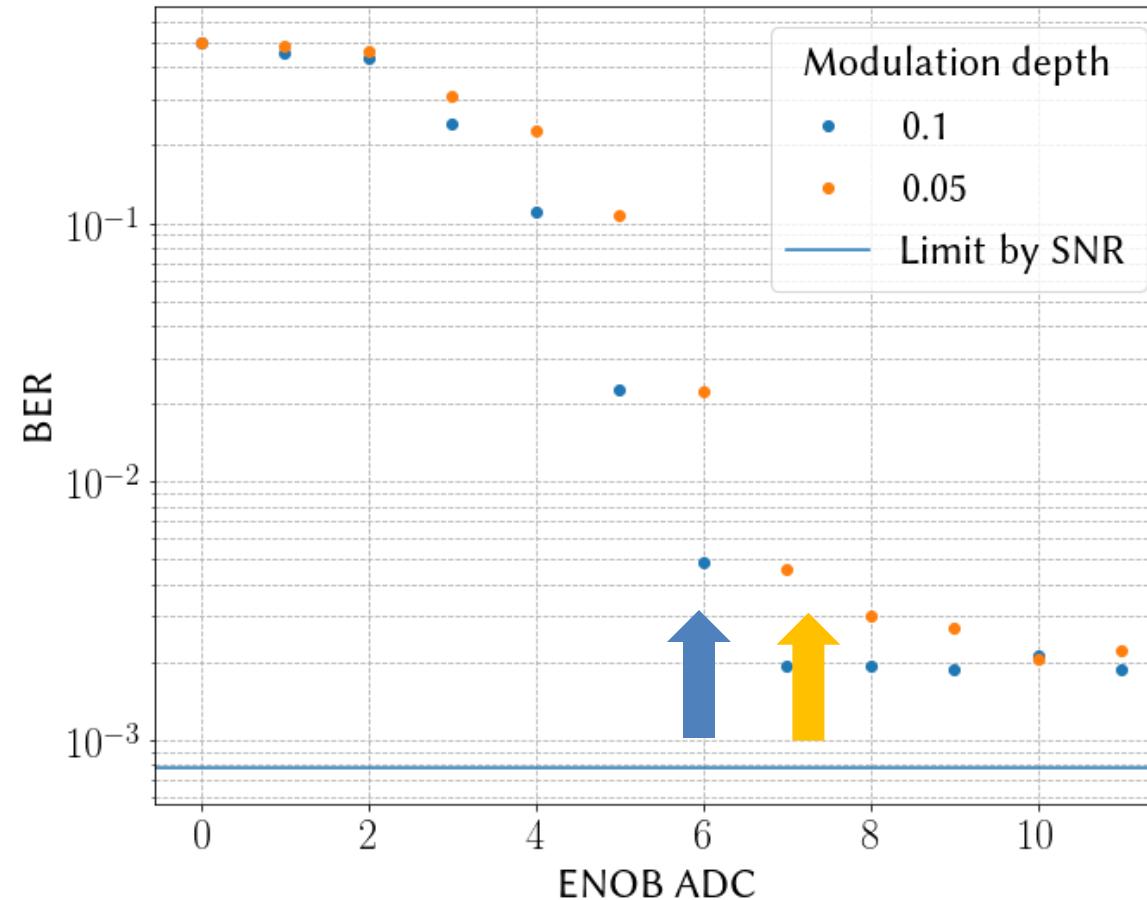
Cryo ADC specifications: resolution

- BER rate function of:
 - Source SNR (10dB)
 - Number of channels
 - Modulation depth
 - ADC resolution



Cryo ADC specifications: resolution

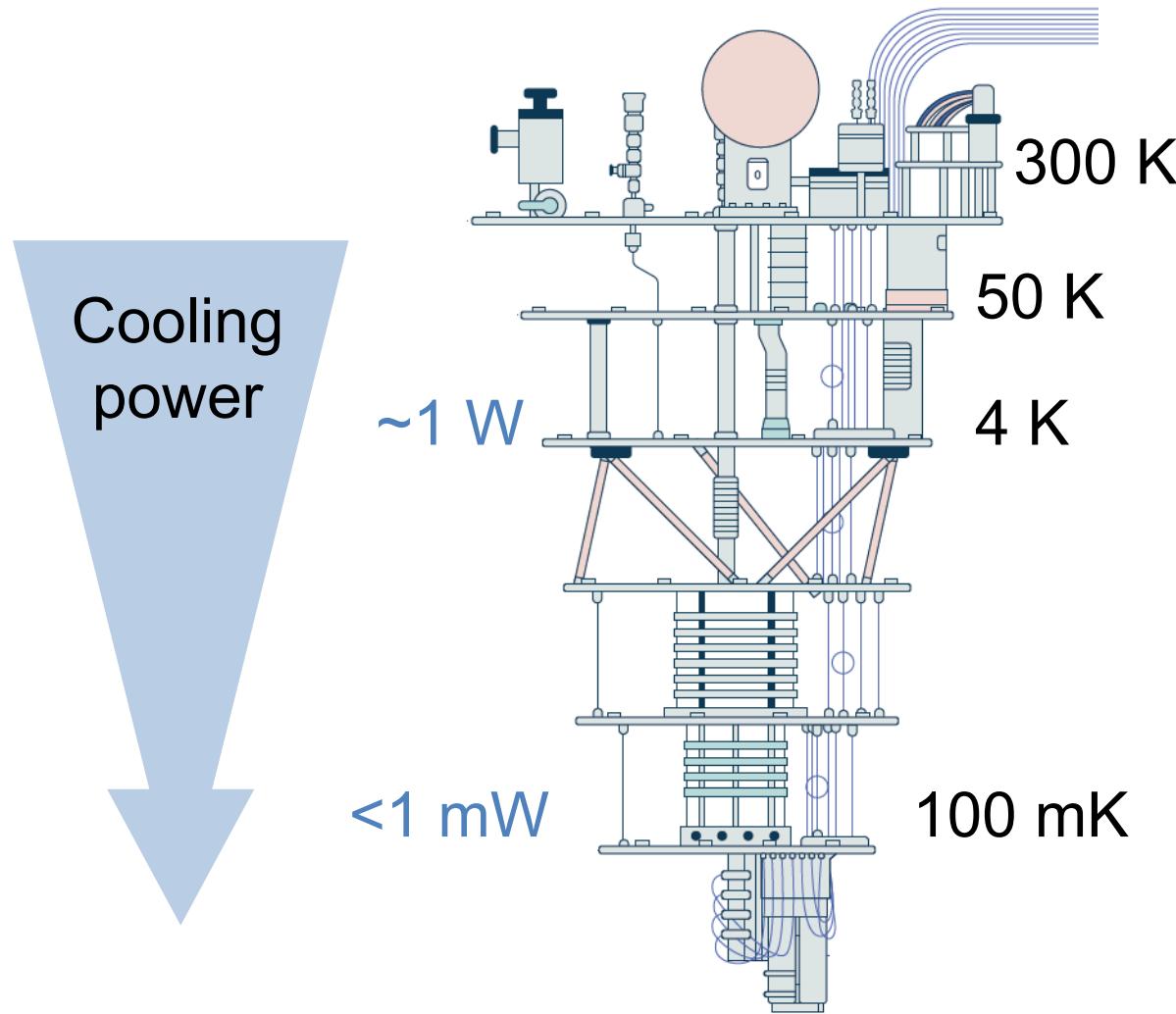
- BER rate function of:
 - Source SNR (10dB)
 - Number of channels
 - Modulation depth
 - ADC resolution
- Flexible 6-7b ENOB necessary



Closing the control loop at cryo

Challenges

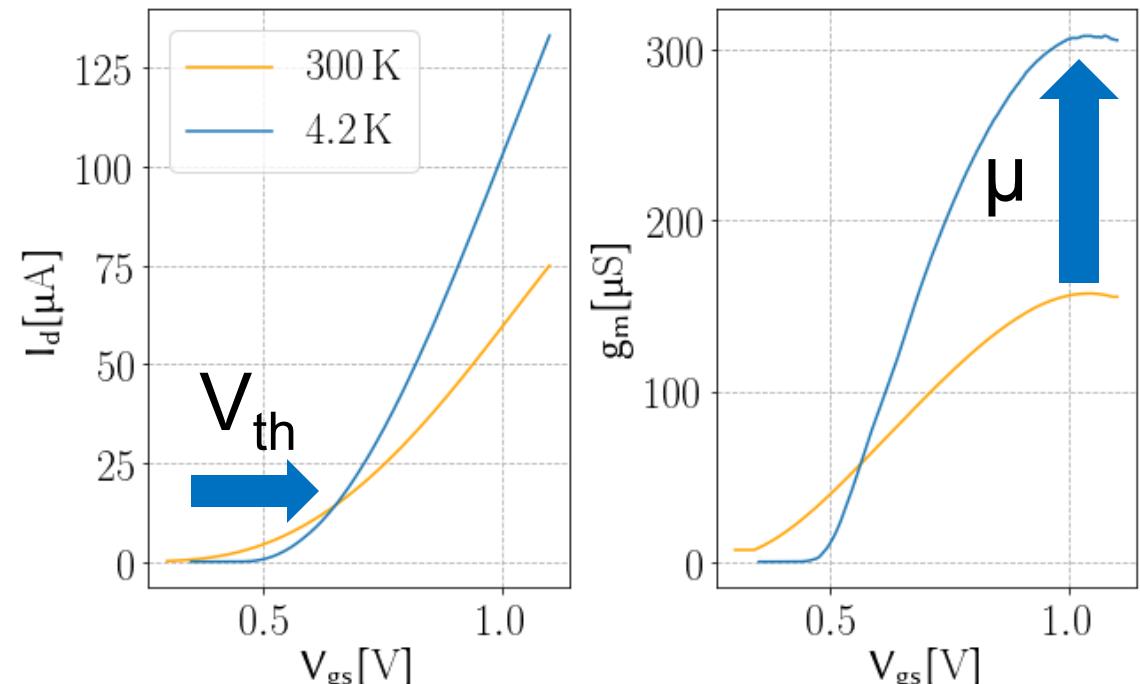
- **Limited cooling power**
 - System power needs to be minimized, $<1\text{mW/qubit}$



Closing the control loop at cryo

Challenges

- Limited cooling power
 - System power needs to be minimized , <1mW/qubit
- **Immature models**
 - No foundry cryogenic models
 - Measured characterization data available



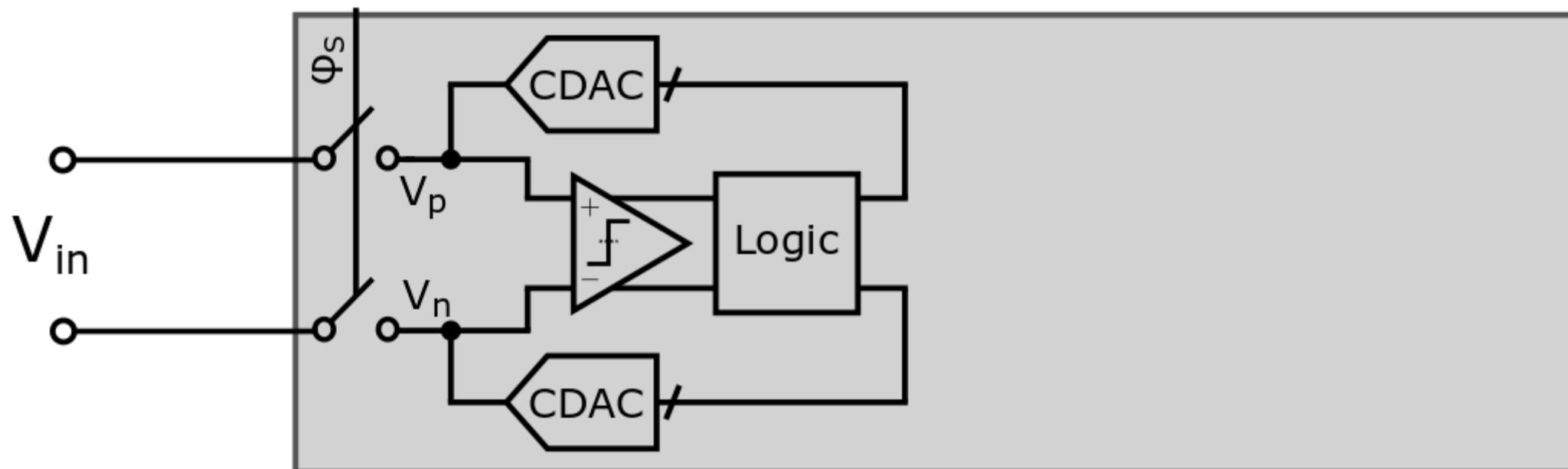
Measured 40nm device data

Outline

- Introduction
- Application
- Circuit implementation
- Experimental characterization
- Conclusion

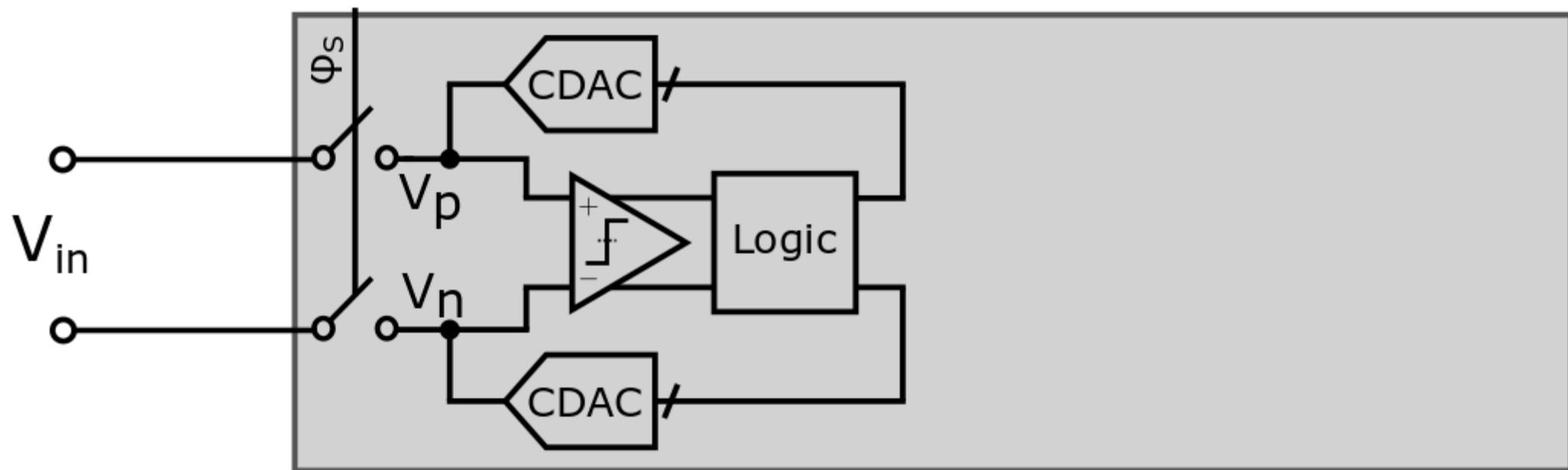
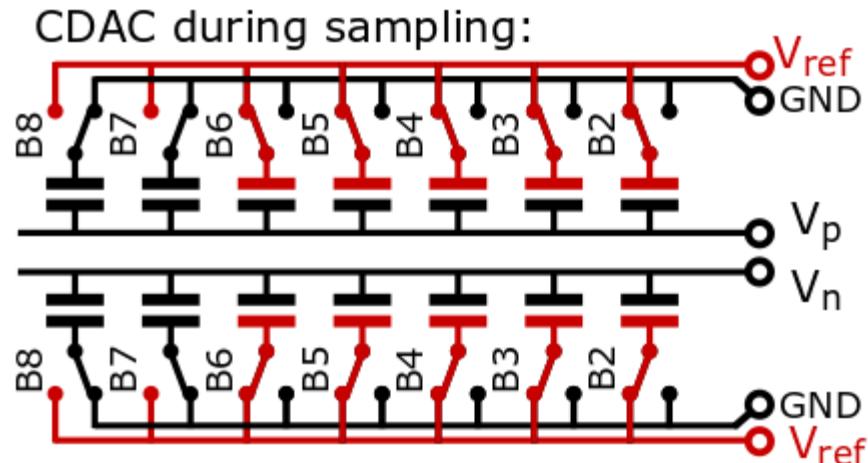
ADC architecture: SAR

- Power efficient
- Mostly digital operation

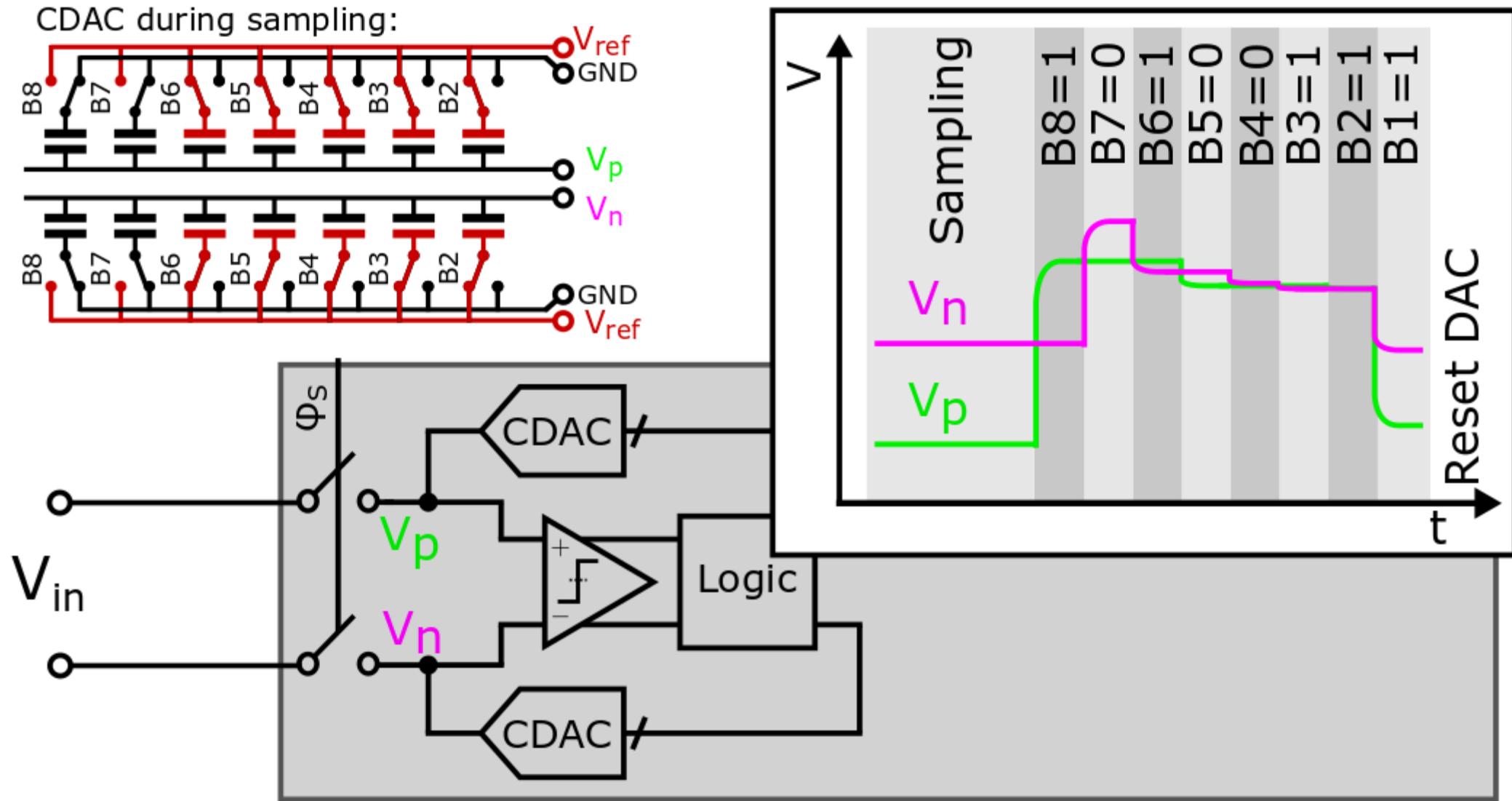


13.4: A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS

ADC architecture: DAC

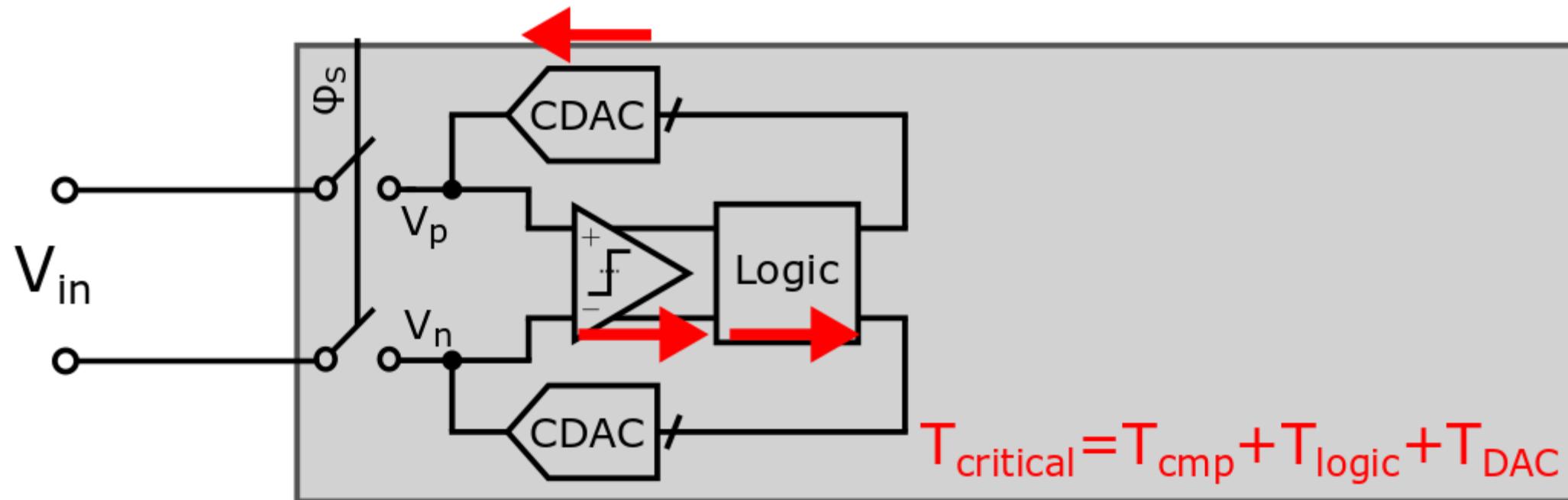


ADC architecture: DAC



ADC architecture: loop-unrolled

- Speed of SAR limited by critical loop!

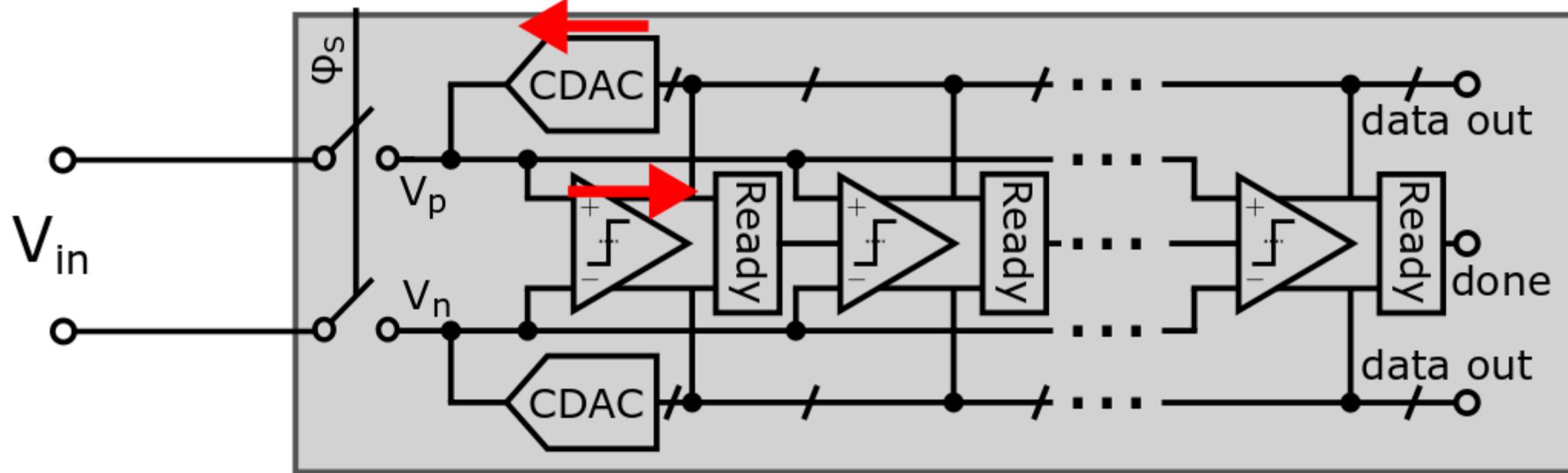


ADC architecture: loop-unrolled

- Unrolled loop speeds up conversion
- Inherently asynchronous
- Problem: Comparator offsets cause distortion

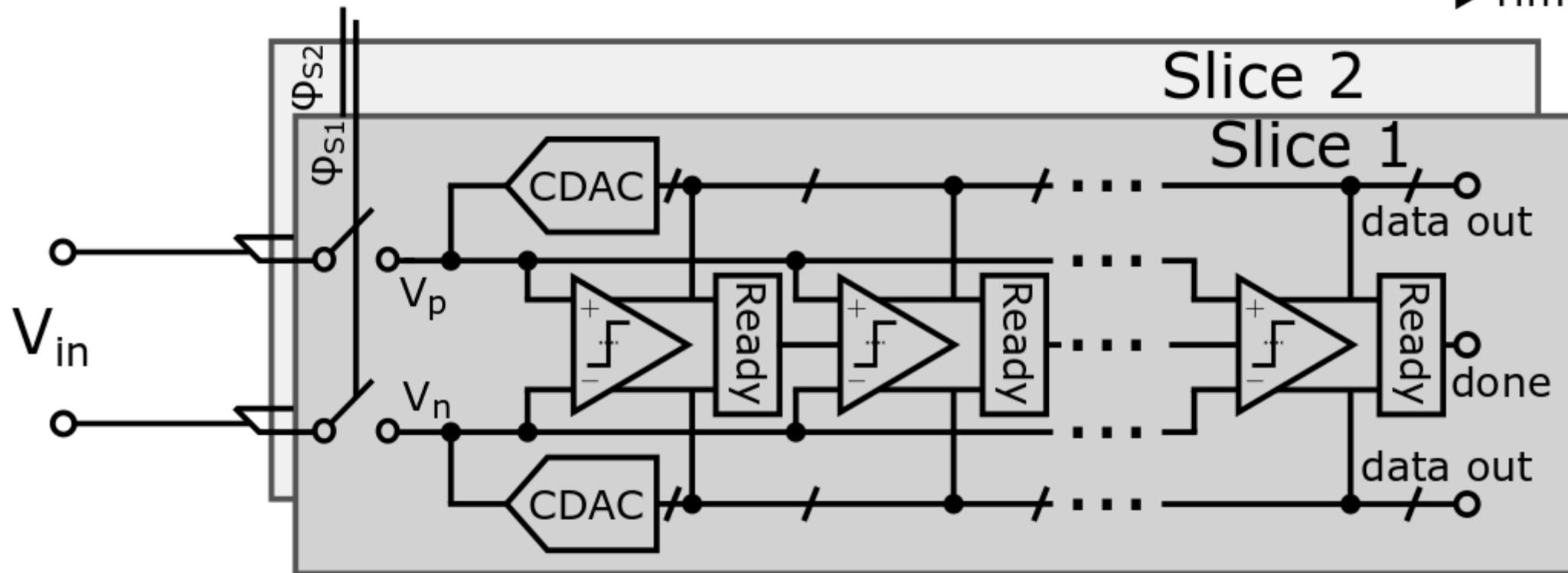
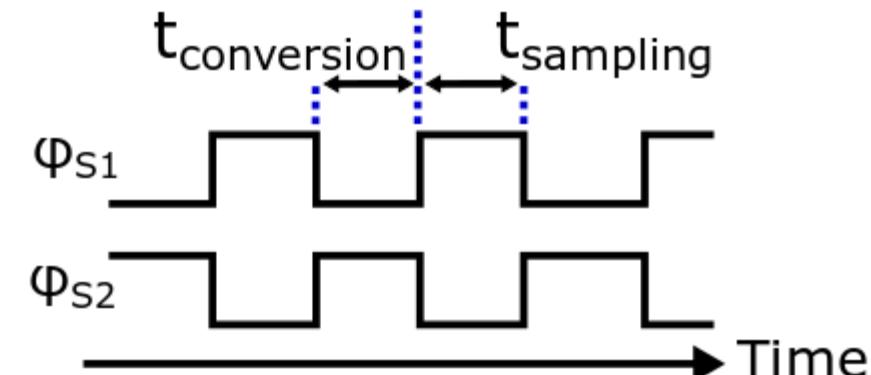
$$T_{\text{critical}} = T_{\text{cmp}} + T_{\text{DAC}}$$

[Jiang, 2012]

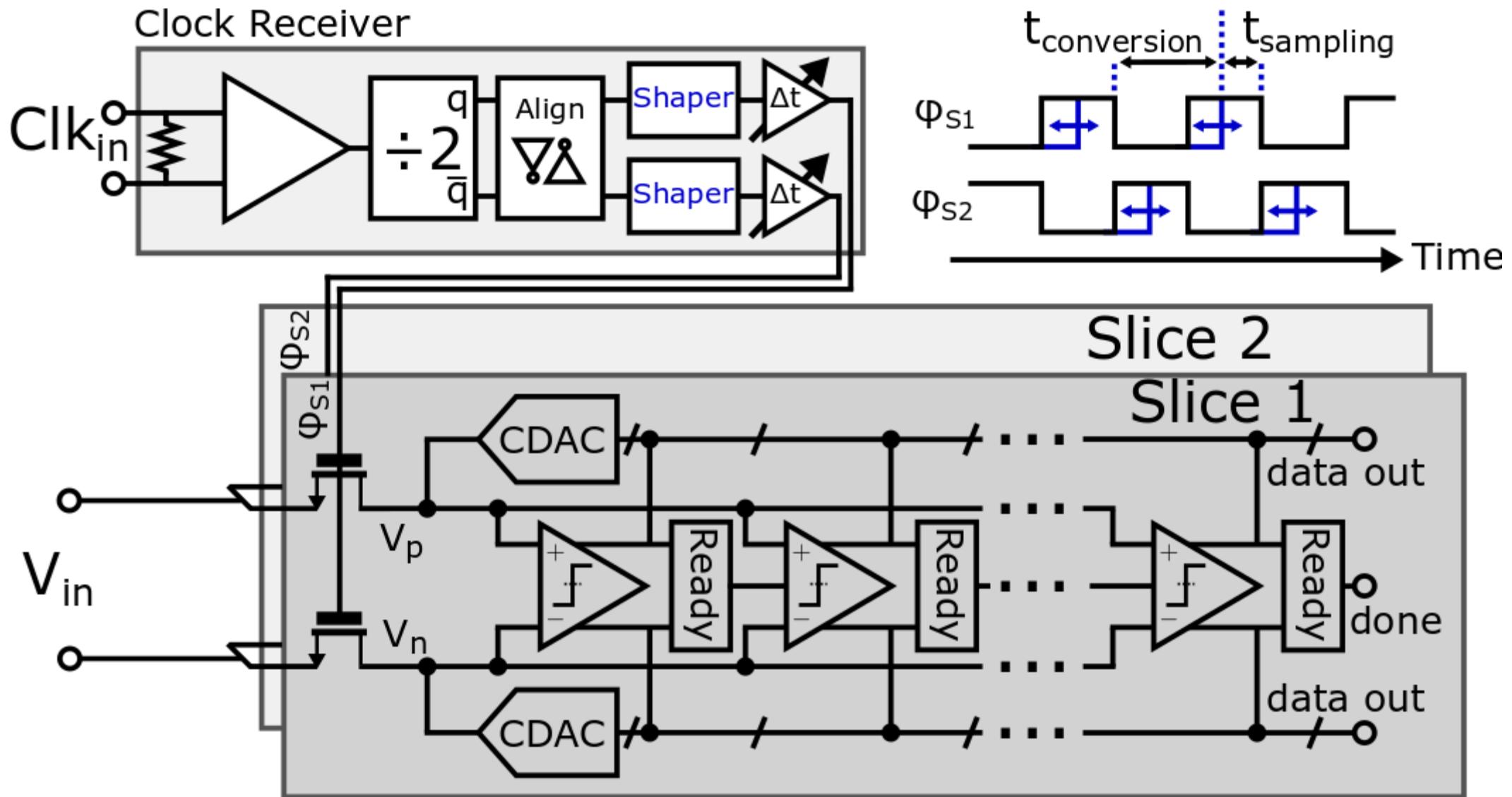


ADC architecture: time interleaved

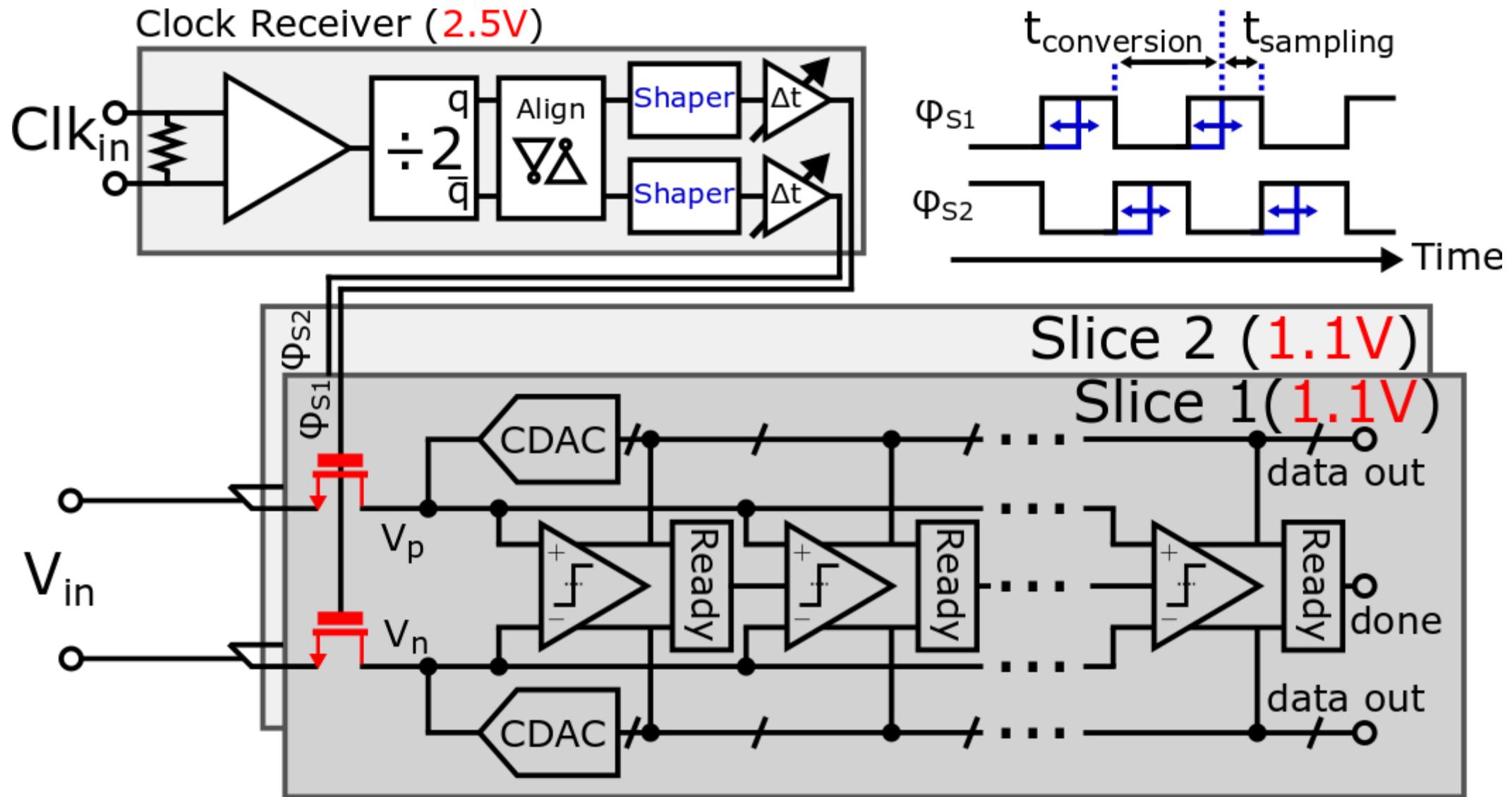
- Speedup by factor of two
- Switch more linear than necessary



ADC architecture: frontend



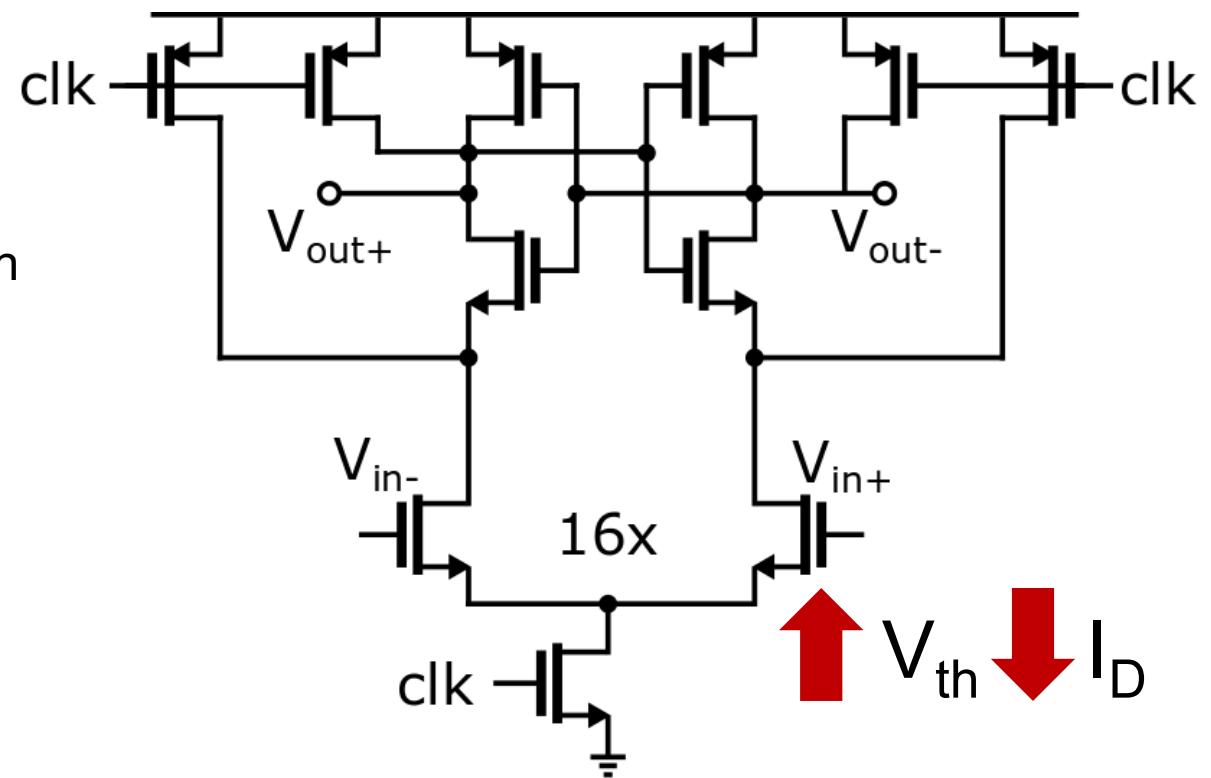
ADC architecture: frontend



Comparator design

Challenge: V_{th} increase

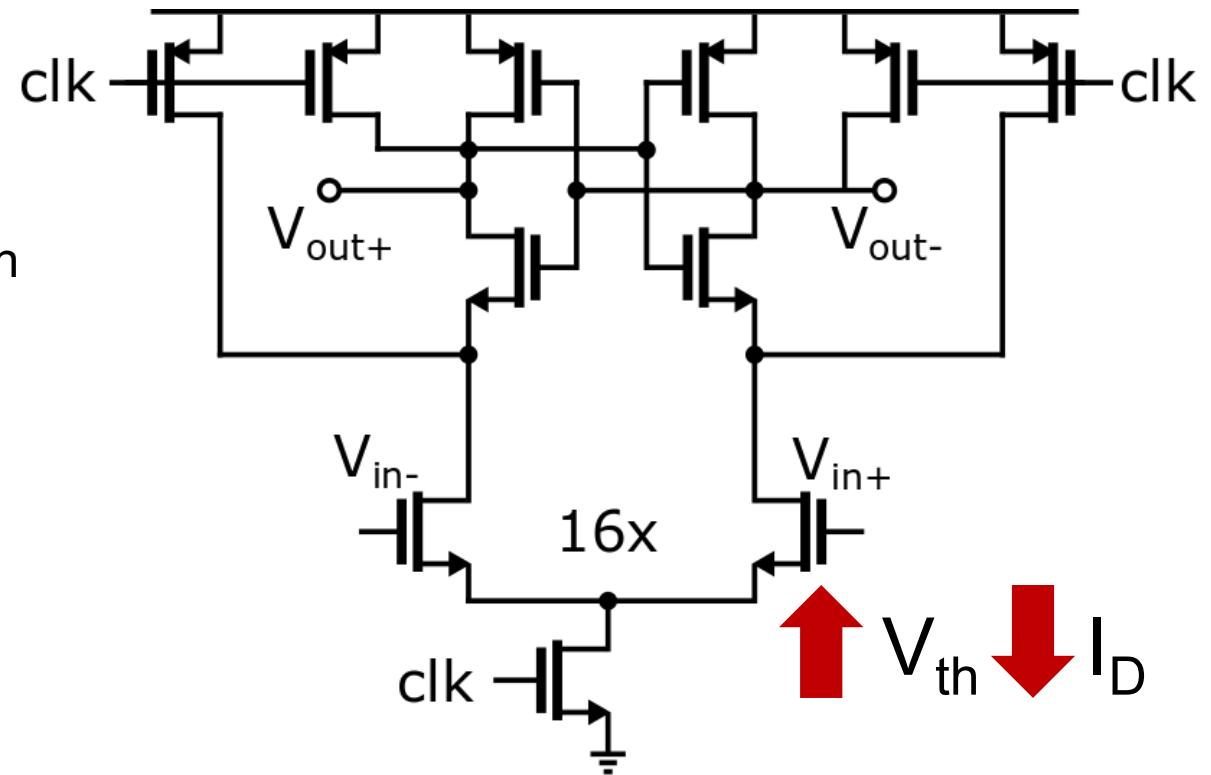
- Strong-ARM comparator
 - Energy efficient
 - Fast
- Speed degrades at higher V_{th}



Comparator design

Challenge: V_{th} increase

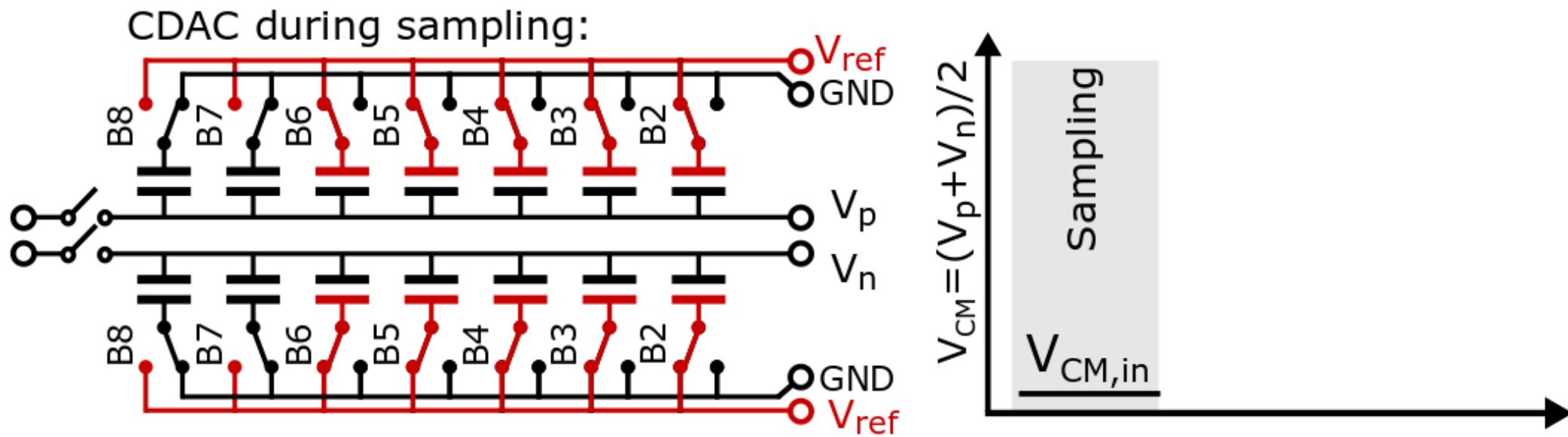
- Strong-ARM comparator
 - Energy efficient
 - Fast
- Speed degrades at higher V_{th}
- Possible solution: raise CM
- Issue: limiting input swing



Common mode switching scheme

Solution: adapted V_{CM}

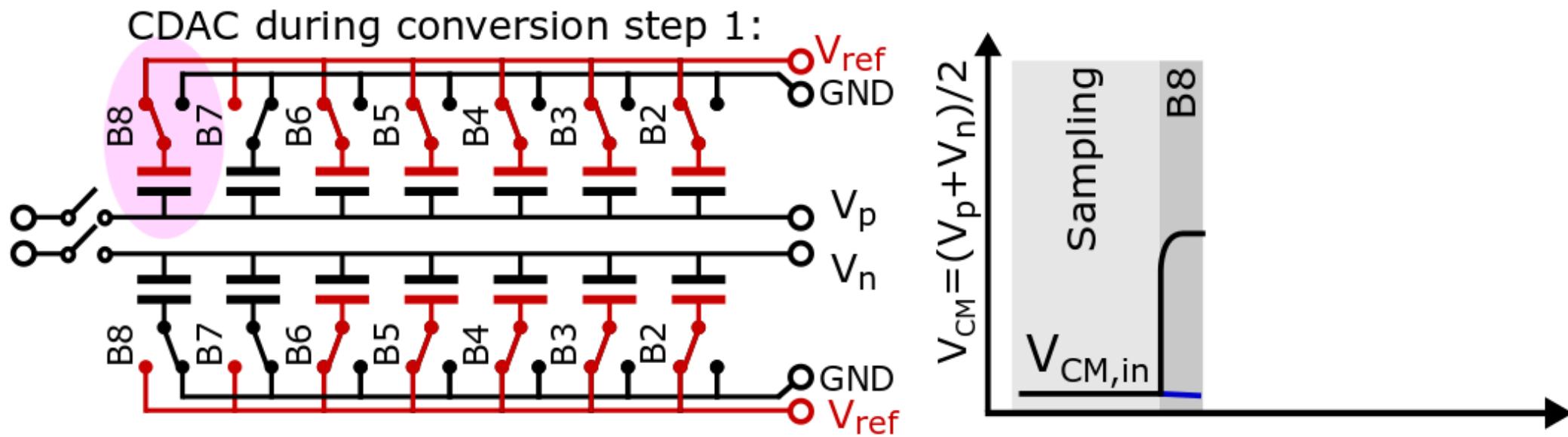
- Input: mid-rail common mode for large-swing core-VDD driver



Common mode switching scheme

Solution: adapted V_{CM}

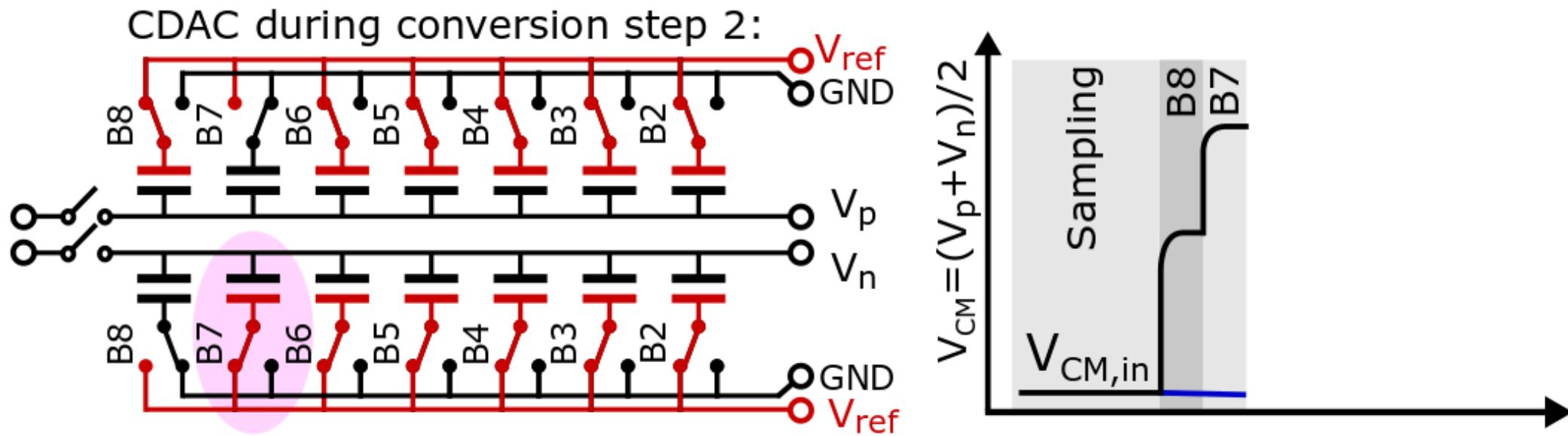
- Input: mid-rail common mode for large-swing core-VDD driver
- First two bits: V_{CM} up



Common mode switching scheme

Solution: adapted V_{CM}

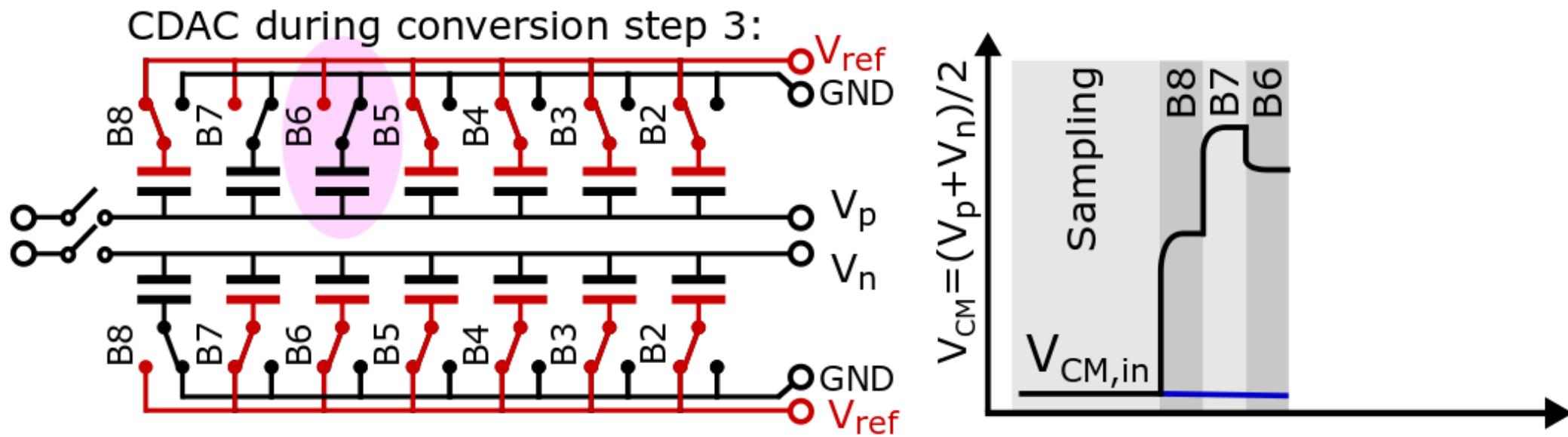
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Common mode switching scheme

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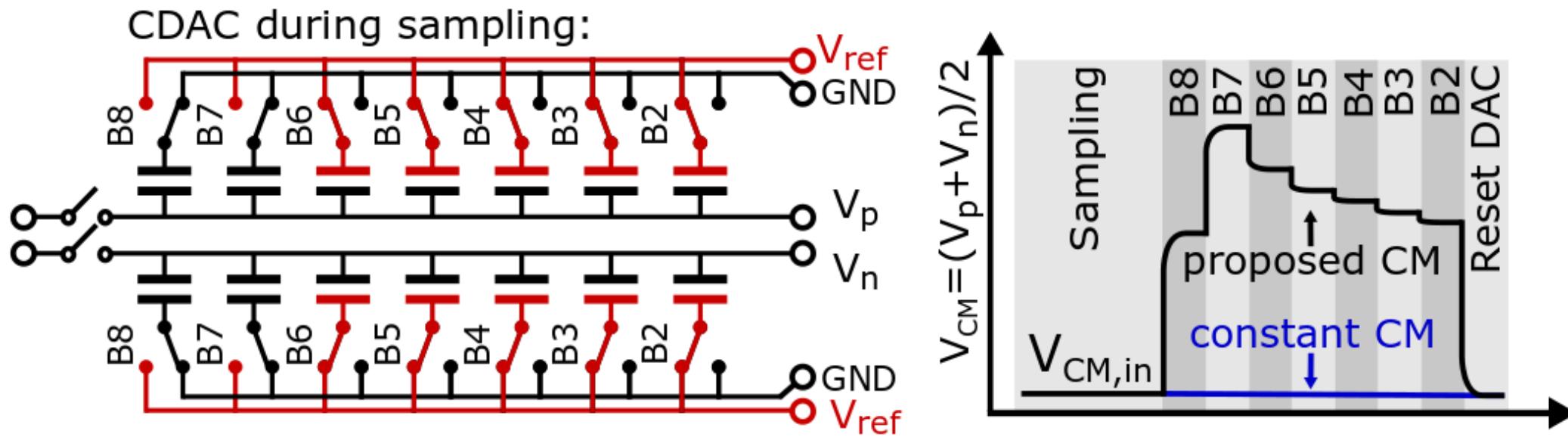
- Input: mid-rail common mode for large-swing core-VDD driver
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- Rest of bits: V_{CM} down



Common mode switching scheme

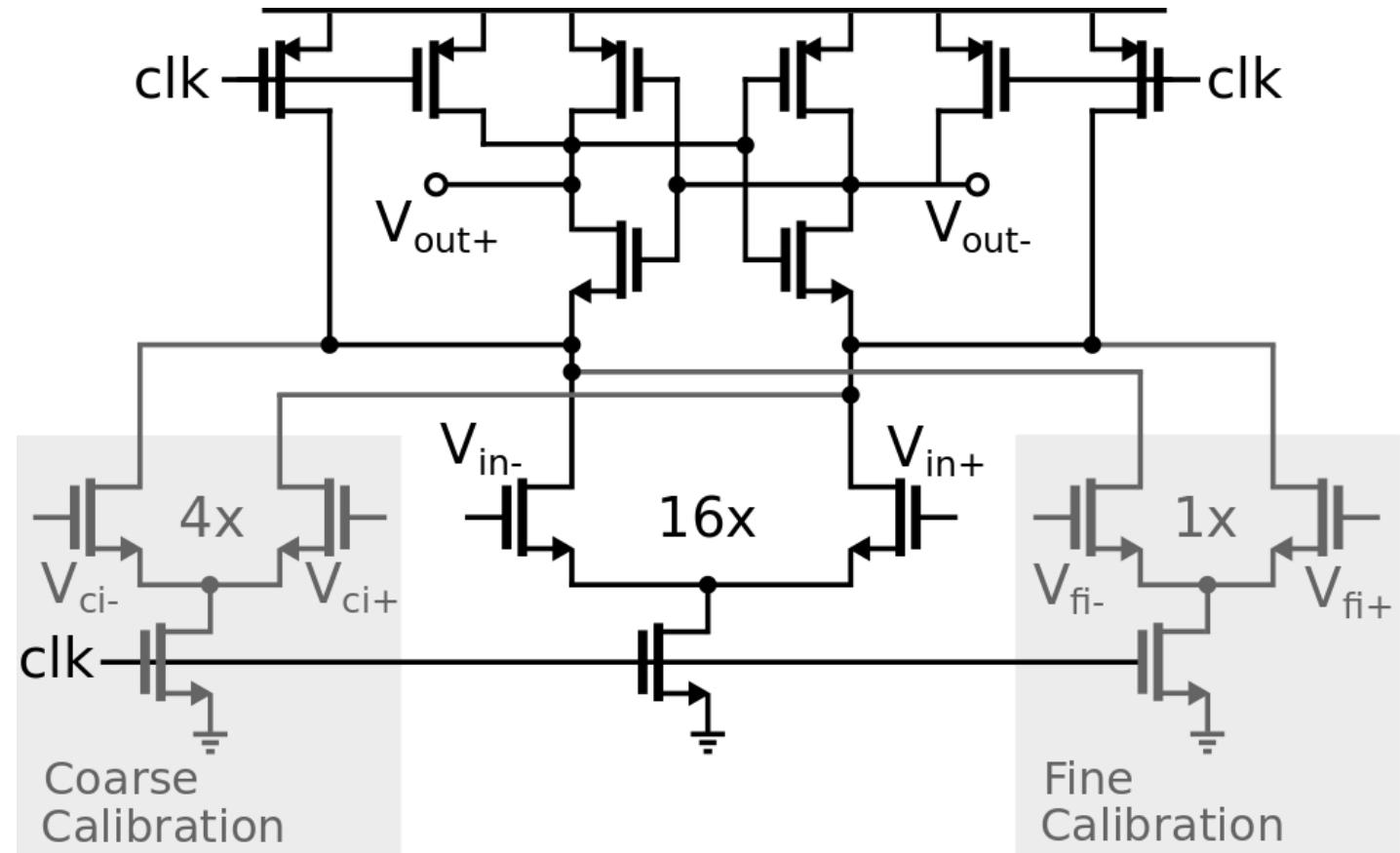
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Comparator design

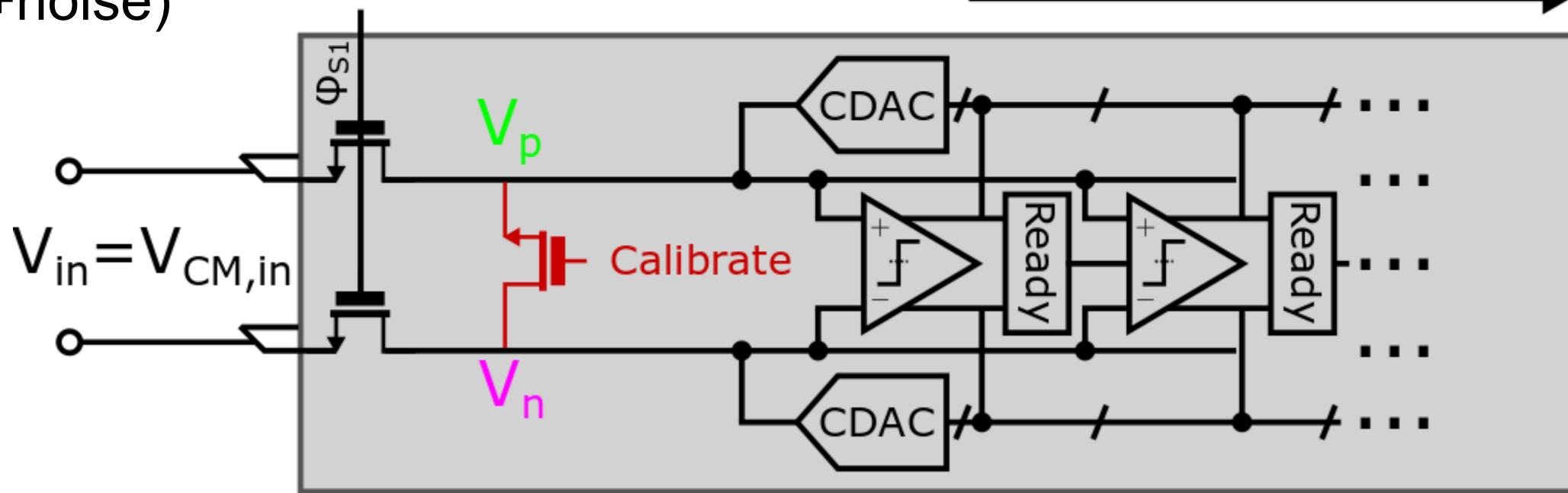
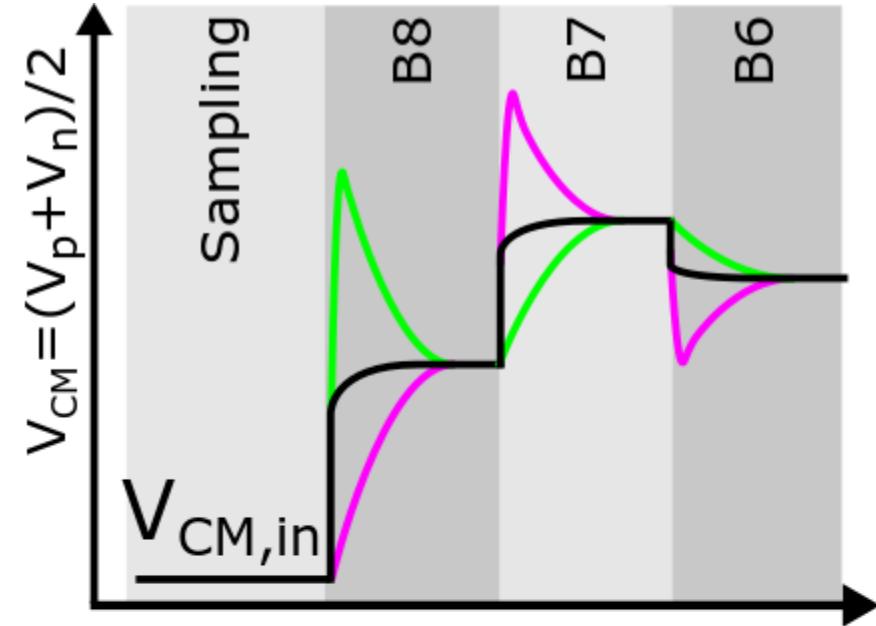
- Employing additional pairs for calibration
 - Adds noise
 - Speeds up conversion
 - Coarse/fine pairs relax specification of calibration DAC
- Calibrate comparator at correct V_{CM}



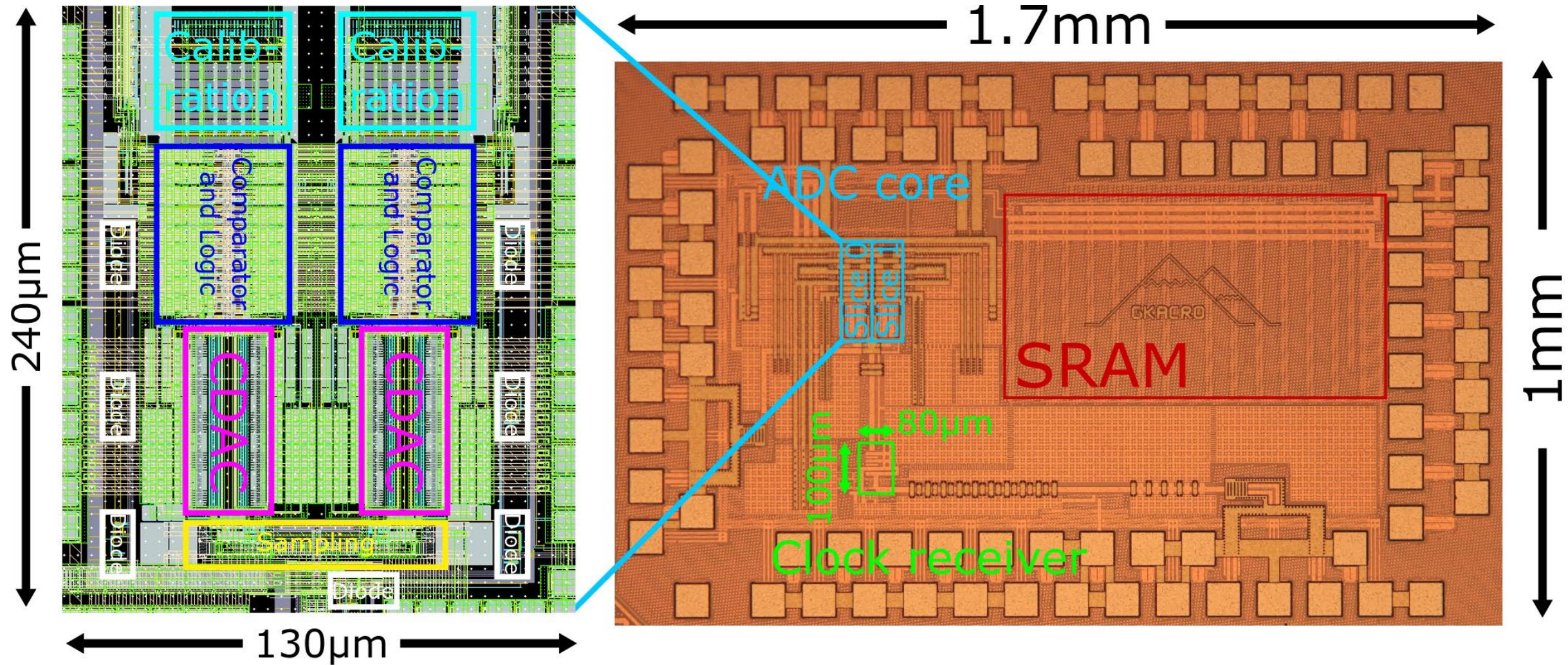
Foreground calibration

With variable common mode

- Short DACs with thick-oxide switch
- Run regular conversion
- Output determined by offset (+noise)



Implementation: 40nm LP process

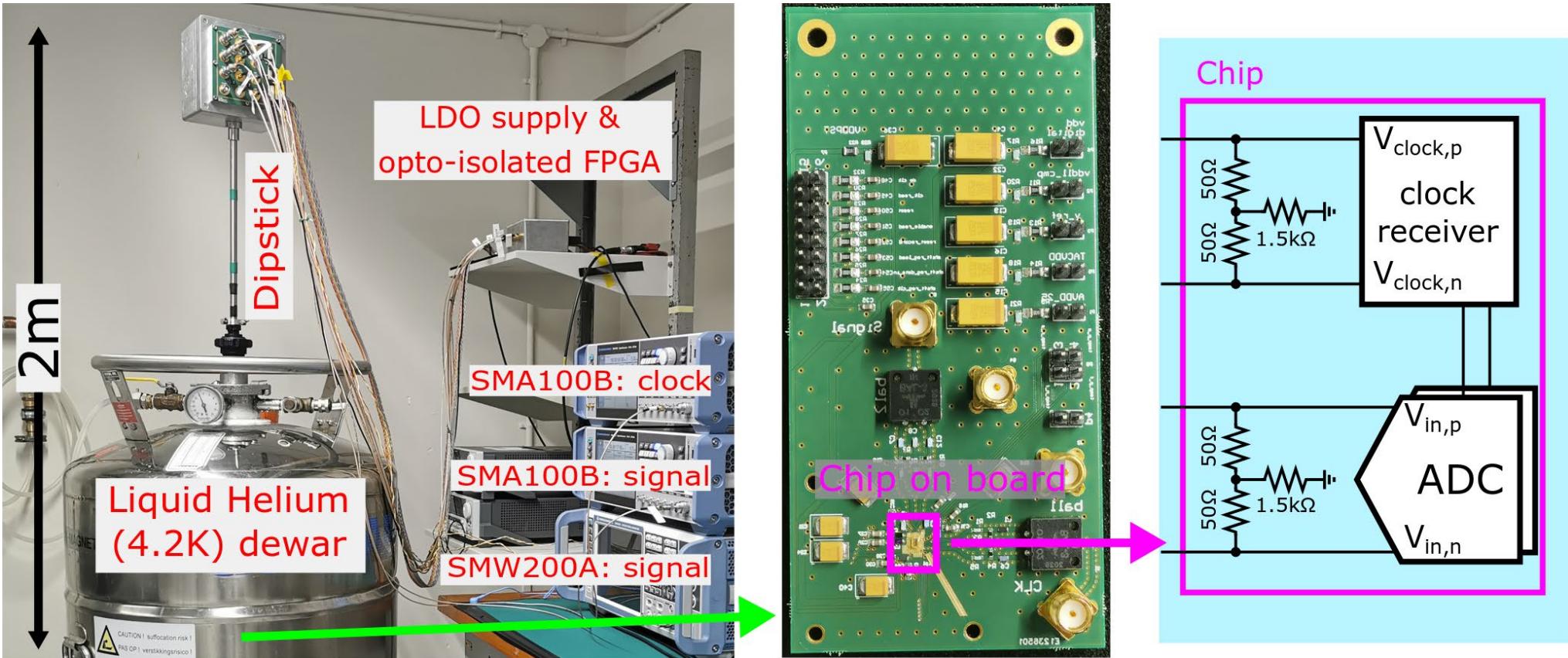


13.4: A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS

Outline

- Introduction
- Application
- Circuit implementation
- Experimental characterization
- Conclusion

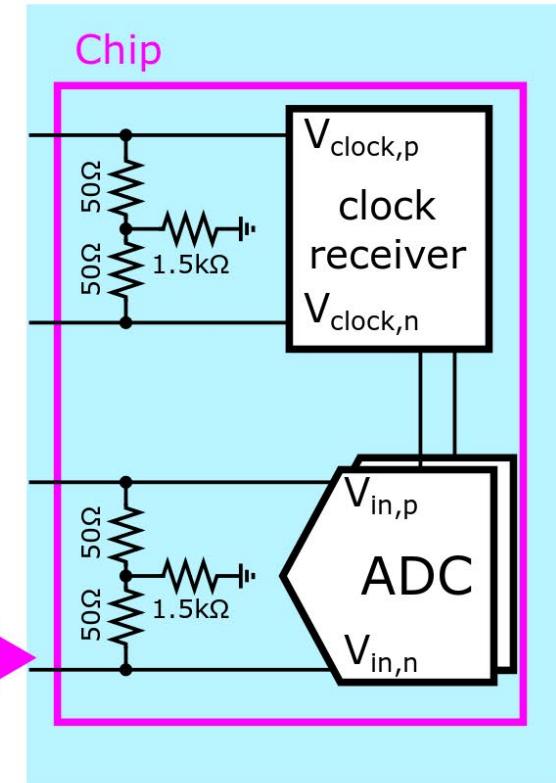
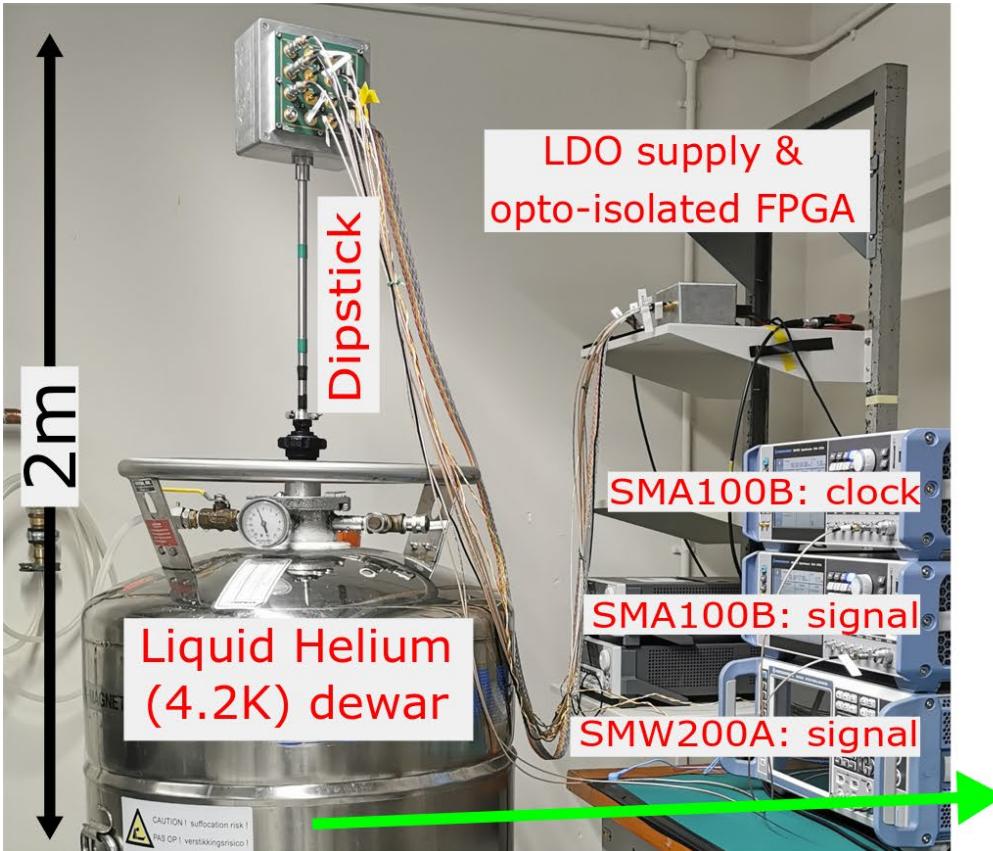
ADC measurements



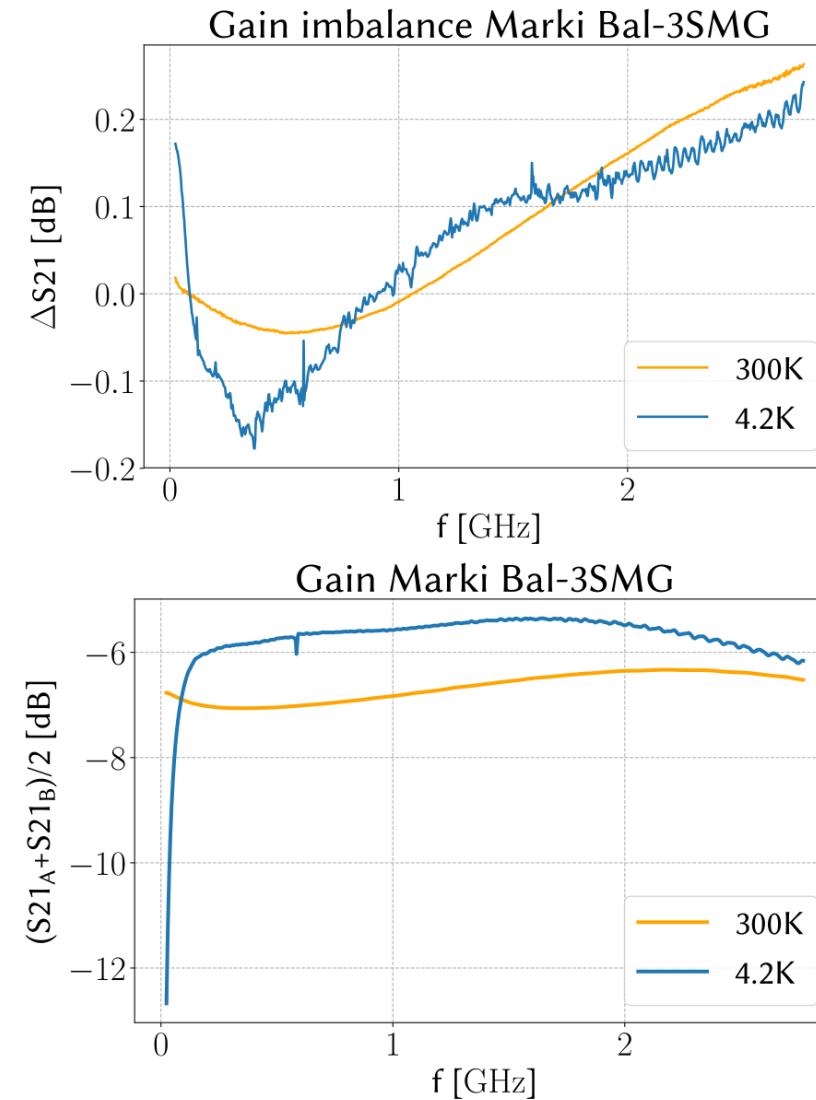
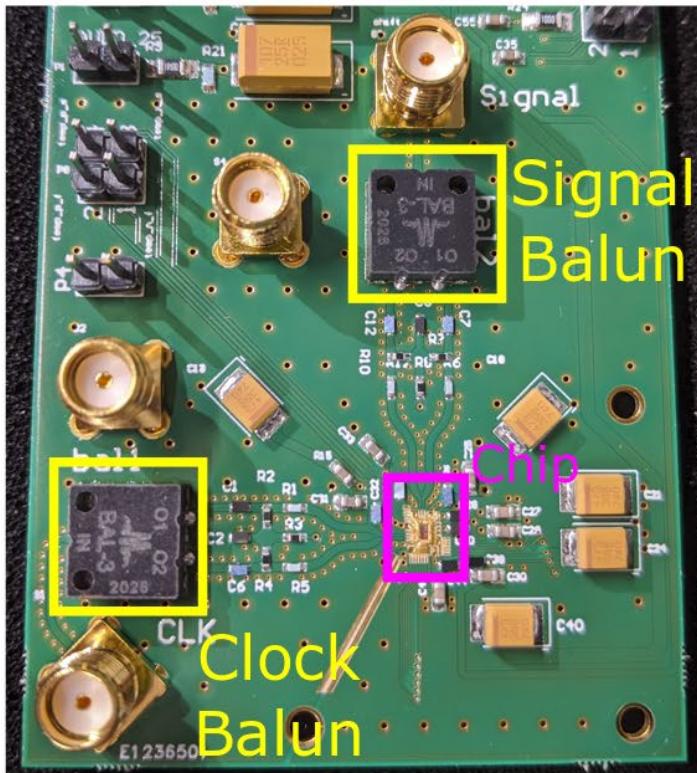
13.4: A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS

ADC measurements

- Challenge: high-fidelity differential signal needed

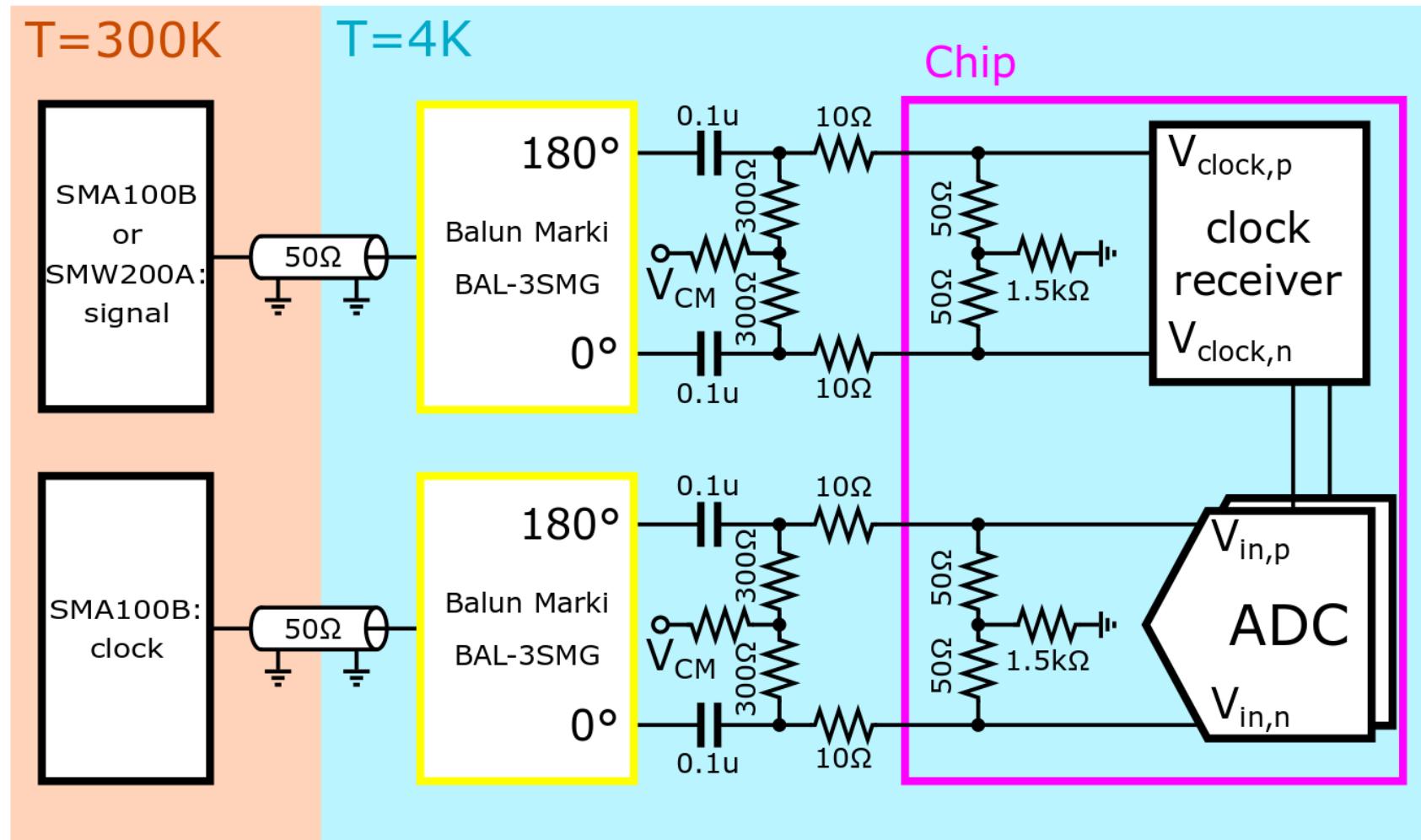
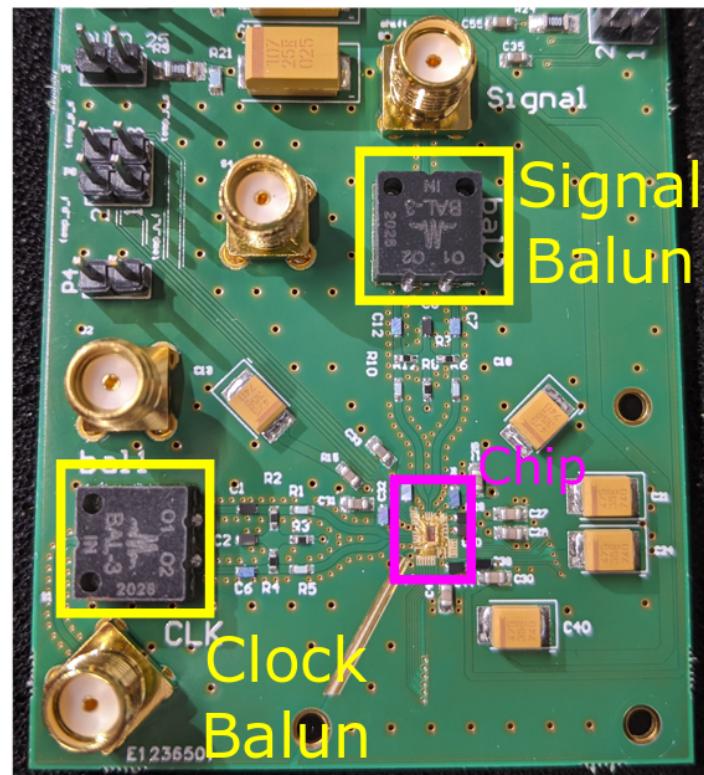


Detailed measurement setup



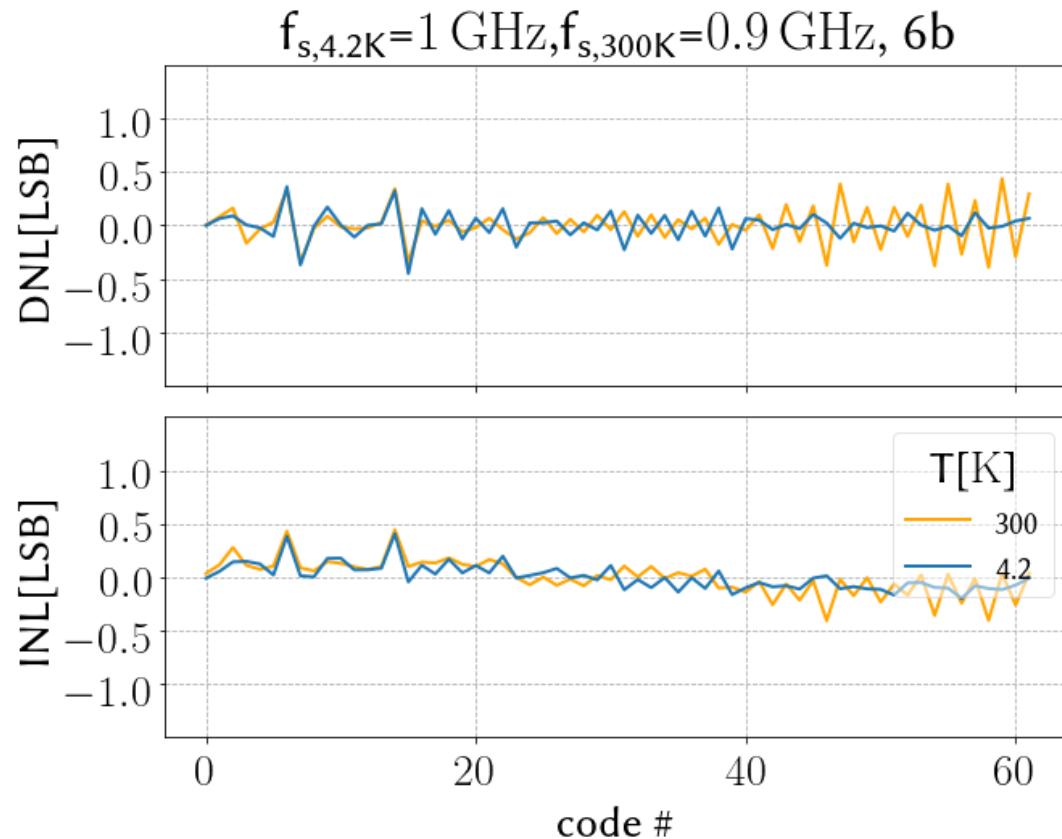
13.4: A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS

Detailed measurement setup



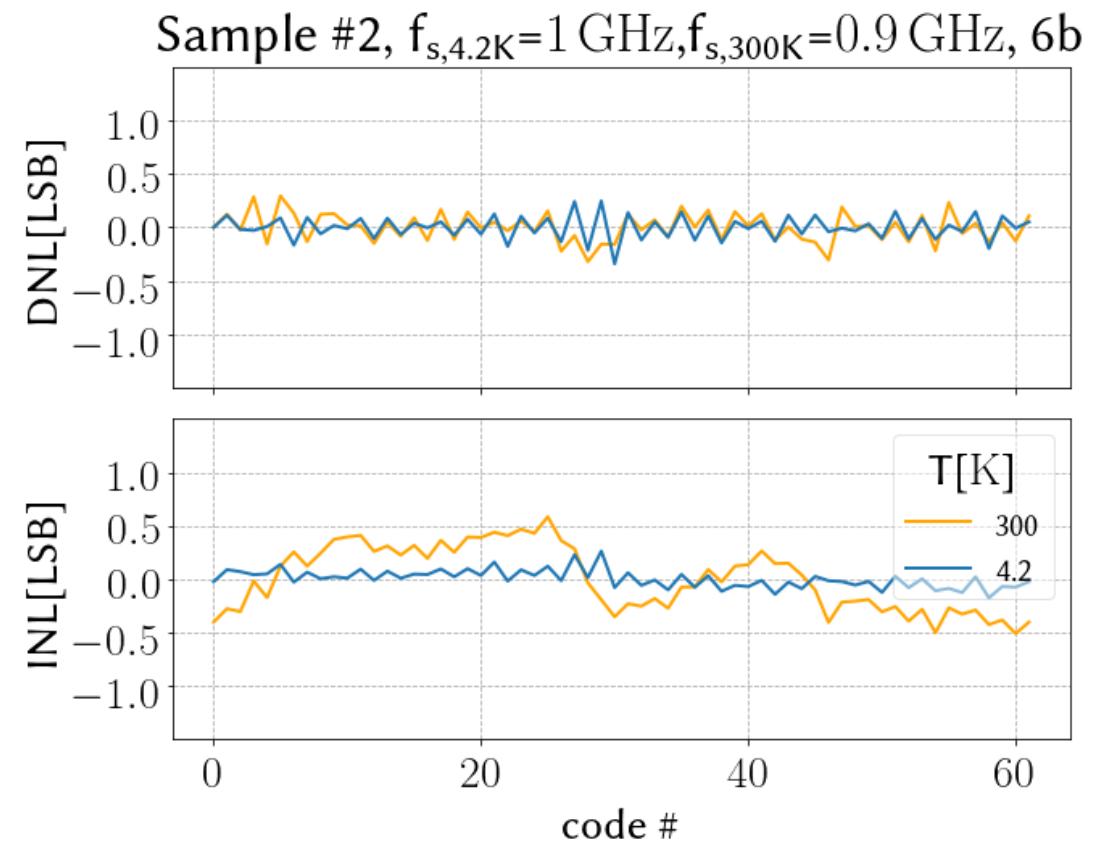
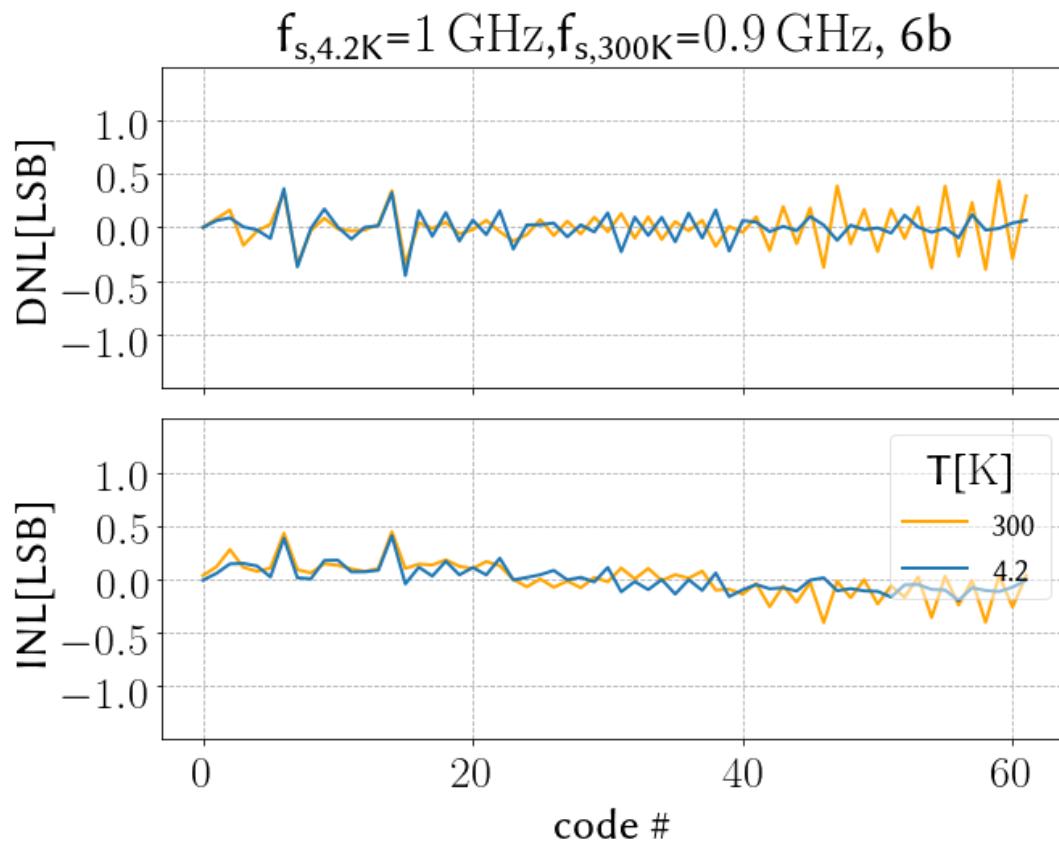
INL/DNL: 6b, 1GS/s

- Without foreground calibration > 10LSB DNL
- Stable calibration set per temperature



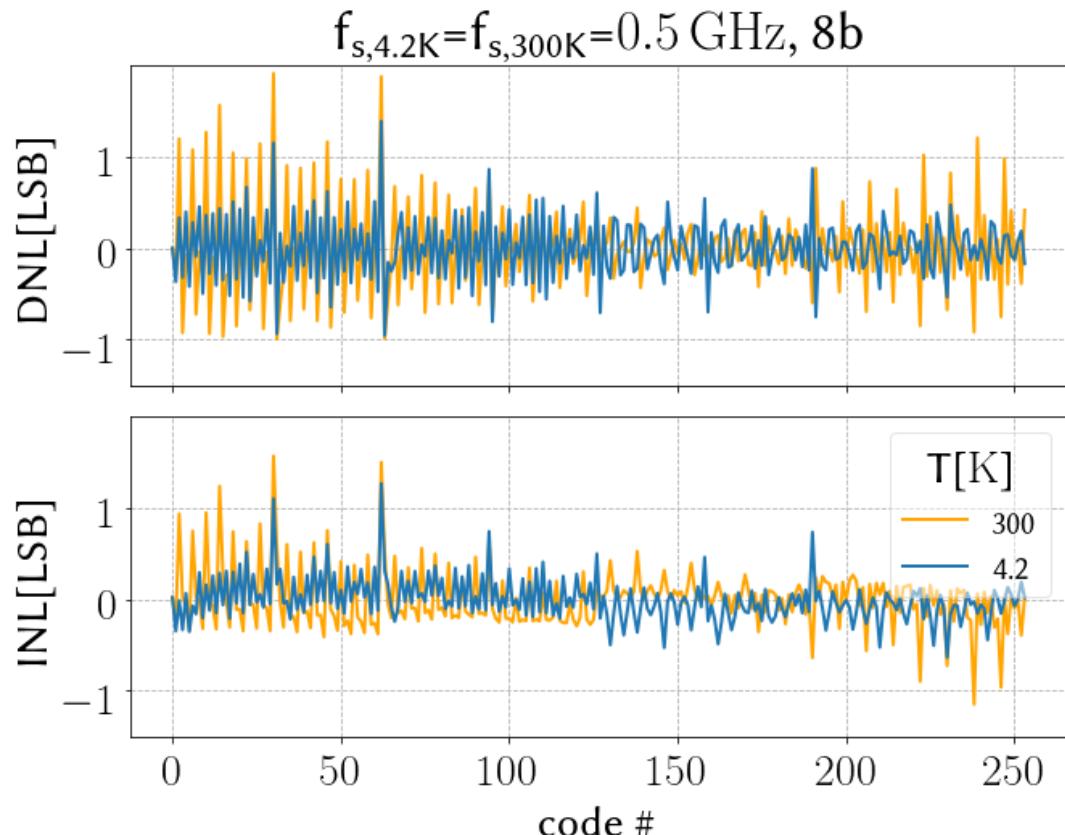
INL/DNL: 6b, 1GS/s

- Second tested sample shows similar performance



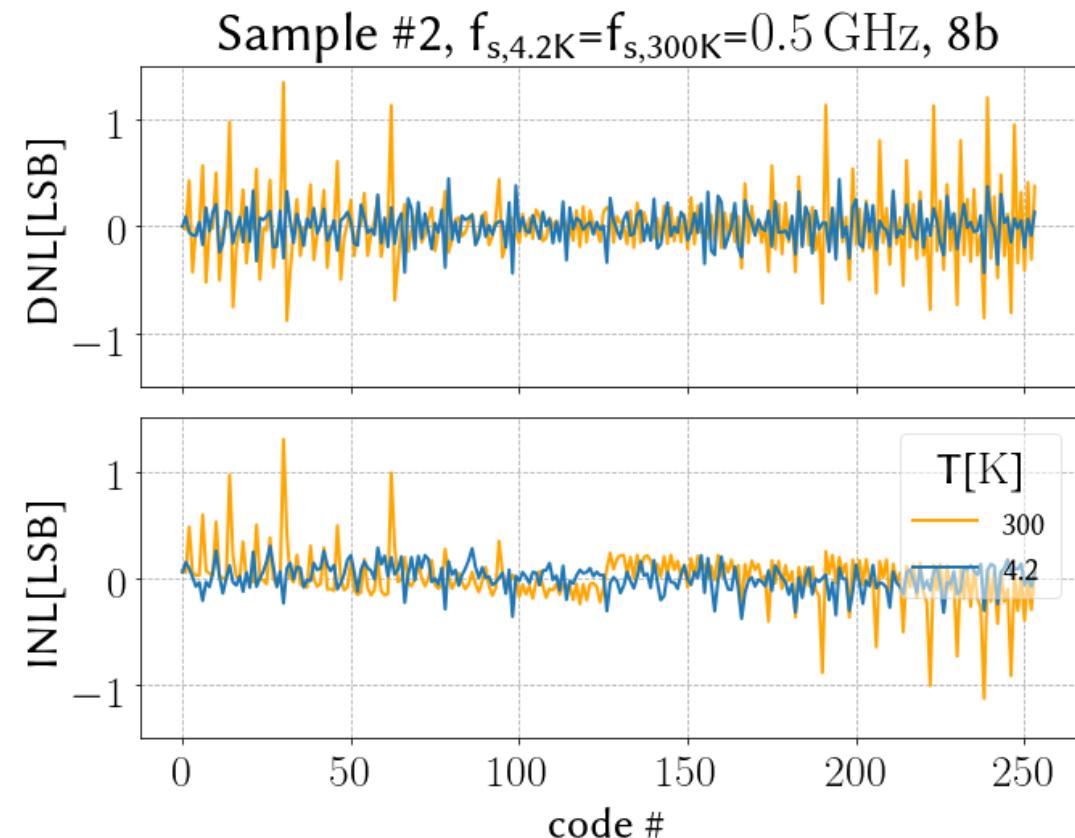
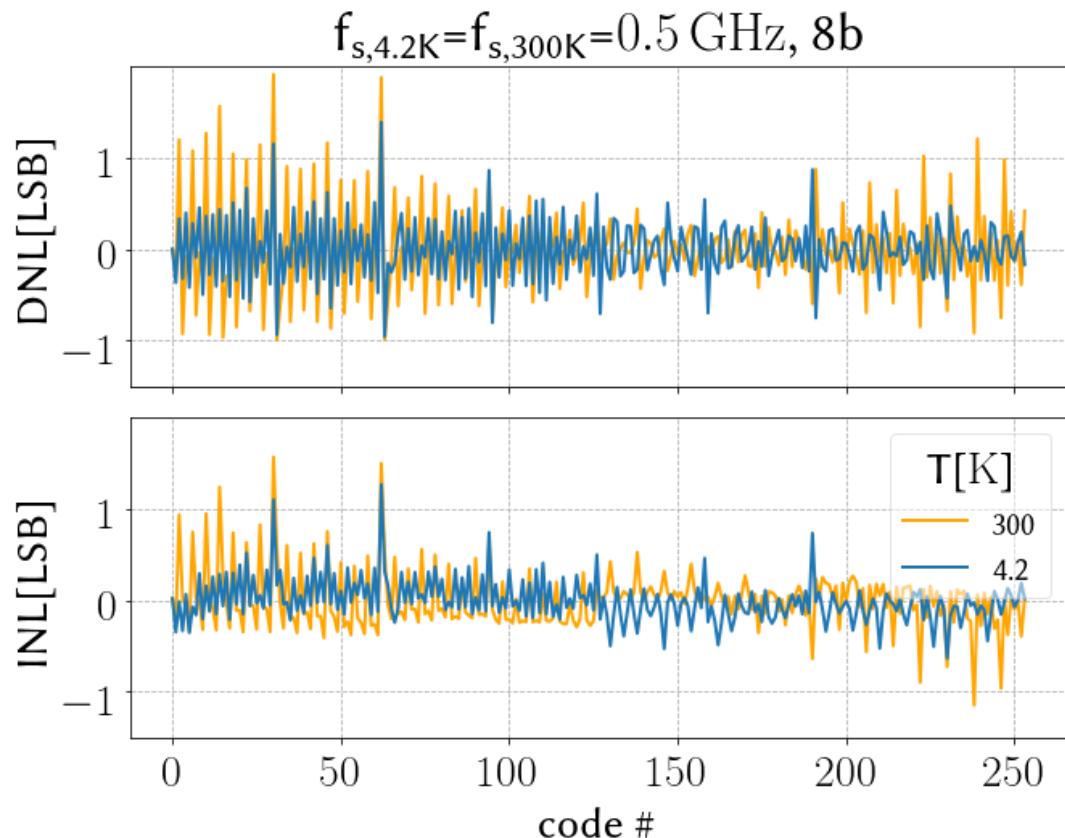
INL/DNL: 8b, 0.5GS/s

- Manual adjustment for 0.5 LSB improvement
- Accuracy of offset cancellation scheme limiting DNL/INL



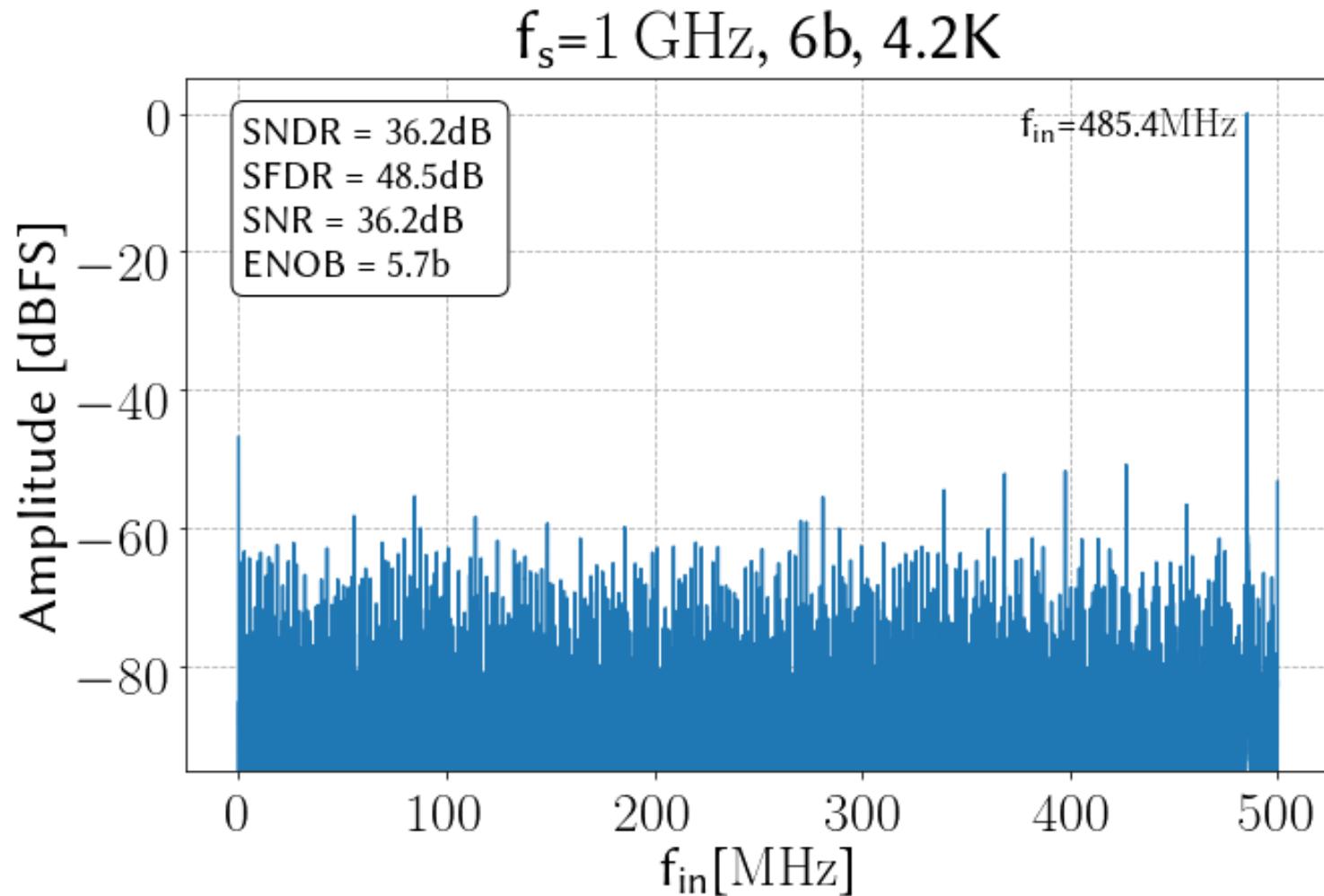
INL/DNL: 8b, 0.5GS/s

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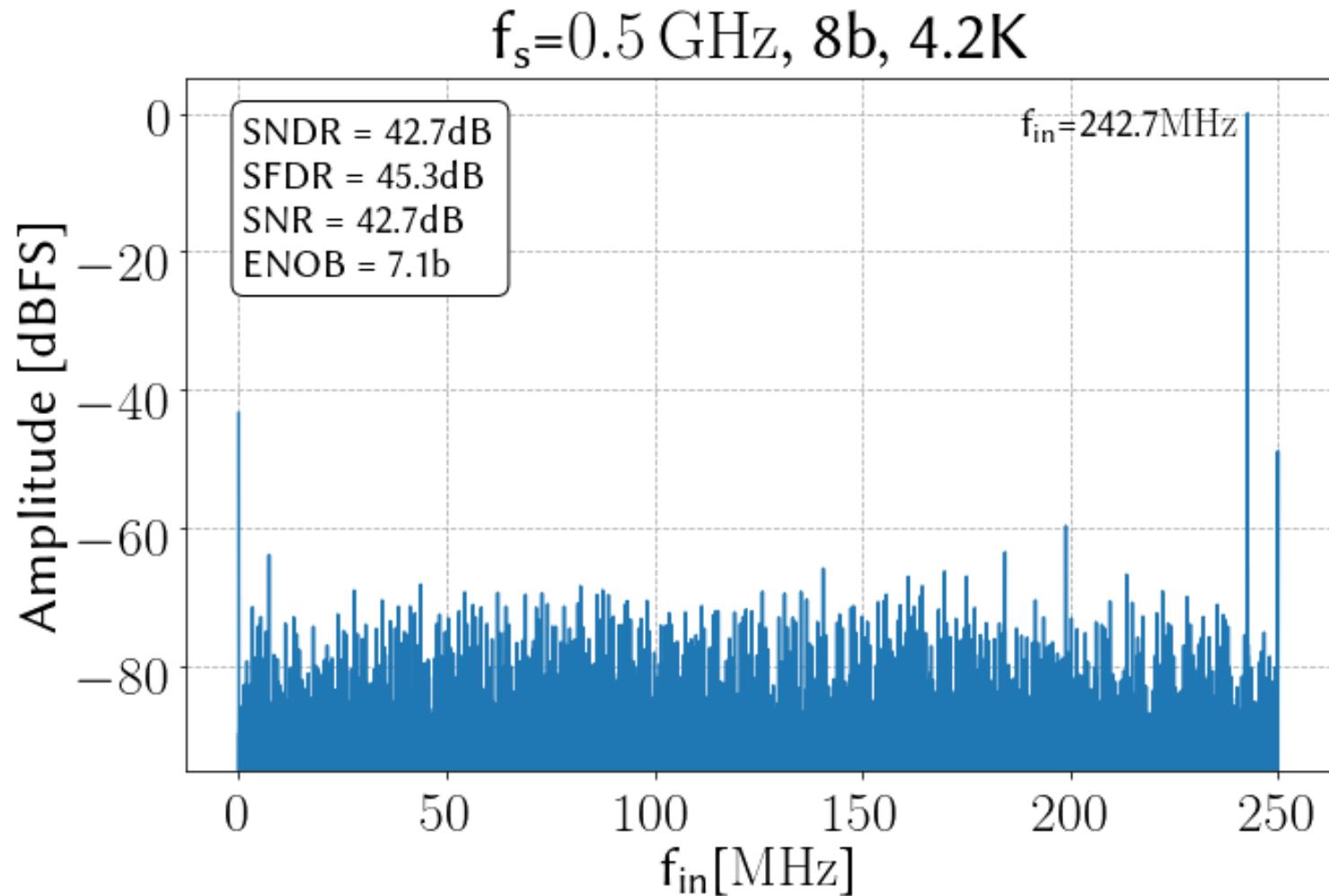
Dynamic performance: 1GS/s

- Nominally 6b
- 1 GS/s
- 5.7b ENOB close to Nyquist

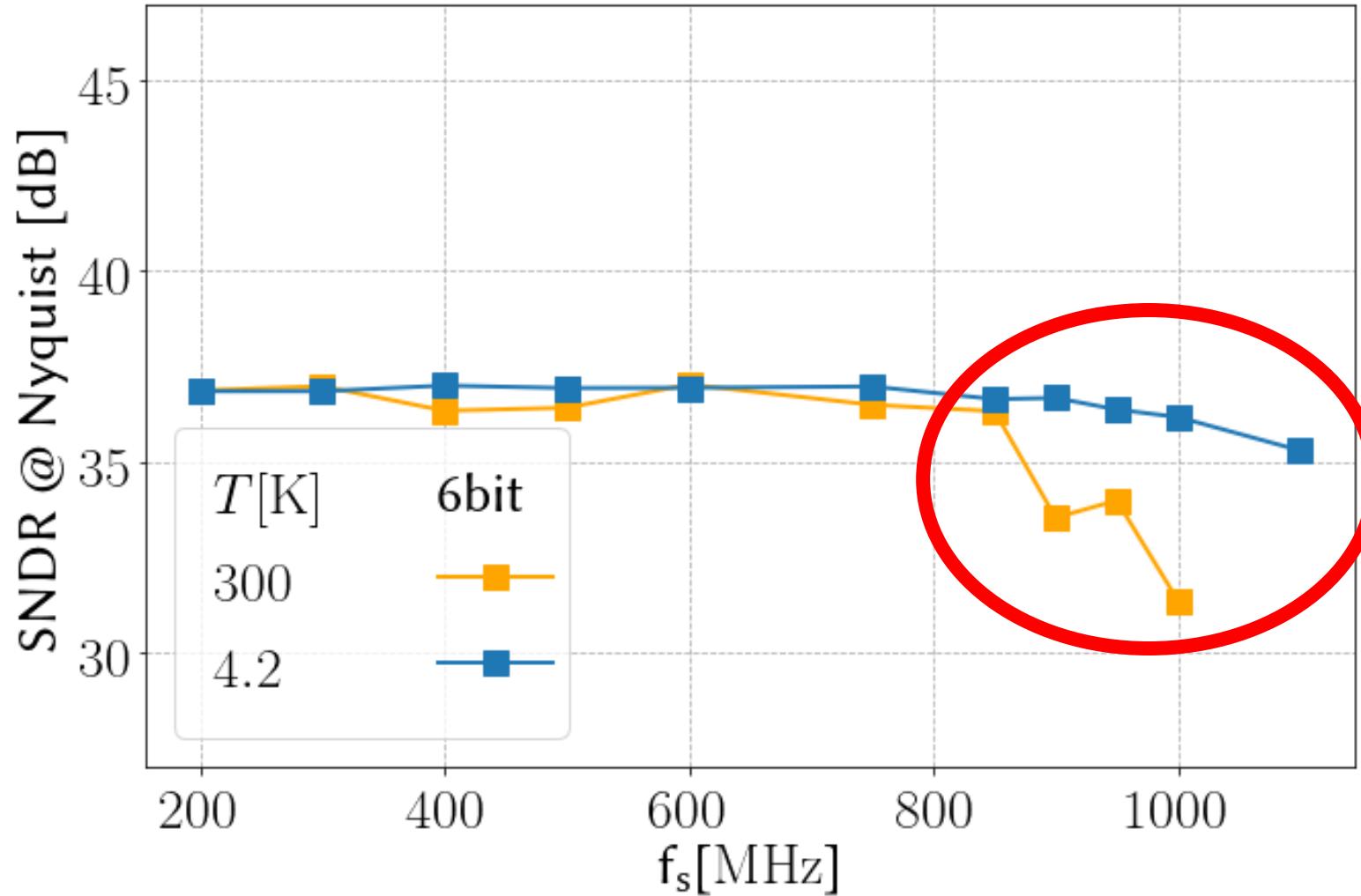


Dynamic performance: 0.5GS/s

- Nominally 8b
- 500MS/s
- 7.1b ENOB close to Nyquist

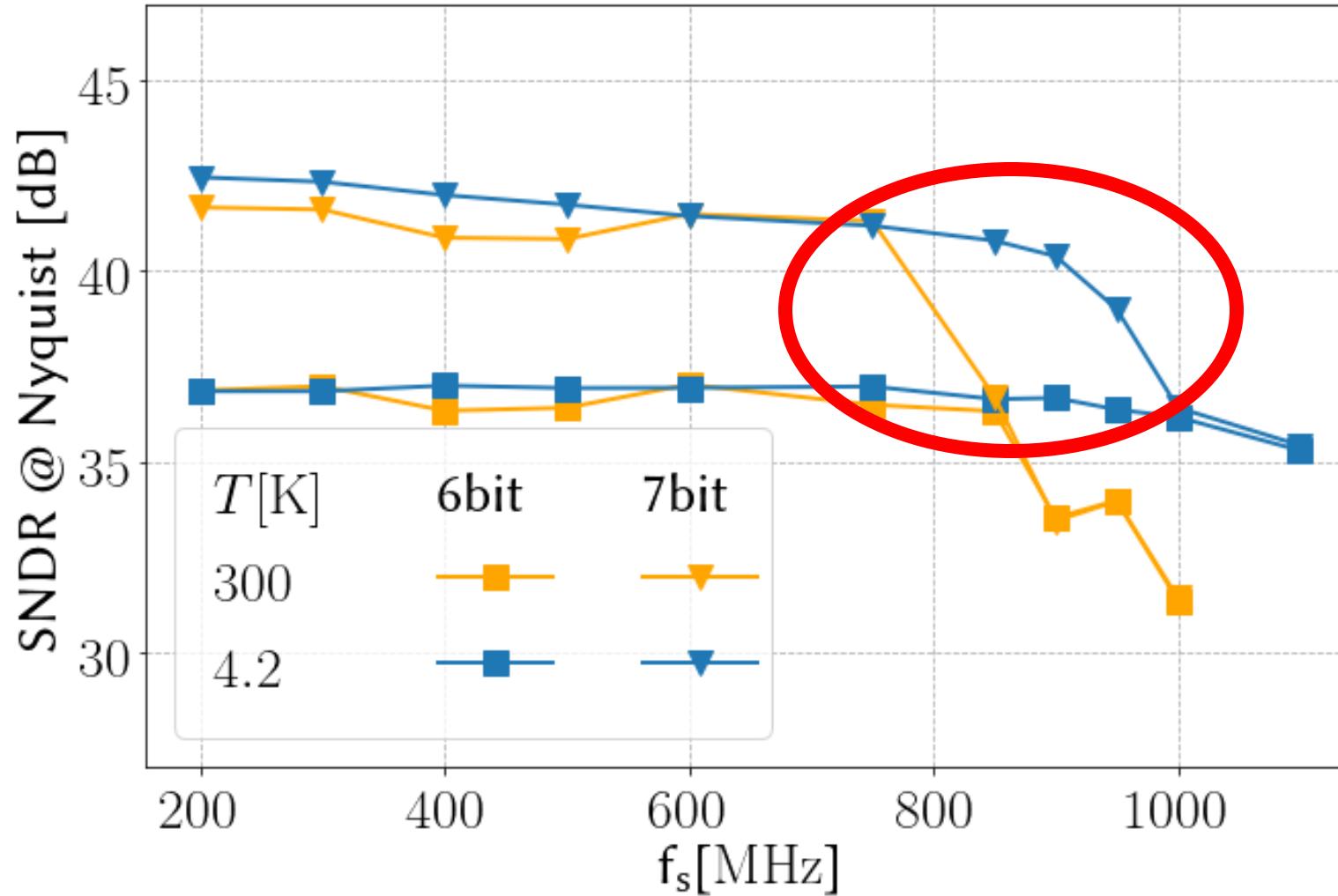


Dynamic performance: f_s sweep



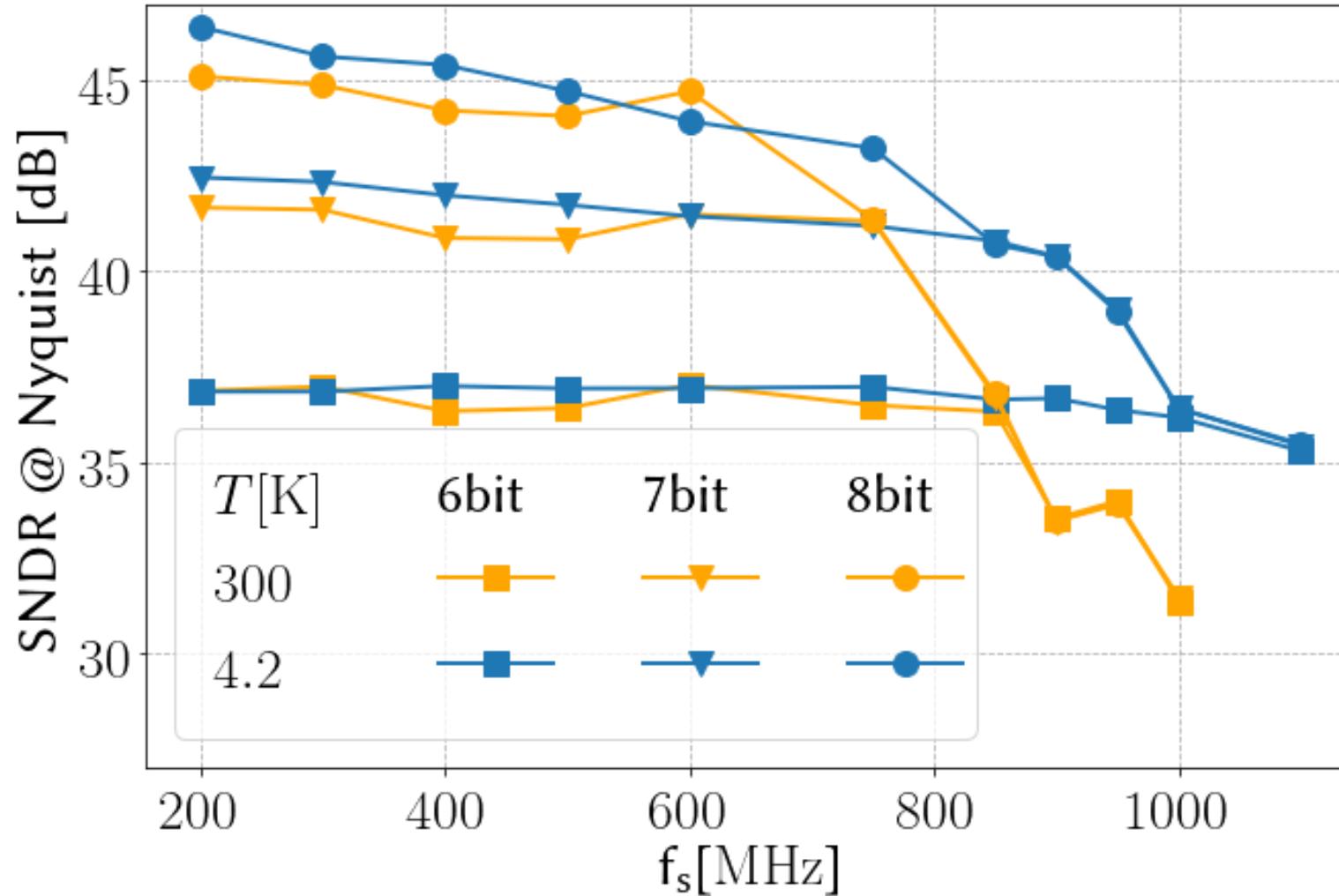
13.4: A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS

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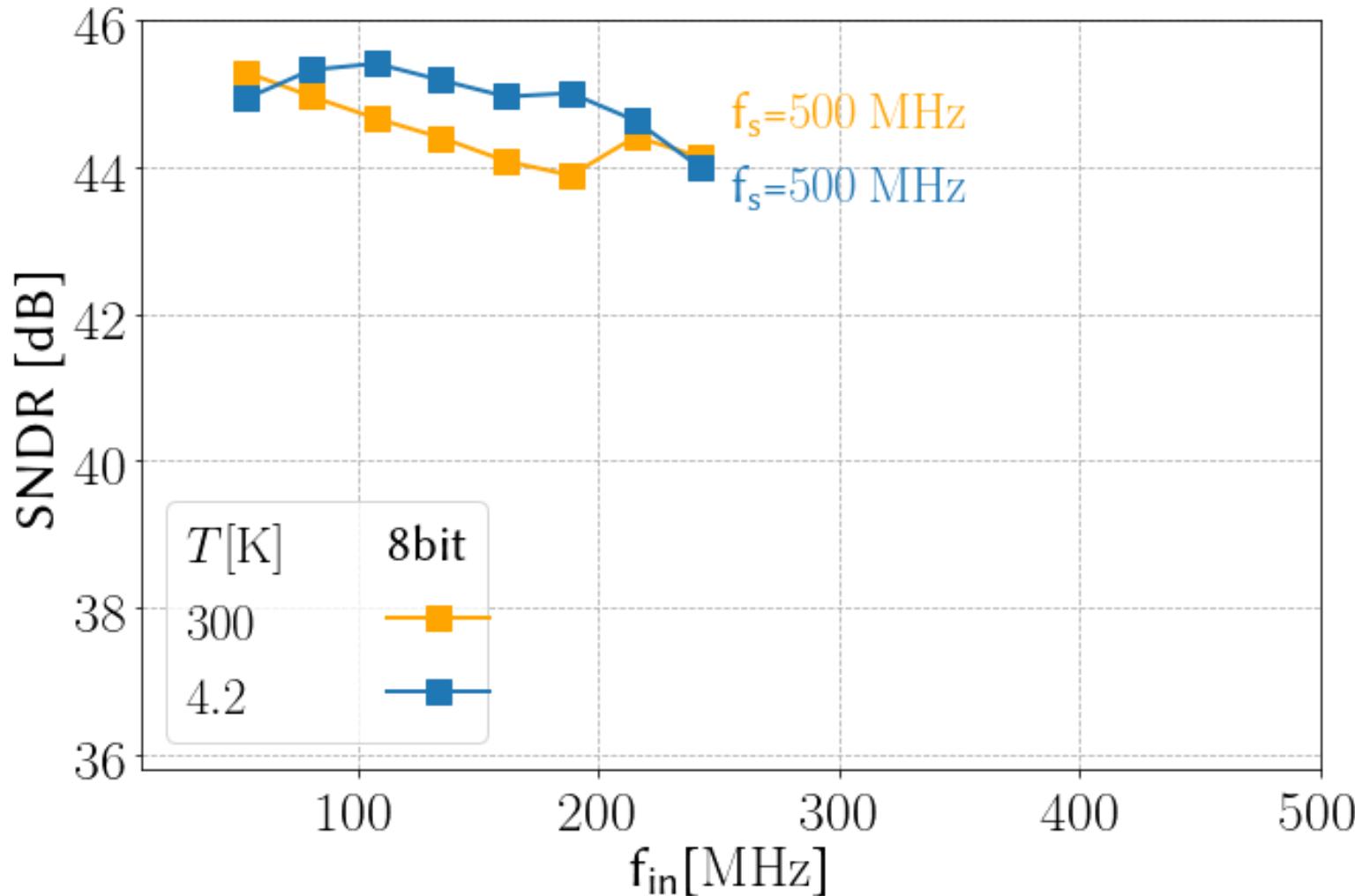
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Dynamic performance: f_s sweep

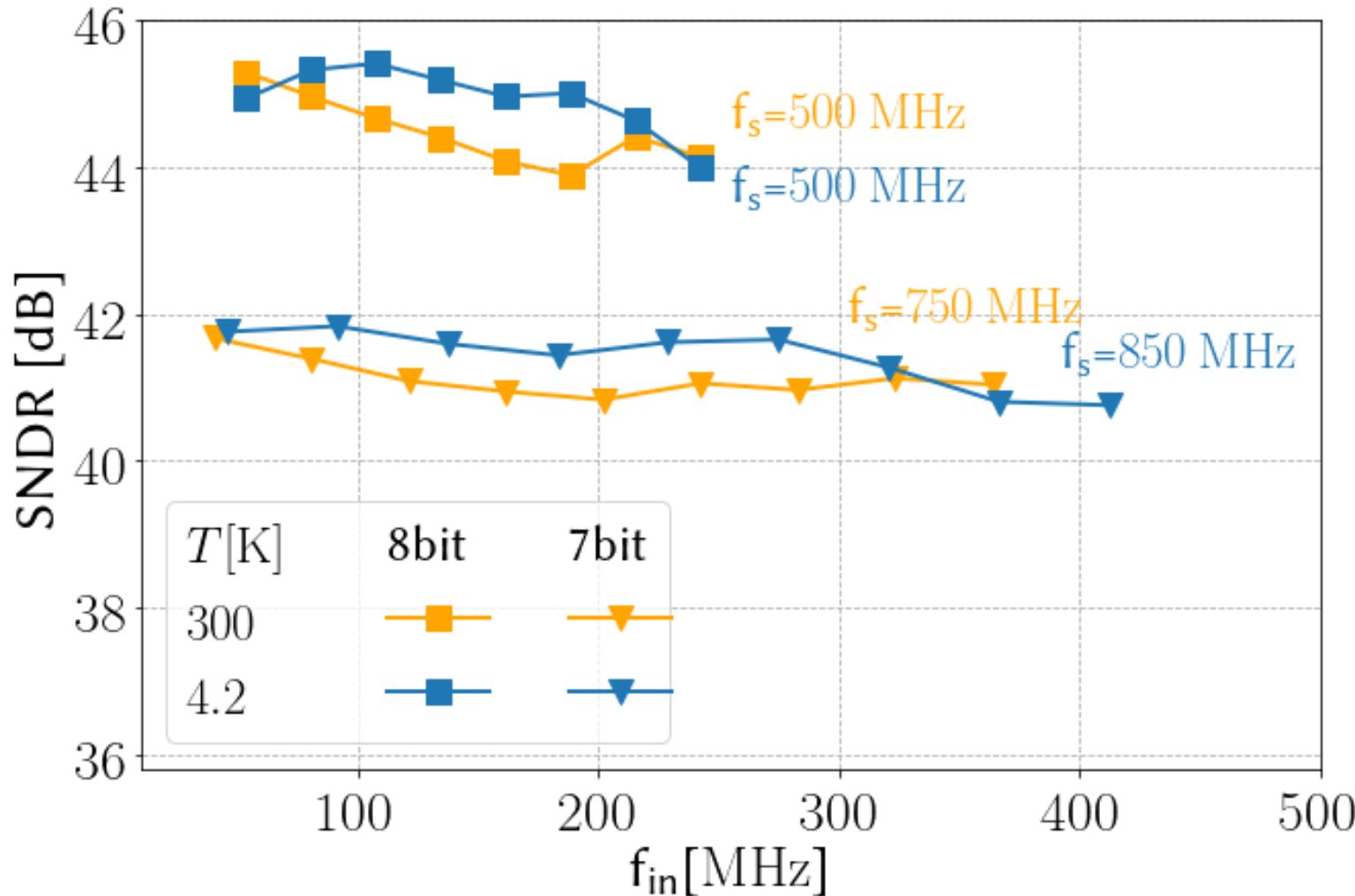


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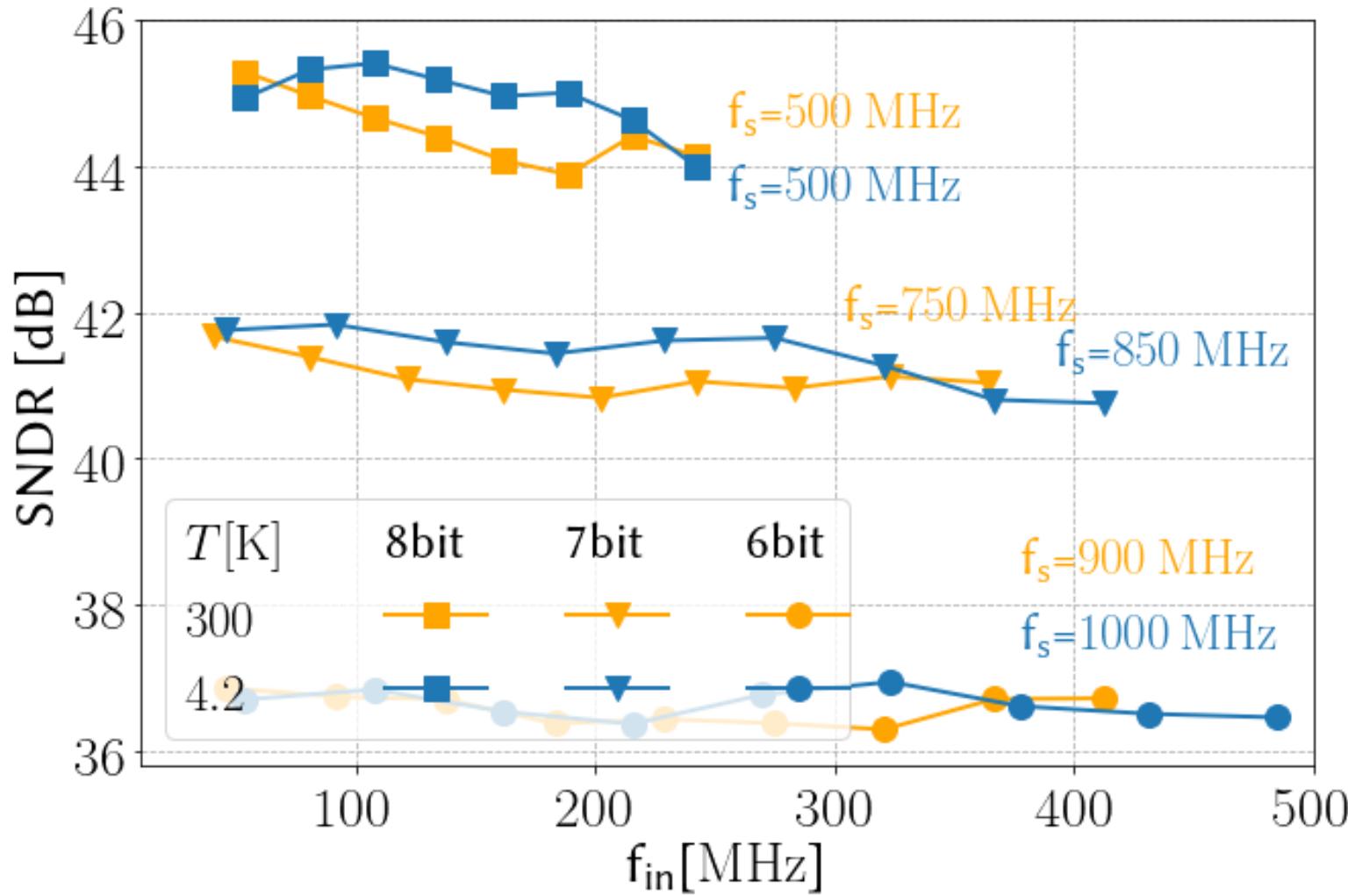
Dynamic performance: f_{in} sweep



Dynamic performance: f_{in} sweep

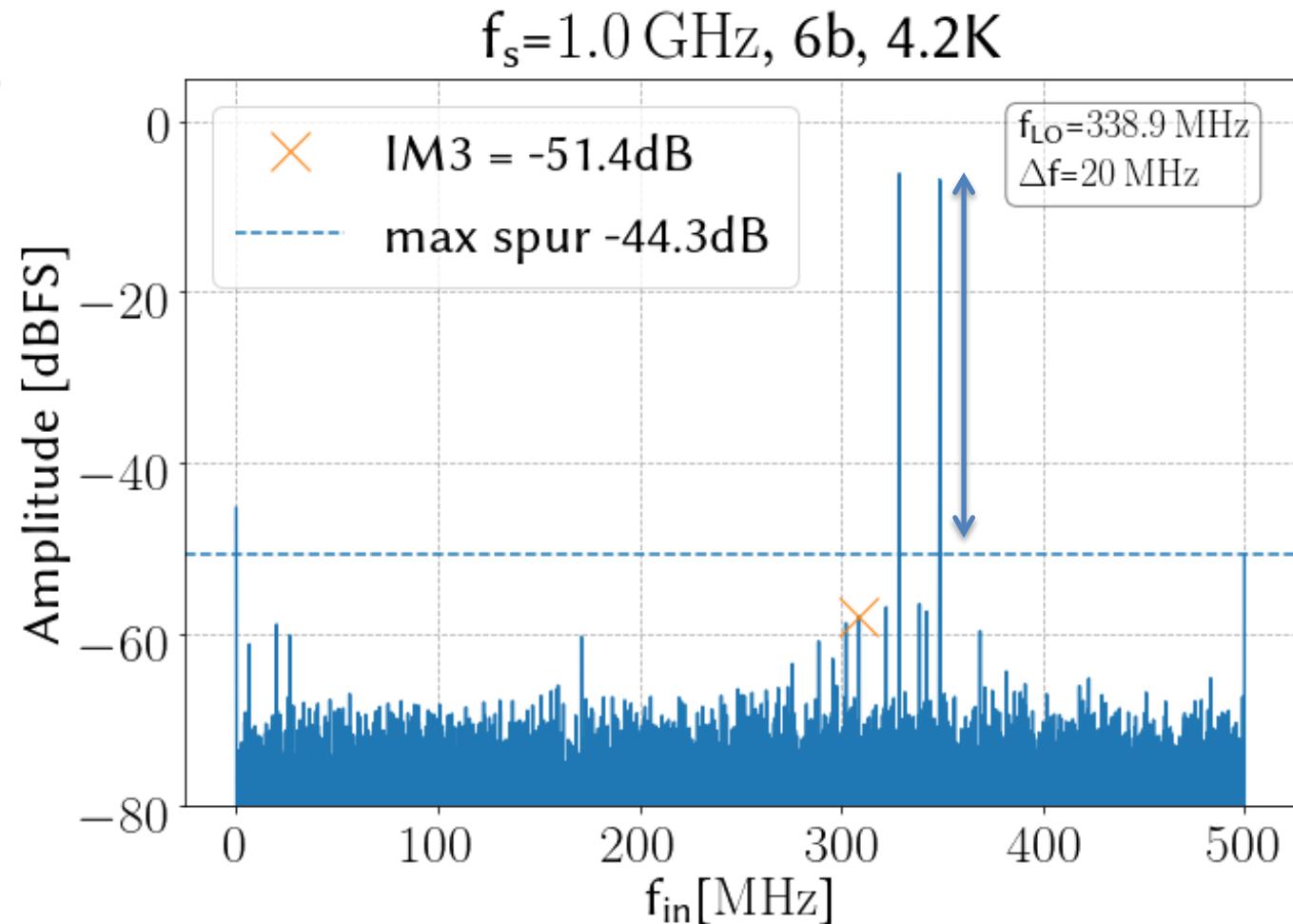


Dynamic performance: f_{in} sweep



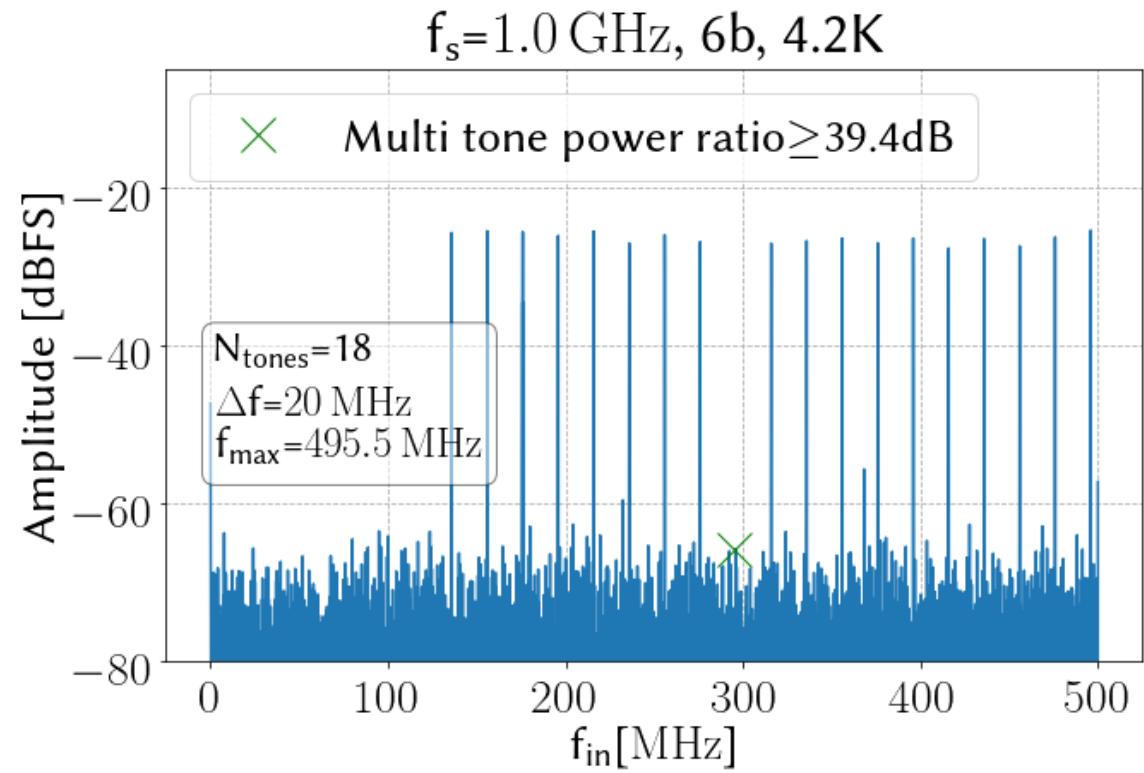
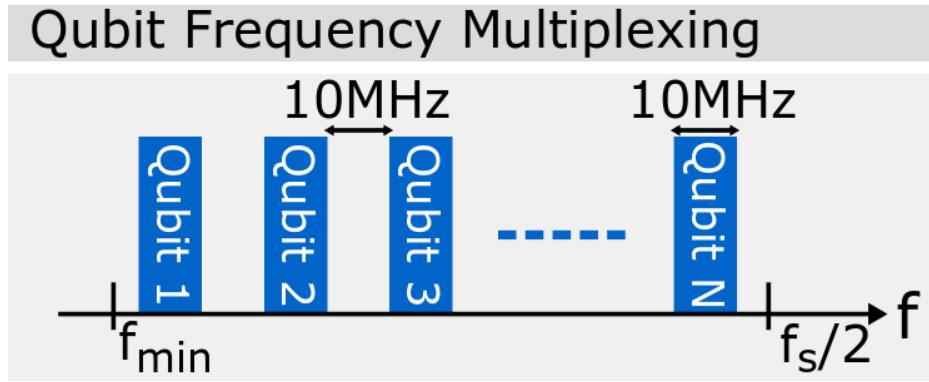
Two tone test

- Maximum spur at $F_s/2$ due to interleaving
- Next spur at <-50dB



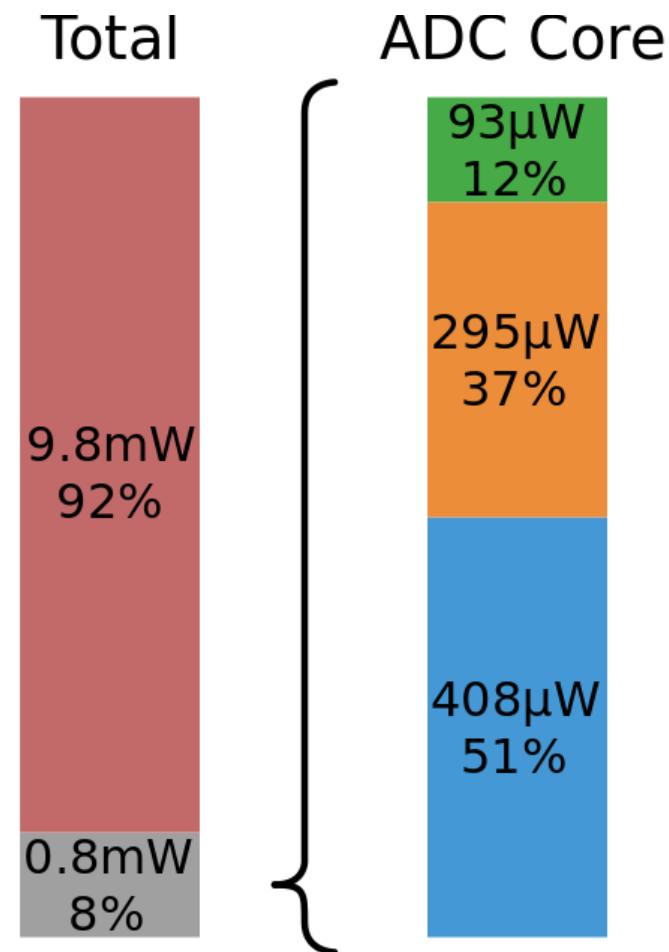
Multi-tone test

- 18 tones, spaced 20MHz
 - 10MHz signal band
 - 10MHz guard band



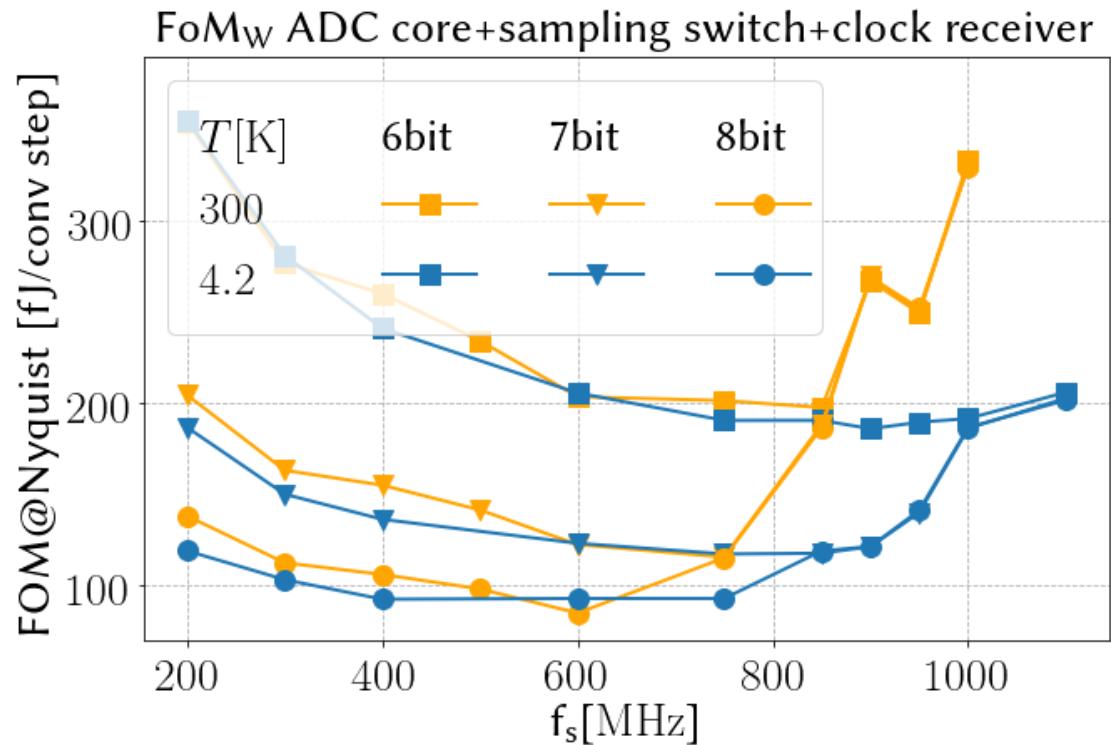
Power breakdown

- Clock receiver: high power
- ADC core: logic power dominating
- For 20x 10MHz qubits:
0.5mW/qubit

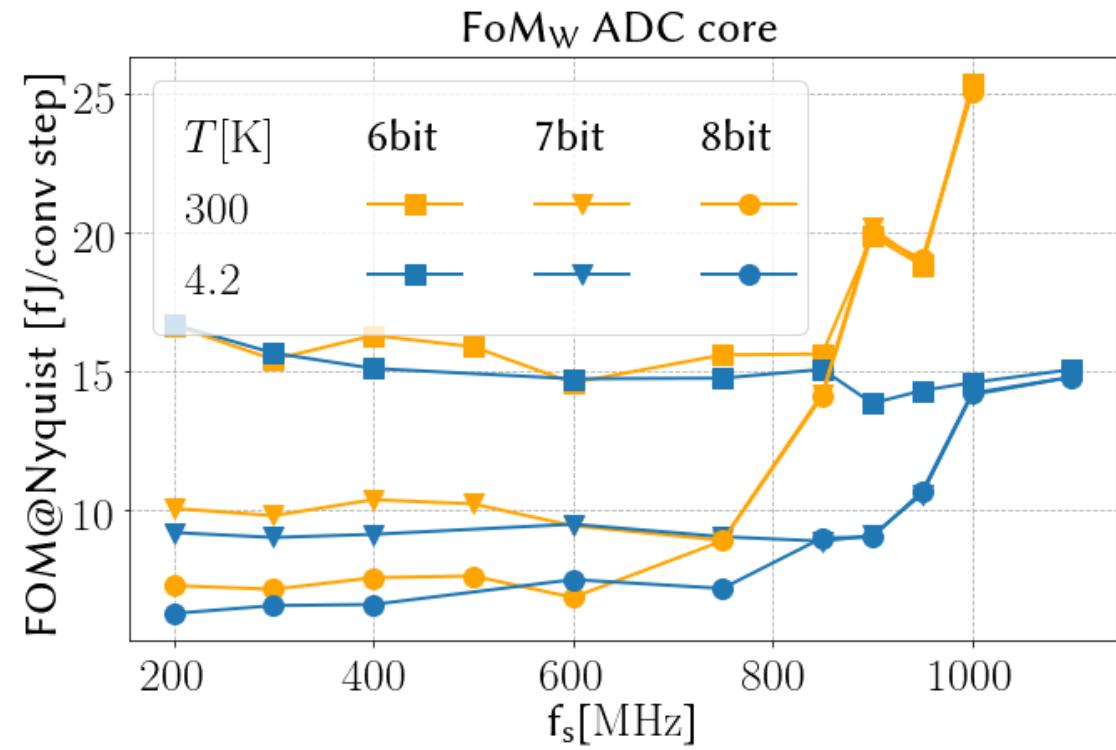
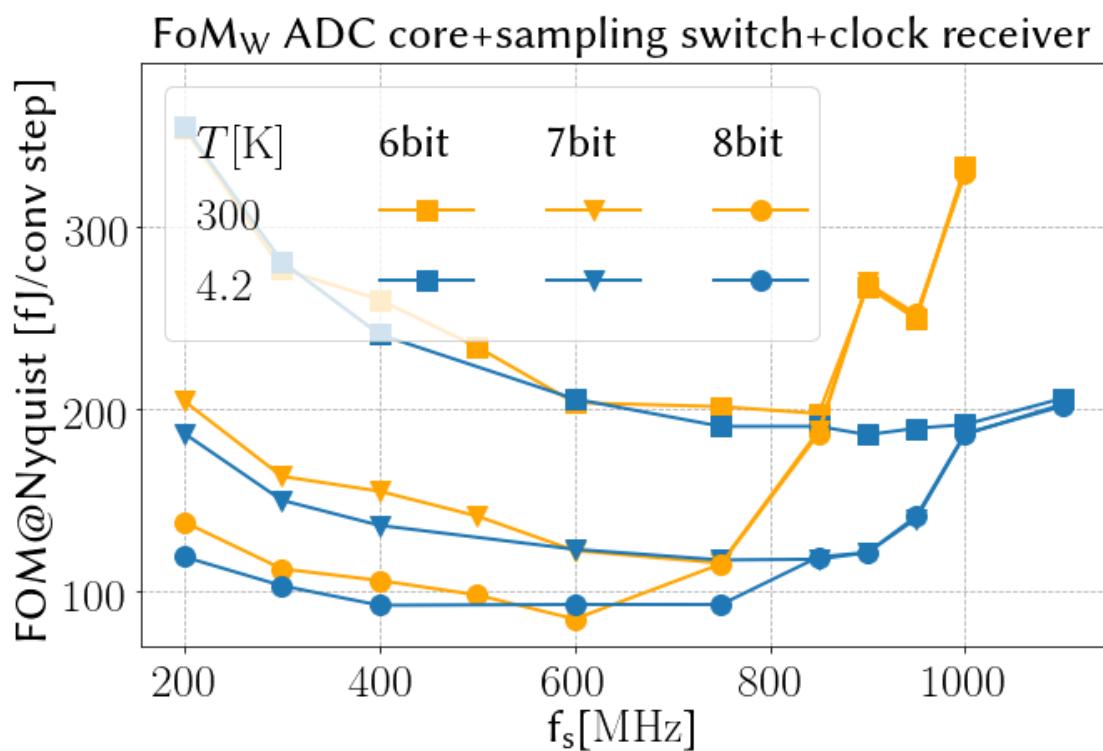


Power@4K,1GS/s ■ ADC Logic
■ ADC Core ■ Reference
■ Clock Receiver ■ Comparators

Efficiency and flexibility

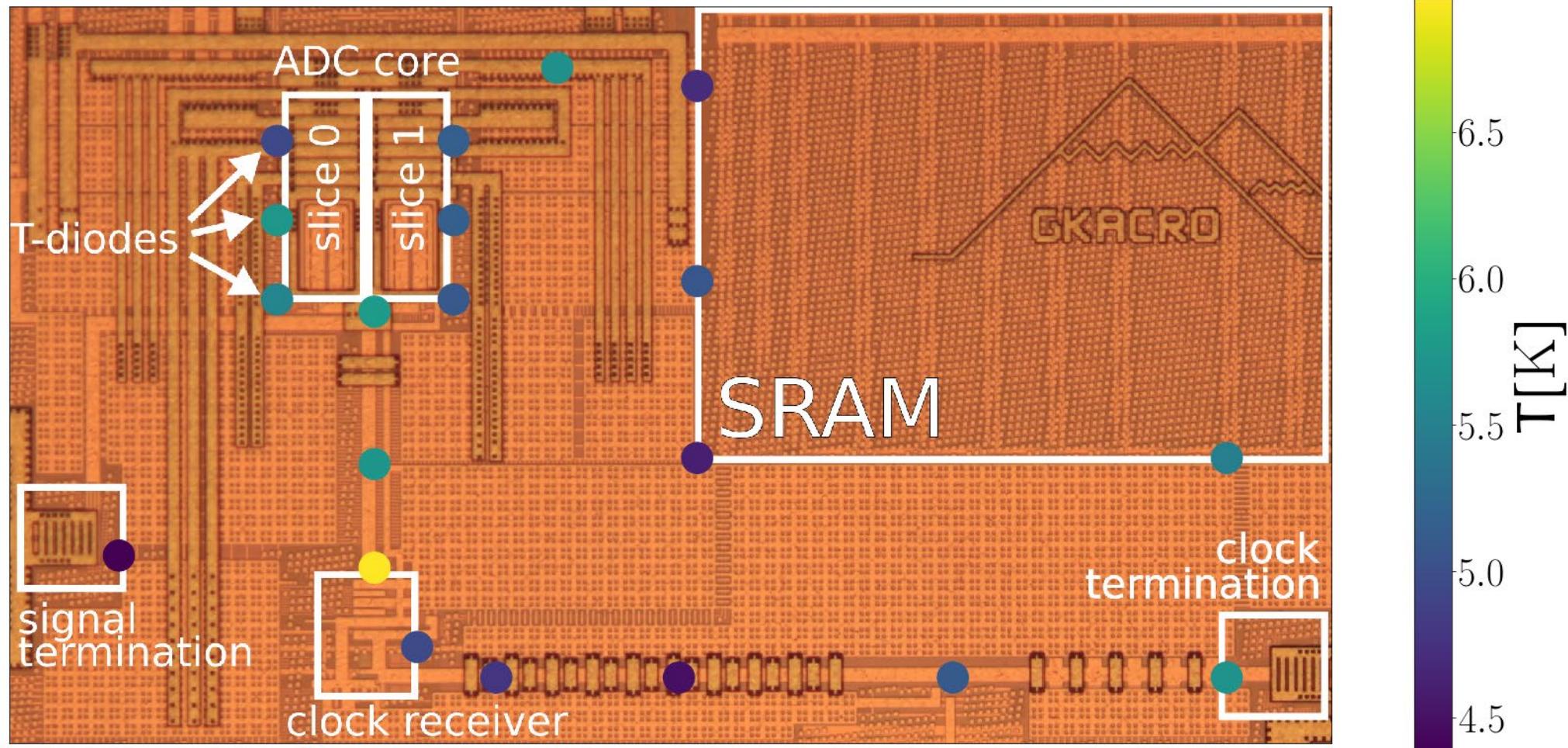


Efficiency and flexibility



On-chip temperature measurement

4.2 K ambient, 6b, $f_s=1$ GHz



13.4: A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS

Outline

- Introduction
- Application
- Circuit implementation
- Experimental characterization
- Conclusion

Comparison table

| | This work | | Okcan, RSI 2010 | Creten, JSSC 2009 | Jiang, JSSC 2012 | Kull, ISSCC 2013 | Kull, ISSCC 2017 |
|------------------------------|--|--|--------------------|-------------------------|------------------------|------------------------|------------------------|
| Temperature [K] | 300 | 4.2 | 4.4 | 4.2 | 300 | 300 | 300 |
| Architecture | TI SAR | | SAR | Flash | SAR | SAR | PP-SAR |
| Max sampling rate [MS/s] | 900 | 1000 | 0.05 | 0.0125 | 1250 | 1300 | 950 |
| Resolution [bit] | 6-8 | | 12 | 8 | 6 | 8 | 10 |
| Technology [nm] | 40 | | 350 | 700 | 40 | 32 | 14 |
| Supplies [V] | 1.1(core), 2.5(clock) | | 3.3 | 5.5 | 1.1 | 1 | 0.7 |
| Input range [Vpp] | 0.7 ² | 0.7 ¹ | - | - | 0.5 | 0.5 | 0.5 |
| SNDR@Nyquist [dB] | 33.4 ² | 36.2 ¹ | 48.7 | - | 27.7 | 39.3 | 50 |
| SFDR [dB] | 48.4 ² | 48.5 ¹ | 57.9 | - | 39 | 49.6 | 58 |
| Power [mW] | 0.7 ^{2,3} (10.3 ^{2,4}) | 0.8 ^{1,3} (10.6 ^{1,4}) | 0.297 | 5.1 | 5.28 | 3.1 | 2.26 |
| FoM _w [fJ/c.step] | 20 ^{2,3} (260 ^{2,4}) | 15 ^{1,3} (200 ^{1,4}) | 16100 | 1.6 · 10 ⁶ ‡ | 148 | 28 | 8.9 |
| Core area [mm ²] | 0.045 | | 2.7 ⁵ | 40 ⁵ | 0.014 | 0.0015 | 0.0016 |

¹6b, 1GS/s ²6b, 0.9GS/s ³ADC core ⁴Core + clock receiver + sampling switch ⁵full chip ‡estimated from INL

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| Power [mW] | 0.7 ^{2,3} (10.3 ^{2,4}) | 0.8 ^{1,3} (10.6 ^{1,4}) | 0.297 | 5.1 | 5.28 | 3.1 | 2.26 |
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¹6b, 1GS/s ²6b, 0.9GS/s ³ADC core ⁴Core + clock receiver + sampling switch ⁵full chip [†]estimated from INL

Comparison table

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| Core area [mm ²] | 0.045 | | 2.7 ⁵ | 40 ⁵ | 0.014 | 0.0015 | 0.0016 |

¹6b, 1GS/s ²6b, 0.9GS/s

³ADC core

⁴Core + clock receiver + sampling switch

⁵full chip

‡estimated from INL

Conclusion

- Scaling up quantum computers requires a cryo-CMOS interface
- First high-speed cryo-CMOS ADC
- Highlights:
 - 1GS/s: 5.7b ENOB
 - Supporting 20x 5MHz qubit channels
 - ADC power <0.5mW/qubit
- Suitable for closing the qubit control loop at cryogenic temperature

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