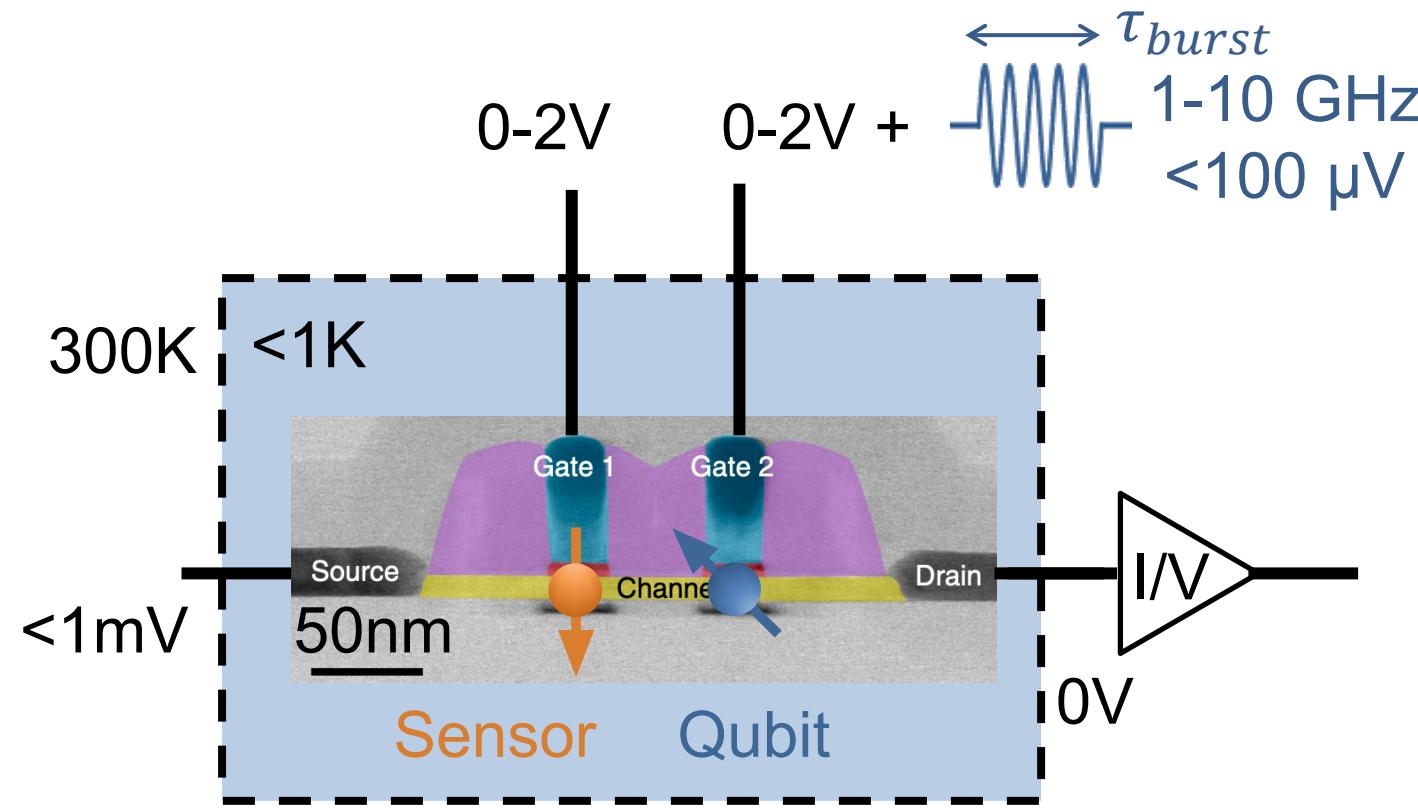
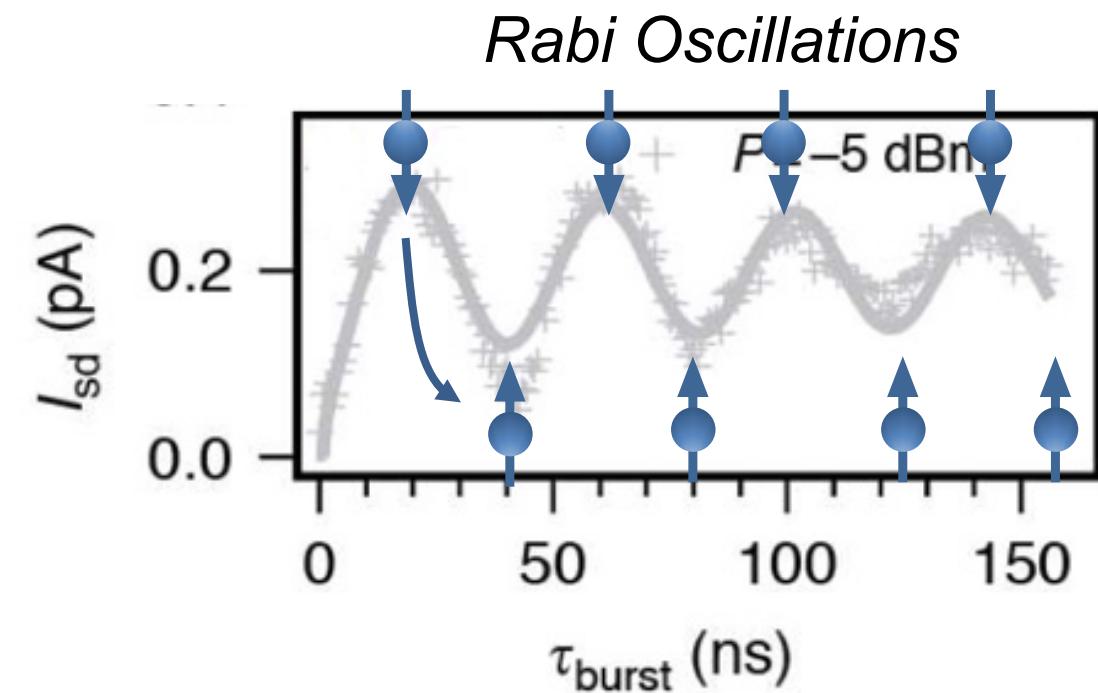


Silicon Spin Qubit Manipulation



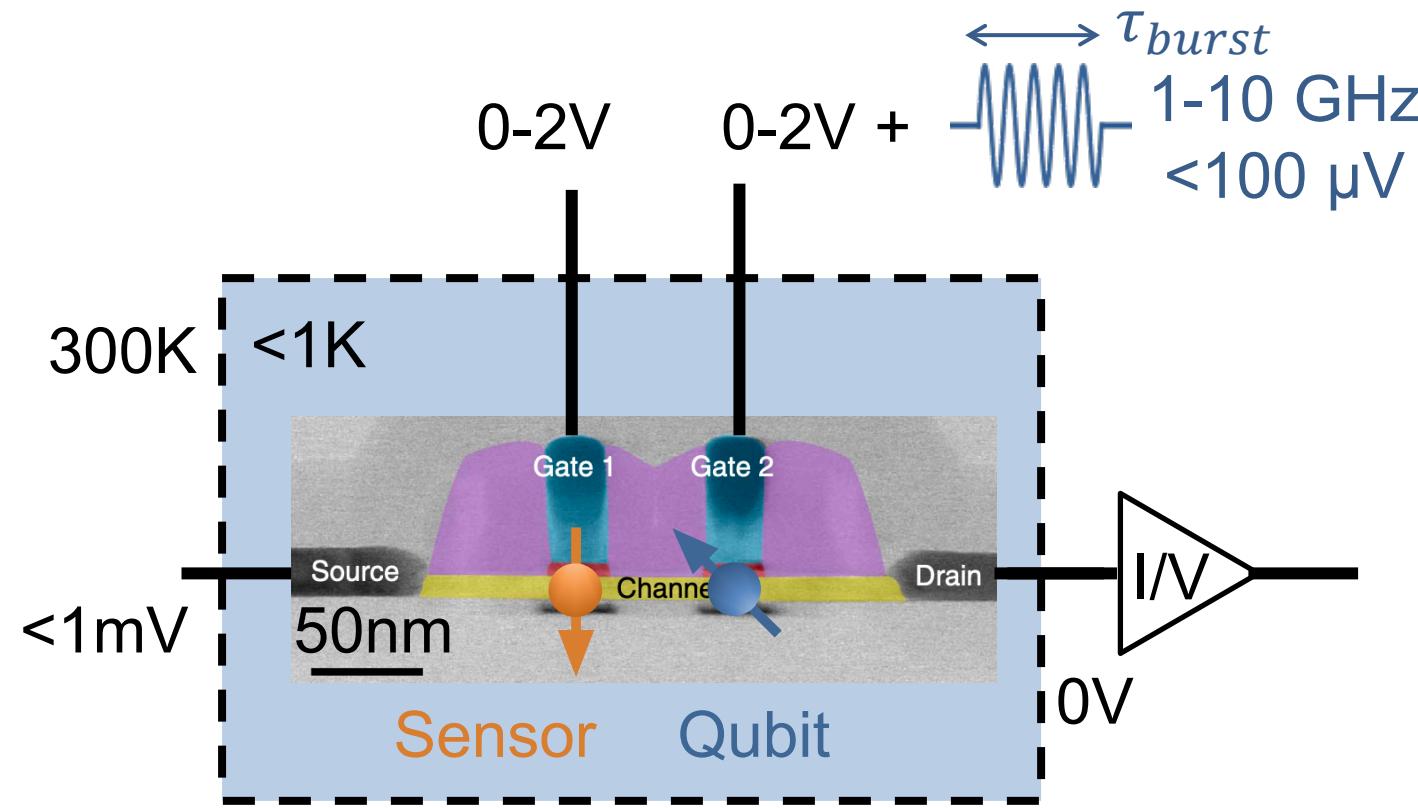
Current Read-out

Charge stability diagram,
quantum effects,...

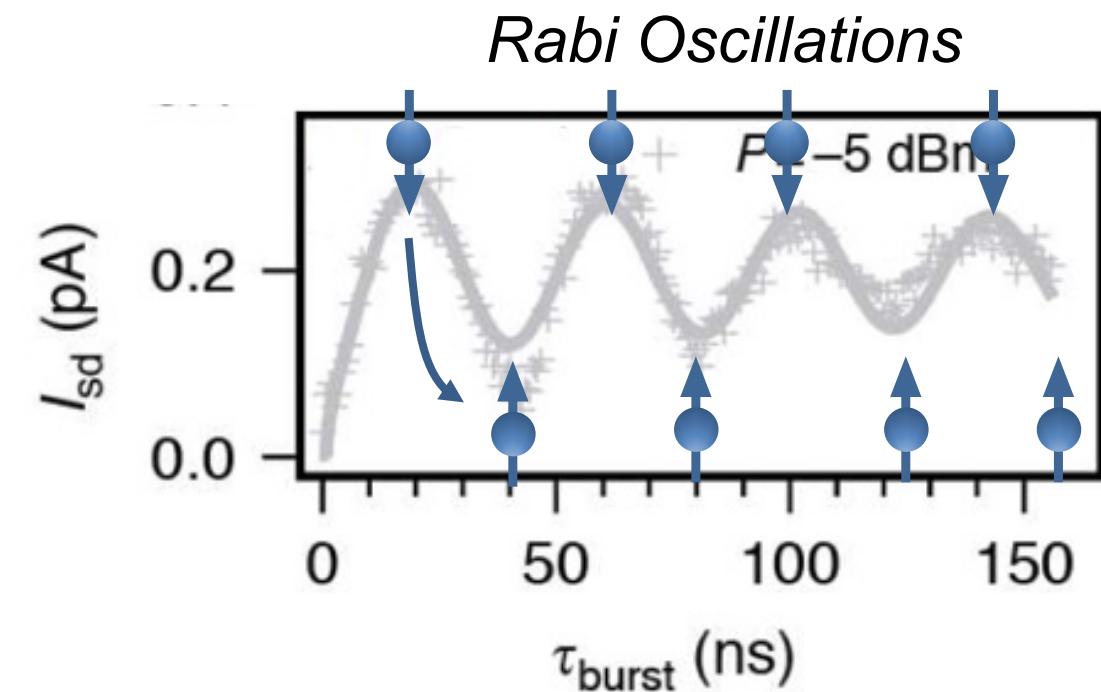


R. Maurand et al. (2016)

Silicon Spin Qubit Manipulation

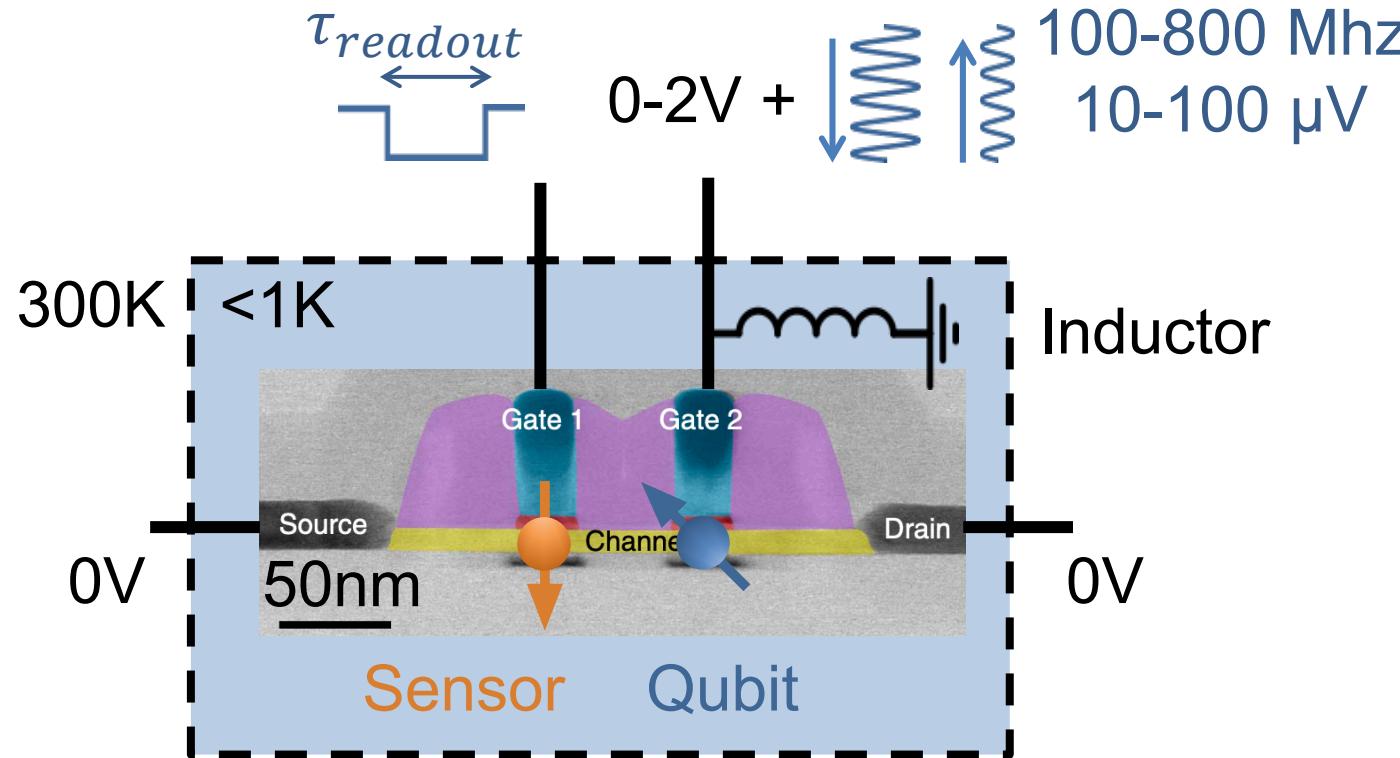


20ns Qubit Manipulation

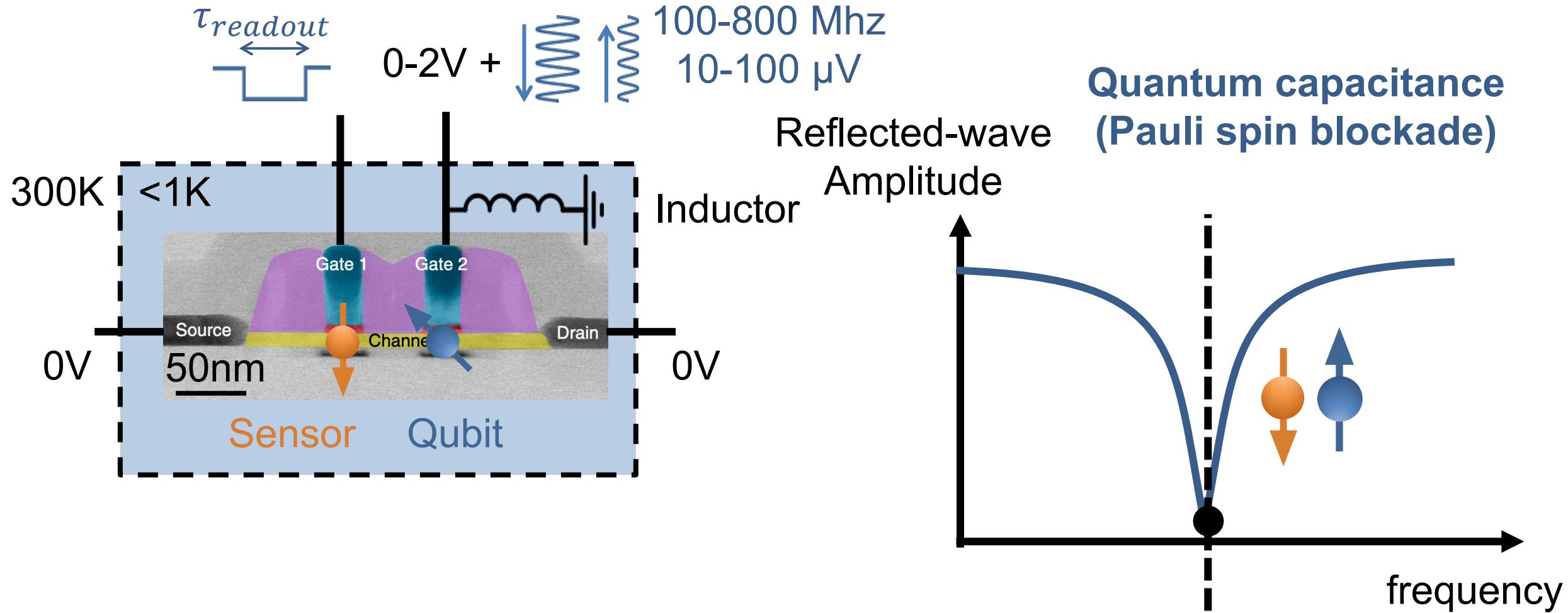


R. Maurand et al. (2016)

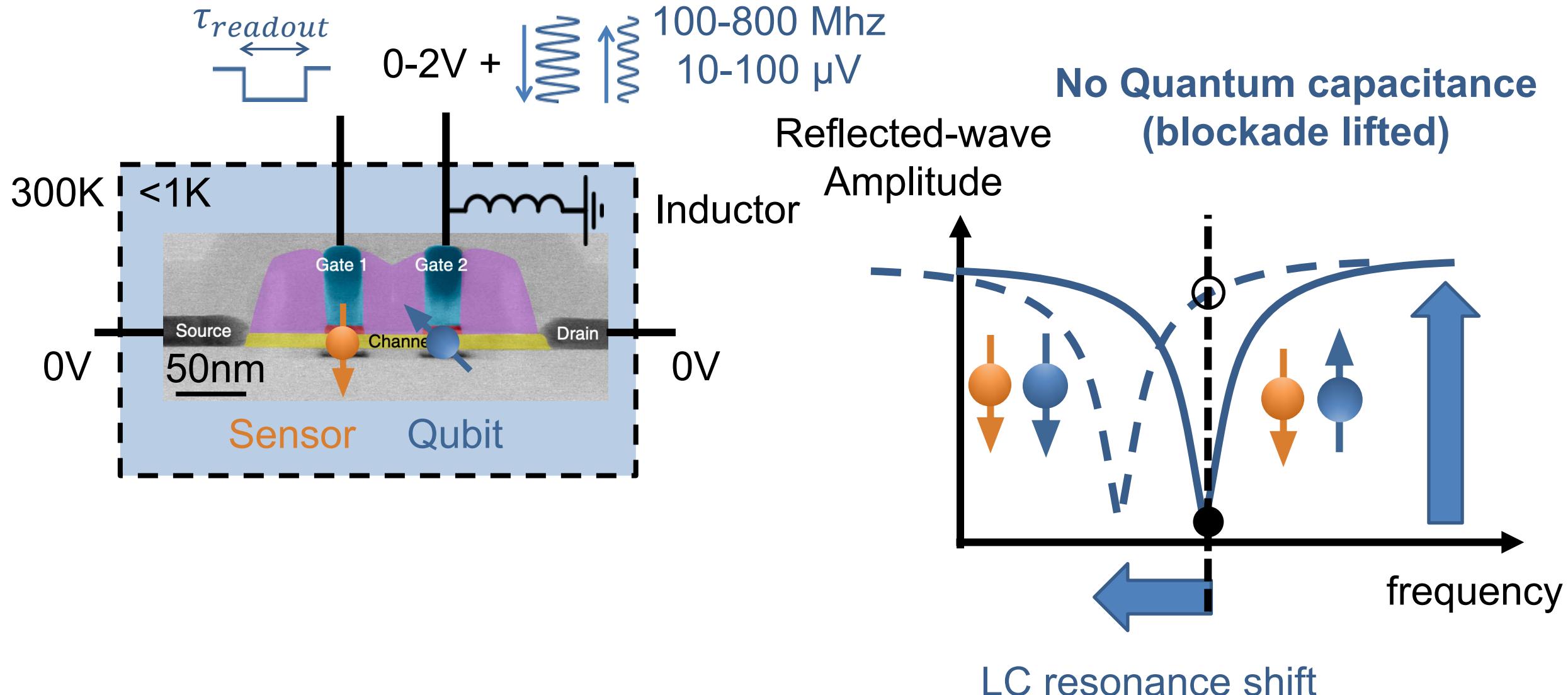
RF Reflectometry Spin Qubit Read-out



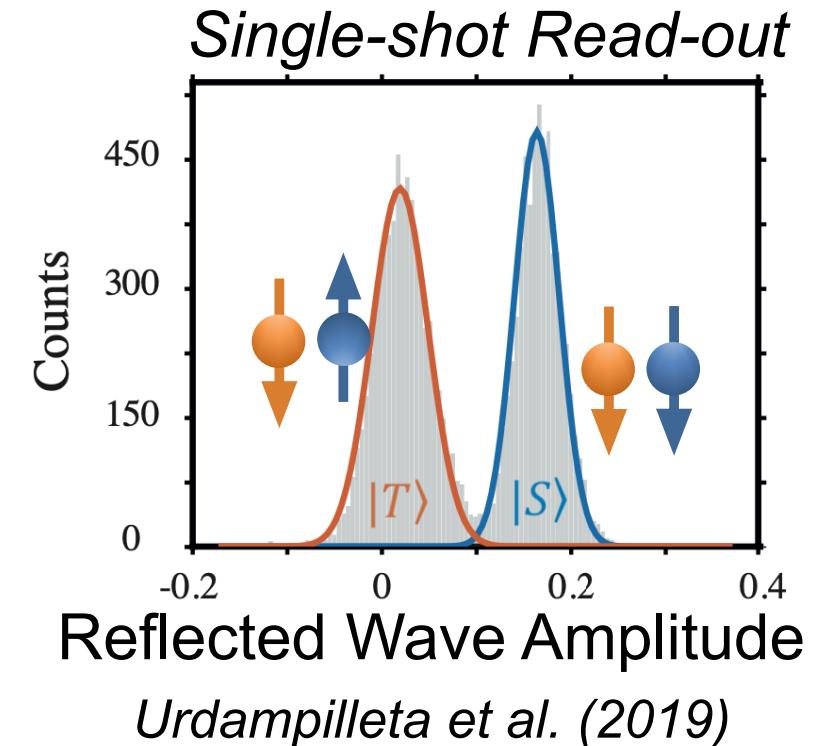
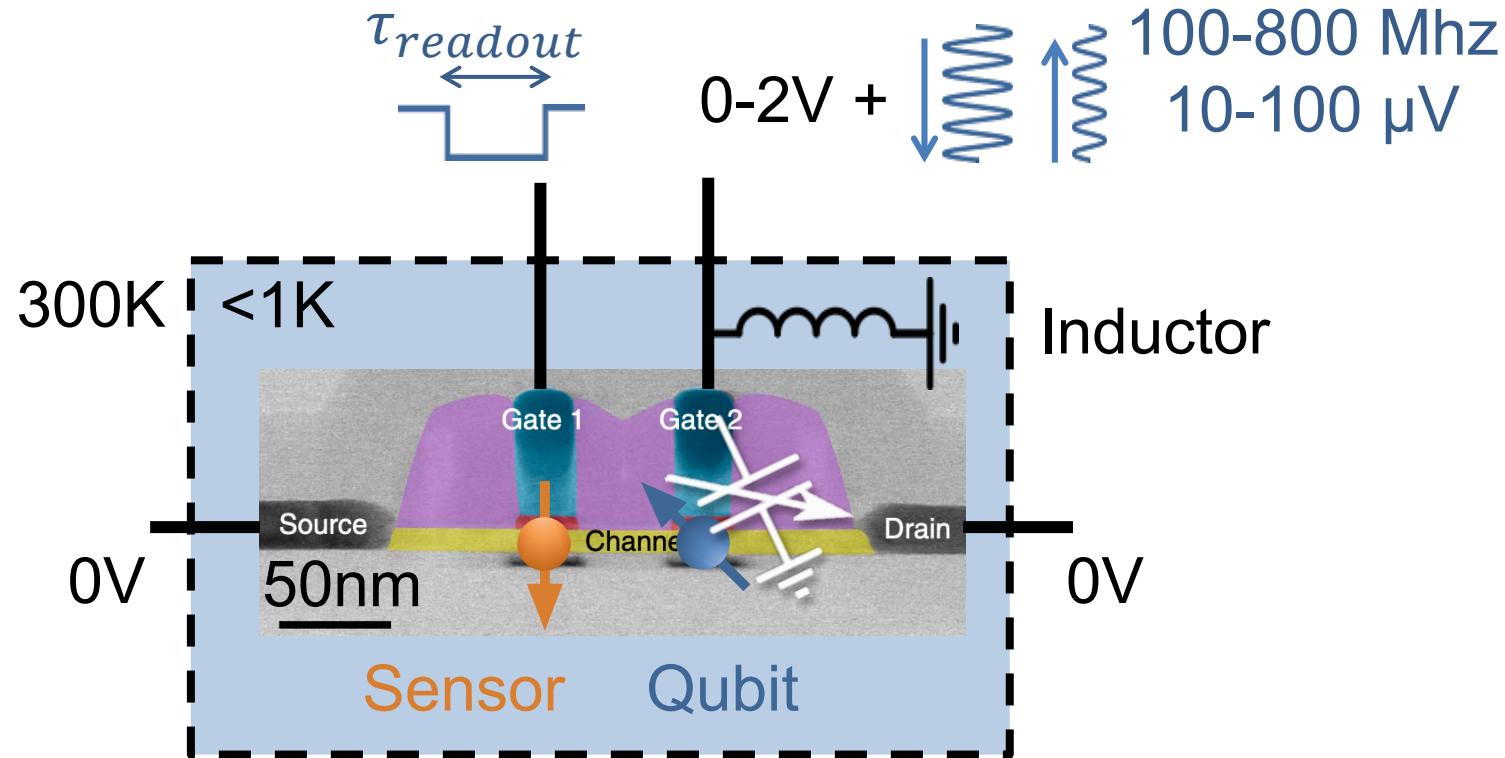
RF Reflectometry Spin Qubit Read-out



RF Reflectometry Spin Qubit Read-out



RF Reflectometry Spin Qubit Read-out

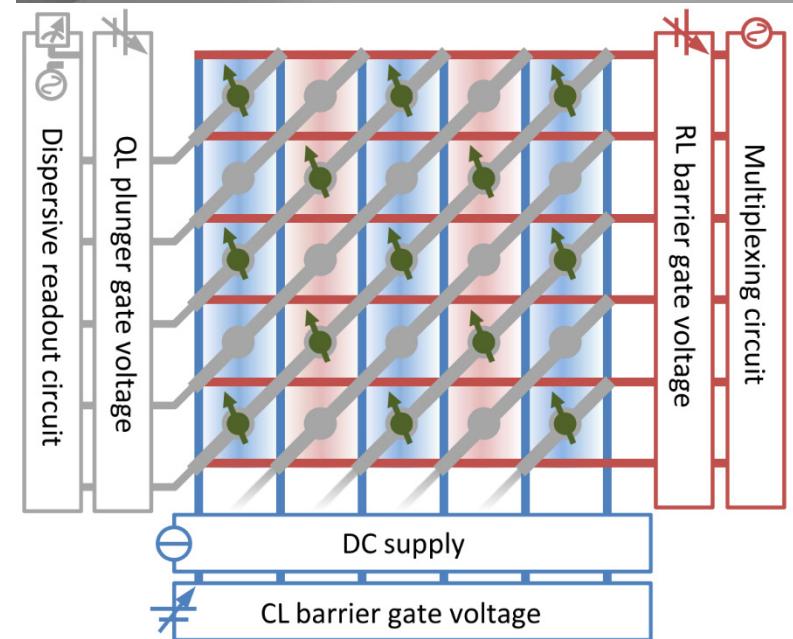
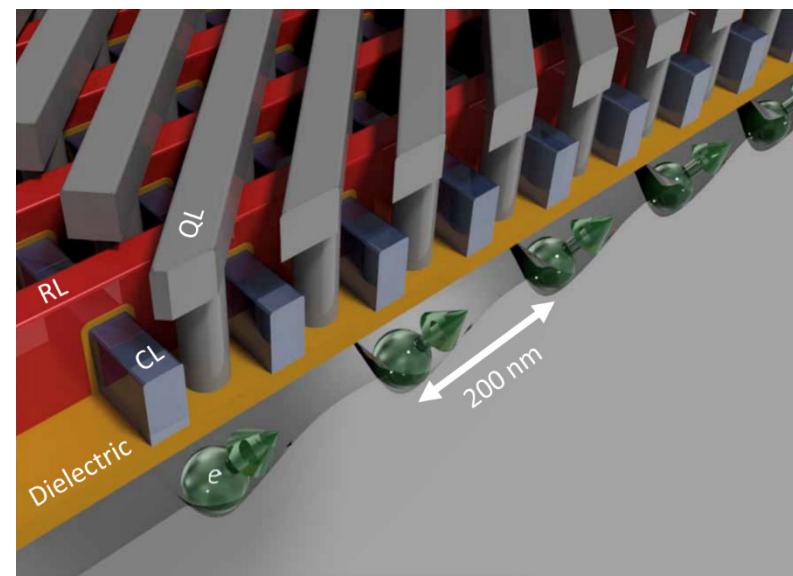
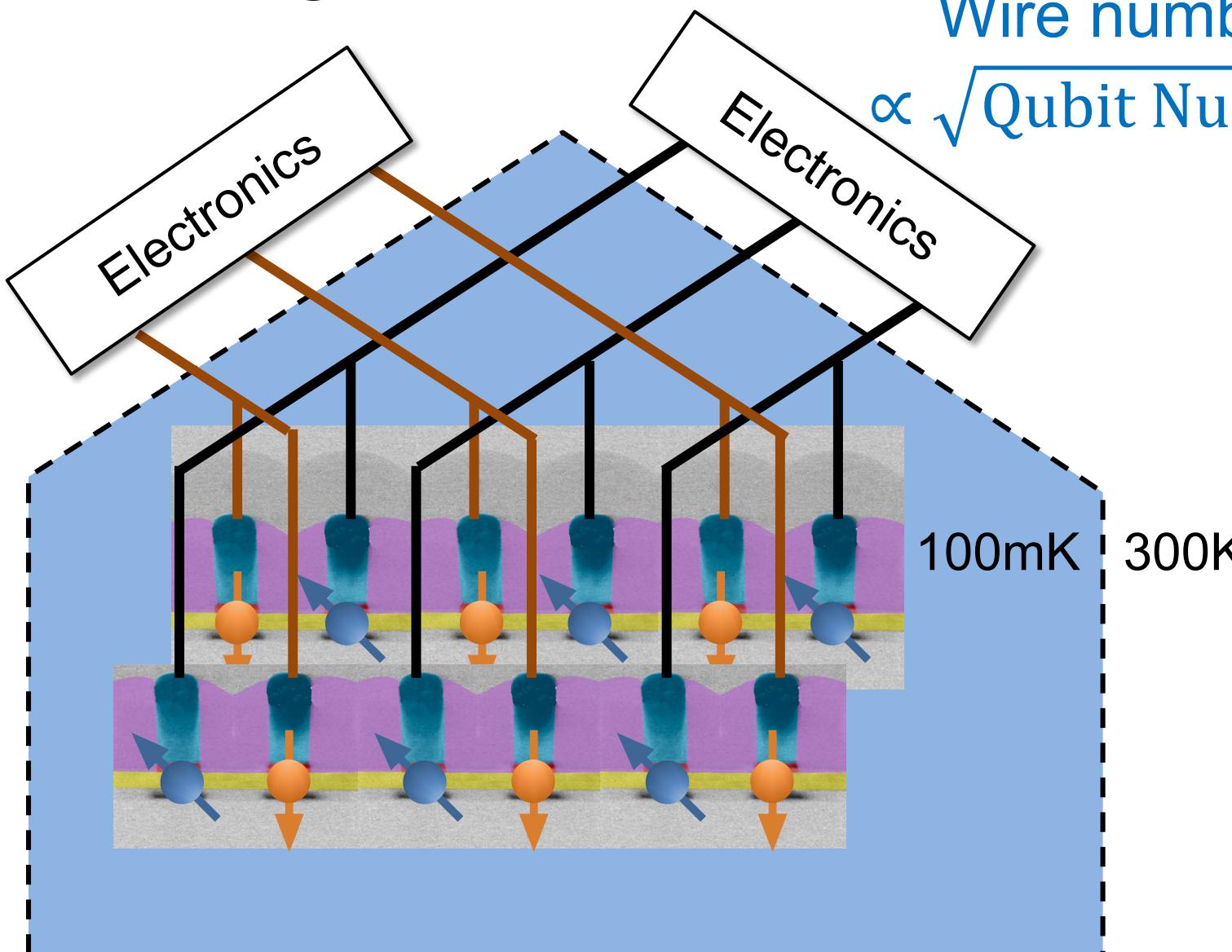


99.7% fidelity at 100mK

Scaling up of the qubit number

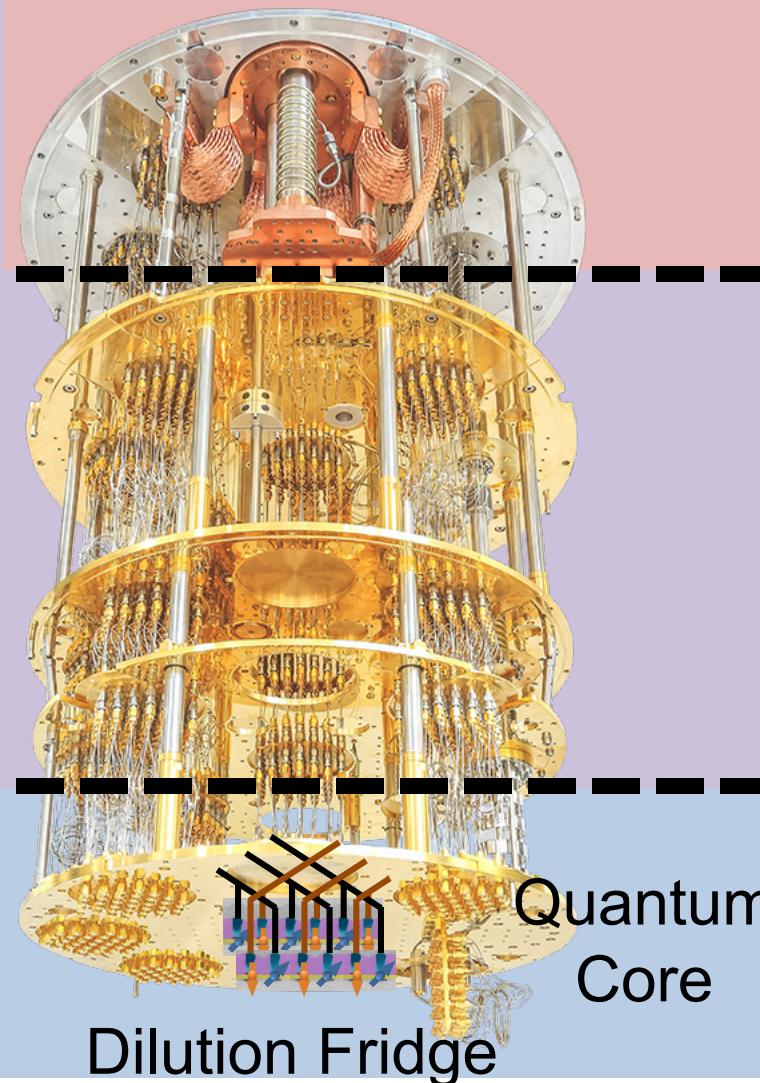
Wire number

$$\propto \sqrt{\text{Qubit Number}}$$



R. Li et al. (2018)

The need for interface electronics



300 K

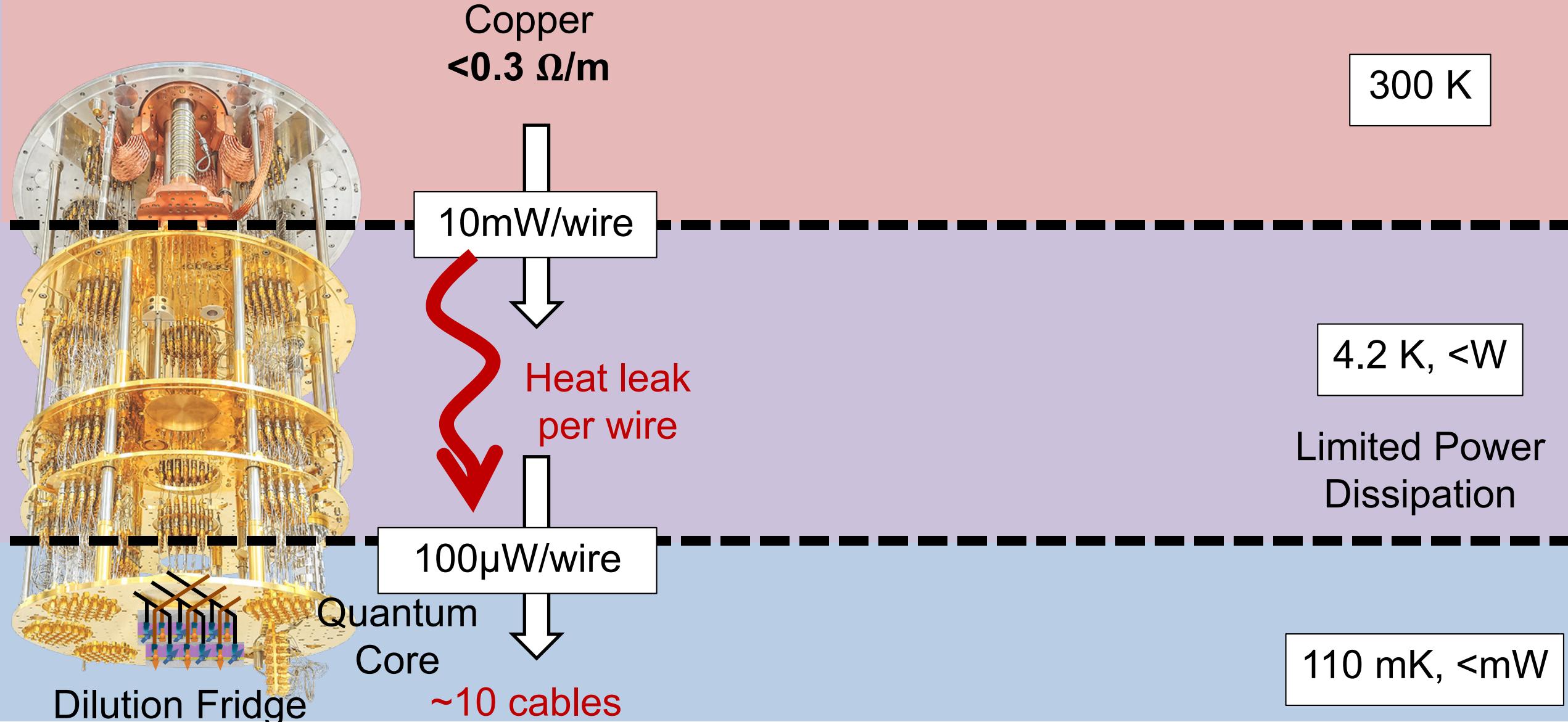
4.2 K, <W

Limited Power
Dissipation

110 mK, <mW

19.2: A 110mK 295 μ W 28nm FDSOI CMOS Quantum Integrated Circuit
with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot

The need for interface electronics



19.2: A 110mK 295 μ W 28nm FDSOI CMOS Quantum Integrated Circuit
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The need for interface electronics



Copper
 $<0.3 \Omega/m$

Manganin
 $35 \Omega/m$

10mW/wire

10 μ W/wire

Heat leak
per wire

100 μ W/wire

100nW/wire

Quantum
Core

~10 cables

~10 000 cables

300 K

Trade-off:
Low attenuation
High Bandwidth



Number of lines
Available Power

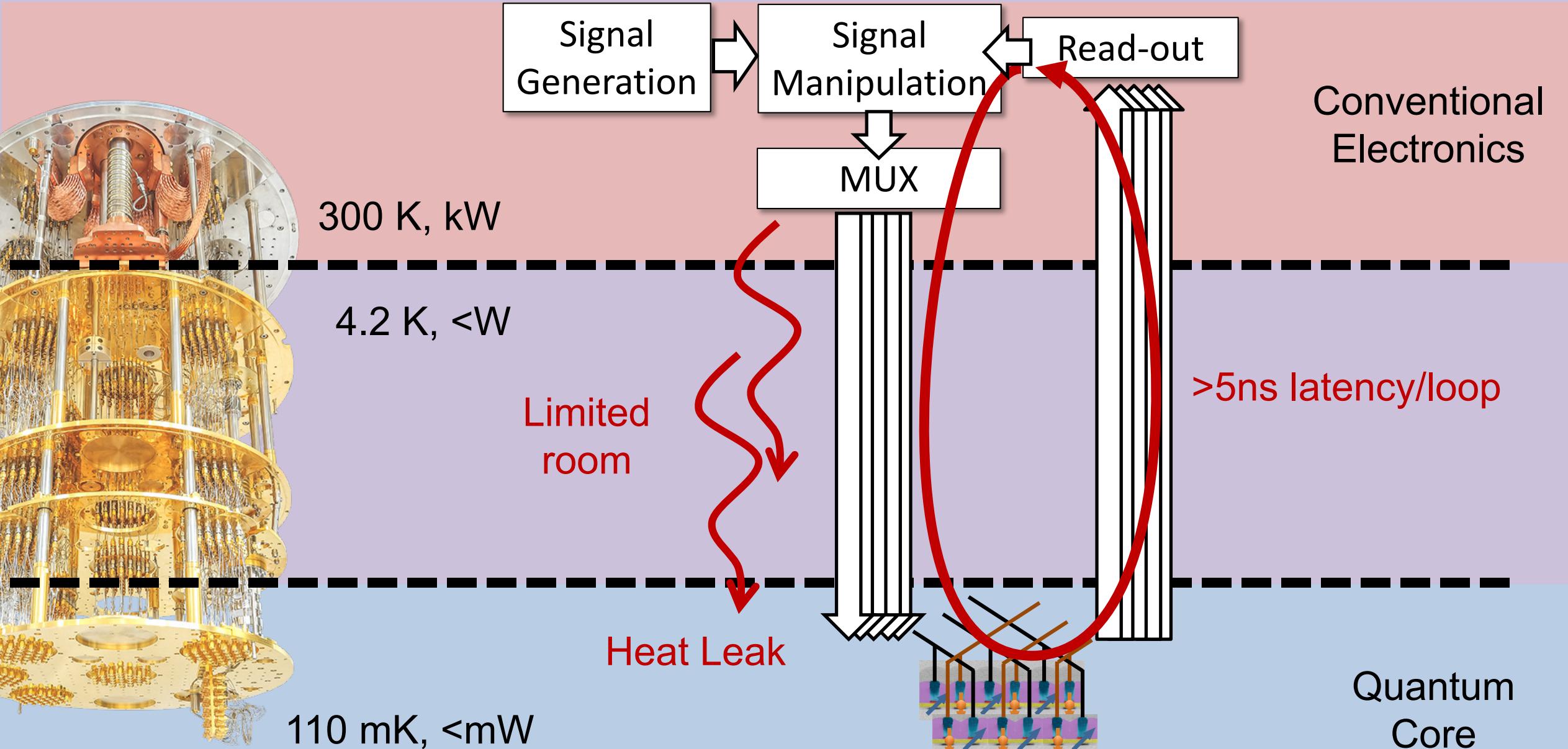
4.2 K, <W

Limited Power
Dissipation

110 mK, <mW

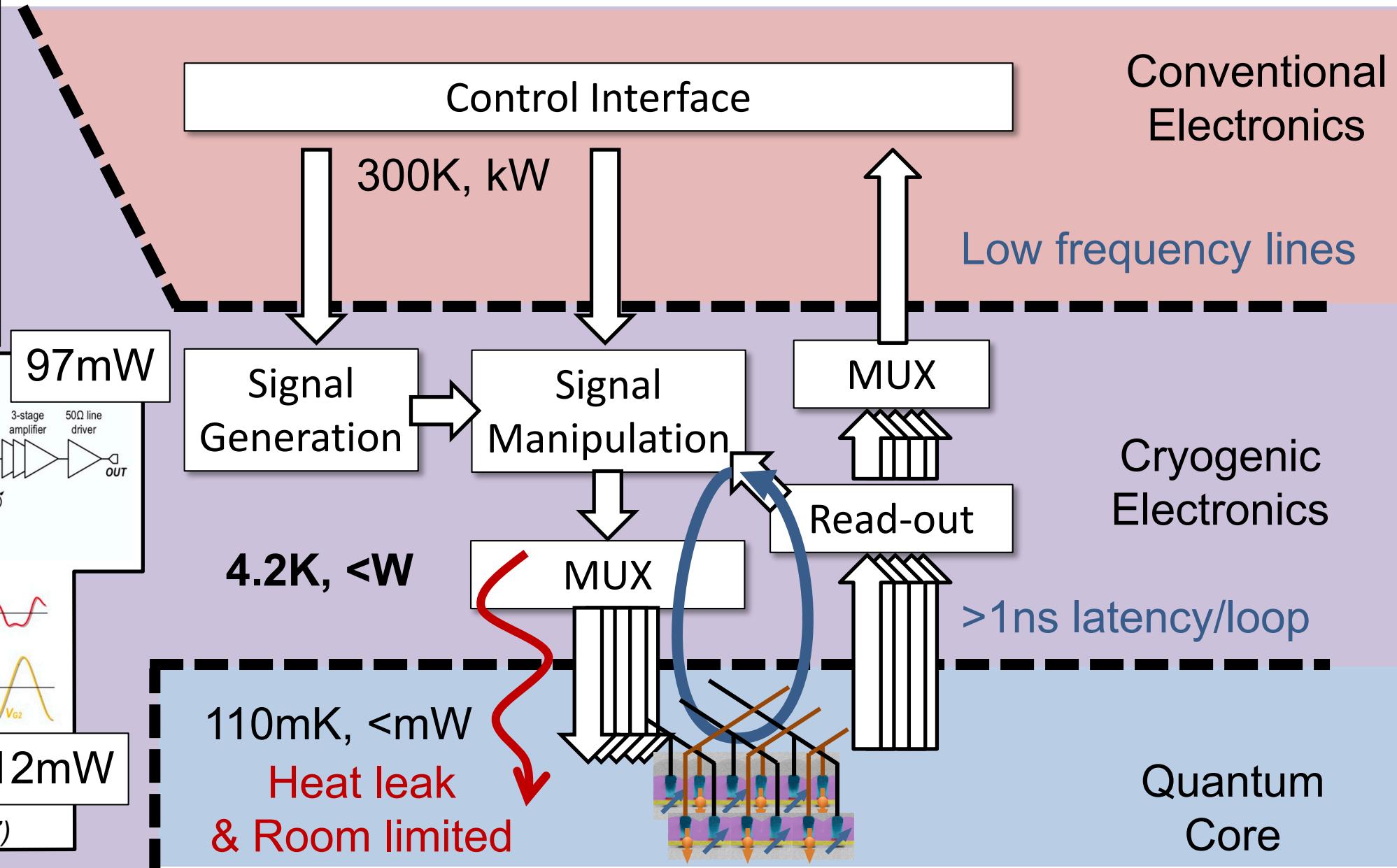
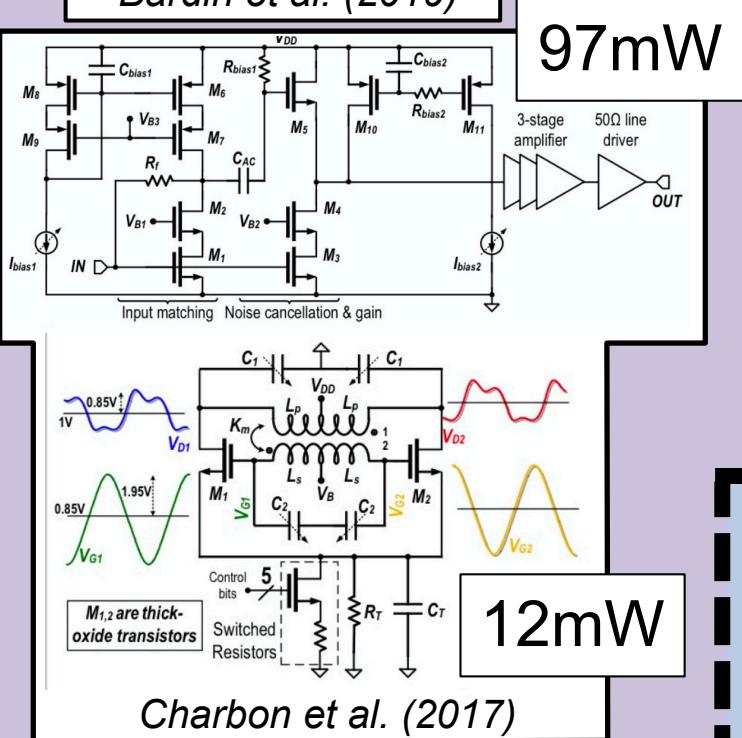
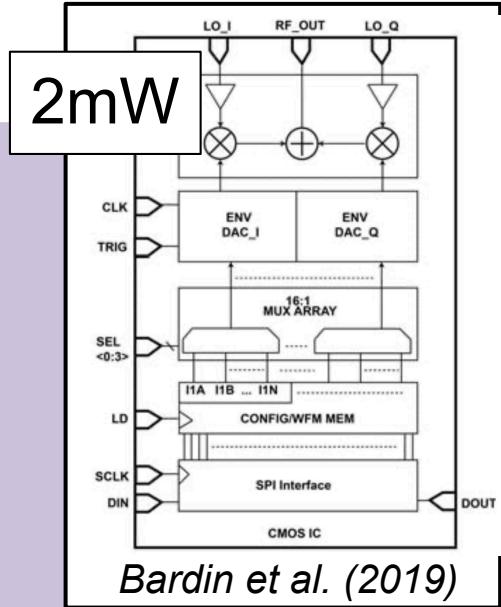
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The need for interface electronics



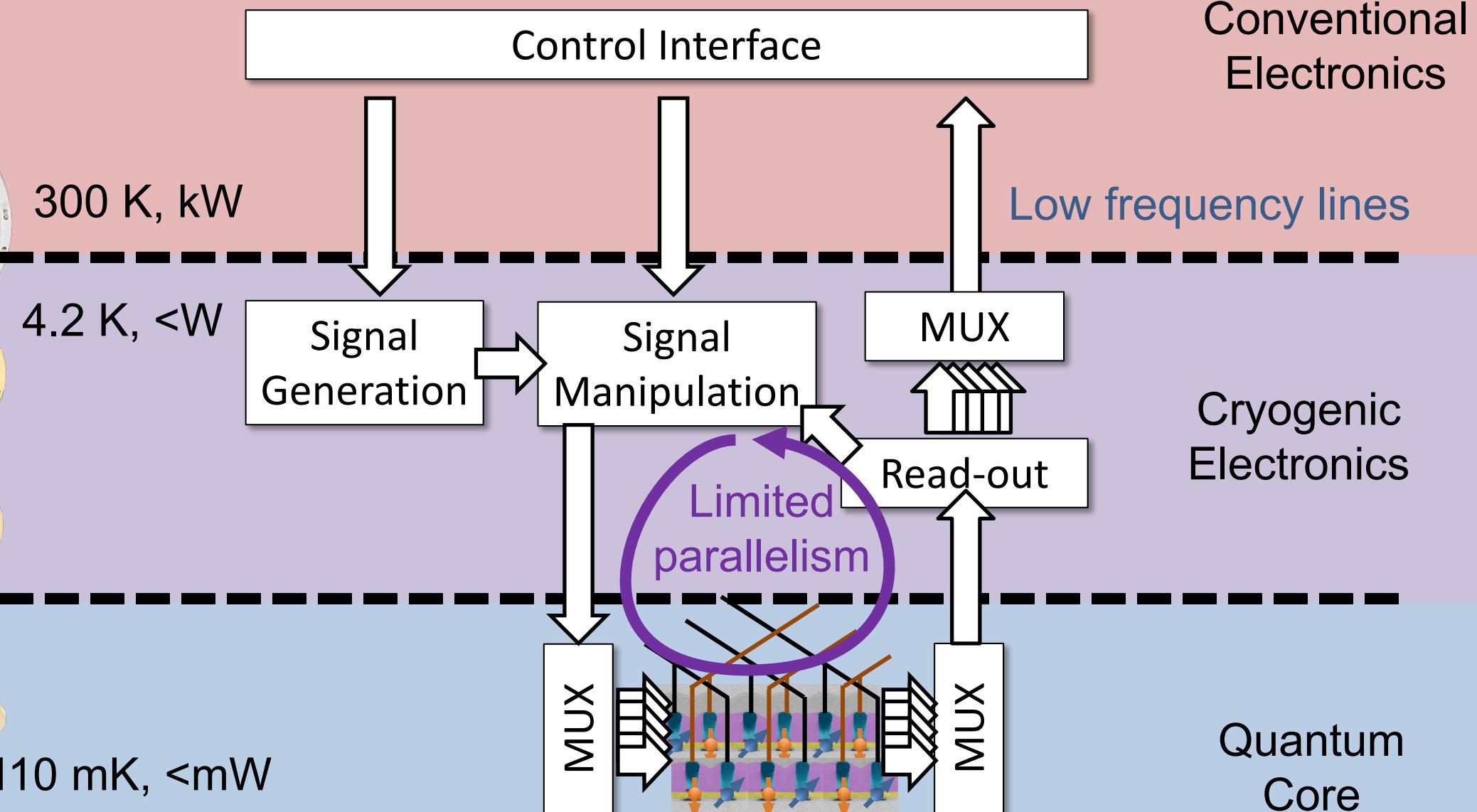
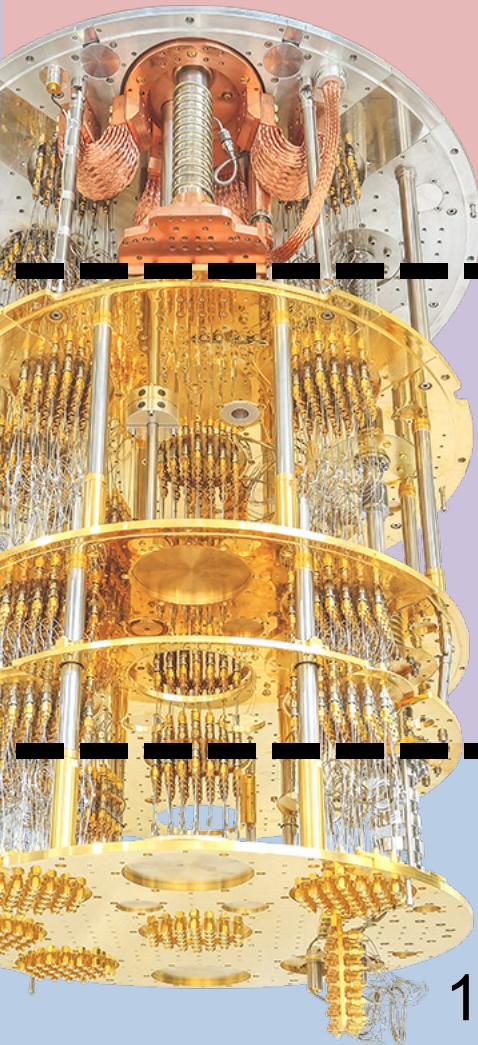
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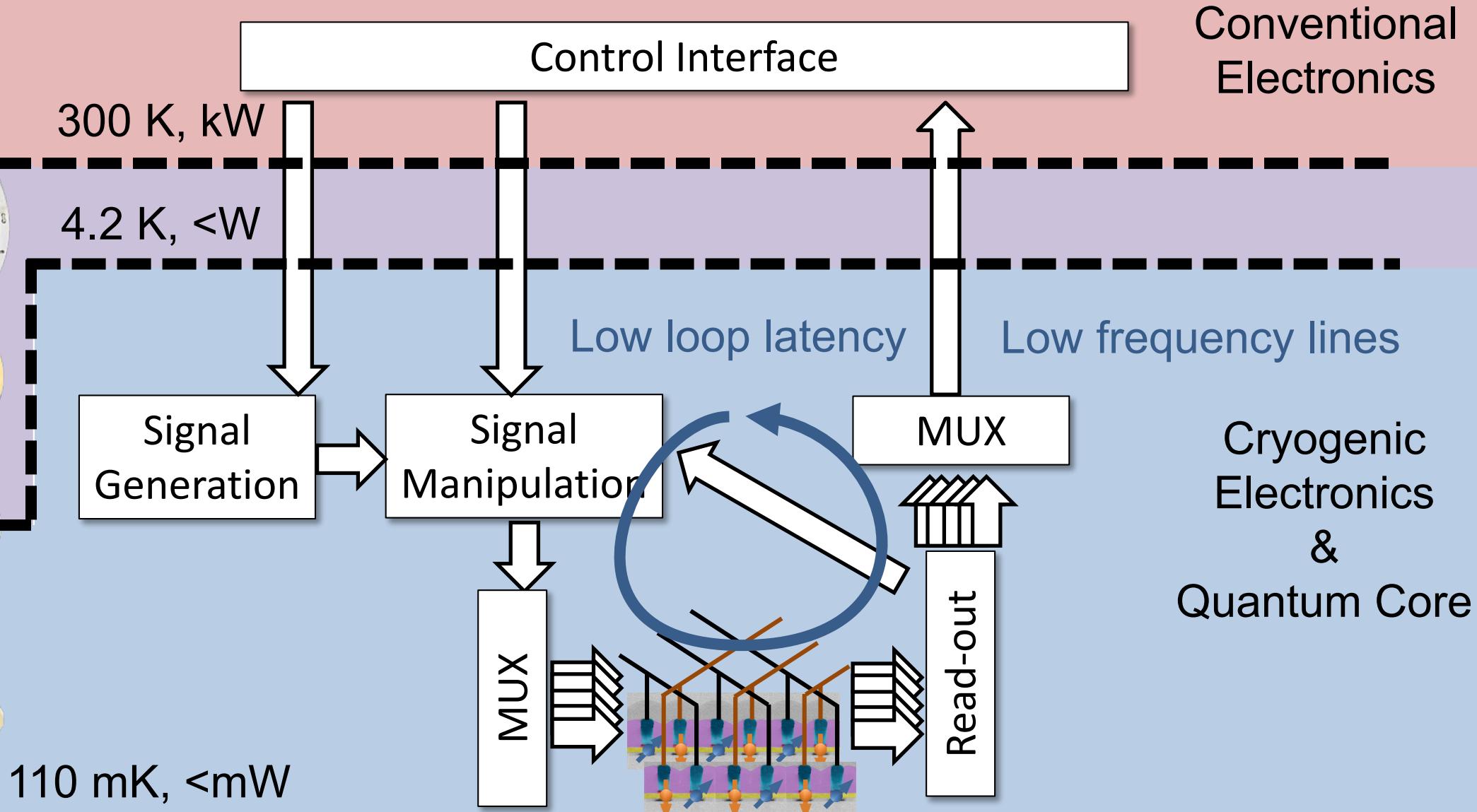
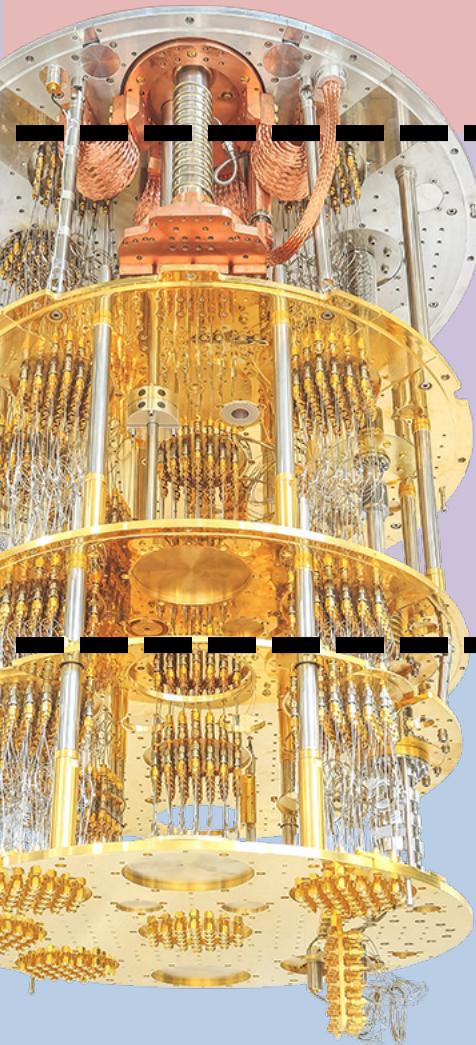
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The need for interface electronics



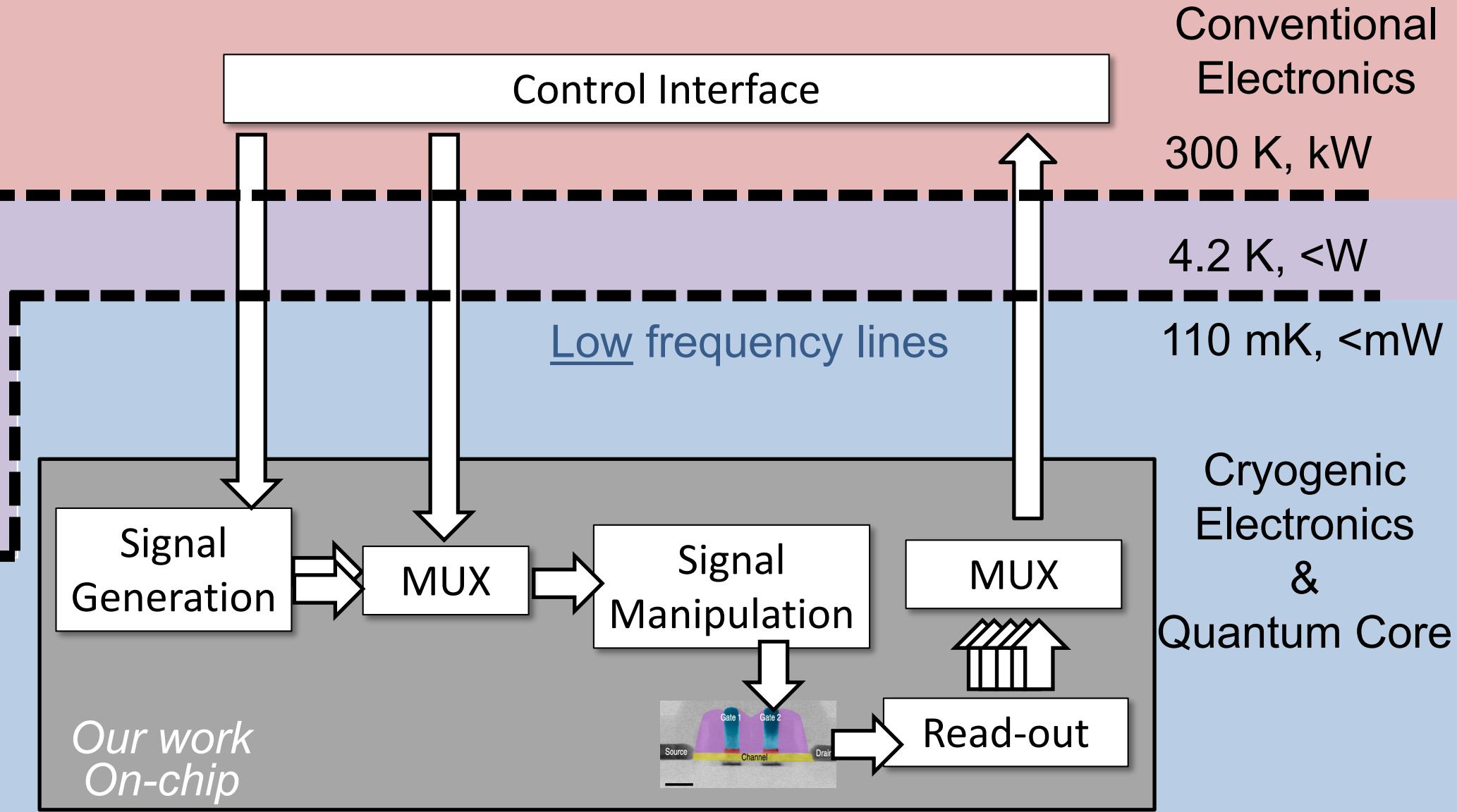
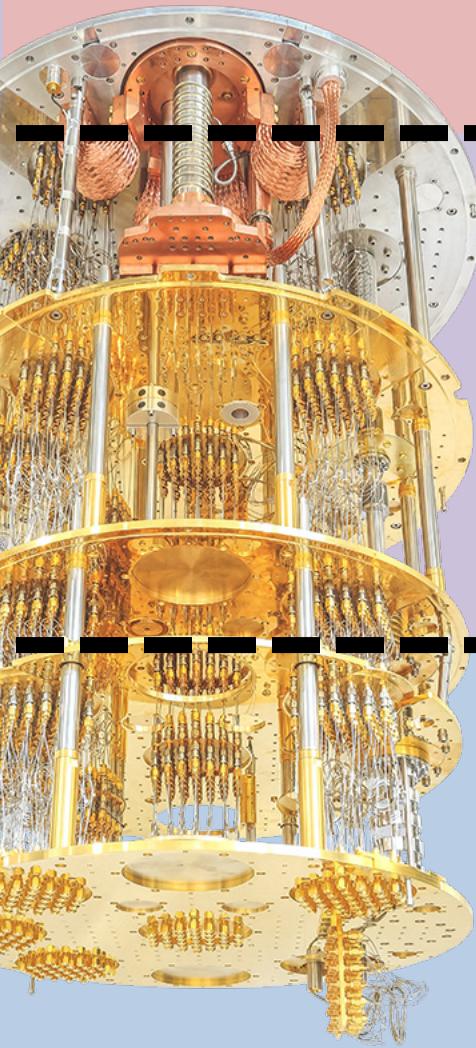
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The need for interface electronics



19.2: A 110mK 295 μ W 28nm FDSOI CMOS Quantum Integrated Circuit
with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot

The need for interface electronics



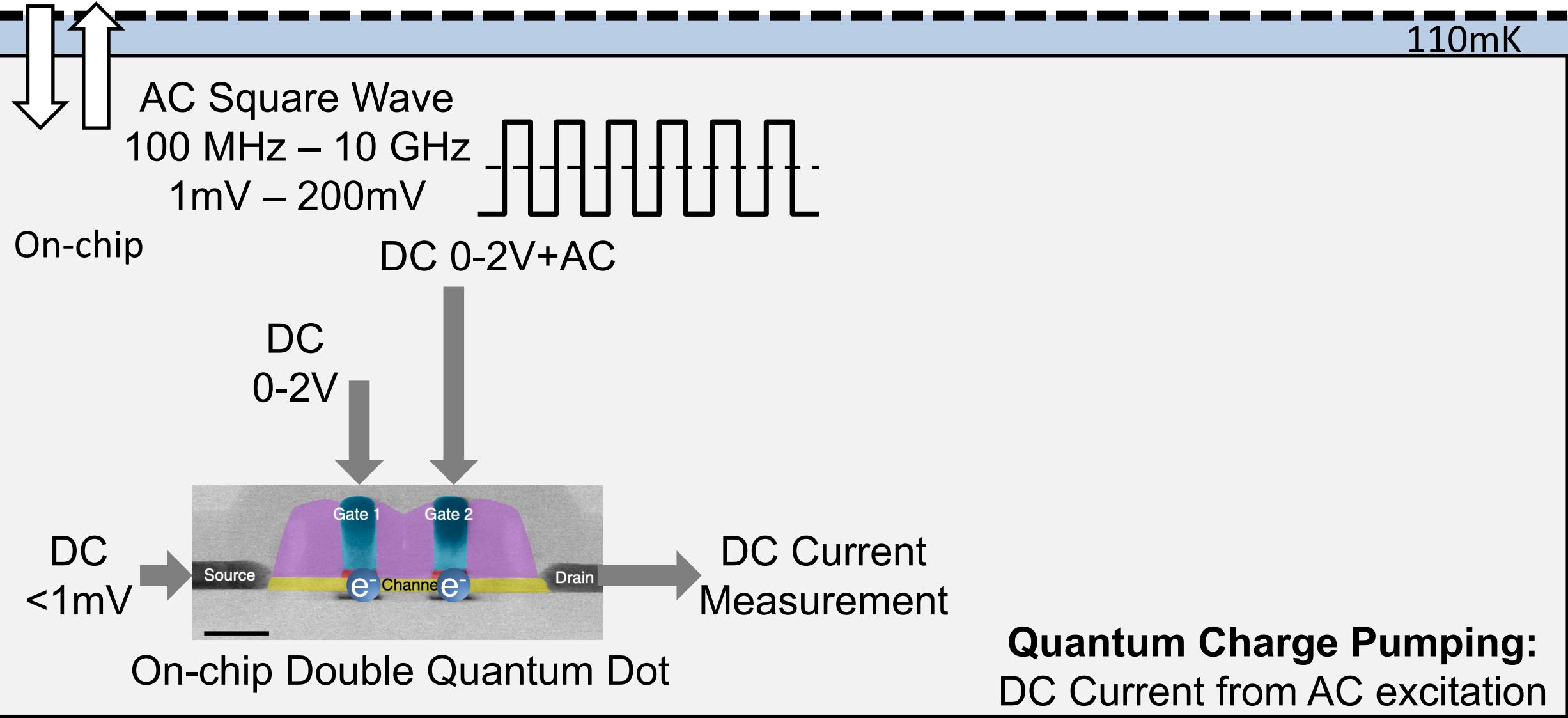
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Quantum Integrated Circuit (QIC)

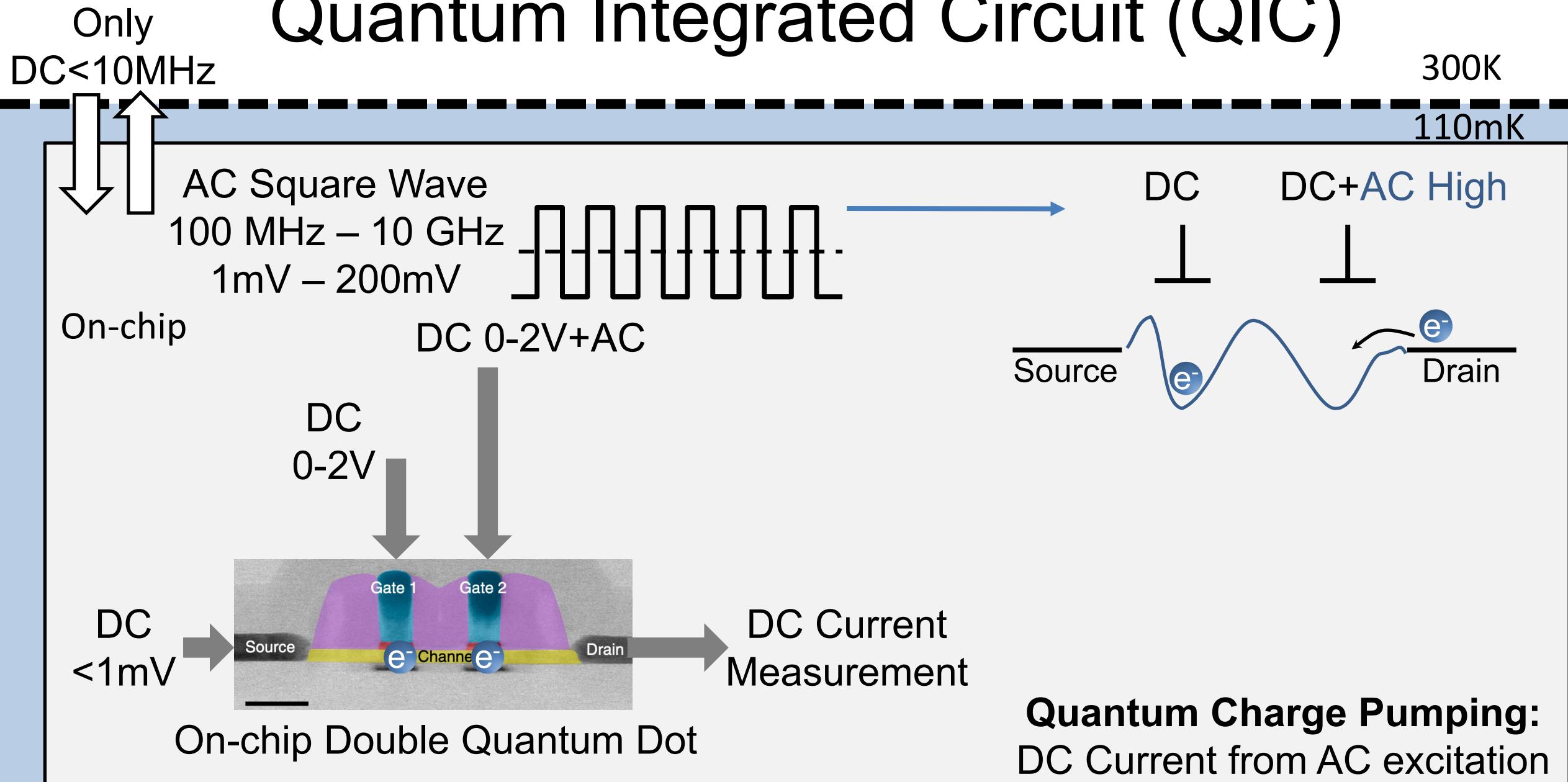
Only
DC<10MHz

300K

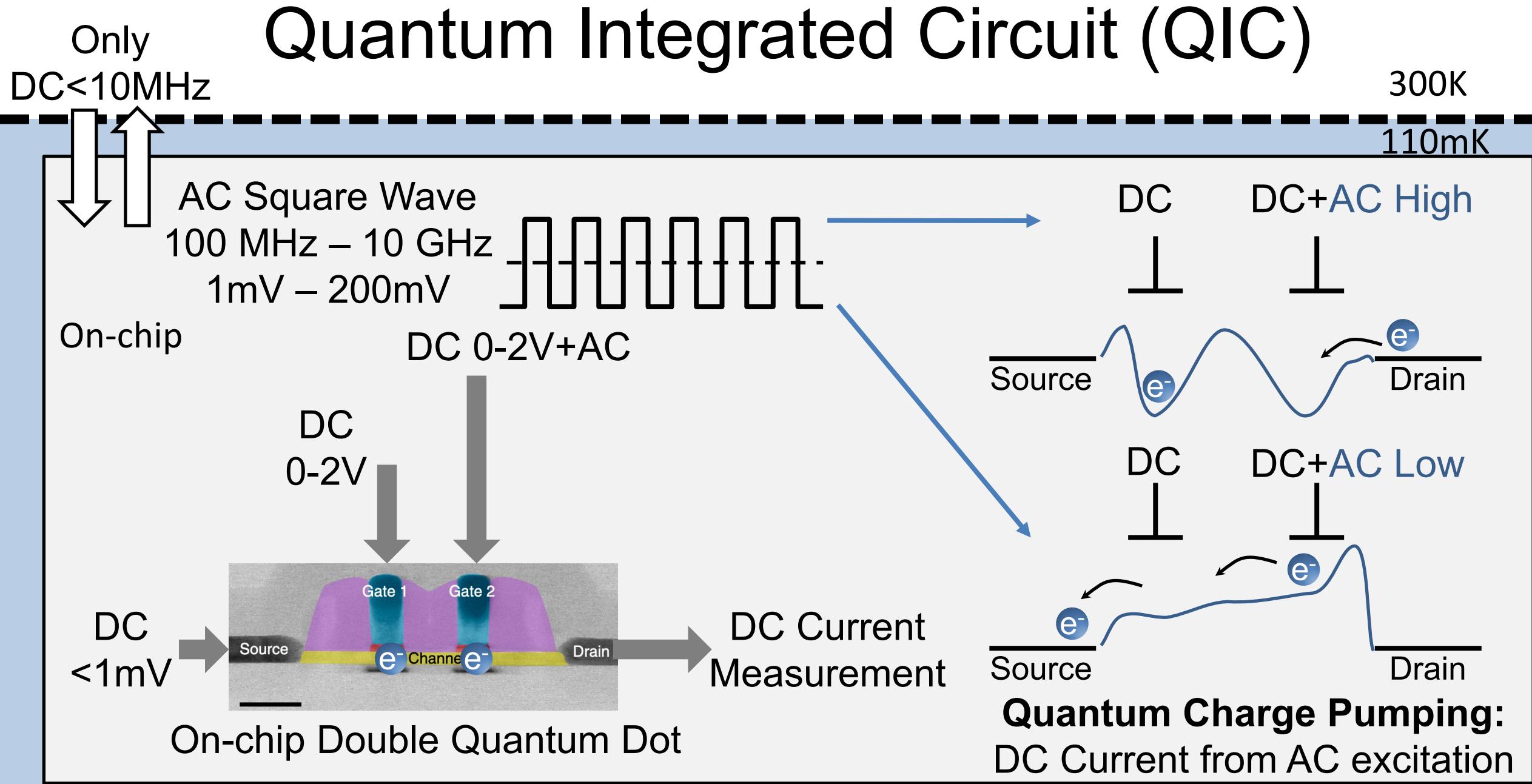
110mK



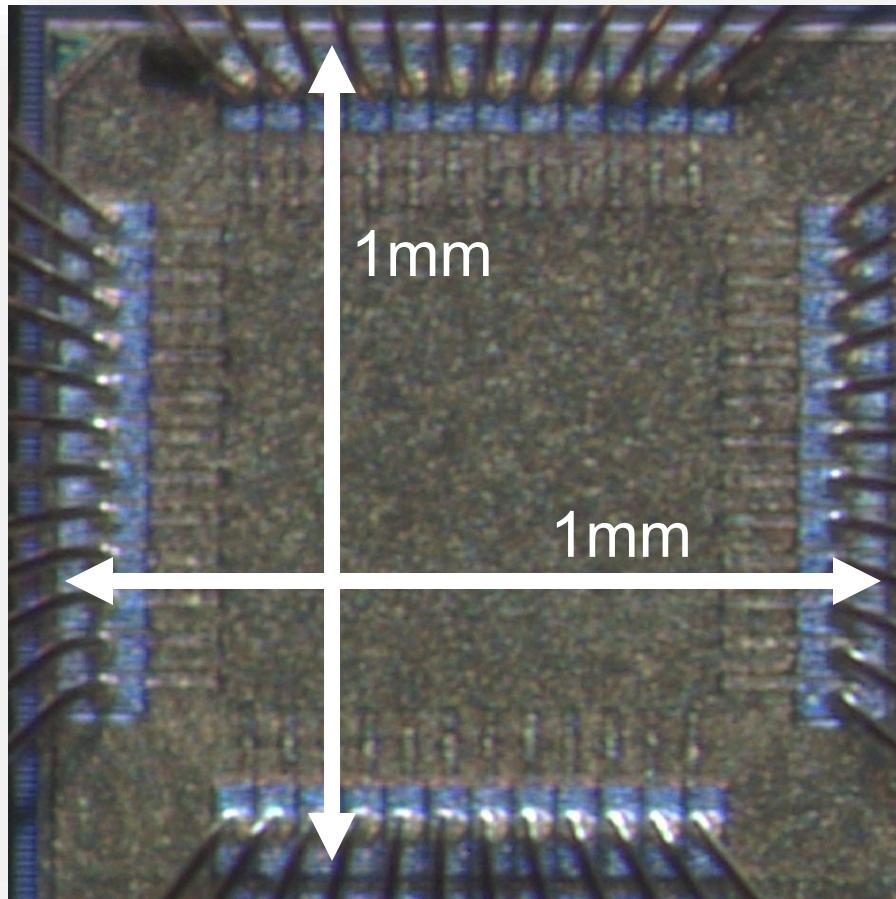
Quantum Integrated Circuit (QIC)



Quantum Integrated Circuit (QIC)



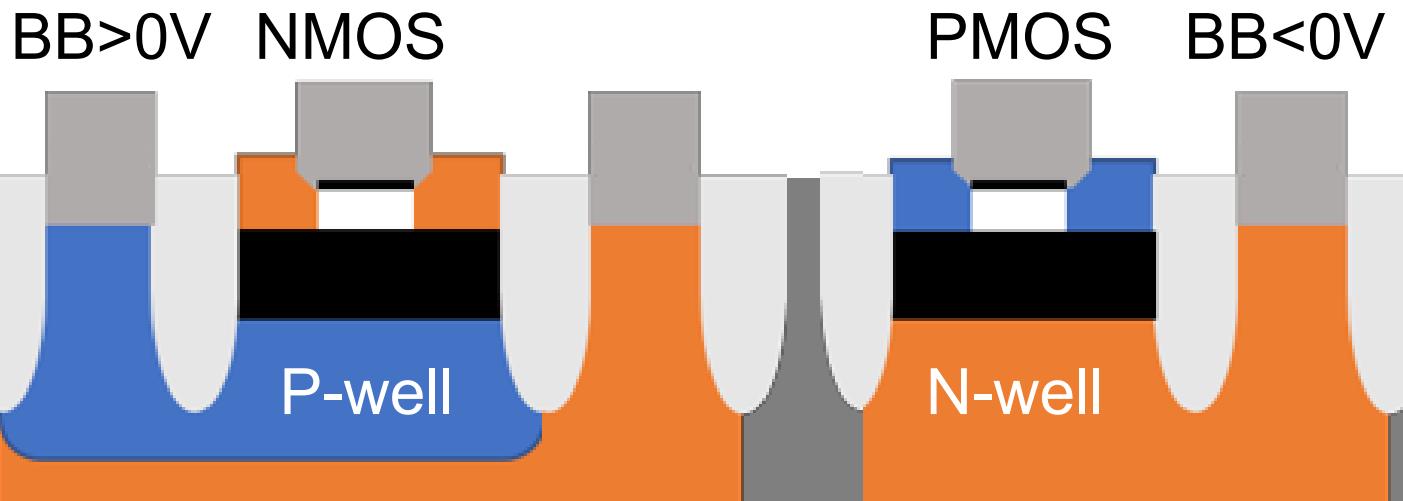
Quantum Integrated Circuit (QIC)



QIC chip micrograph

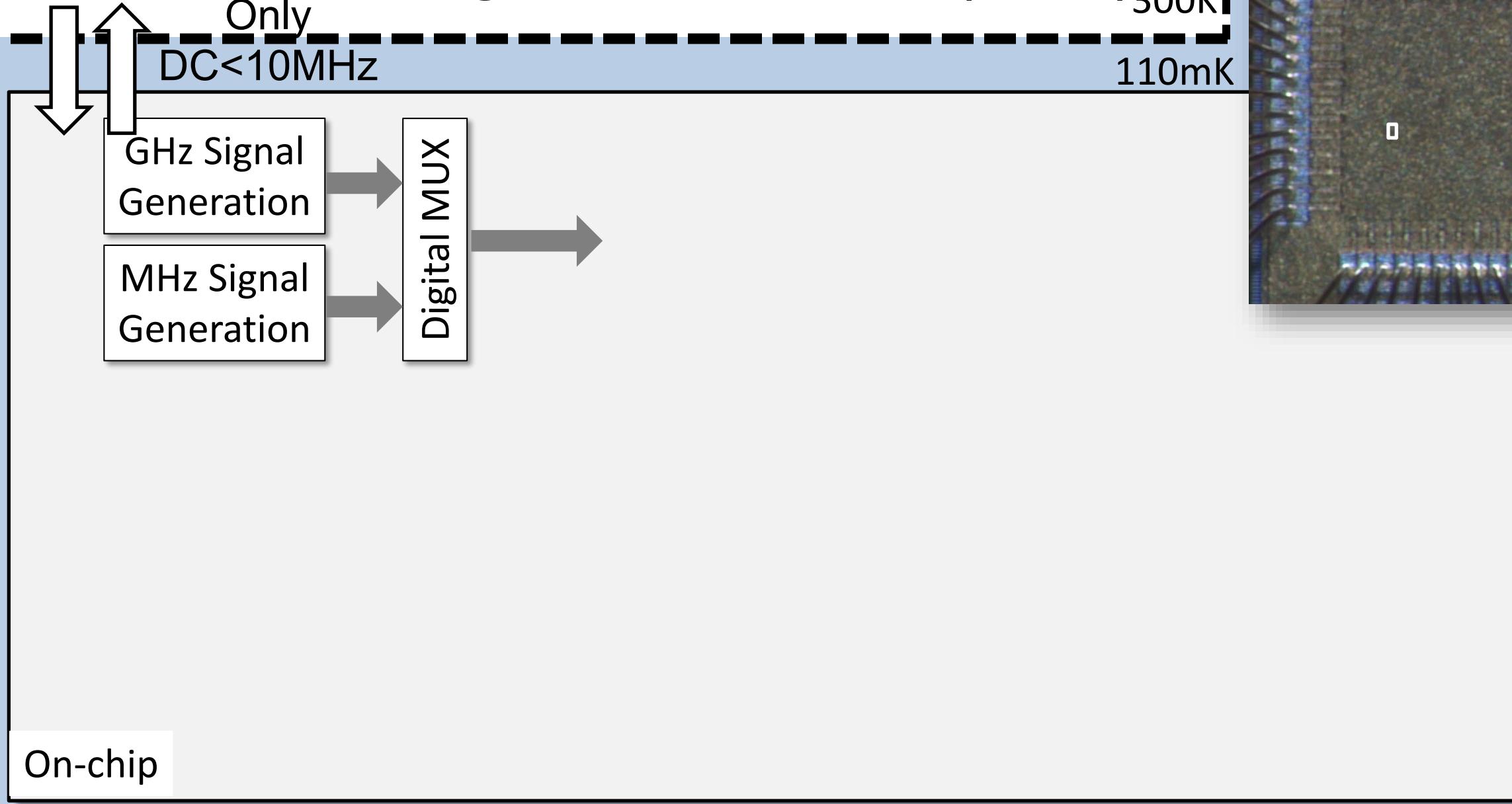
28nm Fully-Depleted Silicon-On-Insulator CMOS Technology

- **>10 GHz signals handling**
- Compatible with FD-SOI qubits
- Triple well structure for **back biasing**



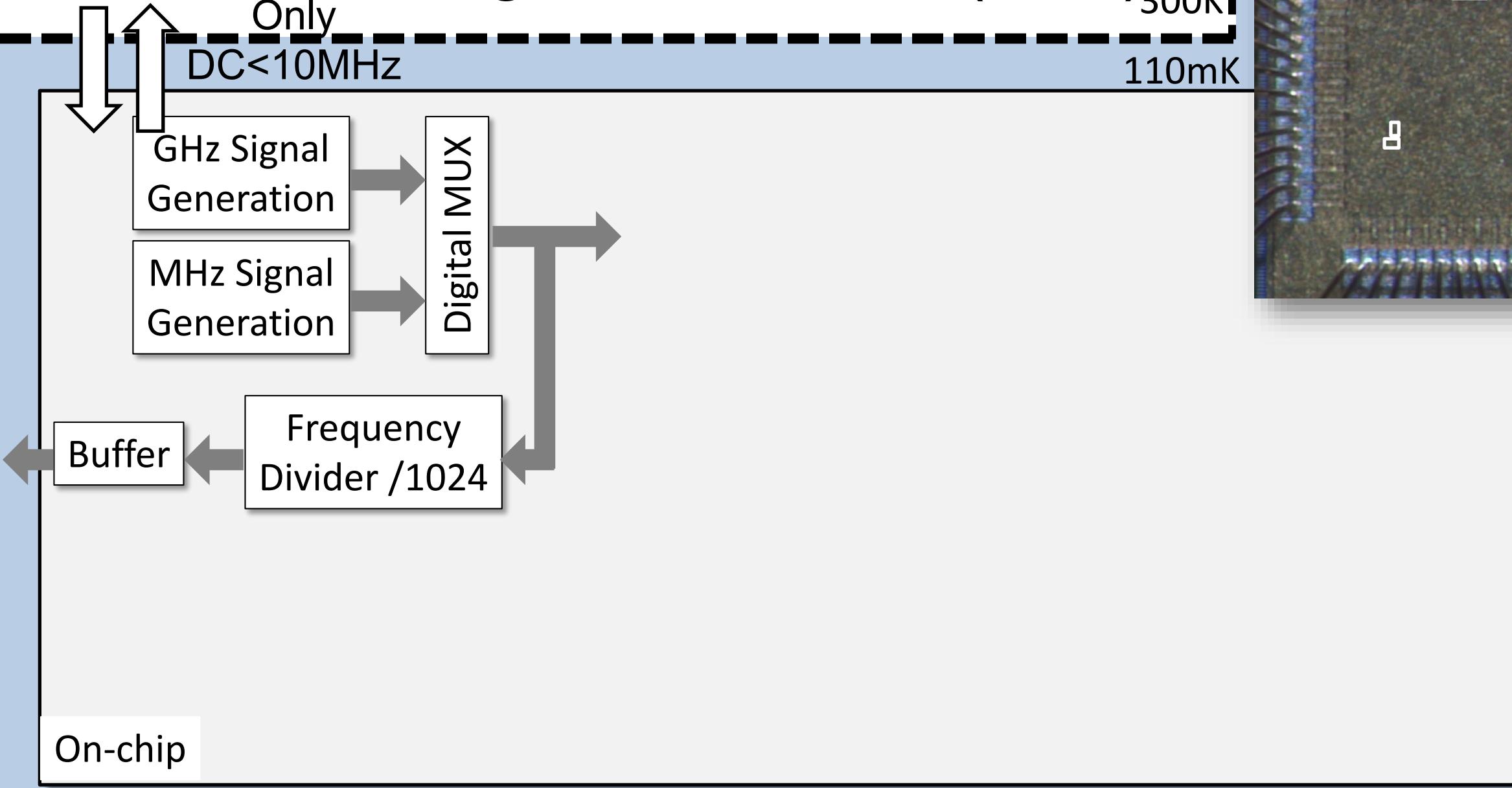
QIC extensively use back biasing
to compensate the increased VTH at low temperature

Quantum Integrated Circuit (QIC)

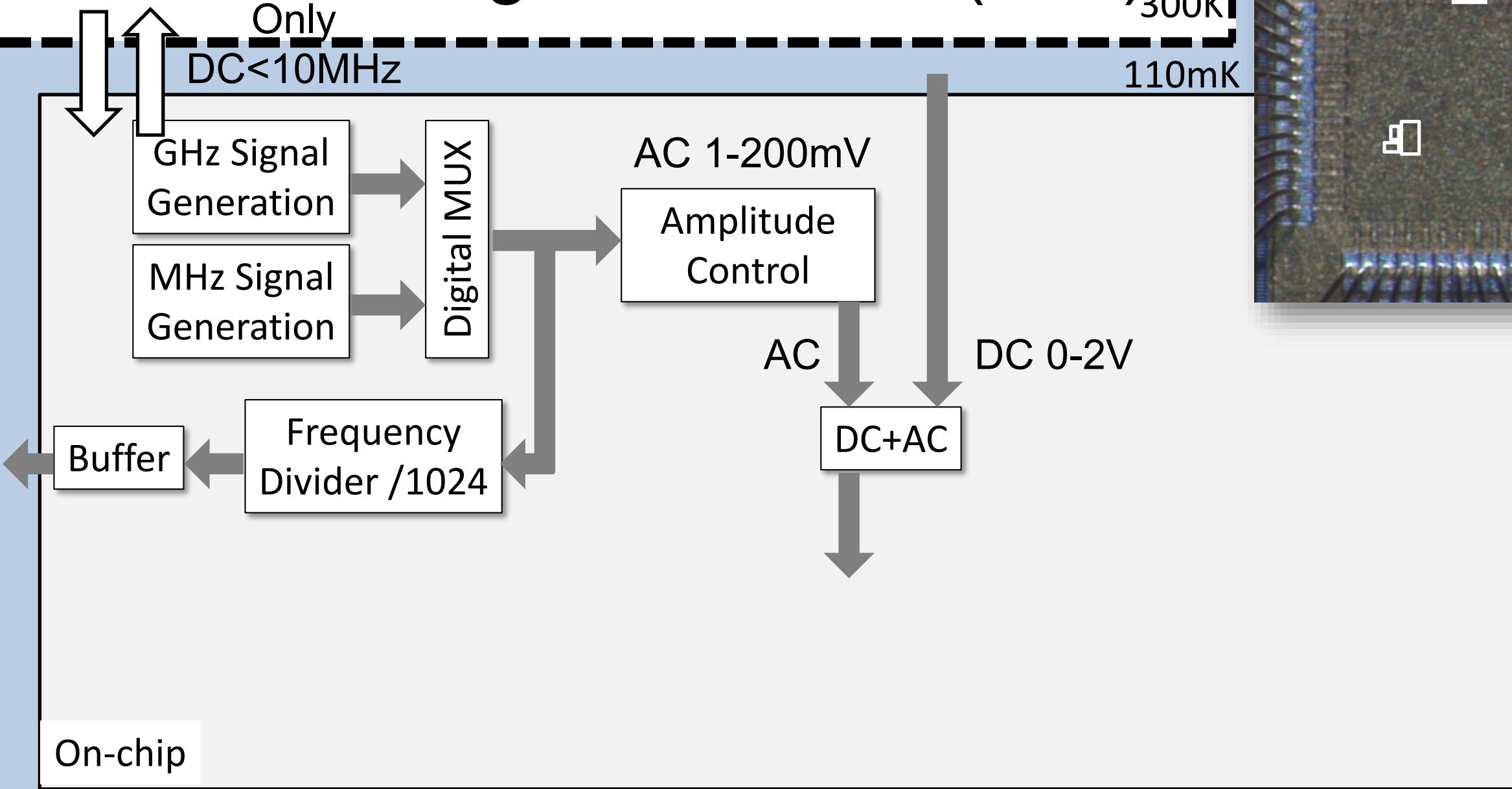


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Quantum Integrated Circuit (QIC)

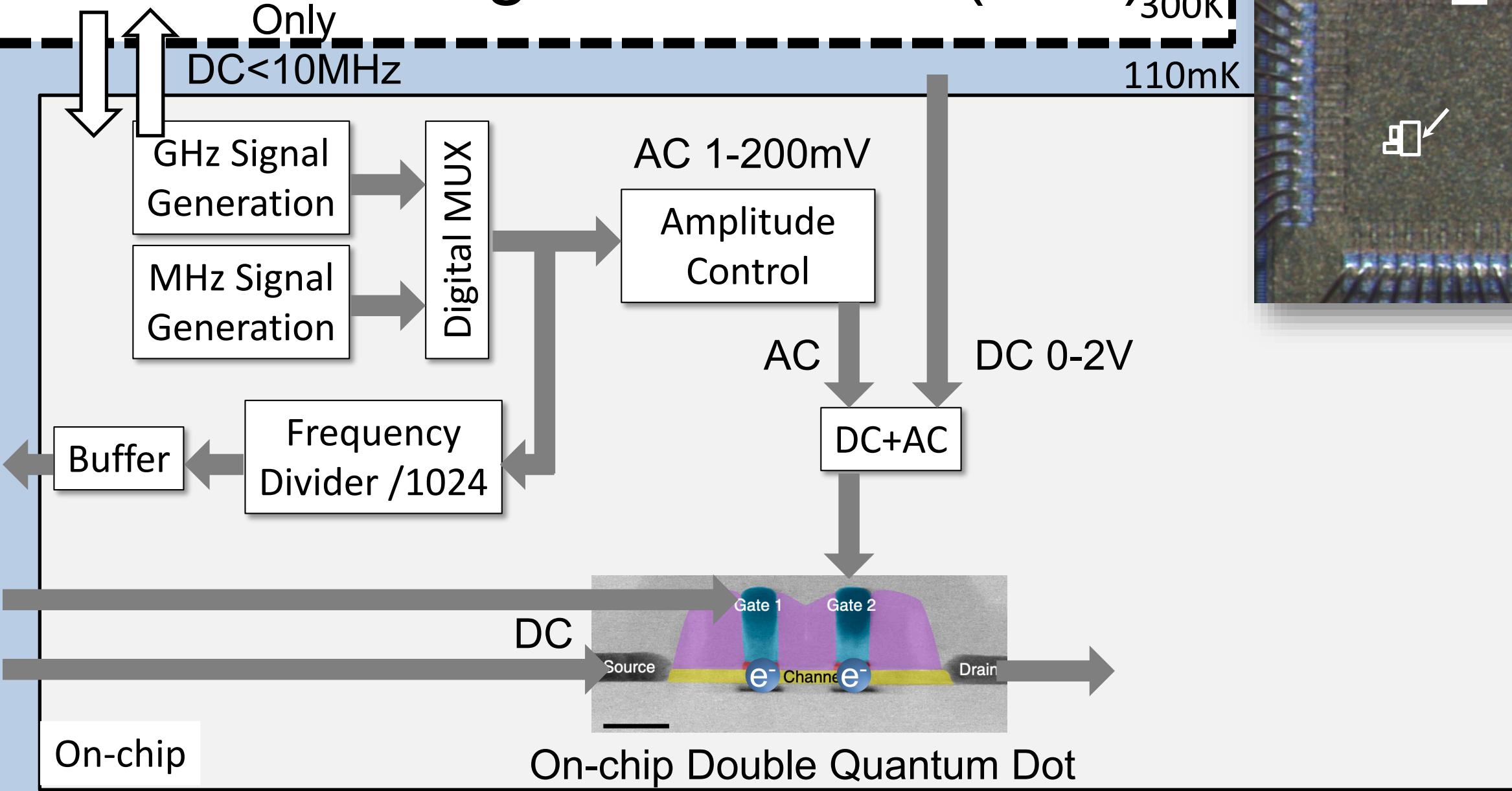


Quantum Integrated Circuit (QIC)



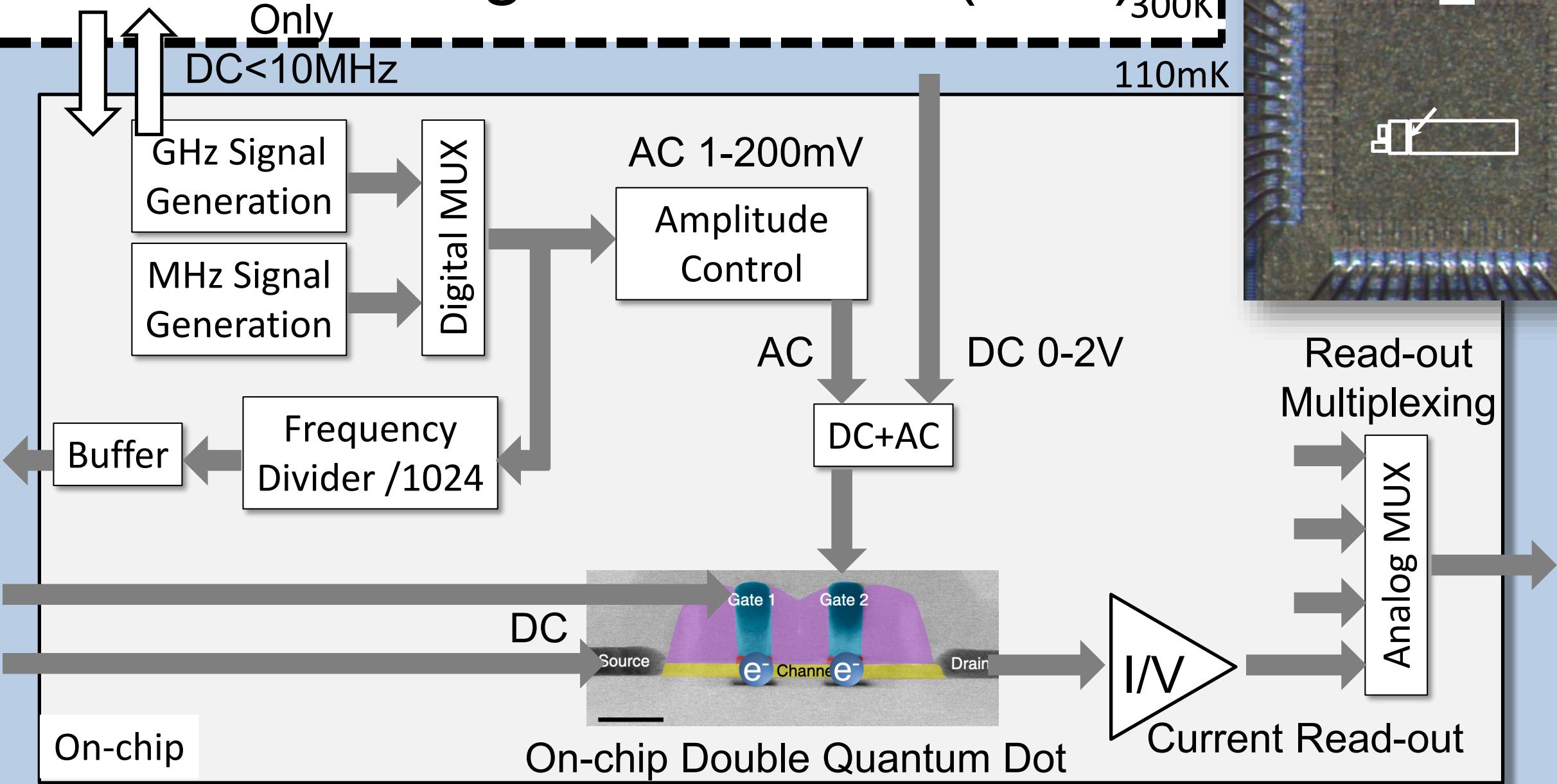
19.2: A 110mK 295 μ W 28nm FDSOI CMOS Quantum Integrated Circuit
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Quantum Integrated Circuit (QIC)



19.2: A 110mK 295 μ W 28nm FDSOI CMOS Quantum Integrated Circuit
with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot

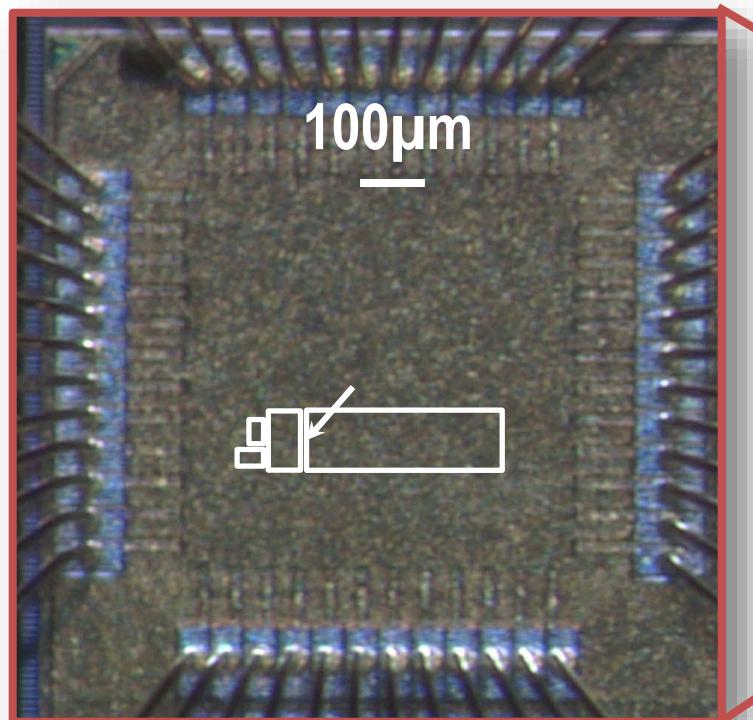
Quantum Integrated Circuit (QIC)



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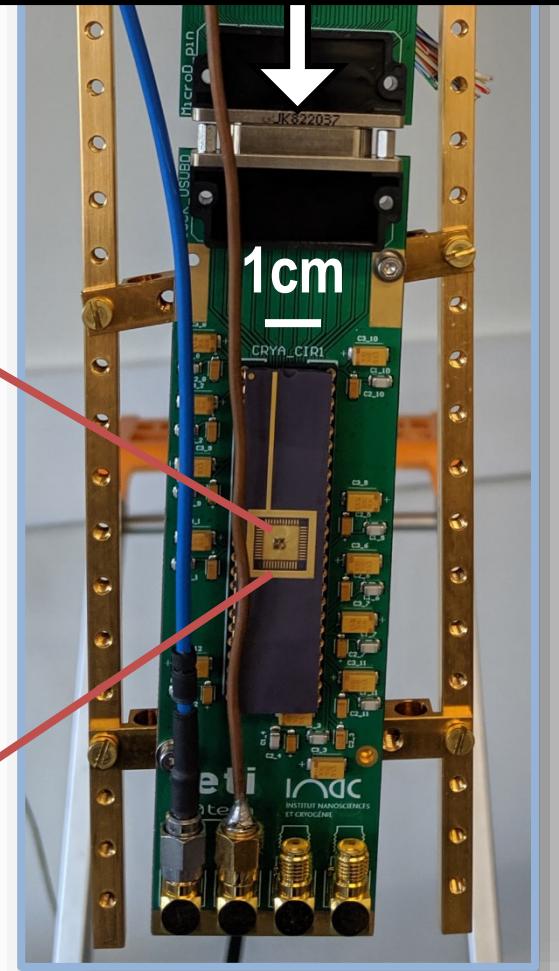
Experimental Setup

All measurements
At 110mK

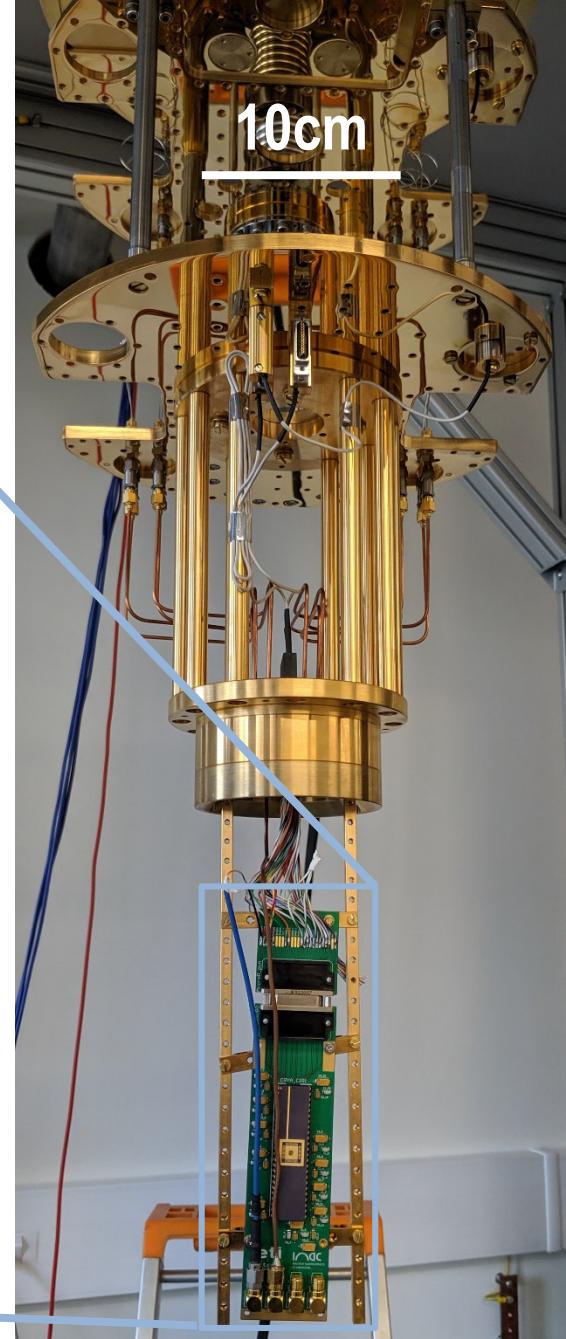


FD-SOI 28nm CMOS Technology

One <10 MHz line
20 DC: supplies and controls



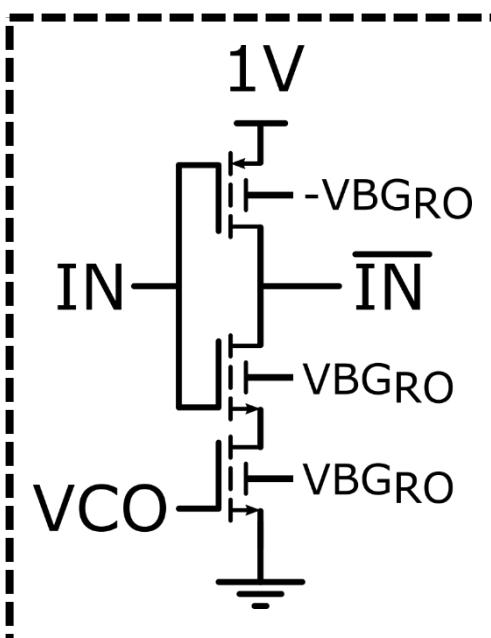
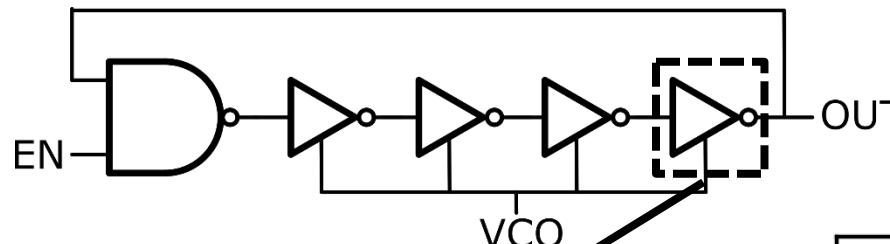
Packaged chip on the circuit board



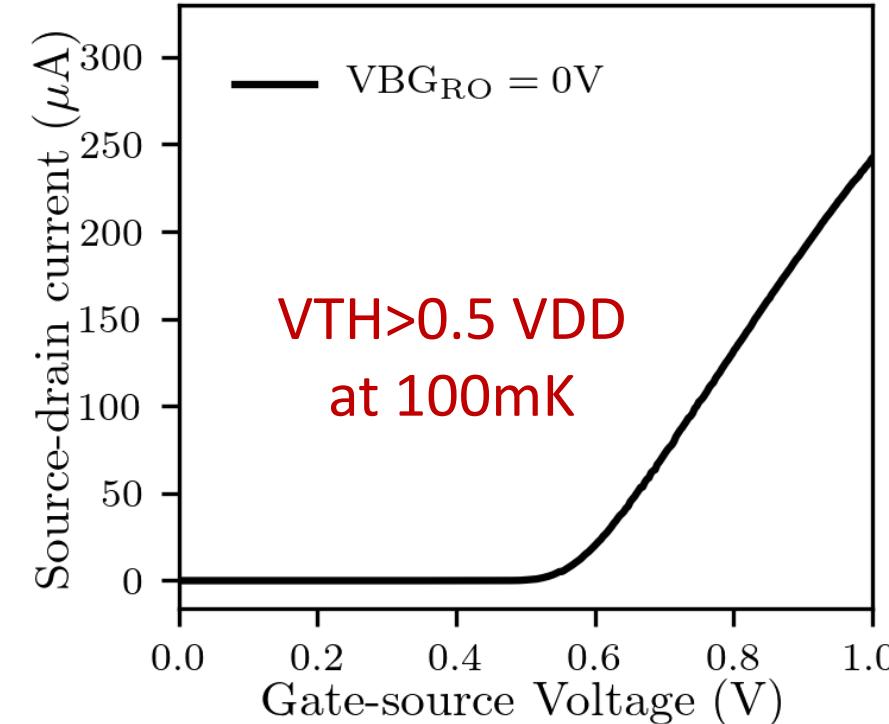
Mounting in the dilution fridge

GHz Signal Generation

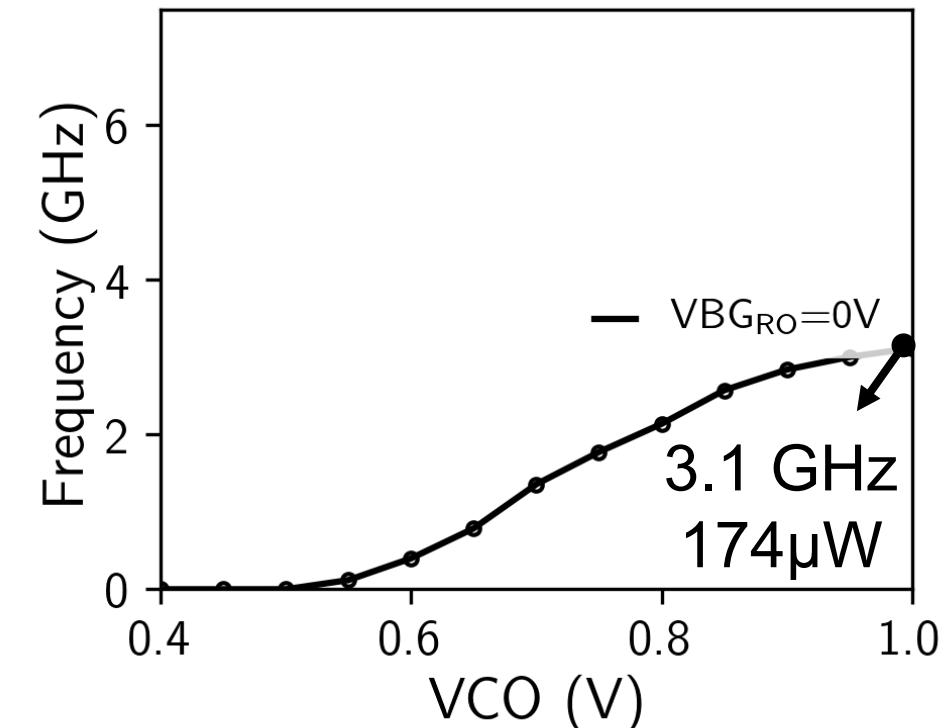
VCO Ring-Oscillator



L=28nm



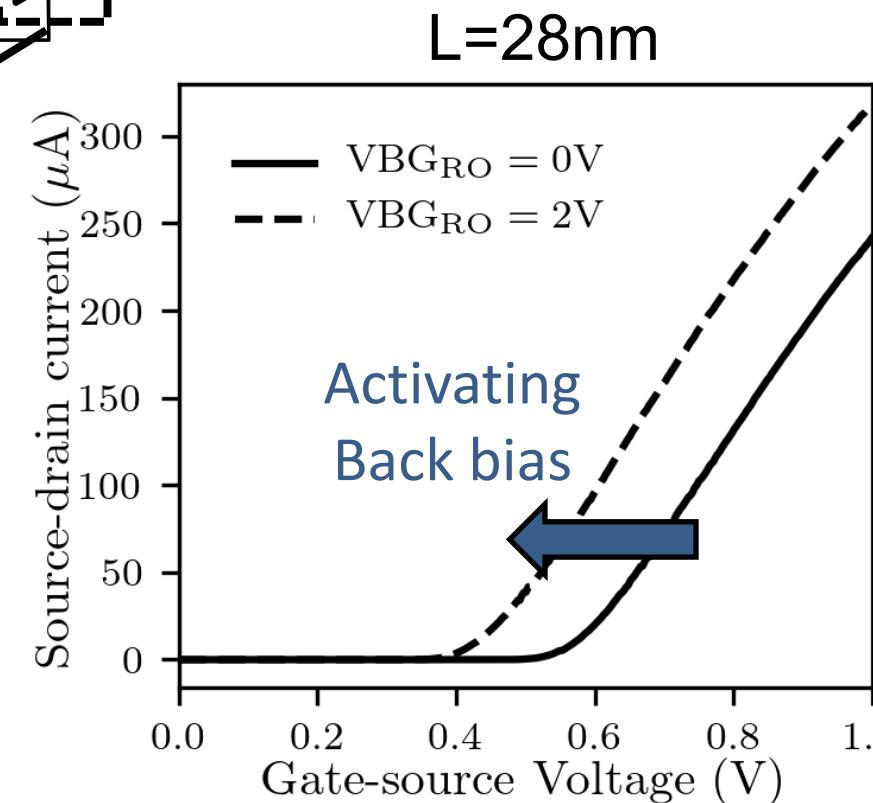
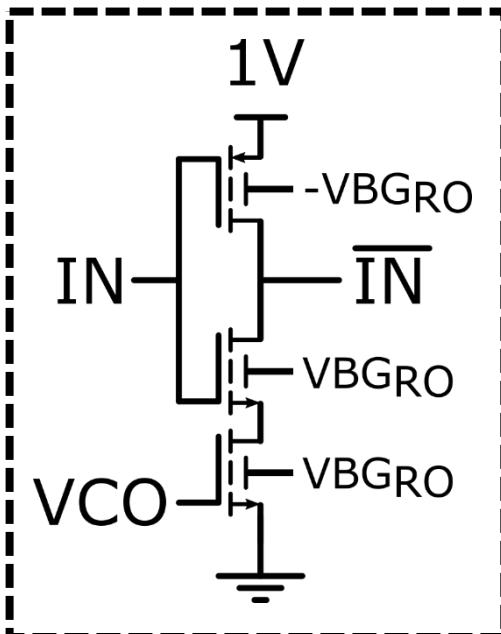
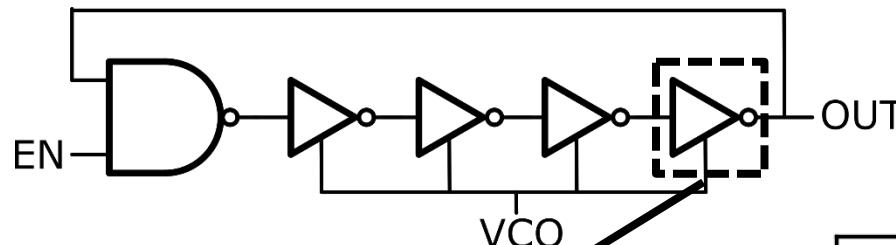
L=28nm



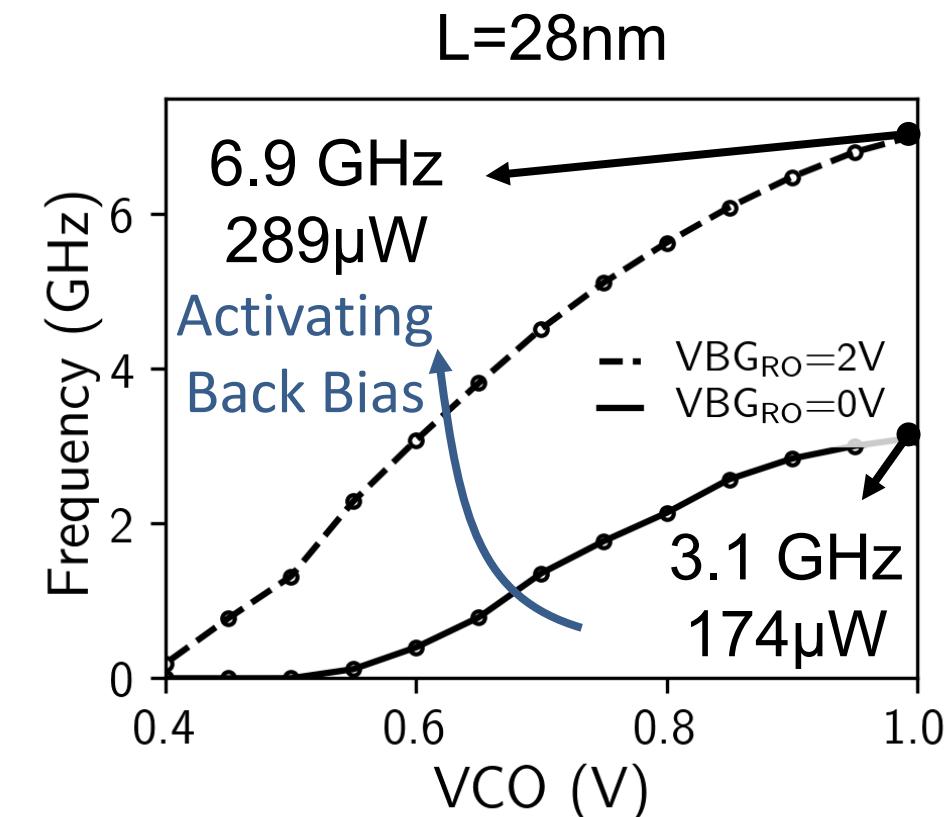
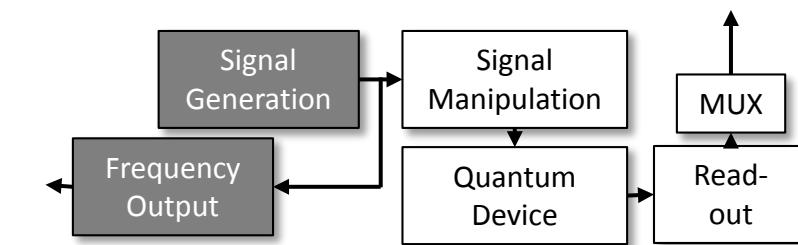
Increased V_{TH} at low temperature limit the oscillator speed

GHz Signal Generation

VCO Ring-Oscillator



Back-gate compensates increased
VTH at low temperature



Forward Back-Gating increases
maximal frequency

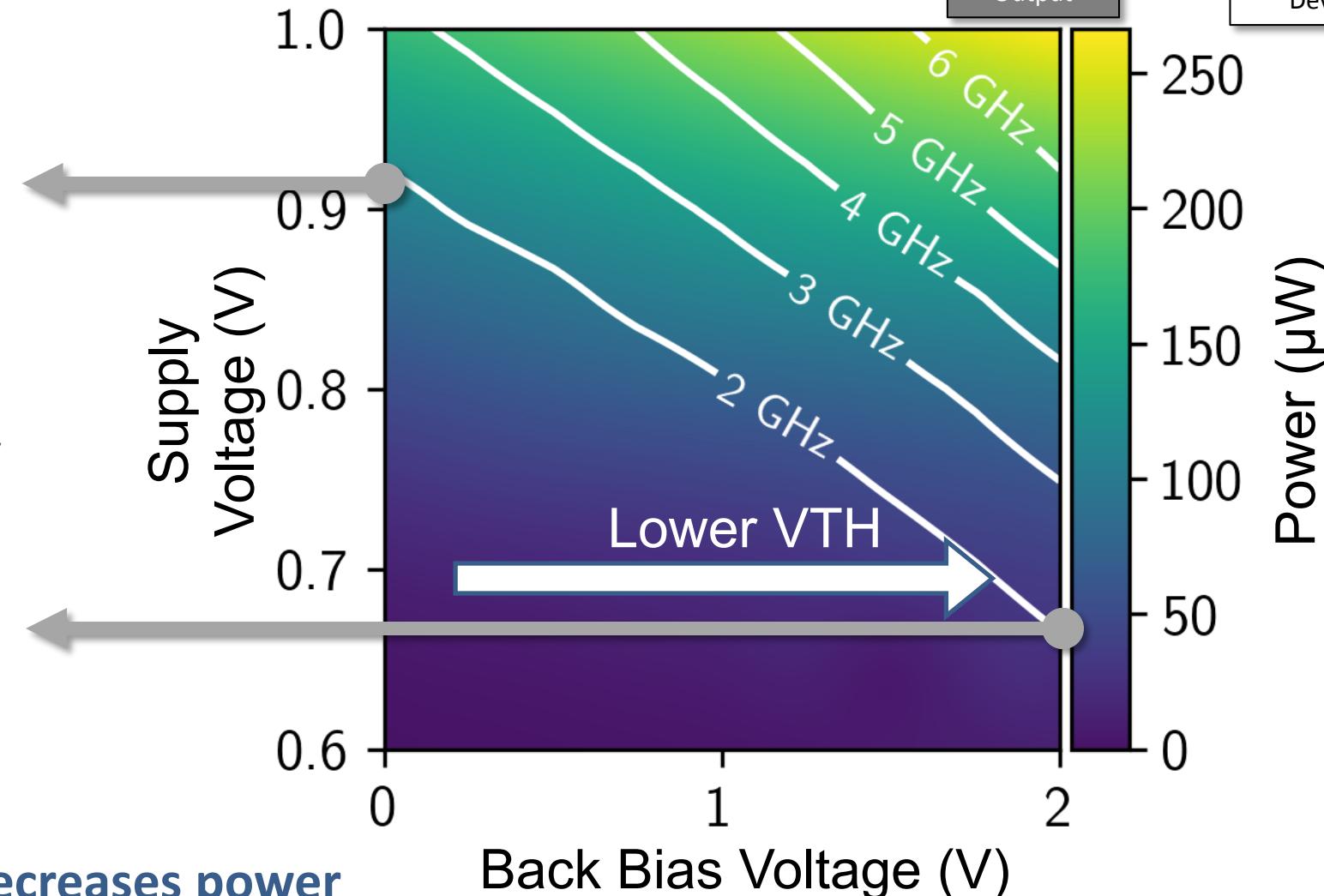
GHz Signal Generation

2GHz for $120\mu\text{W}$
no back-bias

Activating
Back bias
-78%
power

2GHz for $27 \mu\text{W}$
with back-bias

Forward back-gating decreases power
for same frequency



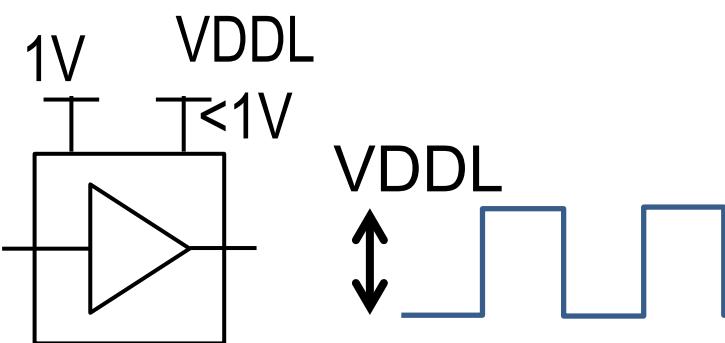
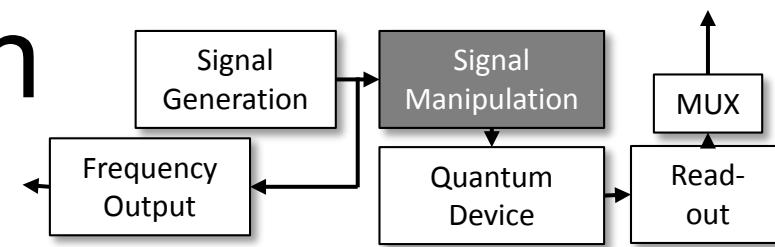
19.2: A 110mK 295 μW 28nm FDSOI CMOS Quantum Integrated Circuit
with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot

State-of-the-art Comparison

	Charbon et al. (2017)	Bohuslavskyi et al. (2018)	Our work	
Type	LC	Ring Oscillator	Low Power	High Perf
Technology	Bulk 40nm	FDSOI 28nm	FDSOI 28nm	
Power (μW)	7,000	119	27	268
Frequency (GHz)	6.7	0.38	2	6.9
Temperature (K)	4.2	4.2	0.11	
Energy Efficiency ($\mu\text{W}/\text{GHz}$)	1,045	313	13.5	38.8

Back bias allows low power mode or high performance mode

Signal Manipulation



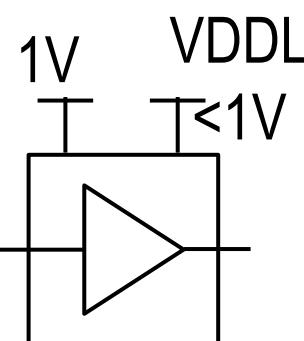
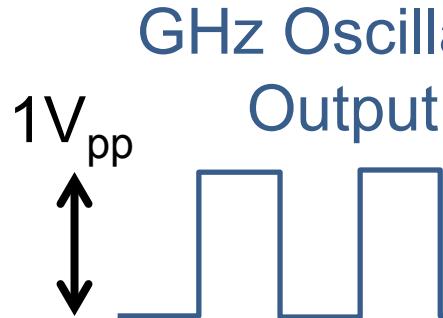
Level Shifter
Fine Amplitude
Tuning

Back-gate Voltage	Bandwidth
1.1 V	0.53 GHz
1.53 V	1.22 GHz
1.76 V	2.8 GHz

Back bias increases analog bandwidth

Signal Manipulation

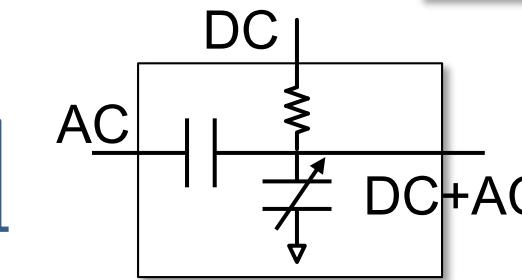
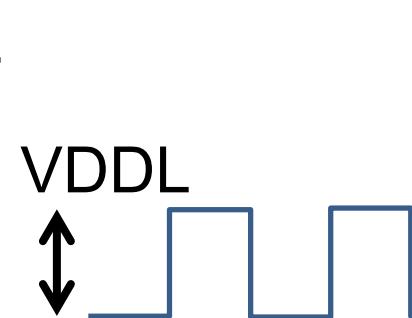
GHz Oscillator Output



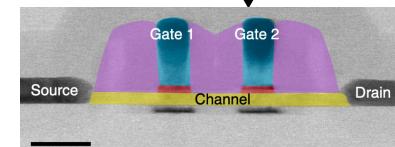
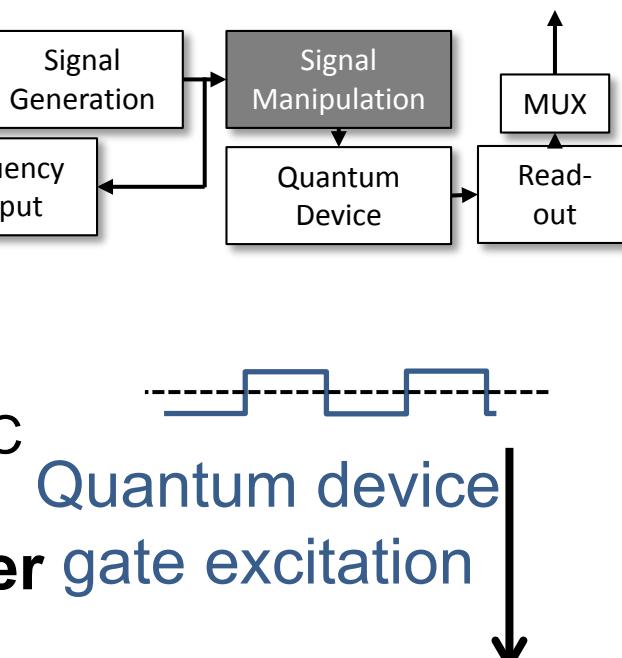
Level Shifter
Fine Amplitude Tuning

Back-gate Voltage	Bandwidth
1.1 V	0.53 GHz
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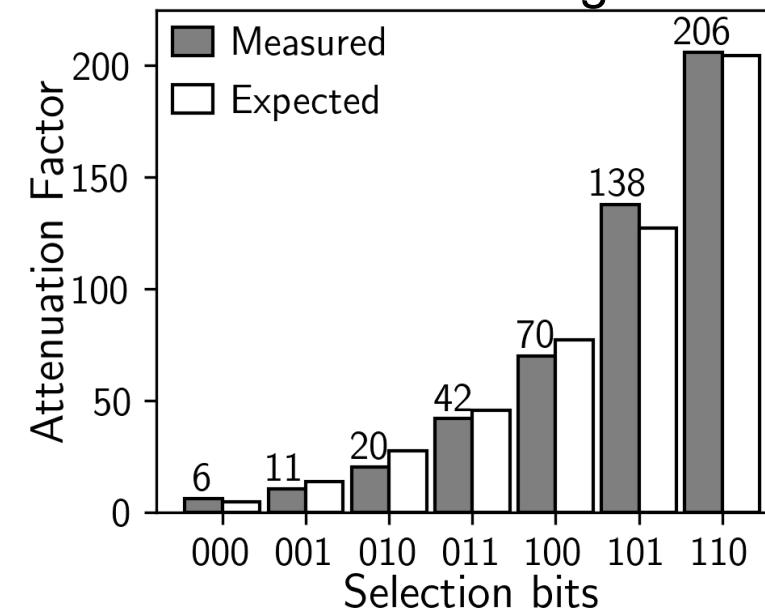
Back bias increases analog bandwidth



Capacitive Divider gate excitation
Coarse Amplitude Tuning

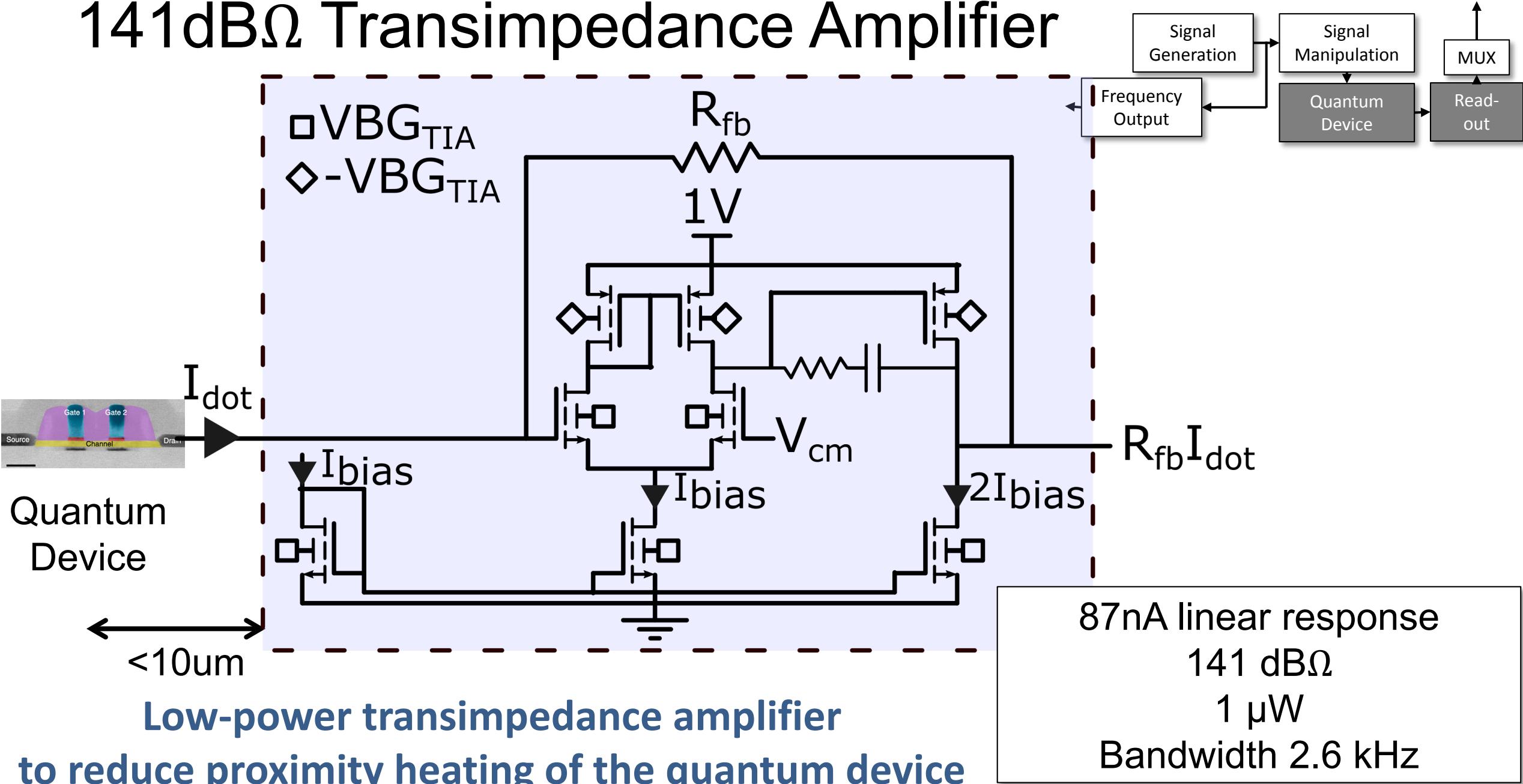


Passive elements operate at 110mK

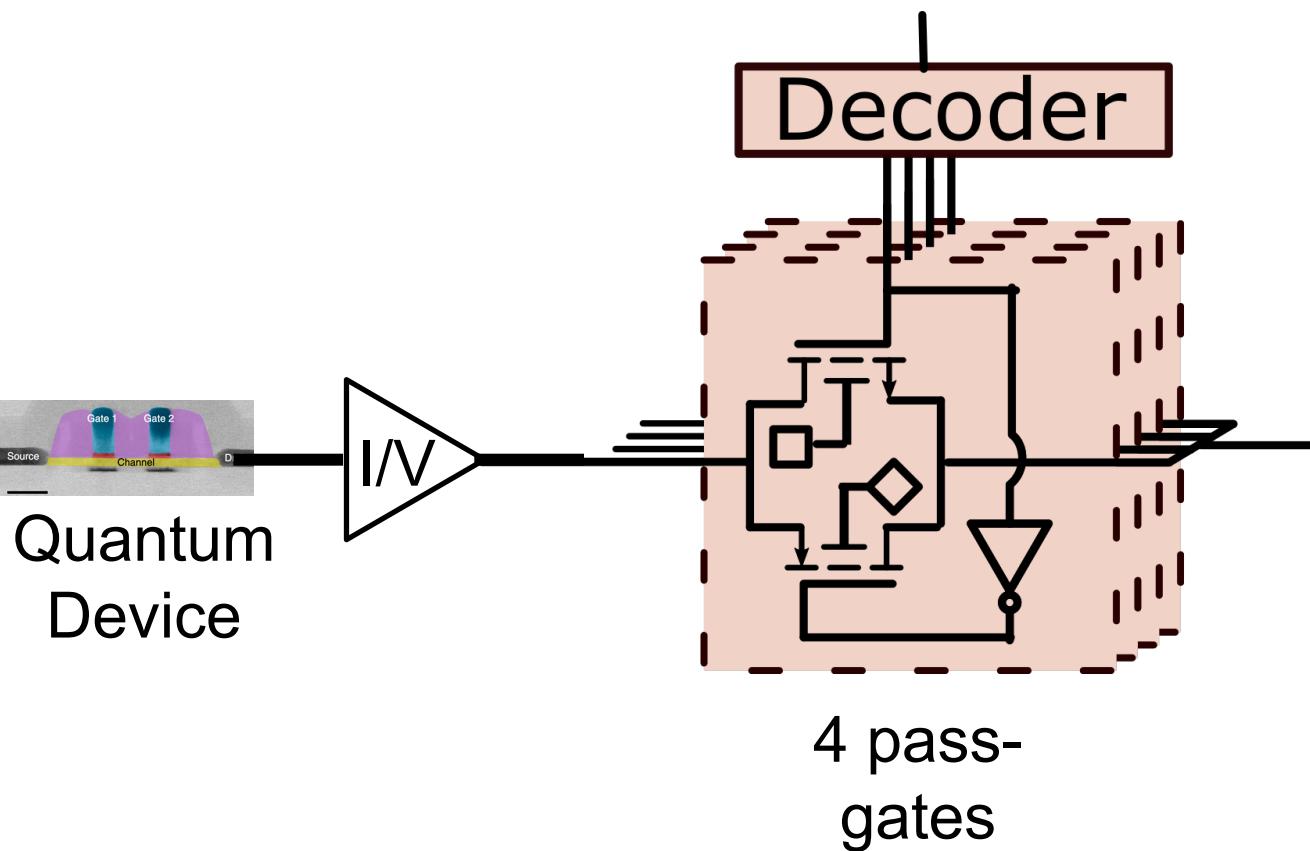


19.2: A TiAlN 295μm 28nm FD-SOI CMOS Quantum Integrated Circuit with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot

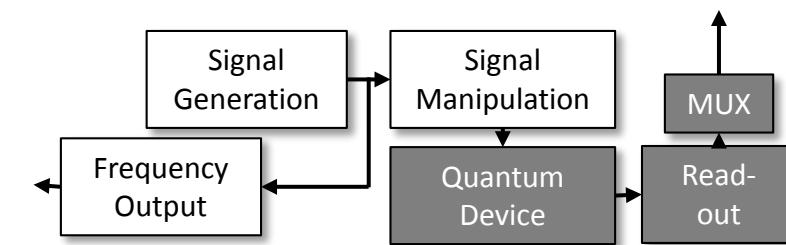
141dB Ω Transimpedance Amplifier



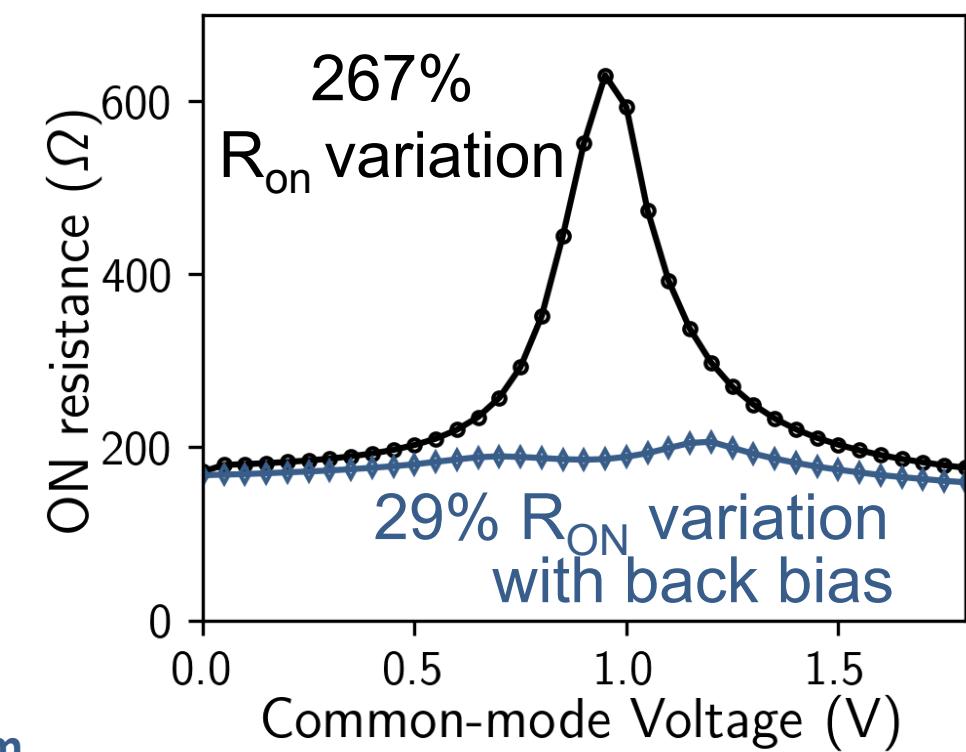
Analog Multiplexing



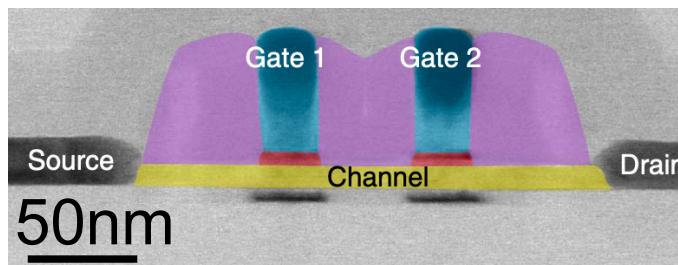
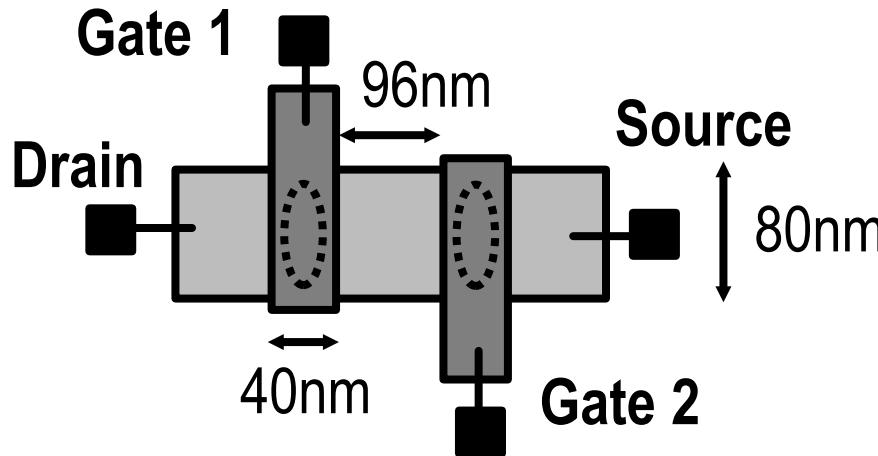
Back bias reduces R_{ON} variation against V_{cm}
Pass-gates operate for large signals



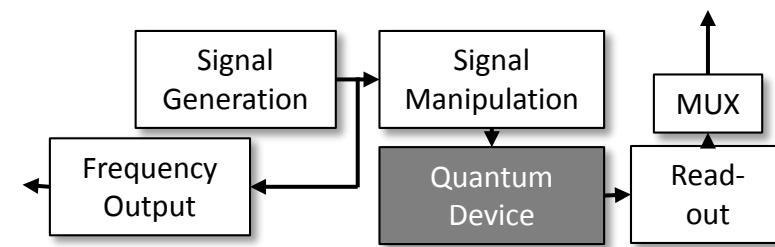
R_{ON} variation with
common-mode voltage



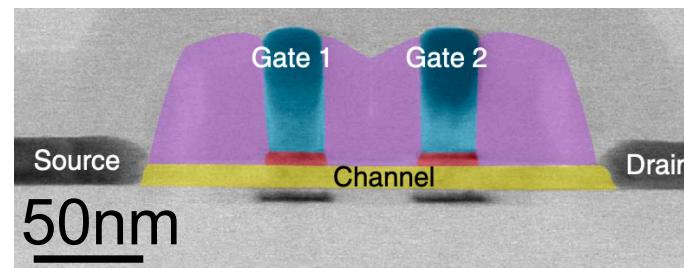
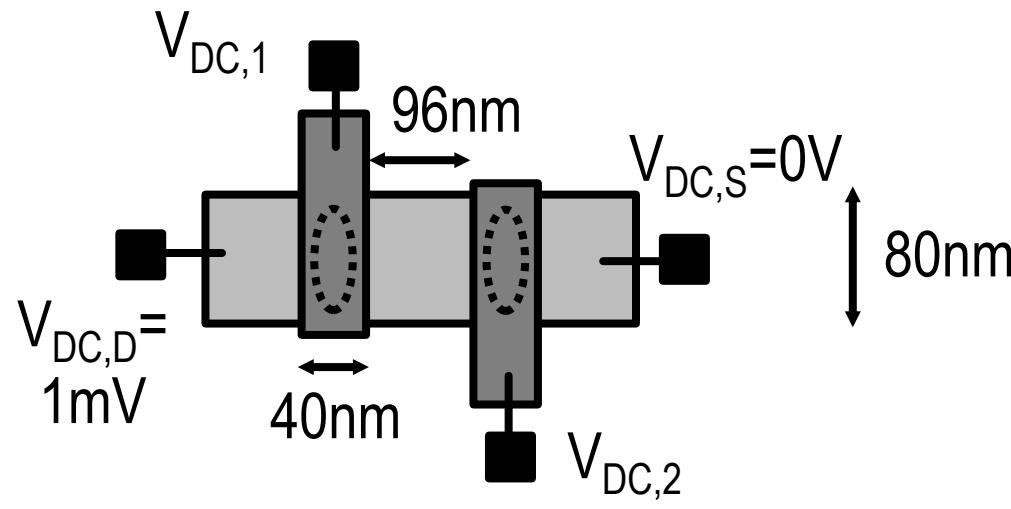
On-chip Double Quantum Dot



Similar layout as
the first CMOS spin qubit

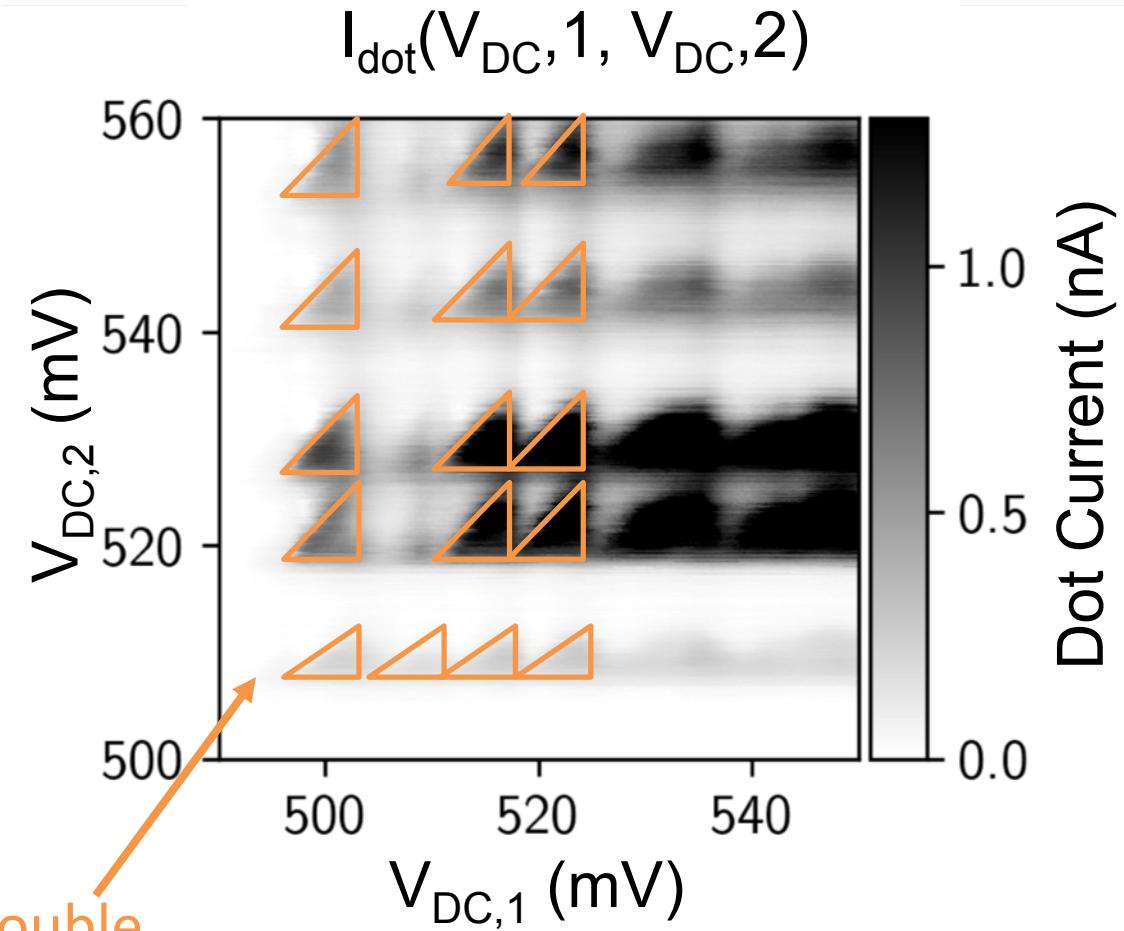
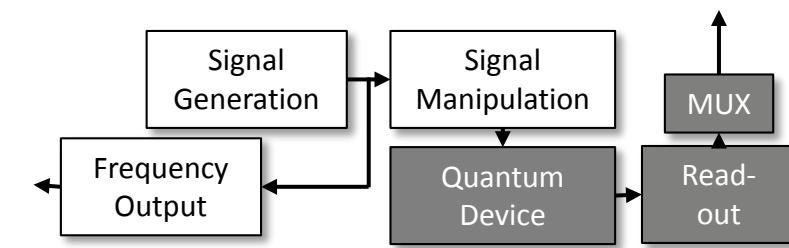


On-chip Double Quantum Dot



Similar layout as
the first CMOS spin qubit

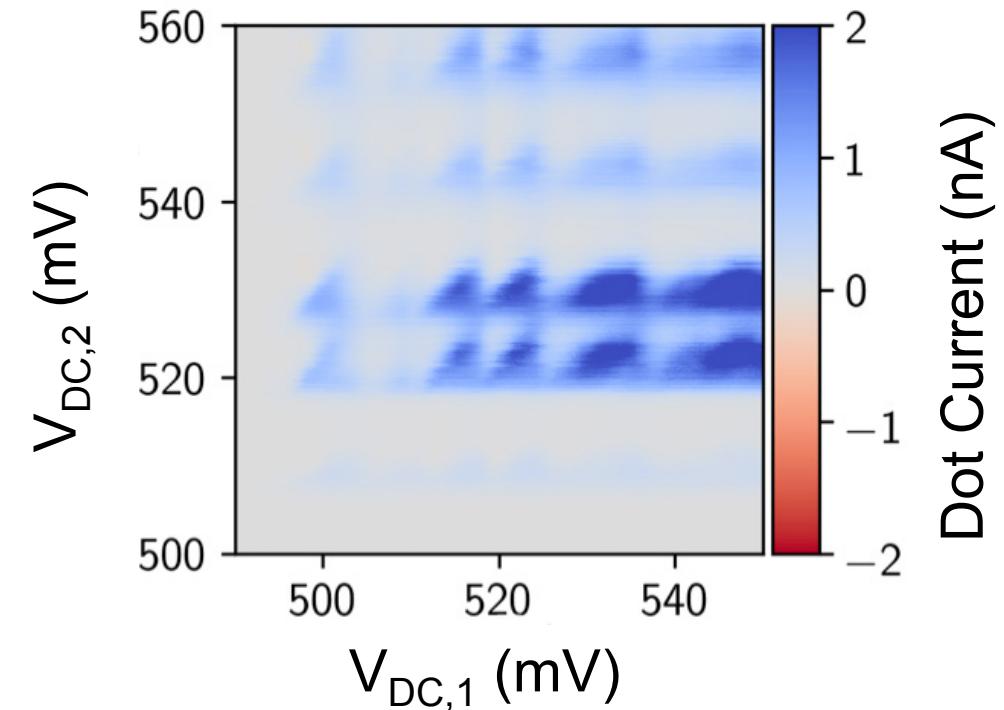
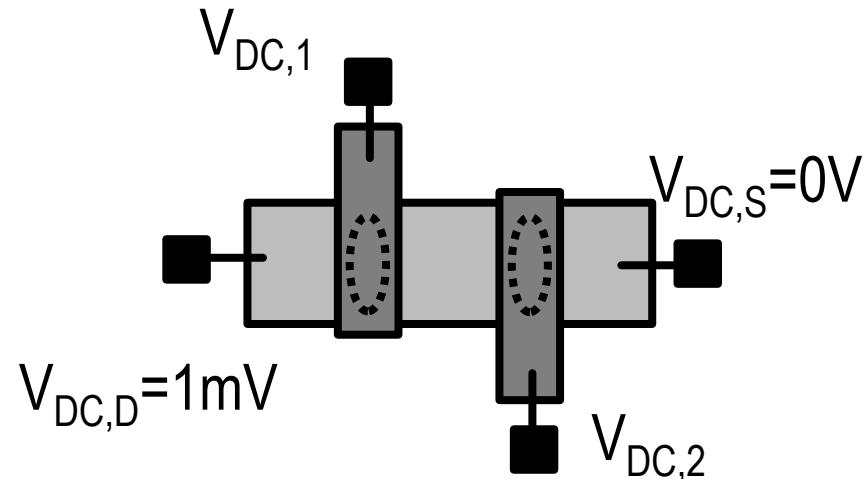
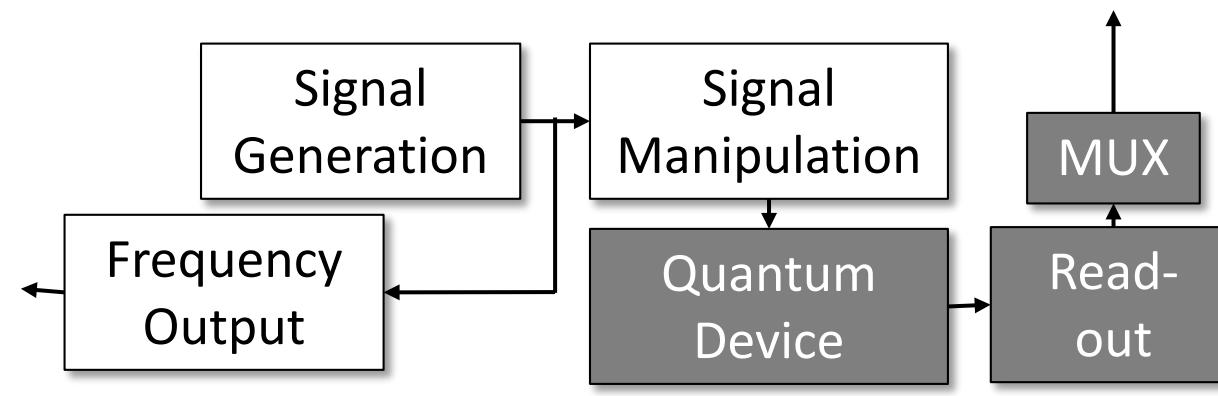
Signature of a double
quantum dot



Working quantum device
on industrial technology

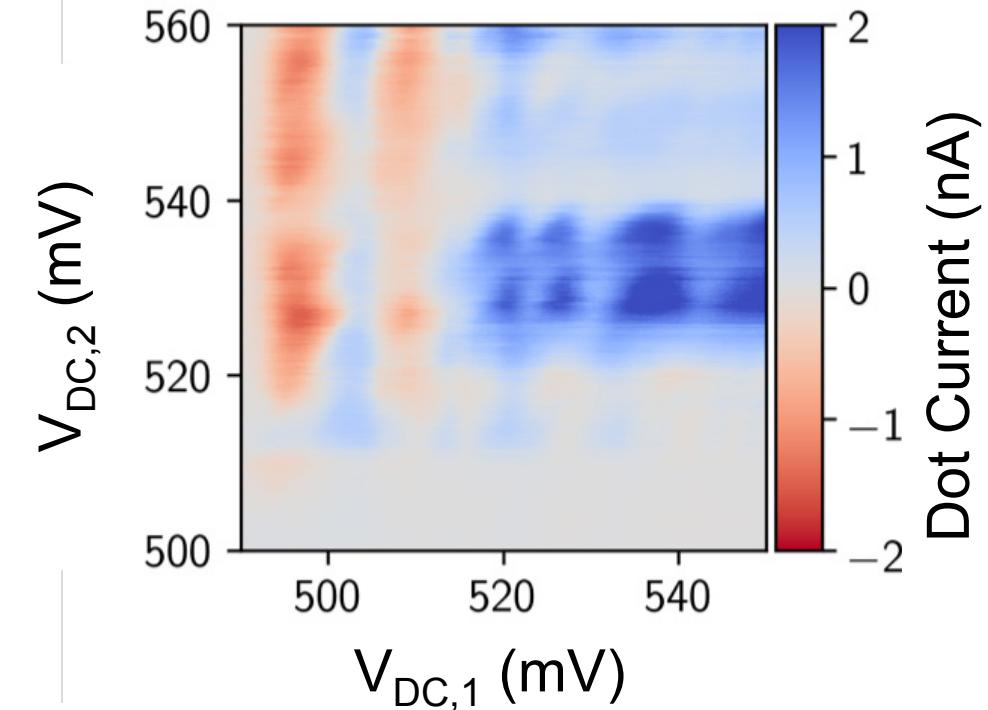
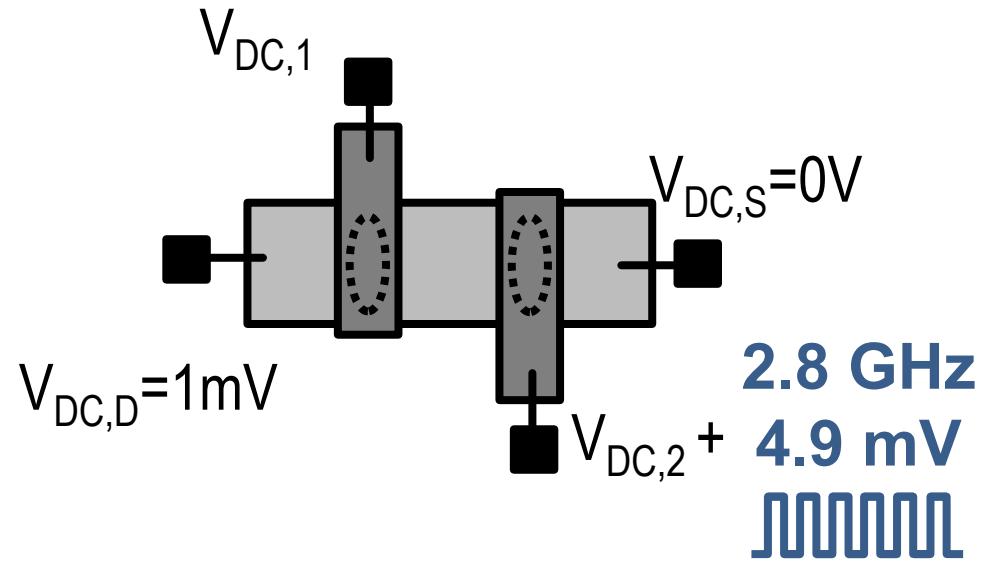
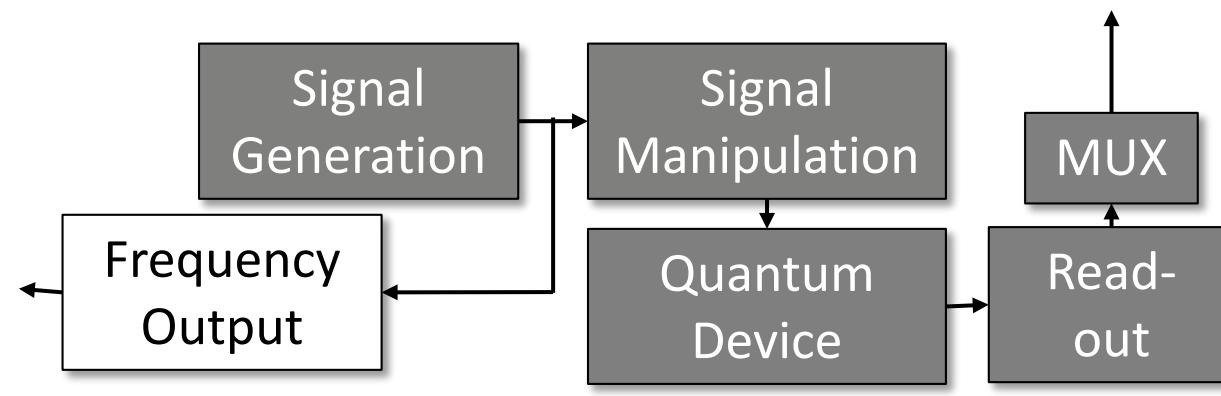
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with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot

DC Measurement of Quantum Dot Device



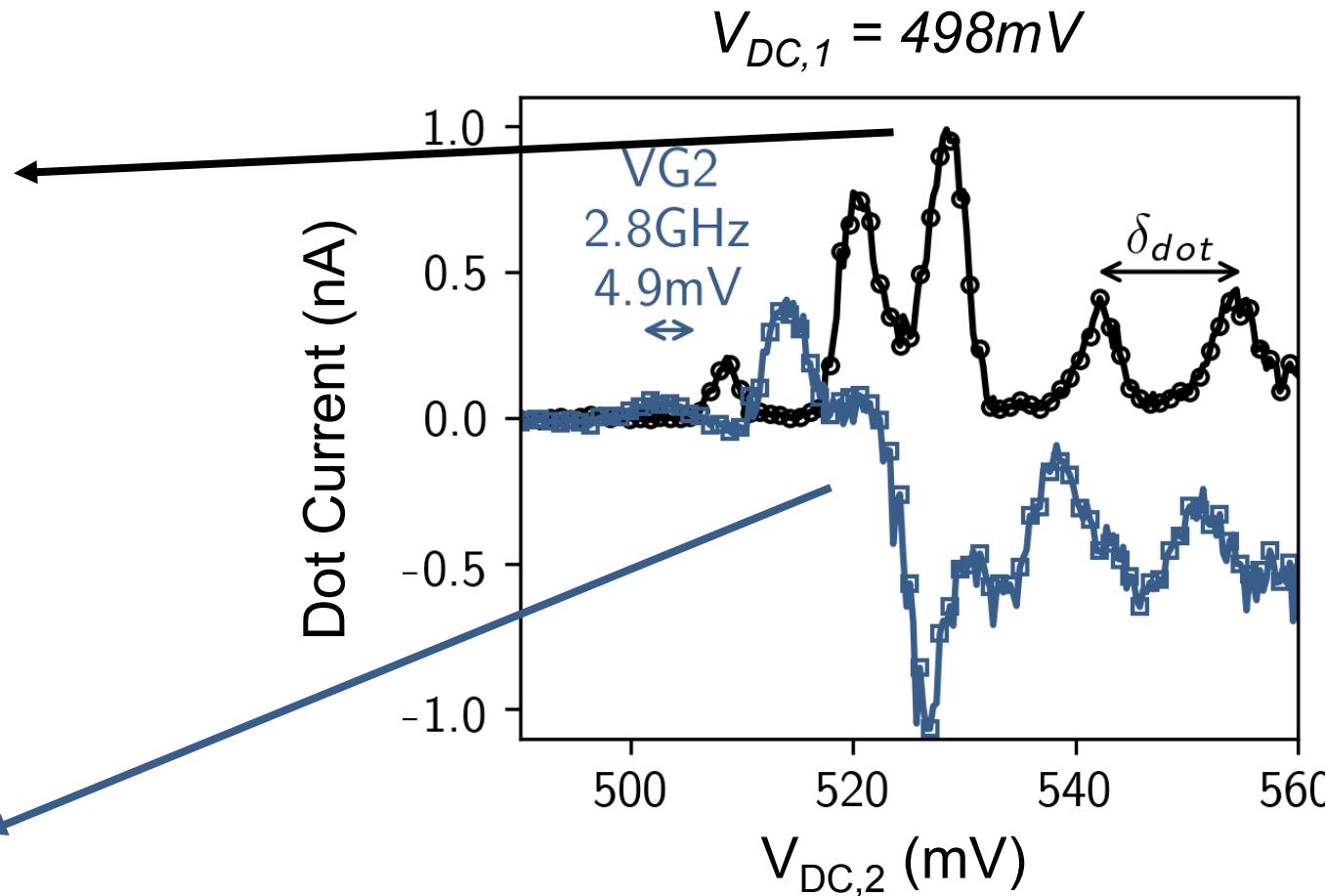
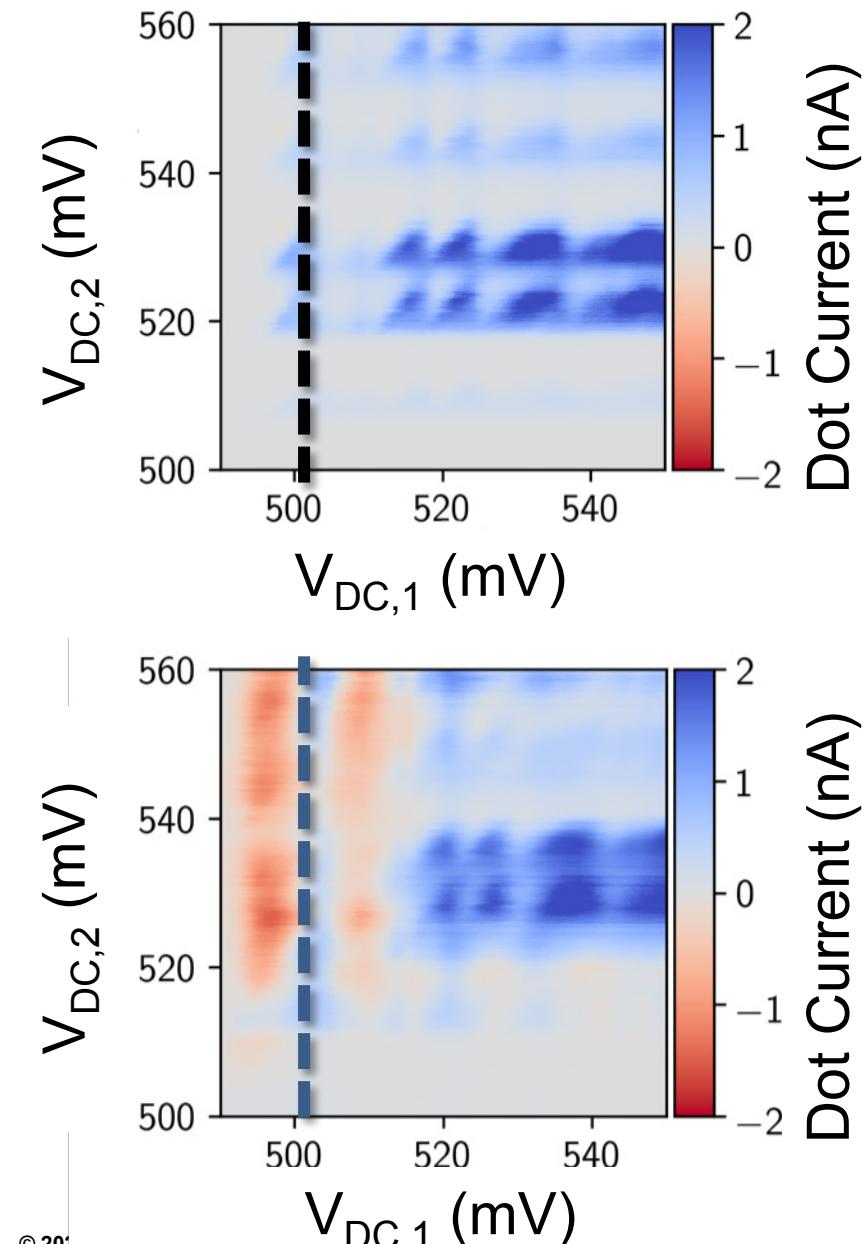
Fully-integrated DC
quantum device measurement

GHz Excitation of Quantum Dot Device



All-integrated quantum device
GHz-excitation and DC measurement

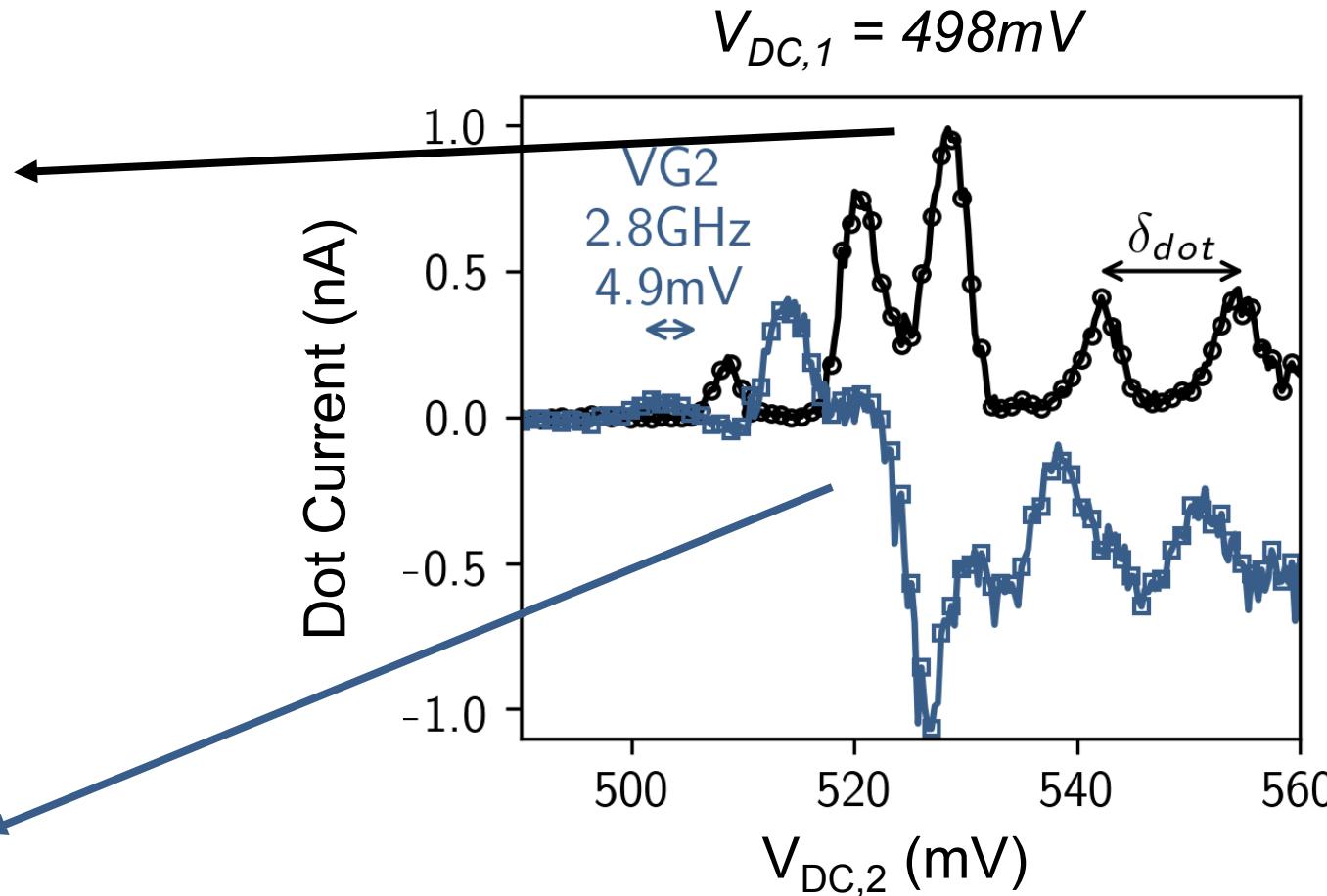
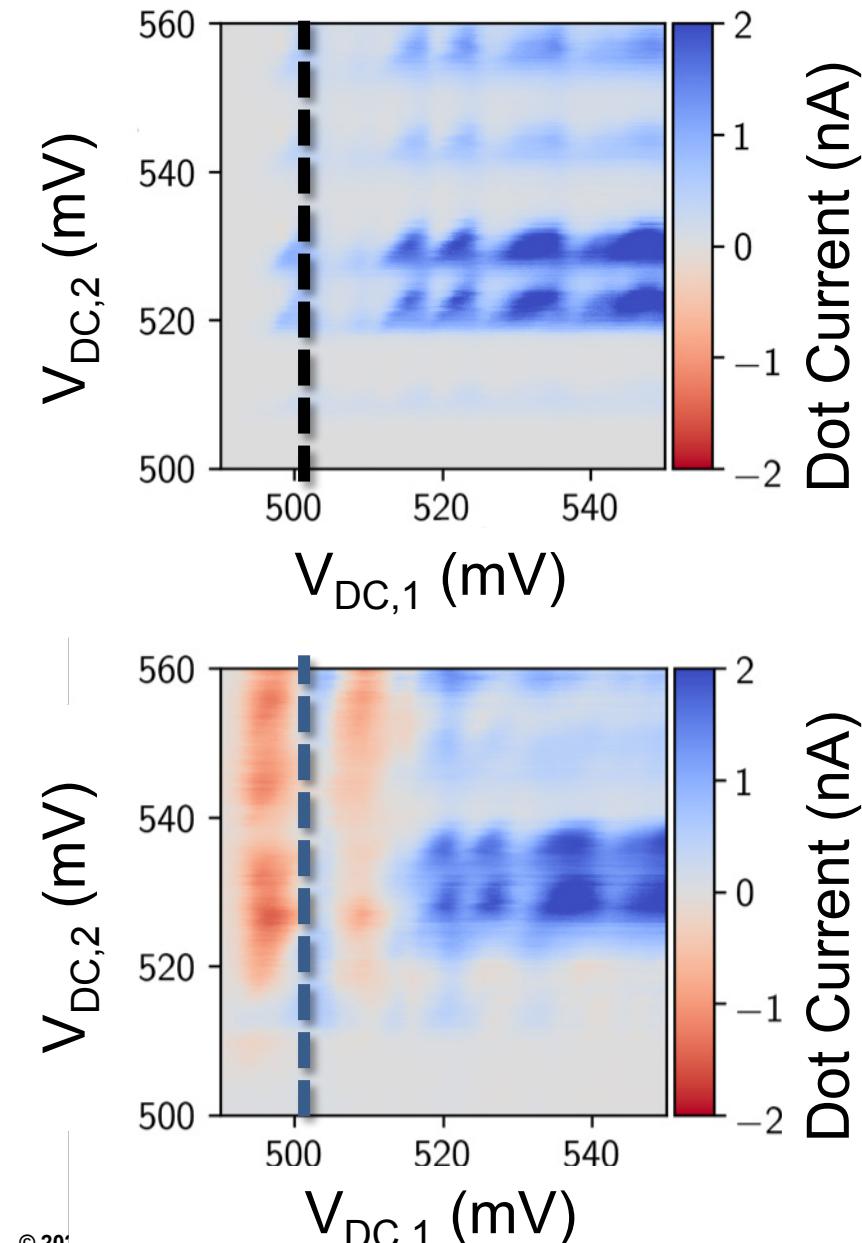
GHz Excitation of Quantum Dot Device



High frequency effect on detected current:

- Charge pumping
- Rectification

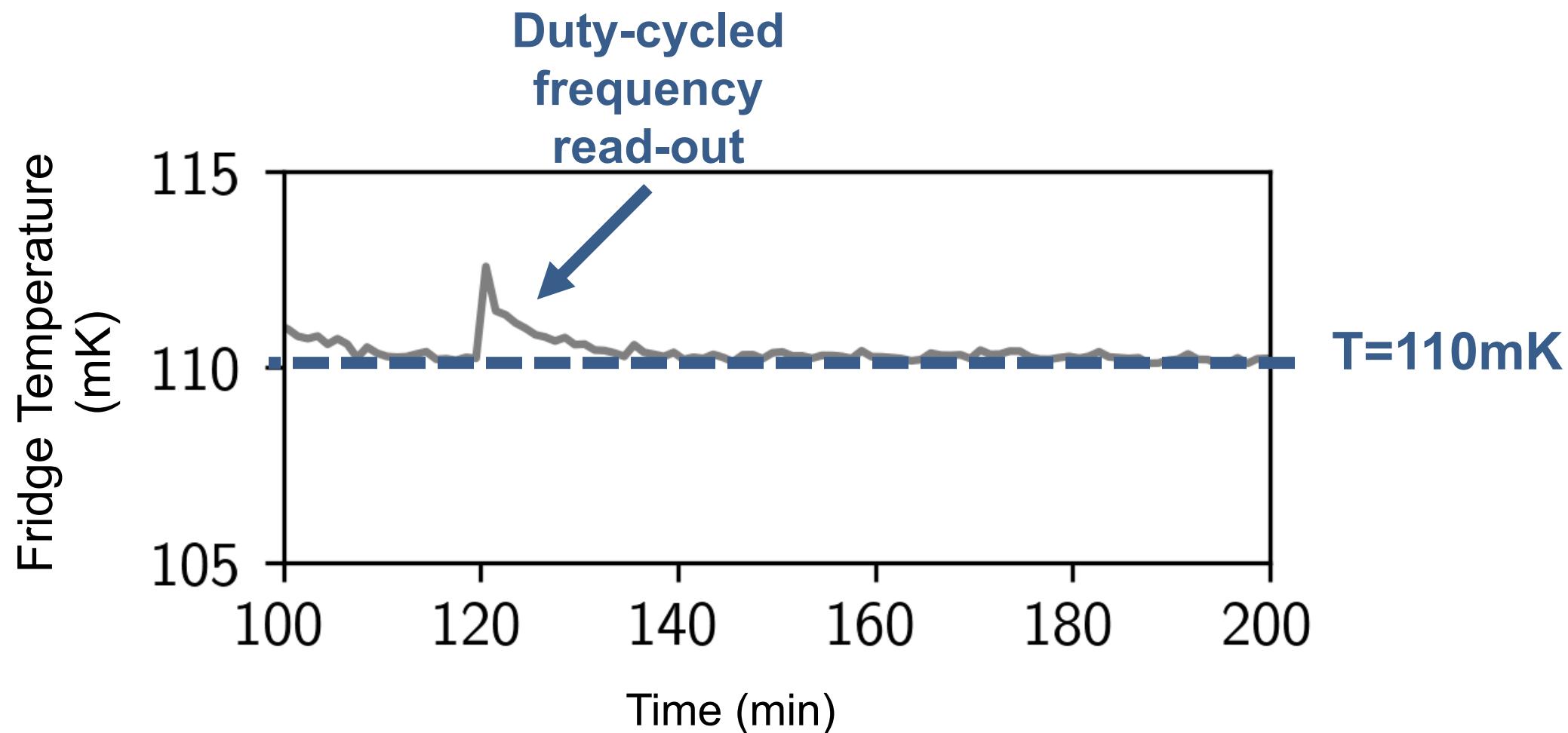
GHz Excitation of Quantum Dot Device



High frequency effect on detected current:

- Charge pumping
- Rectification

Temperature stability with dissipating electronics



Power-consuming pre-calibration operations can be duty-cycled at low-temperature resulting in negligible temperature increase

Cryogenic control & read-out systems

	Charbon et al. (2017)	Bardin et al. (2019)	Our Work
Temperature	4.2 K	3 K	0.11 K
Application	Future Qubits Experiments	XMON Rabi Experiments	Double Quantum Dot Dynamics
On-chip	Analog	Yes	Yes
	Digital	No	Yes
	Quantum	No	Yes

Operation at quantum device temperature

- Increase read-out sensitivity (less interconnection parasitics)
- Higher connectivity to the quantum core (less heat leakage)

Conclusion

- ✓ **Electronics operating at sub-K temperature**
- ✓ **Monolithic integration of Quantum and Classical circuits**
- ✓ **FD-SOI Back bias drastically improves circuit performance**
- ✓ **GHz signals on-chip, <10MHz signals off-chip**



A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Jiang Gong¹, Yue Chen¹, Fabio Sebastian¹,
Edoardo Charbon^{2,3}, Masoud Babaie¹

¹Delft University of Technology, Delft, The Netherlands

²EPFL, Lausanne, Switzerland

³Intel, Hillsboro, OR



Outline

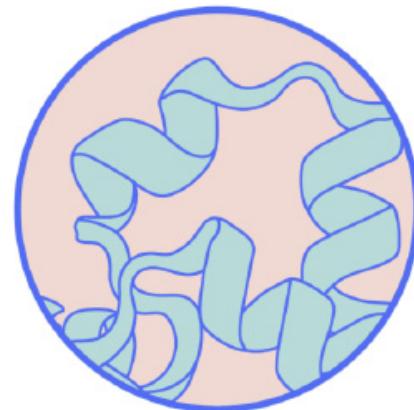
- Motivation
- Cryogenic Oscillators: Design Challenges
- Proposed Calibration for the Optimum Phase Noise
- Circuit Implementation
- Measurement Results
- Conclusions

Why quantum computers?

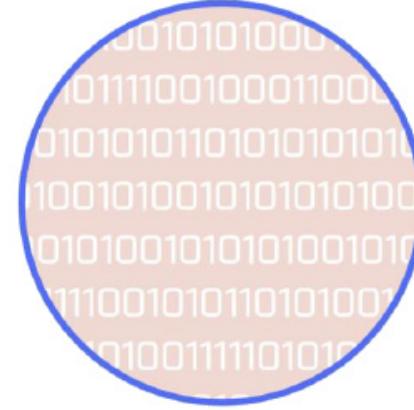
Encryption



Protein folding



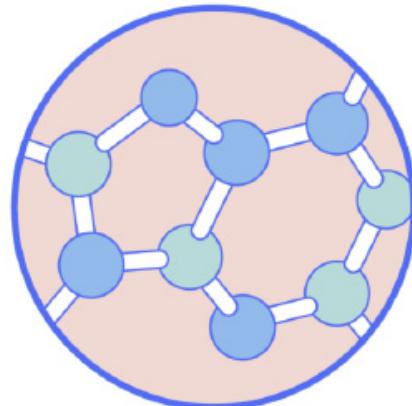
Big data



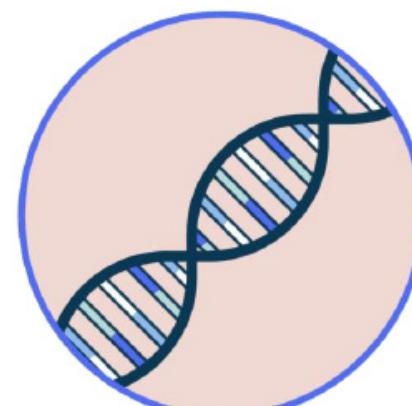
Drug synthesis



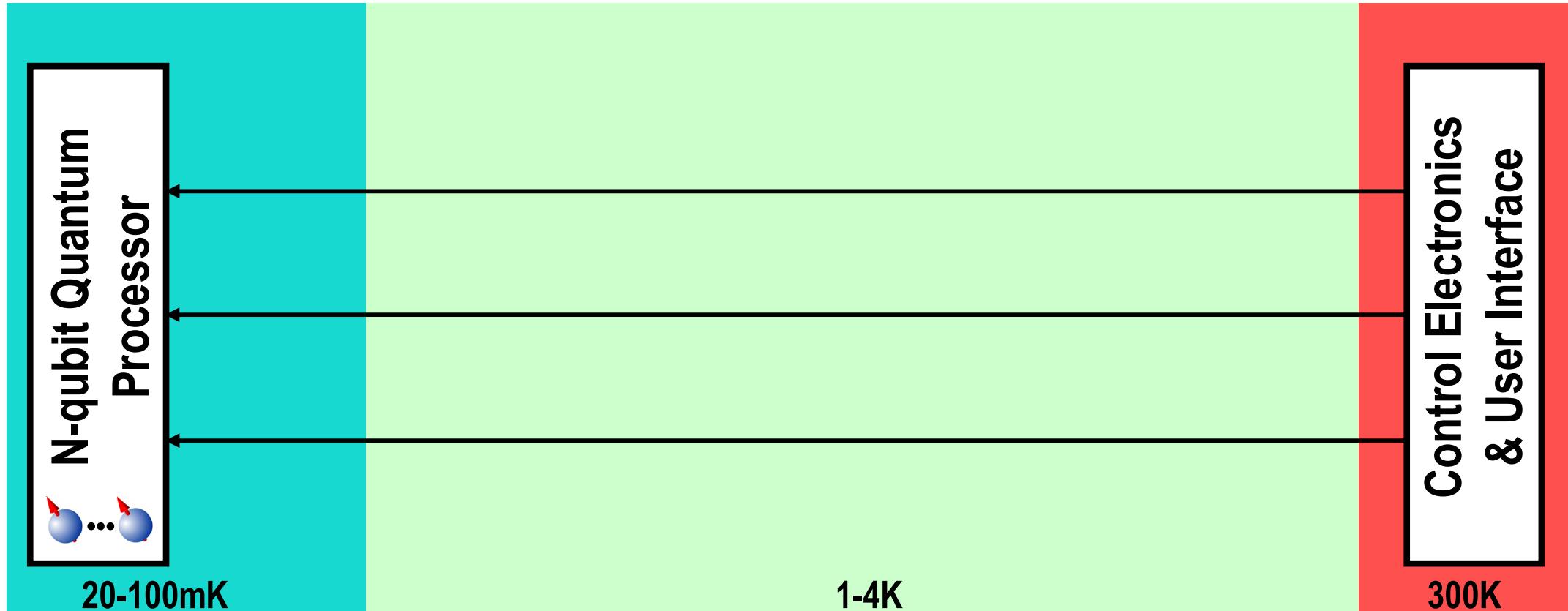
Molecule simulation



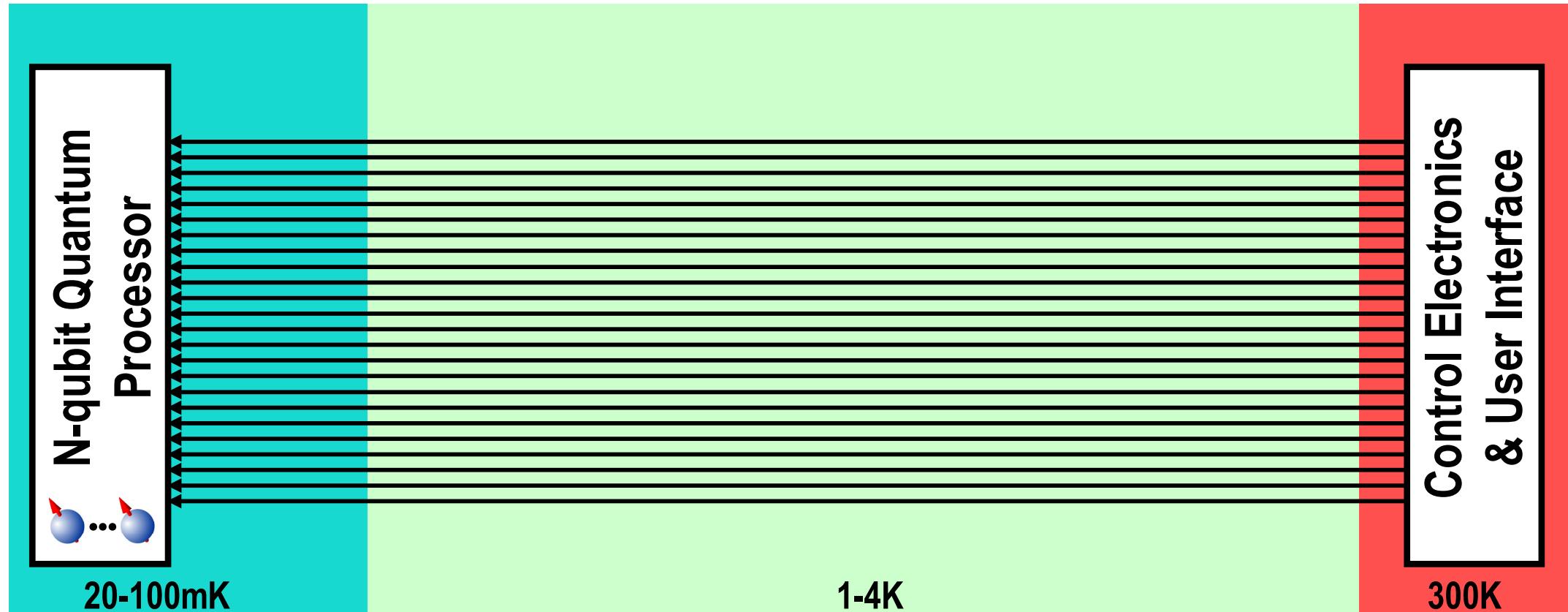
DNA analysis



State-of-the-art quantum computers

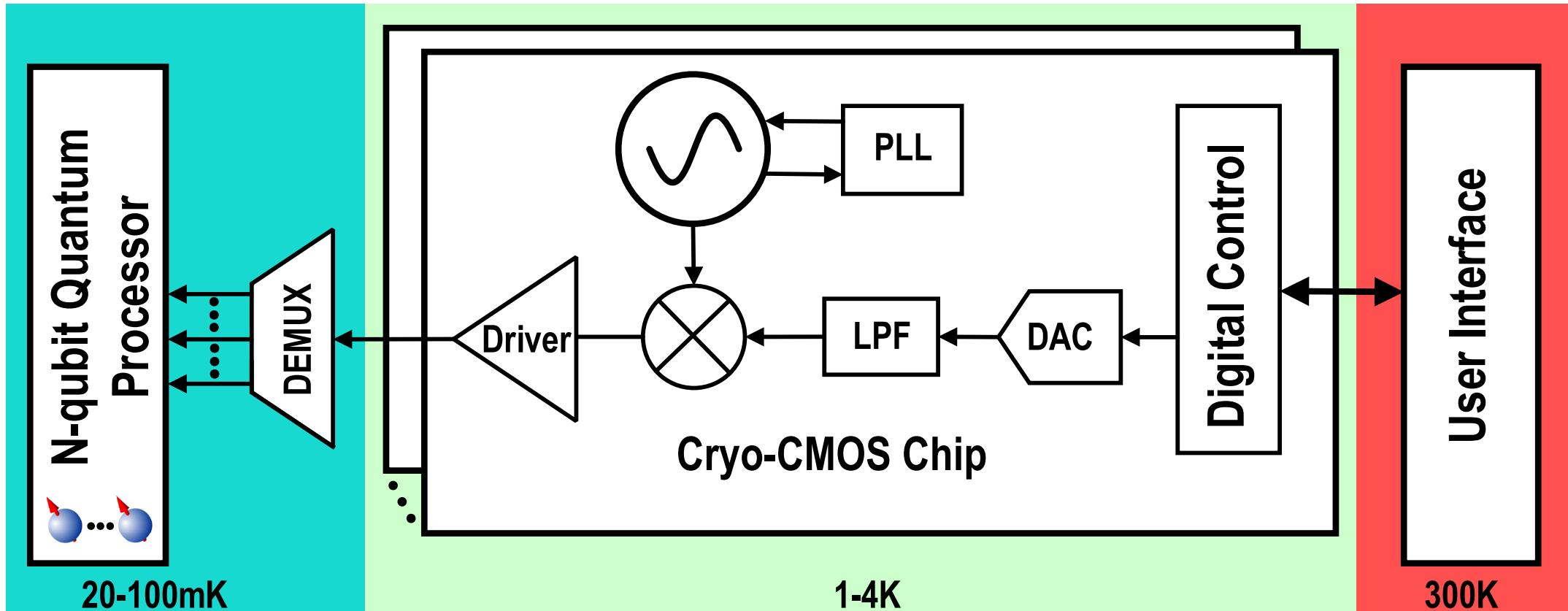


State-of-the-art quantum computers



- Interconnects \Rightarrow bottleneck to scaling

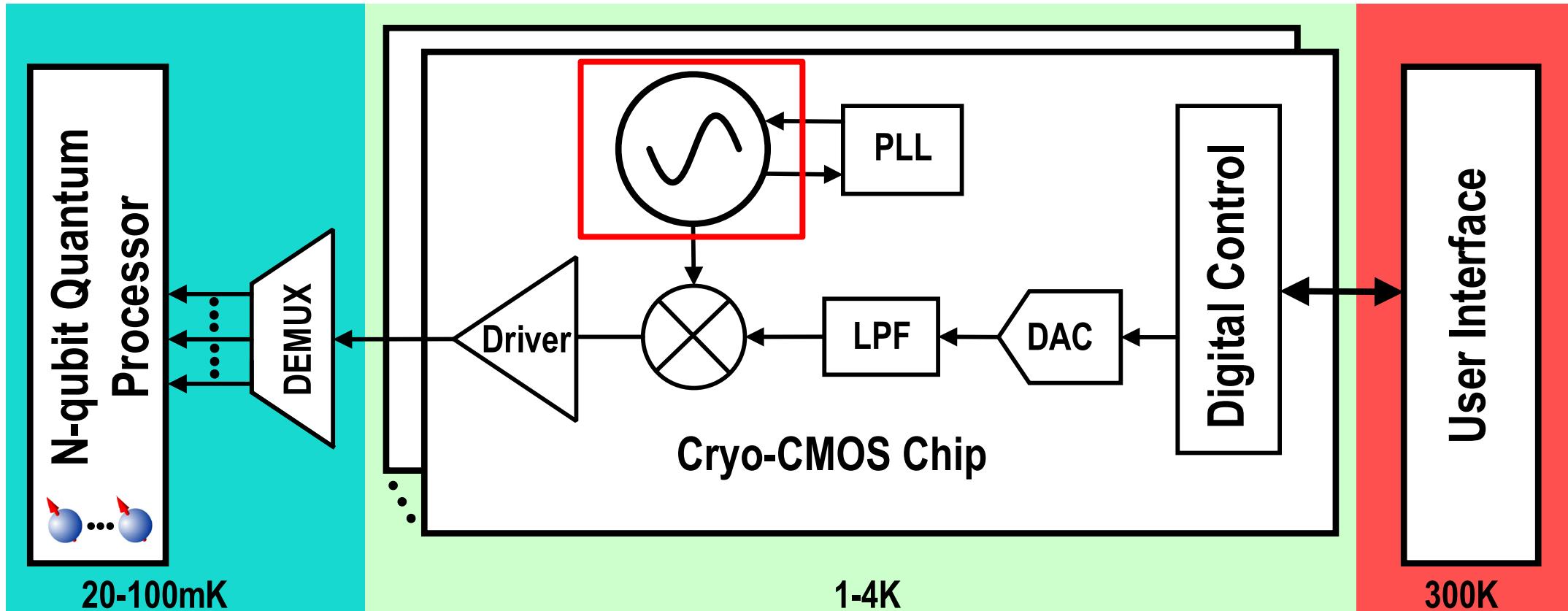
Future – Quantum computers with >1000 qubits



[Charbon, ISSCC'2017]

- Cryo-CMOS \Rightarrow eliminate interconnects \Rightarrow **scalable!**

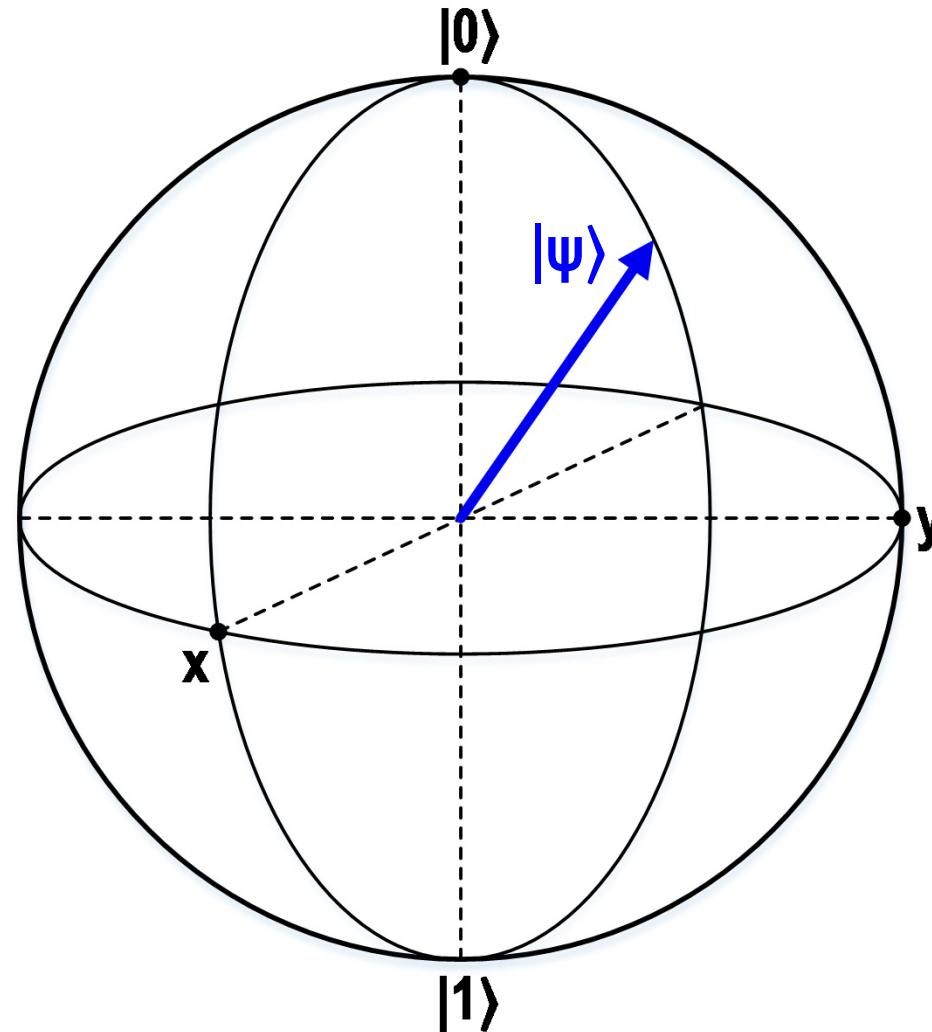
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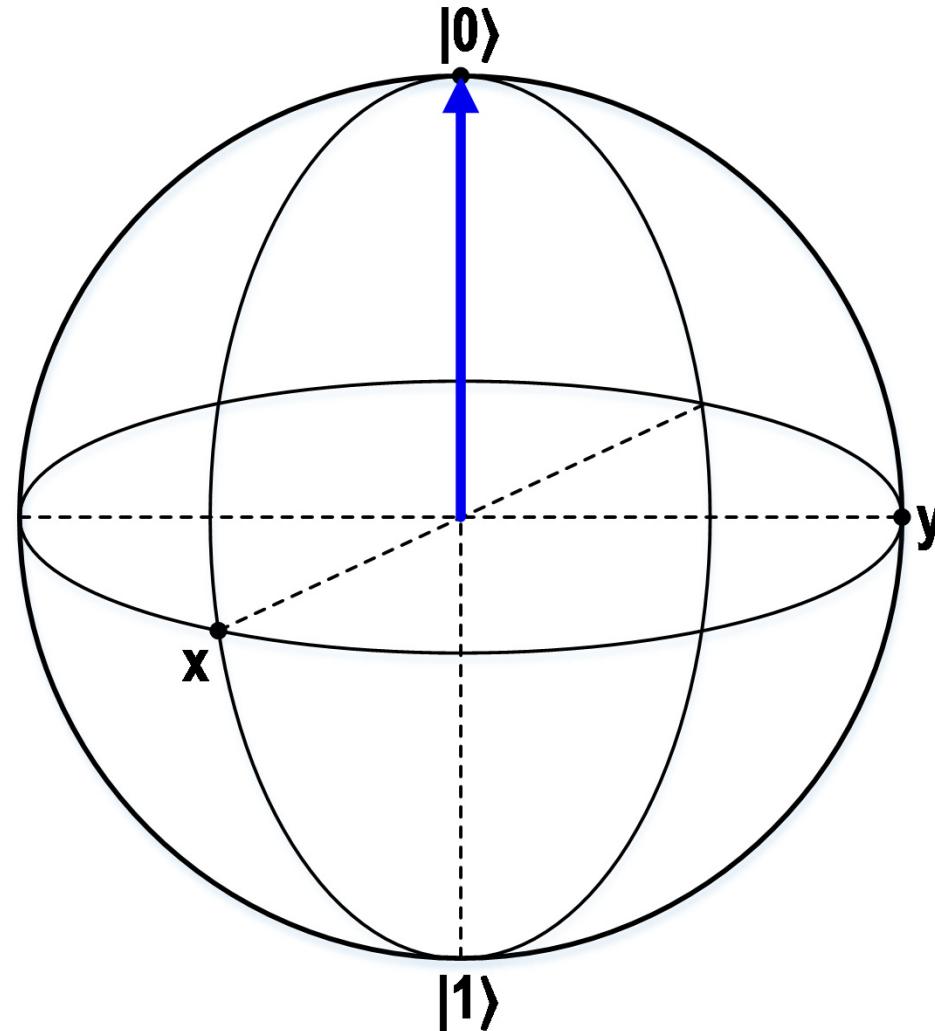
[Charbon, ISSCC'2017]

- Require a low power and low noise oscillator

Qubit representation – Bloch Sphere

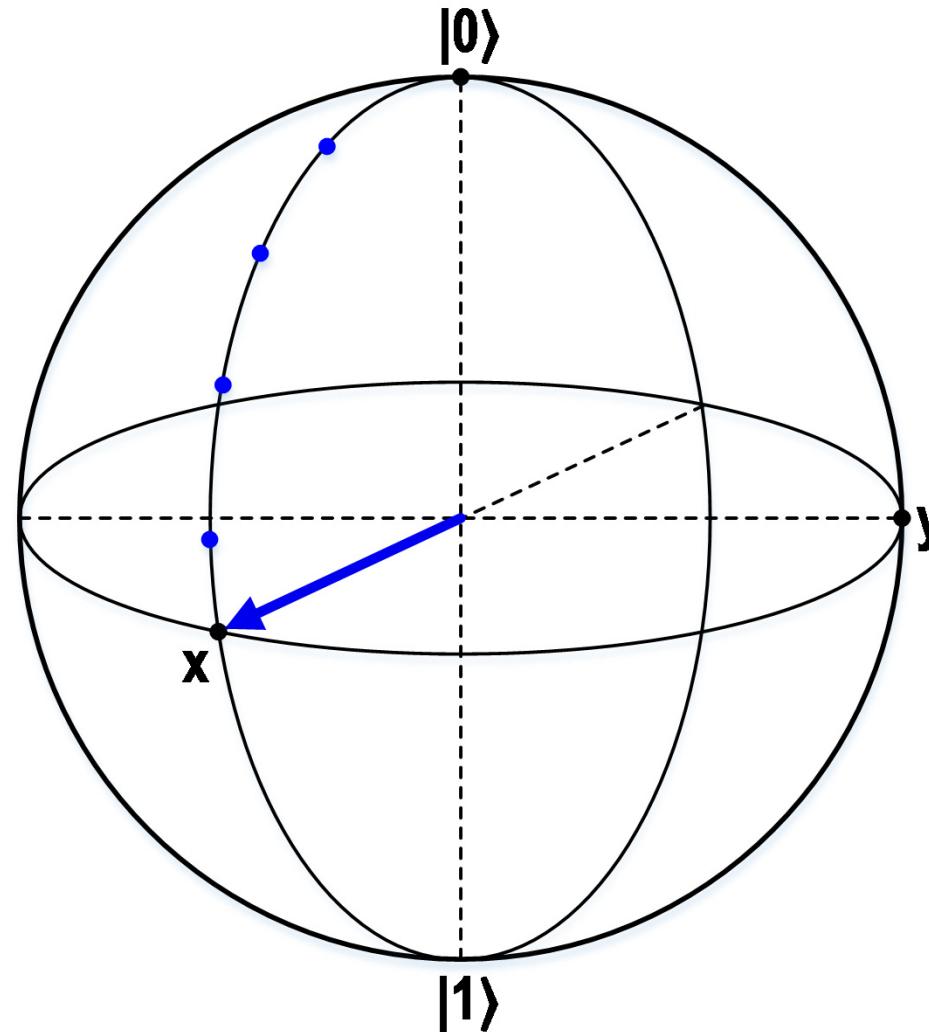
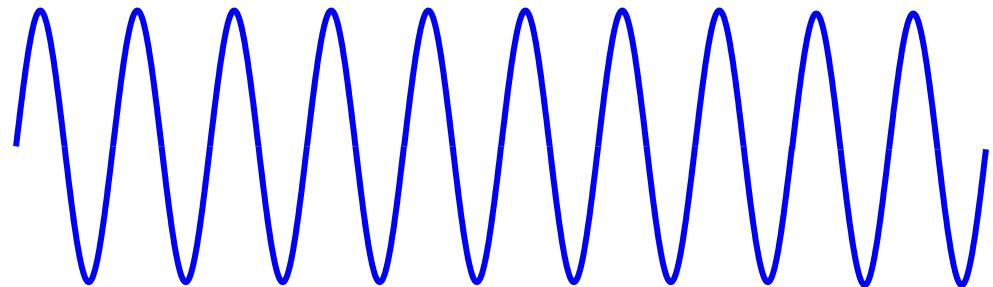


Qubit operation with an ideal oscillator



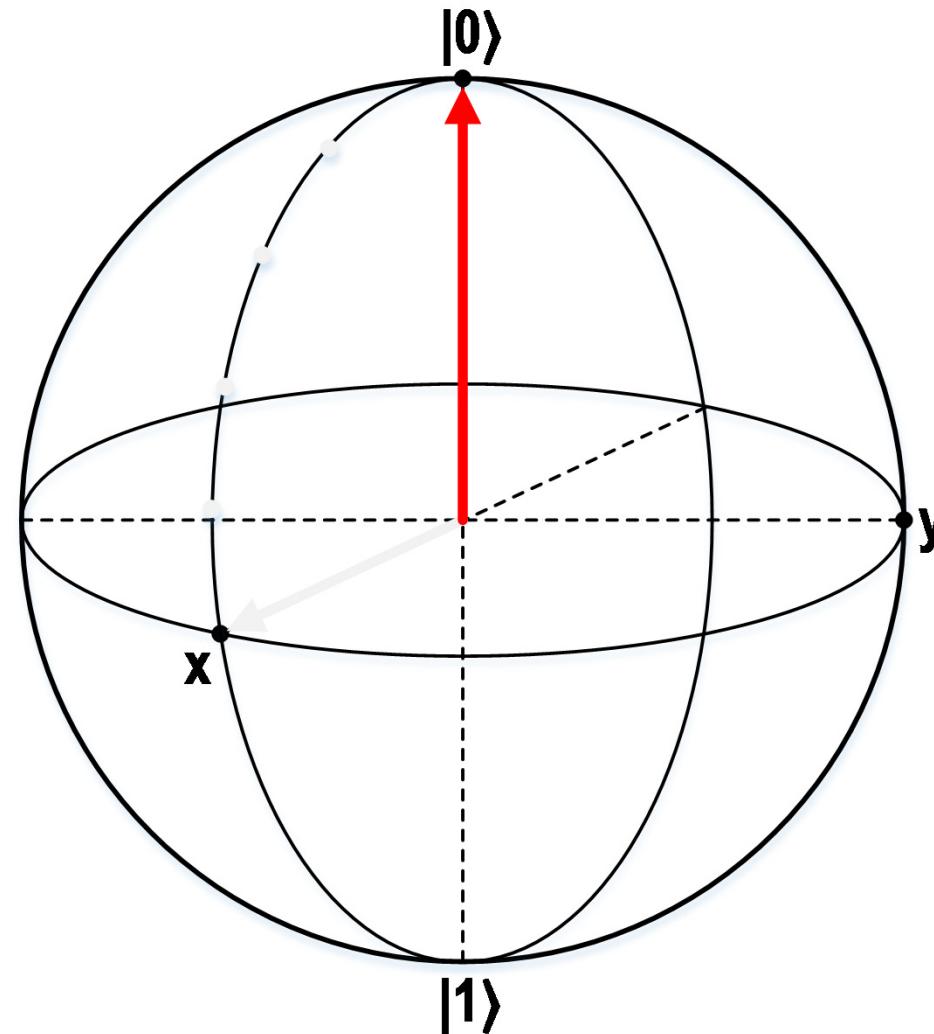
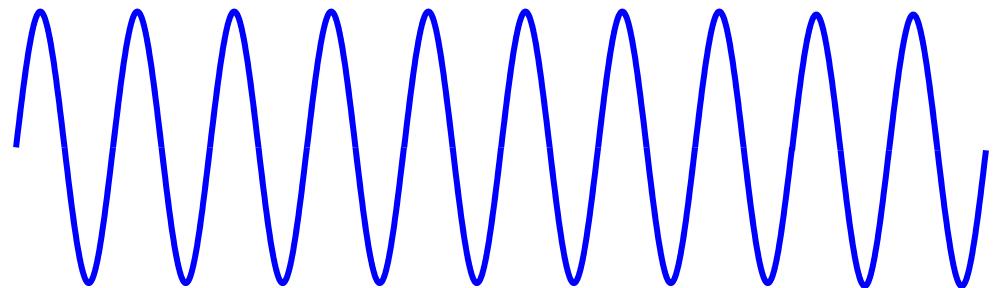
Qubit operation with an ideal oscillator

ideal oscillator

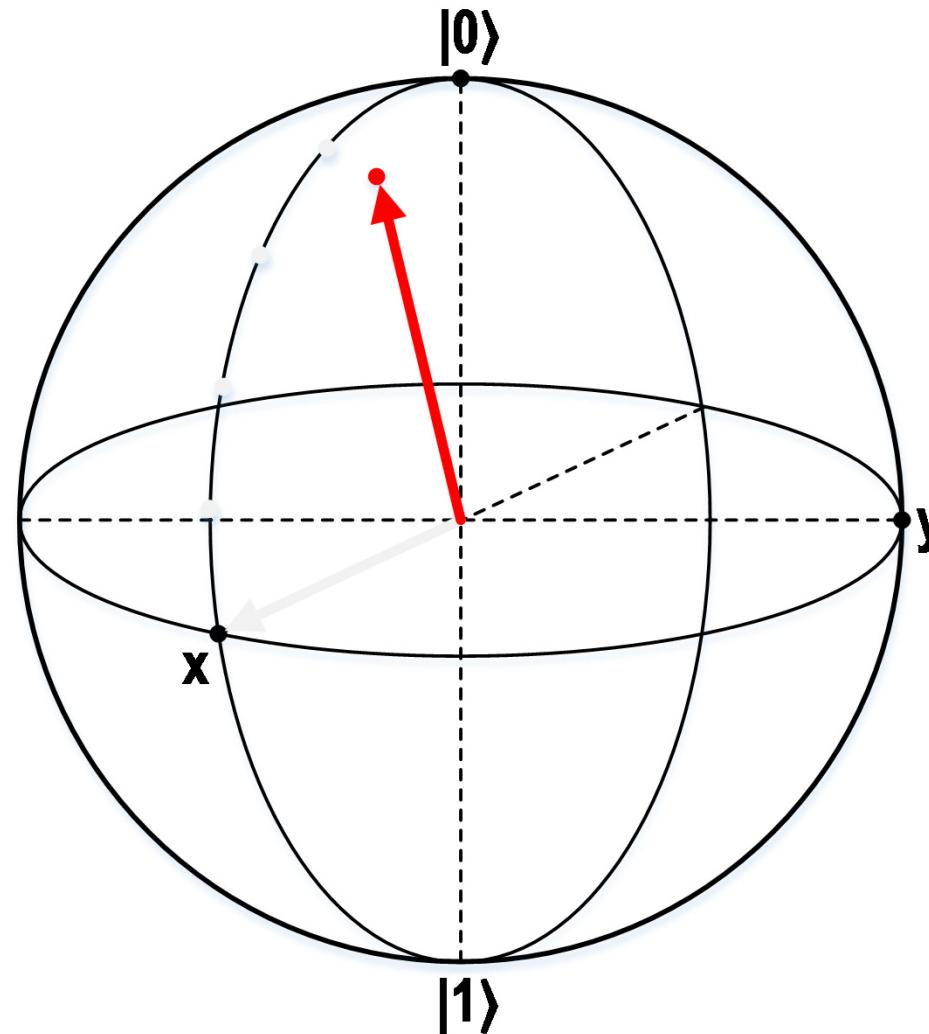
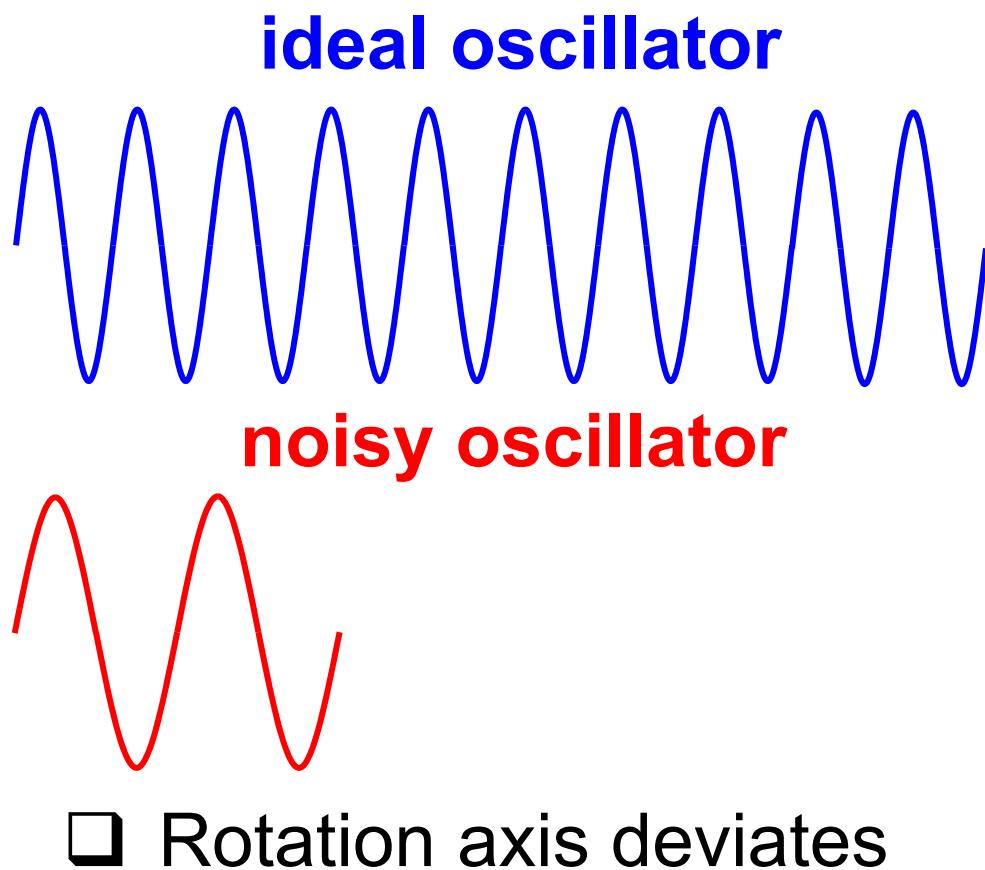


Qubit operation with a noisy oscillator

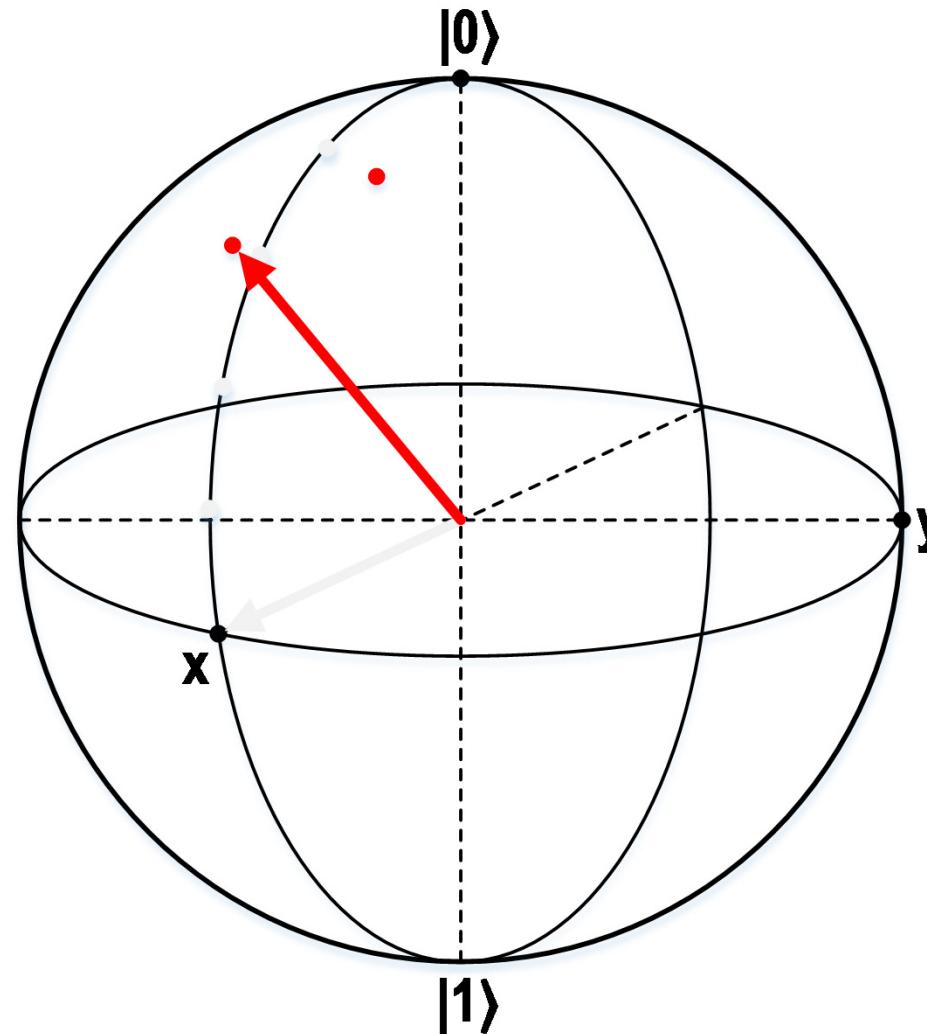
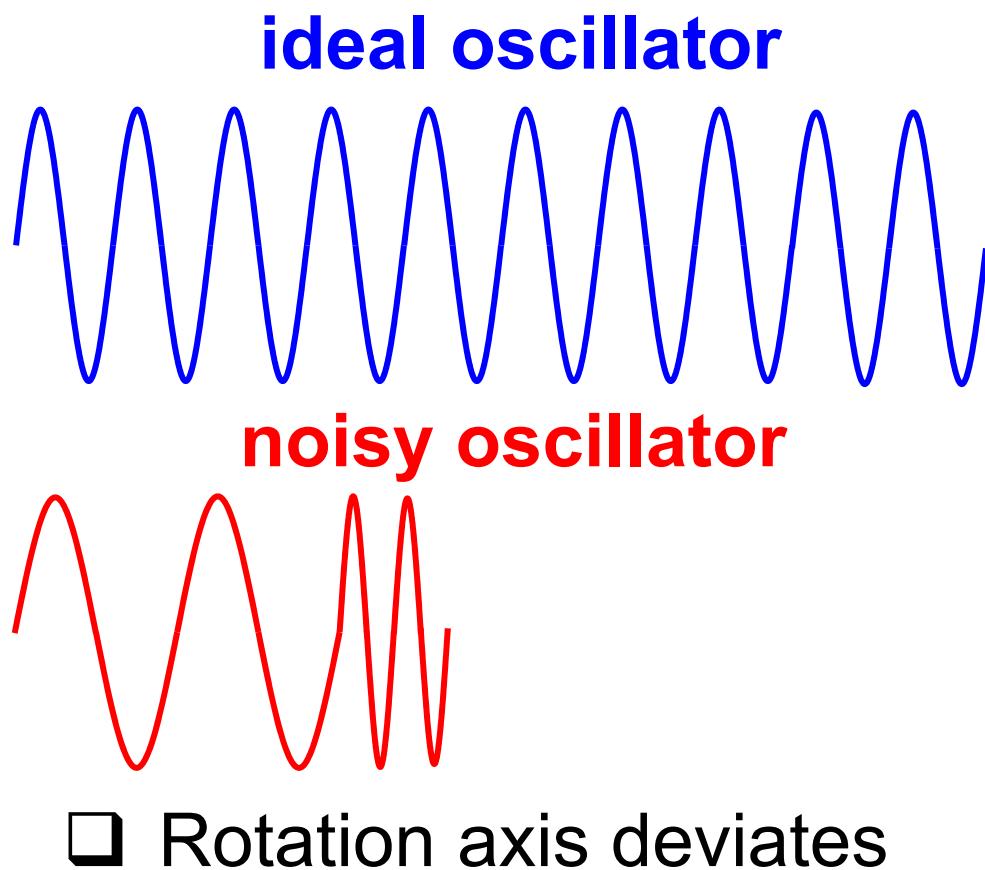
ideal oscillator



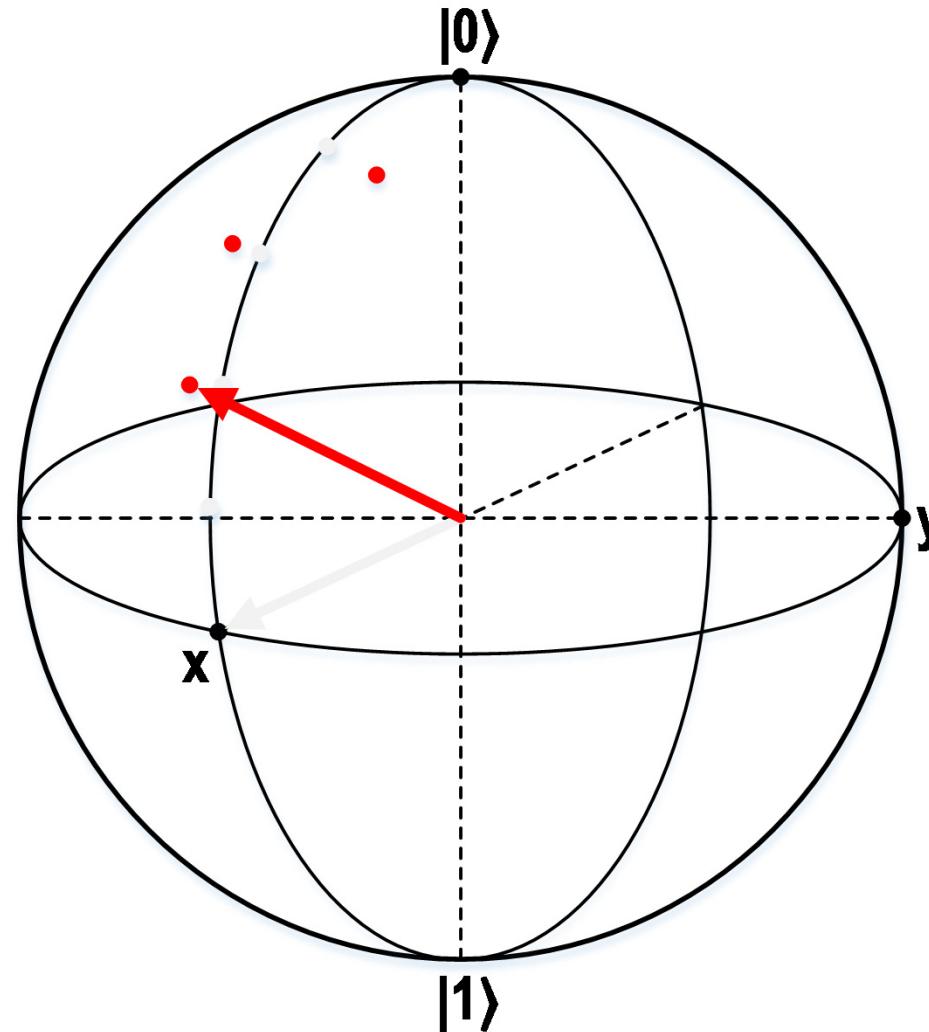
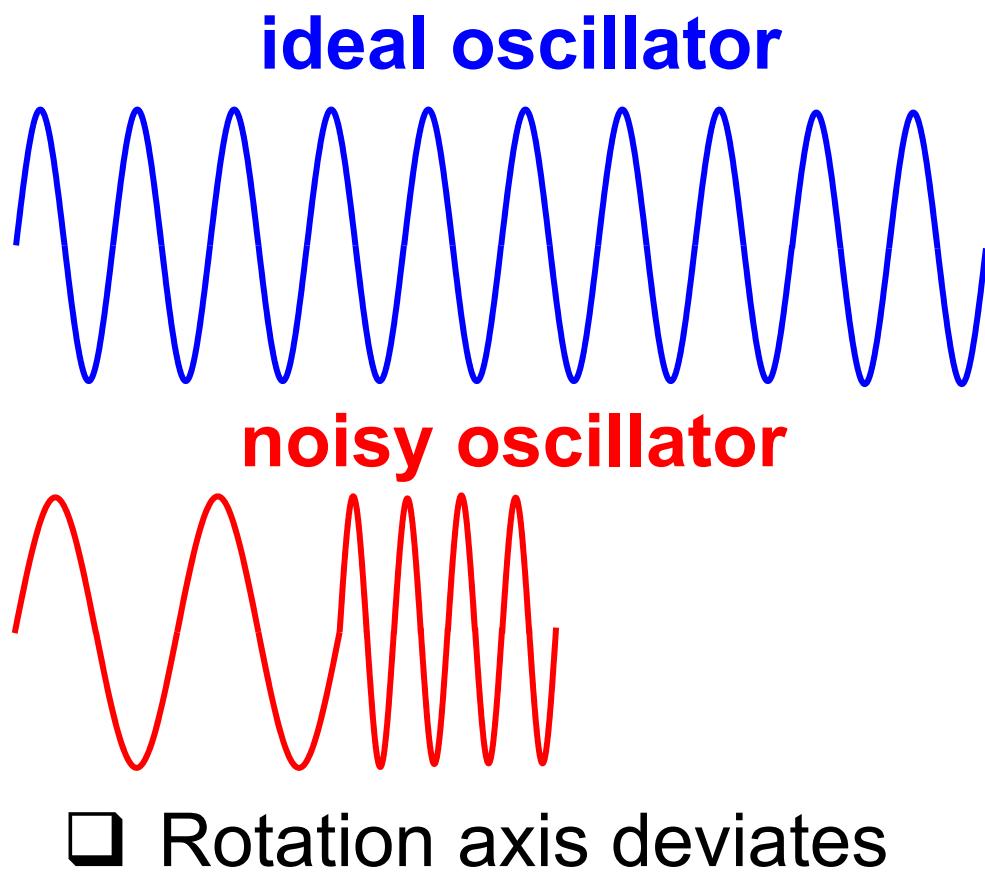
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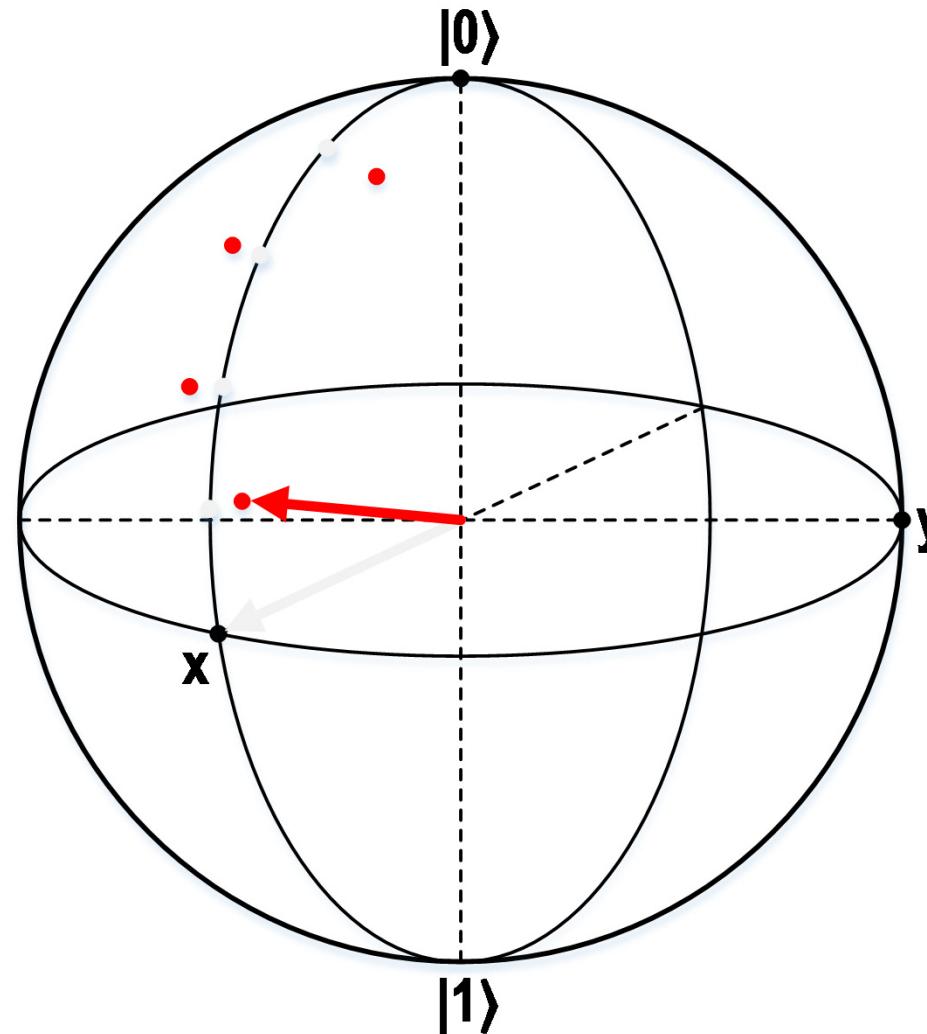
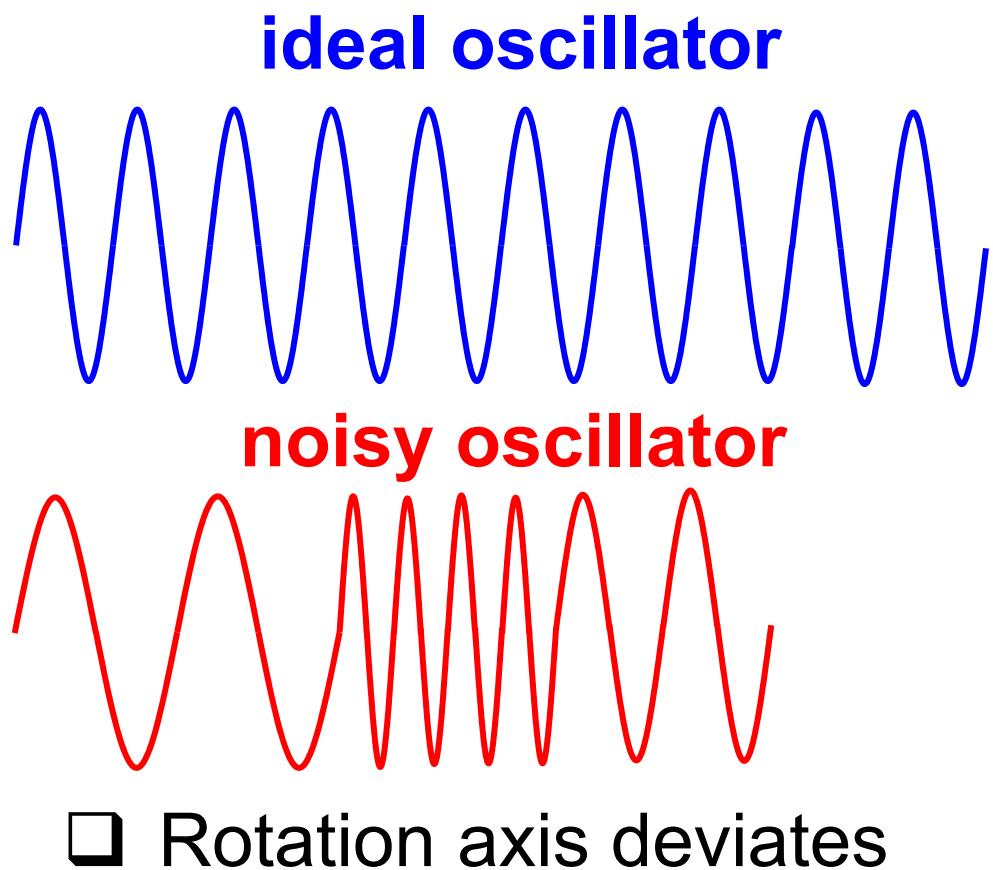
Qubit operation with a noisy oscillator



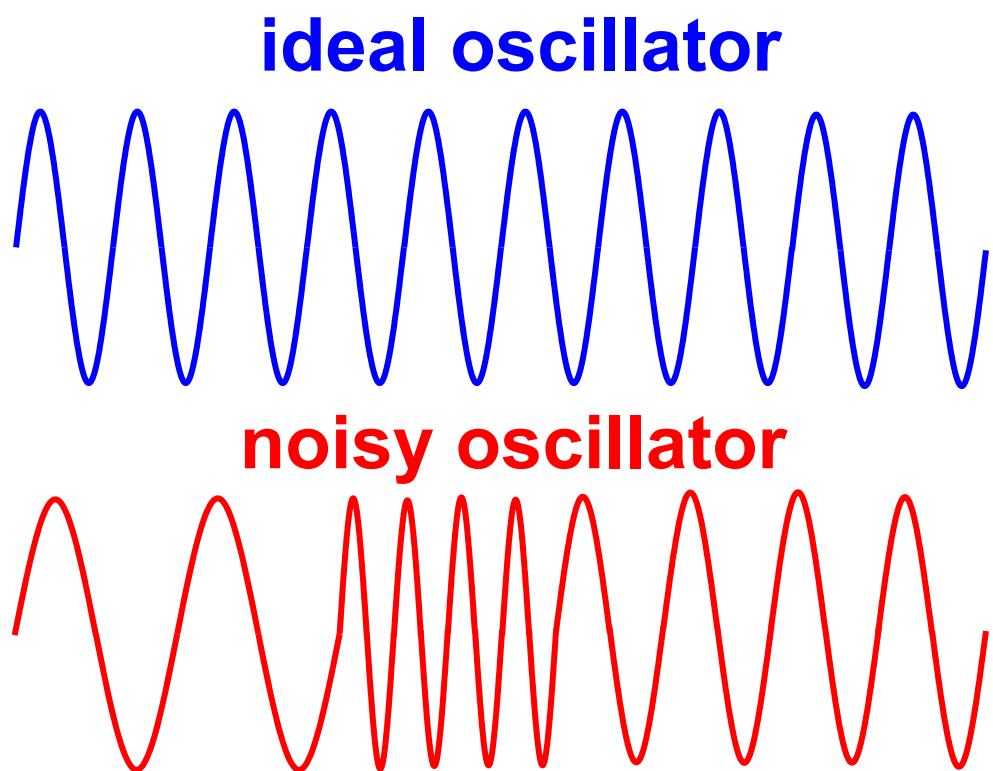
Qubit operation with a noisy oscillator



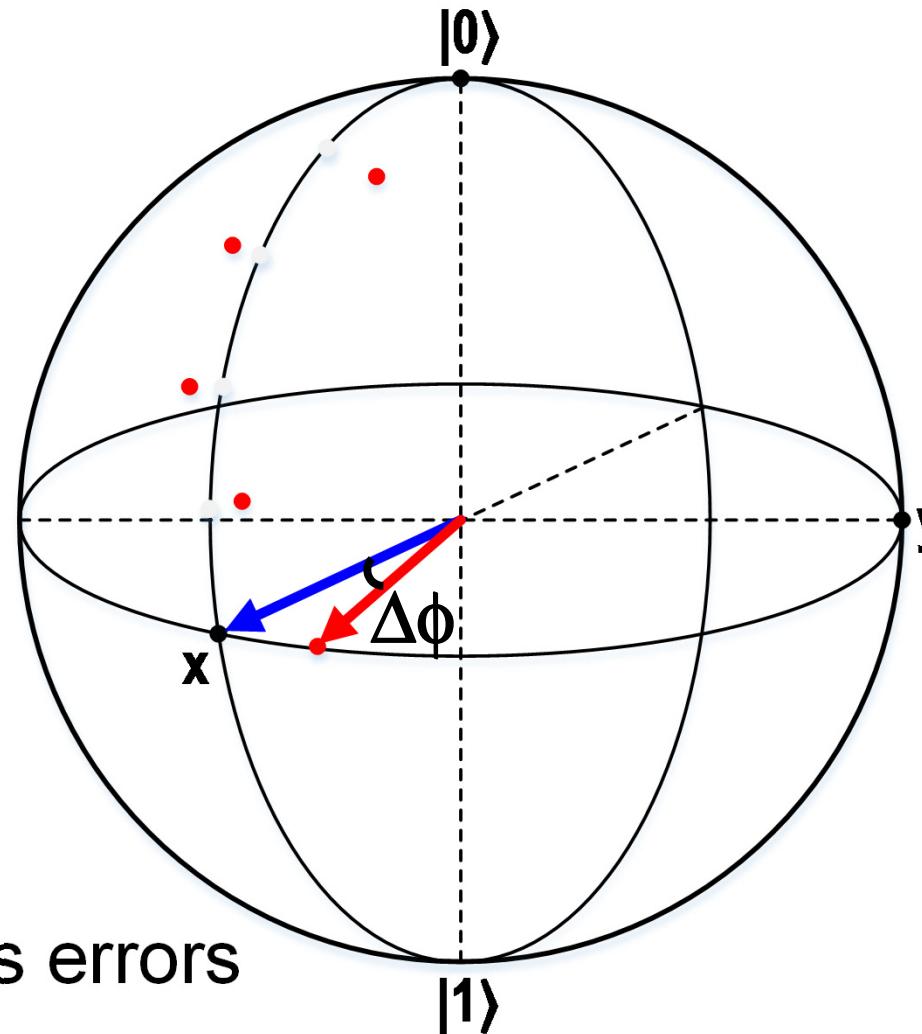
Qubit operation with a noisy oscillator



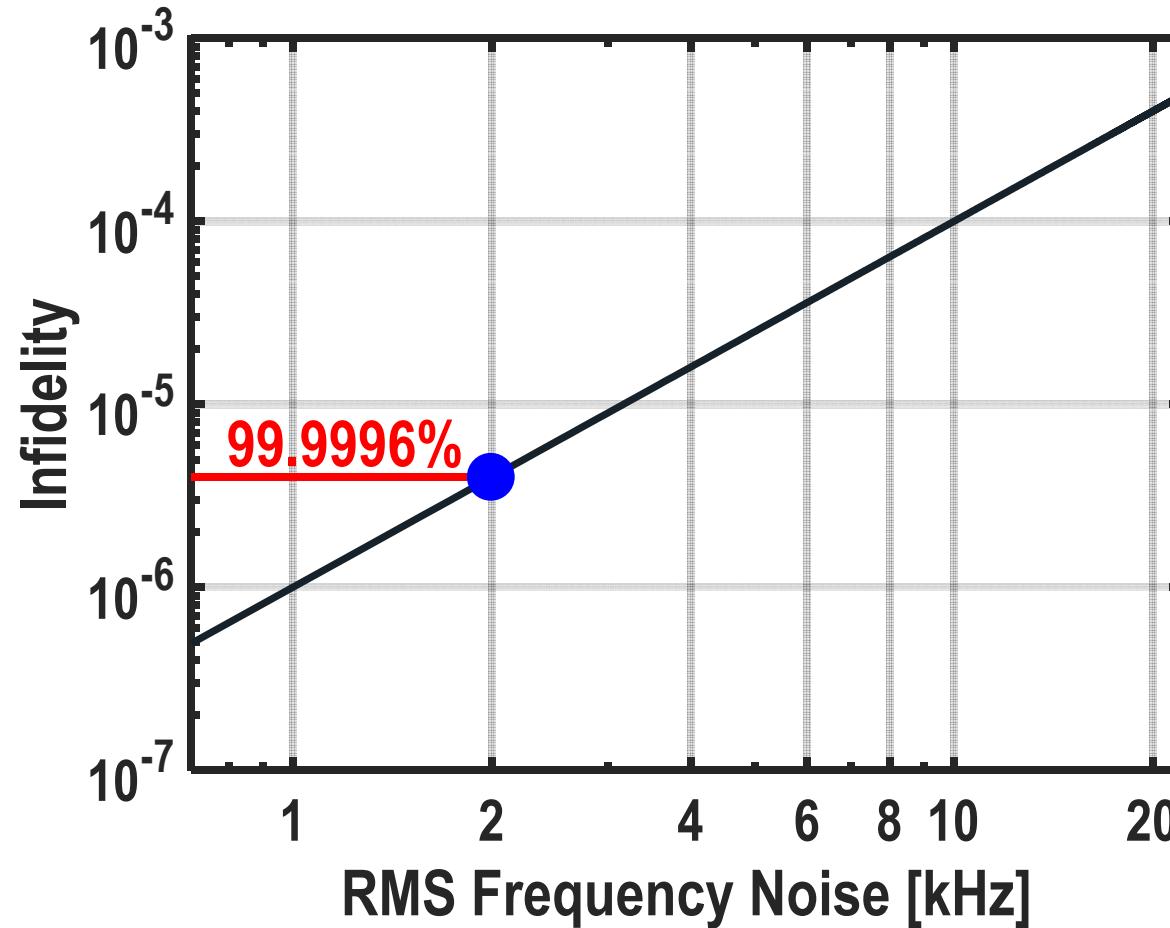
Qubit operation with a noisy oscillator



- Rotation axis deviates
- Oscillator noise introduces errors



Effect of frequency noise on qubit fidelity



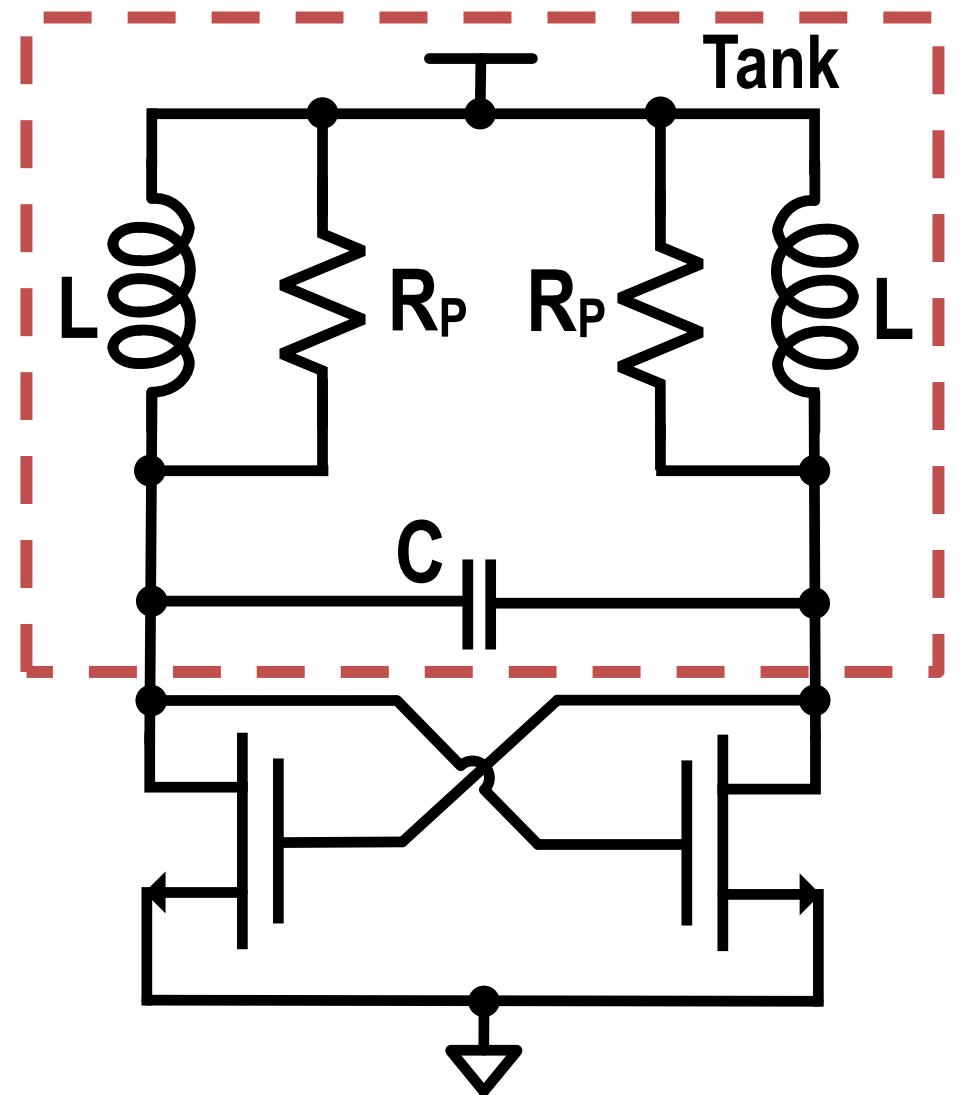
[van Dijk,
Phys. Rev. Applied 2019]

- ☐ Accurate qubit driving \Rightarrow Frequency noise $< 2\text{kHz}_{\text{rms}}$

Outline

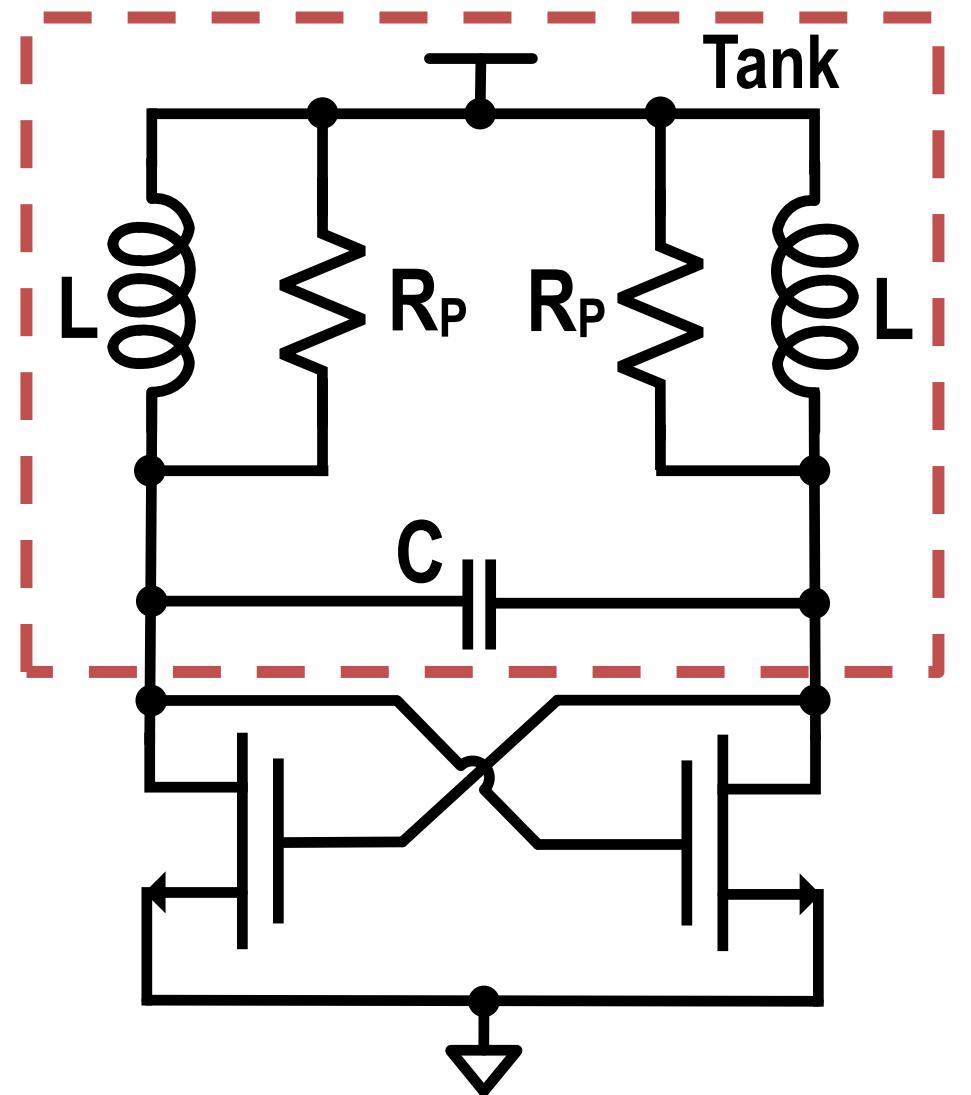
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- **Cryogenic Oscillators: Design Challenges**
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Phase noise in LC oscillators



$$\mathcal{L}(\Delta\omega) = 10\log_{10} \left[\frac{N_{TANK}(T) + N_{MOS}(T)}{8Q^2(T)V_{osc}^2} \left(\frac{\omega_0}{\Delta\omega} \right)^2 \right]$$

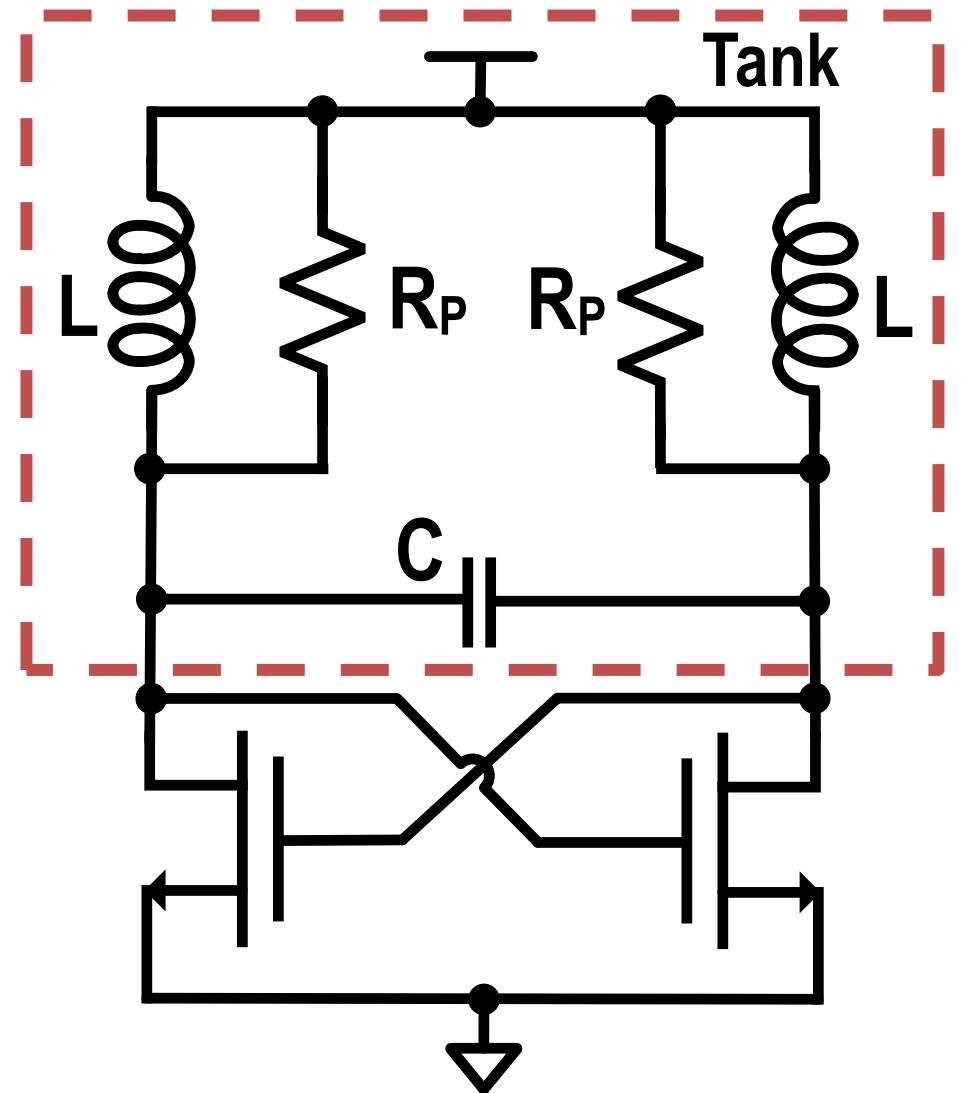
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□ $N_{TANK}(T) \propto 4kTR_P$

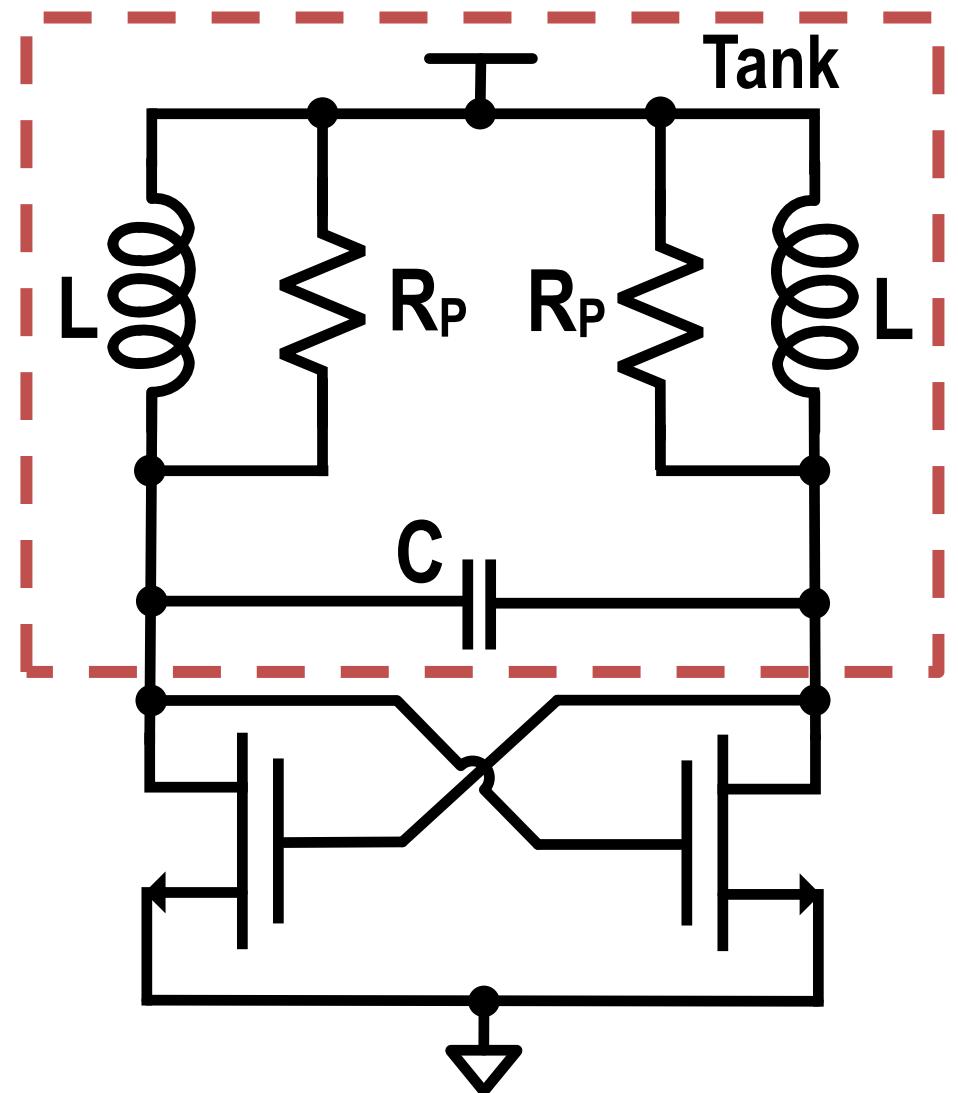
Phase noise in LC oscillators



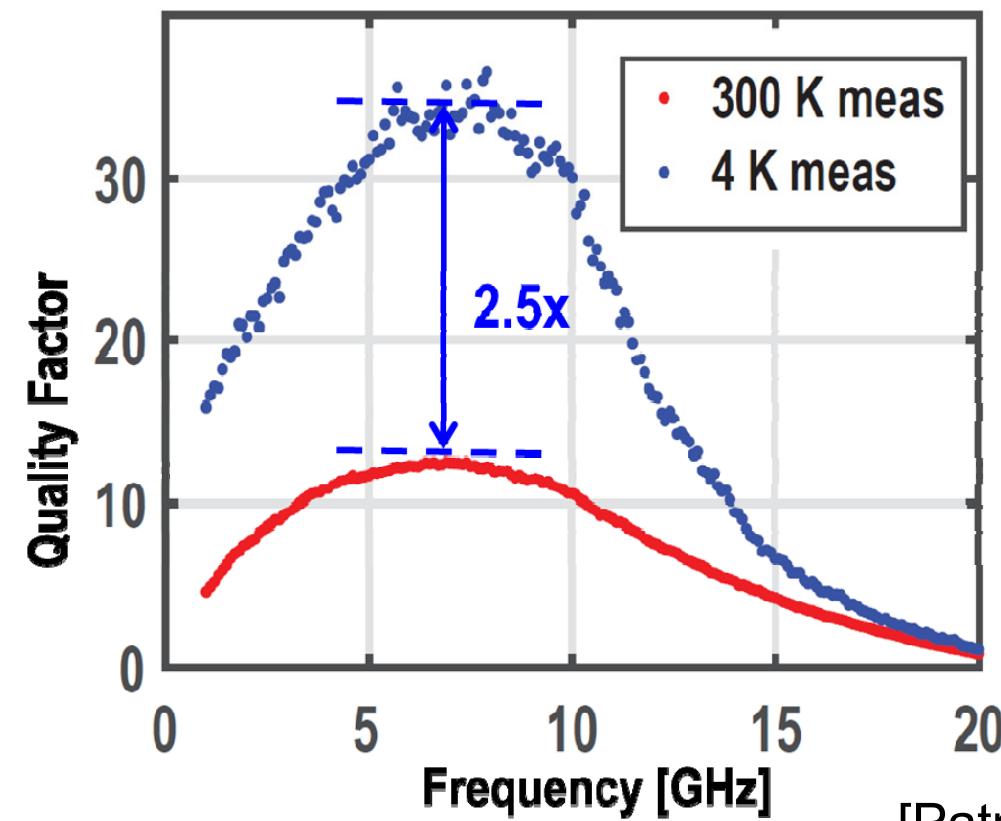
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- $N_{TANK}(T) \propto 4kTR_P$
- Negligible at cryogenic temperatures

Phase noise in LC oscillators

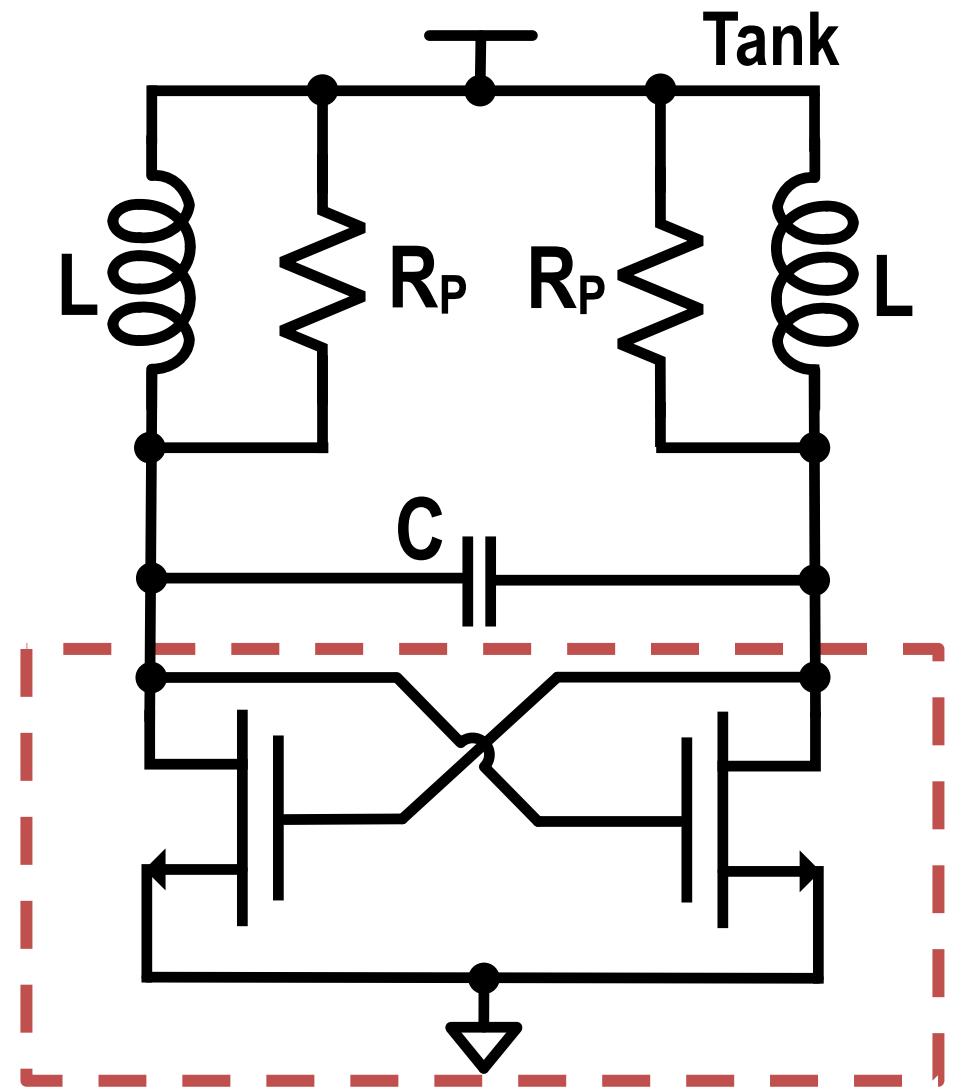


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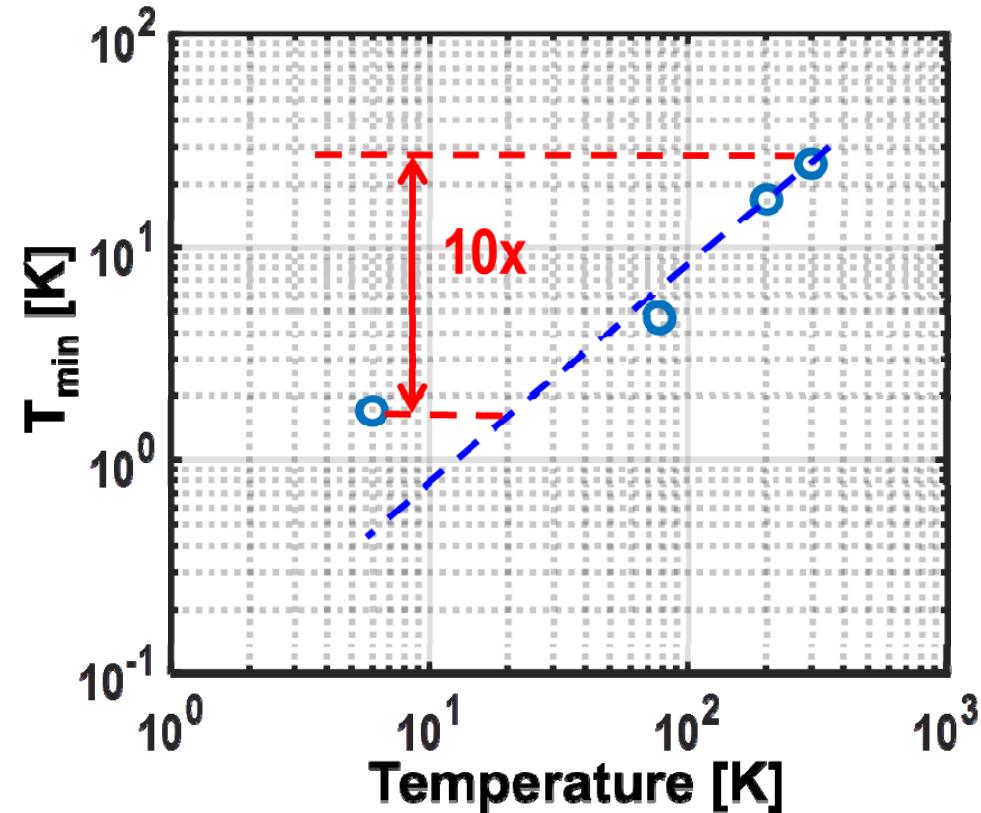


[Patra, arXiv'2019]

Phase noise in LC oscillators

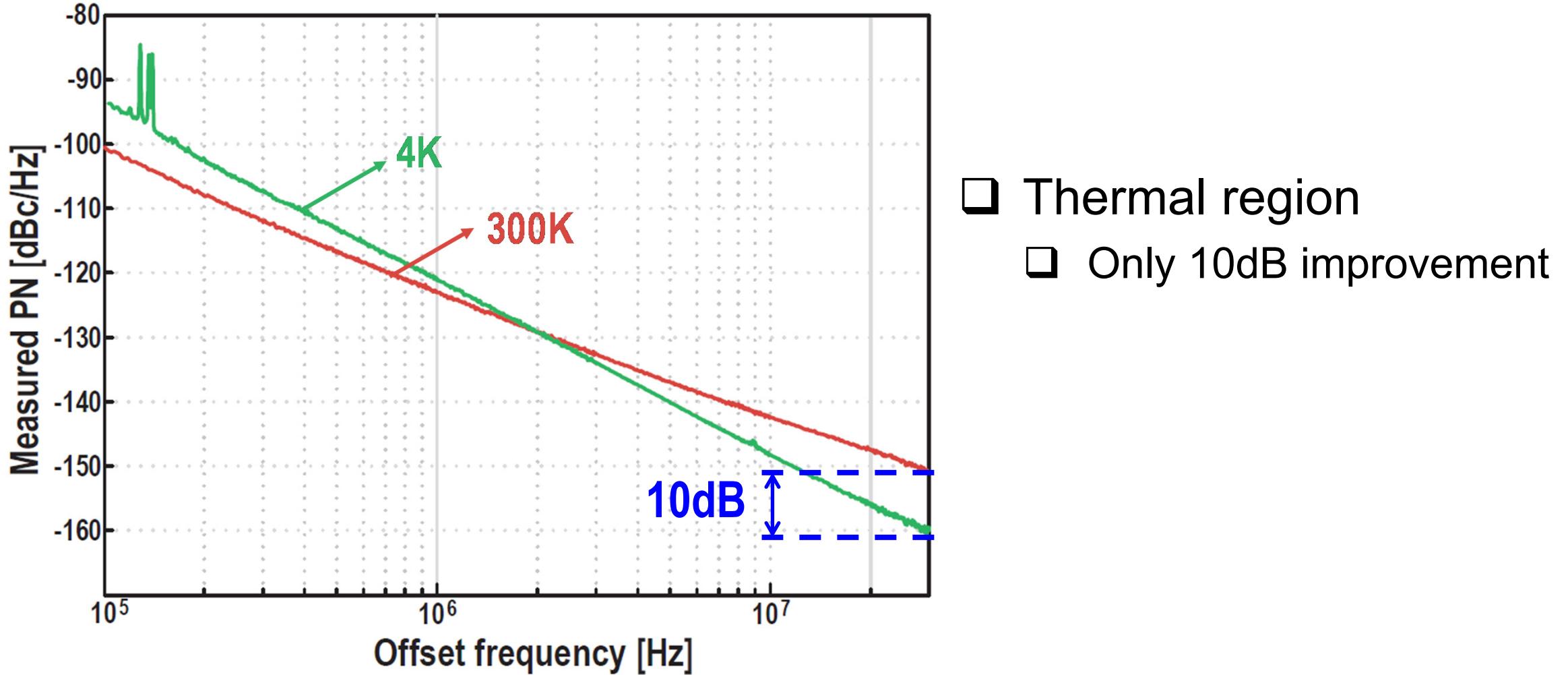


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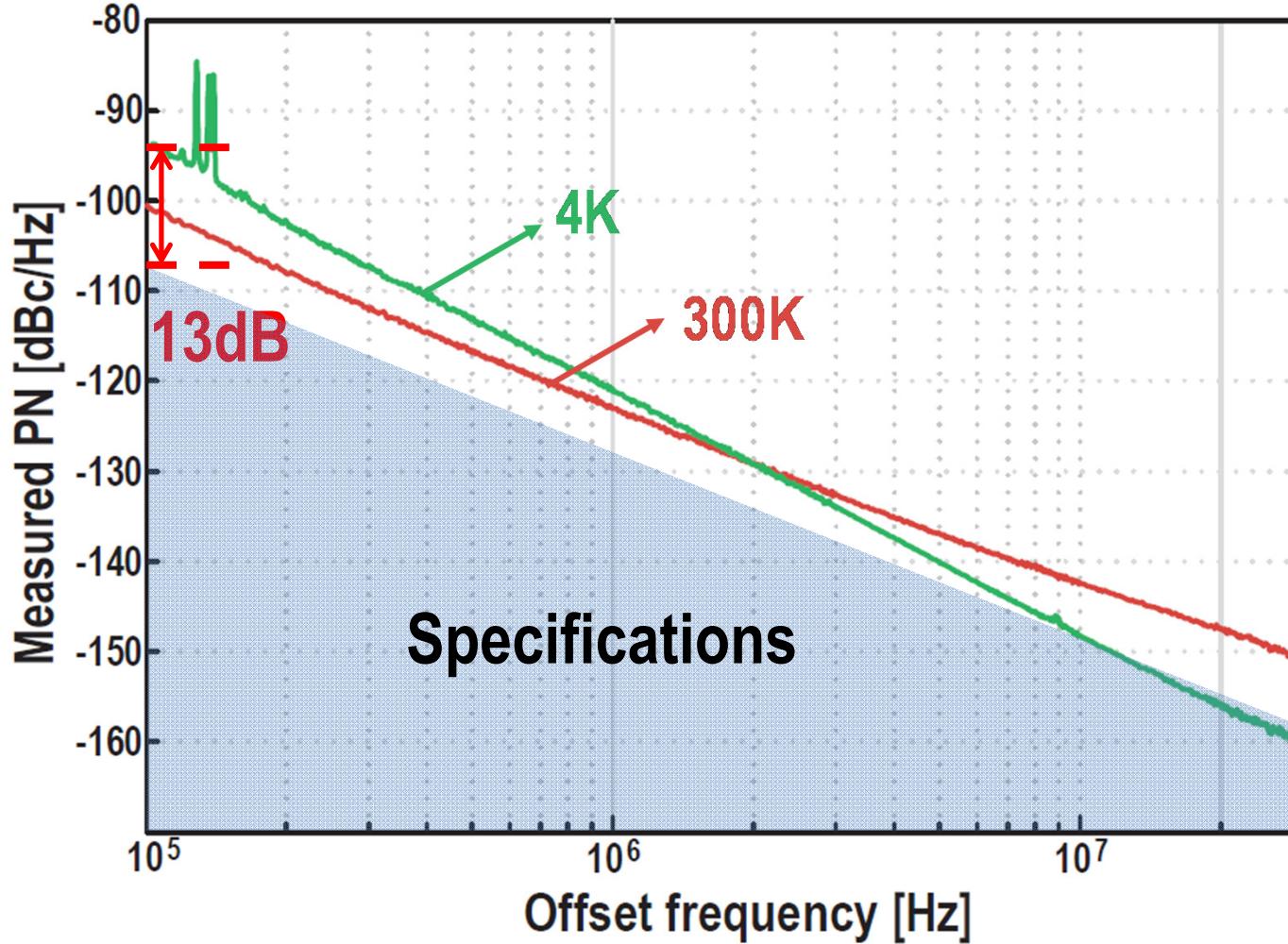
[Coskun, IMS'2014]

Phase noise in LC oscillators – Prior art



[Patra, JSSC'2018]

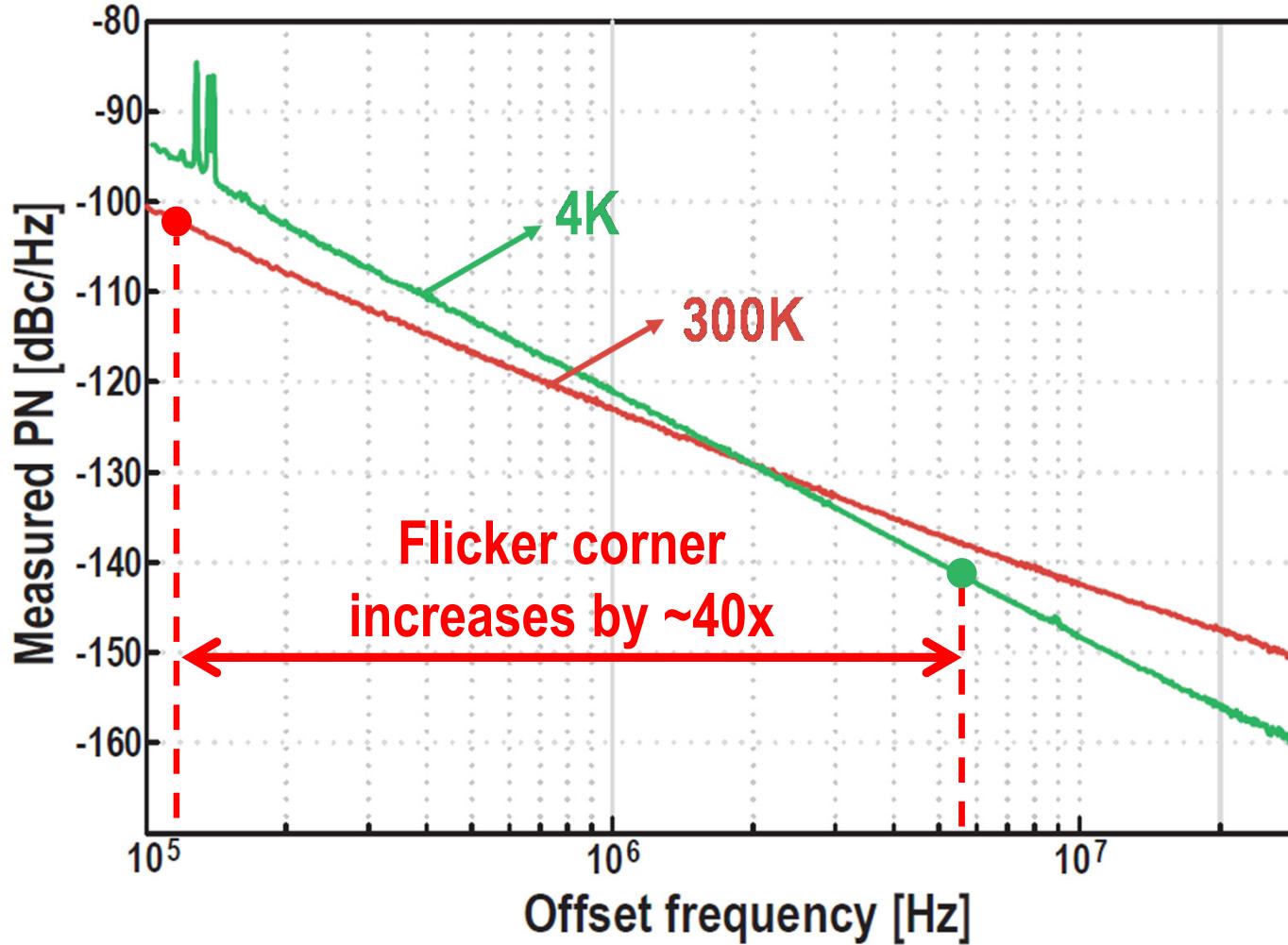
Phase noise in LC oscillators – Prior art



[Patra, JSSC'2018]

- Thermal region
 - Only 10dB improvement
- Low-frequency region
 - Degraded phase noise

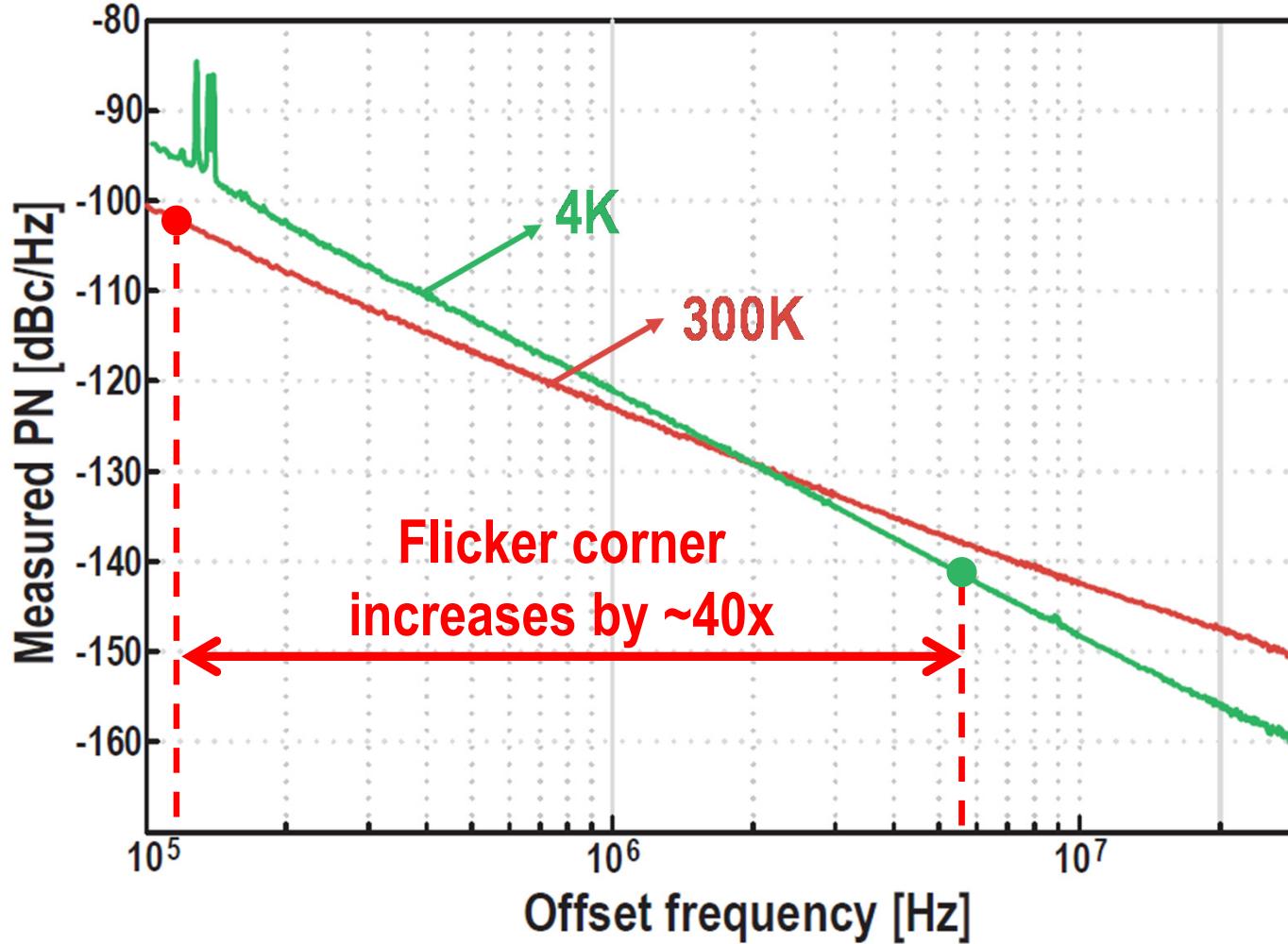
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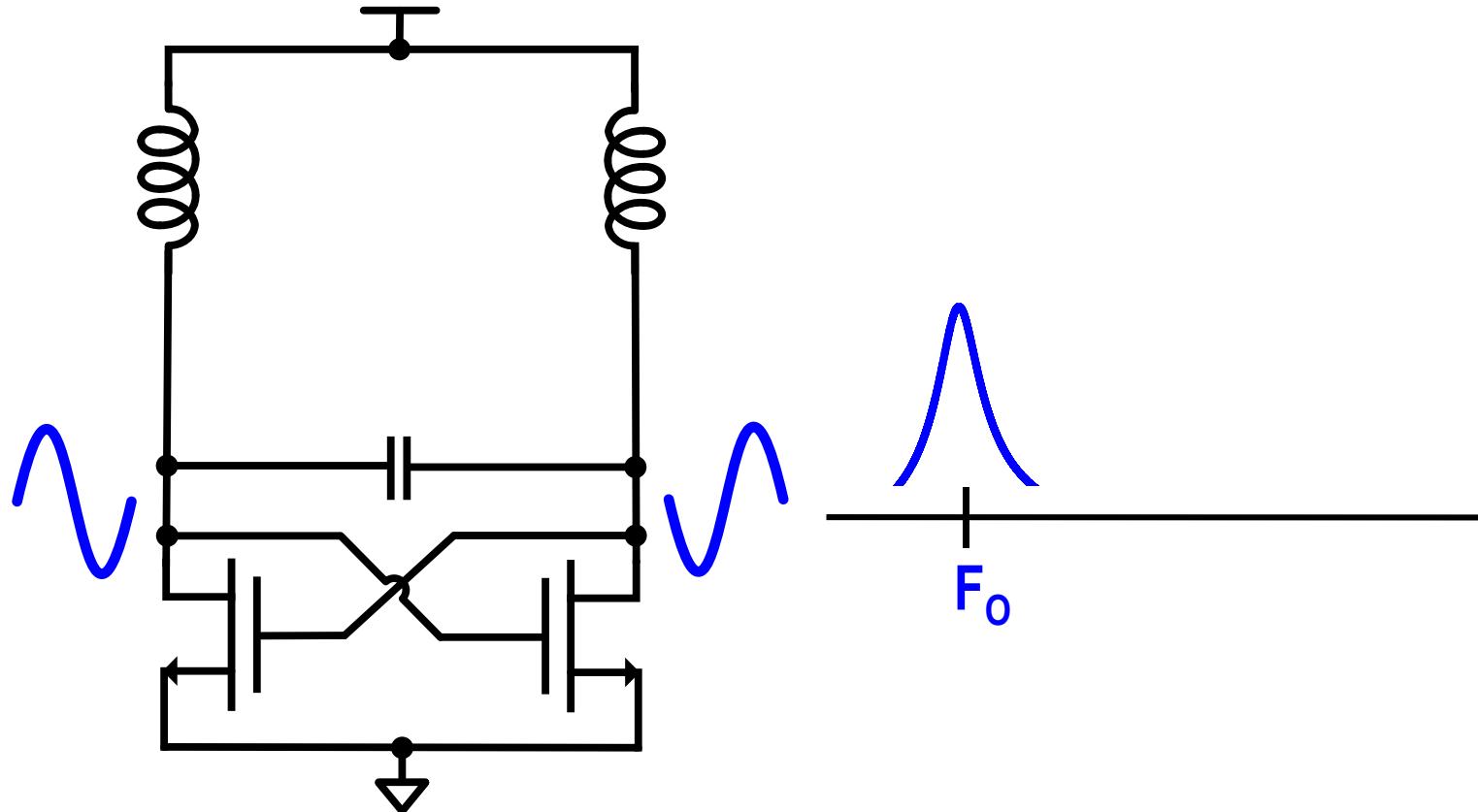
Phase noise in LC oscillators – Prior art



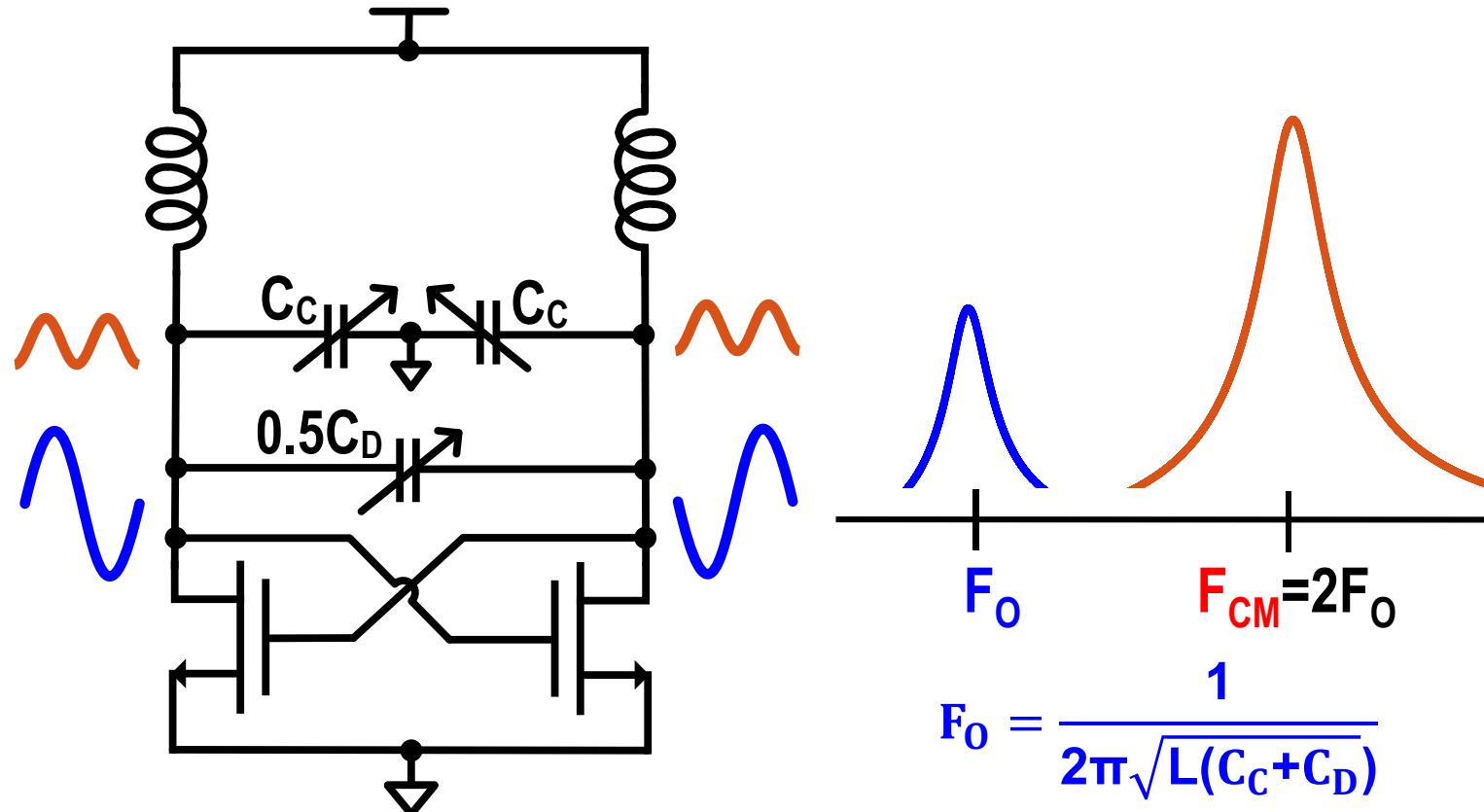
[Patra, JSSC'2018]

- Thermal region
 - Only 10dB improvement
- Low-frequency region
 - Degraded phase noise
 - Higher flicker corner
- Objective: Improve PN**

Traditional LC Oscillator



2nd Harmonic Common-Mode Resonance

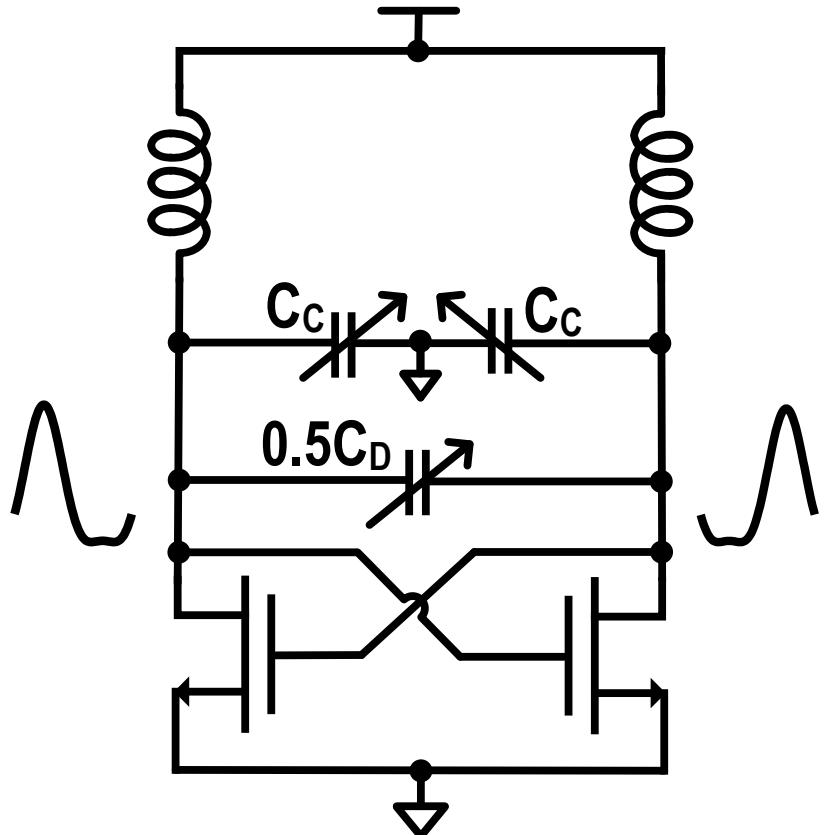


$$F_0 = \frac{1}{2\pi\sqrt{L(C_C+C_D)}}$$

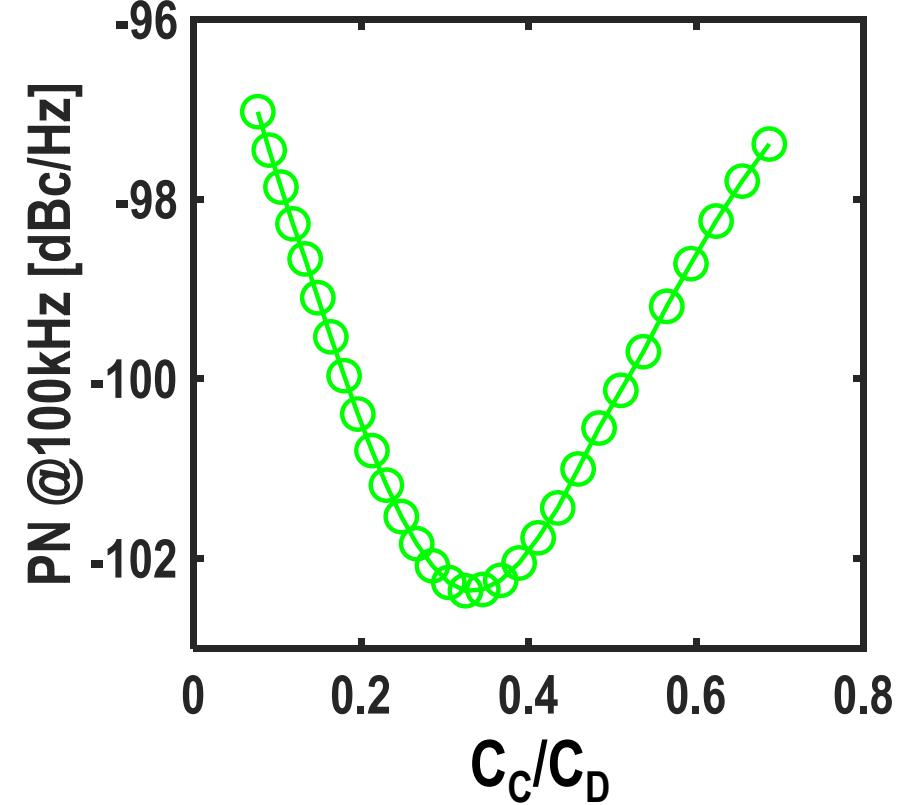
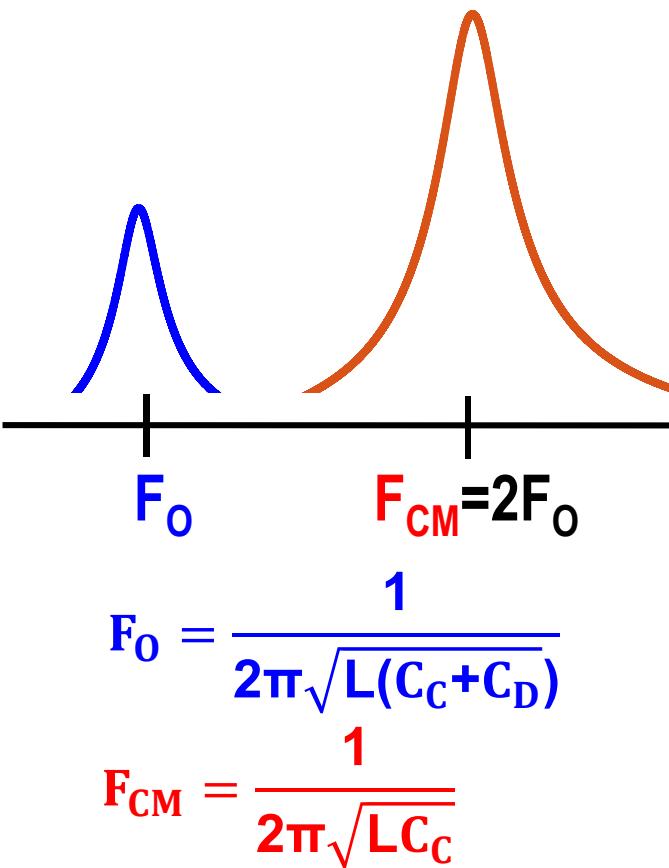
$$F_{CM} = \frac{1}{2\pi\sqrt{LC_C}}$$

[Shahmohammadi, ISSCC'2015]
[Murphy, ISSCC'2015]

2nd Harmonic Common-Mode Resonance

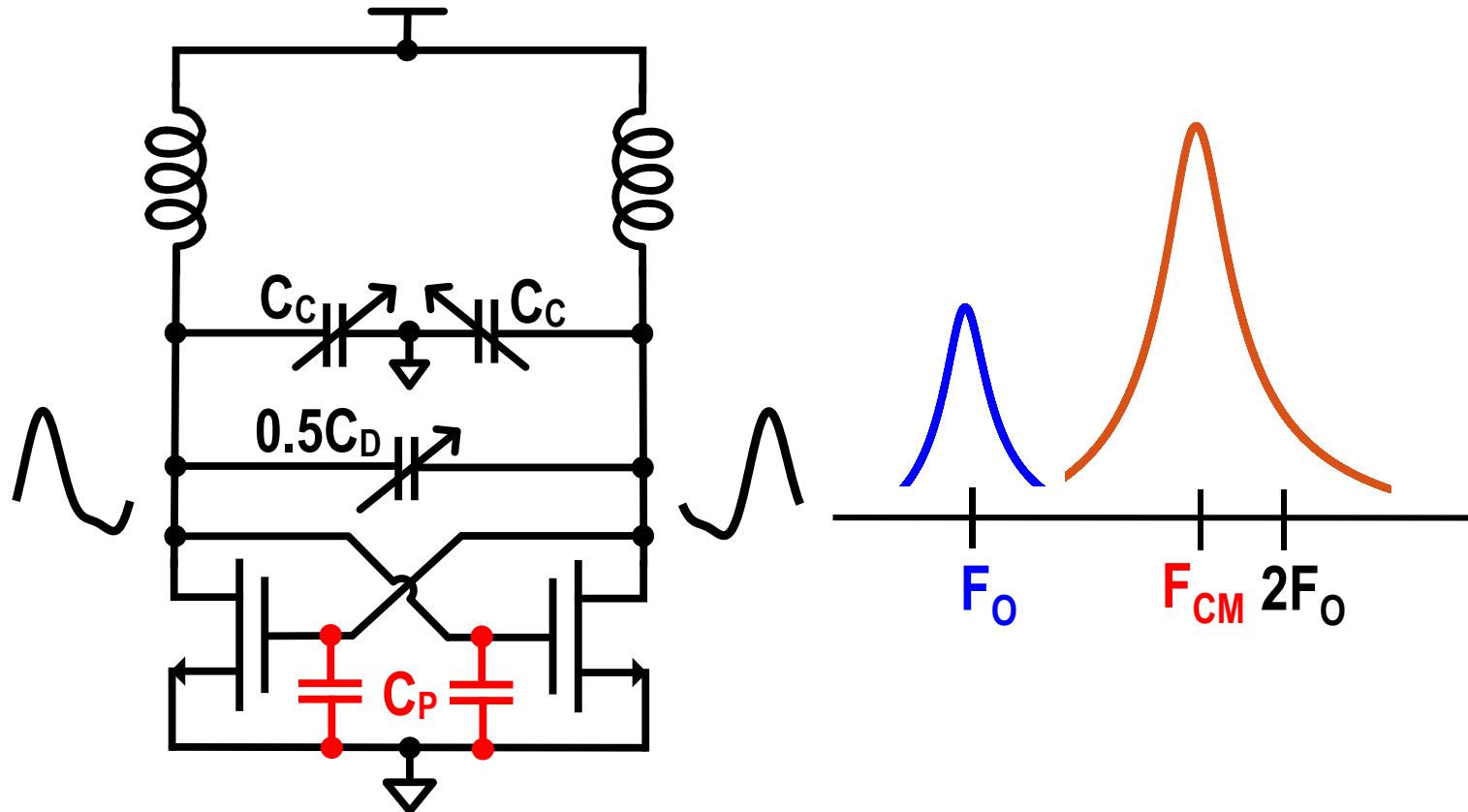


Optimum C_C/C_D
⇒ Lowest phase noise

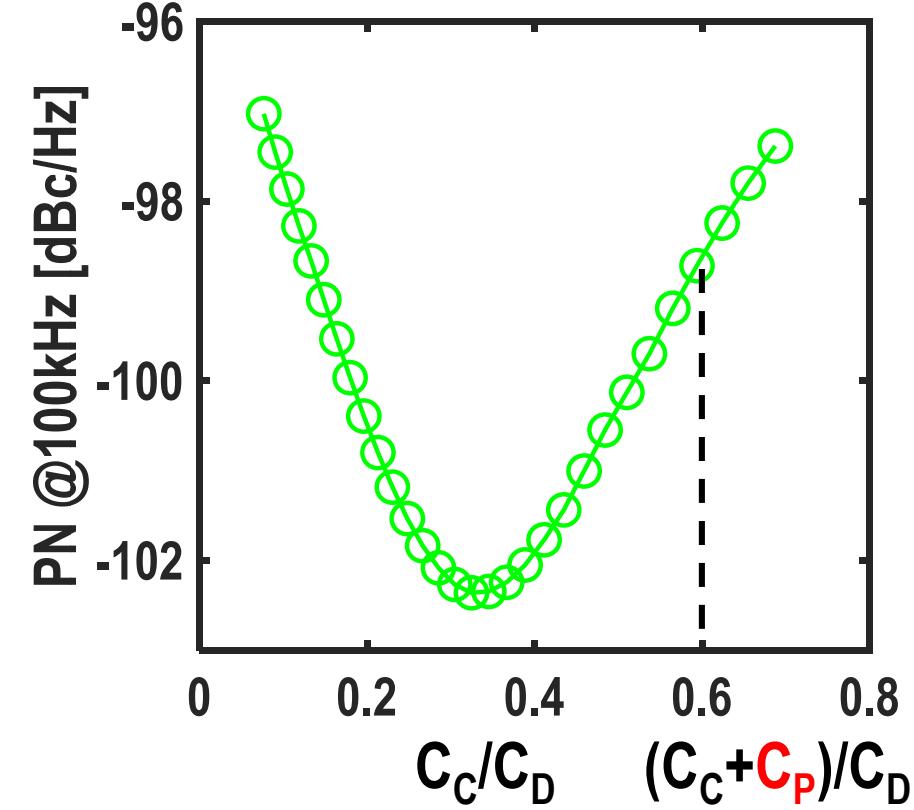


[Shahmohammadi, ISSCC'2015]
[Murphy, ISSCC'2015]

2nd Harmonic Common-Mode Resonance

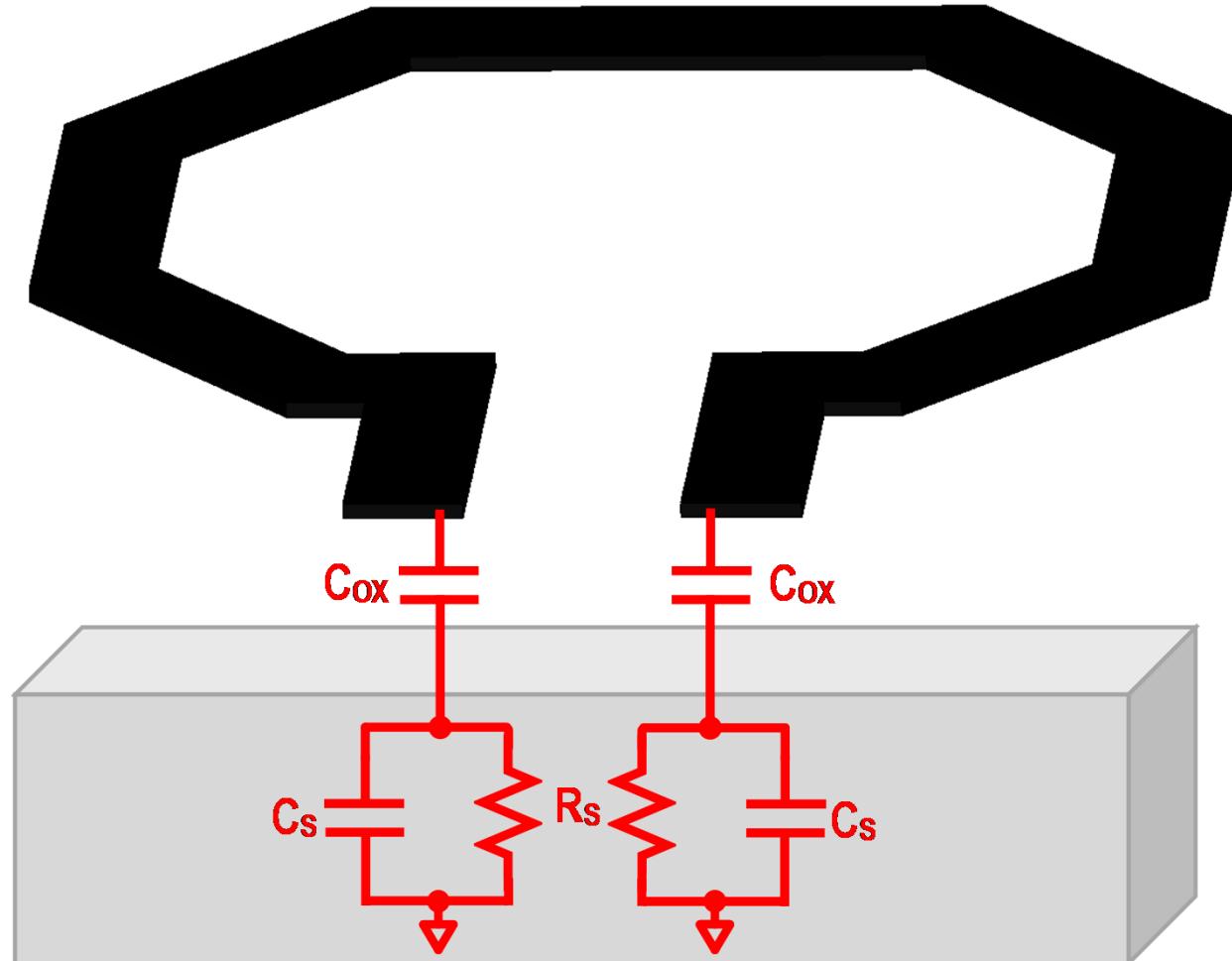


- C_C/C_D is PVT dependent
⇒ phase noise degradation



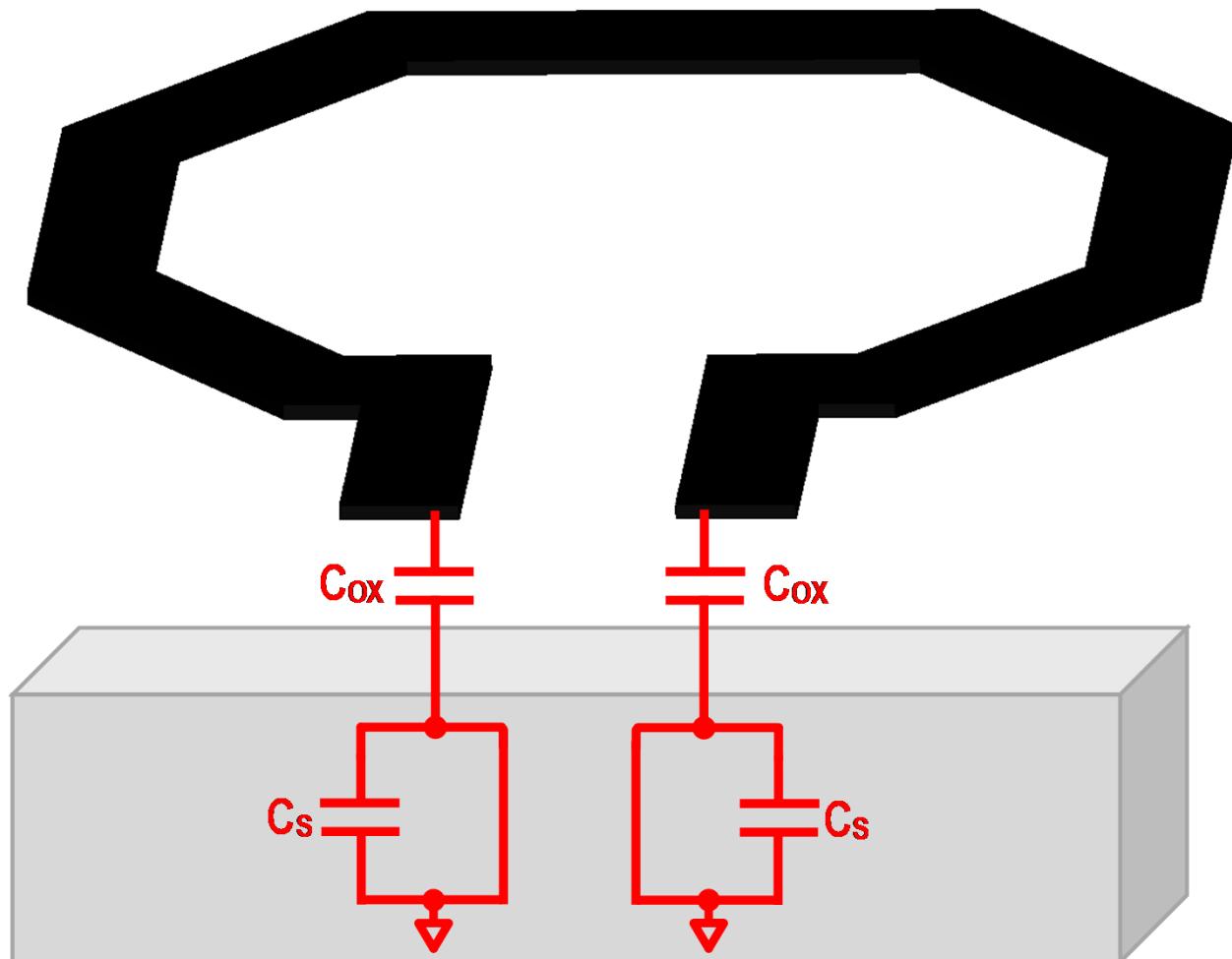
[Shahmohammadi, ISSCC'2015]
[Murphy, ISSCC'2015]

Effect of temperature on C_p



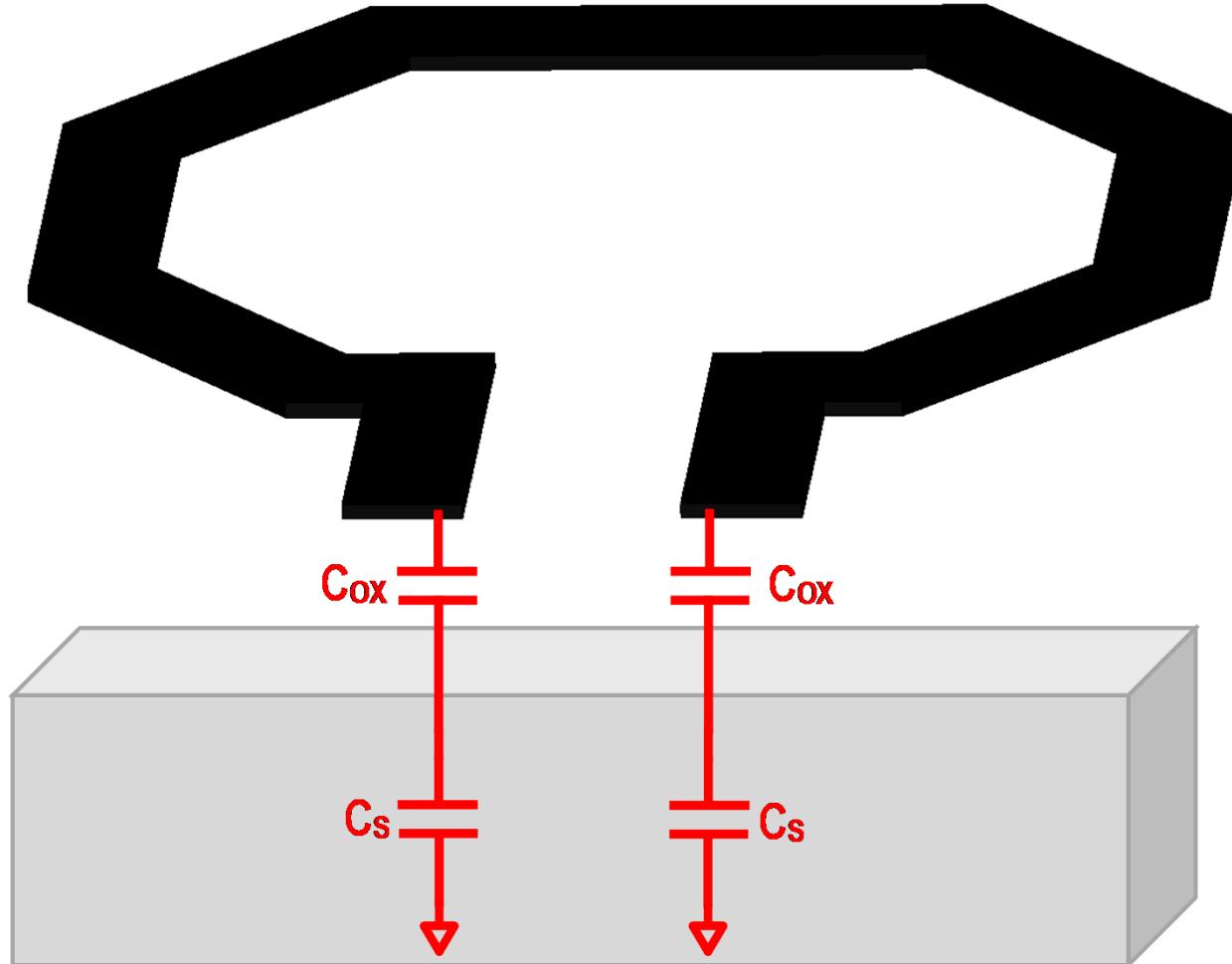
19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Effect of temperature on C_P



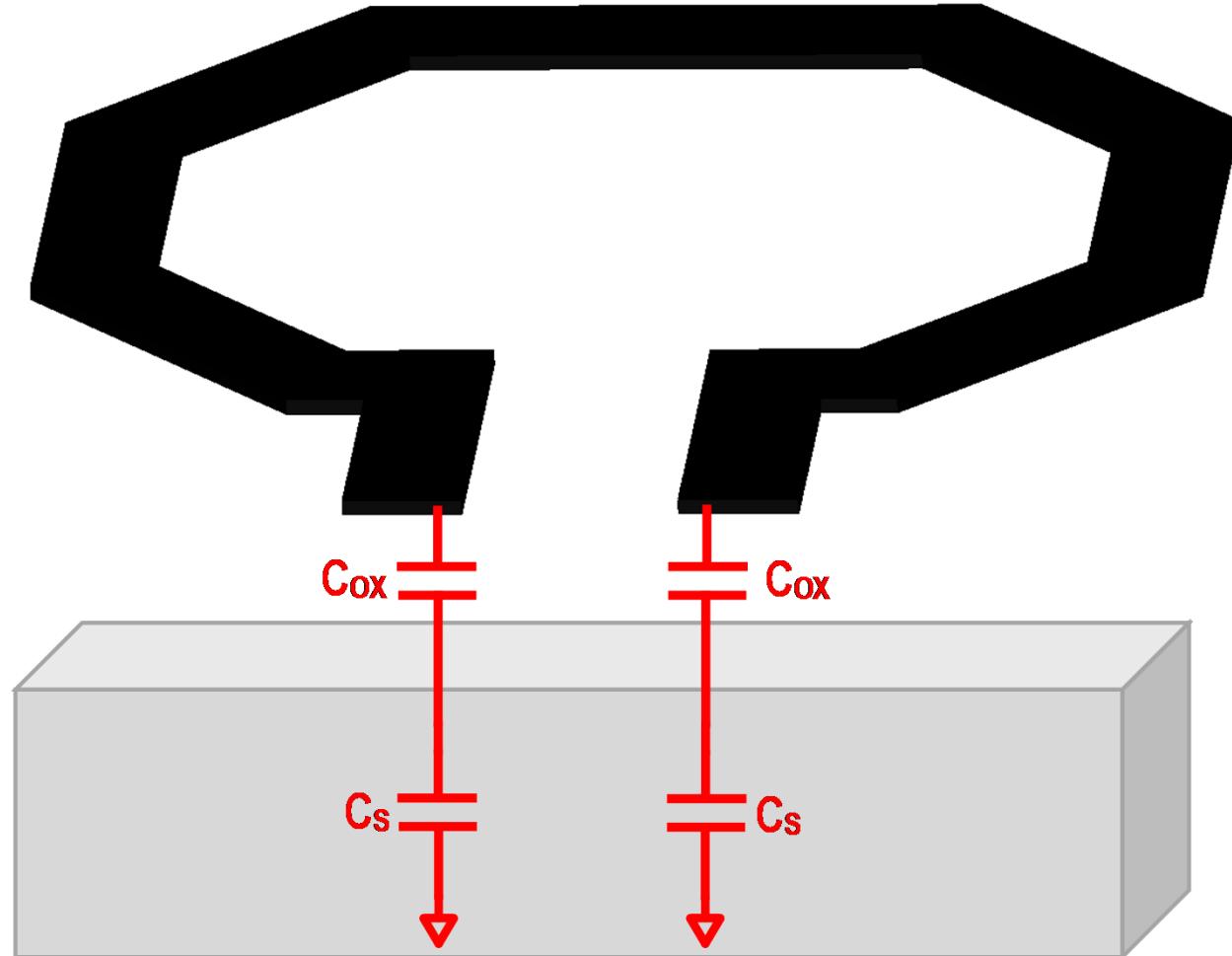
- Low resistivity substrate at 300K
 - $C_P \approx C_{ox}$

Effect of temperature on C_P



- Low resistivity substrate at 300K
 - $C_P \approx C_{ox}$
- Carrier freeze-out at 4K
 - $C_P \approx C_{ox} \parallel C_s \approx C_s$

Effect of temperature on C_P

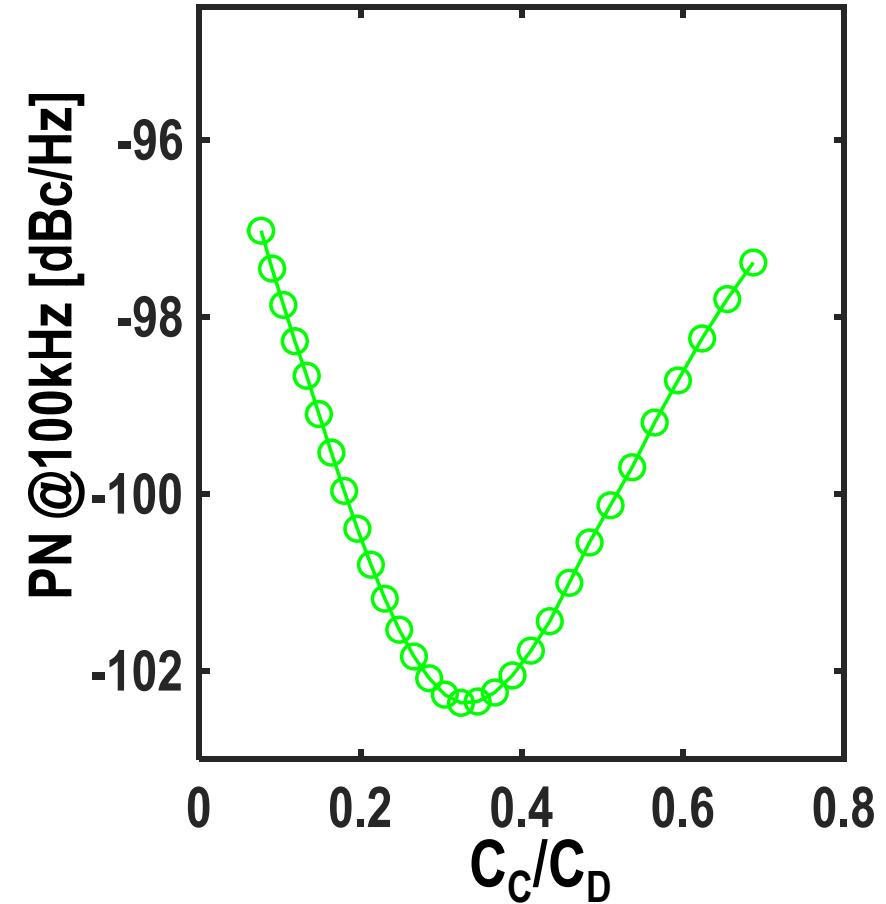
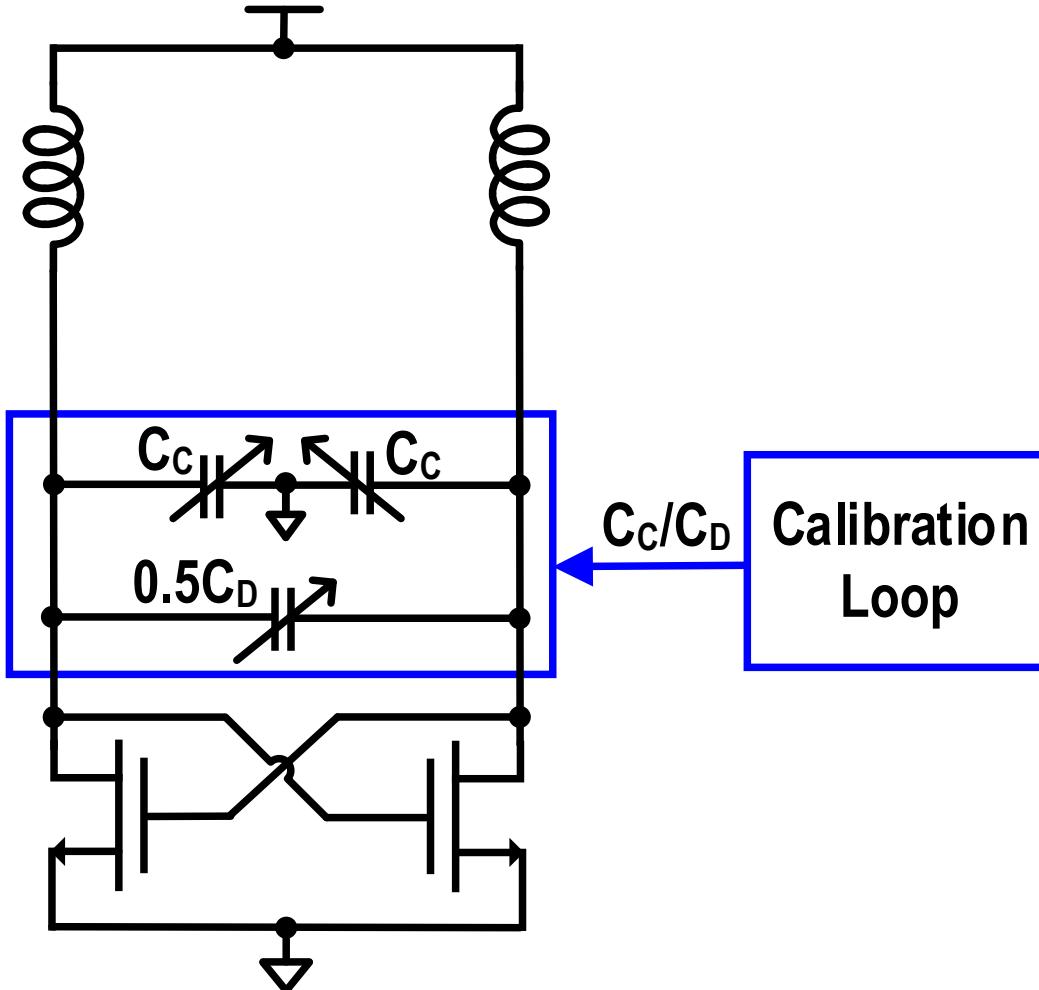


- Low resistivity substrate at 300K
 - $C_P \approx C_{ox}$
- Carrier freeze-out at 4K
 - $C_P \approx C_{ox} \parallel C_s \approx C_s$
- Calibration is required**

Outline

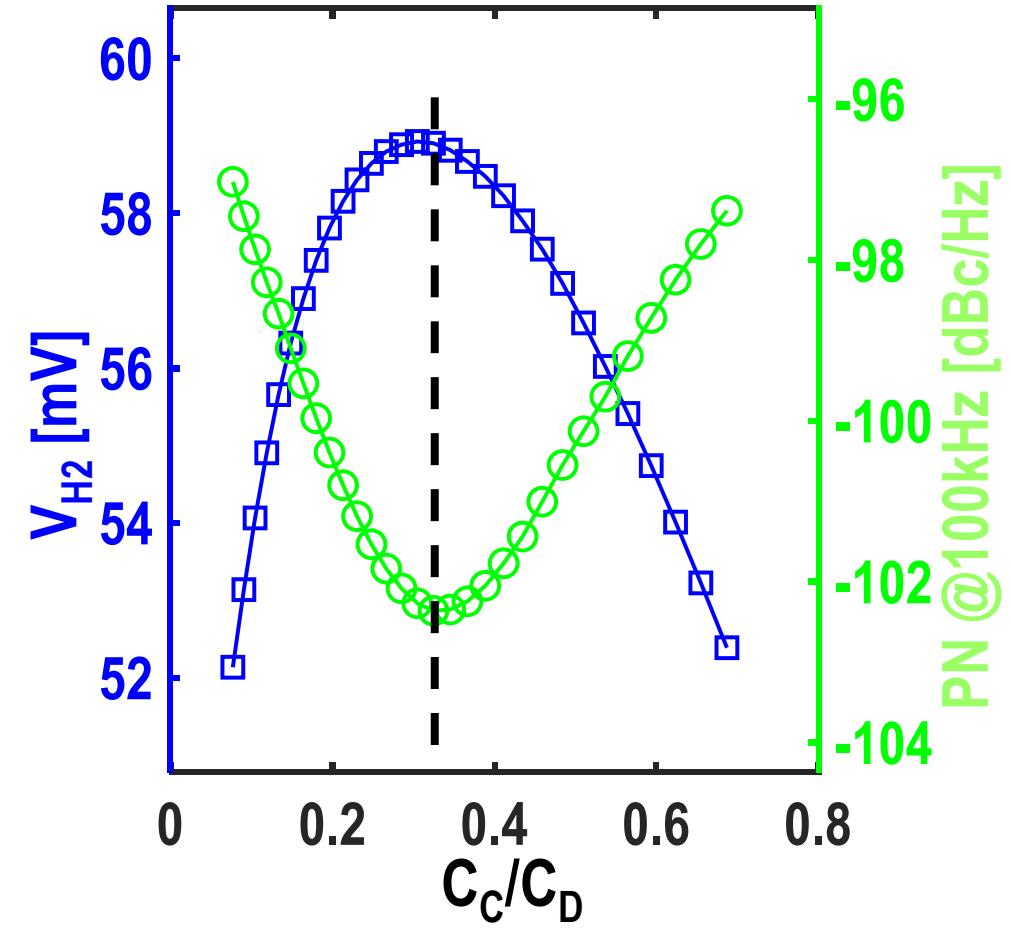
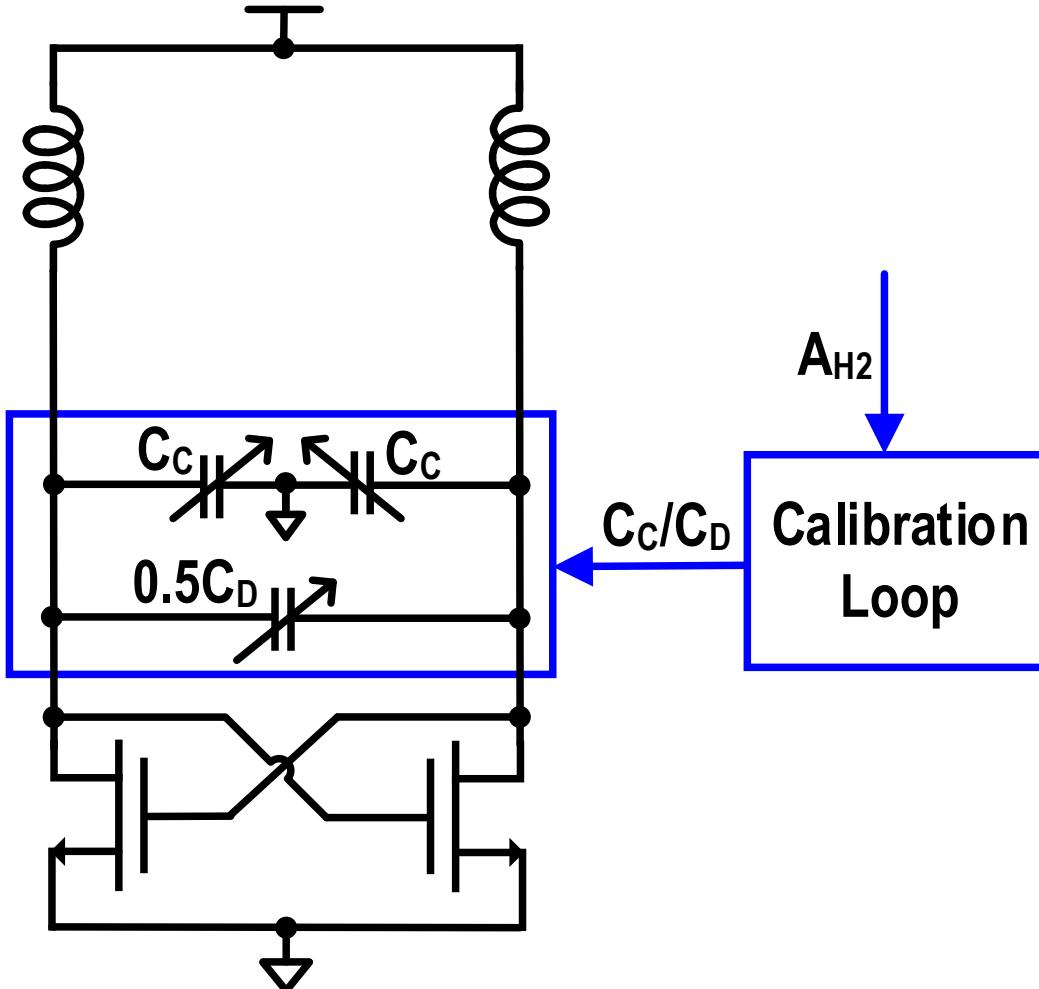
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Calibration – Force & Sense



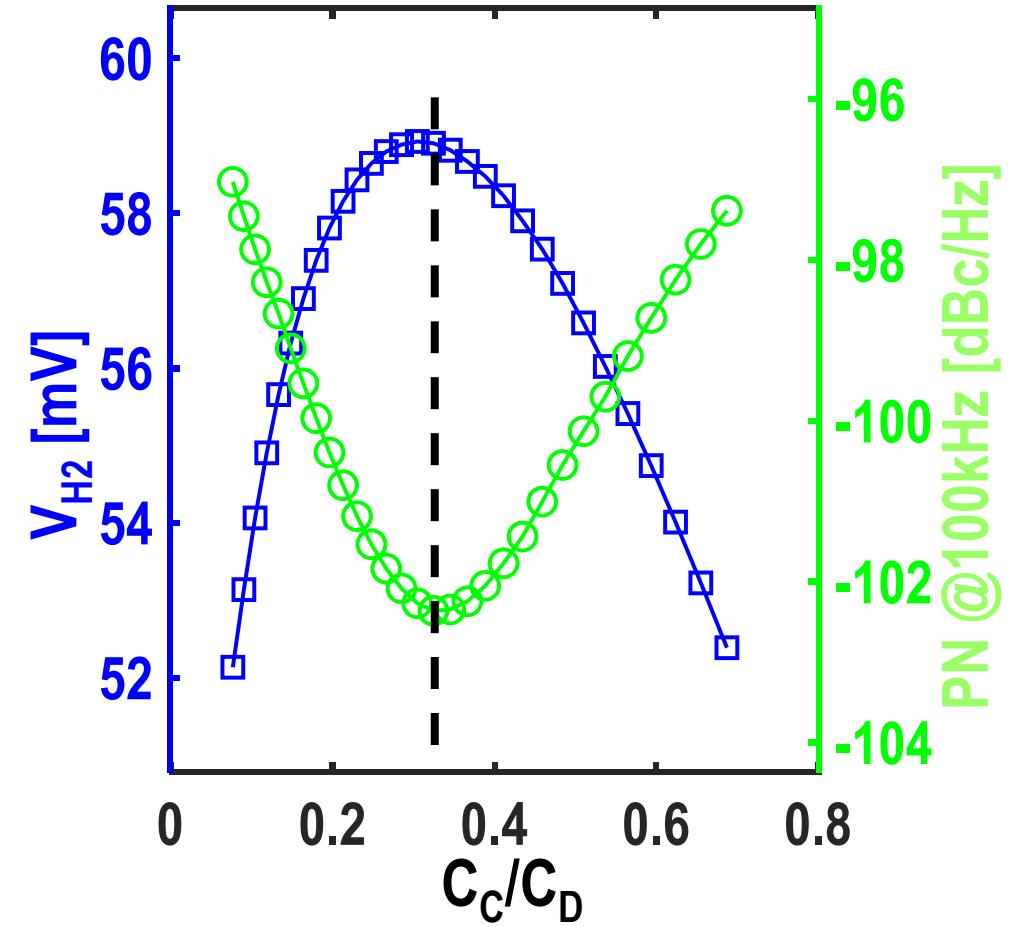
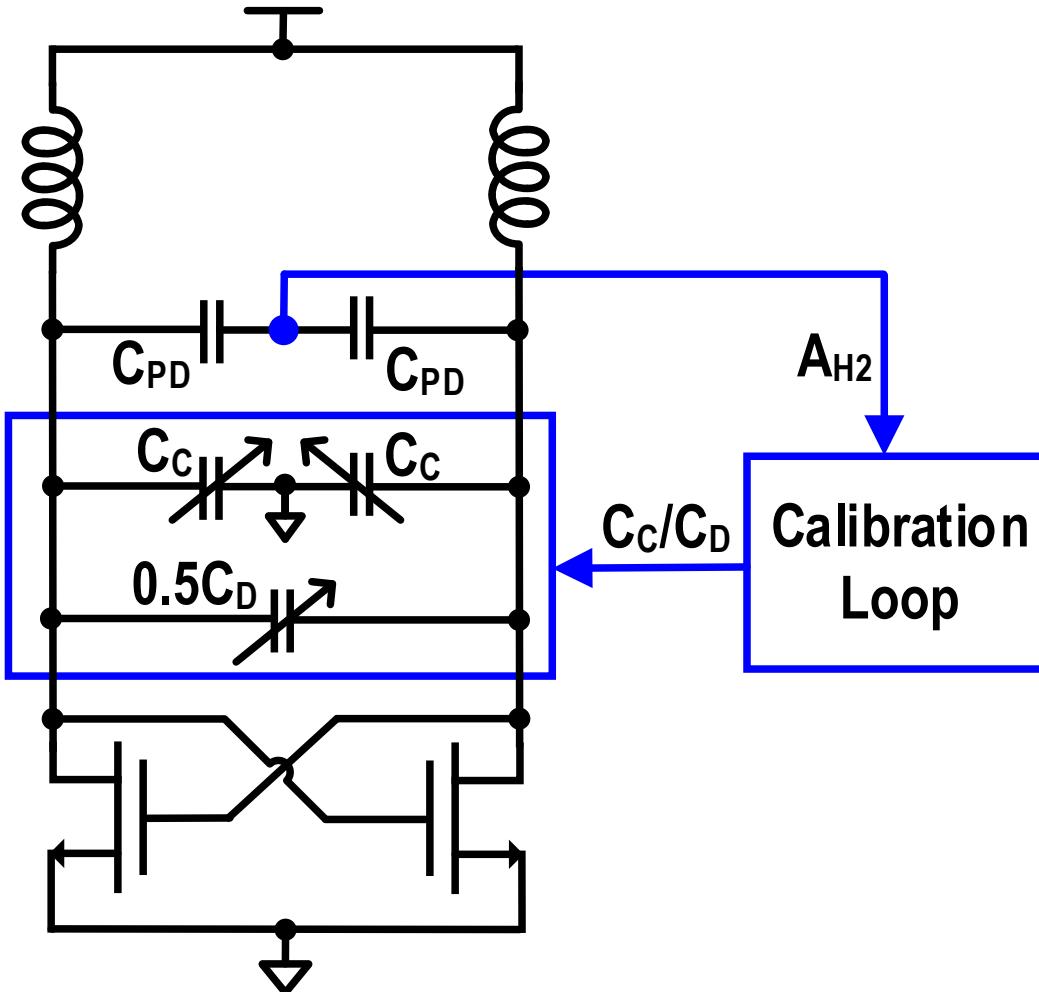
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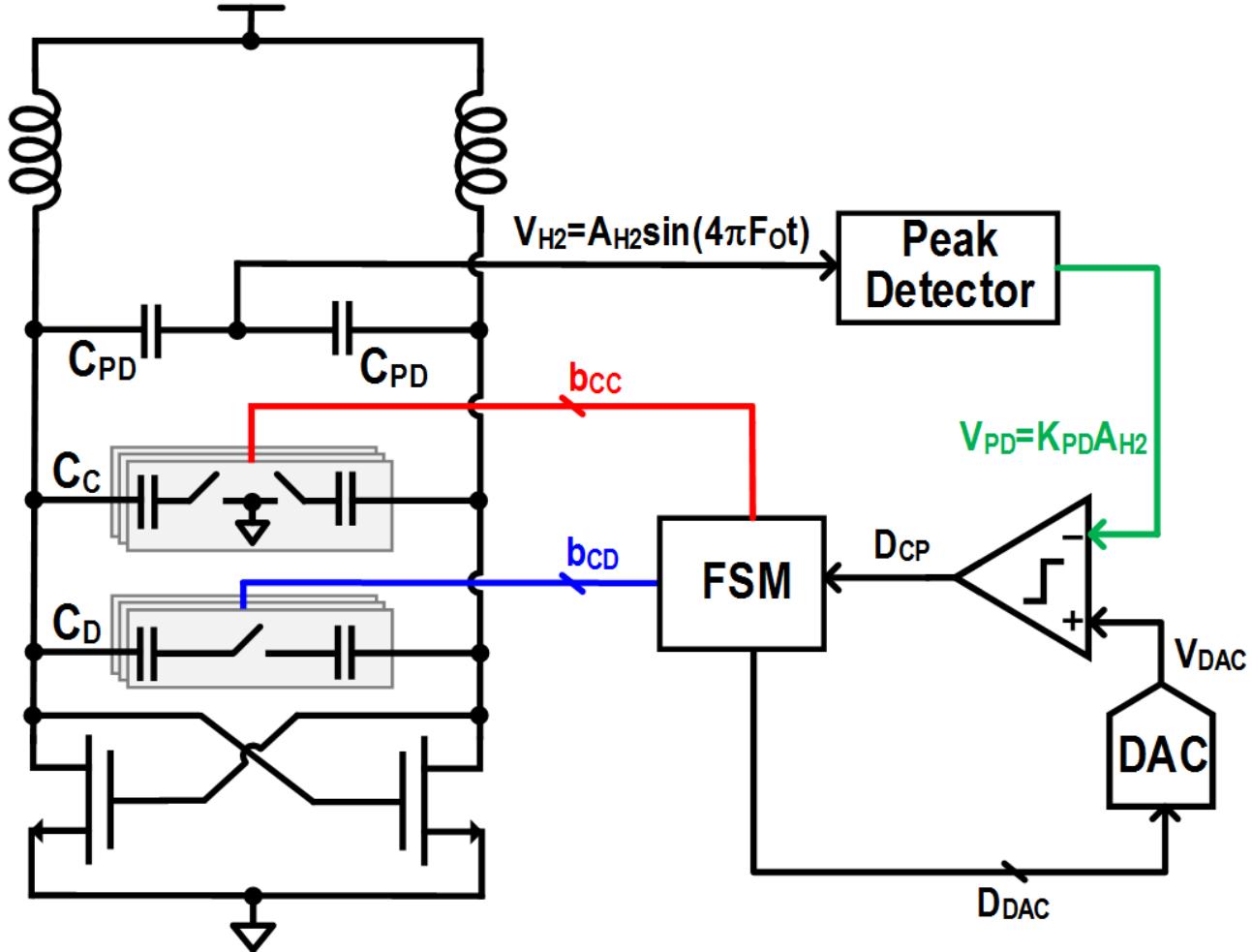
- Maximum A_{H2} and minimum phase noise at the same C_C/C_D

Calibration – Force & Sense

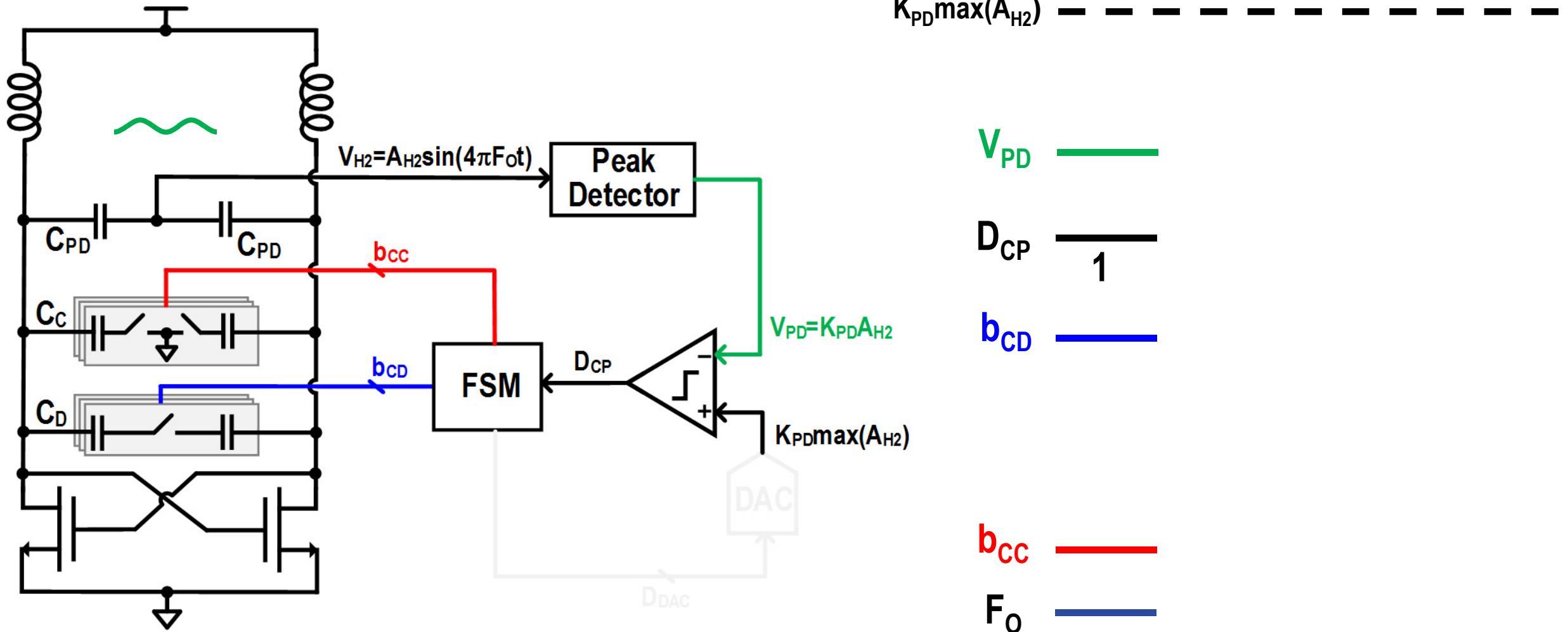


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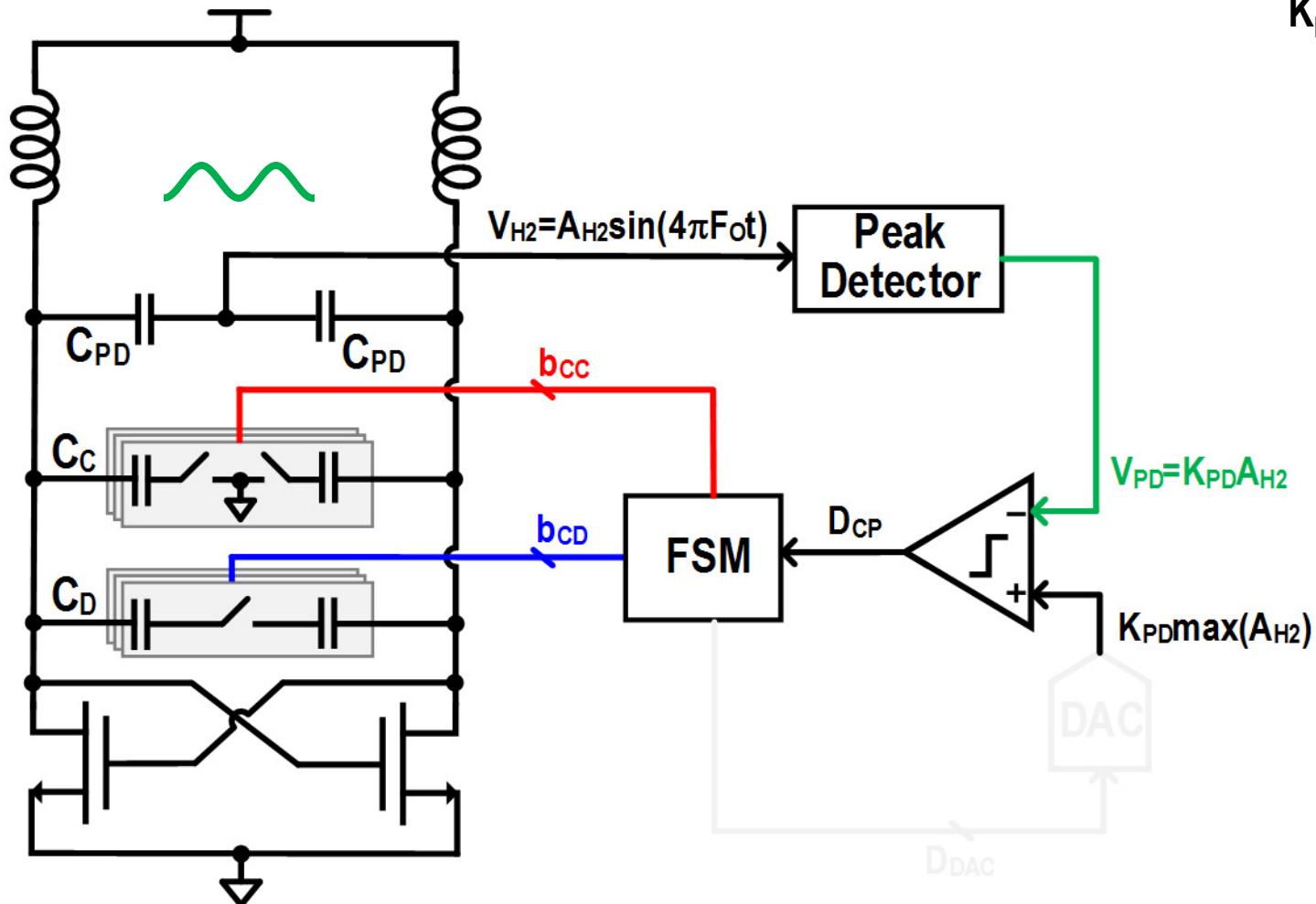
Calibration loop



Calibration loop



Calibration loop



$K_{PDmax}(A_{H2})$ ——————

V_{PD}

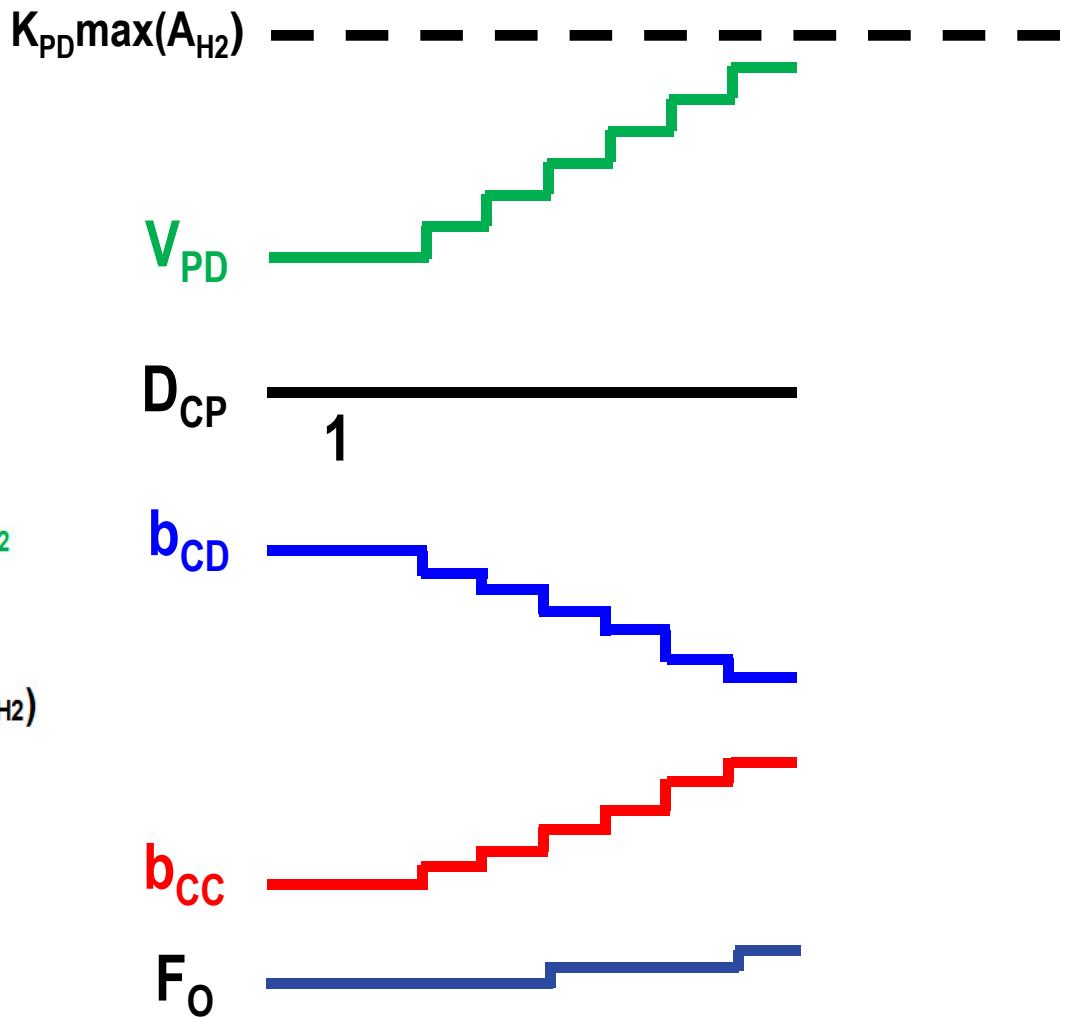
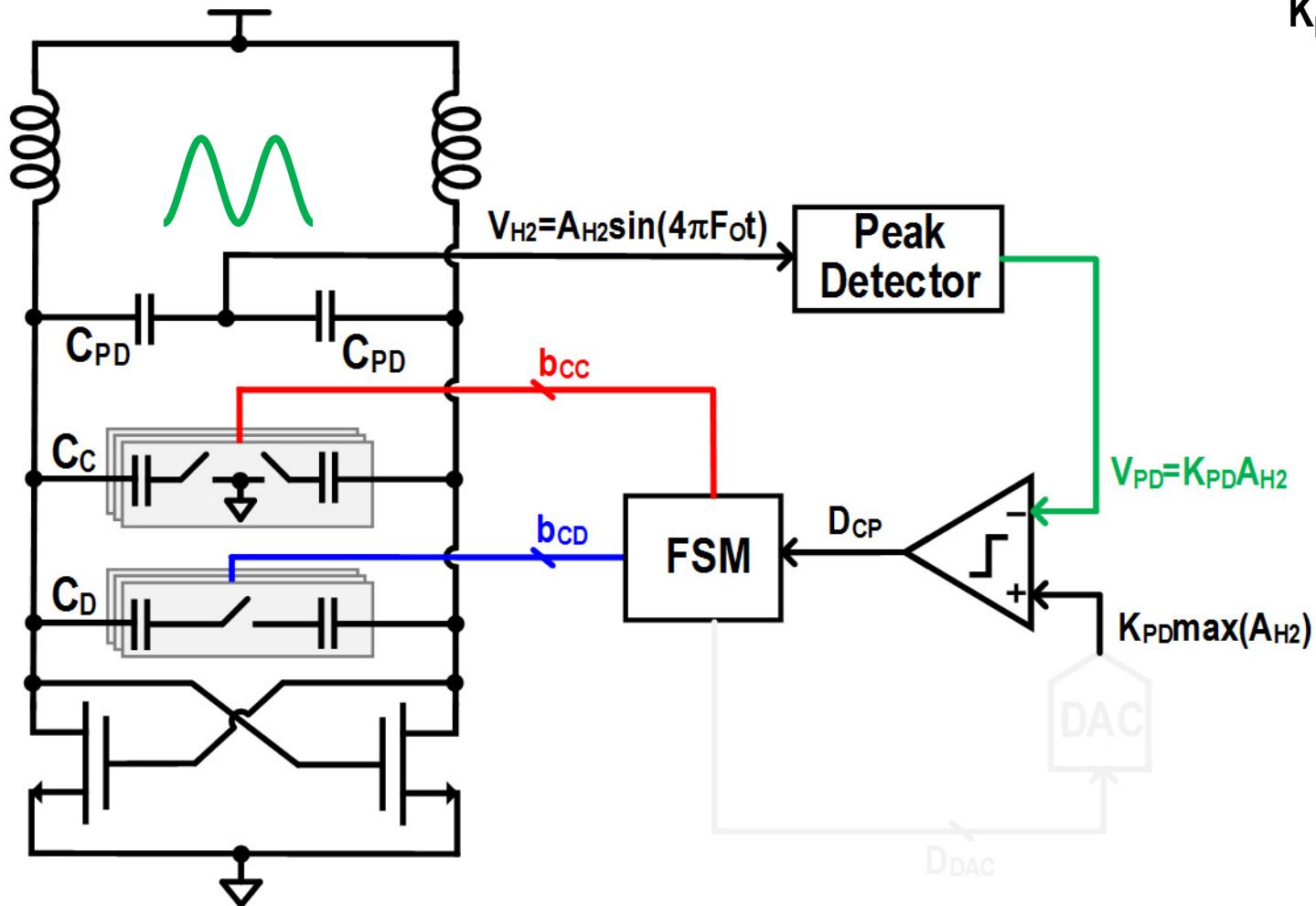
D_{CP} 1

b_{CD}

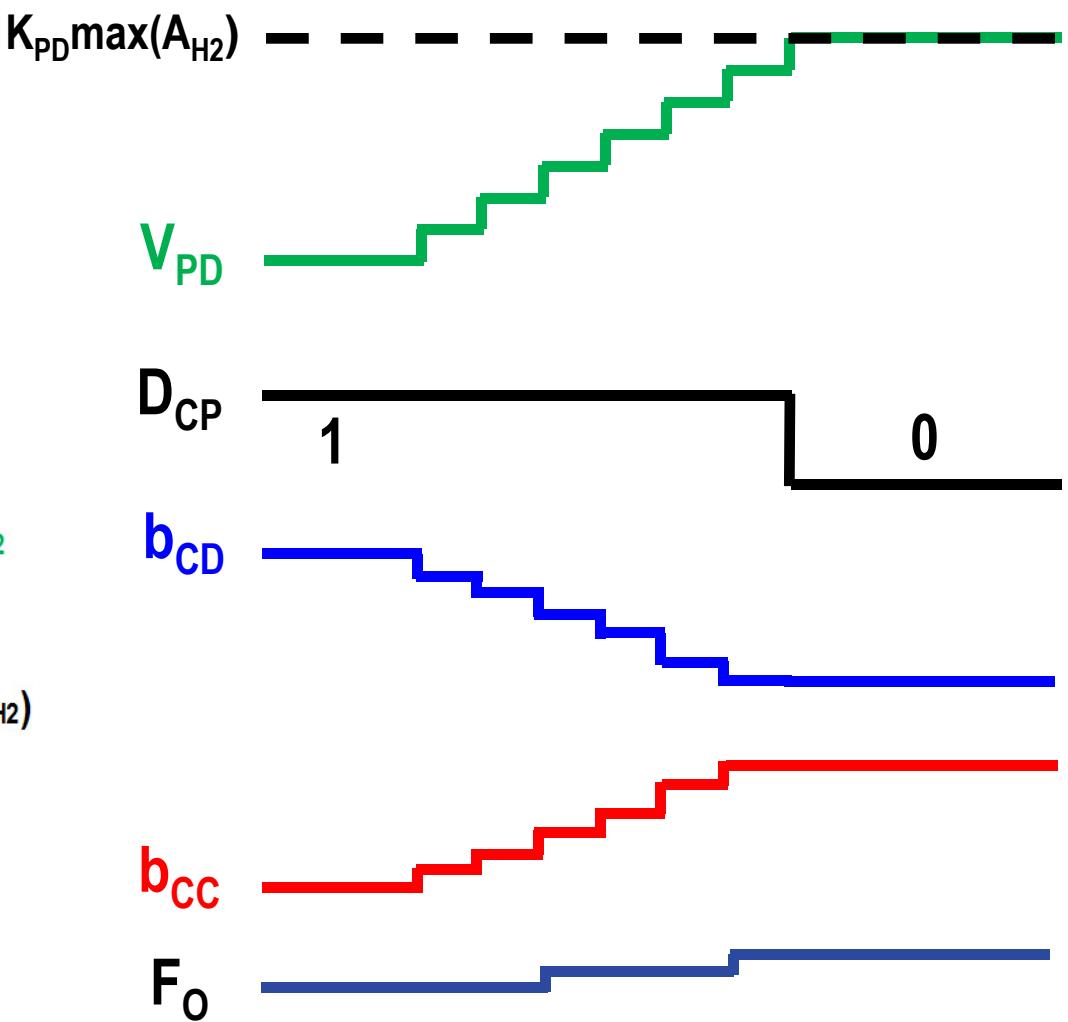
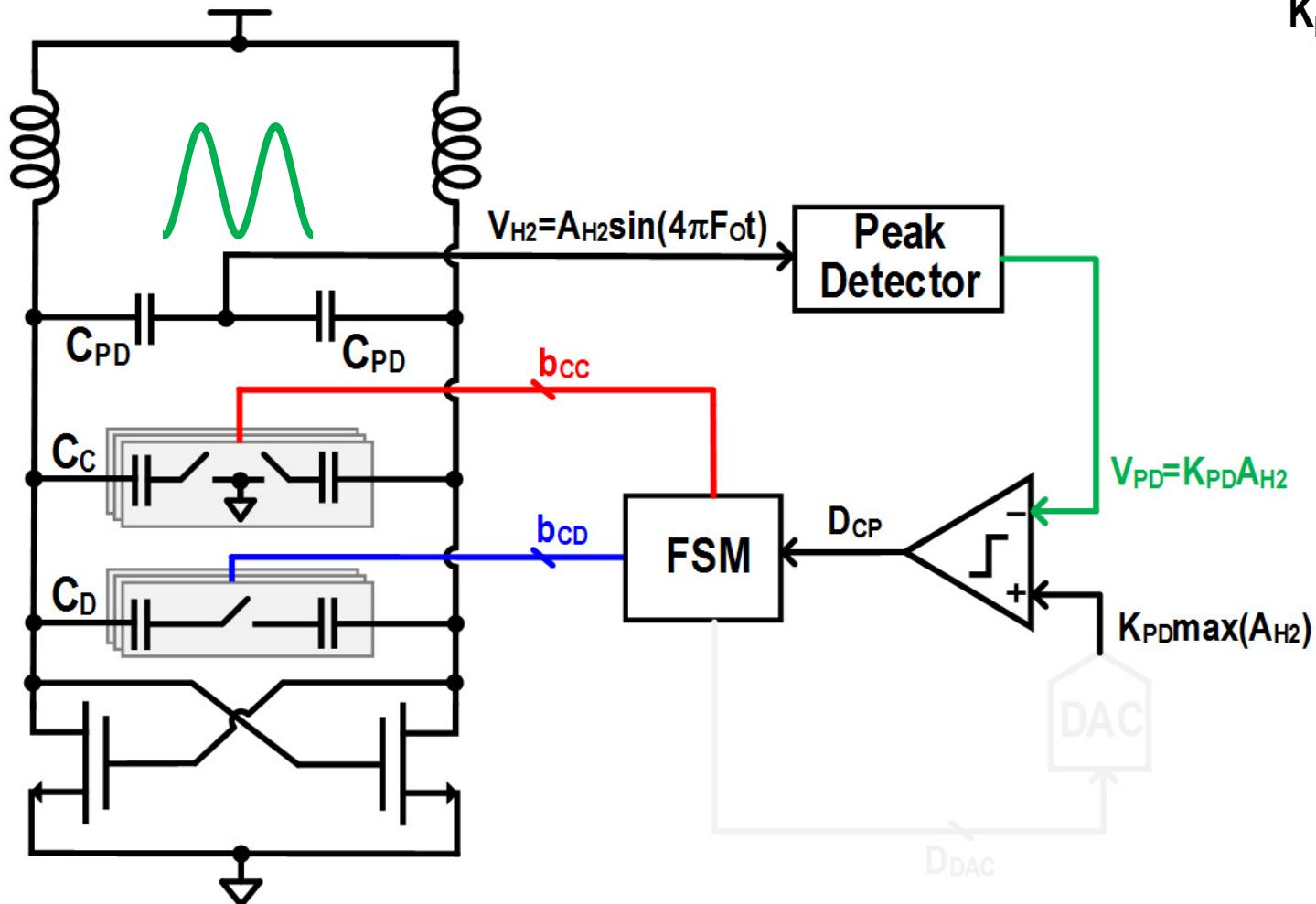
b_{CC}

F_0

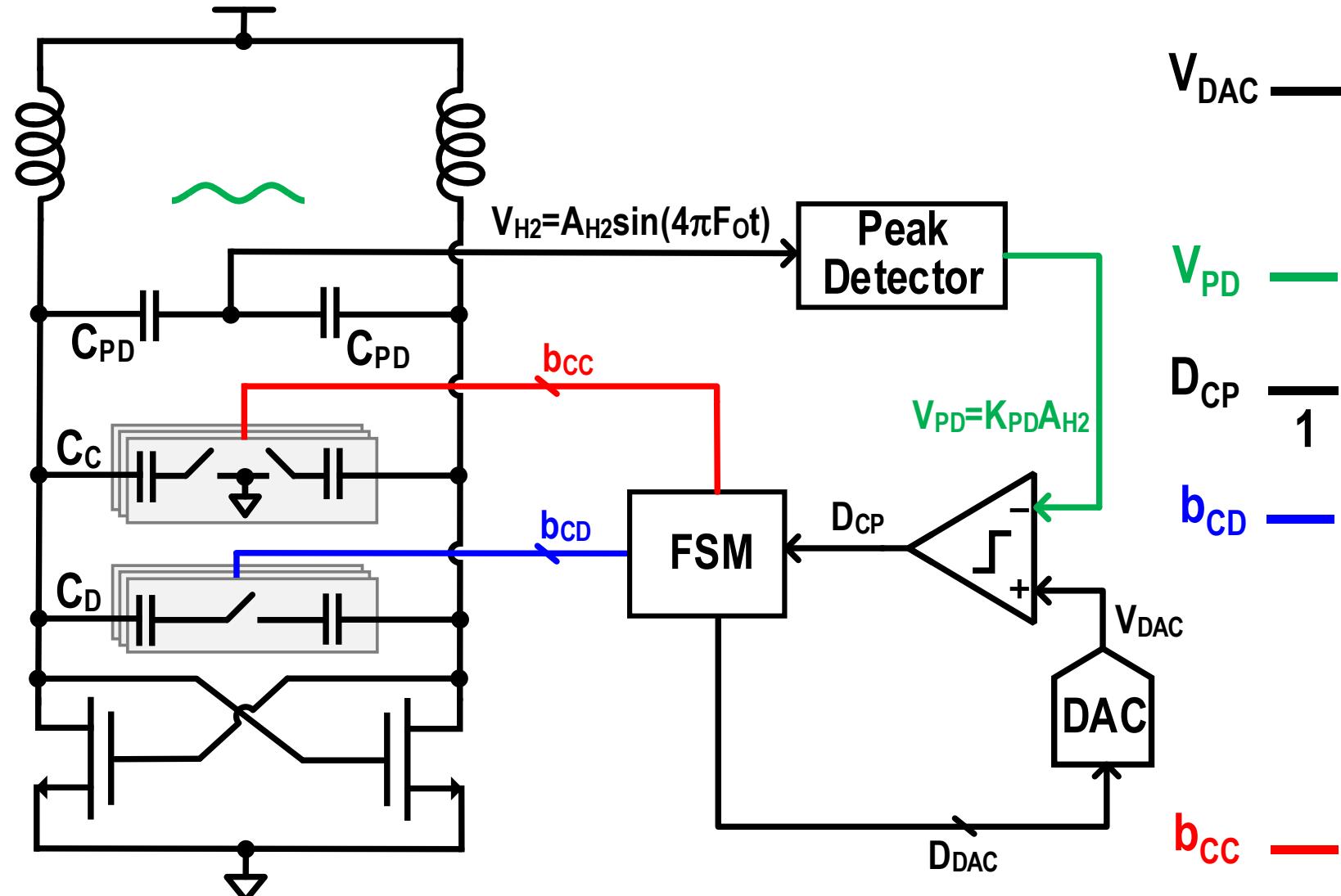
Calibration loop



Calibration loop

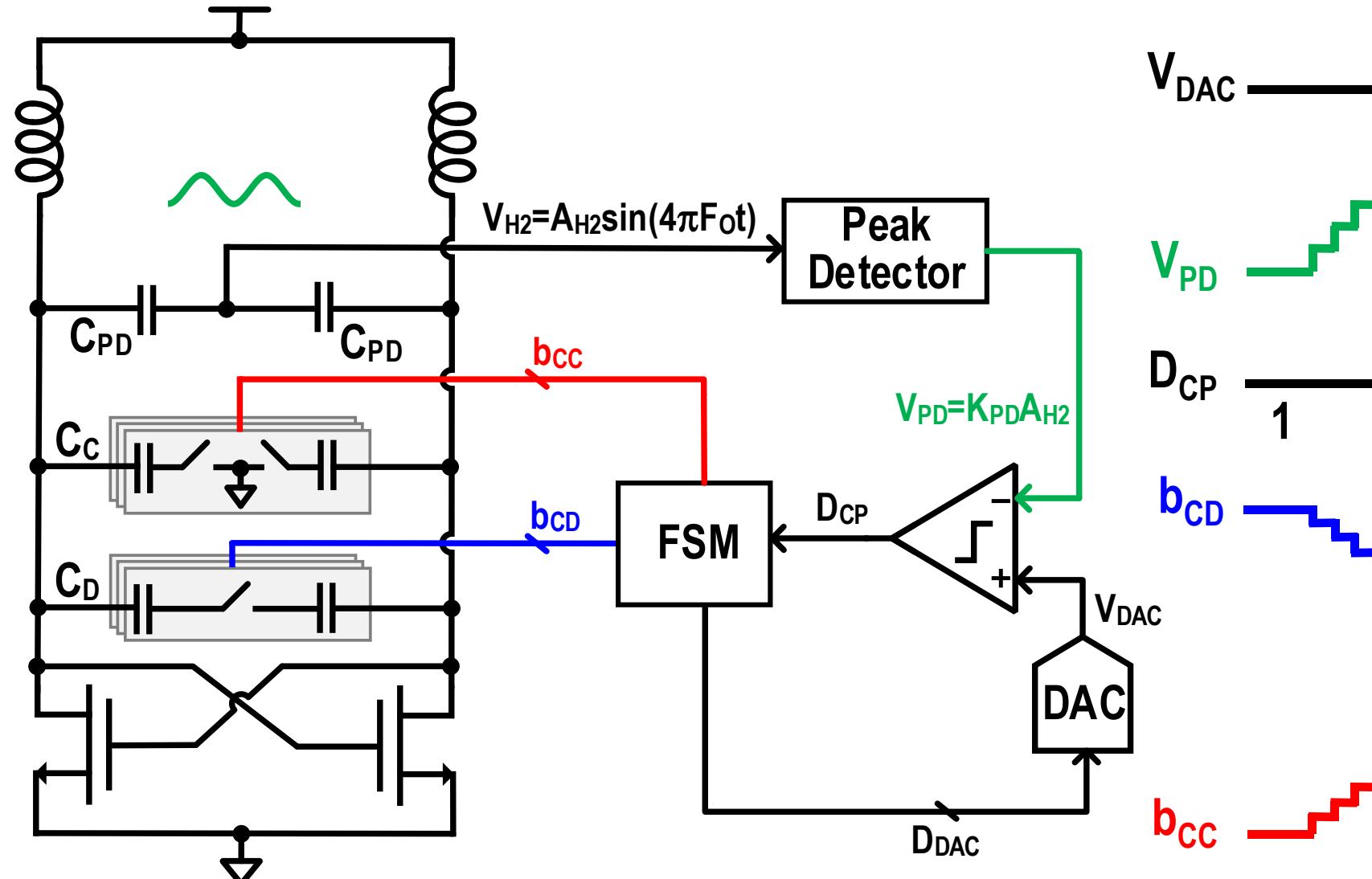


Calibration loop – Finding DAC setting



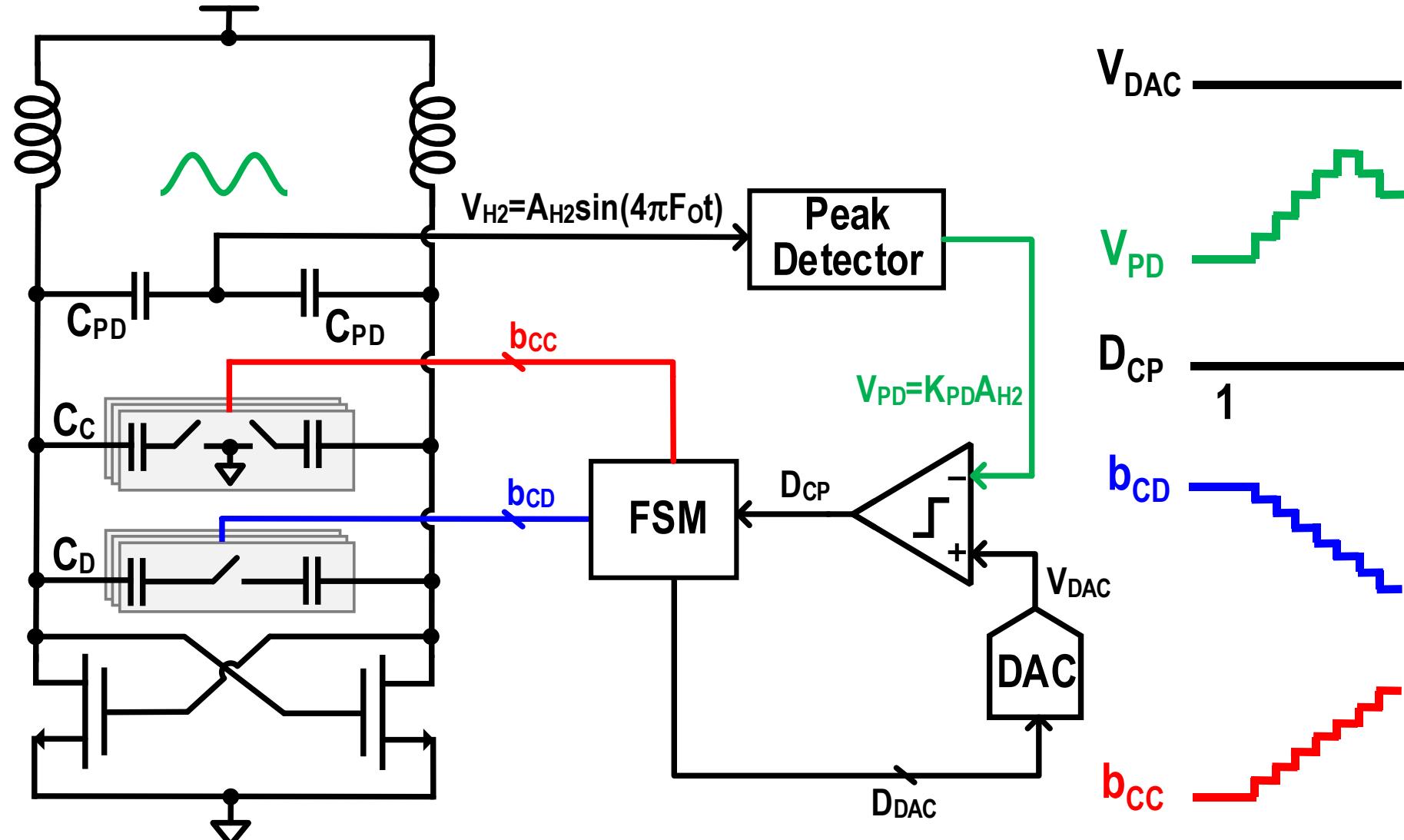
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Calibration loop – Finding DAC setting



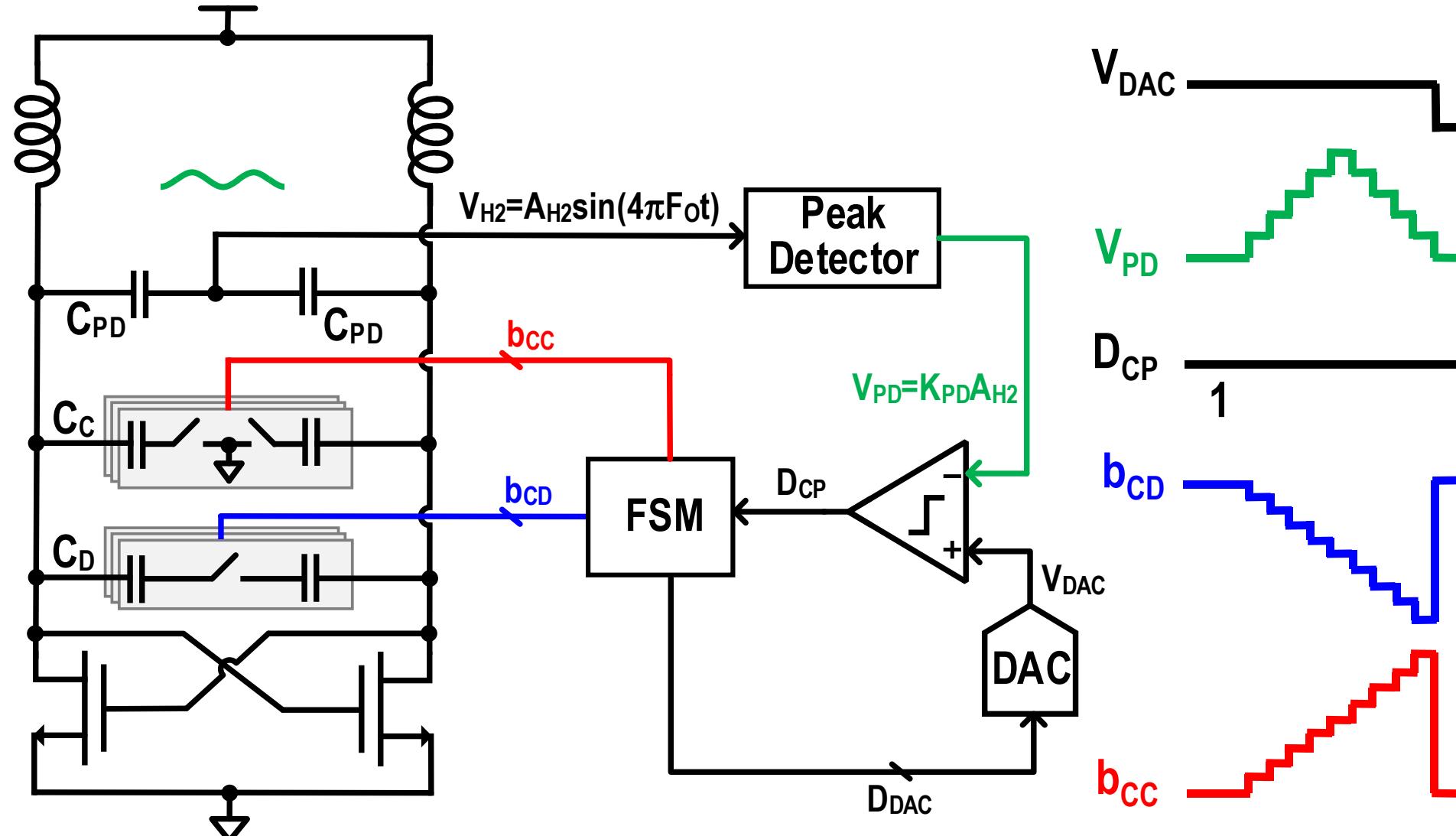
19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Calibration loop – Finding DAC setting



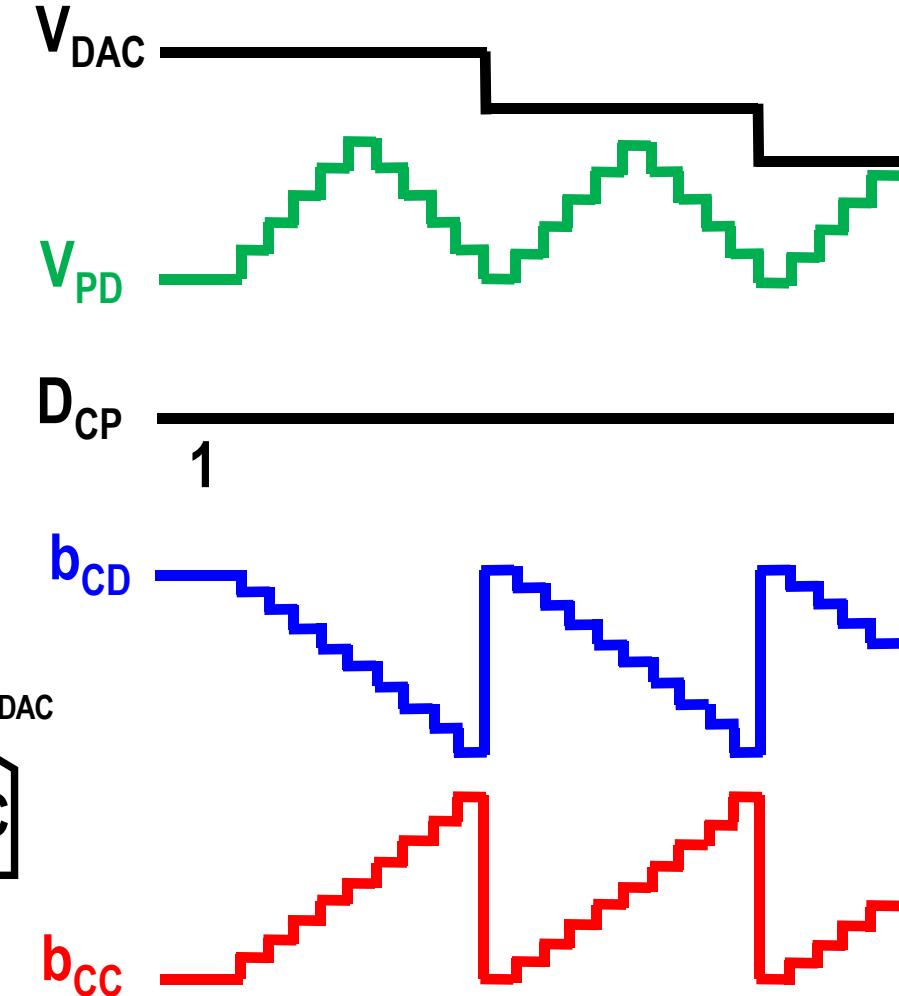
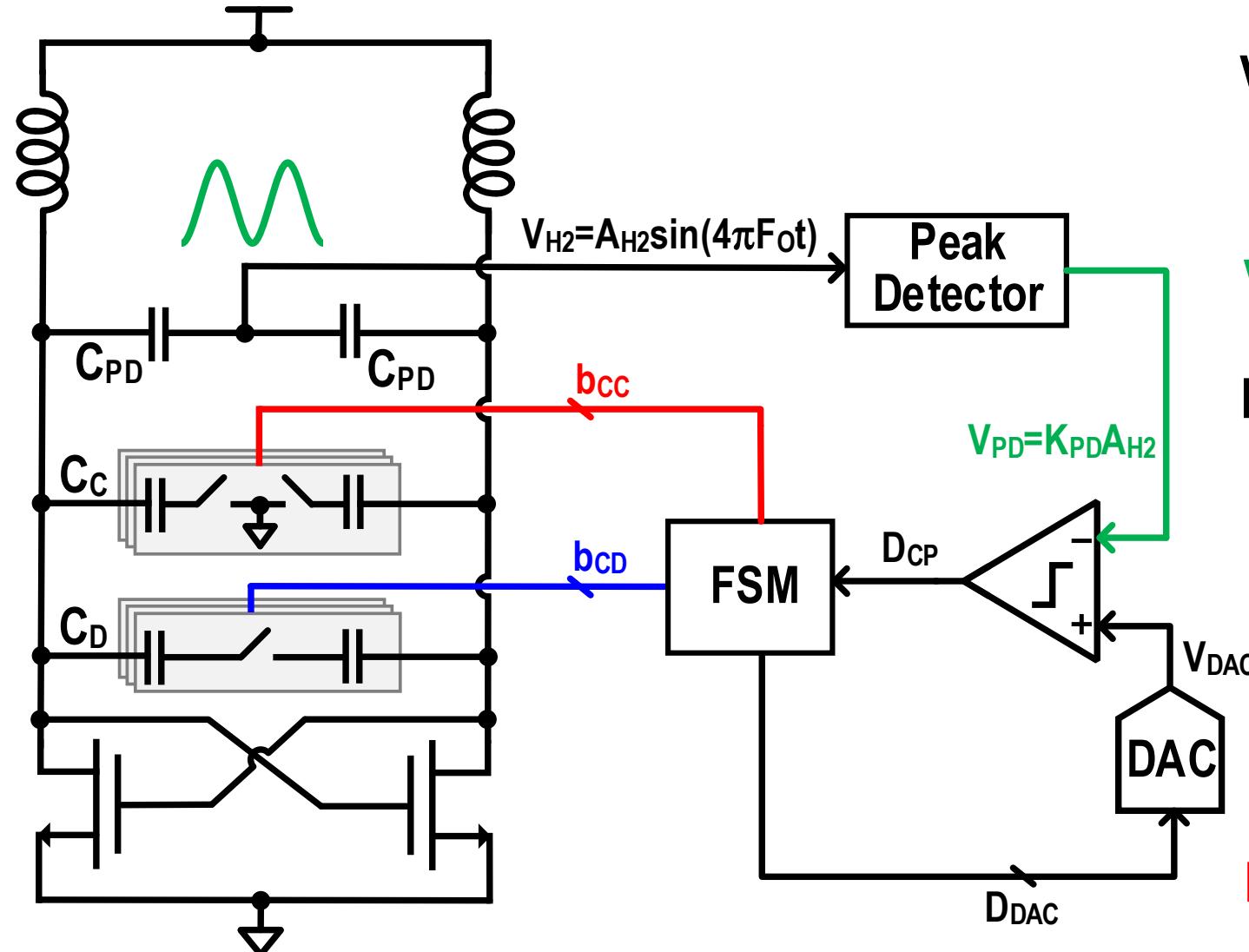
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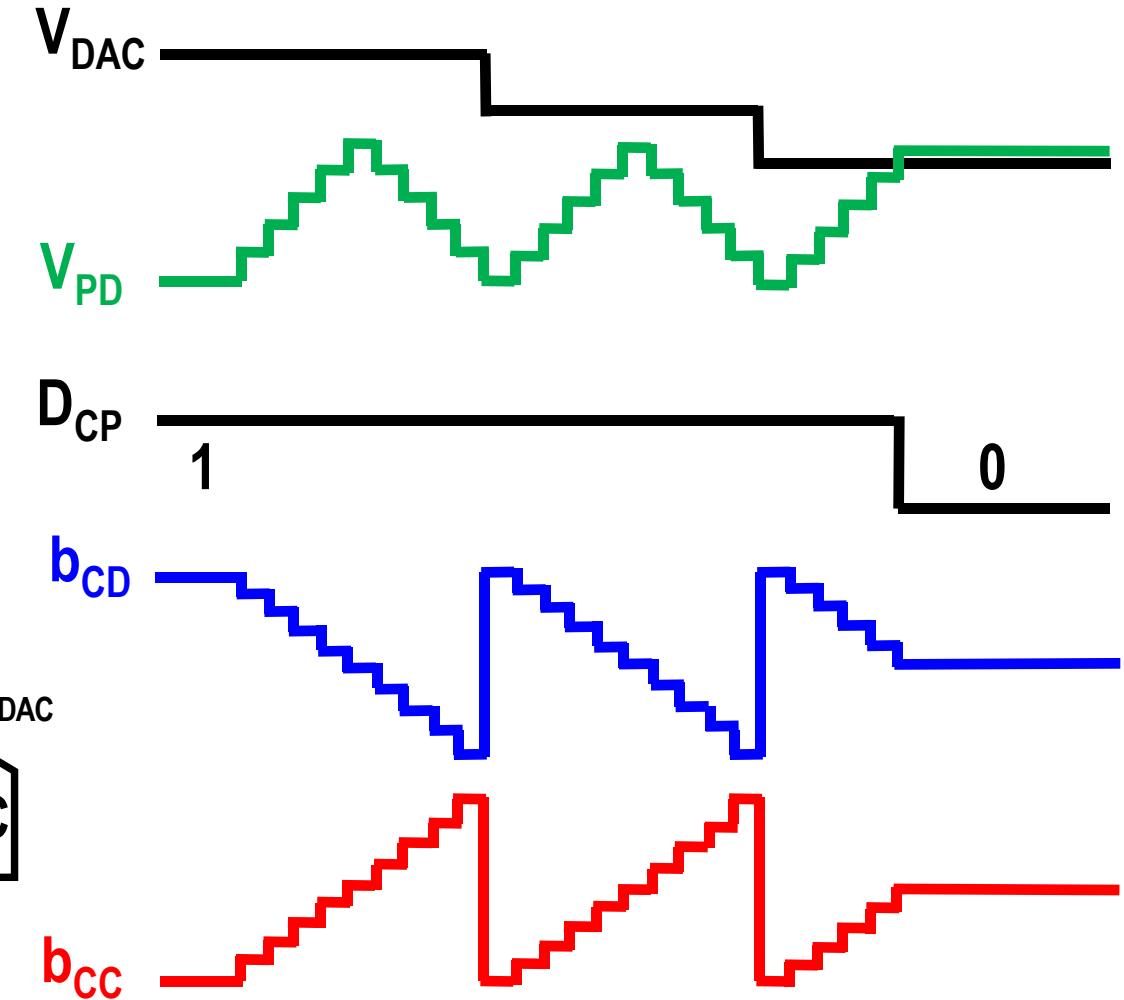
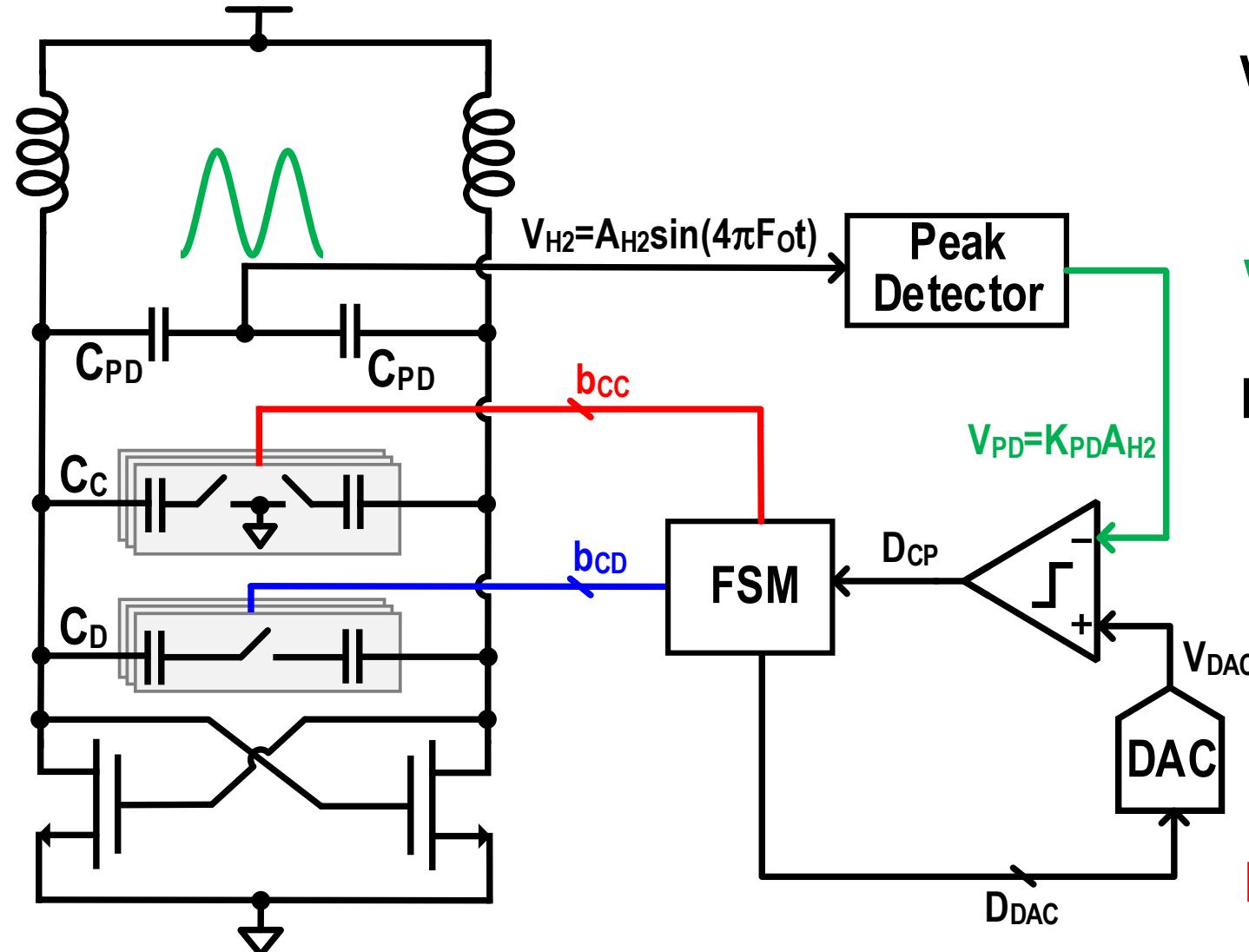
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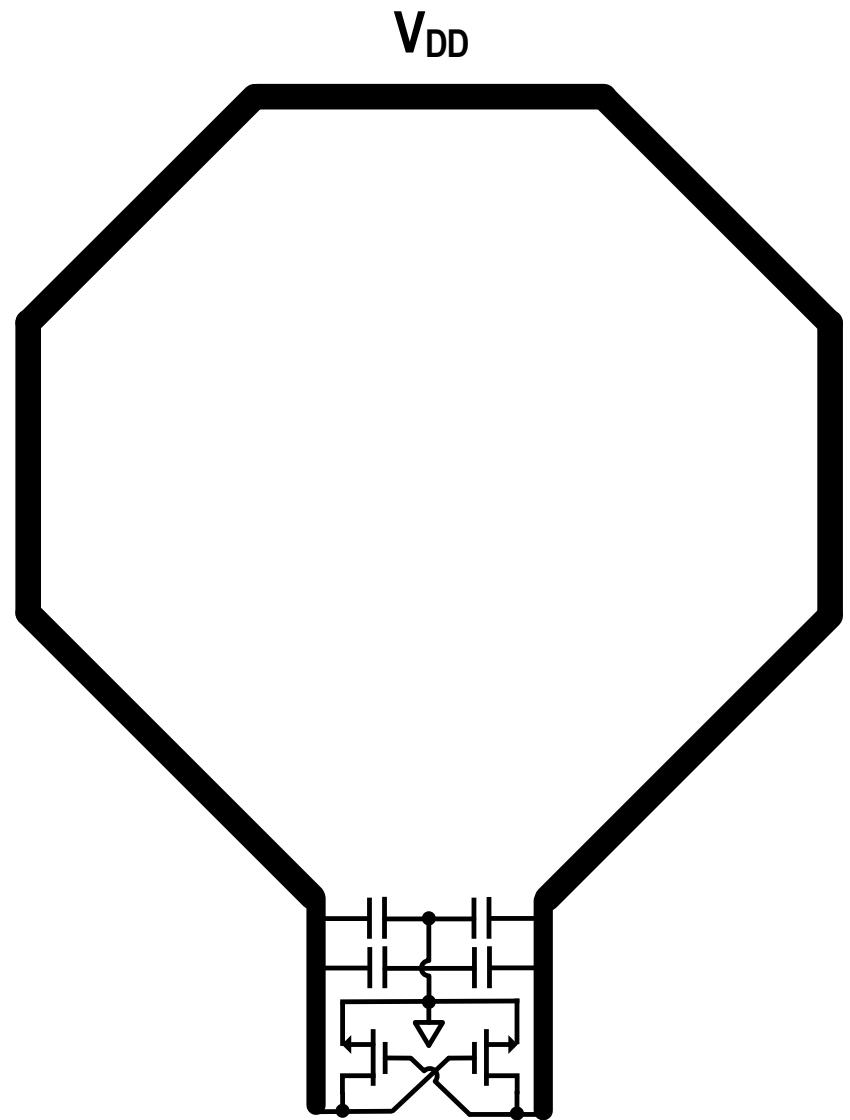


19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Outline

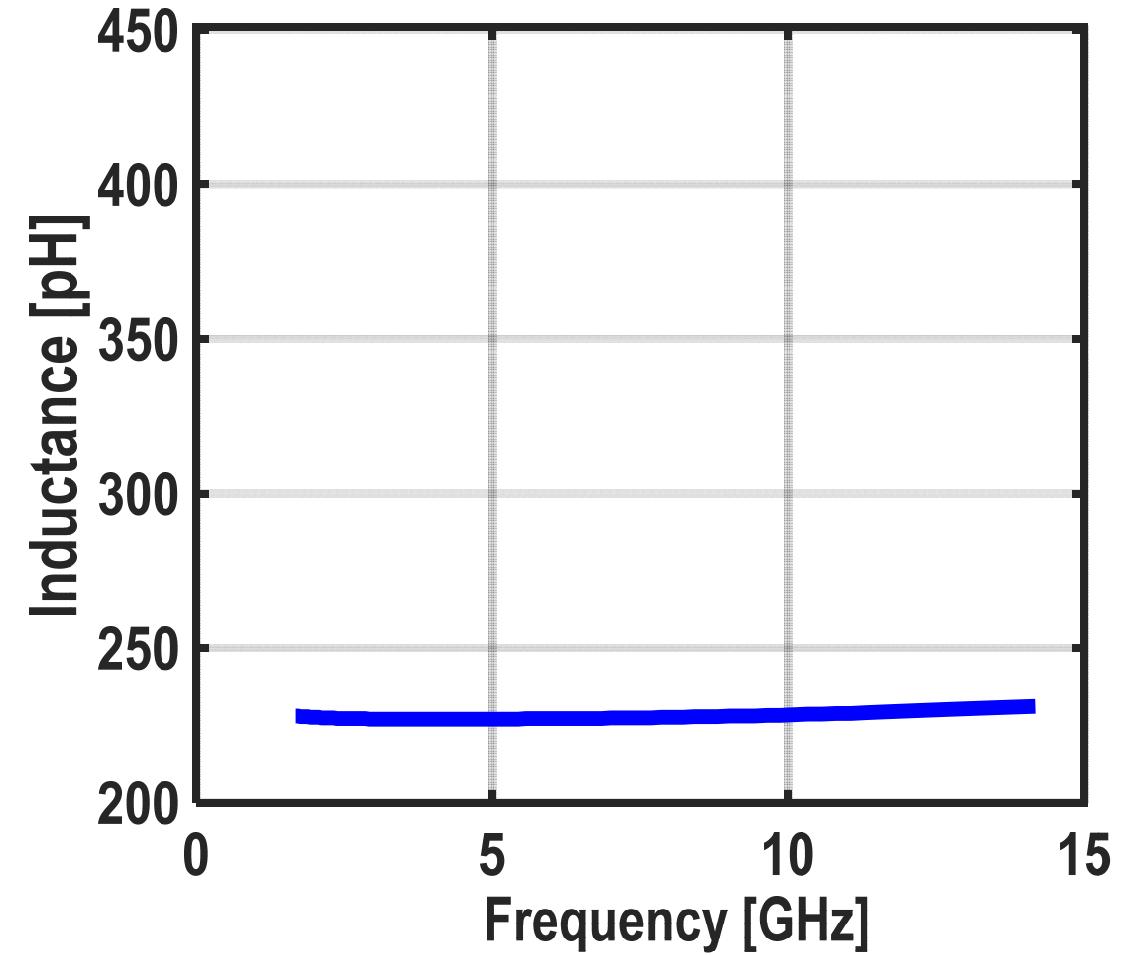
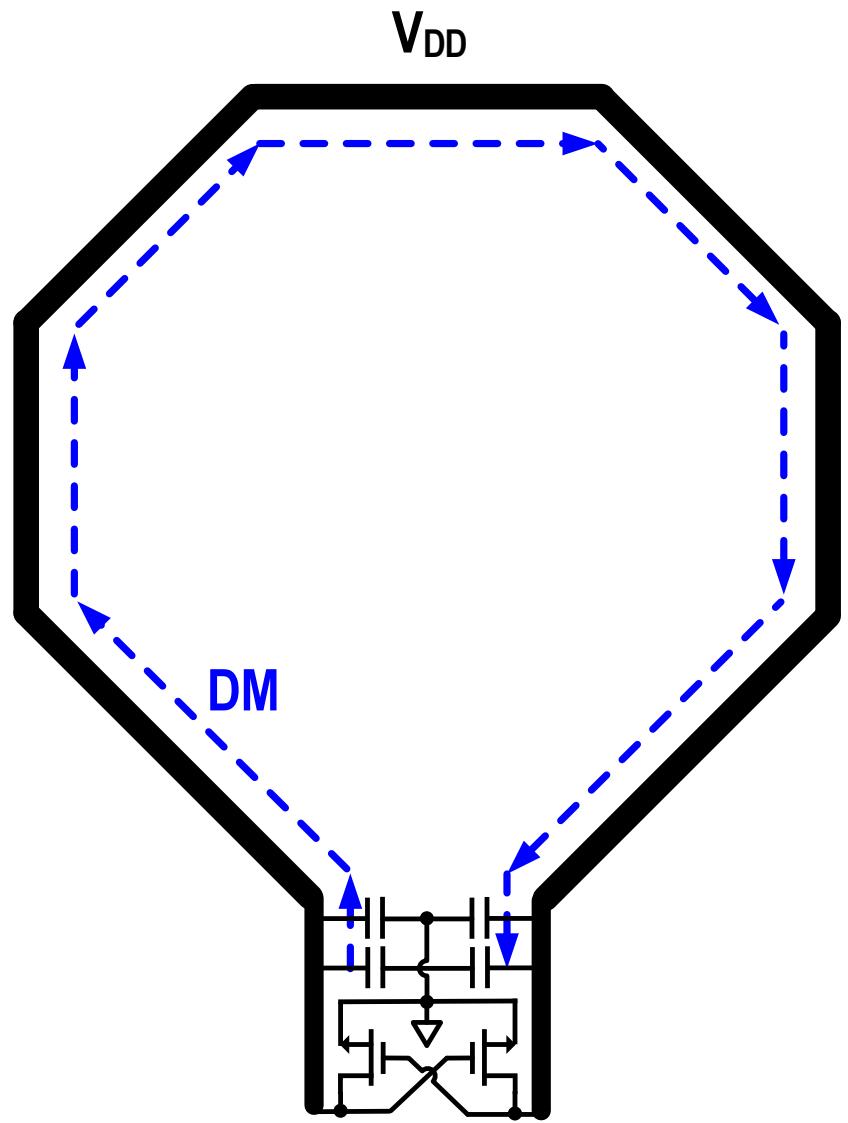
- Motivation
- Cryogenic Oscillators: Design Challenges
- Proposed Calibration for the Optimum Phase Noise
- Circuit Implementation**
- Measurement Results
- Conclusions

One-Turn inductor for low phase noise

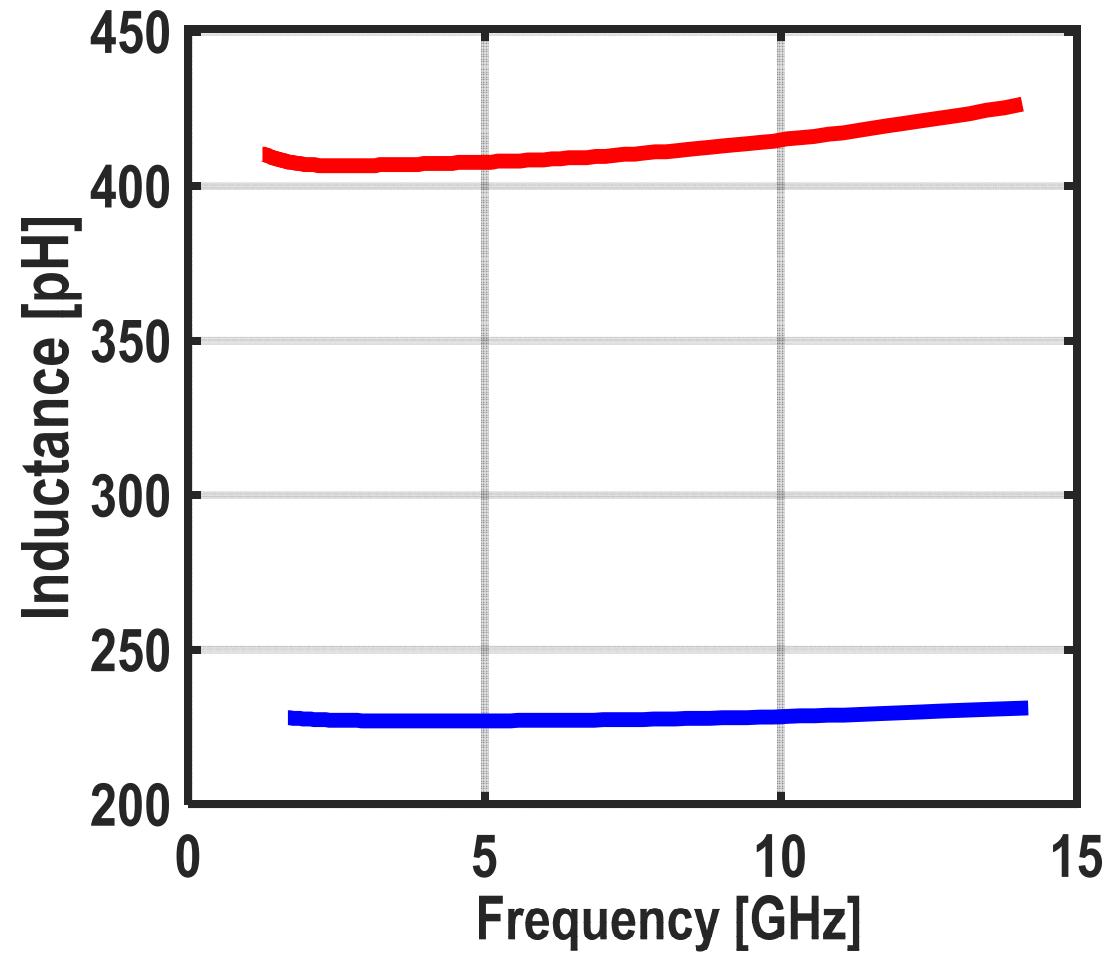
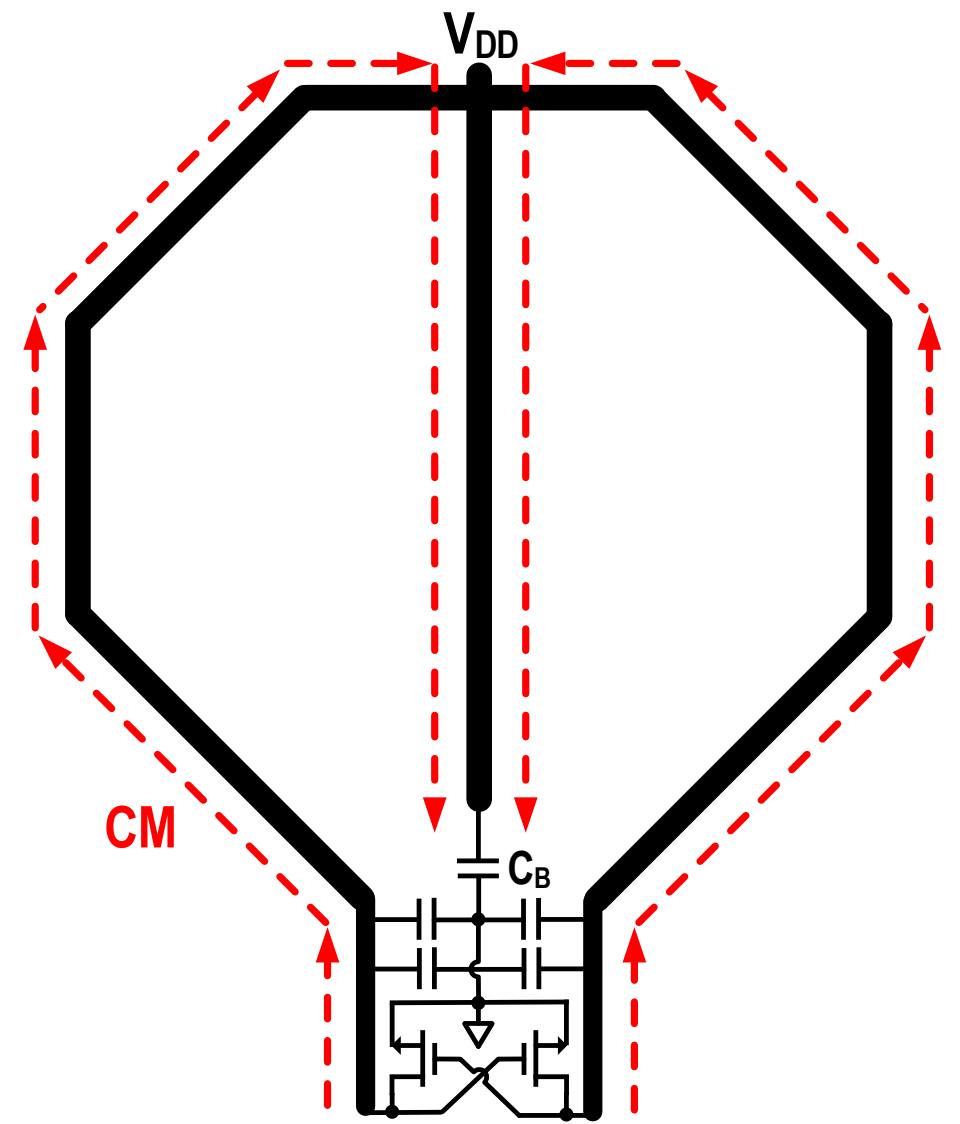


$$\mathcal{L}(\Delta\omega) = 10\log_{10} \left(L \frac{KT}{2QV_{osc}^2} \frac{\omega_0^3}{\Delta\omega^2} (1 + \gamma) \right)$$

Conventional one-turn inductor – DM

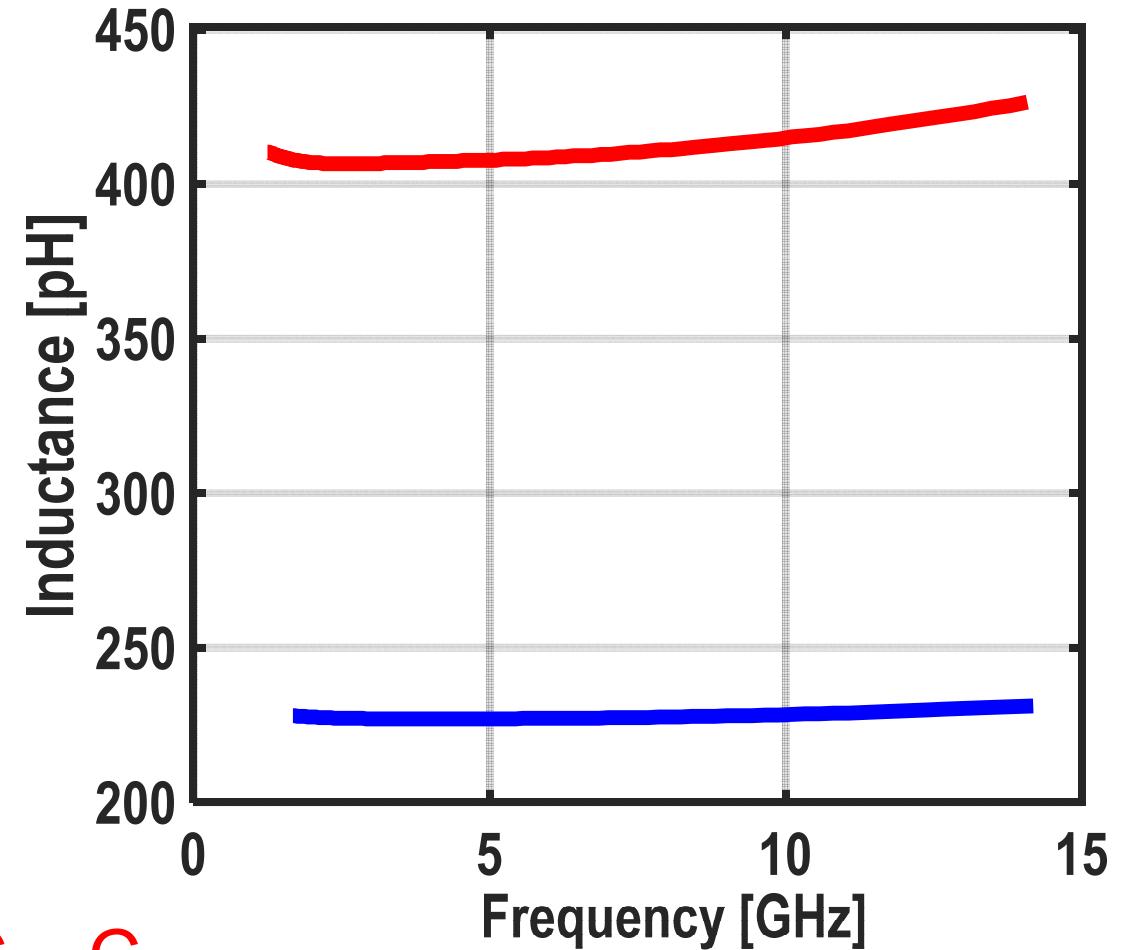
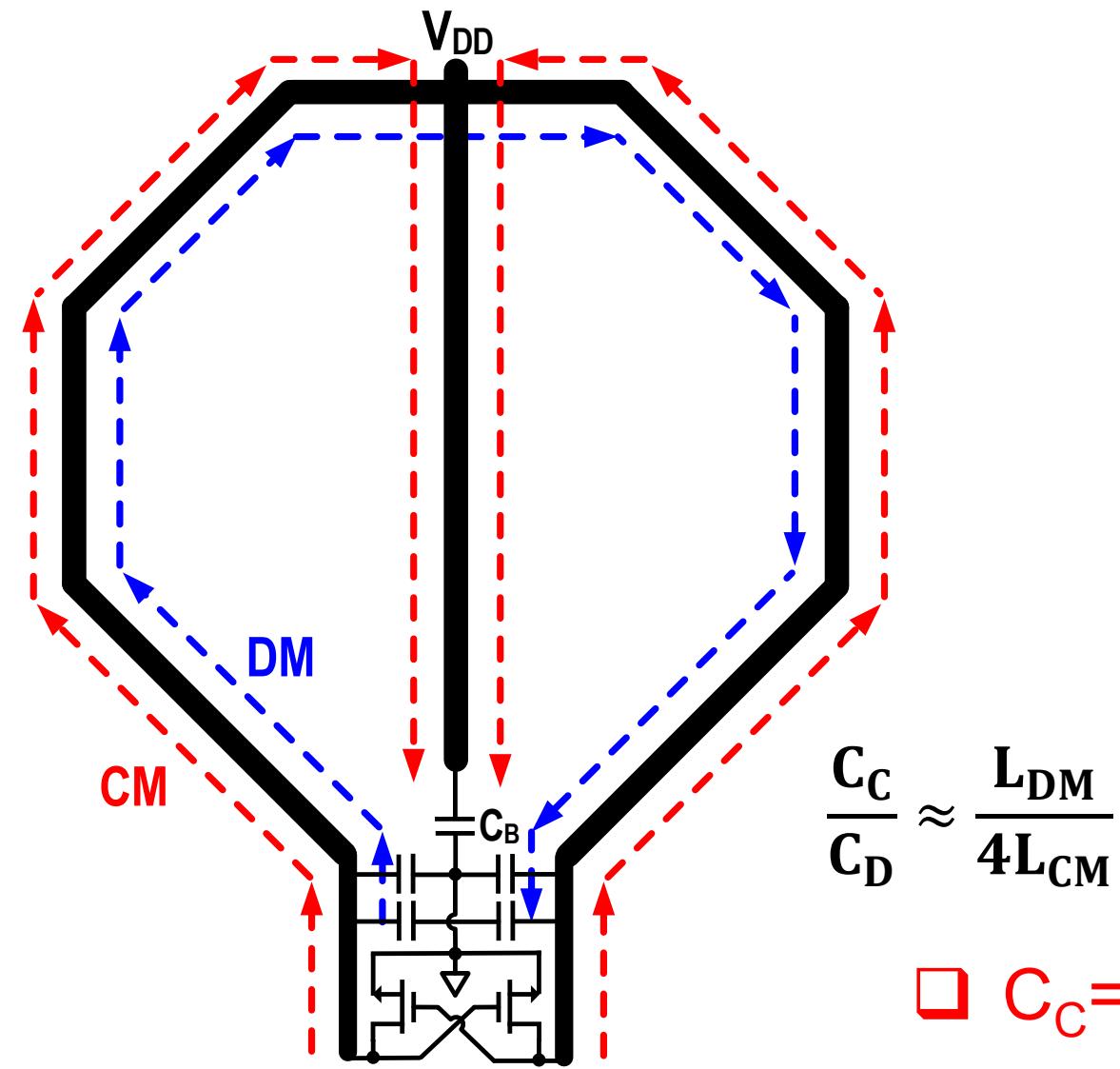


Conventional one-turn inductor – CM



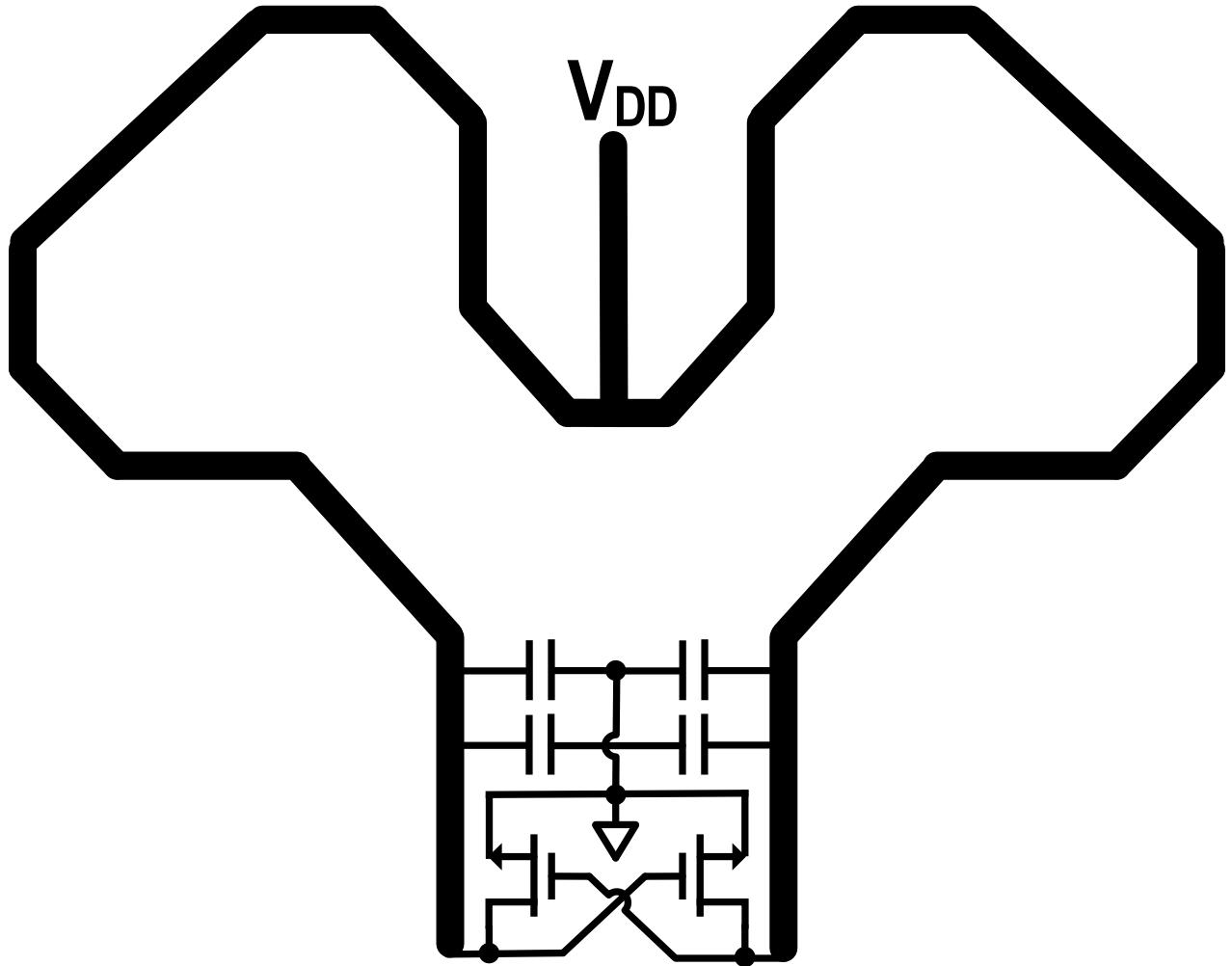
19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Conventional one-turn inductor – Limitations



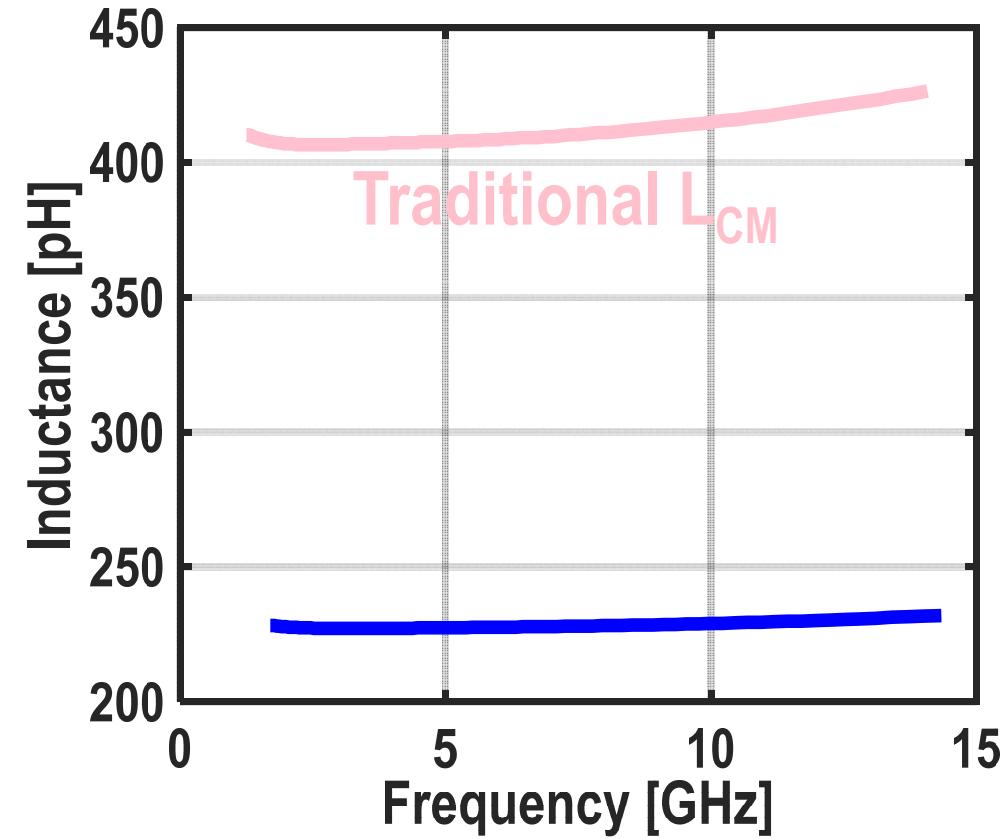
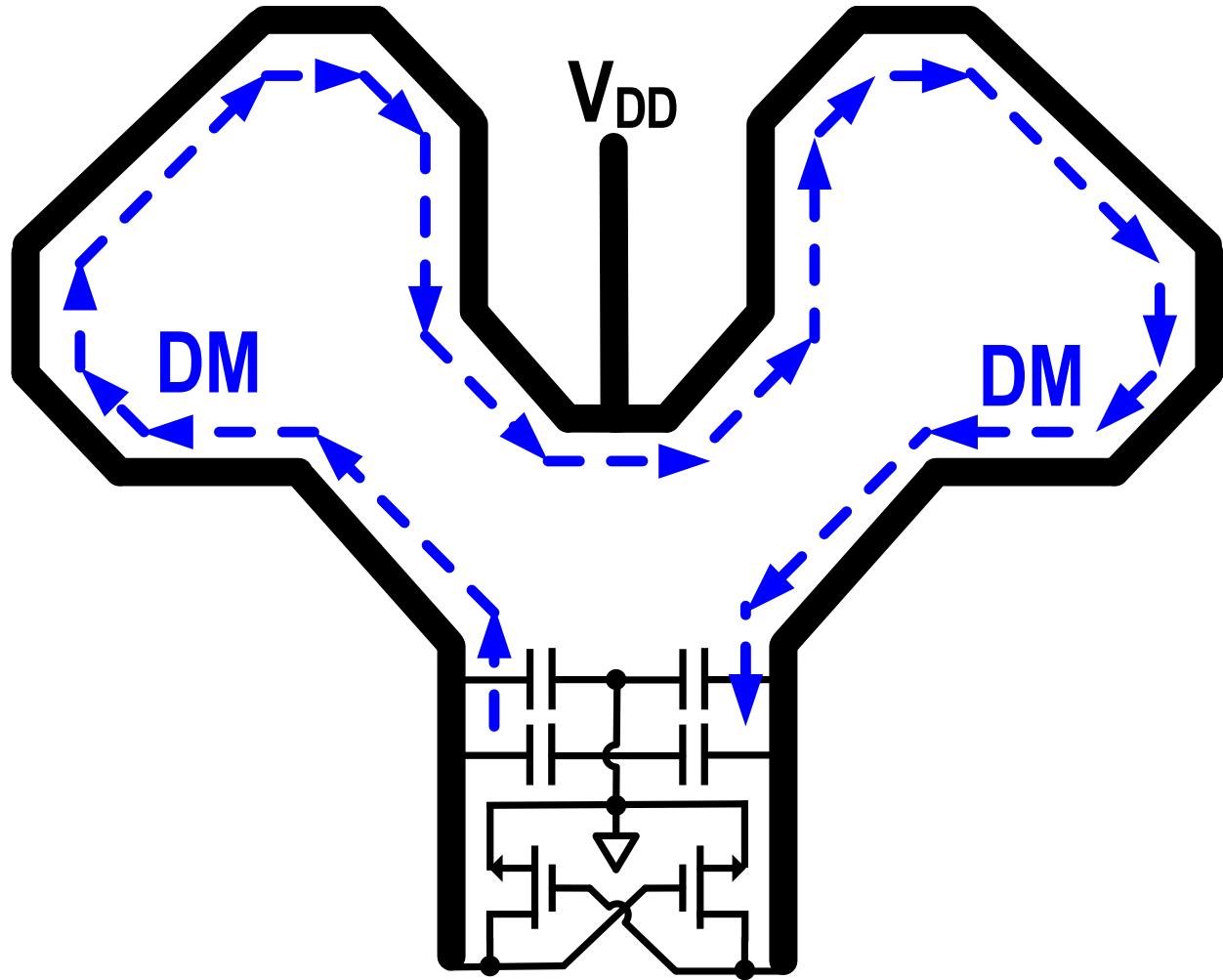
19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Optimized one-turn inductor



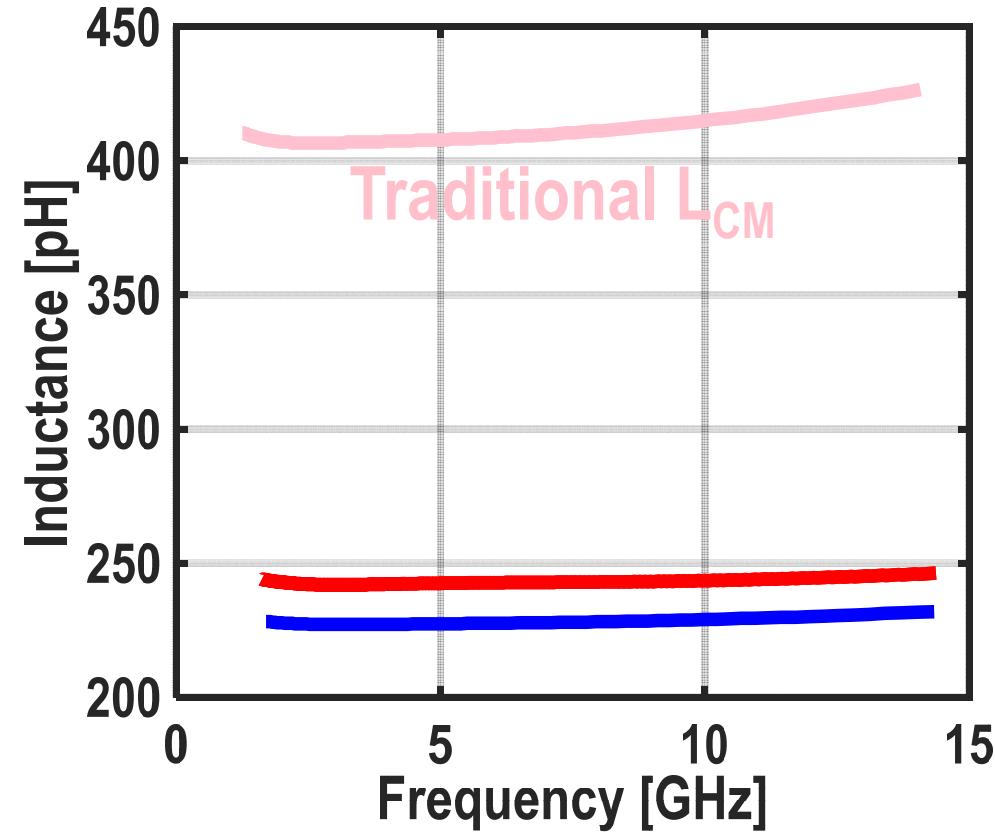
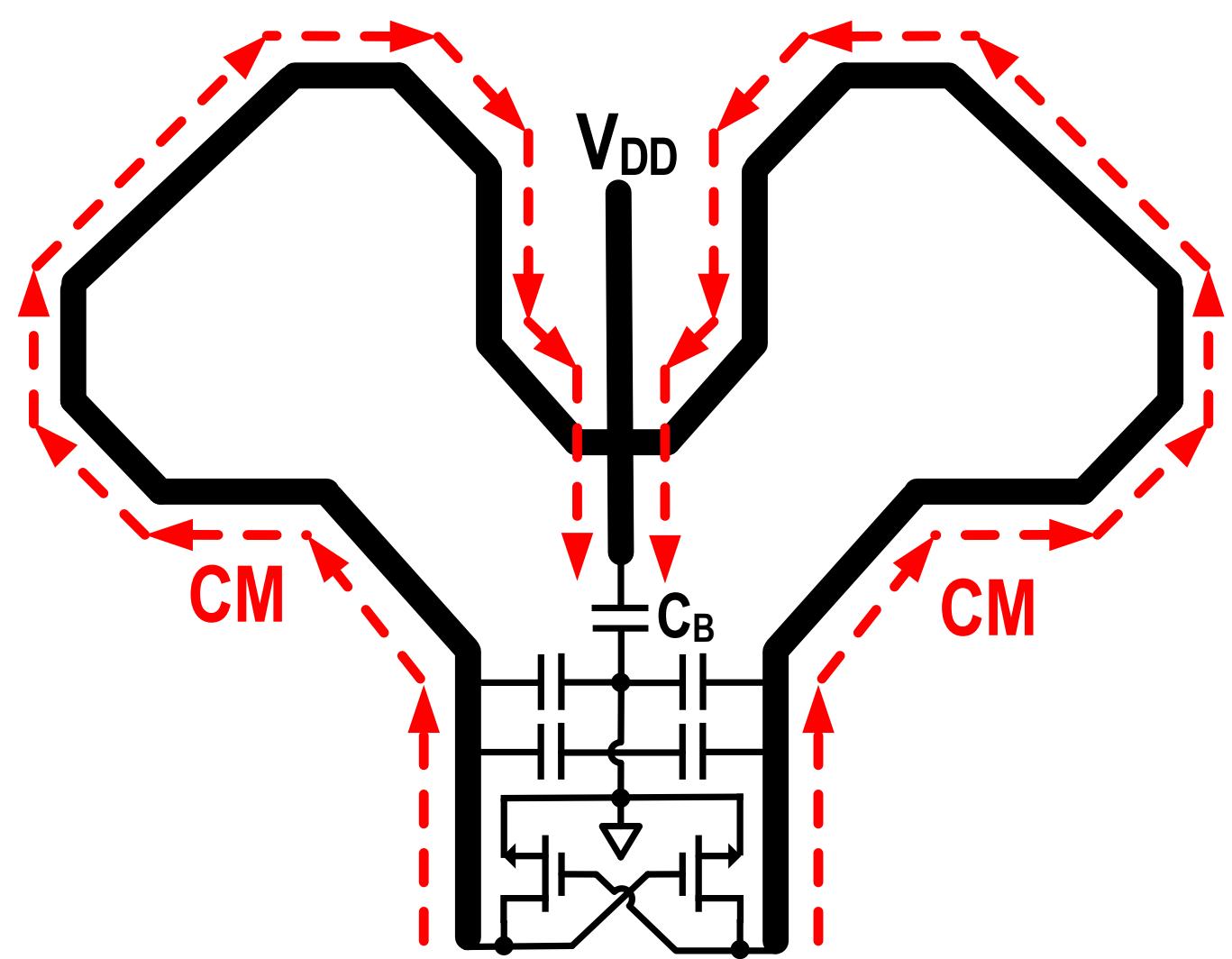
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Optimized one-turn inductor – DM



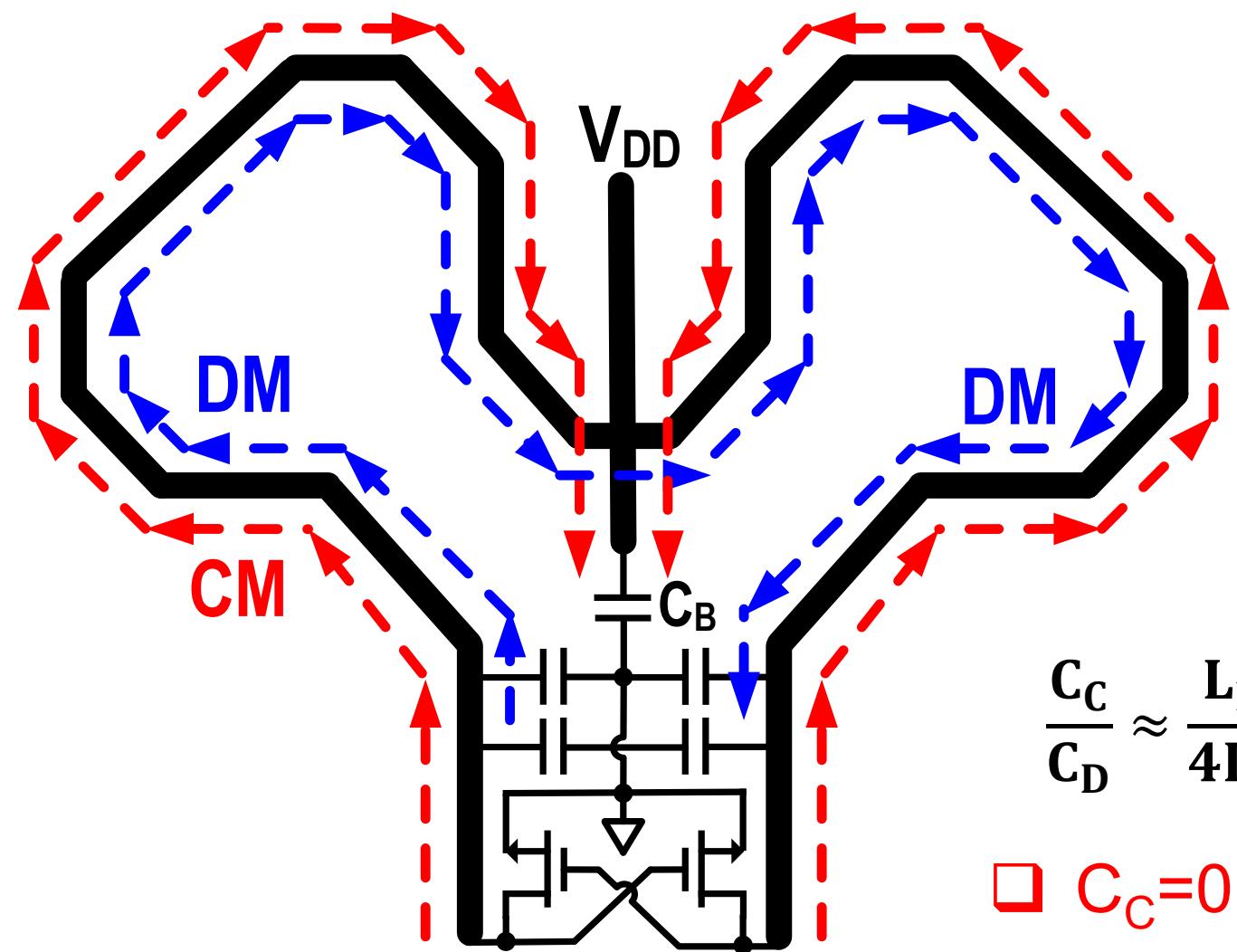
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Optimized one-turn inductor – CM



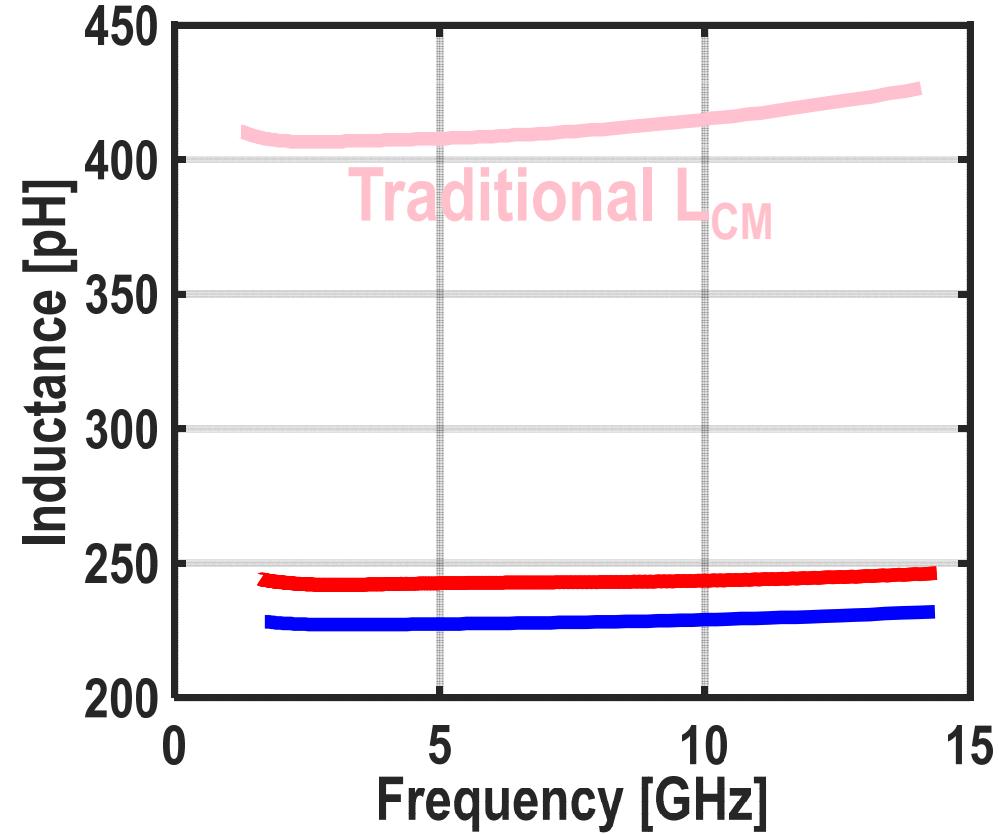
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Optimized one-turn inductor



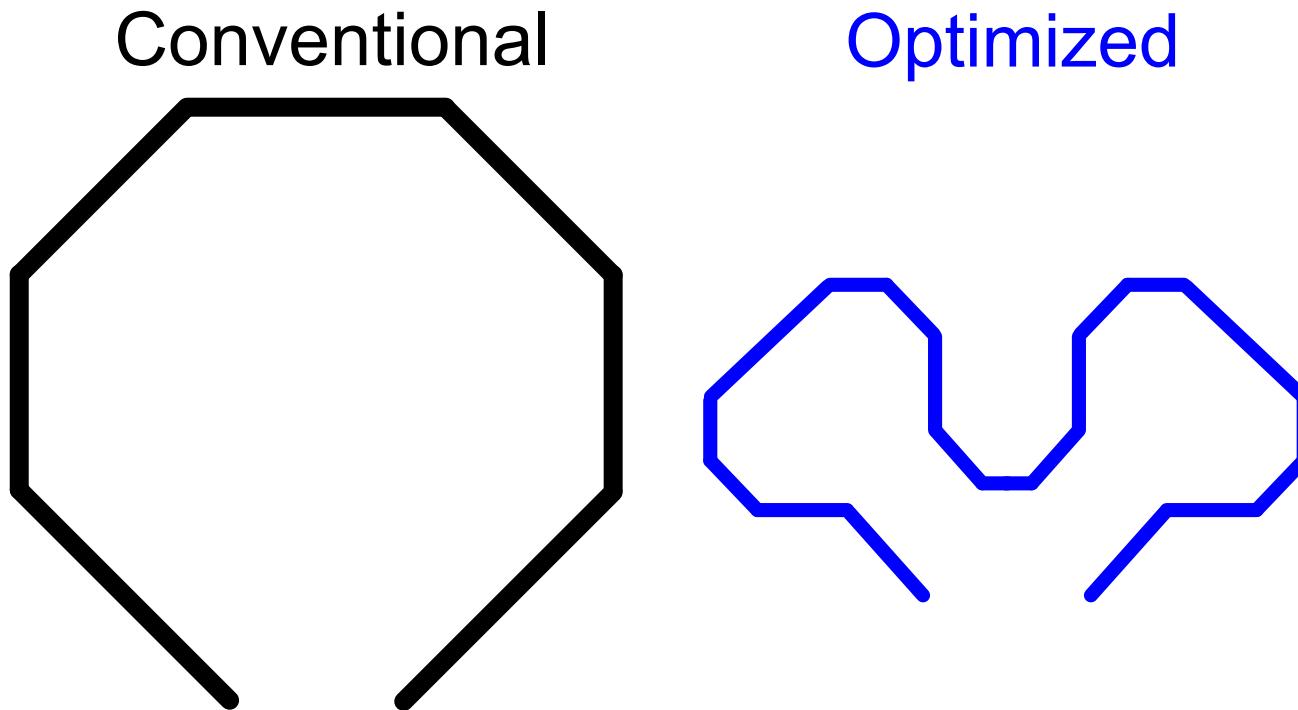
$$\frac{C_C}{C_D} \approx \frac{L_{DM}}{4L_{CM}}$$

□ $C_C = 0.28C_D > C_P$

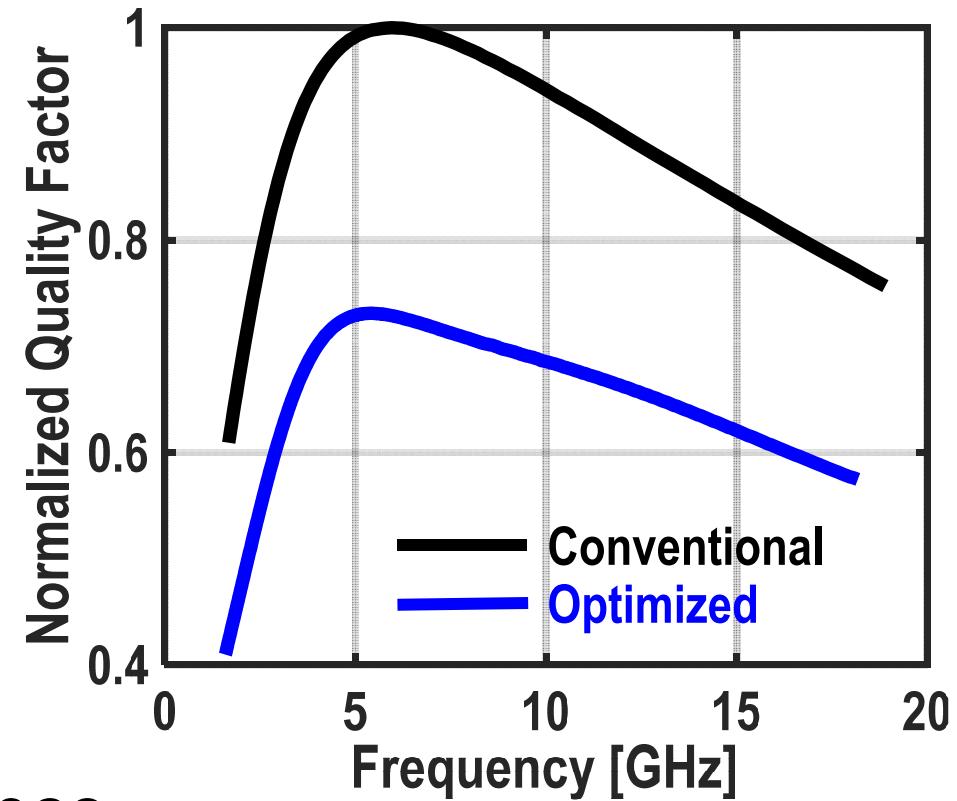


19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

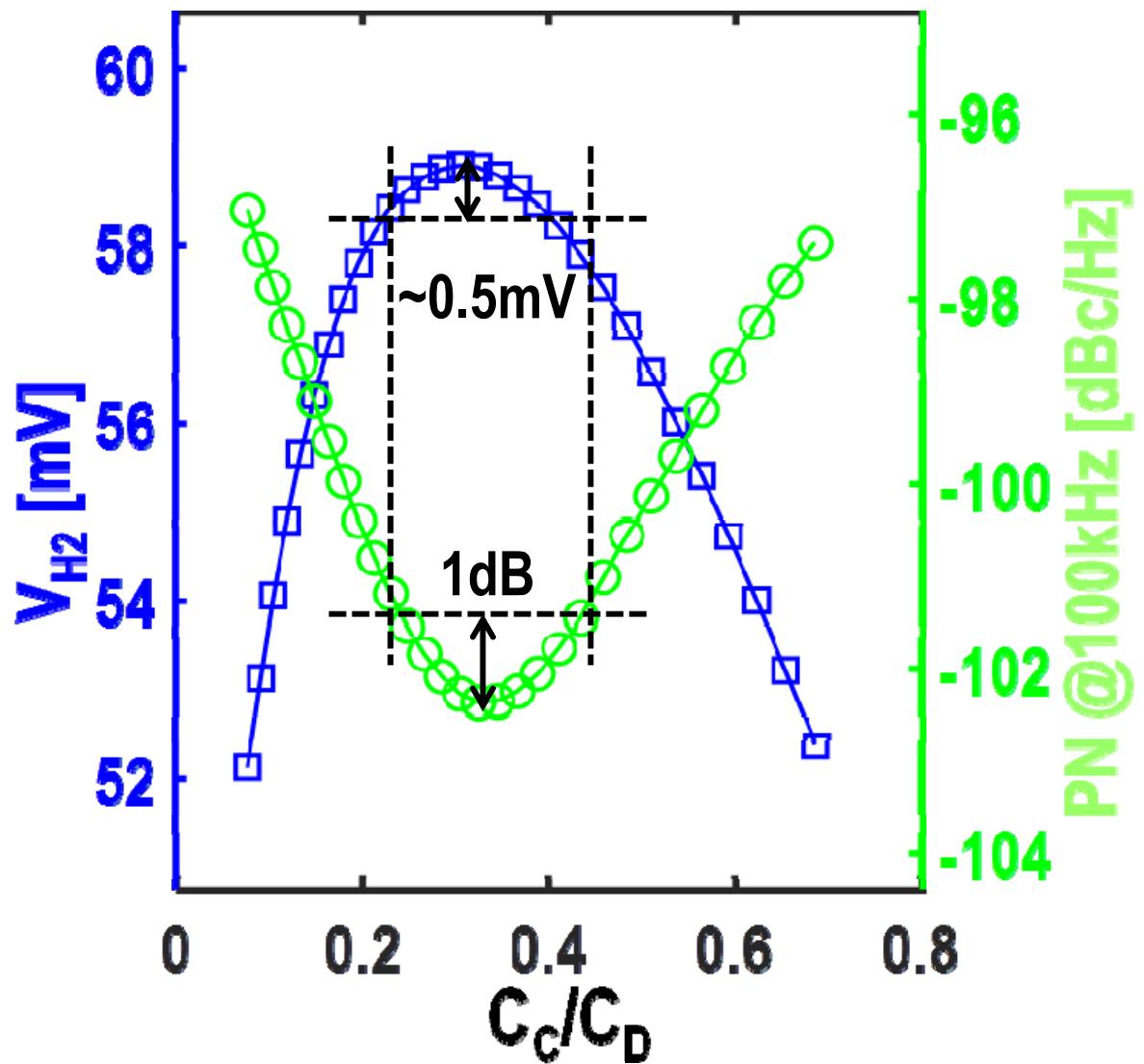
Comparison with conventional inductor



- ~30% area smaller for the same inductance
- ~30% lower quality factor
- Low CM inductance \Rightarrow allows for feasible C_c

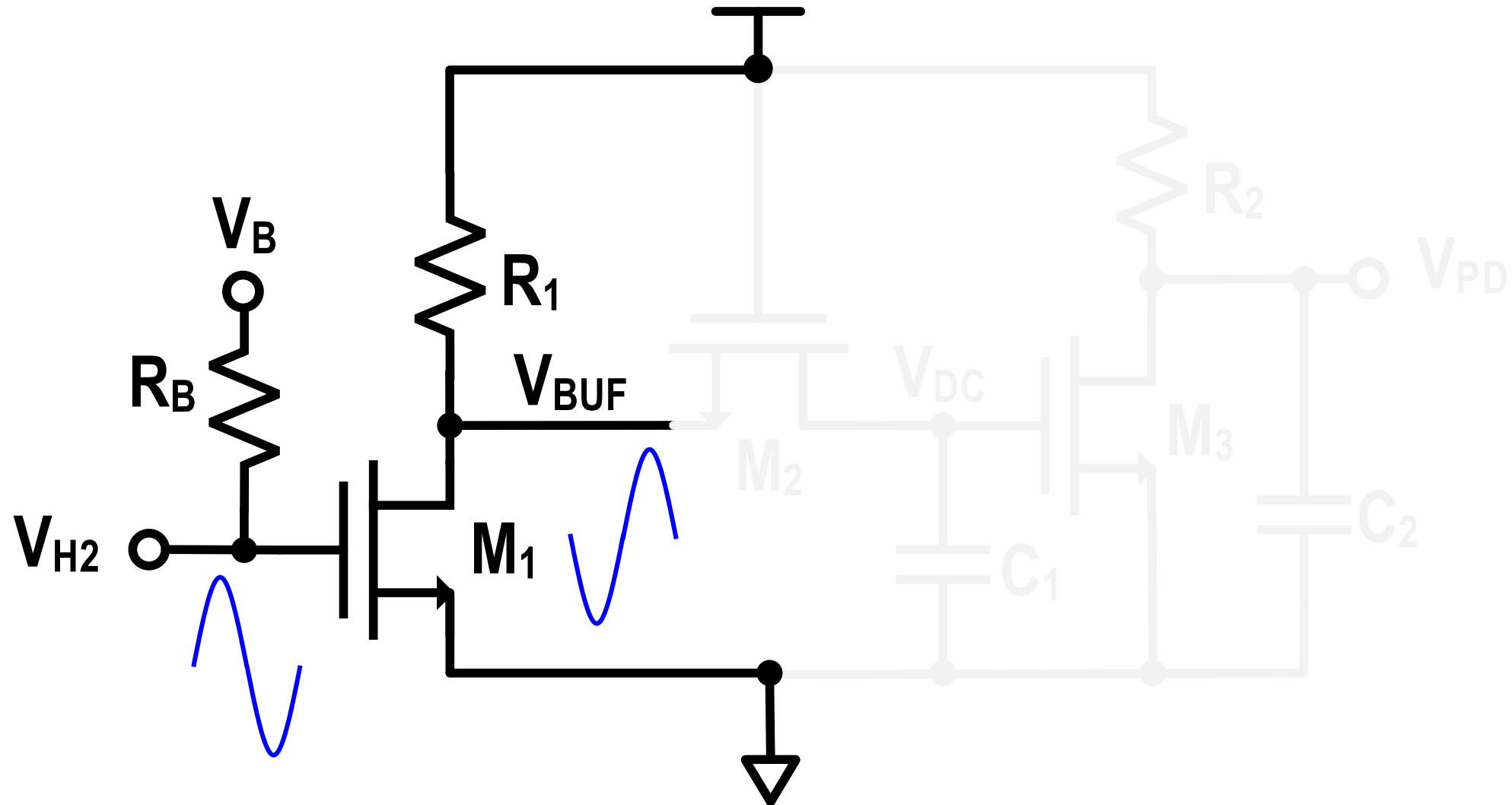


Calibration loop – Noise requirements

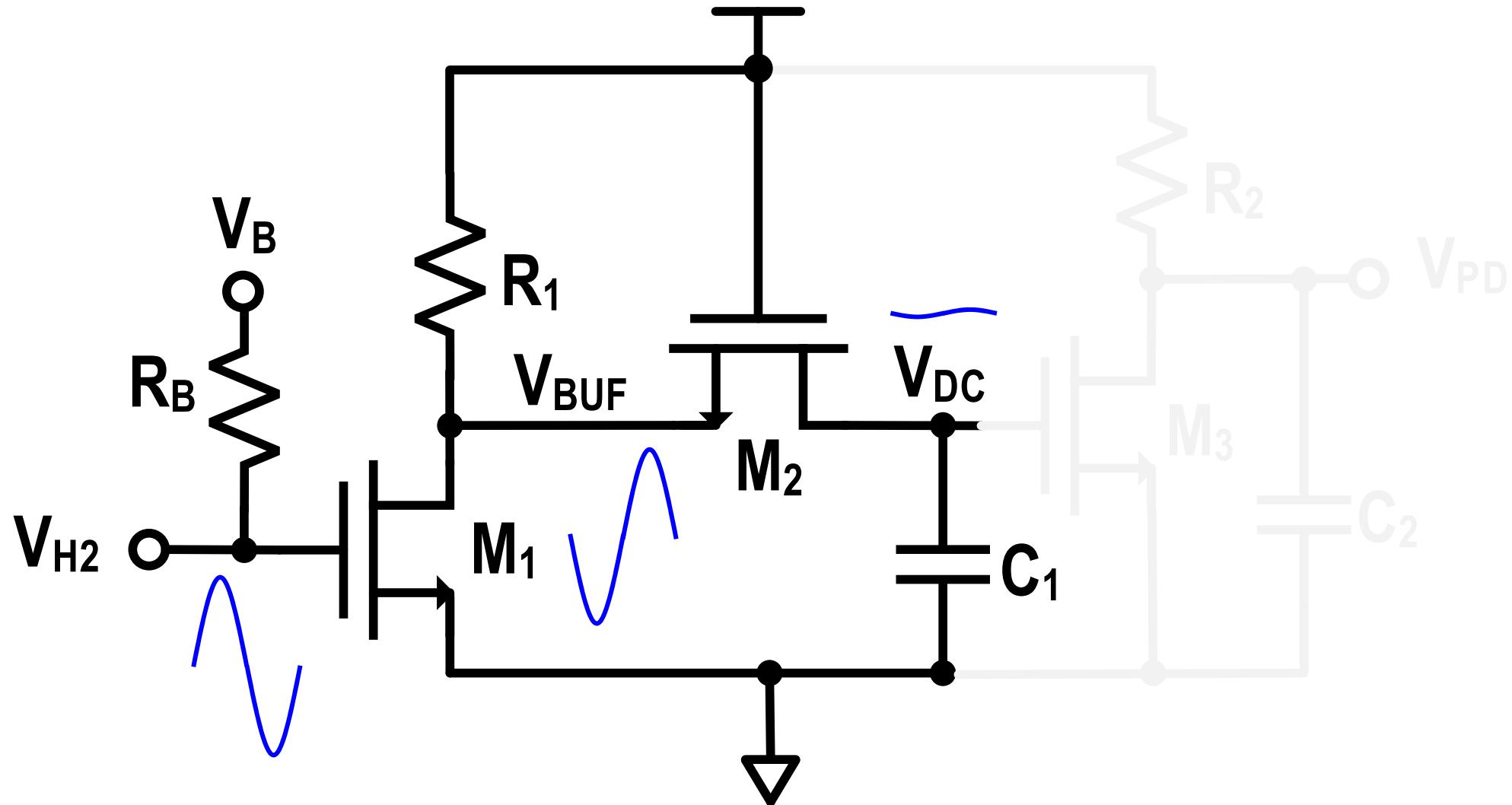


19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Peak detector

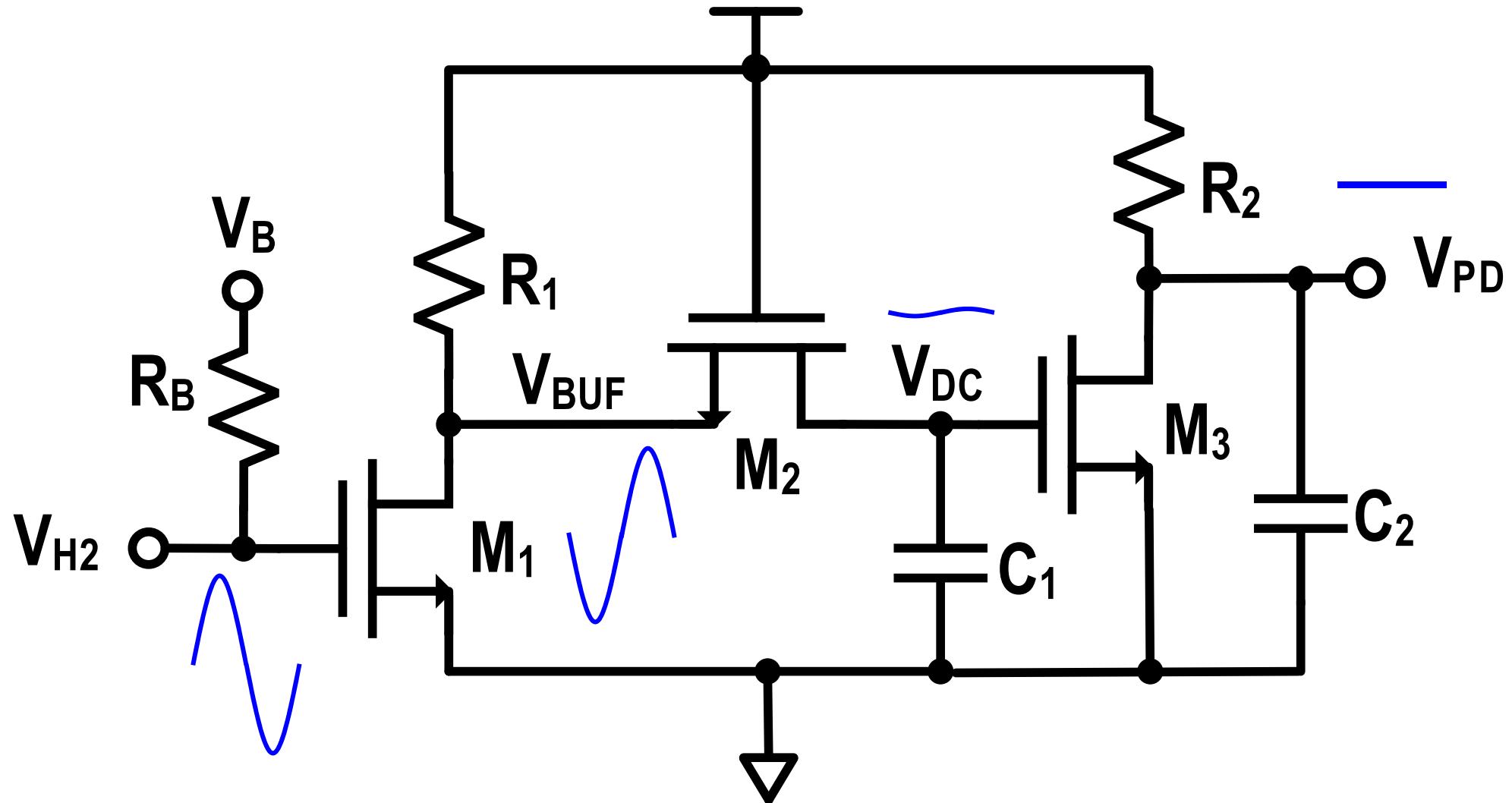


Peak detector



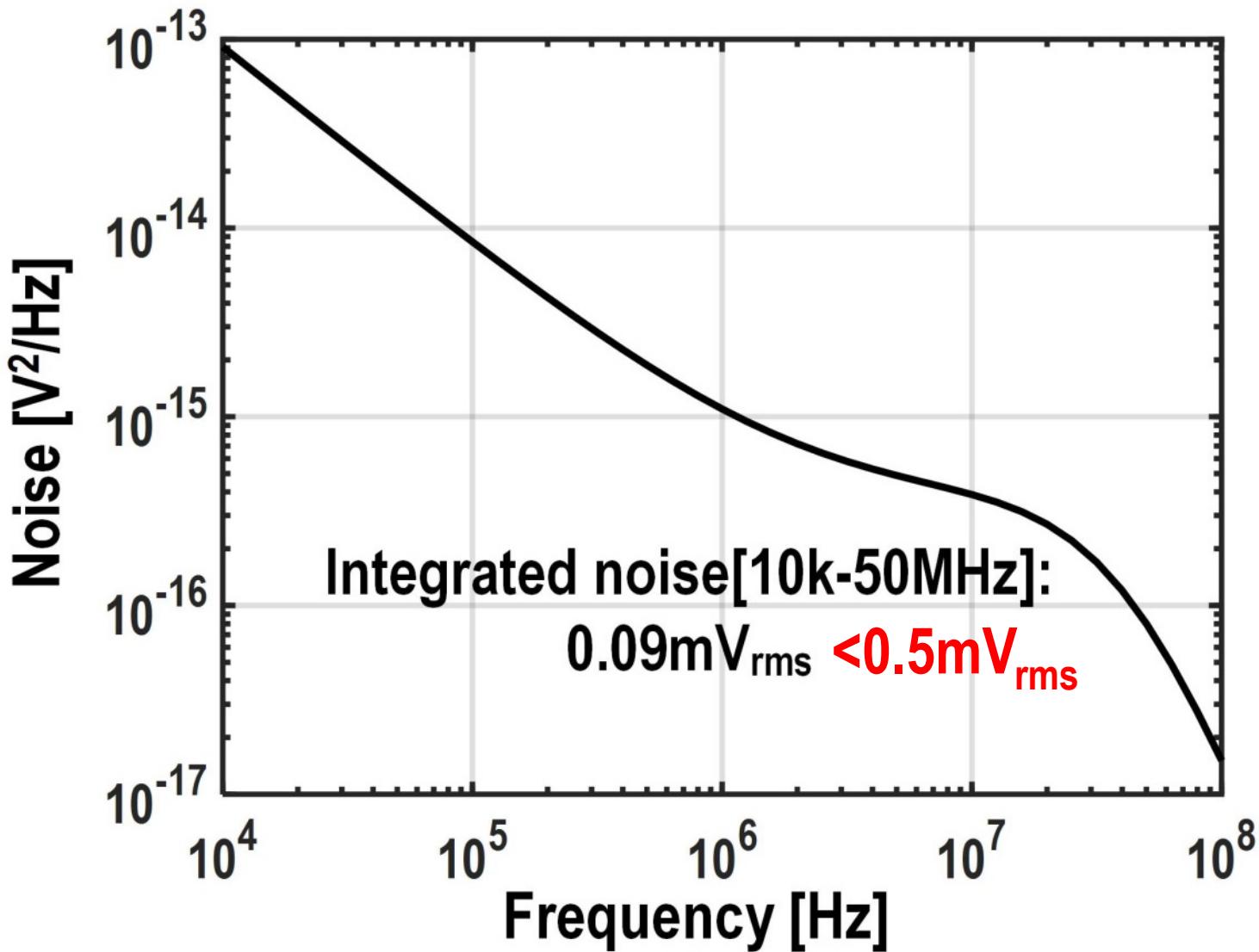
19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Peak detector



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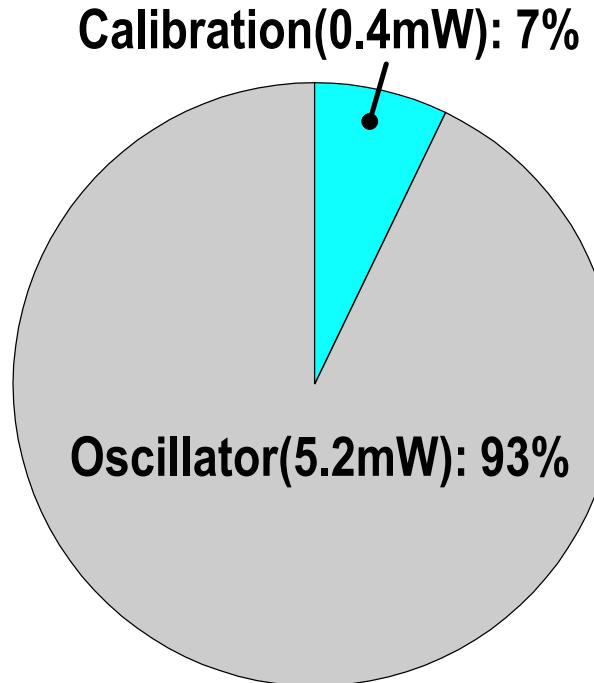
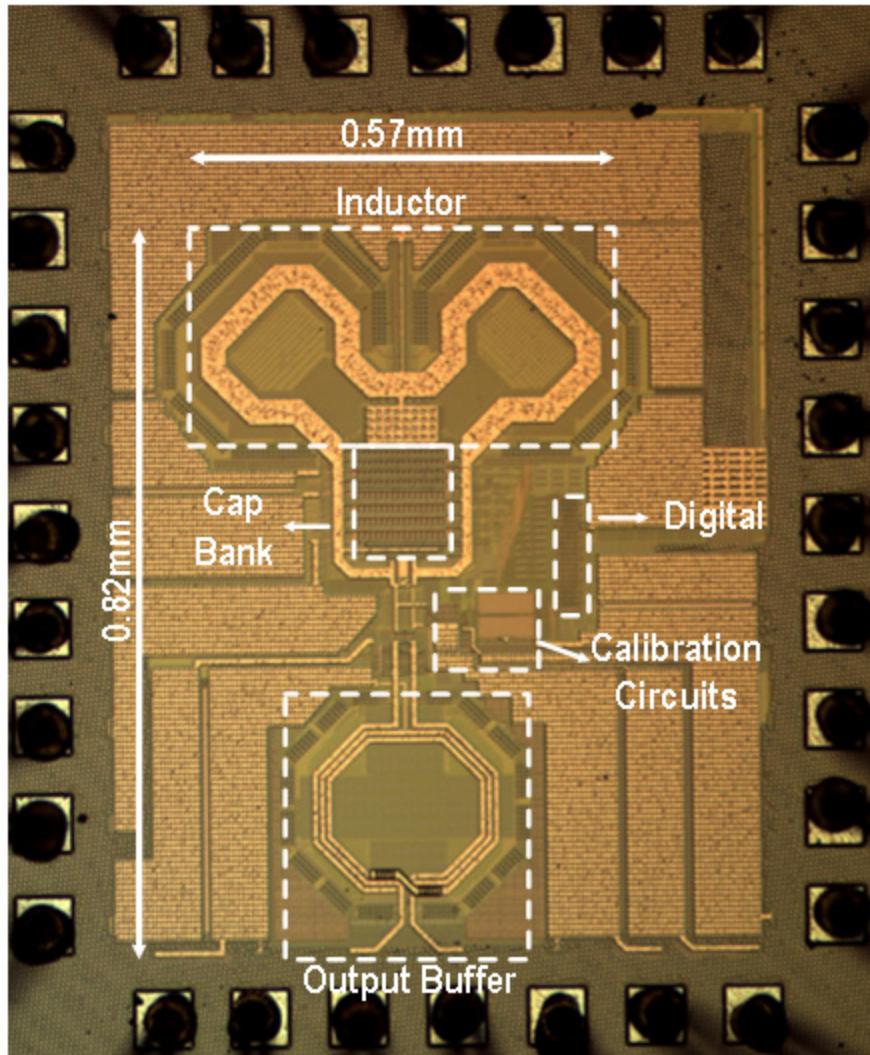
Simulated noise



Outline

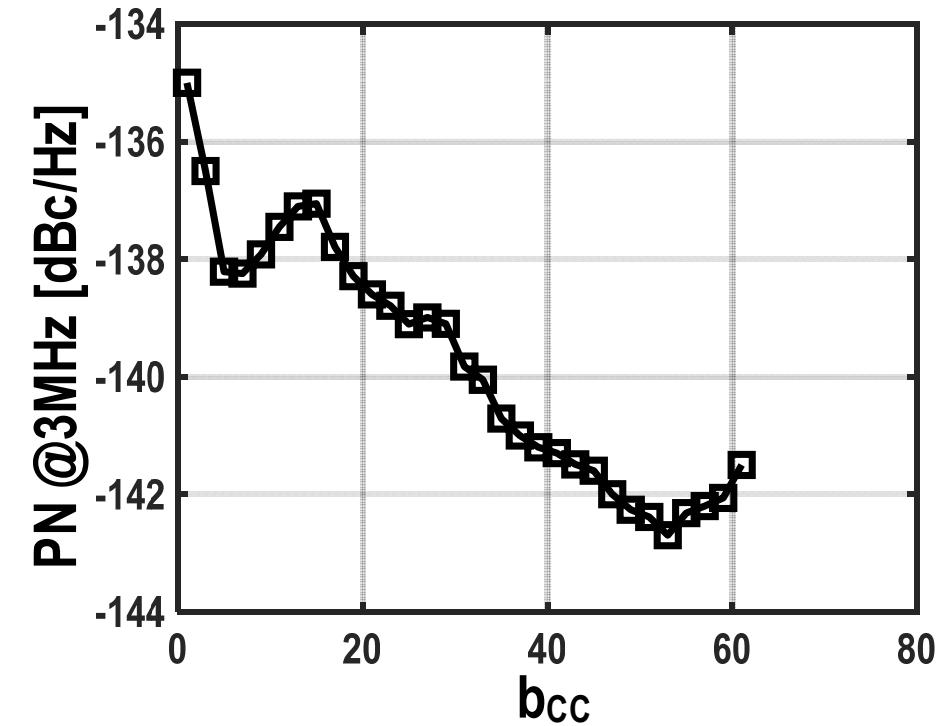
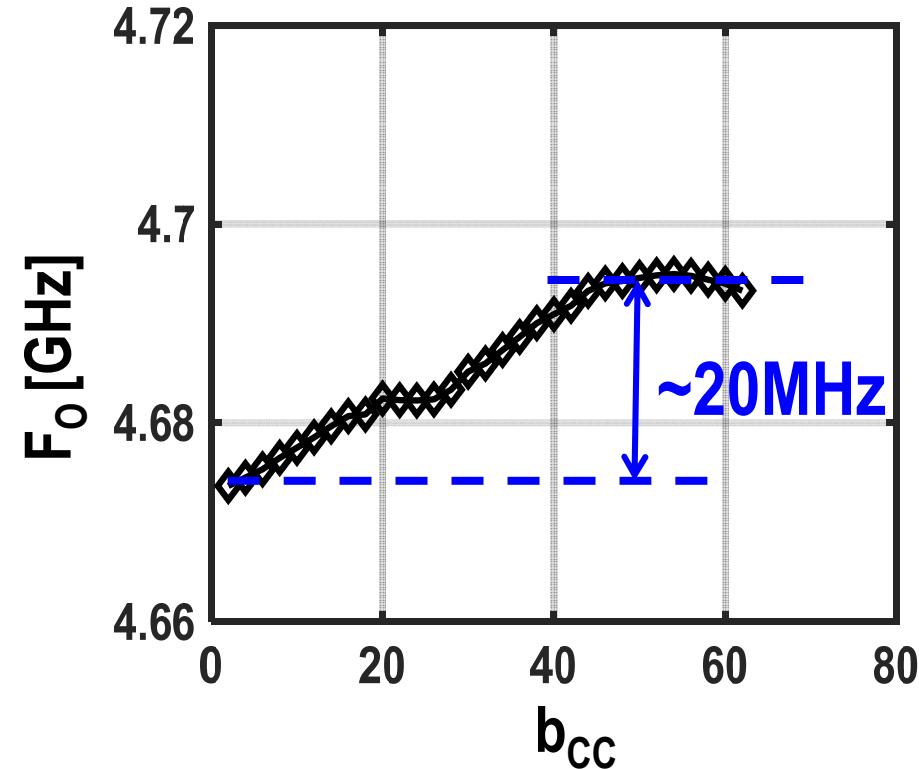
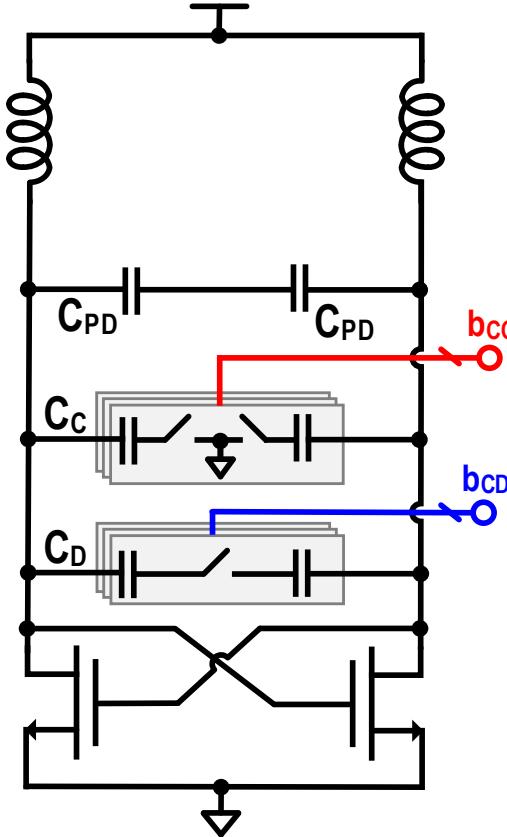
- Motivation
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- Circuit Implementation
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Chip micrograph



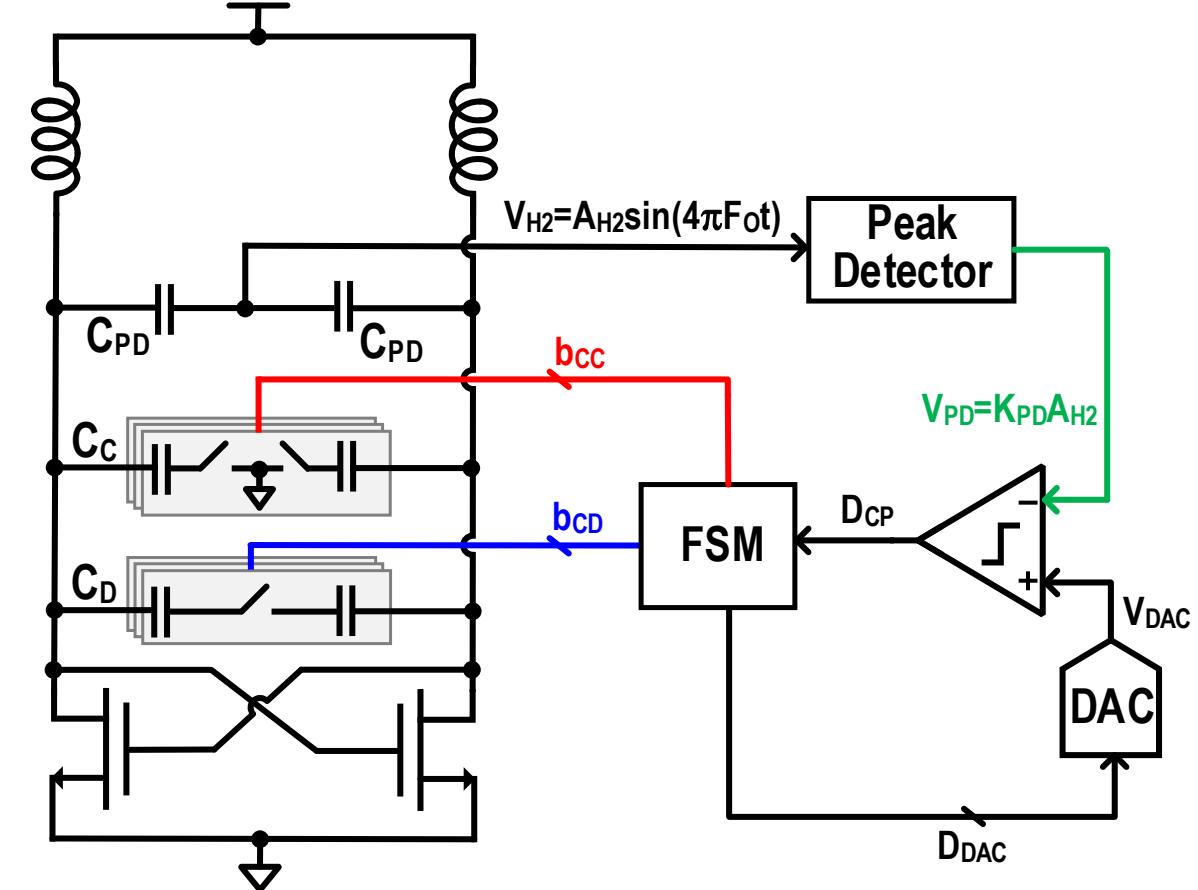
- 40nm bulk CMOS
- Frequency range: 4 – 5GHz
- 0.01mm² for calibration
- 0.4mW for calibration

Measured Frequency and Phase Noise vs. Single-ended Capacitor Control Code

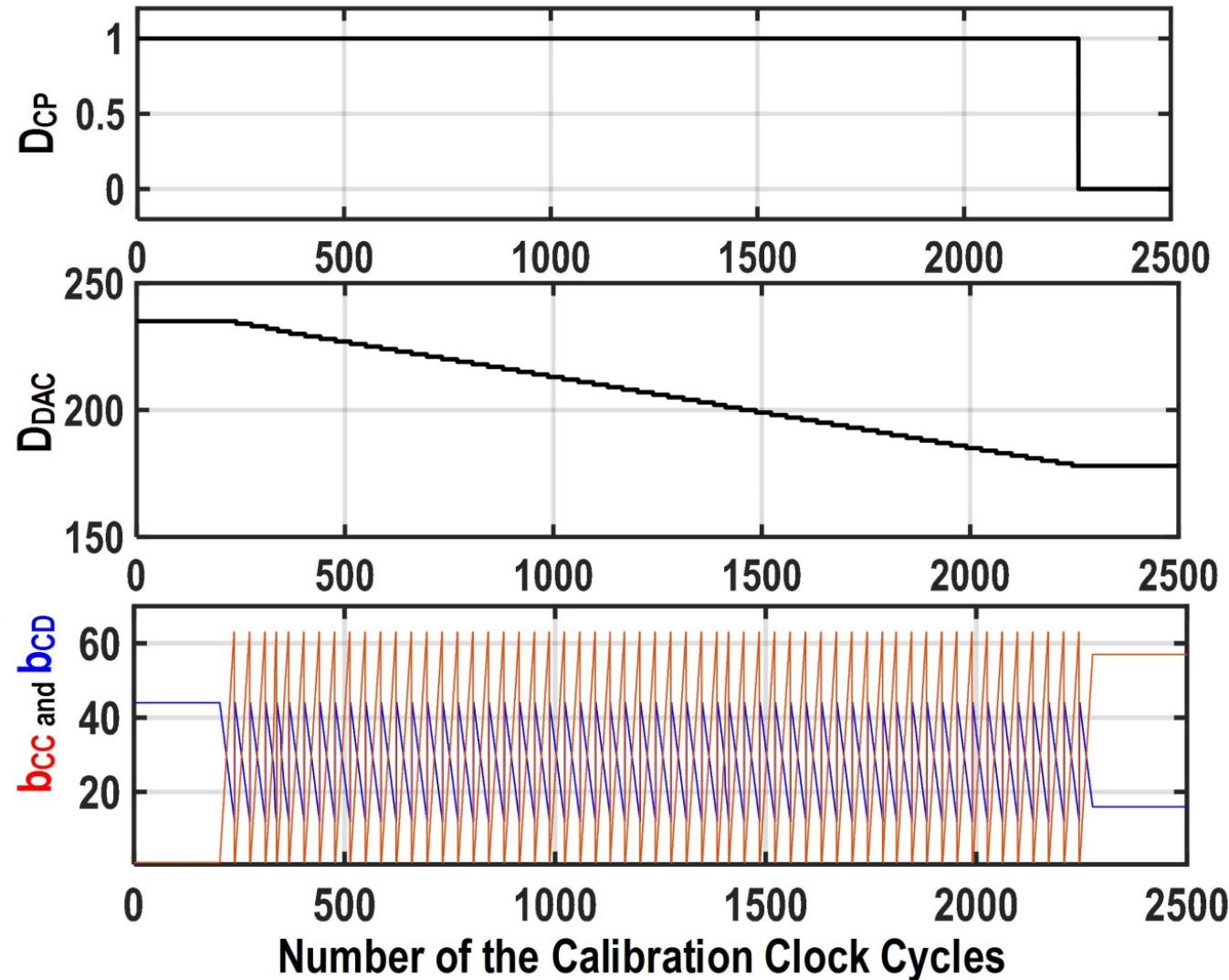


- b_{CC} and b_{CD} manually set for fixed F_0

Measured settling of the calibration loop

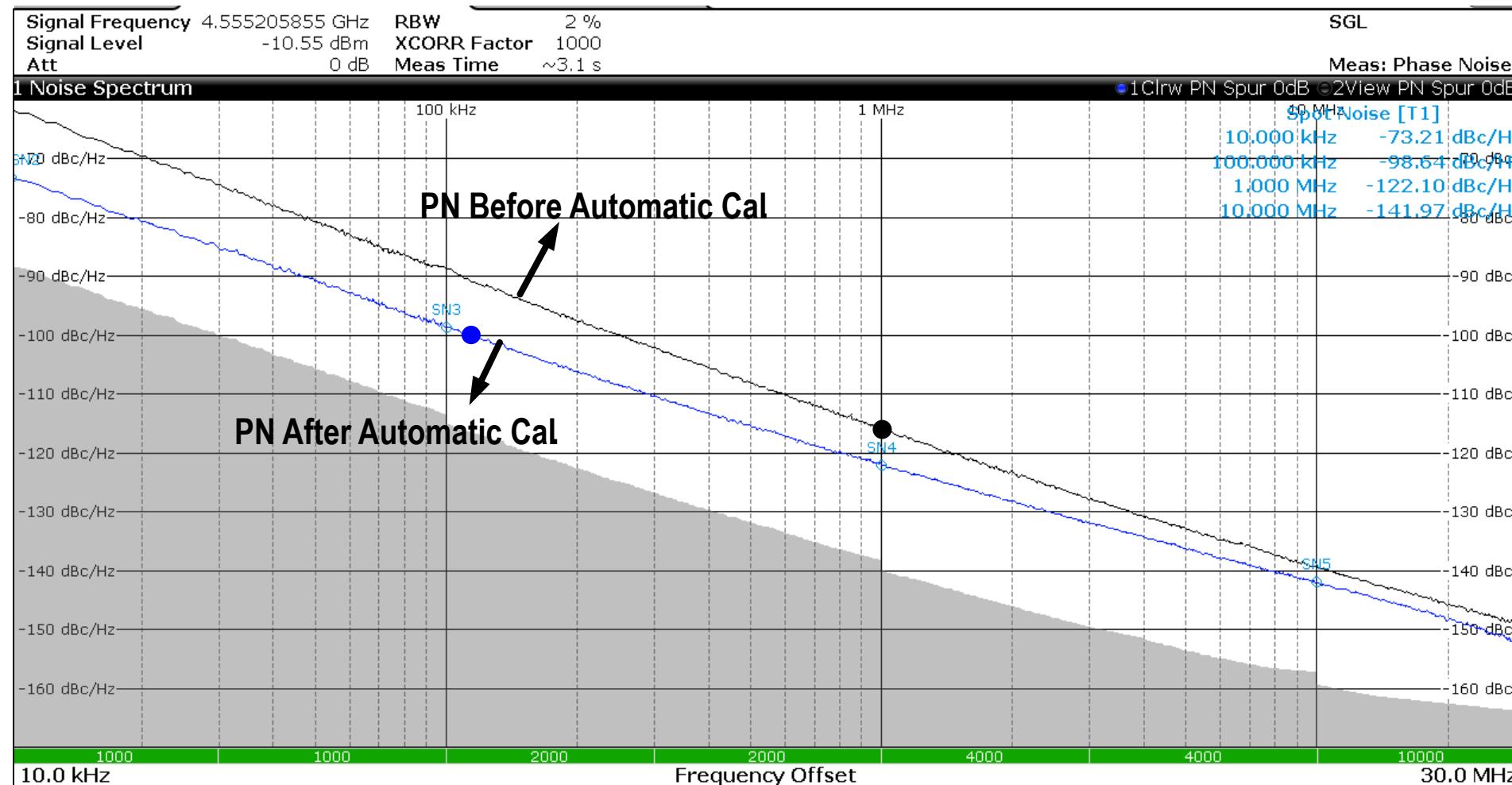


□ Calibration time: $\sim 40\mu\text{s}$



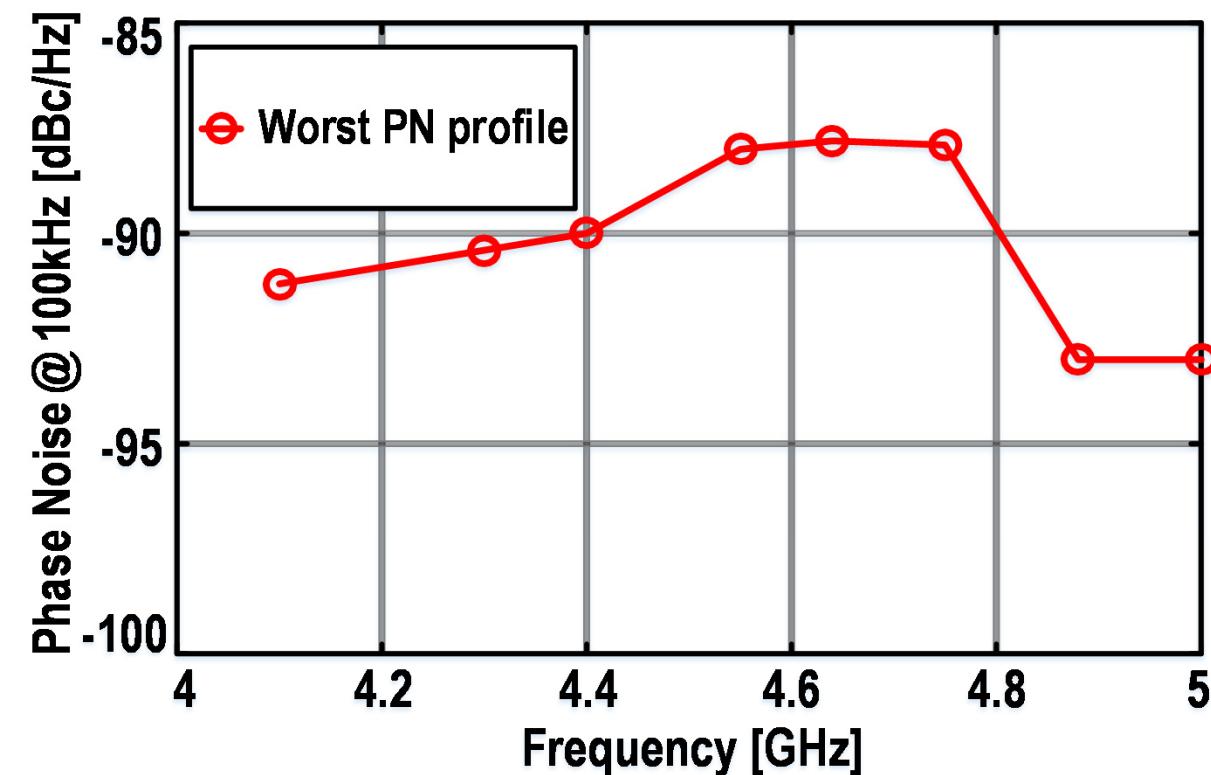
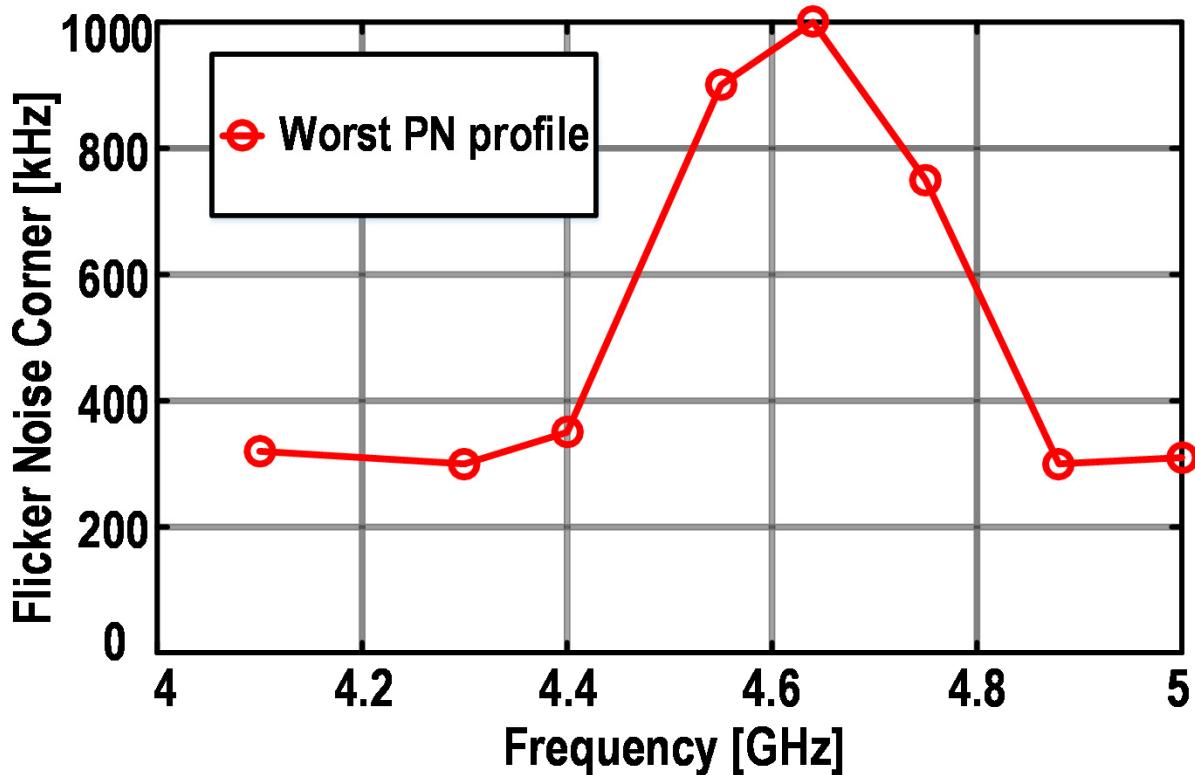
19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Measured phase noise at 300K

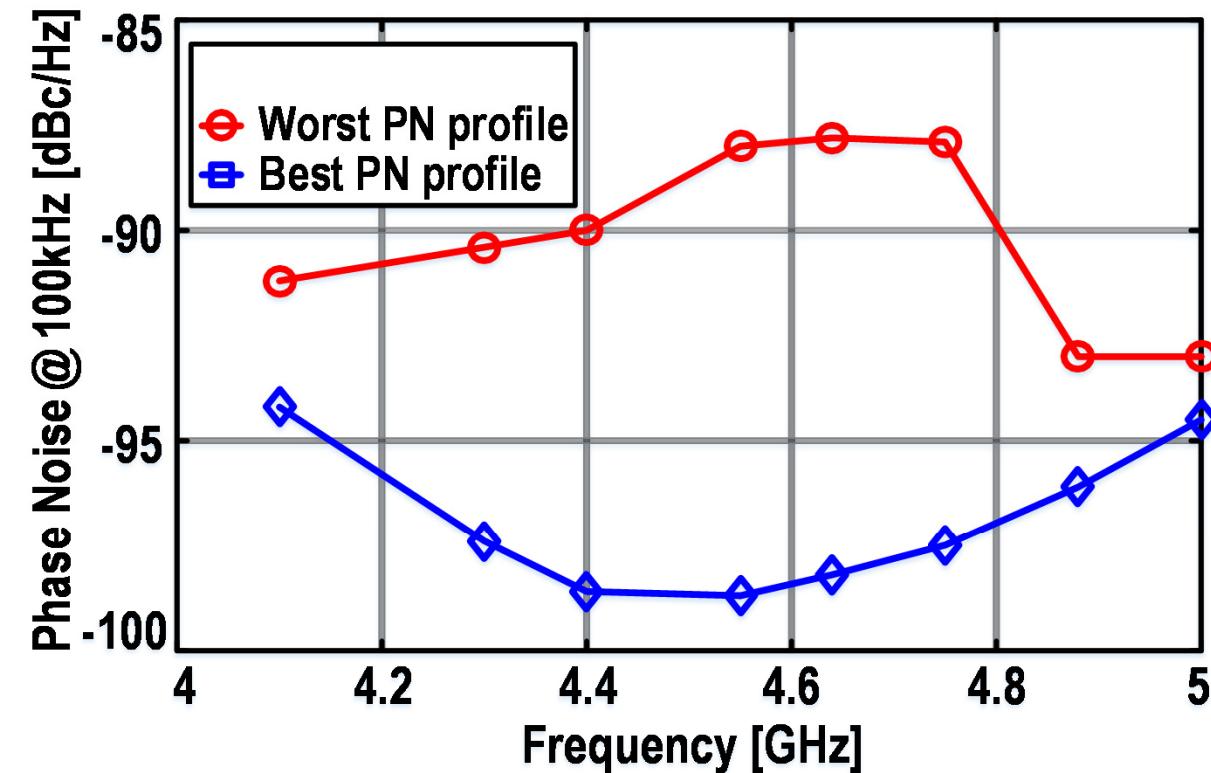
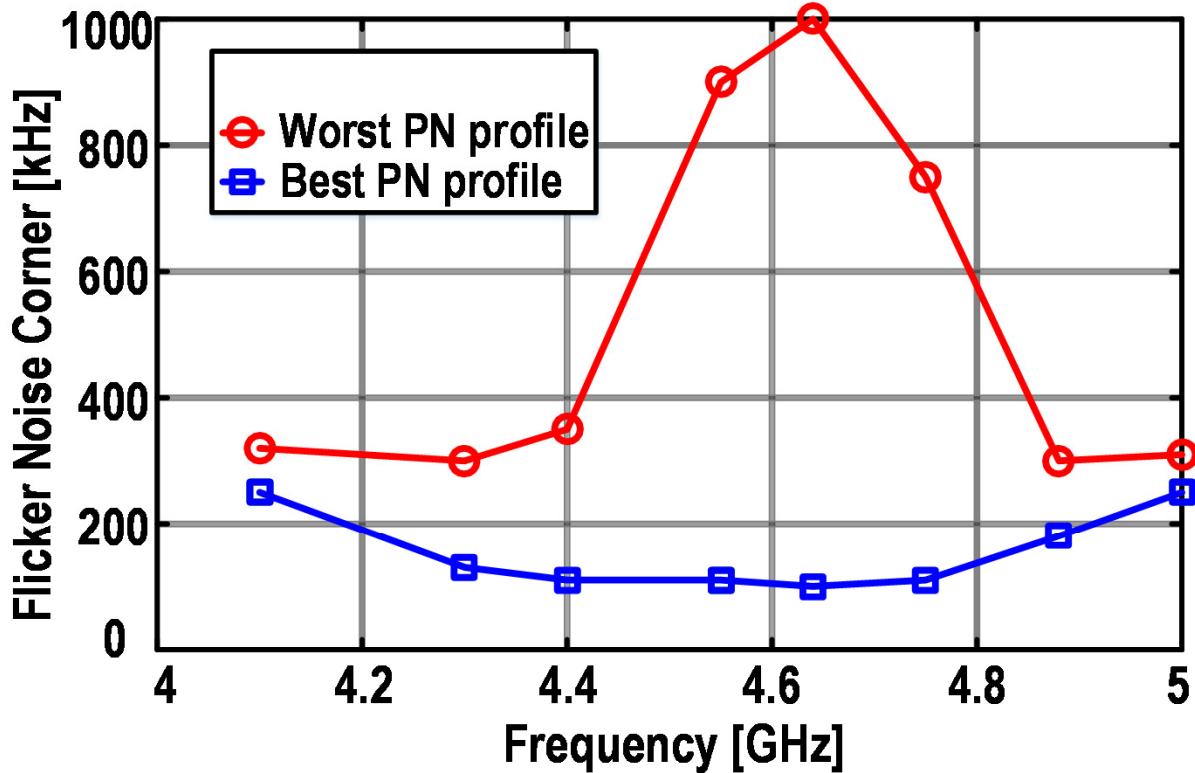


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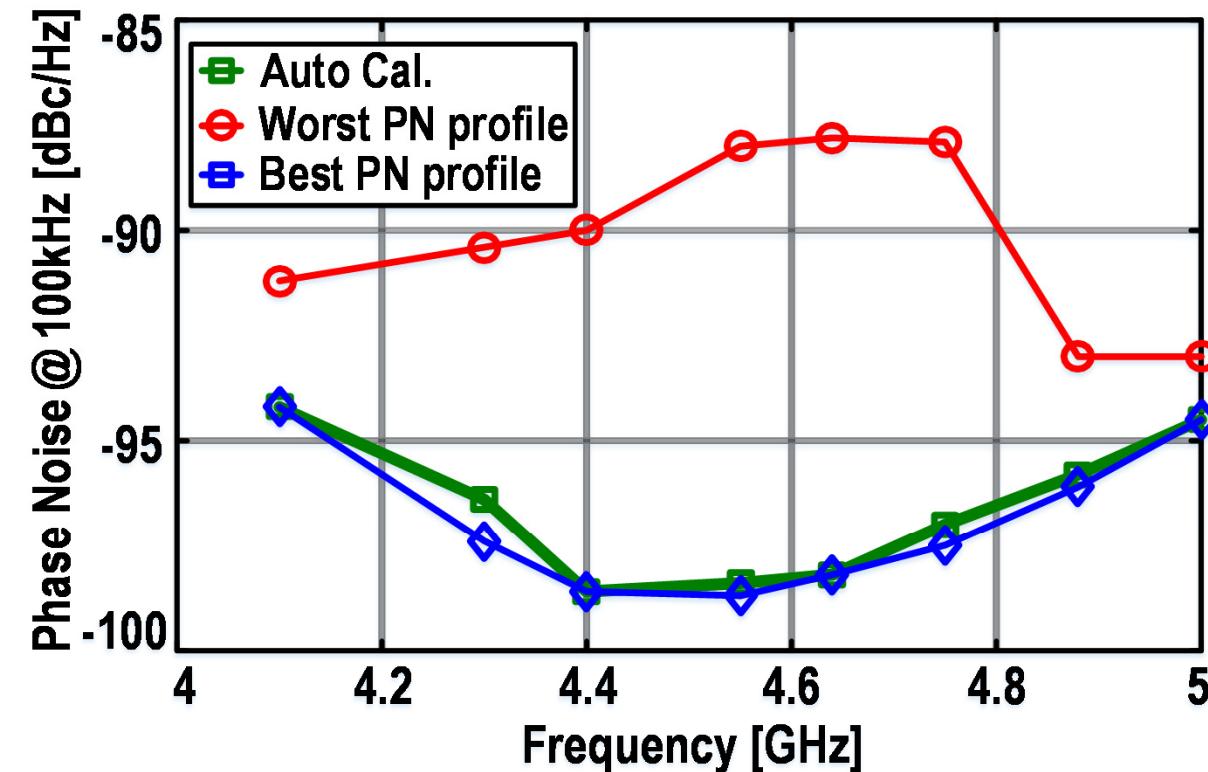
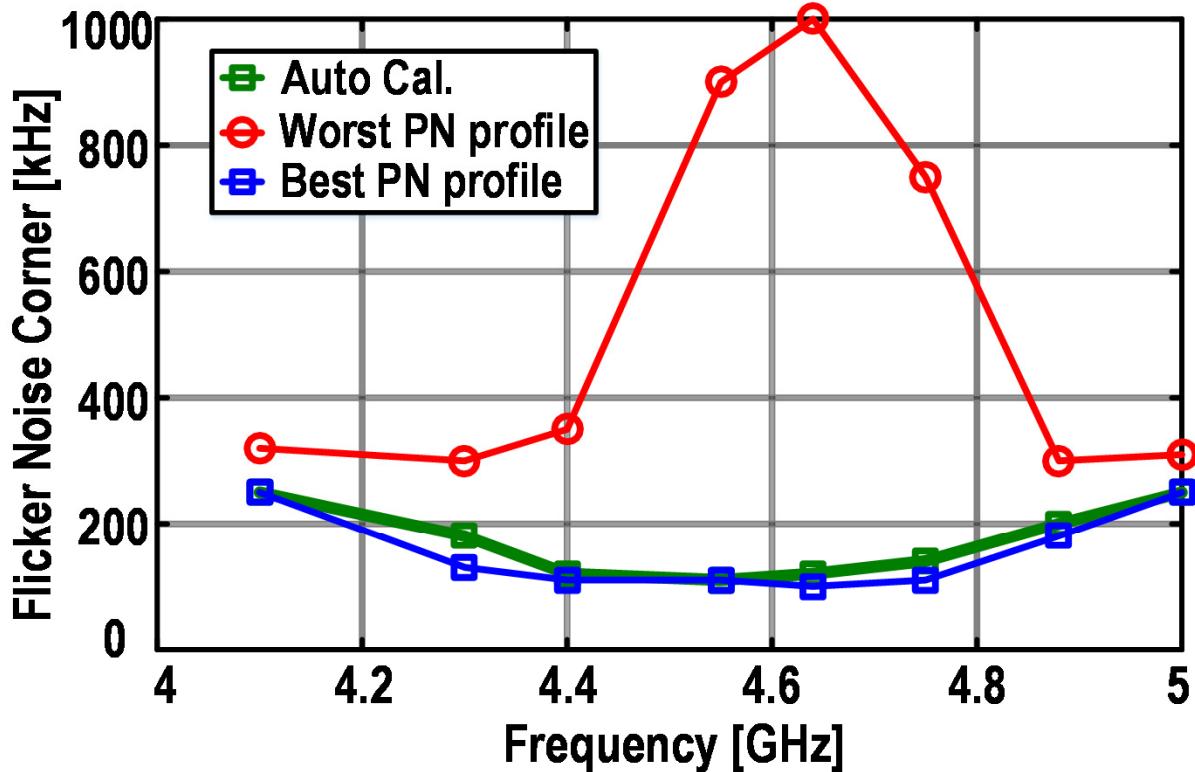
Measured phase noise and flicker corner at 300K



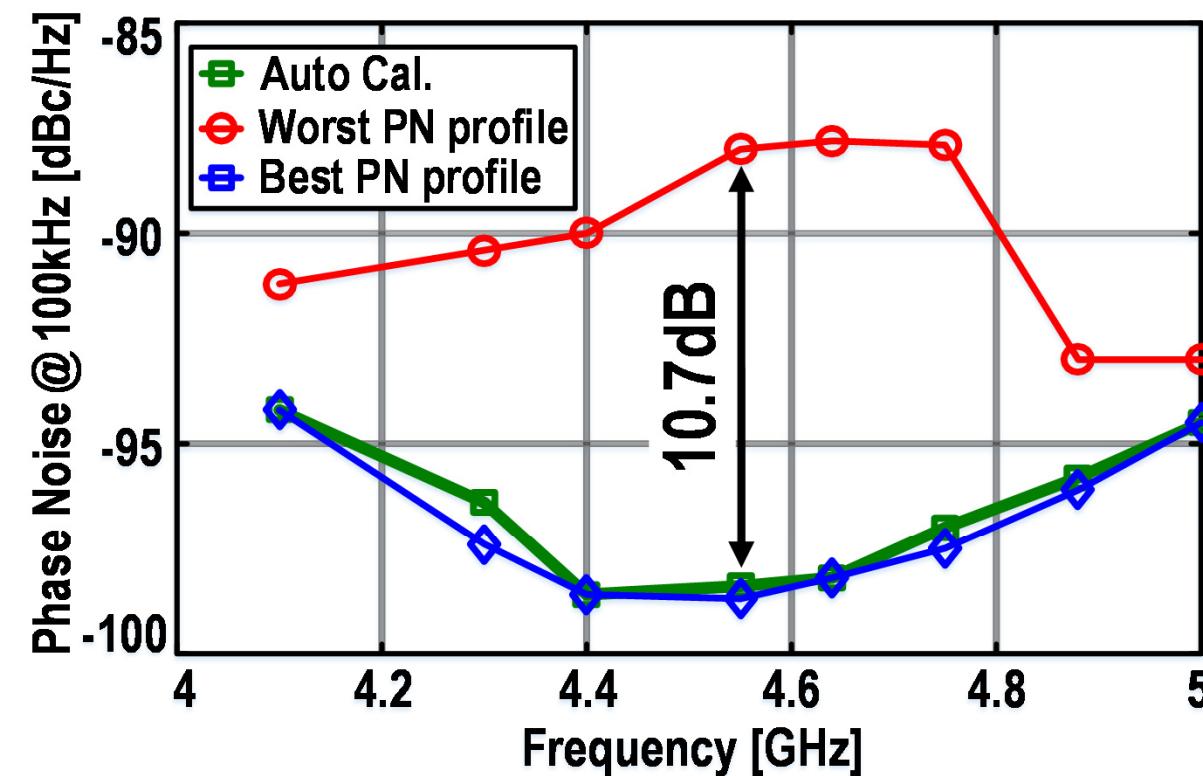
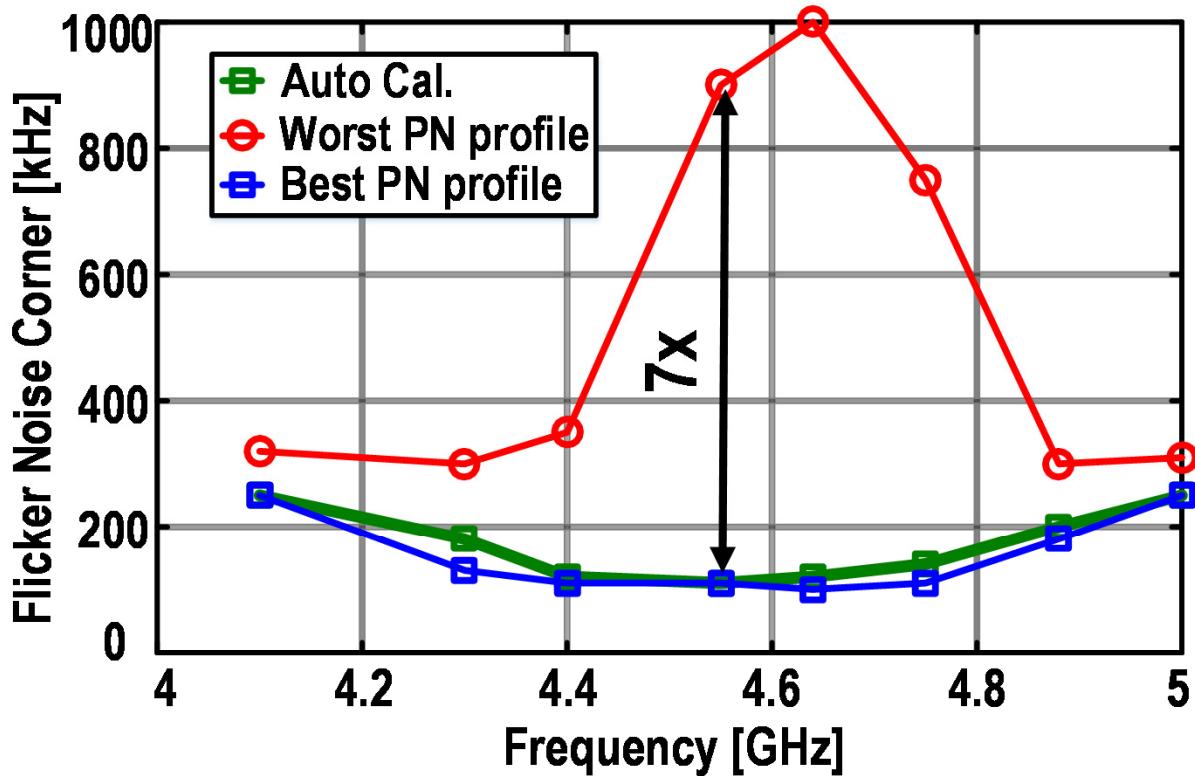
Measured phase noise and flicker corner at 300K



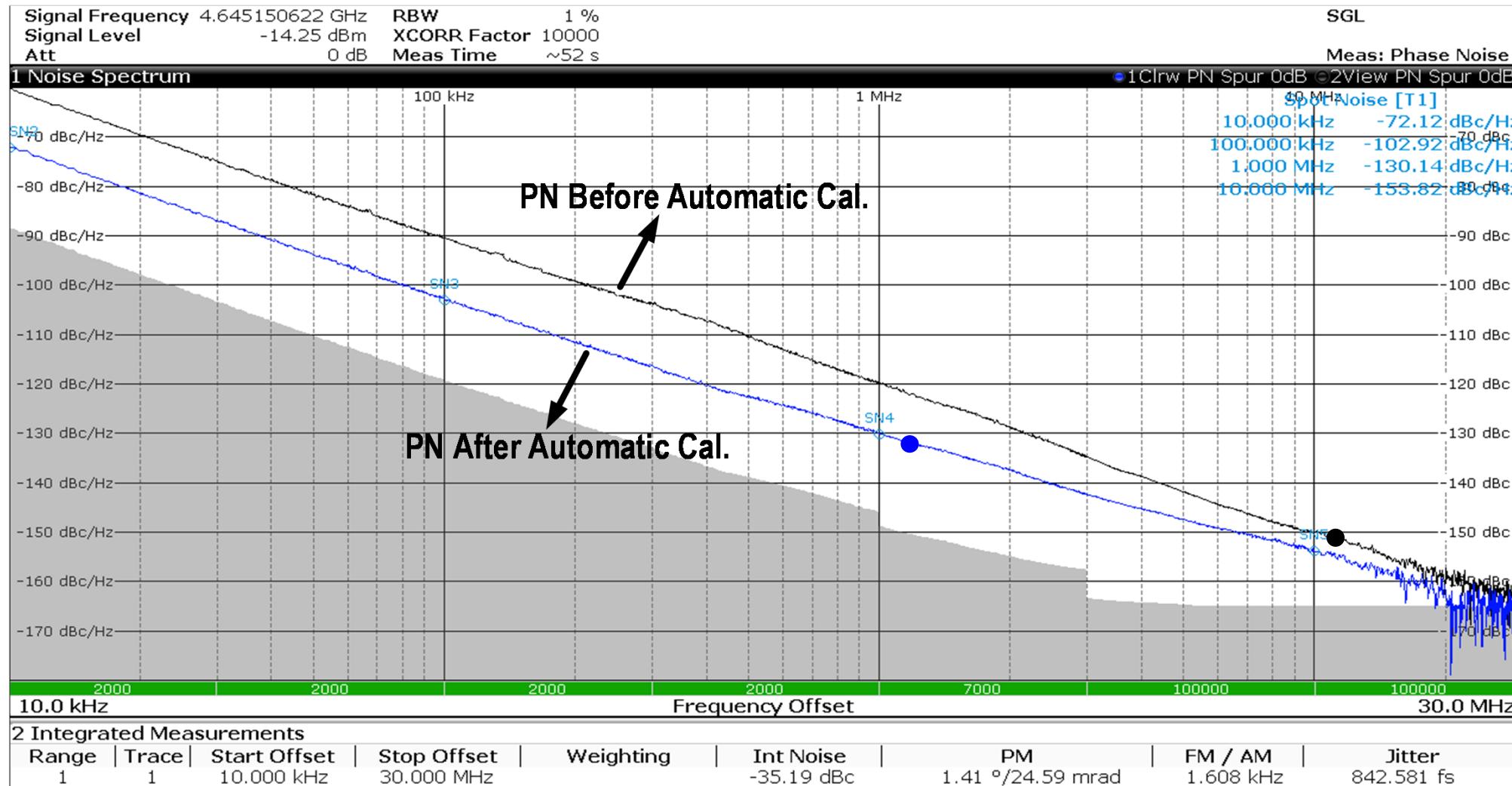
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Measured phase noise and flicker corner at 300K

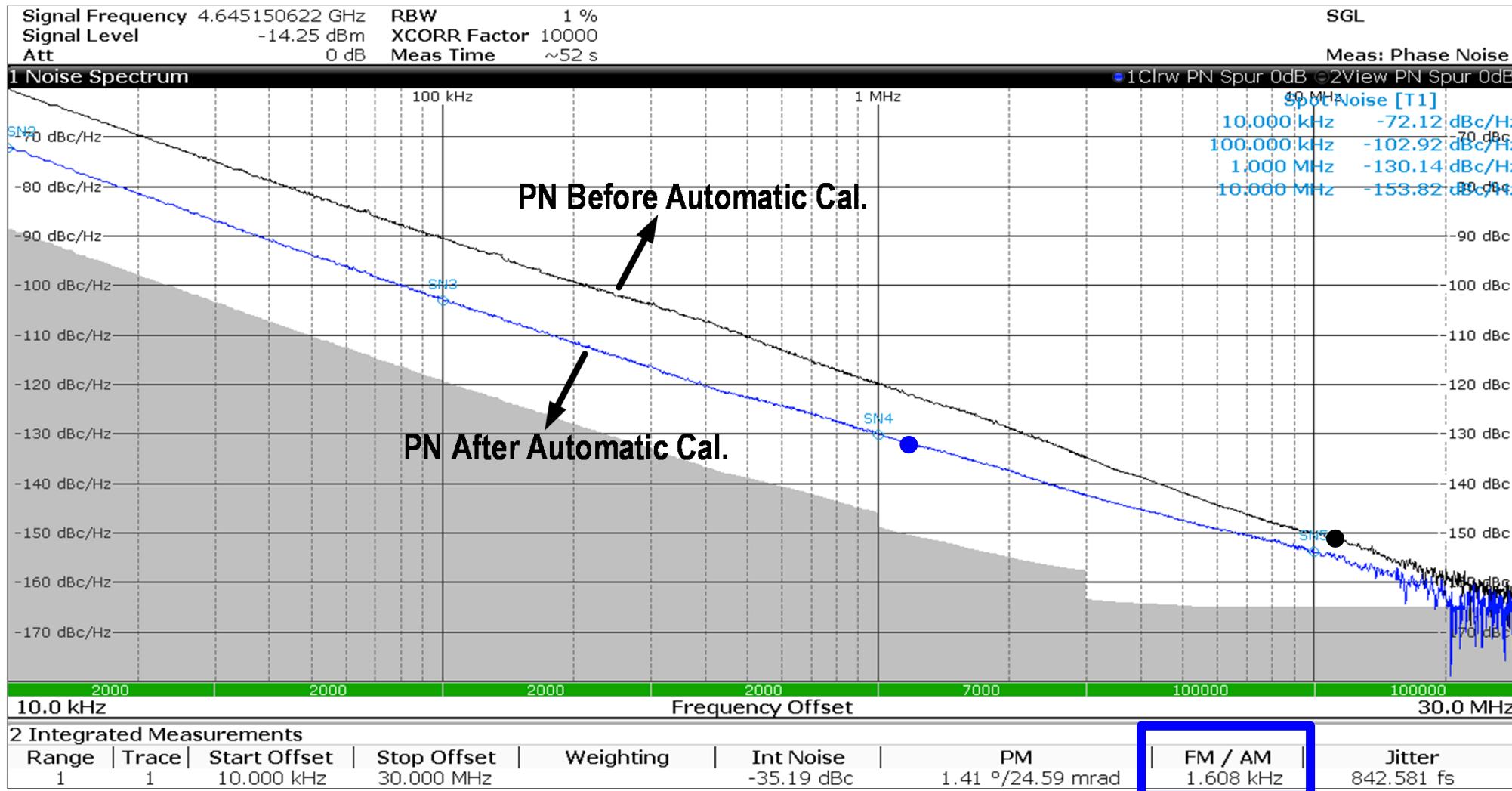


Measured phase noise at 4.2K



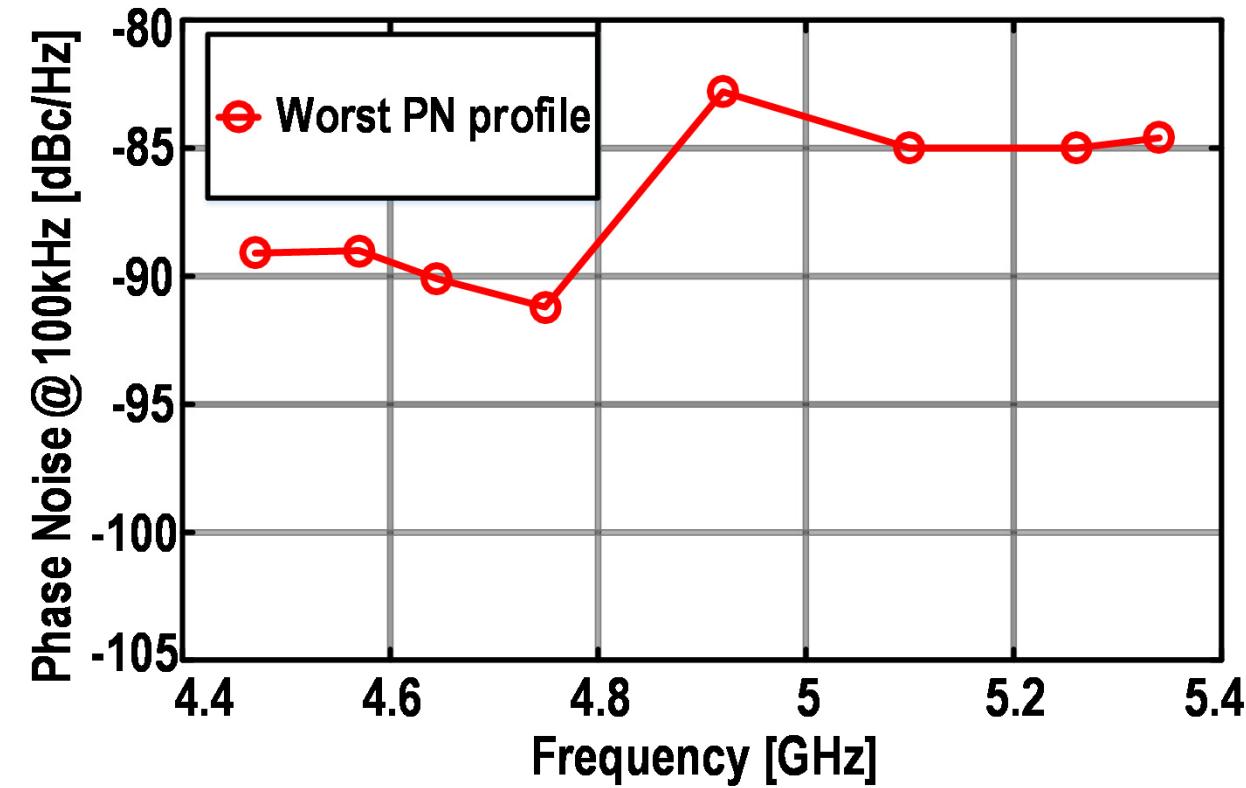
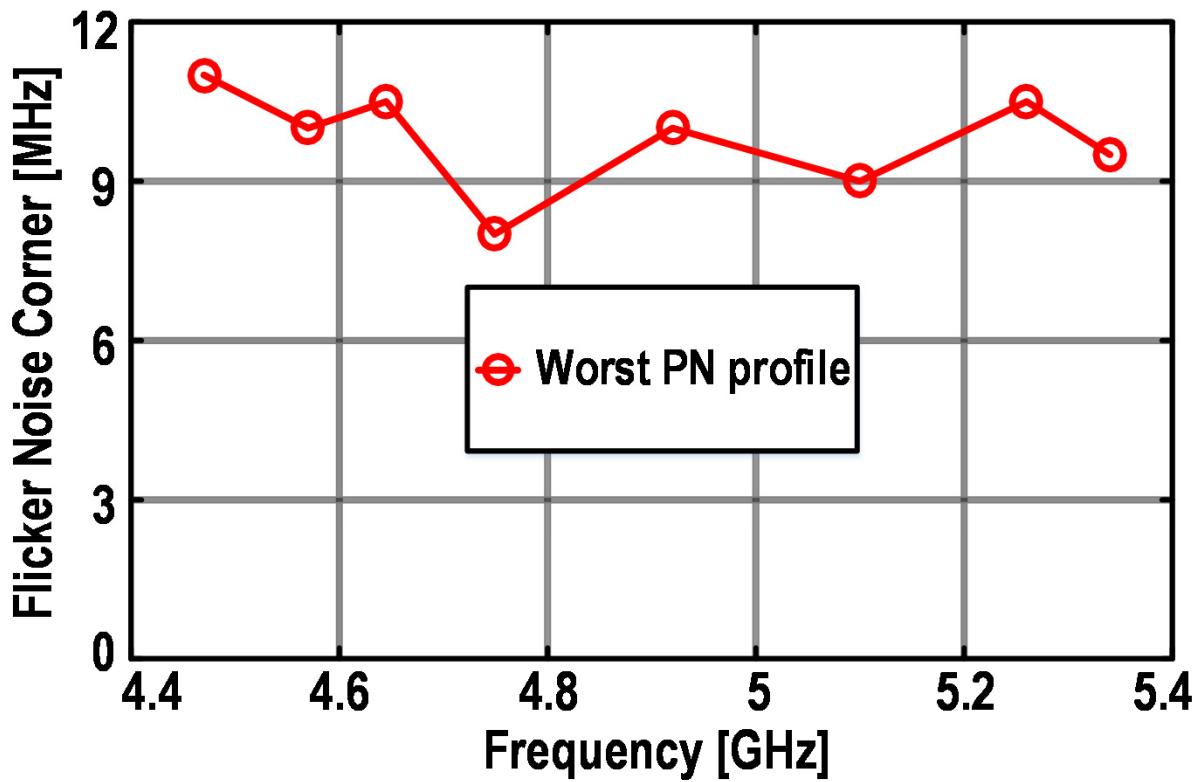
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Measured phase noise at 4.2K

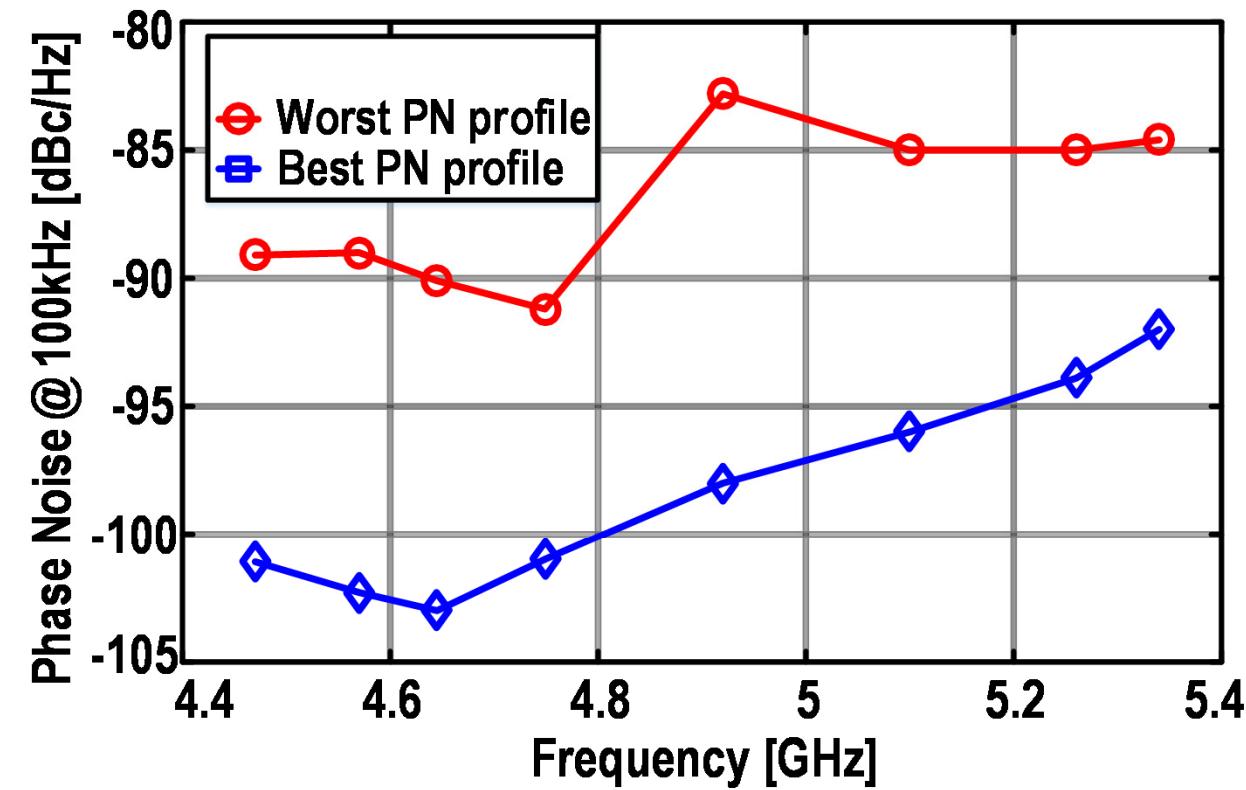
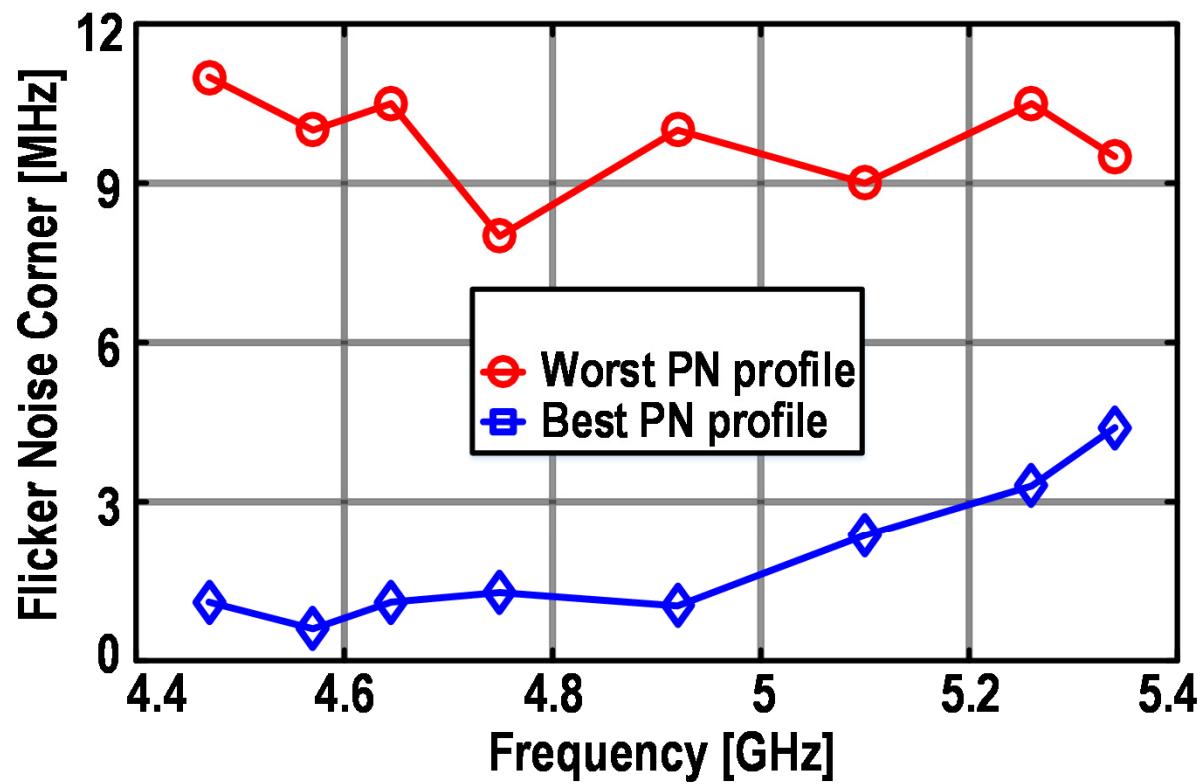


- 1.6kHz frequency noise ⇒ specifications are achieved

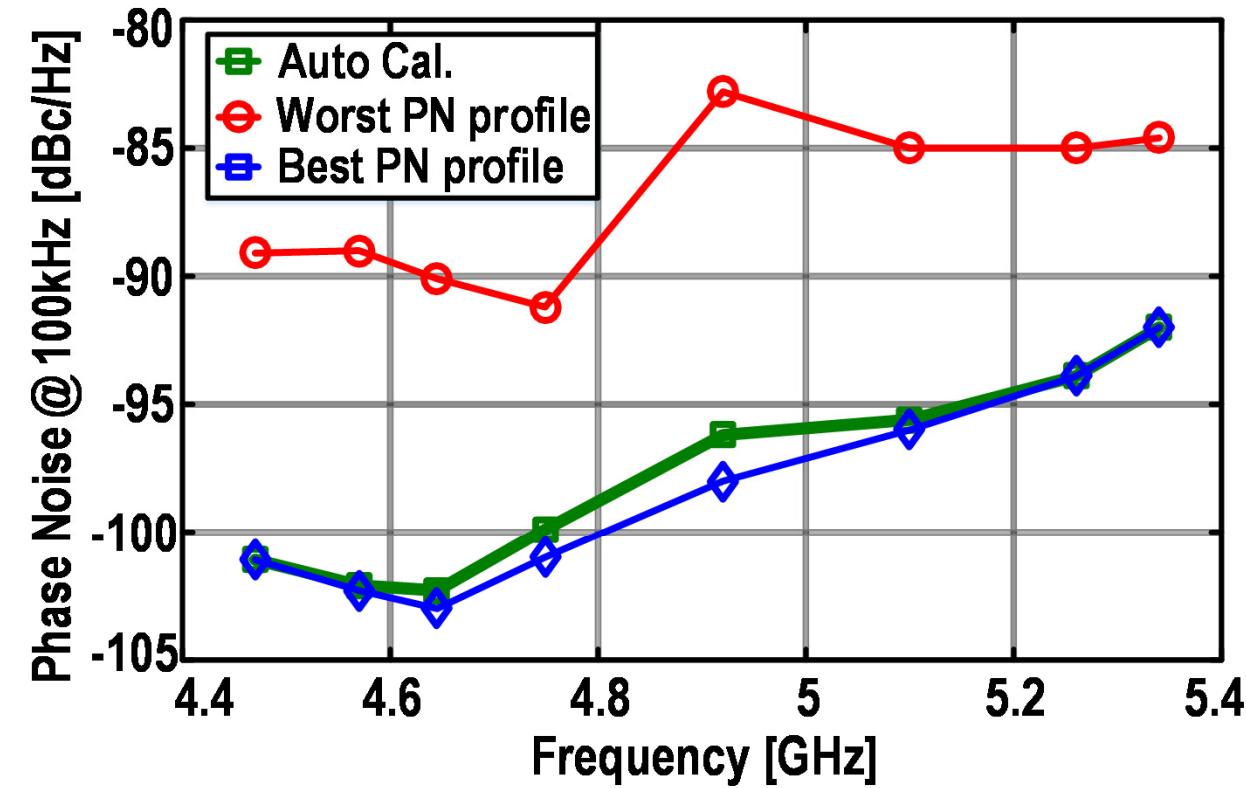
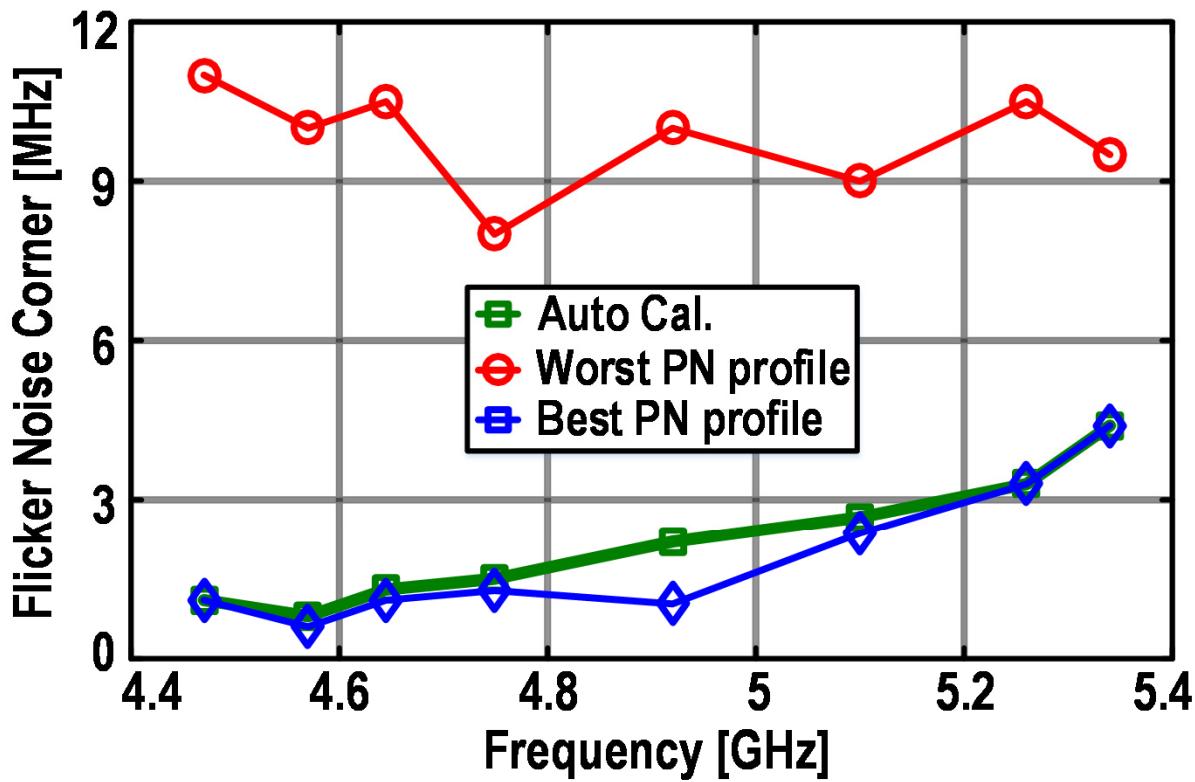
Measured phase noise and flicker corner at 4.2K



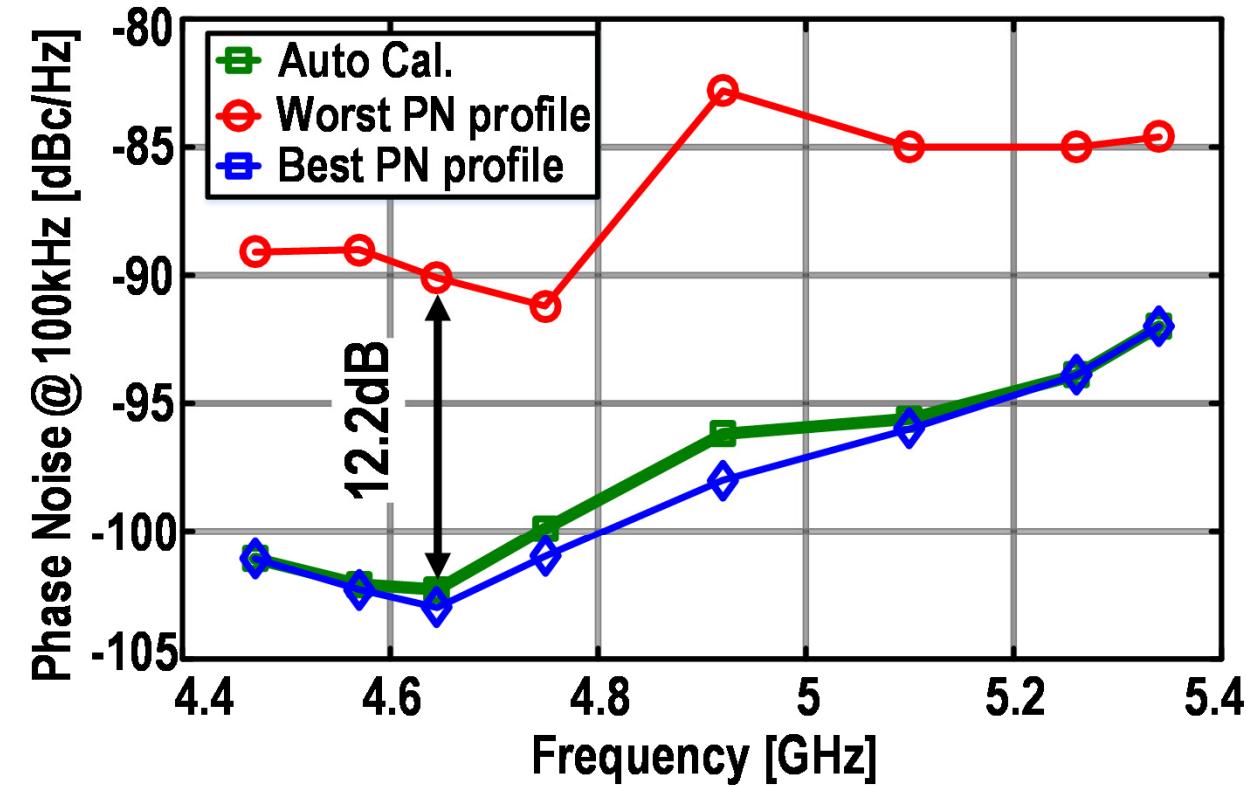
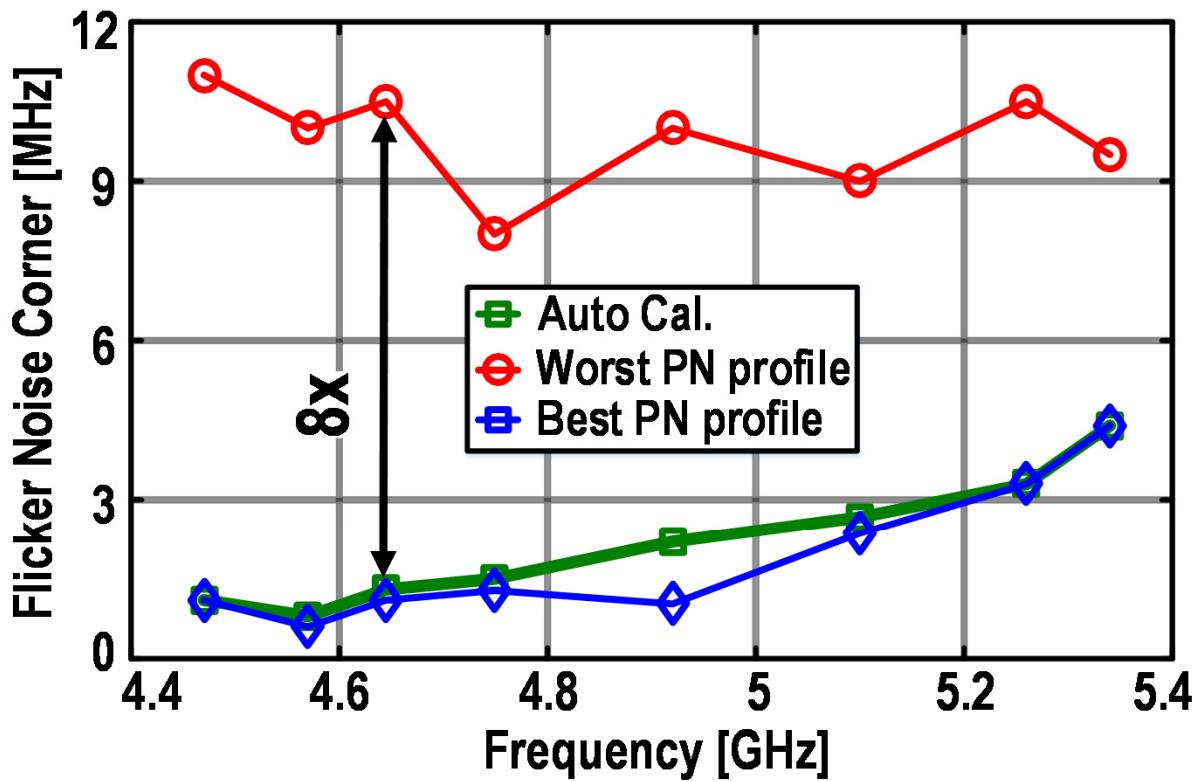
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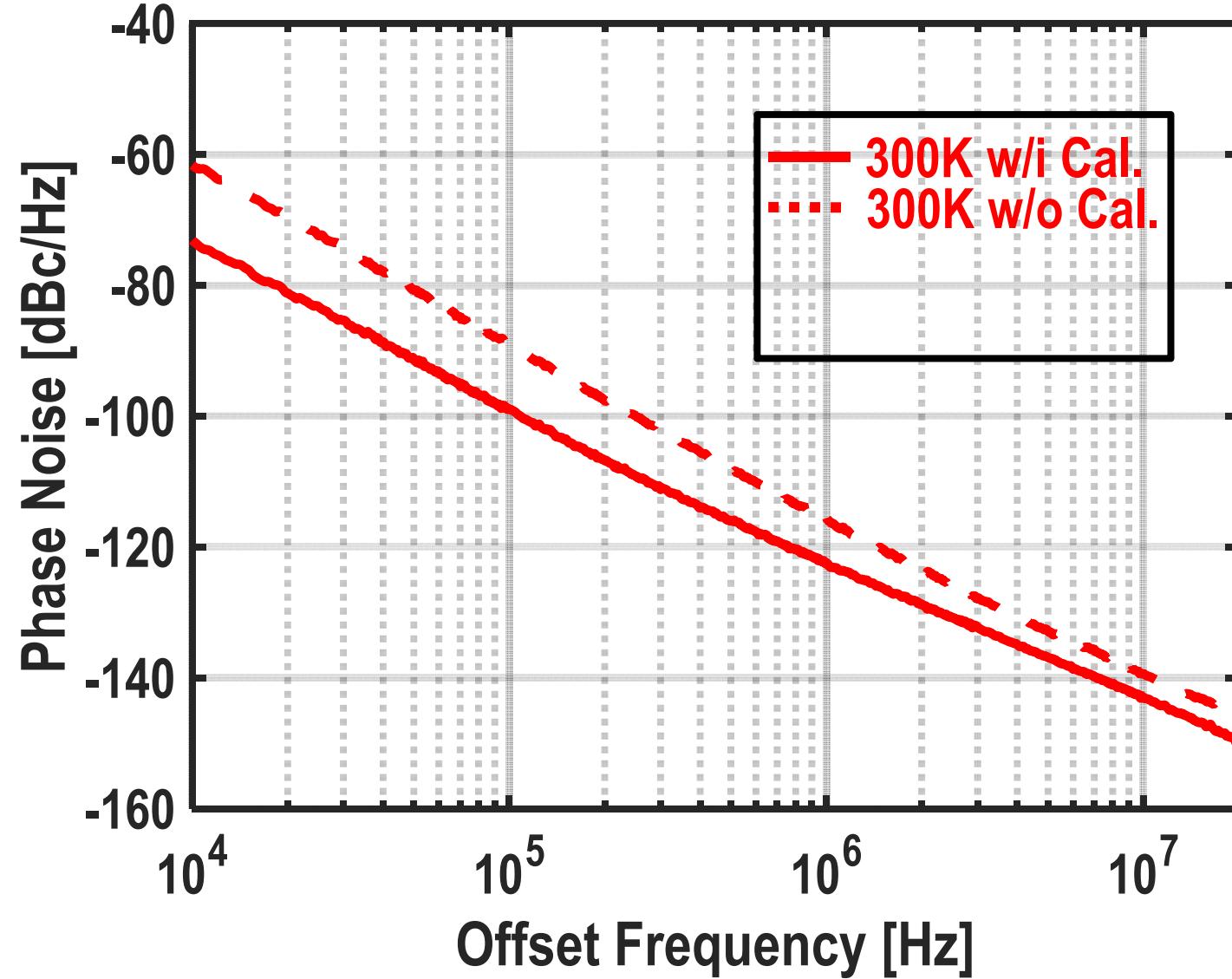
Measured phase noise and flicker corner at 4.2K



Measured phase noise and flicker corner at 4.2K

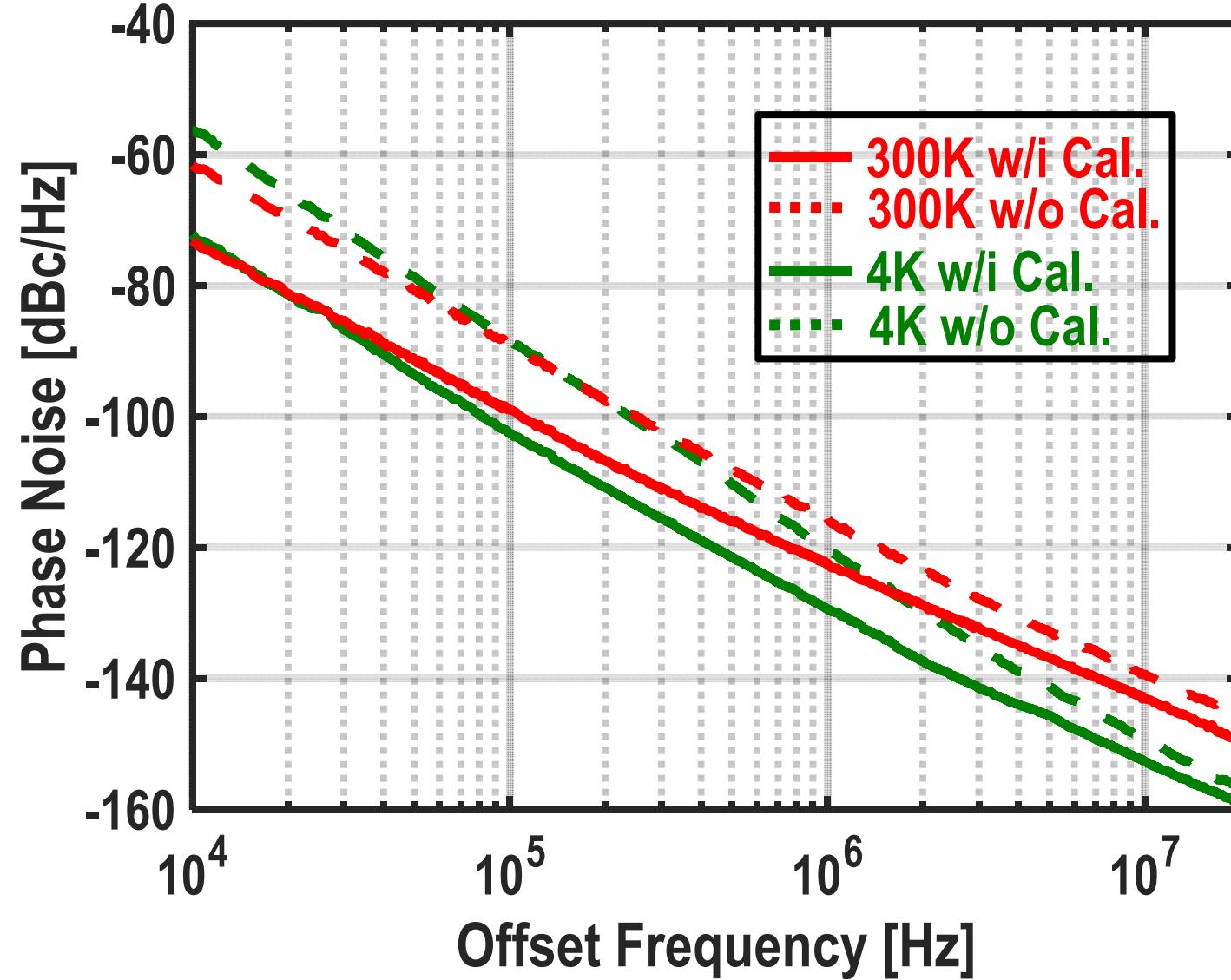


Measured phase noise – Summary



19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Measured phase noise – Summary



19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Performance comparison – 300K

	This Work	ISSCC'2015 [2]	ISSCC'2015 [3]	ISSCC'2018 [4]	JSSC'2015 [5]
Temperature [K]	300	300	300	300	300
Frequency [GHz]	4.6	3.3	7	4.51	8.4
Supply Voltage [V]	0.5	0.9	1	0.6	1.5
Tuning Range	4.1-5 (19.8%)	2.85-3.37 (27.2%)	5.4-7 (25%)	3.49-4.51 (25.5%)	7.4-8.4 (12.7%)
Power [mW]	4.3	6.8	10	1.14	20
PN [dBc/Hz] @100kHz/10MHz	-99.3/-143.1	-106*/-150.2*	-102.1/-144.5	-98.5/-143.7	-88*/-146.8
FOM [dBc/Hz] @100kHz/10MHz	186.2/190	188/192.2	188.9/191.4	191/196.2	173.5/192.3
Flicker Corner [kHz]	130	200	130	300	600
Technology	40nm	28nm	40nm	65nm	55nm
Osc. Area [mm ²]	0.14	0.19	0.13	0.14	0.17
Cal. Area [mm ²]	0.01	NA	NA	NA	NA
Inductor	One Turn	Two Turns	1:2 XFMR	2:4 XFMR	One turn+tail Ind.
Common-mode Resonance Cal.	Auto	Manual	Manual	Manual	NA

*Estimated from the measured phase noise plot of the oscillator

Performance comparison – 4.2K

	This Work	ISSCC'2017 [1]
Temperature [K]	4.2	4.2
Frequency [GHz]	4.65	6.3
Supply Voltage [V]	0.6	1
Tuning Range	4.4-5.3 (18.6%)	5.8-7.3(25%)
Power [mW]	5.3	12
PN [dBc/Hz] @100kHz	-102.9	-94
PN [dBc/Hz] @10MHz	-153.8	-149
FOM [dBc/Hz] @100kHz	189	179.2
FOM [dBc/Hz] @10MHz	200	194
Flicker Corner [kHz]	1300	5700
Technology	40nm	40nm
Osc. Area [mm ²]	0.14	0.13
Cal. Area [mm ²]	0.01	NA
Inductor	One Turn	1:2 XFMR
Common-mode Resonance Cal.	Auto	Manual

19.3: A 200dB FOM 4-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

Conclusions

- **Automatic common-mode resonance calibration**
 - General approach to minimize oscillator phase noise
- **Calibration effective at 4.2K**
 - Suppress the oscillator phase noise at 100kHz >10dB
 - 200dB FOM
- **State-of-the-art performance**
 - Low power (5mW)
 - Low frequency noise (1.6kHz)
- **Enable frequency synthesizers for quantum computers**