ISSCC 2020

SESSION 19

CRYO-CMOS for Quantum Technologies

A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for 4×32 Frequency Multiplexed Spin Qubits/Transmons in 22nm FinFET Technology for Quantum Computers

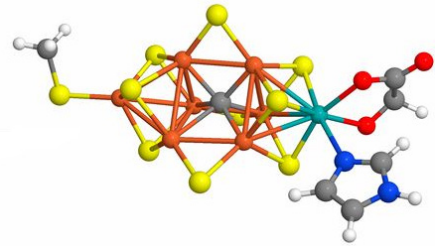
B. Patra*[1], J. P. G. van Dijk*[1], S. Subramanian[2], A. Corna[1], X. Xue[1],
C. Jeon[2], F. Sheikh[2], E. Hernandez[3], B. Esparza[3], H. Rampurawala[2], B. Carlton[2],
N. Samkharadze[4], S. Ravikumar[2], C. Nieva[2], S. Kim[2], H. Lee[2],
A. Sammak[4], G. Scappucci[1], M. Veldhorst[1], L. M. K. Vandersypen[1,2],
M. Babaie**[1], F. Sebastiano**[1], E. Charbon**[2,5], S. Pellerano**[2]

[1]Delft University of Technology, Delft, The Netherlands,
[2]Intel, Hillsboro, OR, [3]Intel, Guadalajara, Mexico,
[4]TNO, Delft, The Netherlands, [5]EPFL, Neuchatel, Switzerland

*Equally-Credited Authors (ECAs), **Equally-Credited Authors (ECAs)

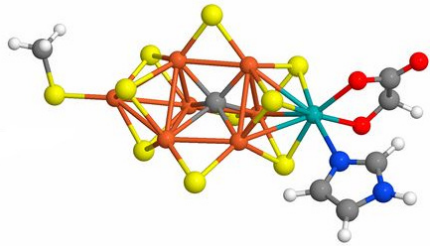
Why quantum computing?

- Exponential speed up for classically intractable problems:
  - Quantum chemistry



Why quantum computing?

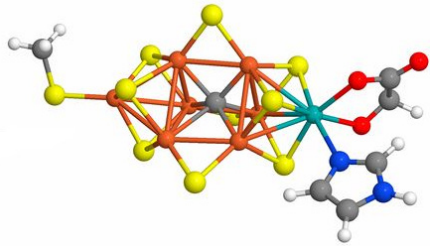
- Exponential speed up for classically intractable problems:
  - Quantum chemistry



  - Optimization problems

Why quantum computing?

- Exponential speed up for classically intractable problems:
  - Quantum chemistry

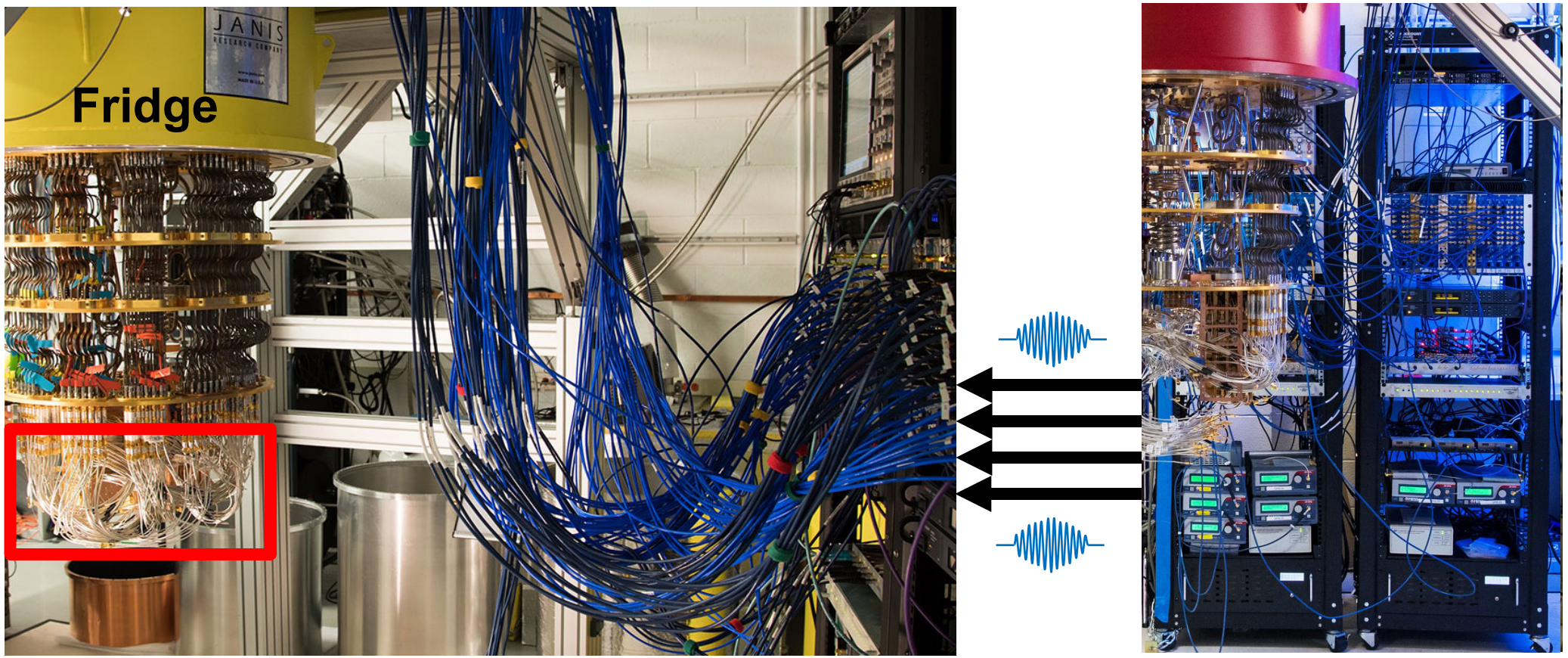


  - Optimization problems

  - Cryptography

Largest quantum computer < 100 qubits

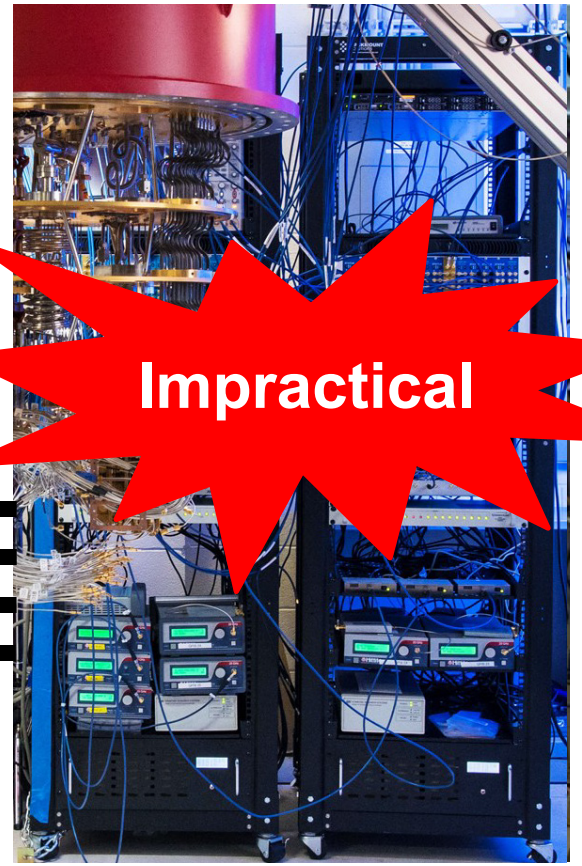
Qubits



[Bardin, 2019]

Largest quantum computer < 100 qubits

- Scalability: cabling becoming impractical



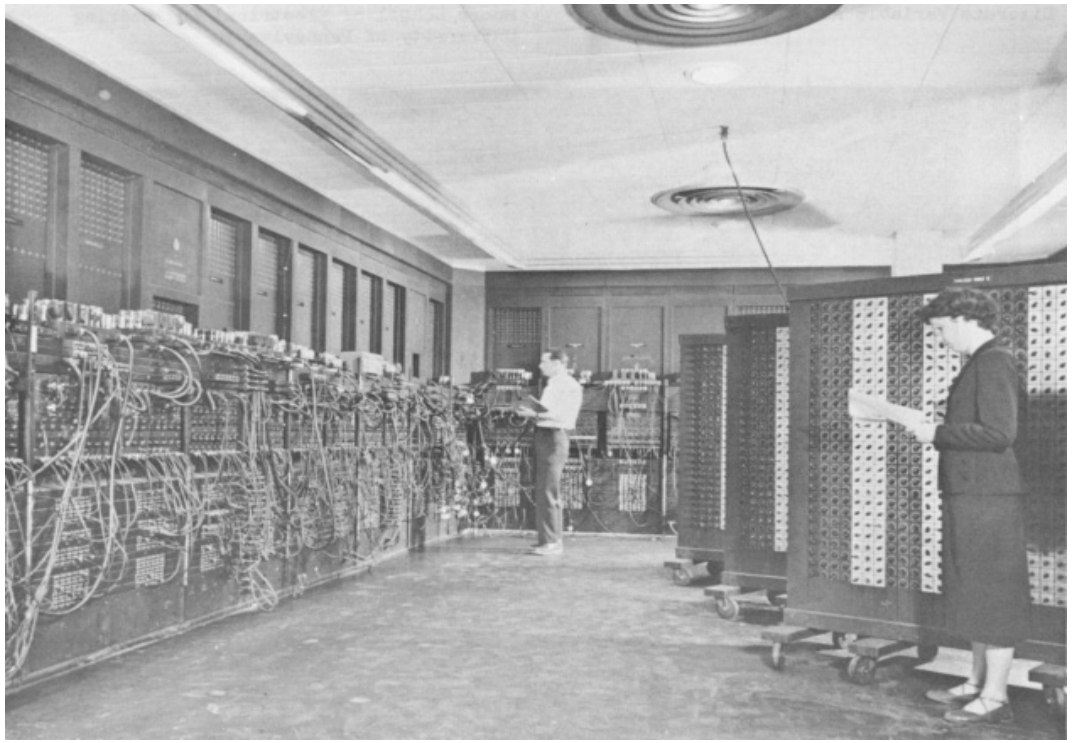
Impractical

1 Million qubits

Qubits

[Bardin, 2019]

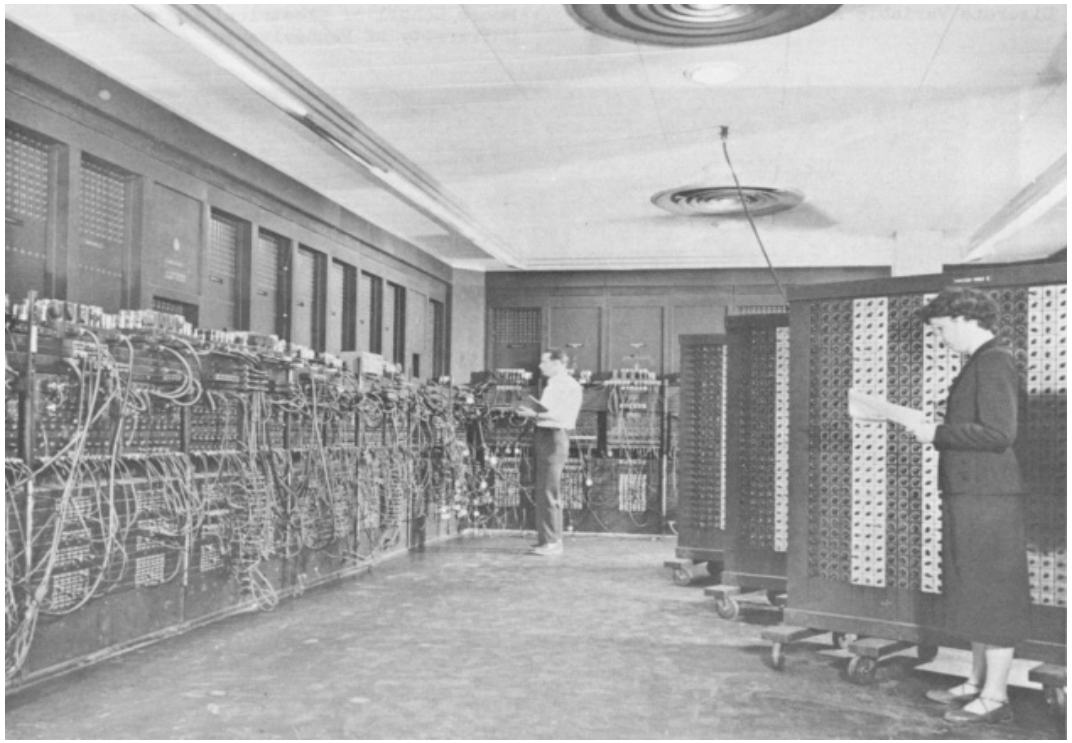
What can we learn from history?

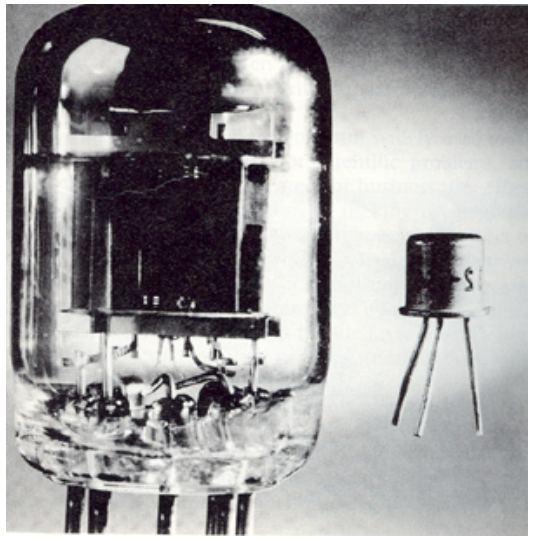


ENIAC (Vacuum tube)

What can we learn from history?

- Miniaturization – Vacuum tube to transistors

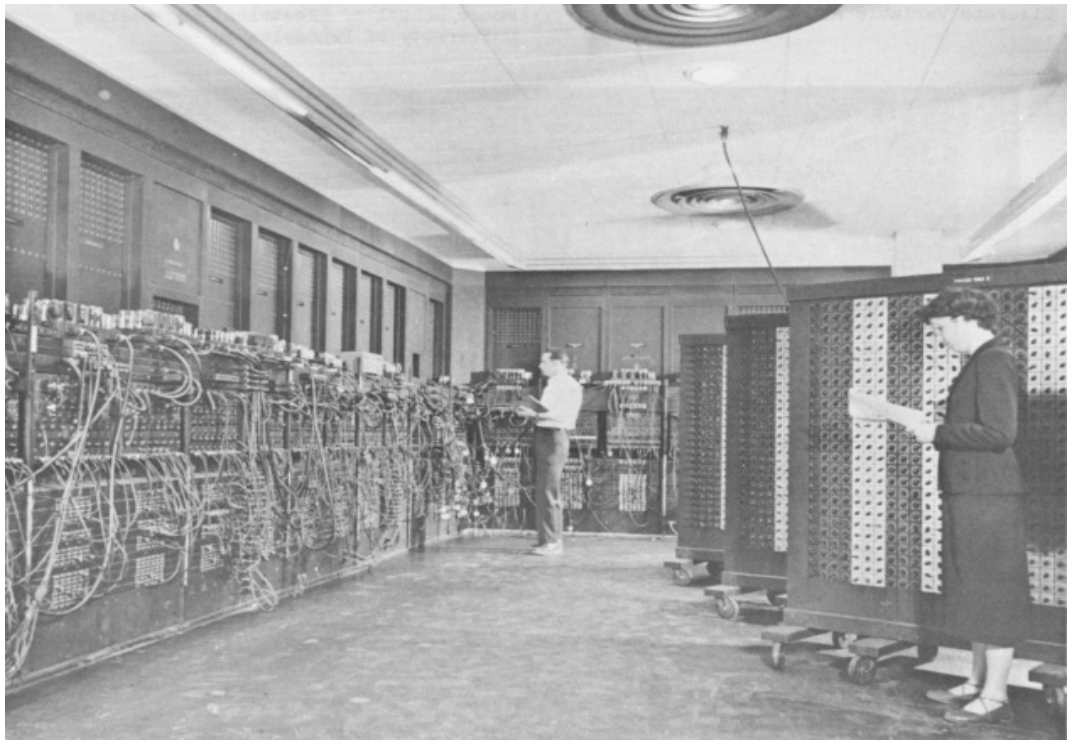


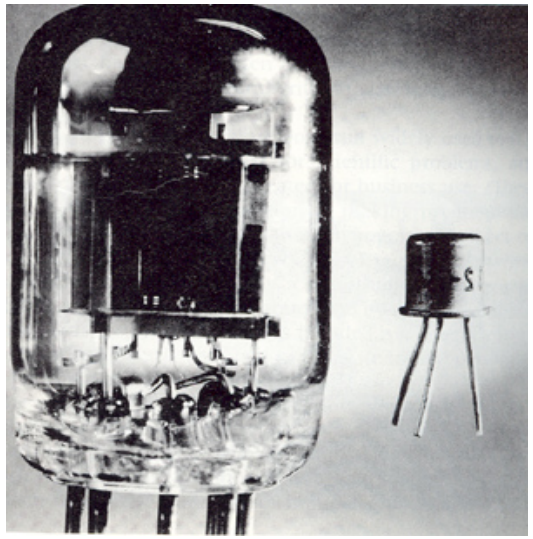


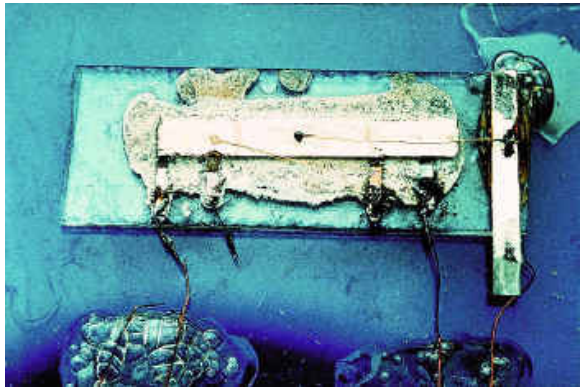
ENIAC (Vacuum tube) → Transistor

What can we learn from history?

- Miniaturization – Vacuum tube to transistors
- Integration – Transistor to Integrated Circuit

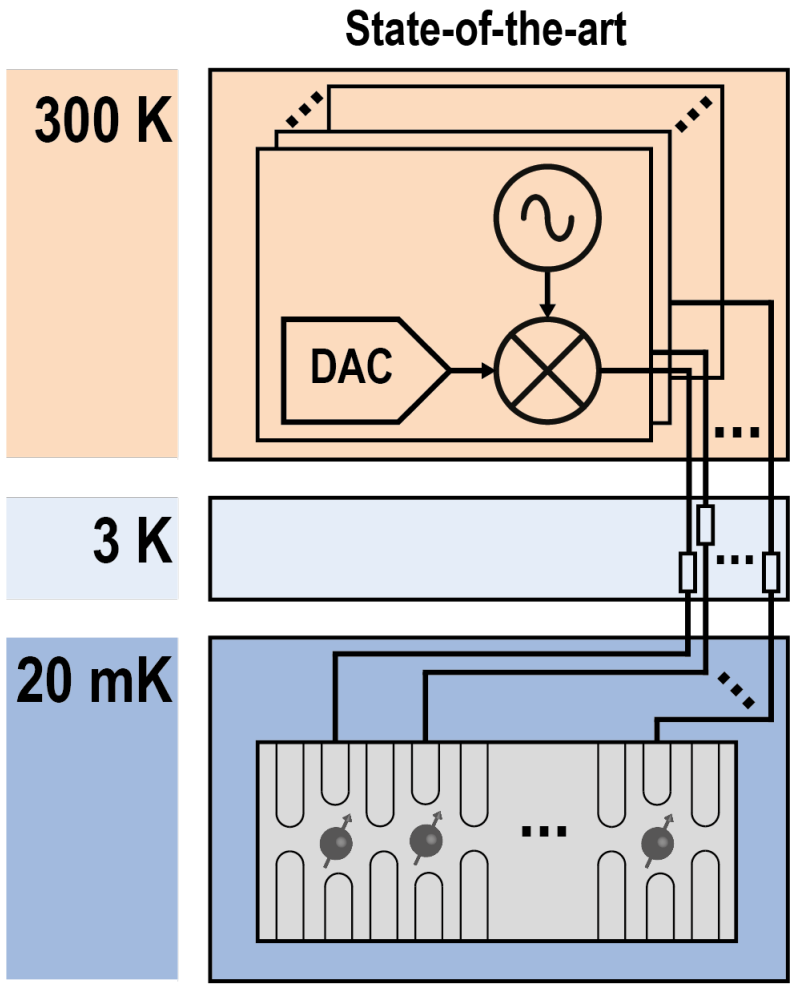




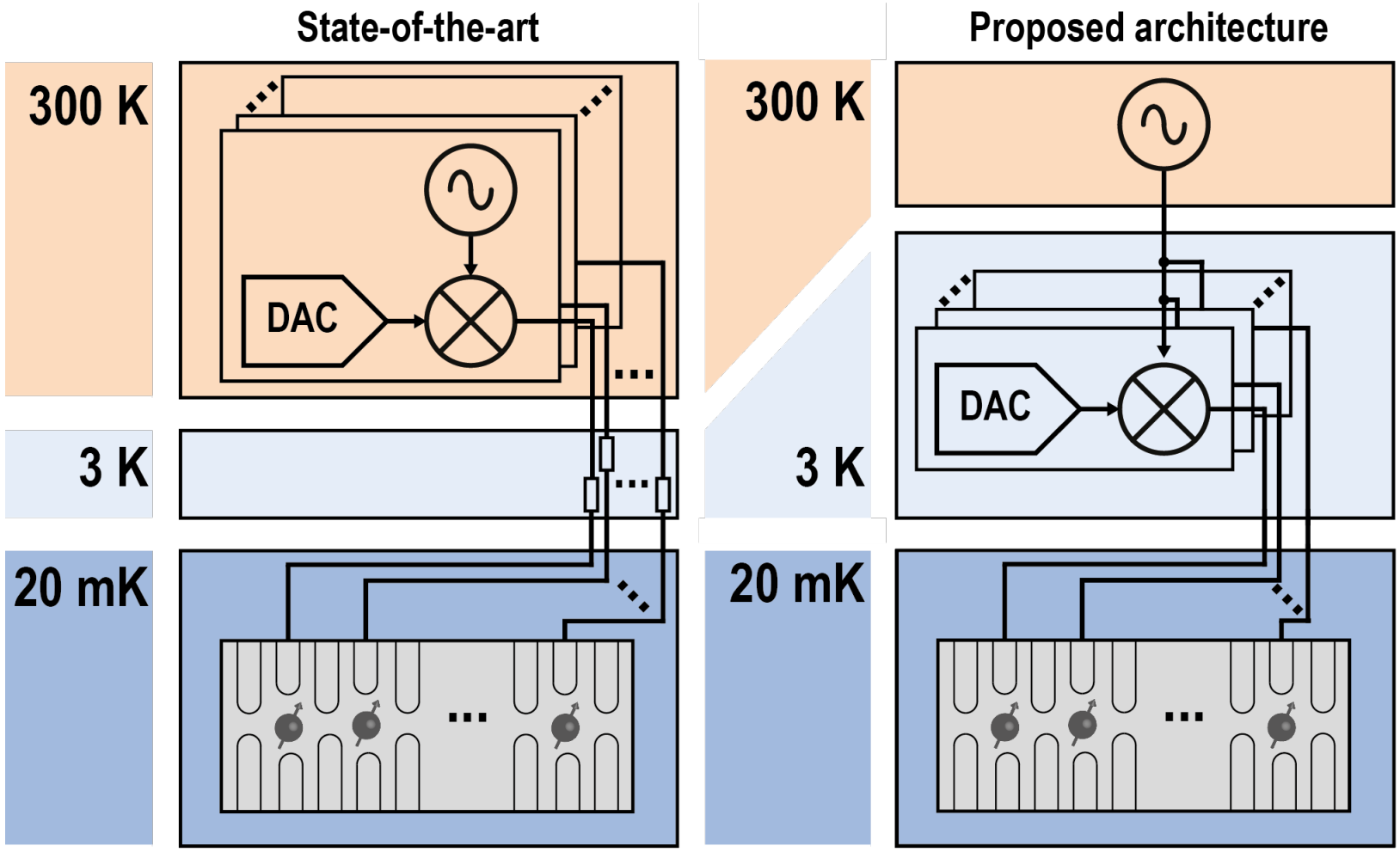


ENIAC (Vacuum tube) → Transistor → First Integrated Circuit

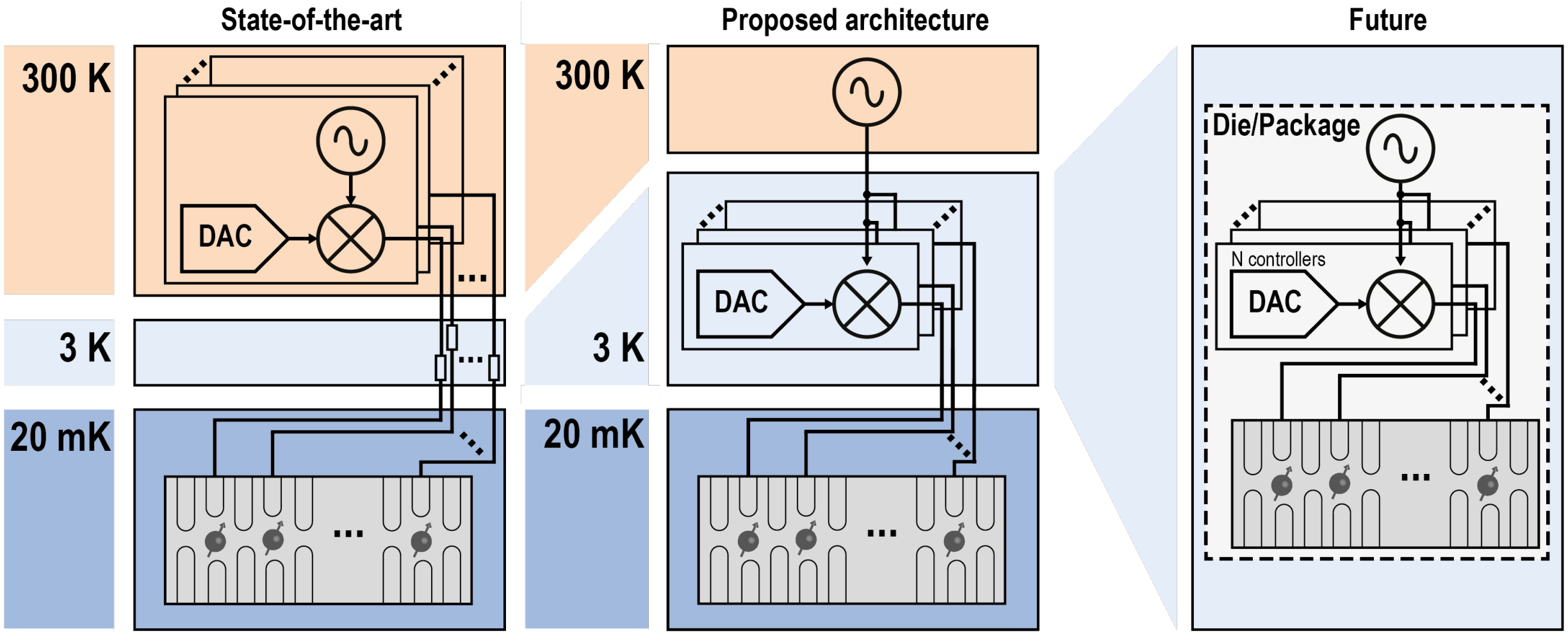
Towards a scalable quantum computer



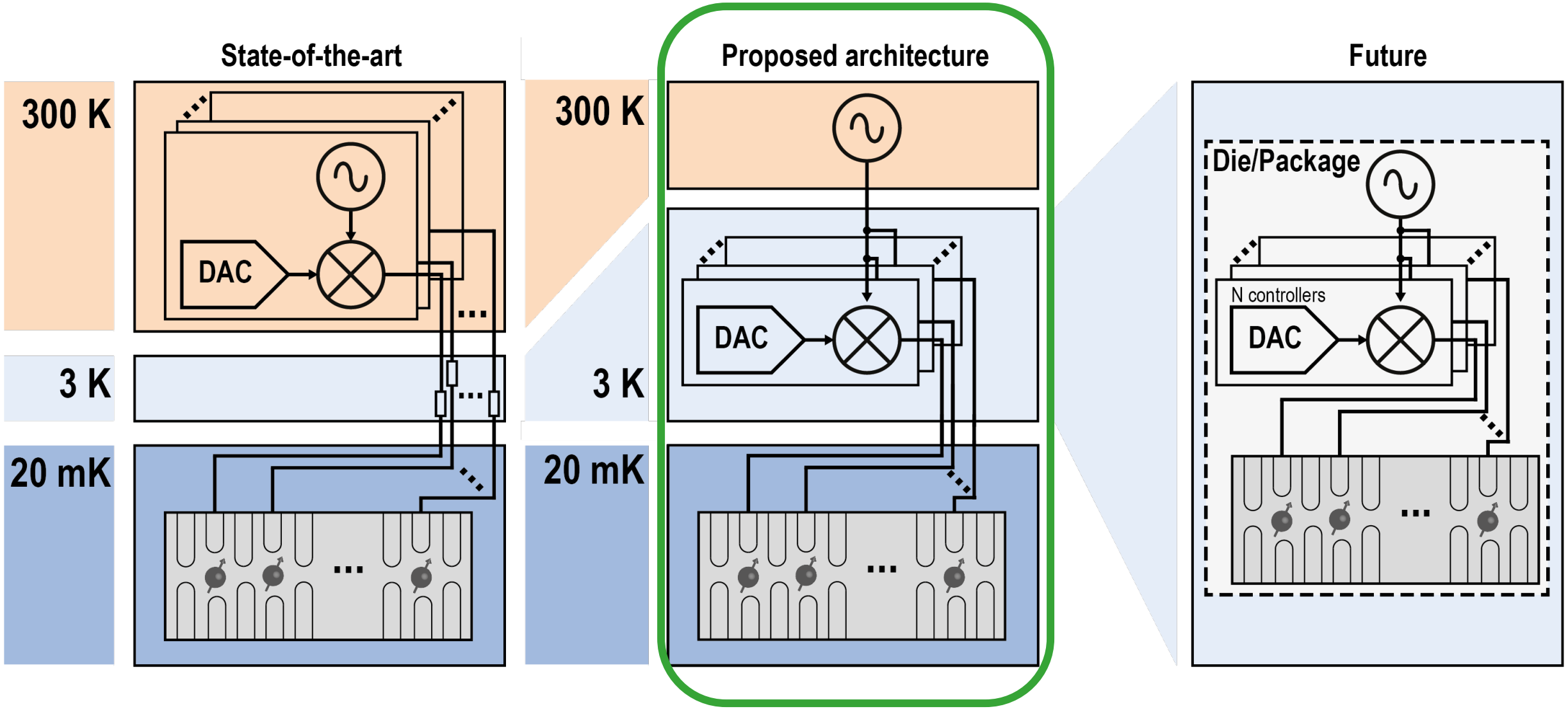
Towards a scalable quantum computer



Towards a scalable quantum computer

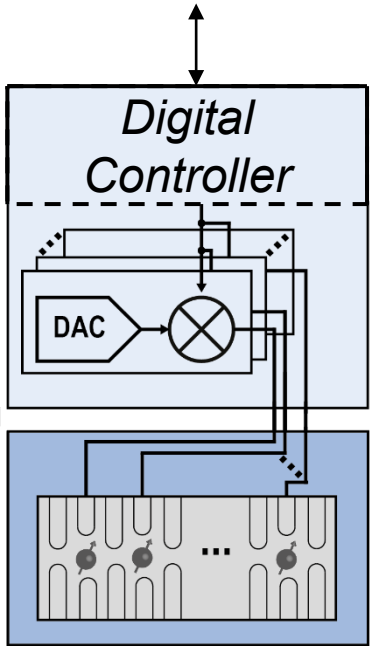


Towards a scalable quantum computer



Challenge (1)

Scalability



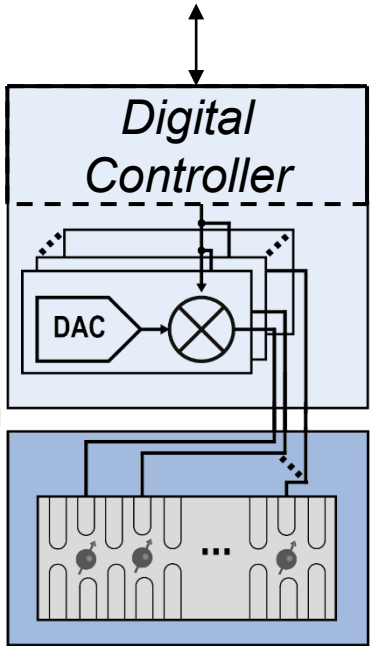
Solution:

- Use solid-state qubits: spin qubits & transmons
- Need an integrated cryogenic digital controller

- Need a scalable cryogenic technology

Challenge (1)

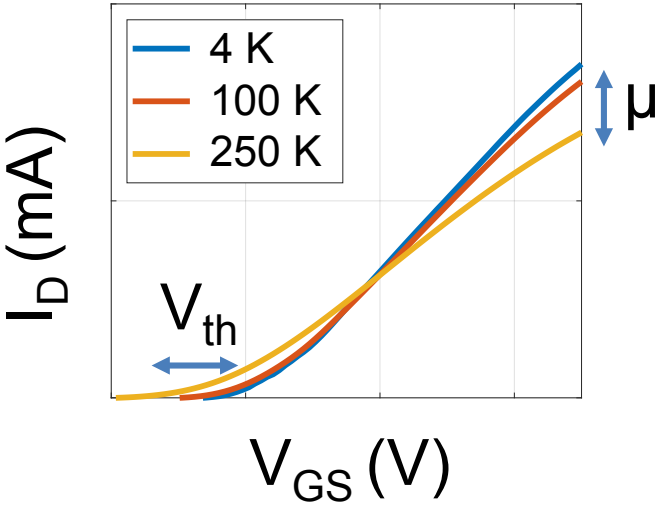
Scalability



Solution:

- Use solid-state qubits: spin qubits & transmons
- Need an integrated cryogenic digital controller

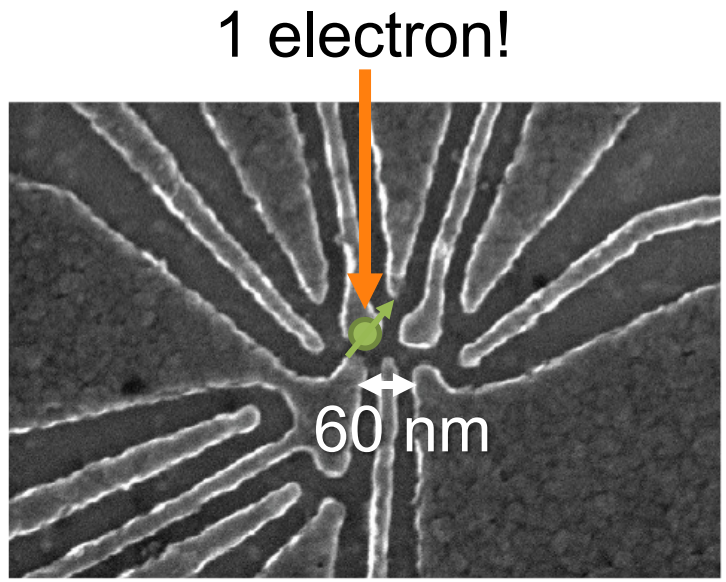
- Need a scalable cryogenic technology: CMOS
  - \+ High level of integration
  - \+ Works down to ~ 30 mK
  - – Not optimized for cryogenic
  - – No mature models



Challenge (2)

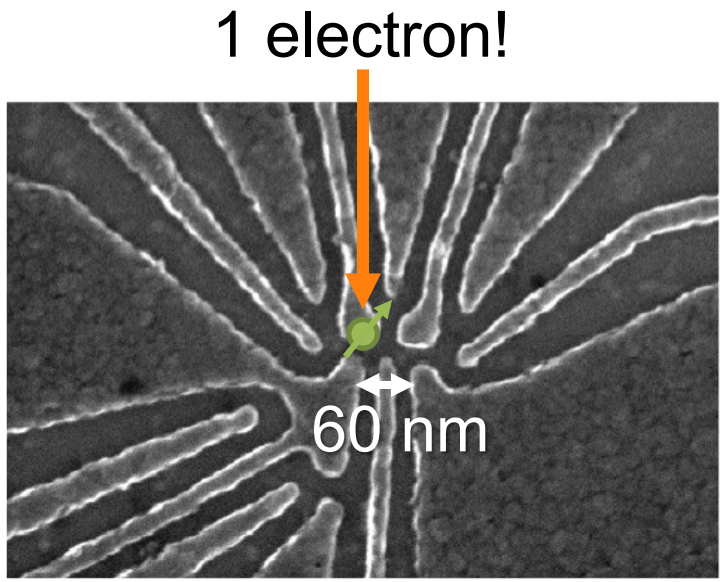
Highly accurate RF signals

- Qubits are fragile:
  - Spin qubit: spin states $|\uparrow\rangle$, $|\downarrow\rangle$ of 1 electron



Challenge (2)

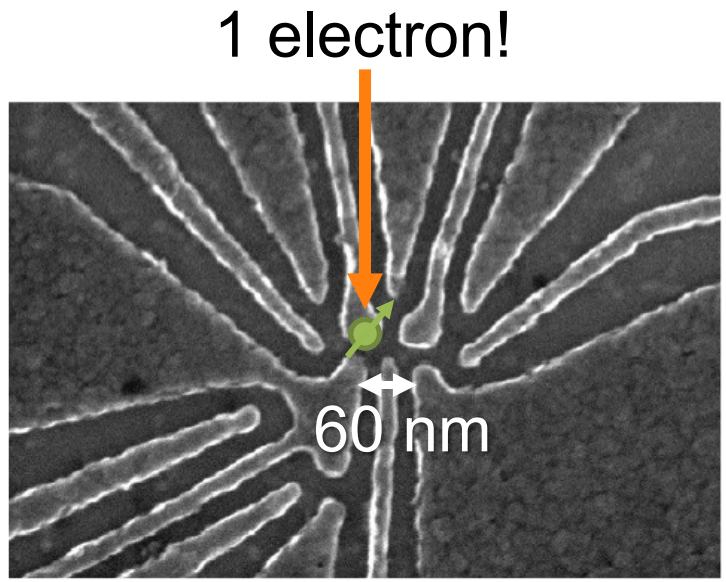
Highly accurate RF signals



- Qubits are fragile:
  - Spin qubit: spin states $|\uparrow\rangle$, $|\downarrow\rangle$ of 1 electron
  - Need high-performance RF instruments for accurate microwave pulses:
    - *Frequency* $f \sim 2\text{-}20$ GHz
    - *Pulse duration* $t < 100$ ns

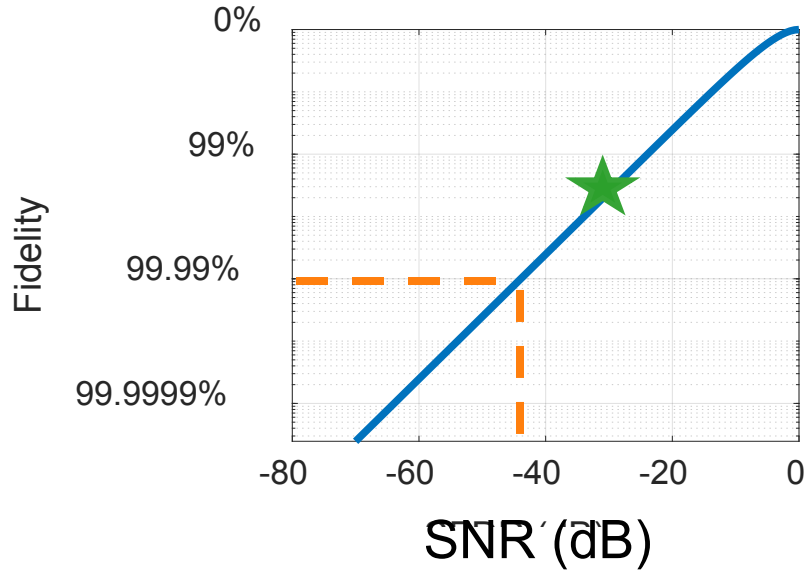
Challenge (2)

Highly accurate RF signals



- Qubits are fragile:
  - Spin qubit: spin states $|\uparrow\rangle$, $|\downarrow\rangle$ of 1 electron
  - Need high-performance RF instruments for accurate microwave pulses:
    - *Frequency* $f \sim 2\text{-}20$ GHz
    - *Pulse duration* $t < 100$ ns

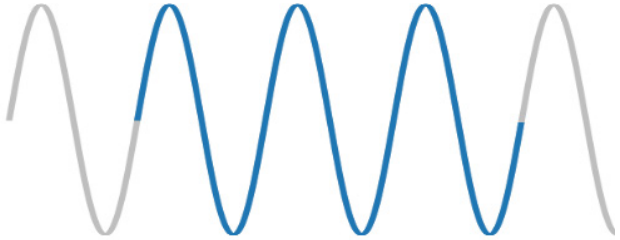
- Operation accuracy: *fidelity*
  - *State-of-the-art spin qubits:* < 99.9%
  - *Target:* > 99.99%
    - *SNR > 44 dB in 25 MHz [van Dijk, 2019]*

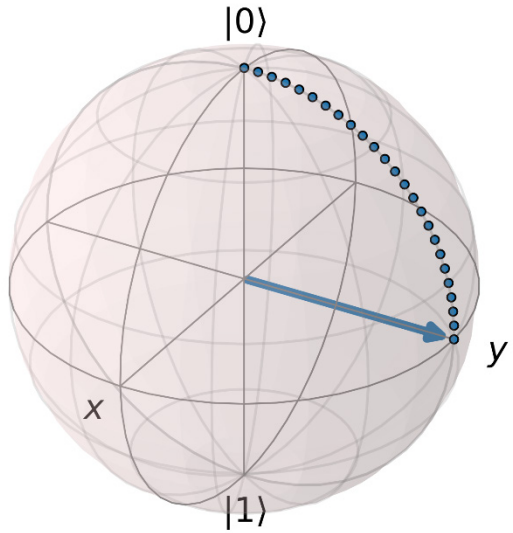


Challenge (3)

Accurate phase tracking

- Effect of the microwave pulse phase on the qubit:

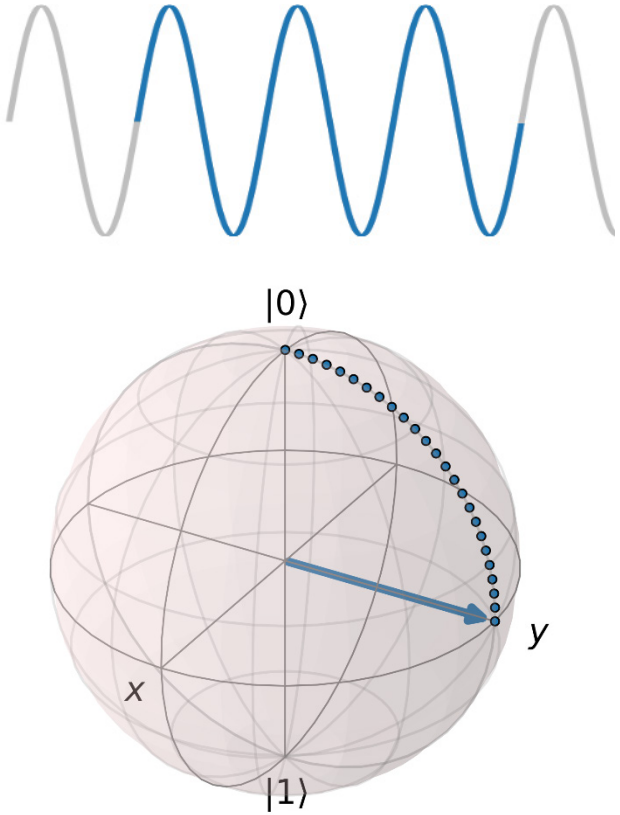


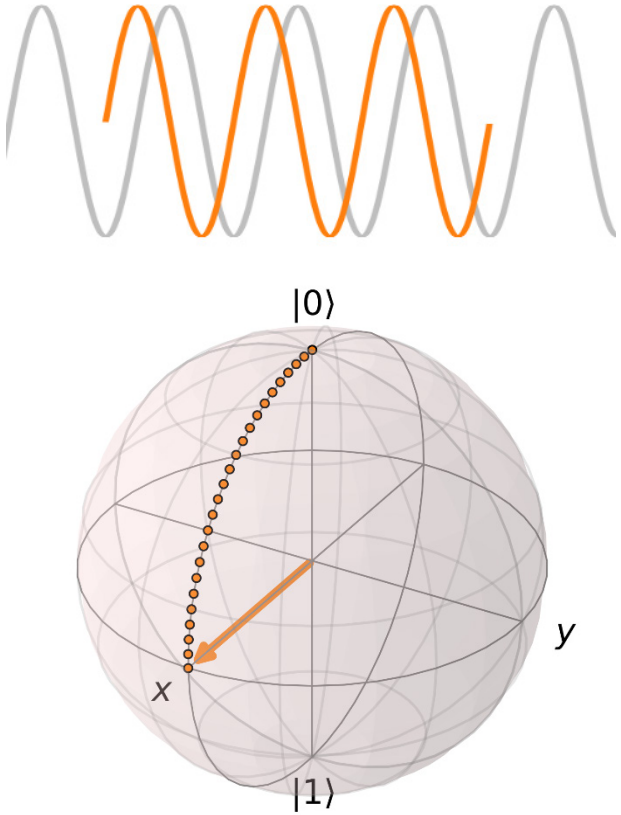


Challenge (3)

Accurate phase tracking

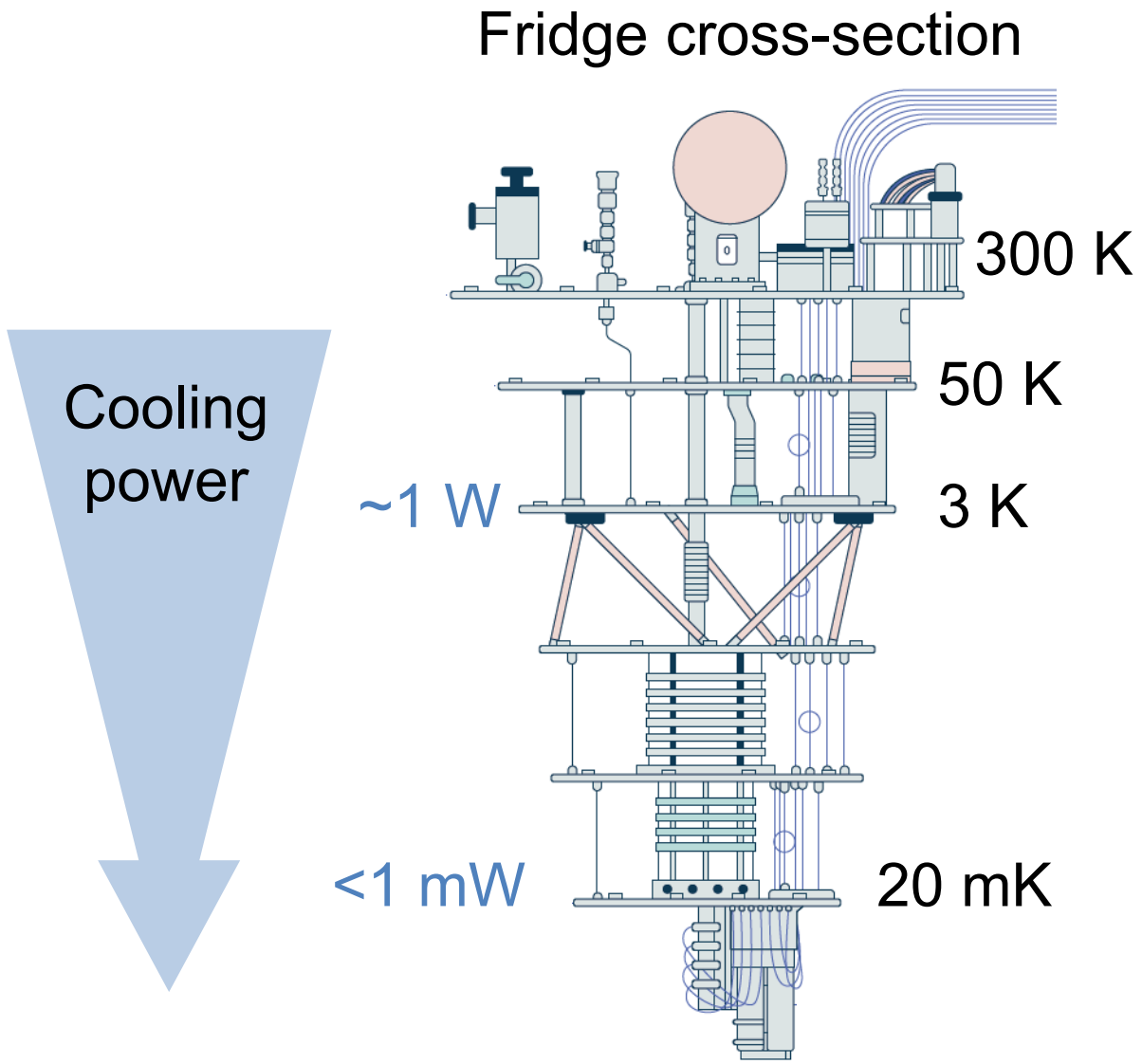
- Effect of the microwave pulse phase on the qubit:





Challenge (4)

Low-power budget

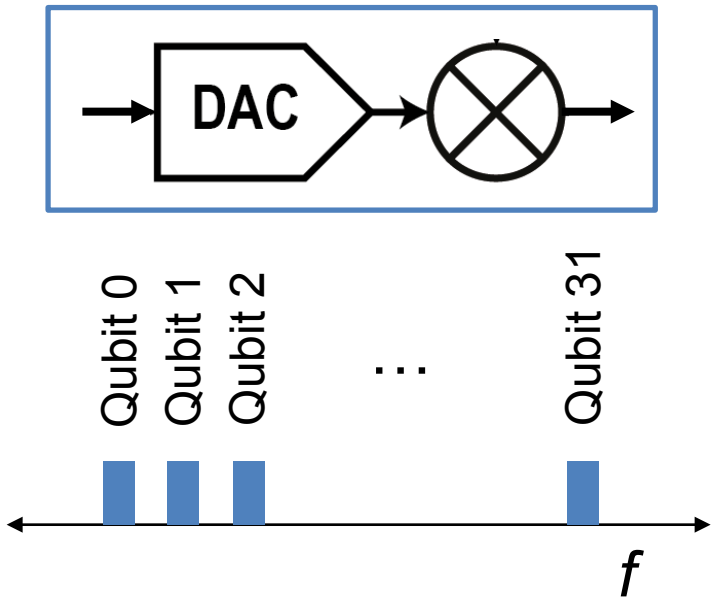


Challenge (4)

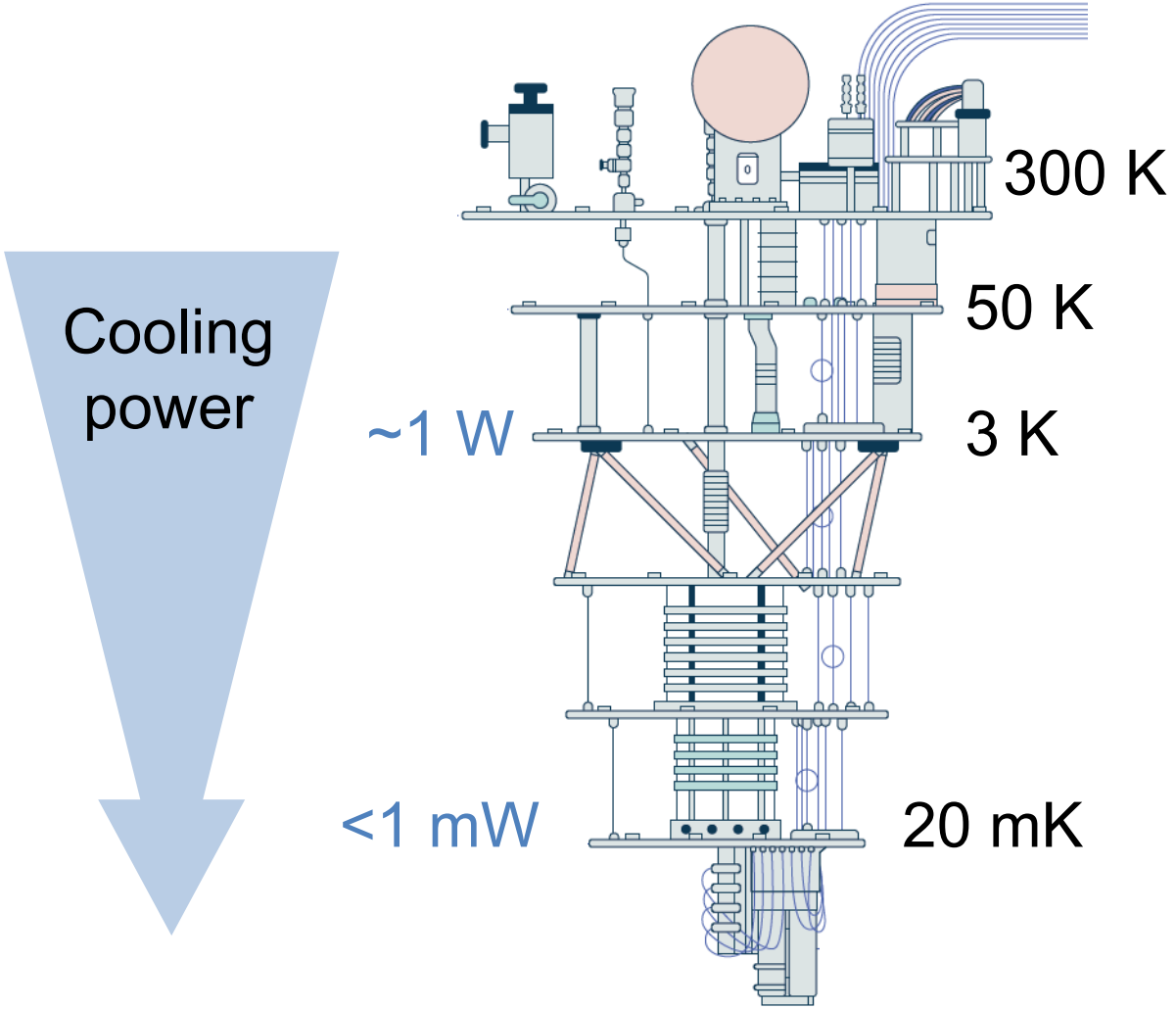
Low-power budget

Solution:

- Frequency multiplexing:
  - 1 controller for *N* qubits



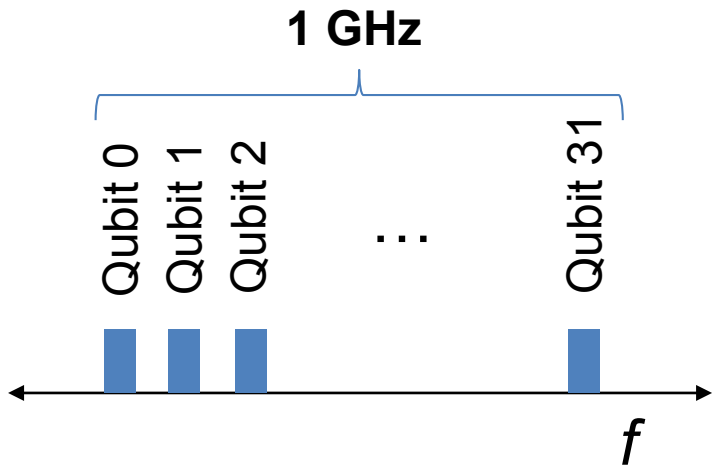
Fridge cross-section



Challenge (5)

Highly linear wideband multi-channel controller

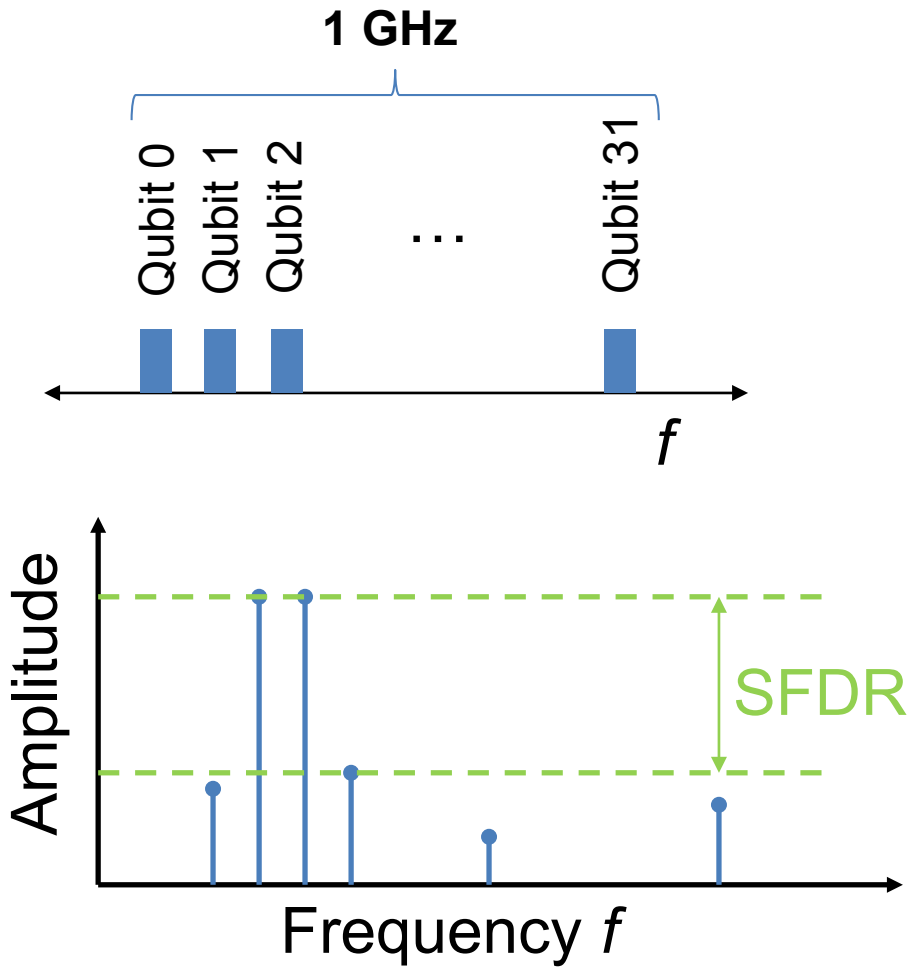
- Support 32 qubits:
  - Wide bandwidth (1 GHz)



Challenge (5)

Highly linear wideband multi-channel controller

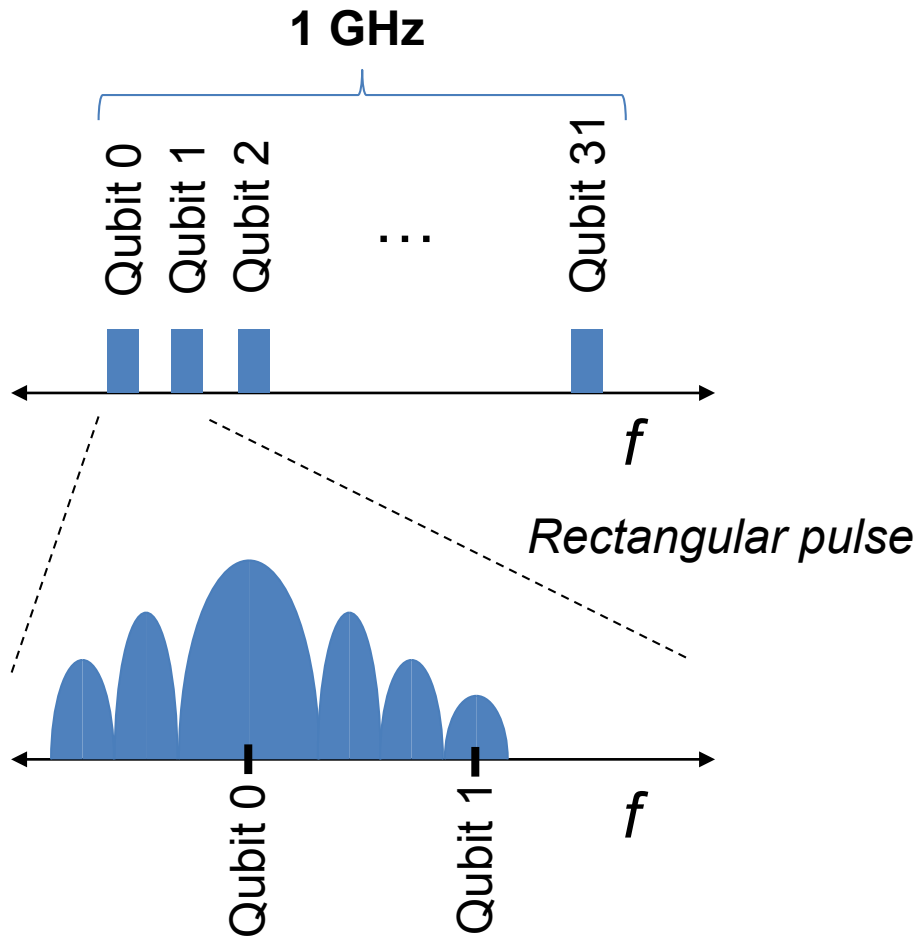
- Support 32 qubits:
  - Wide bandwidth (1 GHz)
  - High SFDR (44 dB)



Challenge (5)

Highly linear wideband multi-channel controller

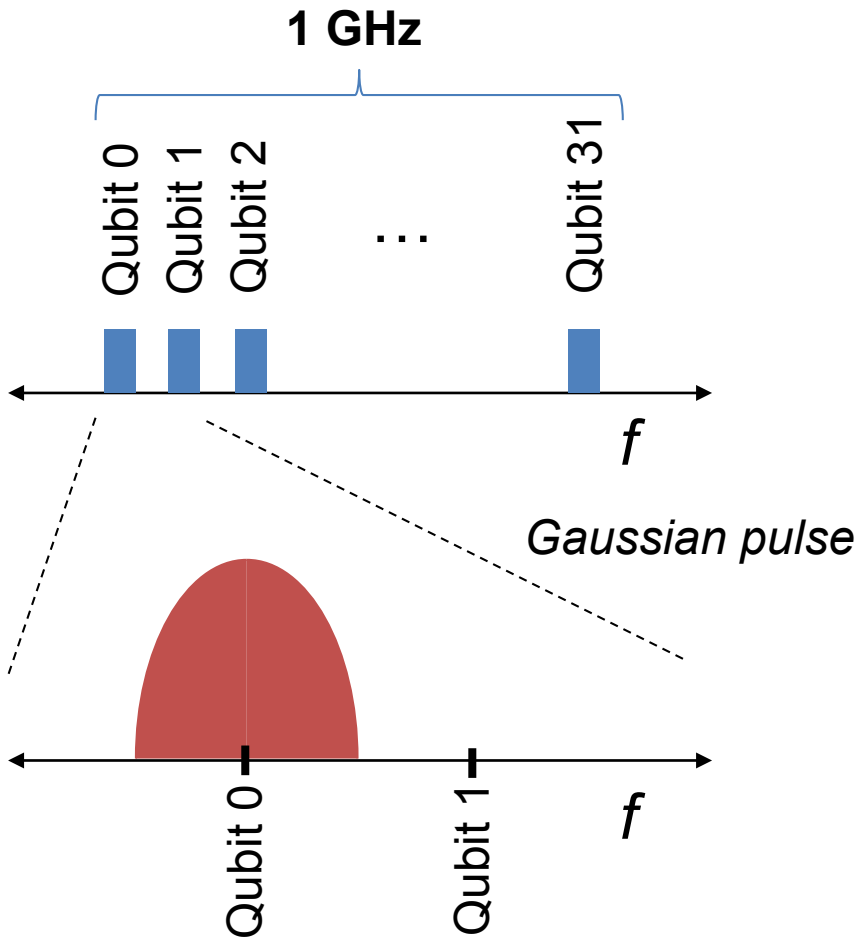
- Support 32 qubits:
  - Wide bandwidth (1 GHz)
  - High SFDR (44 dB)
  - Pulse shaping



Challenge (5)

Highly linear wideband multi-channel controller

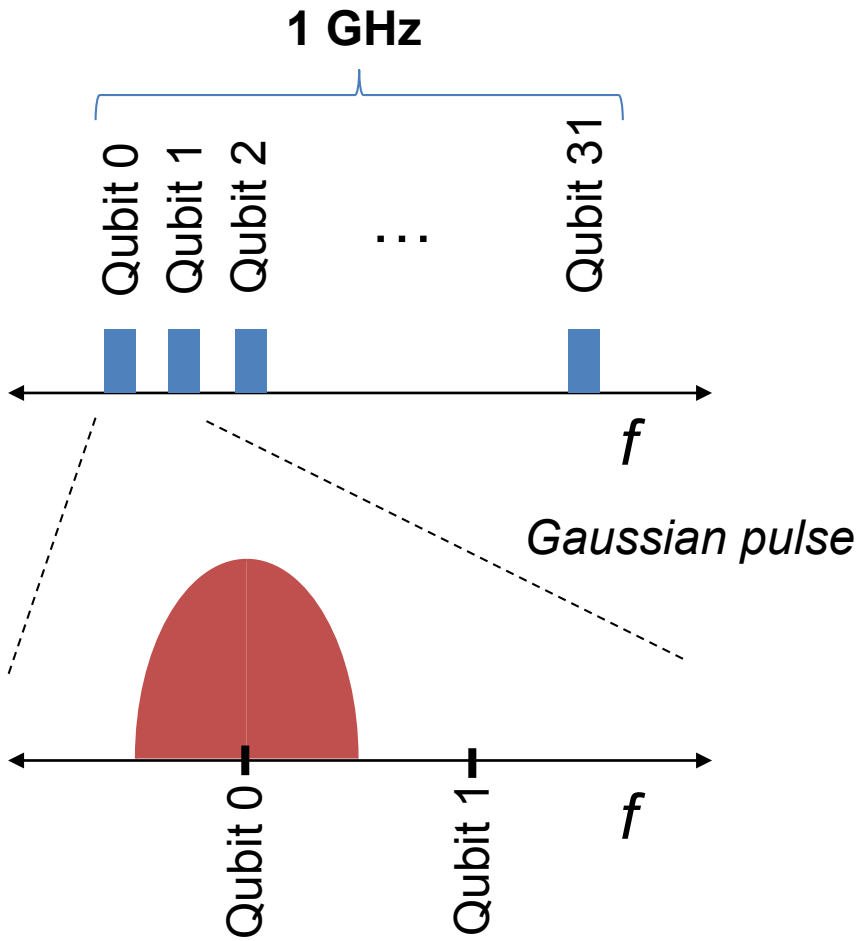
- Support 32 qubits:
  - Wide bandwidth (1 GHz)
  - High SFDR (44 dB)
  - Pulse shaping



Challenge (5)

Highly linear wideband multi-channel controller

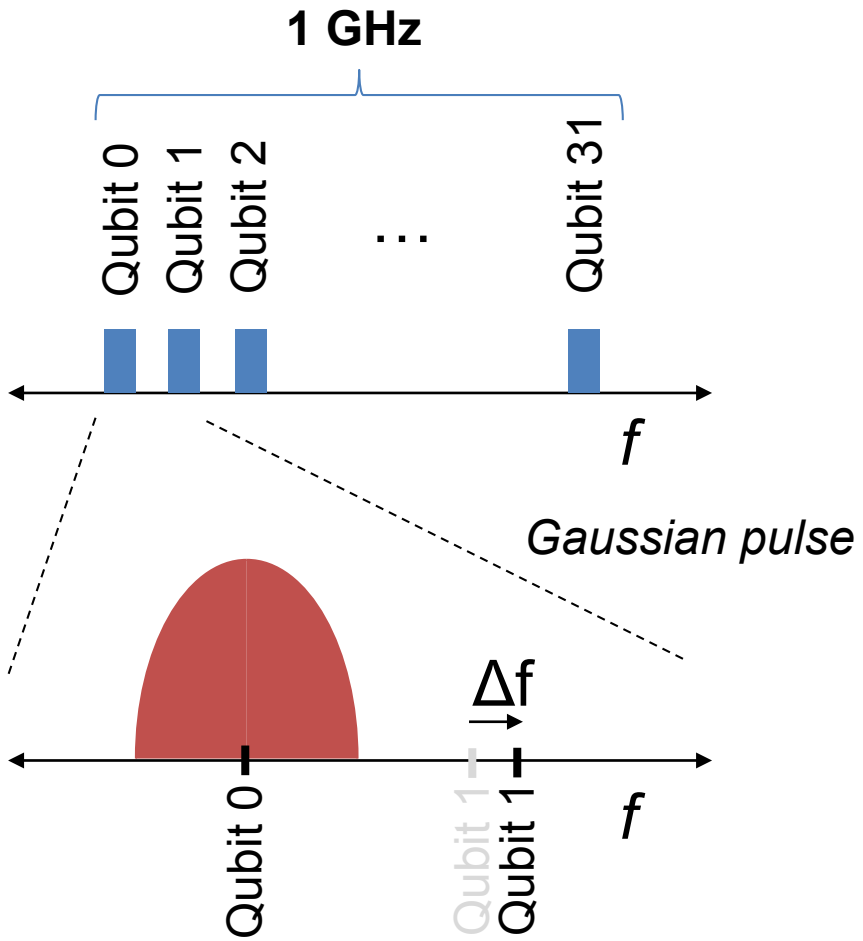
- Support 32 qubits:
  - Wide bandwidth (1 GHz)
  - High SFDR (44 dB)
  - Pulse shaping
  - Tracking phase of 32 qubits



Challenge (5)

Highly linear wideband multi-channel controller

- Support 32 qubits:
  - Wide bandwidth (1 GHz)
  - High SFDR (44 dB)
  - Pulse shaping
  - Tracking phase of 32 qubits
  - Phase-correction required
    - *Compensate frequency shift Δf*



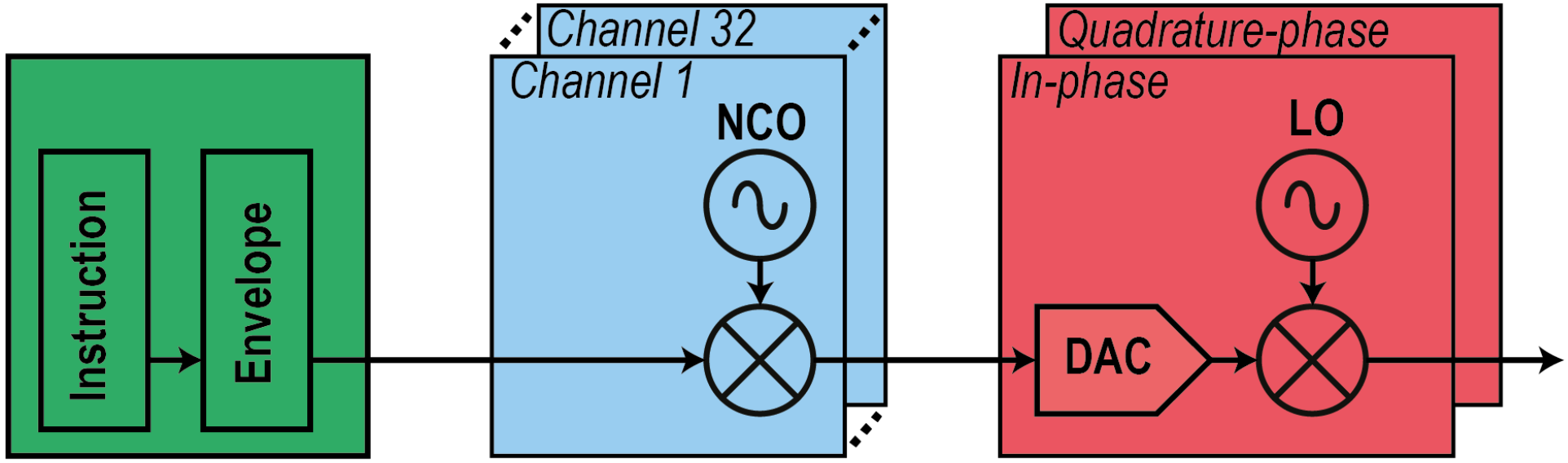
Proposed controller: Horse Ridge

- **Scalability:**
  - Support spin qubits and transmons
  - Integrated digital controller
  - CMOS operating at 3 K

"Horse Ridge", Oregon

- **High performance RF signals:**
  - Fidelity: 99.99% (SNR: 44 dB, SFDR: 44 dB)
  - Output frequency: 2 - 20 GHz (0.025 ppm resolution)
  - Pulse duration: up to 40 us (1 ns resolution)
  - Pulse shape: Fully programmable
- **Power-efficiency:**
  - Multi-qubit control using *frequency multiplexing*

System Architecture

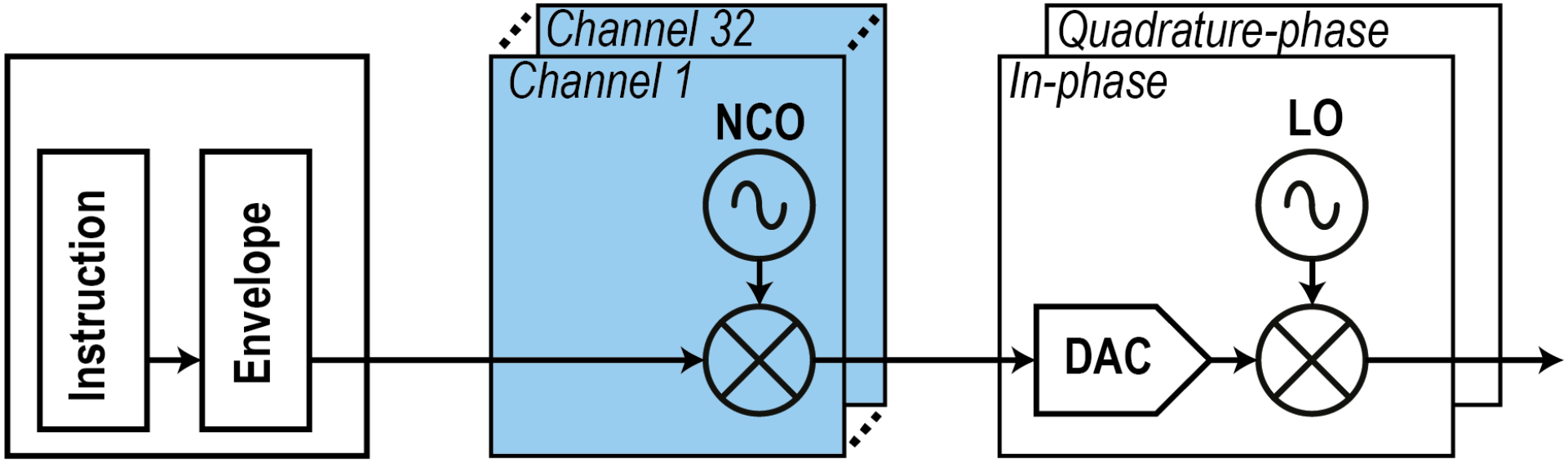


Digital Controller

Digital Signal Generation

Single-Sideband Transmitter

System Architecture



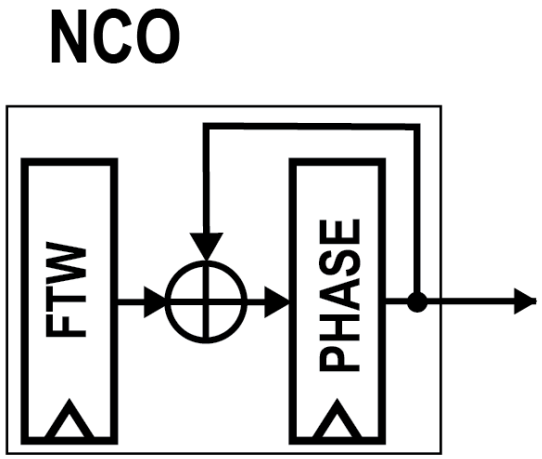
Digital Controller

Digital Signal Generation

Single-Sideband Transmitter

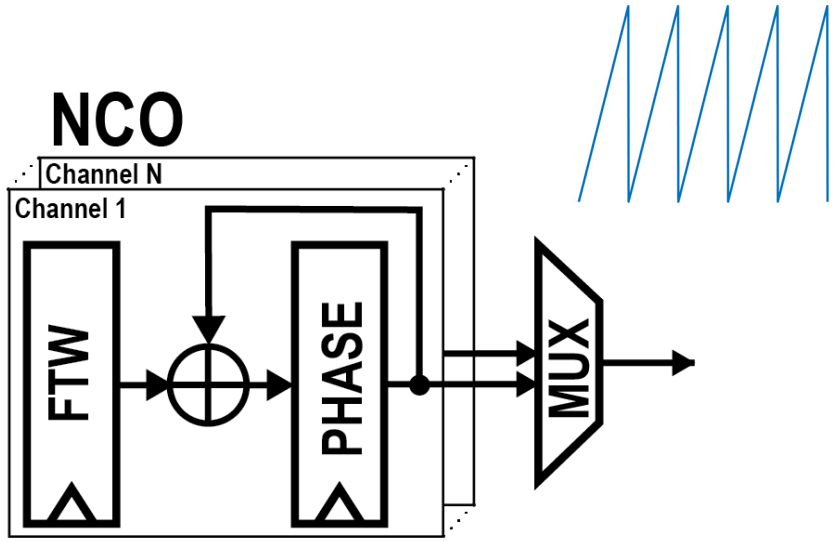
Digital Signal Generation

- Phase tracking
- Frequency accuracy: ~ 0.025 ppm



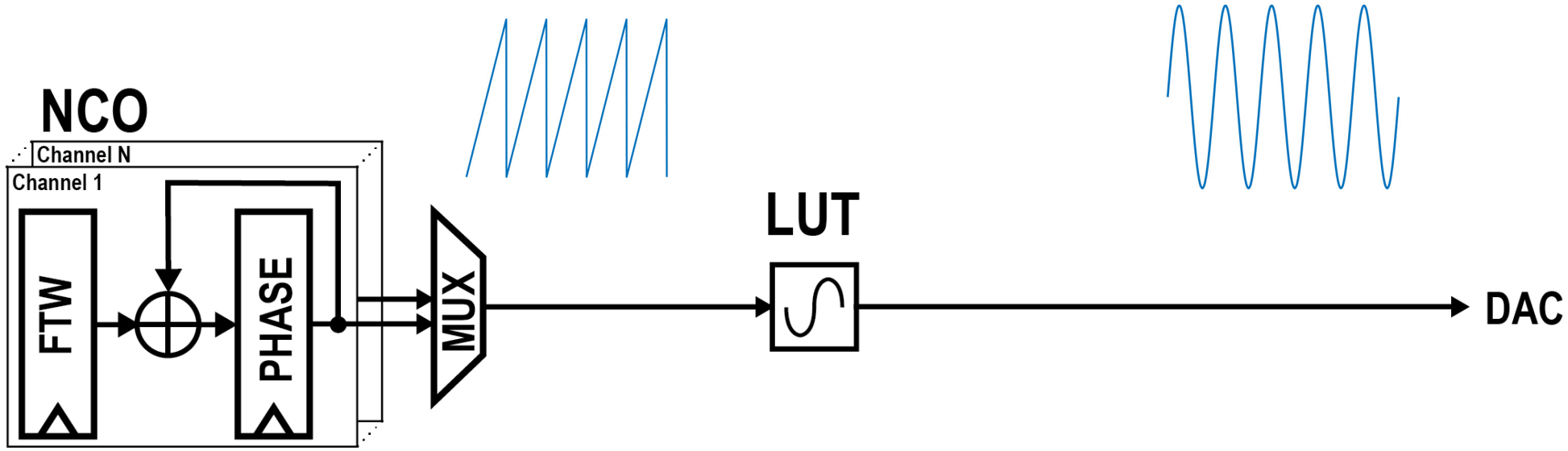
Digital Signal Generation

- Phase tracking
- Frequency accuracy: ~ 0.025 ppm



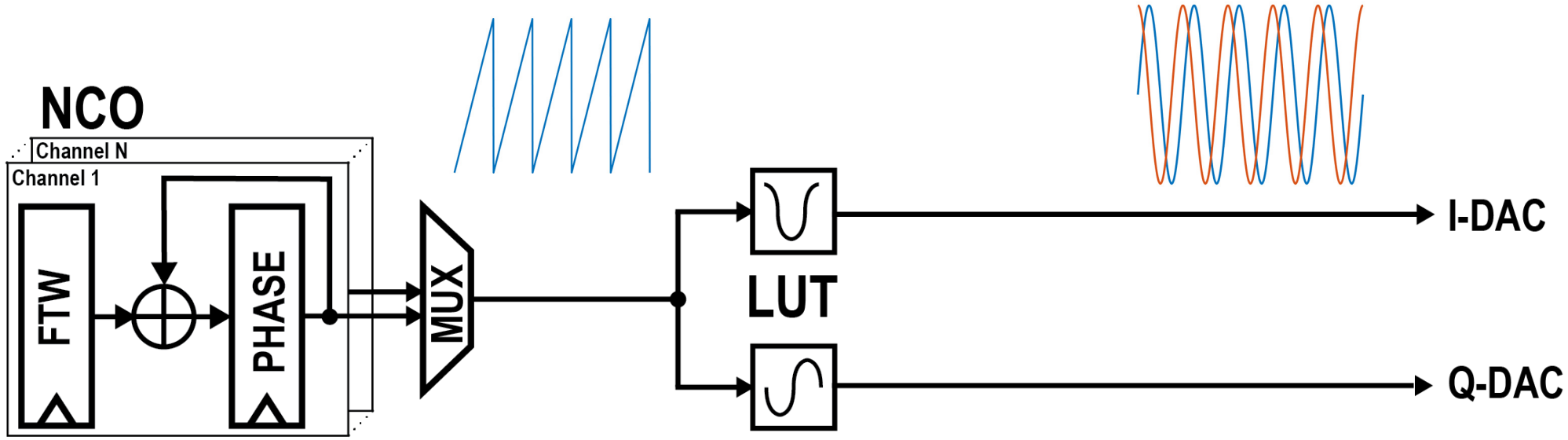
1 NCO/qubit

Digital Signal Generation



1 NCO/qubit

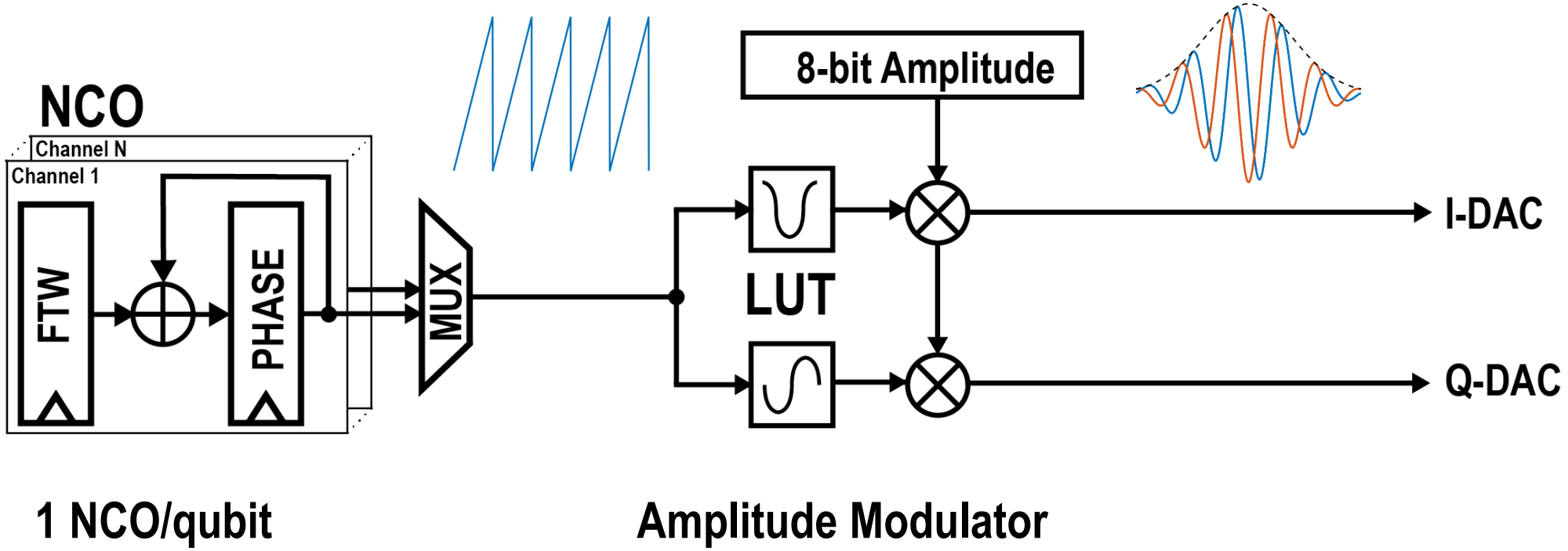
Digital Signal Generation



1 NCO/qubit

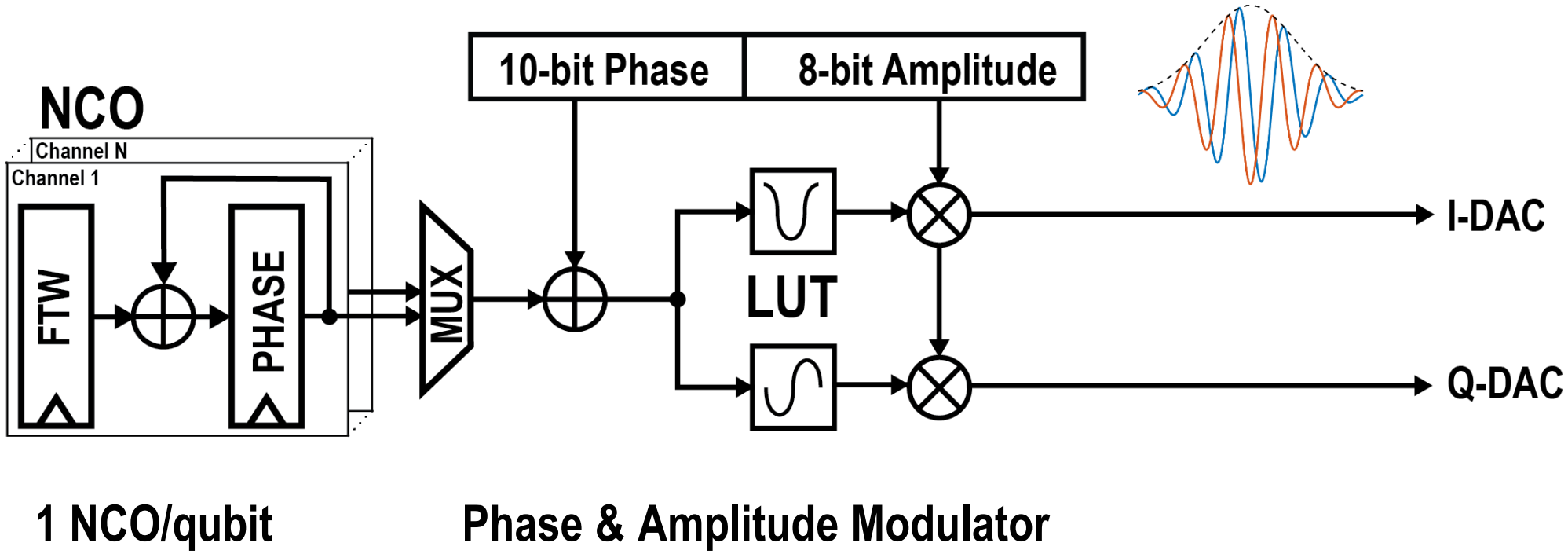
Digital Signal Generation

- Pulse shaping



Digital Signal Generation

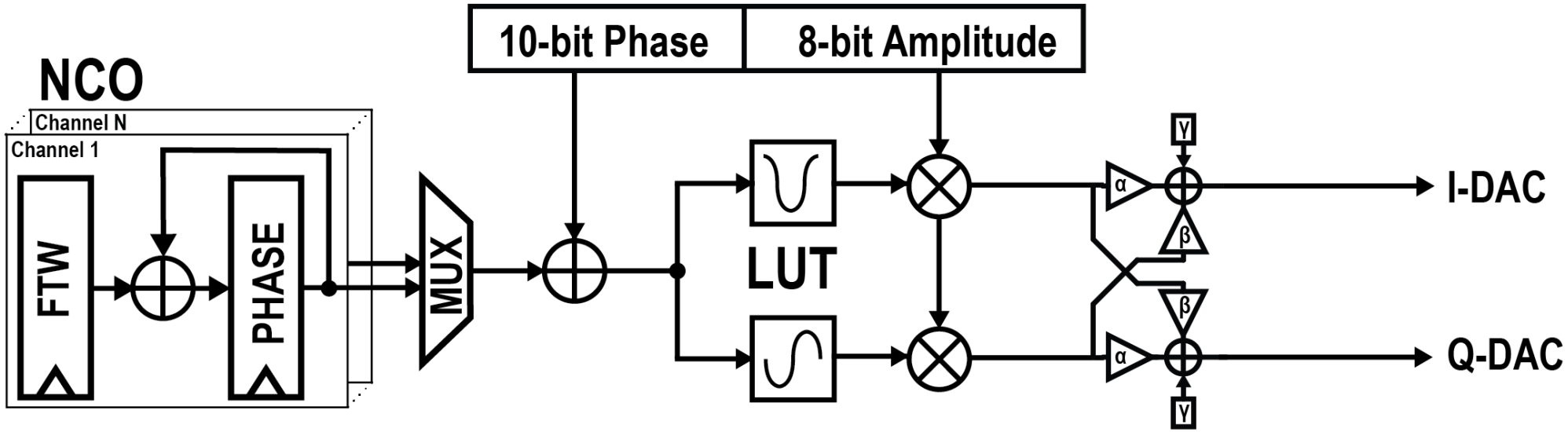
- Pulse shaping
- Bit widths tuned for > 99.99% fidelity



Digital Signal Generation

- Phase imbalance < 0.7 degree
- Gain imbalance < 0.1 dB

} SFDR > 44 dB

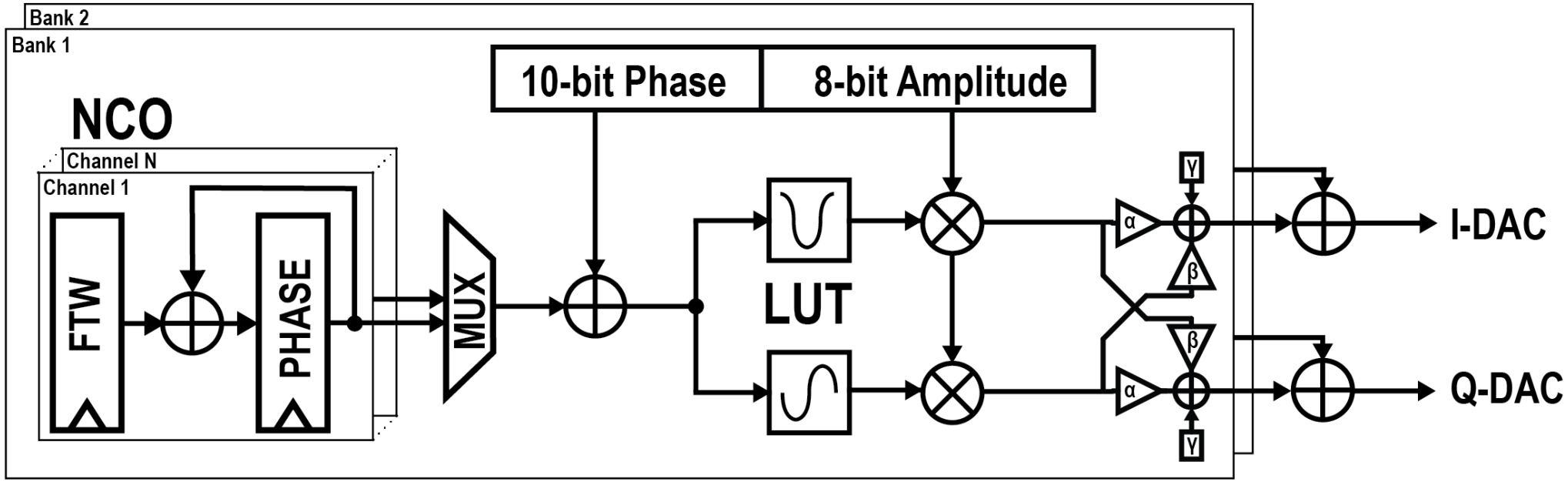


1 NCO/qubit

Phase & Amplitude Modulator

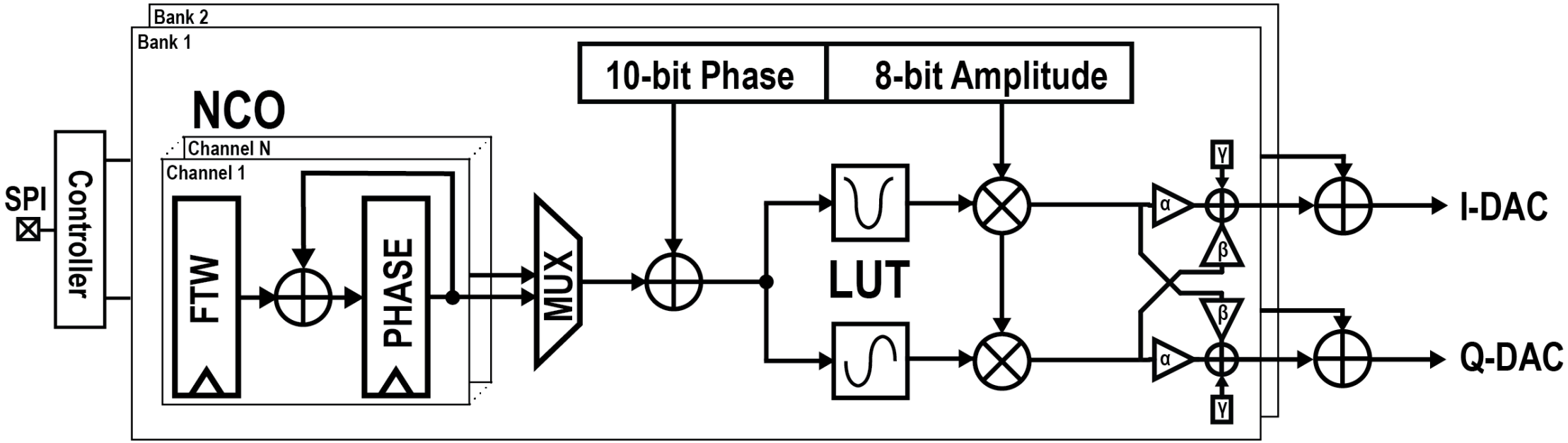
I/Q and LO leakage calibration

Digital Signal Generation



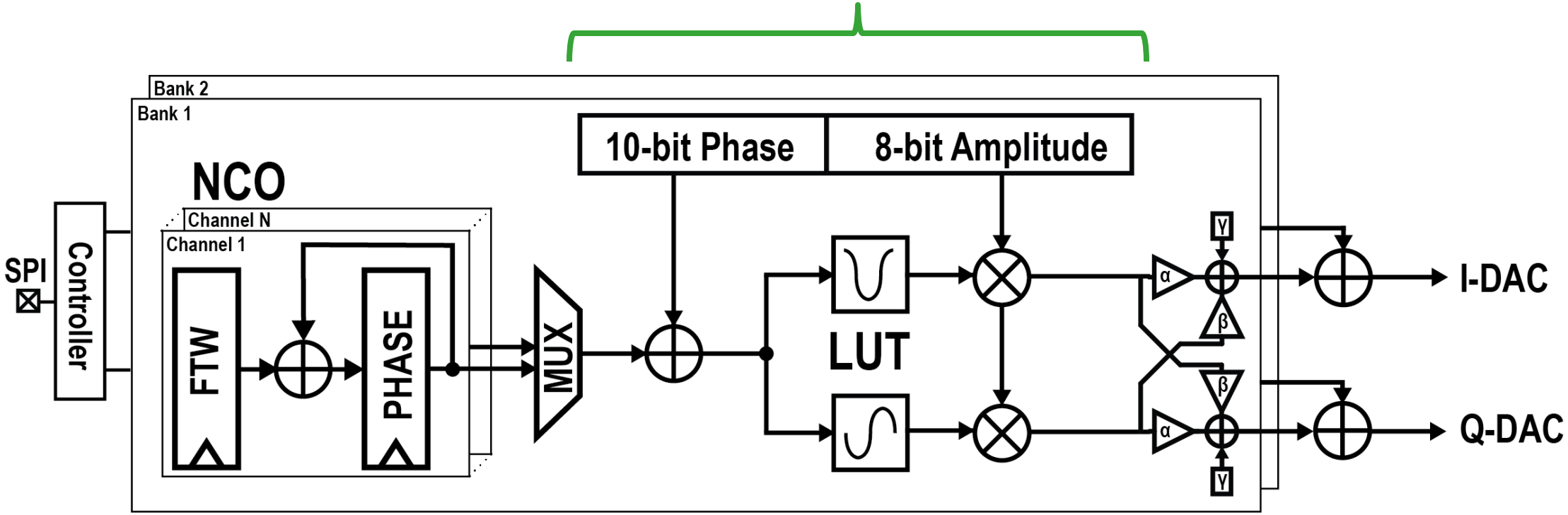
2 Banks for simultaneous excitation

Digital Signal Generation

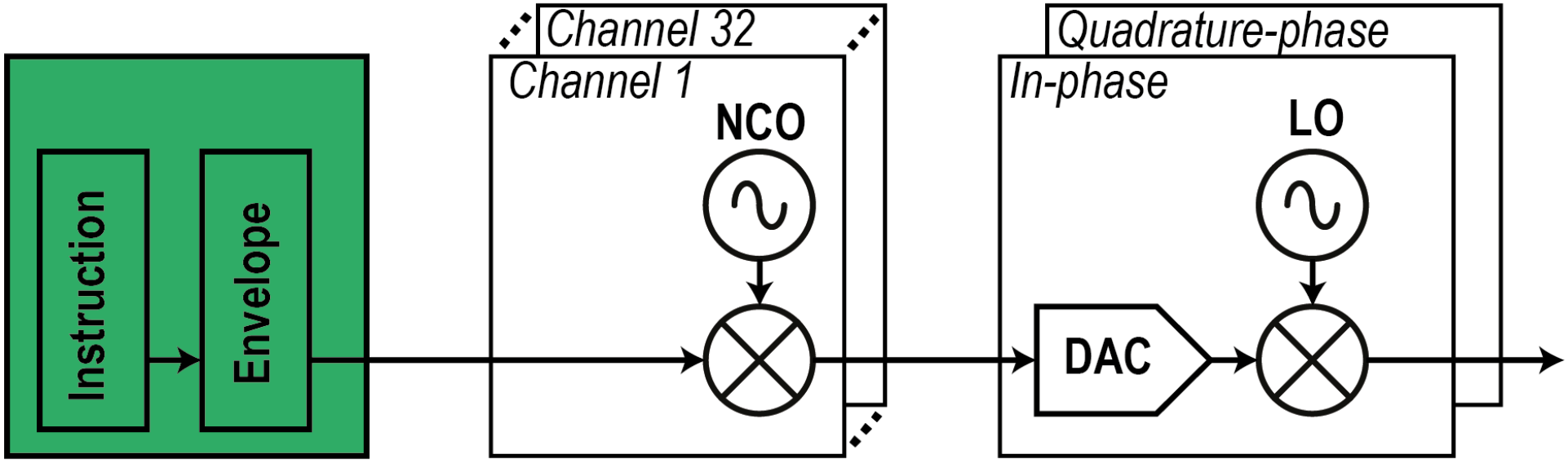


Digital Signal Generation

Modulator input: 18-bit @ 1 GHz → **18 Gb/s**



System Architecture



Digital Controller

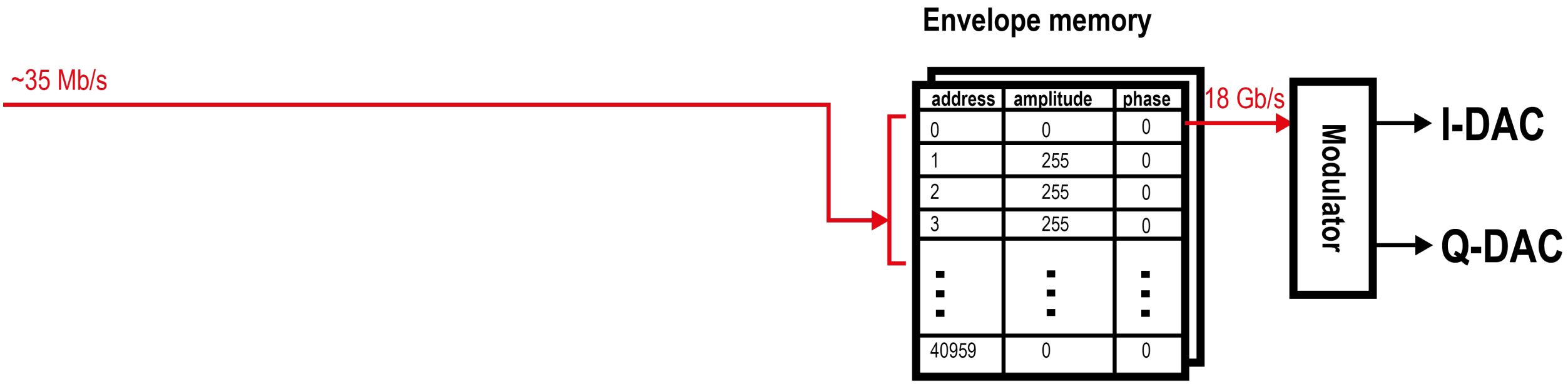
Digital Signal Generation

Single-Sideband Transmitter

Digital Controller

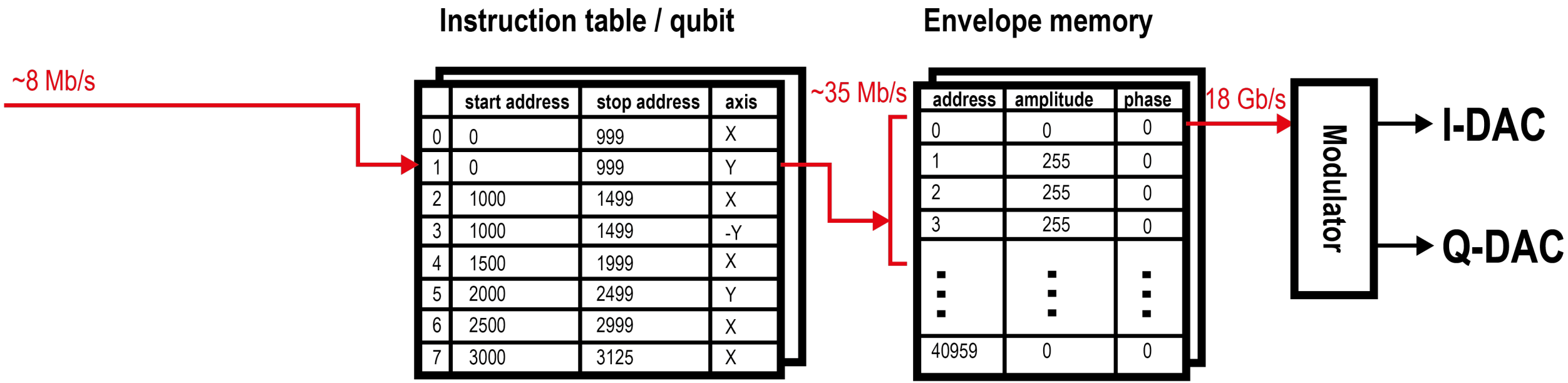
Problem: large on-chip data rate

Digital Controller



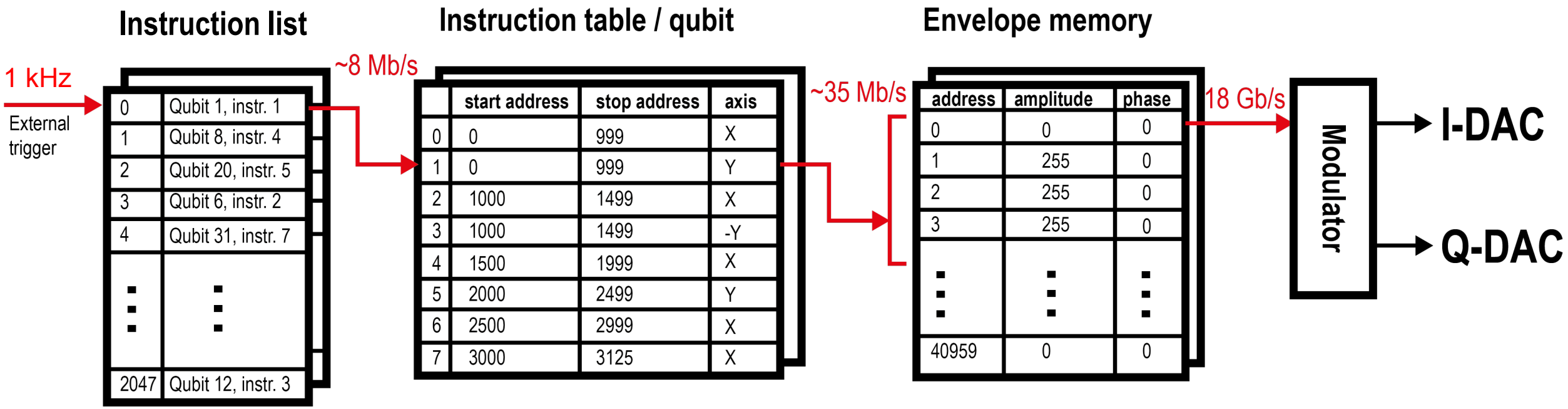
1) SRAM, 40960 points:
   - Amplitude
   - Phase

Digital Controller



2) Instruction table, 8 instructions/qubit:

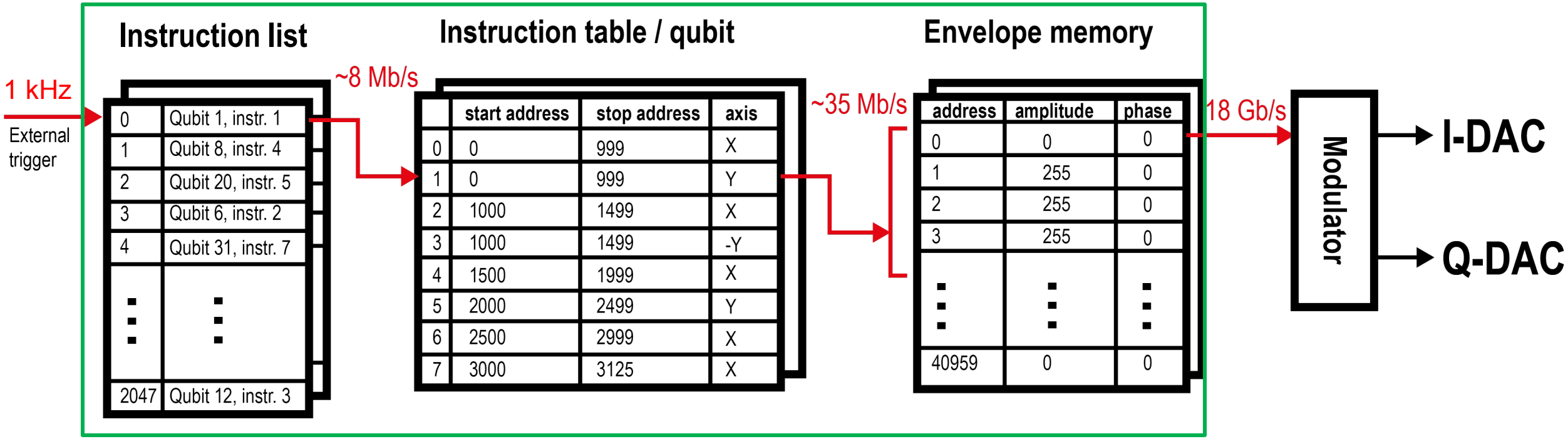
Digital Controller



3) Instruction list, 2048 entries:

- Qubit & Instruction

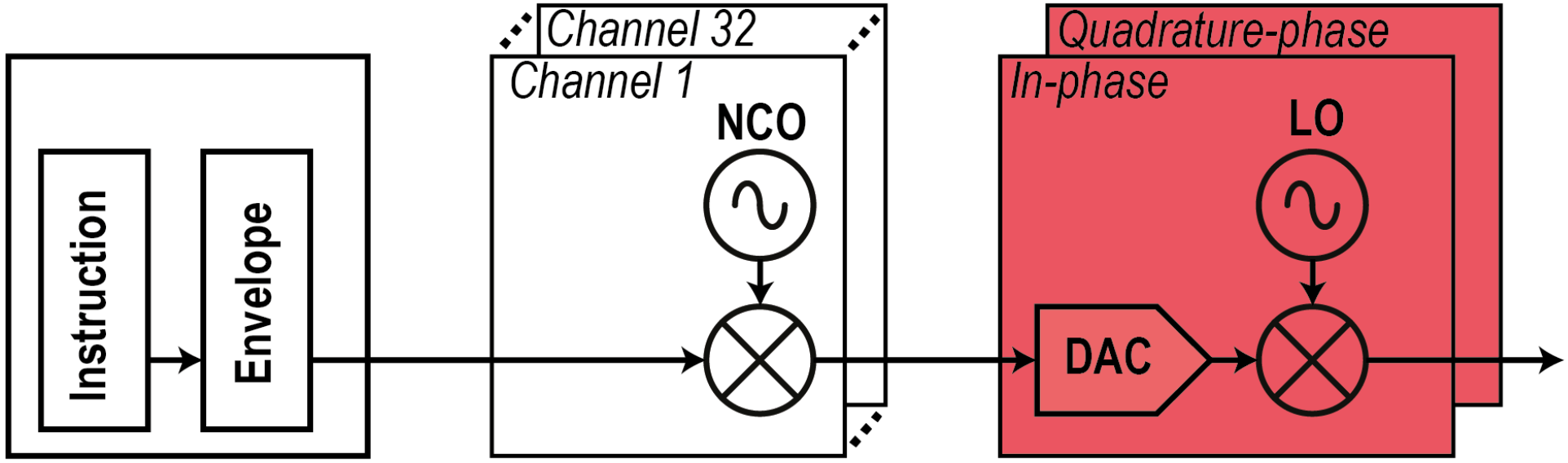
Digital Controller



On-chip memory

- No high-speed connection required during quantum algorithm execution

System Architecture

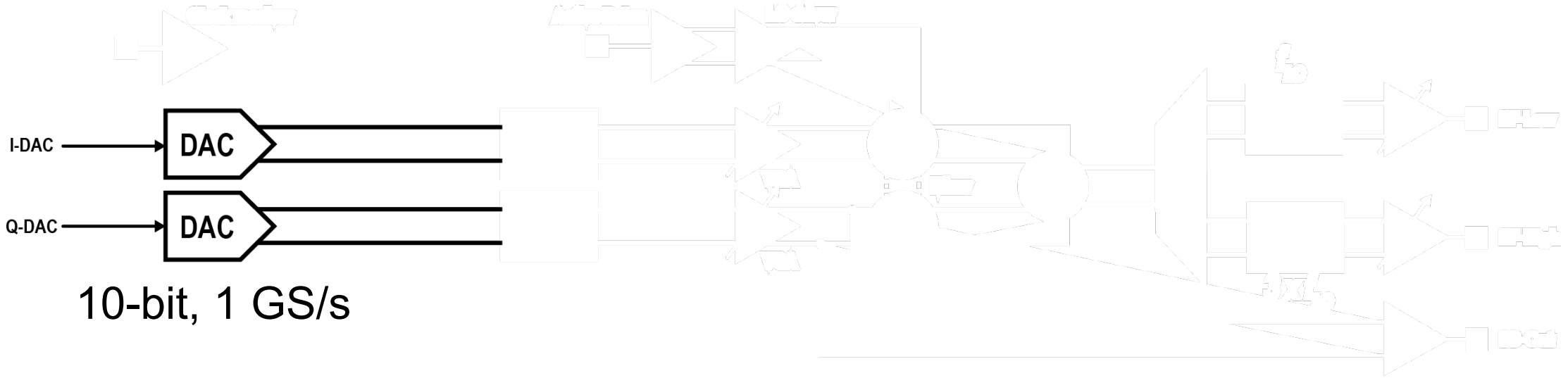


Digital Controller

Digital Signal Generation

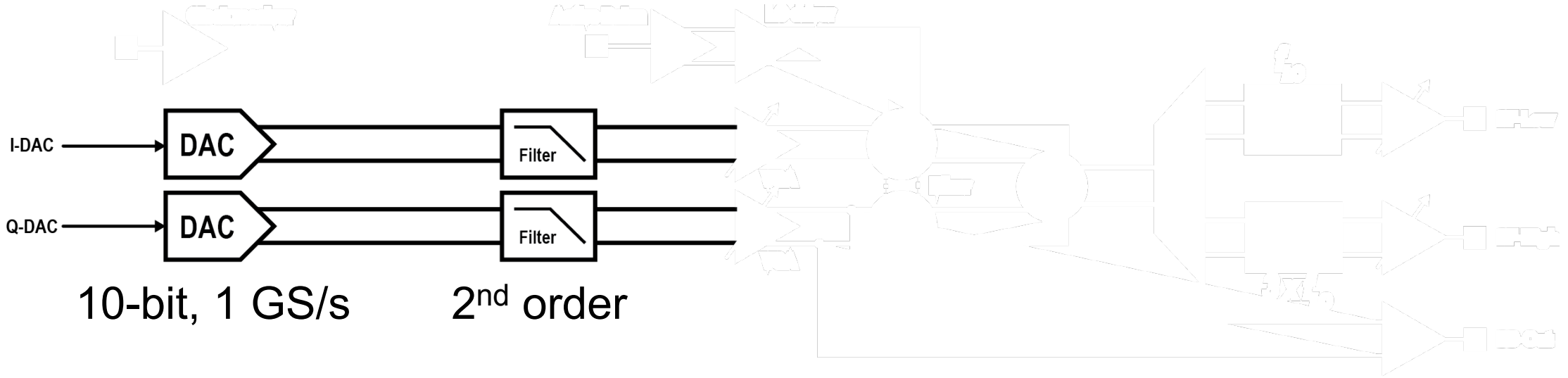
Single-Sideband Transmitter

Single-Sideband Transmitter



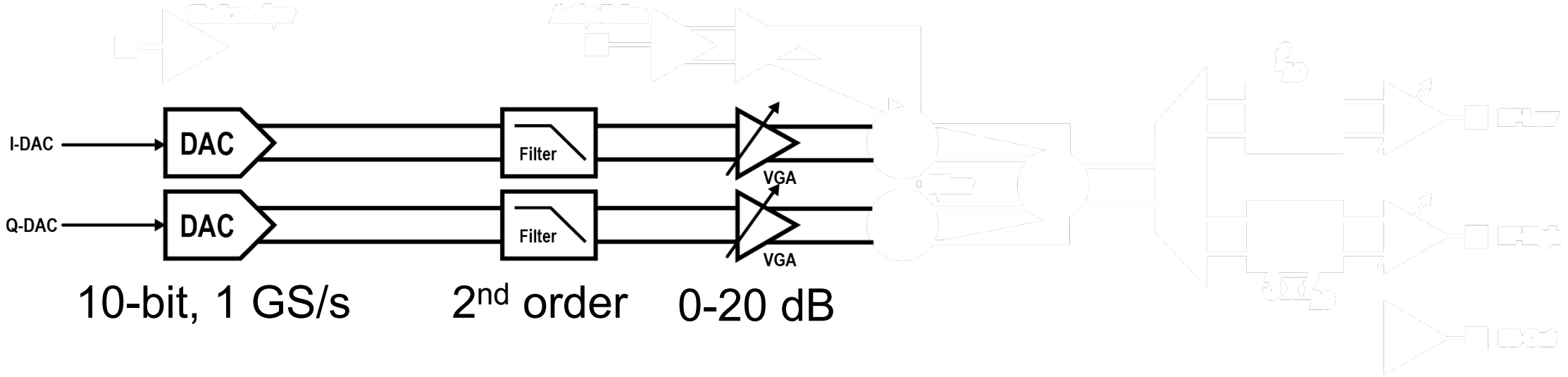
10-bit, 1 GS/s

Single-Sideband Transmitter



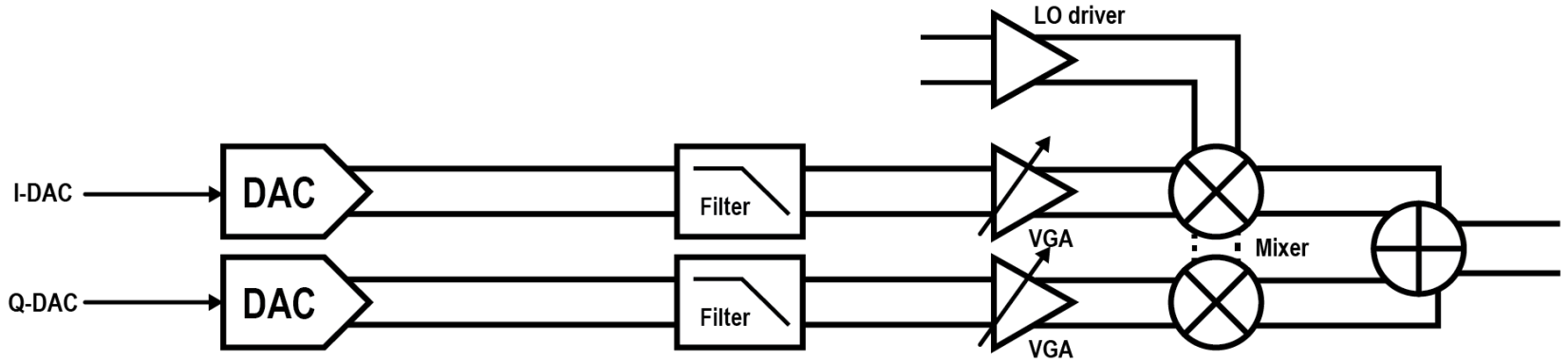
10-bit, 1 GS/s 2nd order

Single-Sideband Transmitter



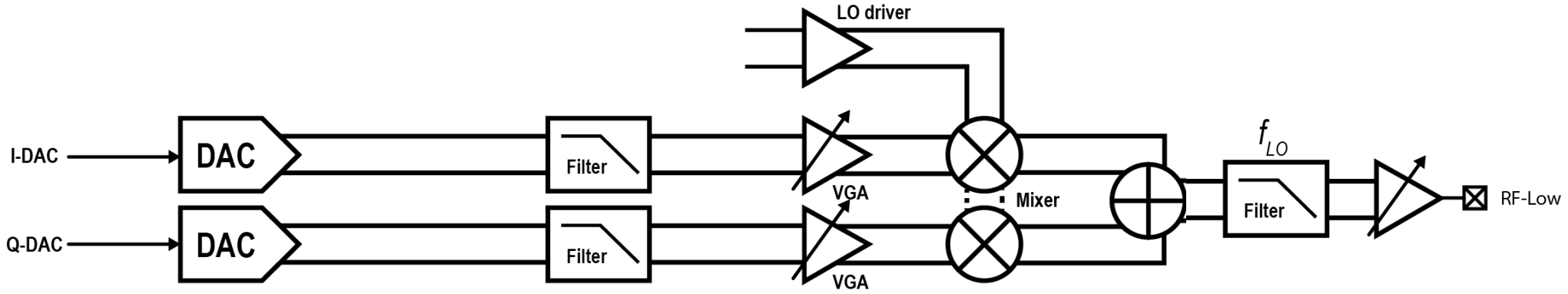
10-bit, 1 GS/s 2nd order 0-20 dB

Single-Sideband Transmitter



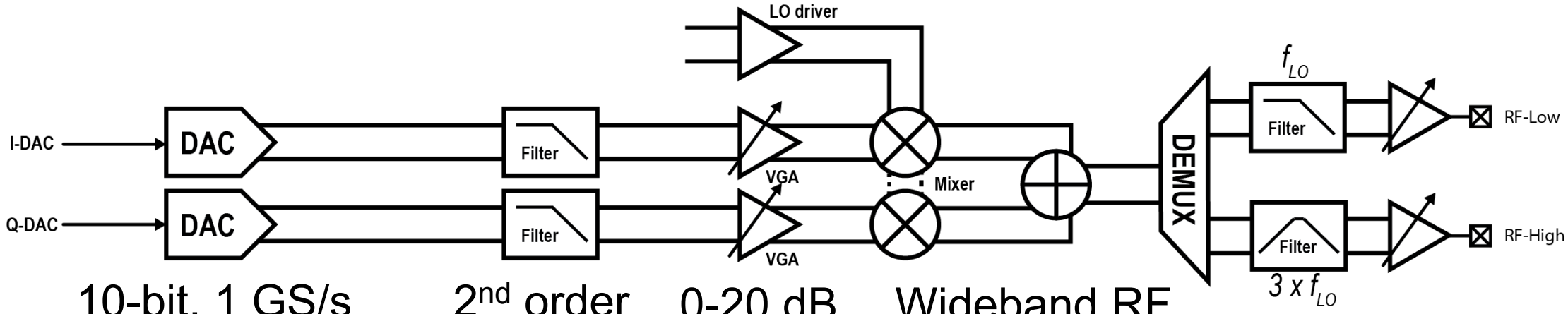
10-bit, 1 GS/s 2nd order 0-20 dB Wideband RF

Single-Sideband Transmitter



10-bit, 1 GS/s 2nd order 0-20 dB Wideband RF

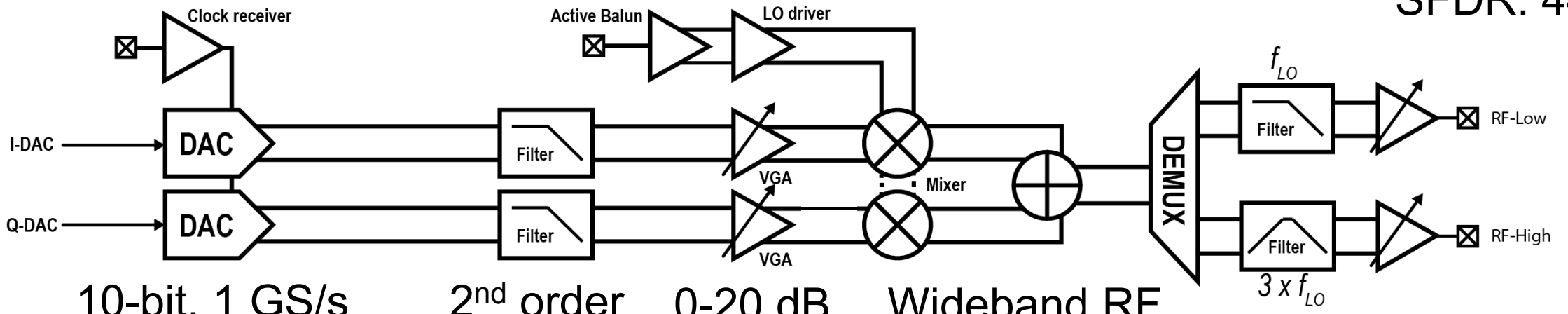
Single-Sideband Transmitter



Single-Sideband Transmitter

SNR: 44 dB

SFDR: 44 dB

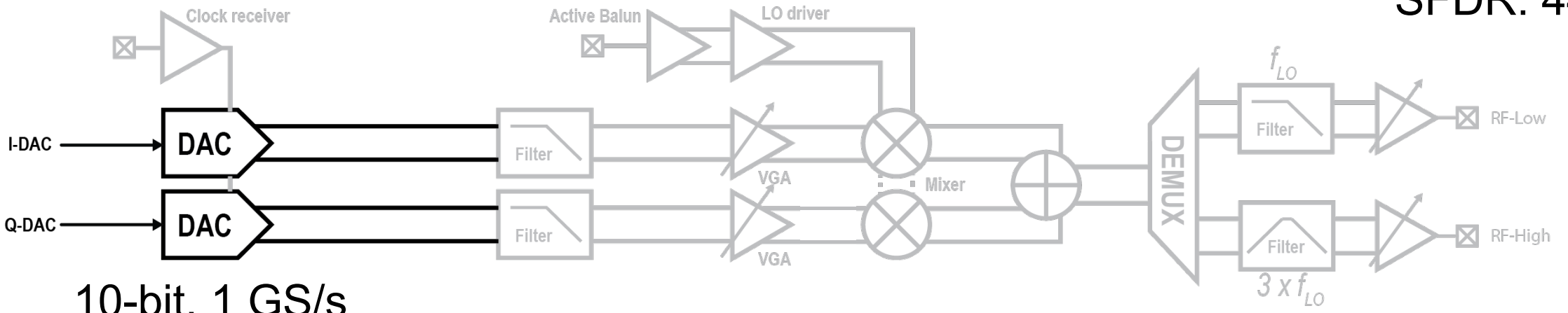


10-bit, 1 GS/s 2nd order 0-20 dB Wideband RF

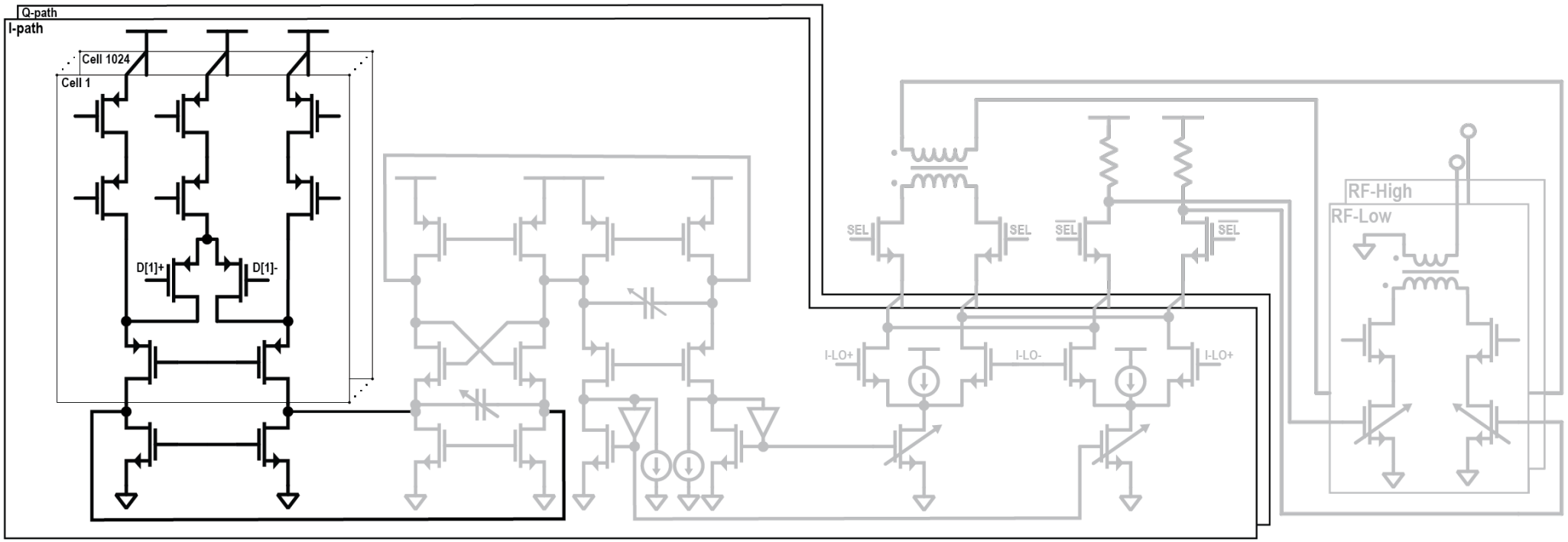
Single-Sideband Transmitter

SNR: 44 dB

SFDR: 44 dB

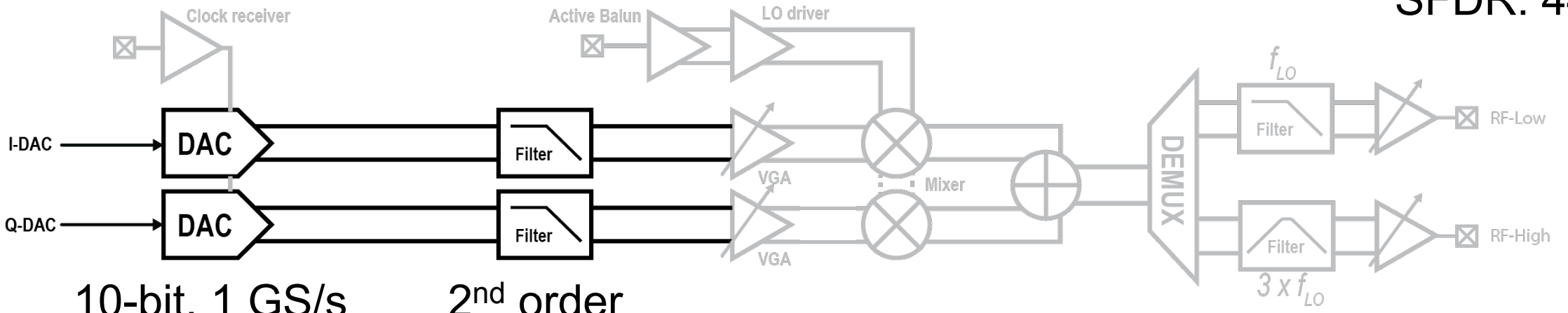


10-bit, 1 GS/s

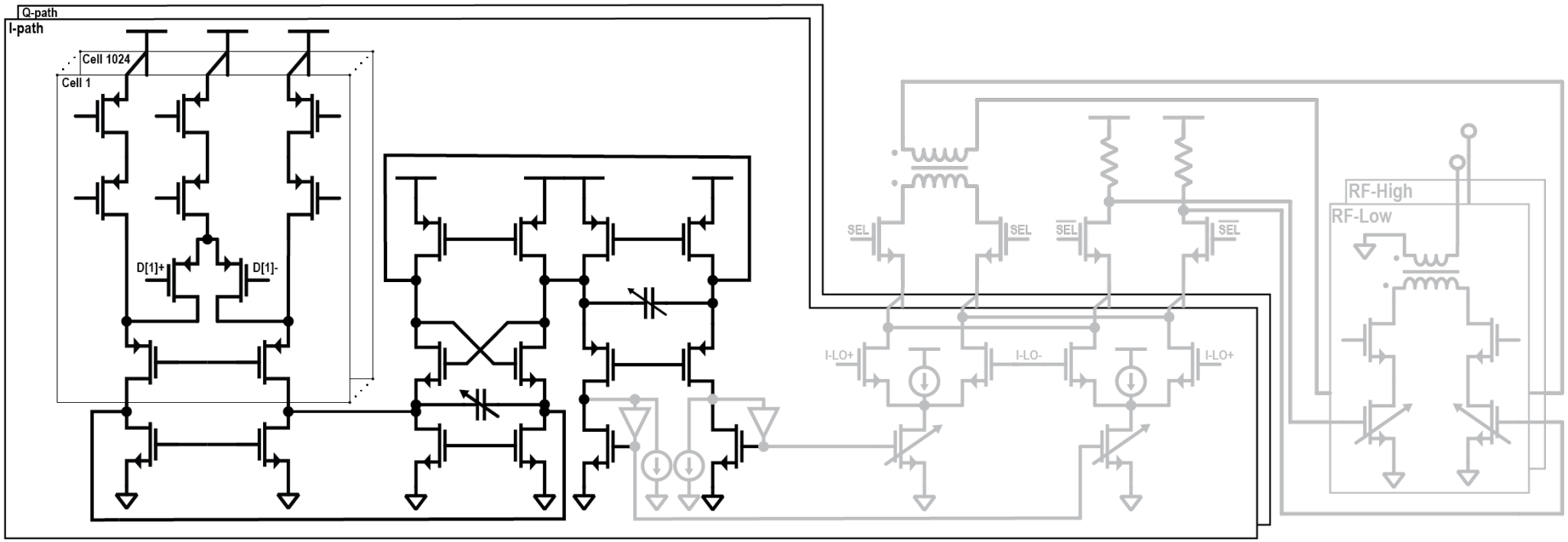


Single-Sideband Transmitter

SNR: 44 dB
SFDR: 44 dB

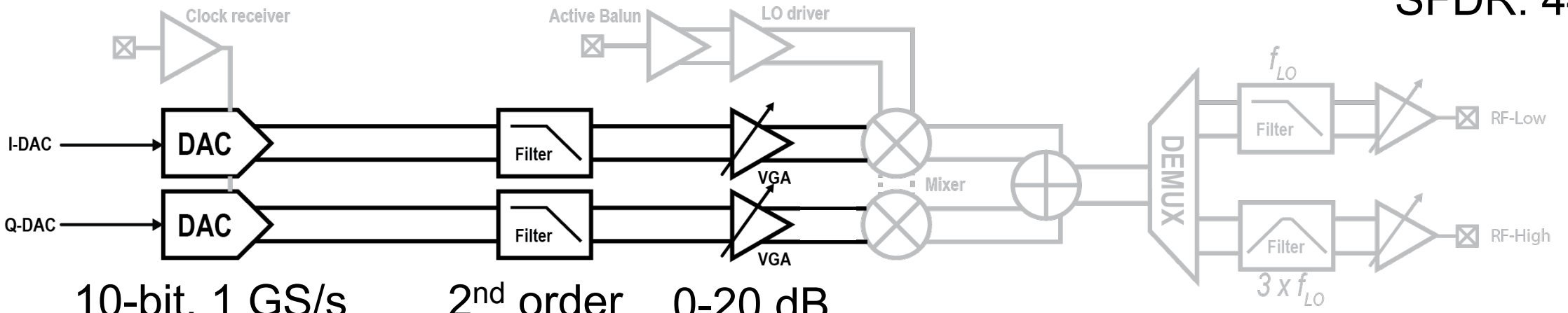


10-bit, 1 GS/s 2nd order

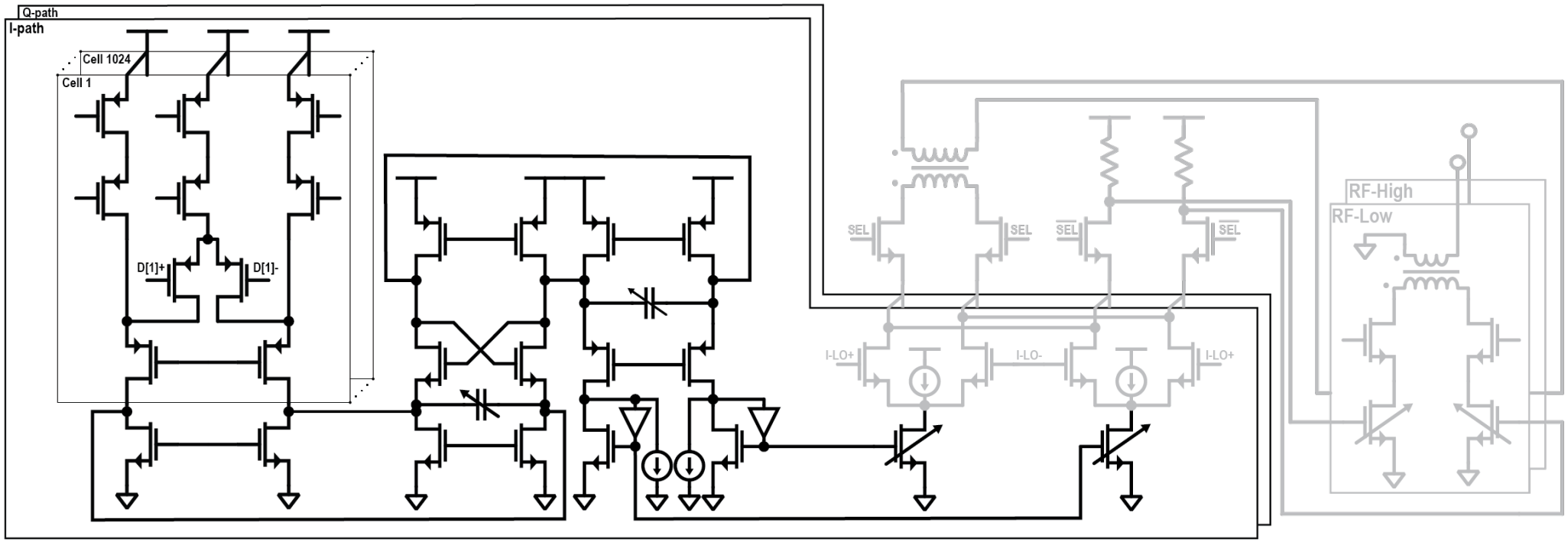


Single-Sideband Transmitter

SNR: 44 dB
SFDR: 44 dB

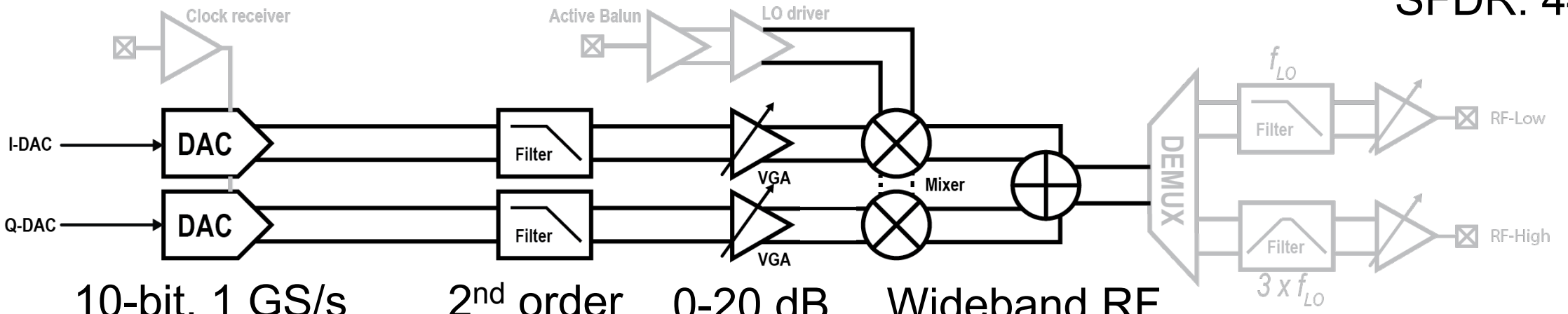


10-bit, 1 GS/s 2nd order 0-20 dB

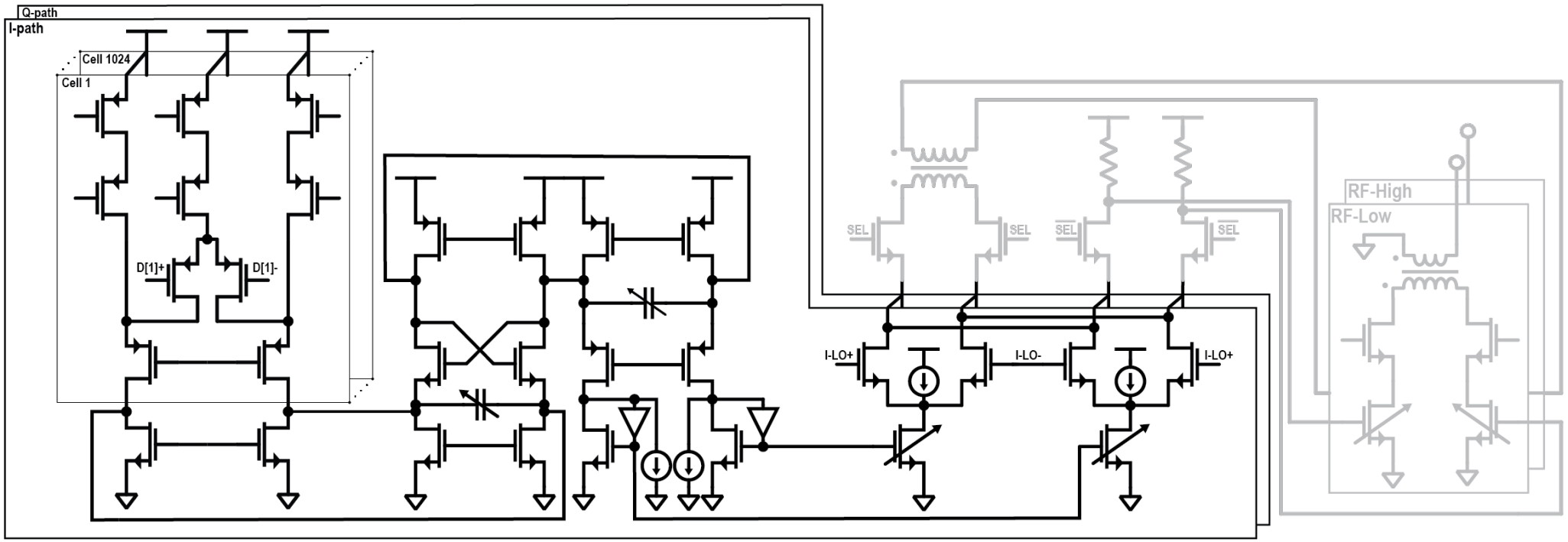


Single-Sideband Transmitter

SNR: 44 dB
SFDR: 44 dB

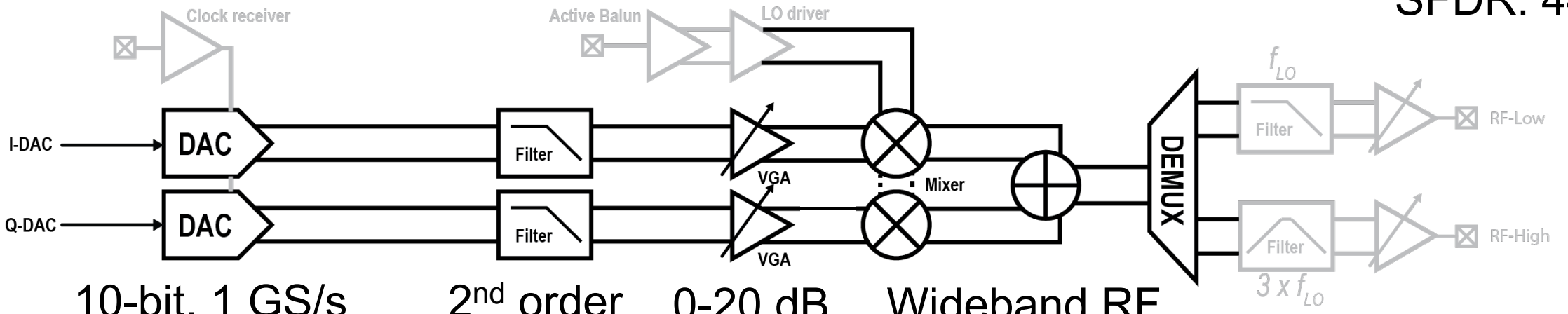


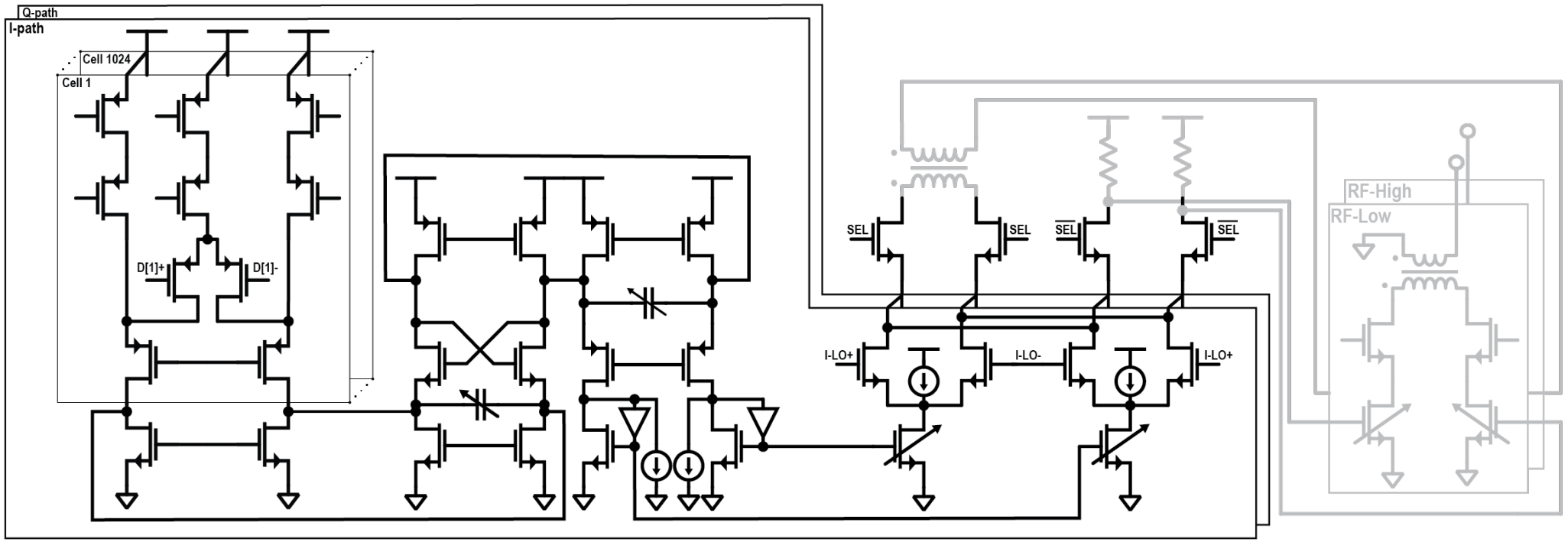
10-bit, 1 GS/s 2nd order 0-20 dB Wideband RF



Single-Sideband Transmitter

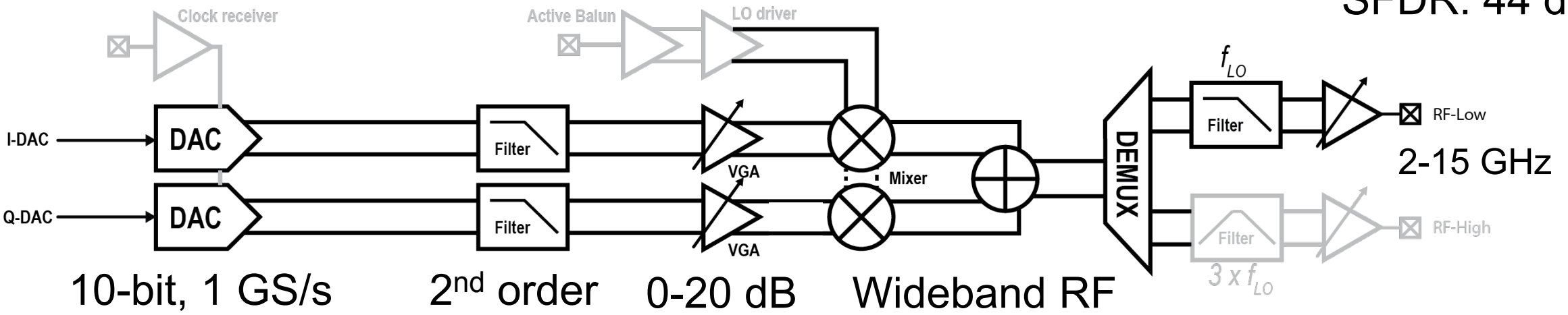
SNR: 44 dB
SFDR: 44 dB

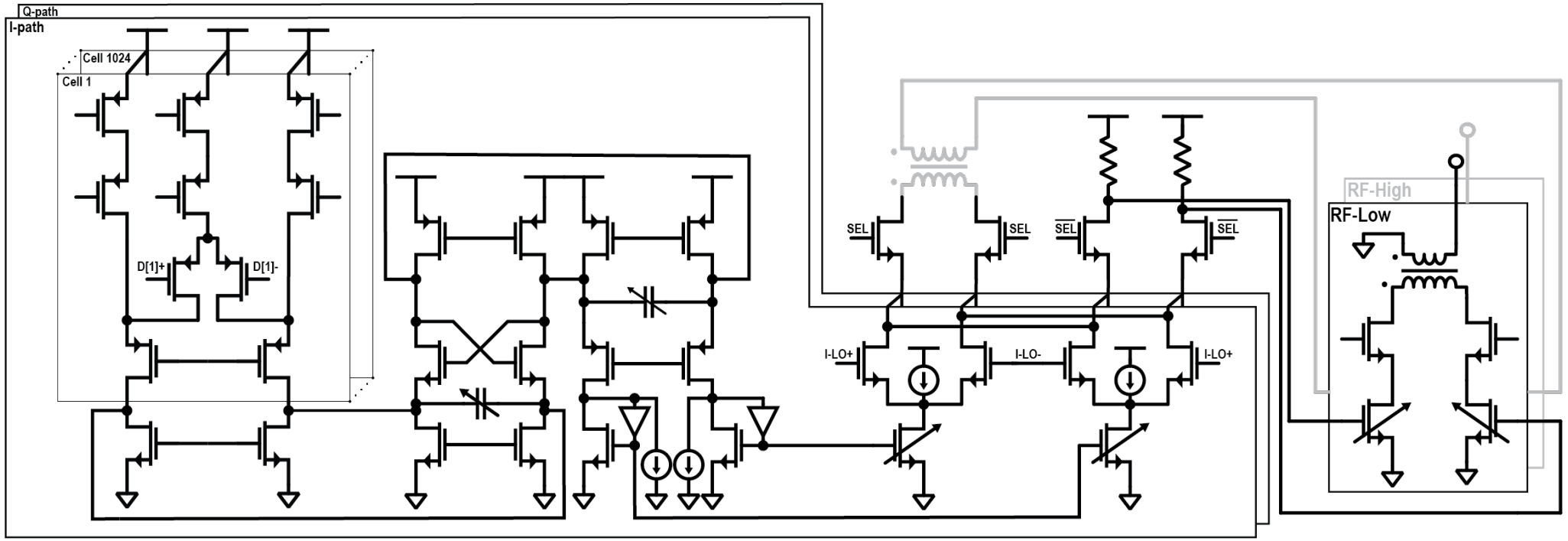




Single-Sideband Transmitter

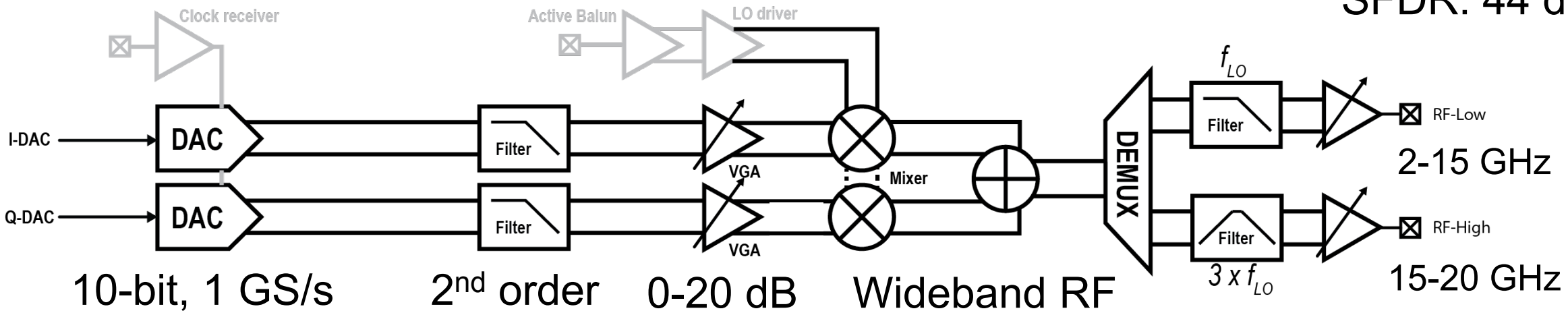
SNR: 44 dB
SFDR: 44 dB

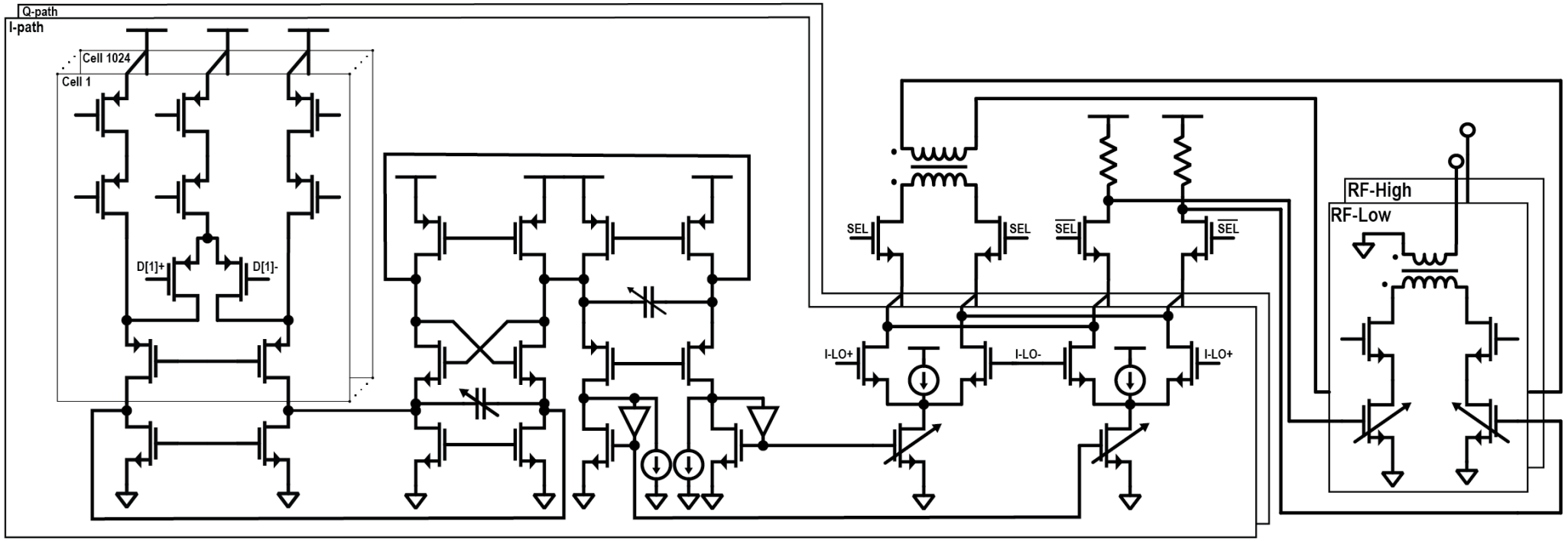




Single-Sideband Transmitter

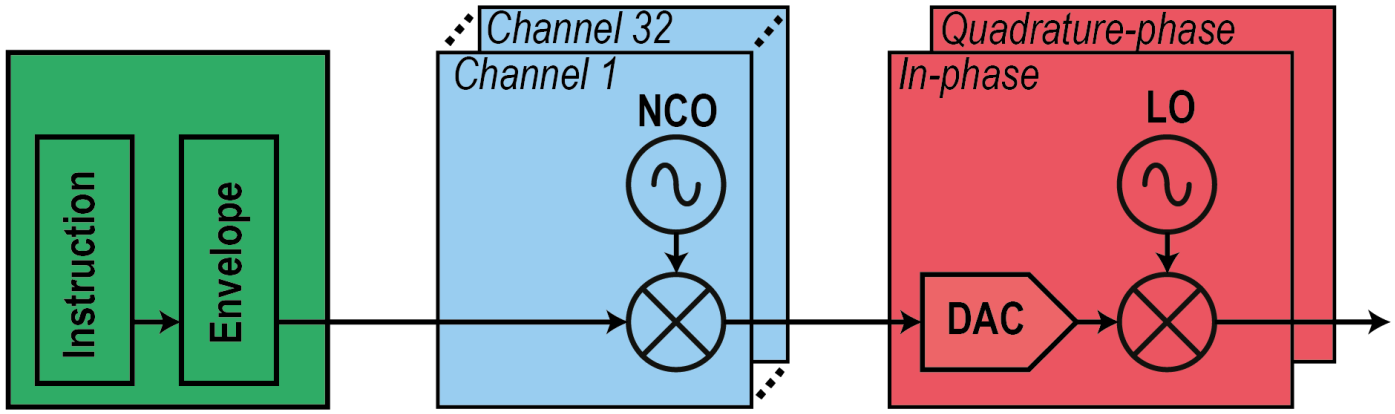
SNR: 44 dB
SFDR: 44 dB

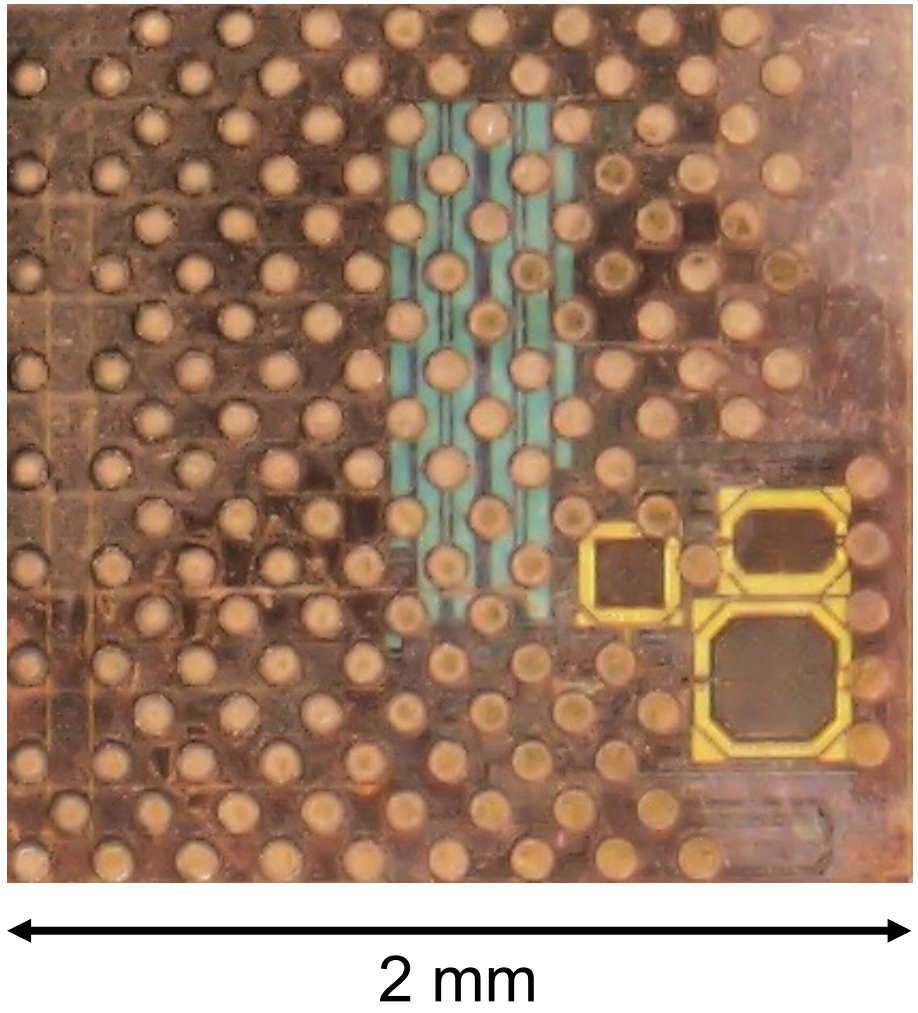




Horse Ridge SoC Die Photo

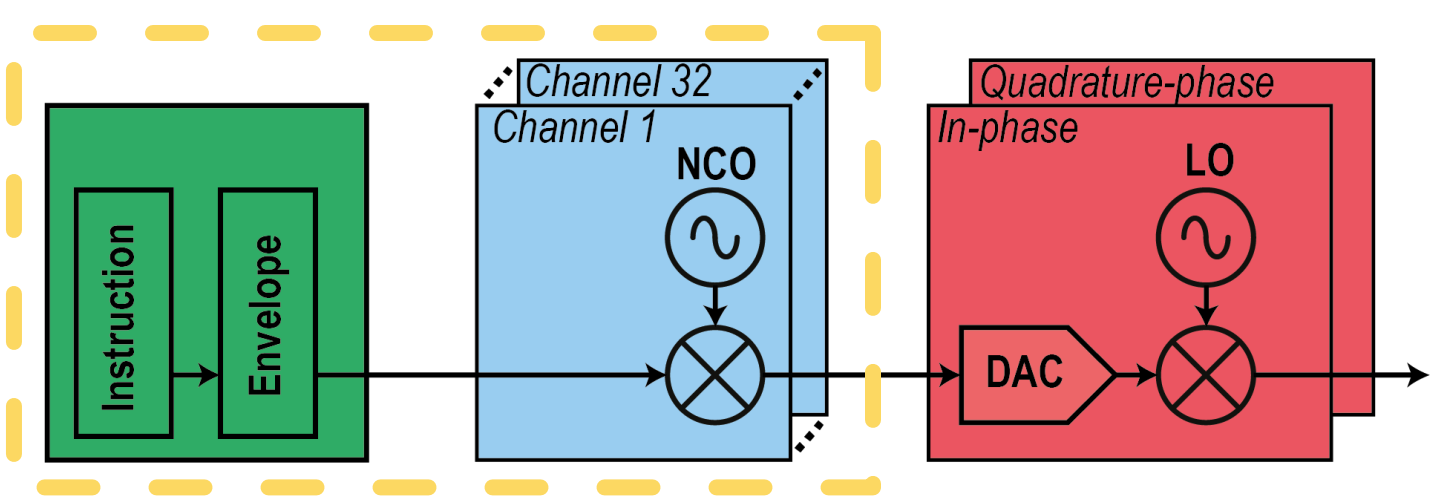
- Intel 22nm FinFET (22FFL) Technology

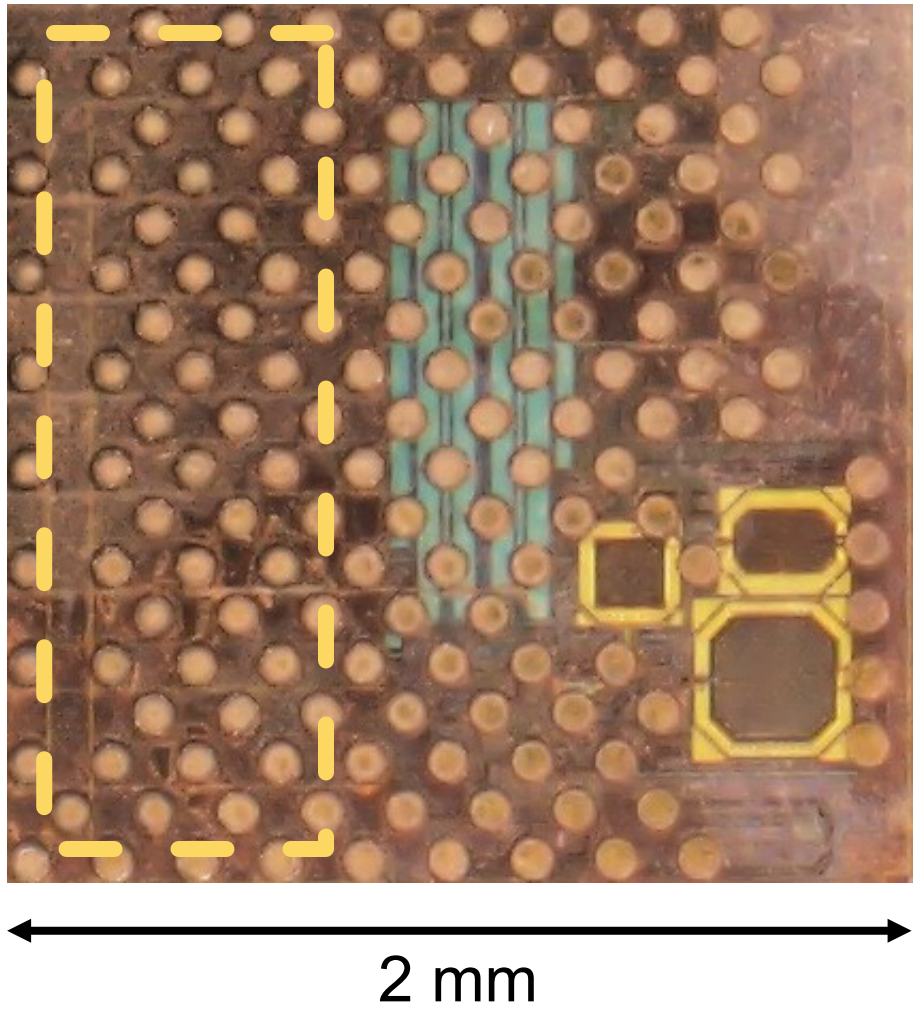




Horse Ridge SoC Die Photo

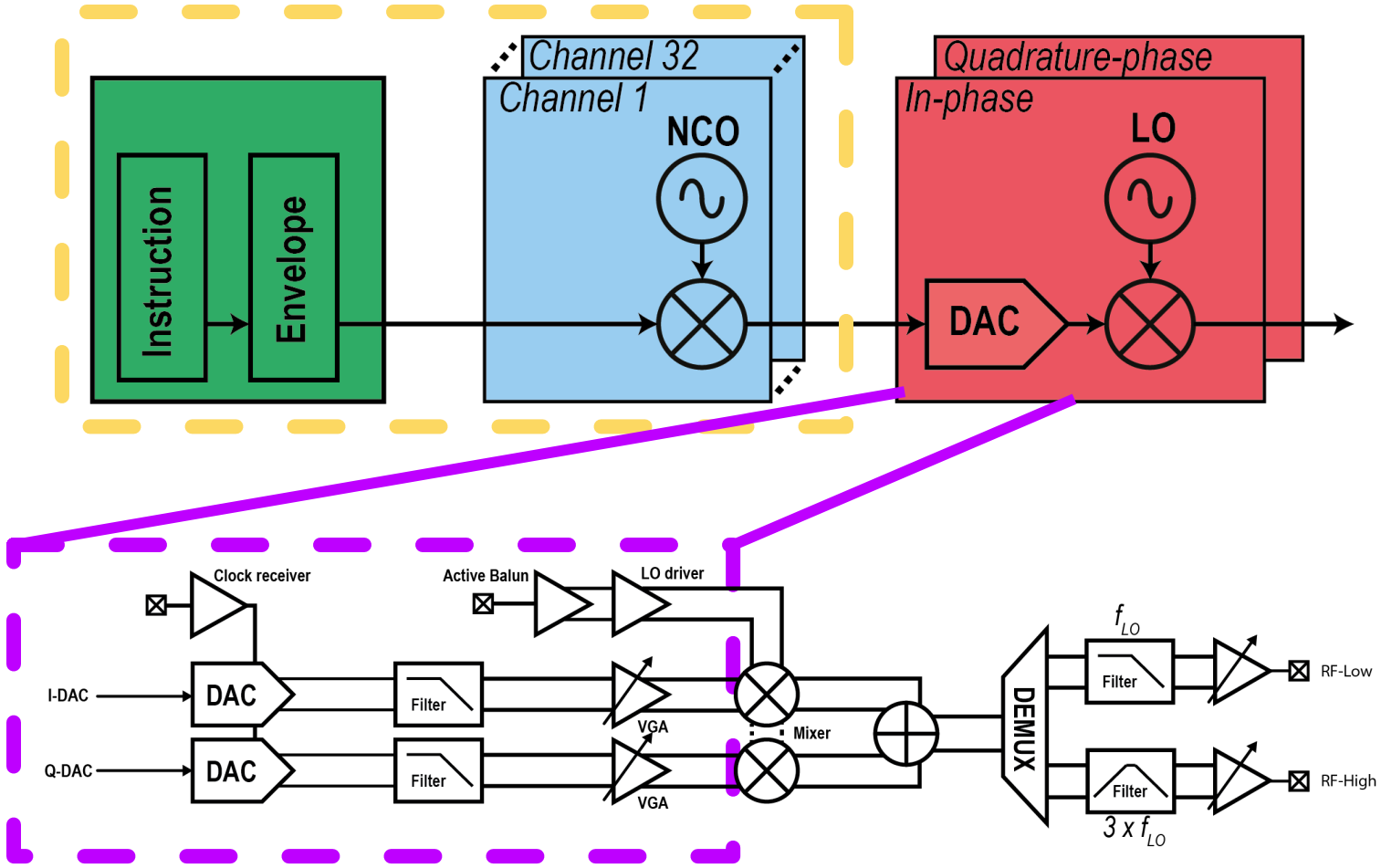
- Intel 22nm FinFET (22FFL) Technology

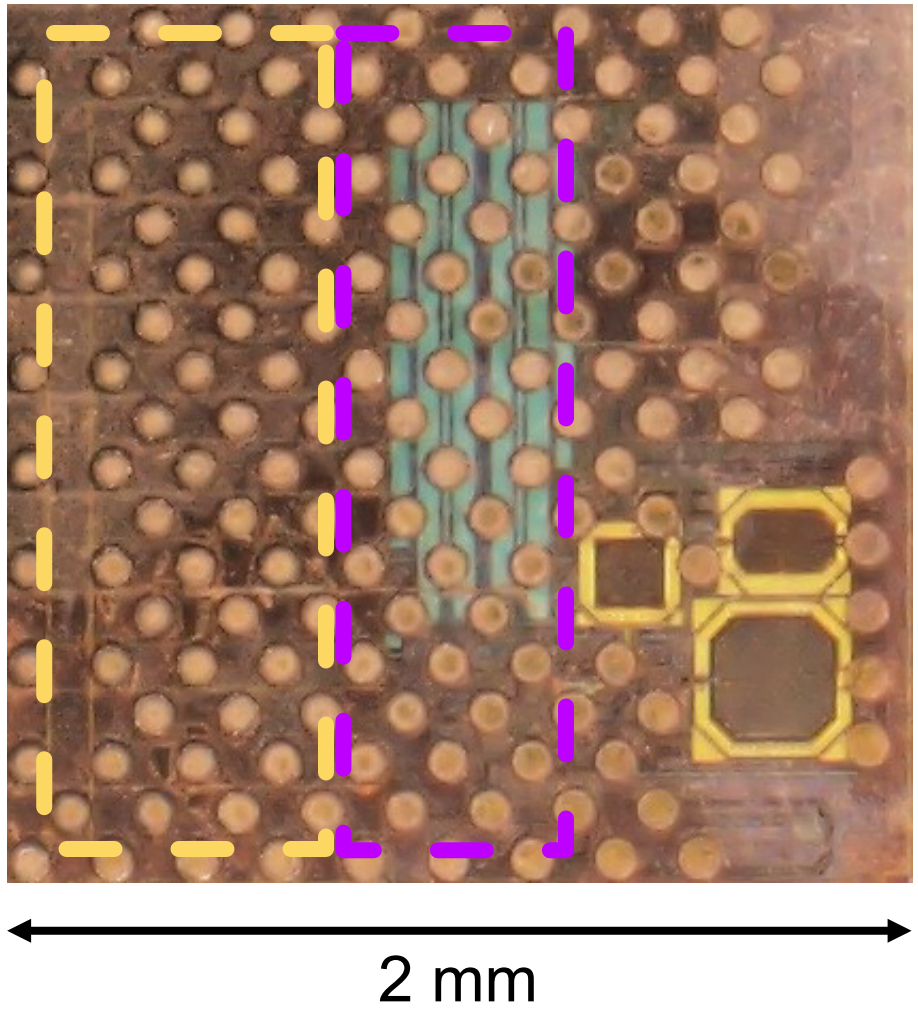




Horse Ridge SoC Die Photo

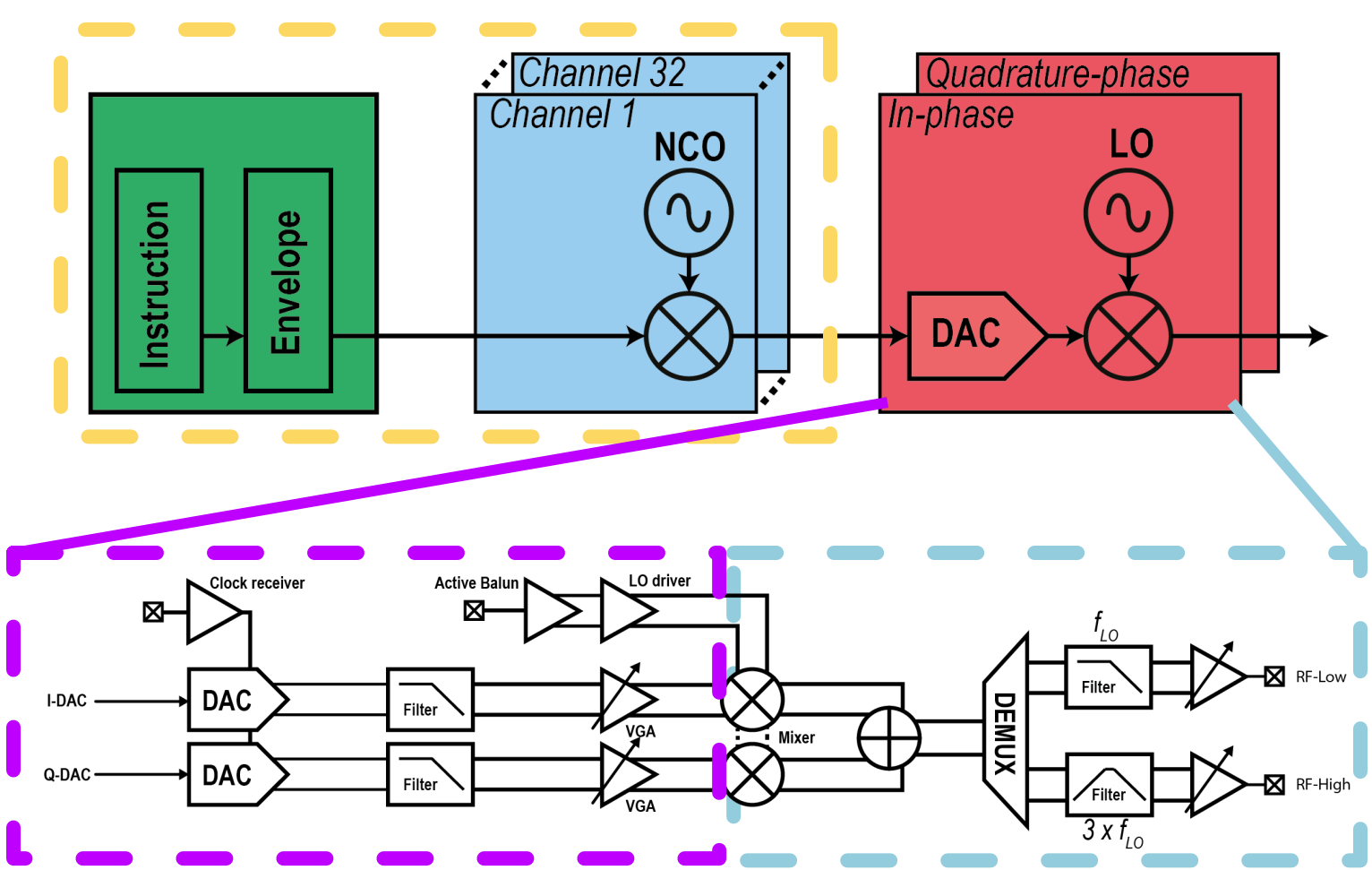
- Intel 22nm FinFET (22FFL) Technology

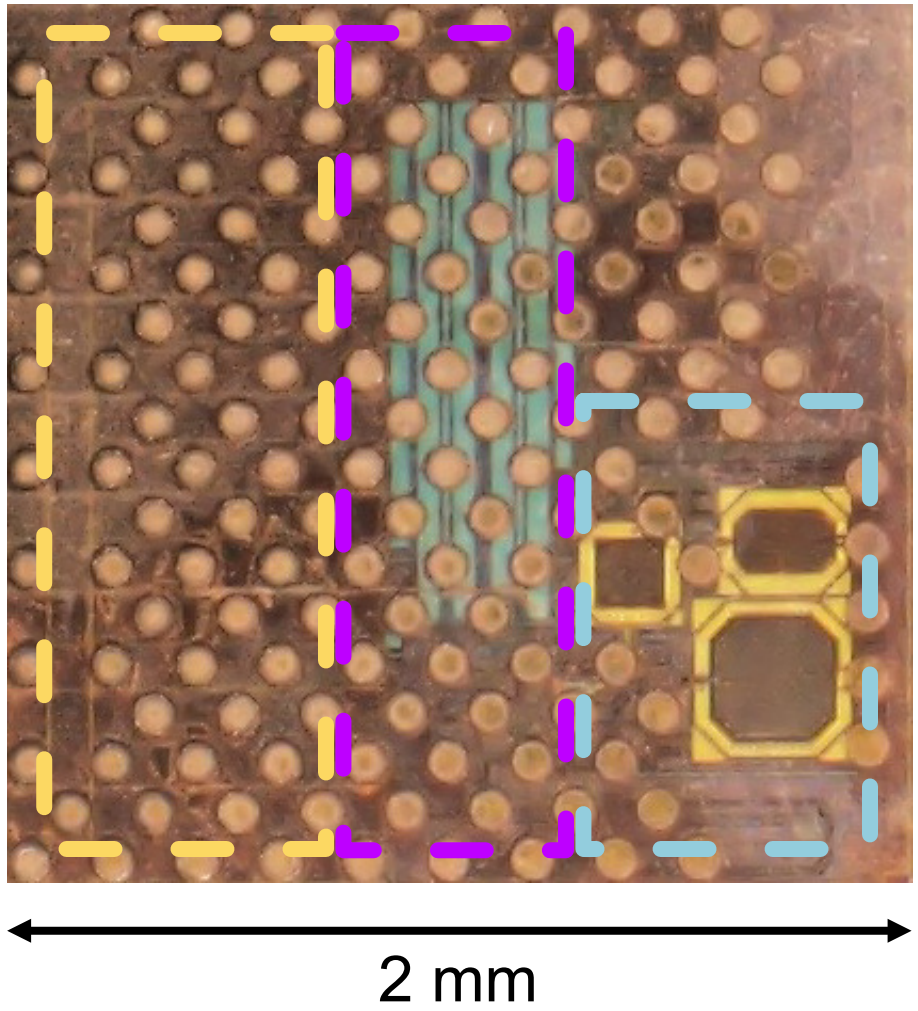




Horse Ridge SoC Die Photo

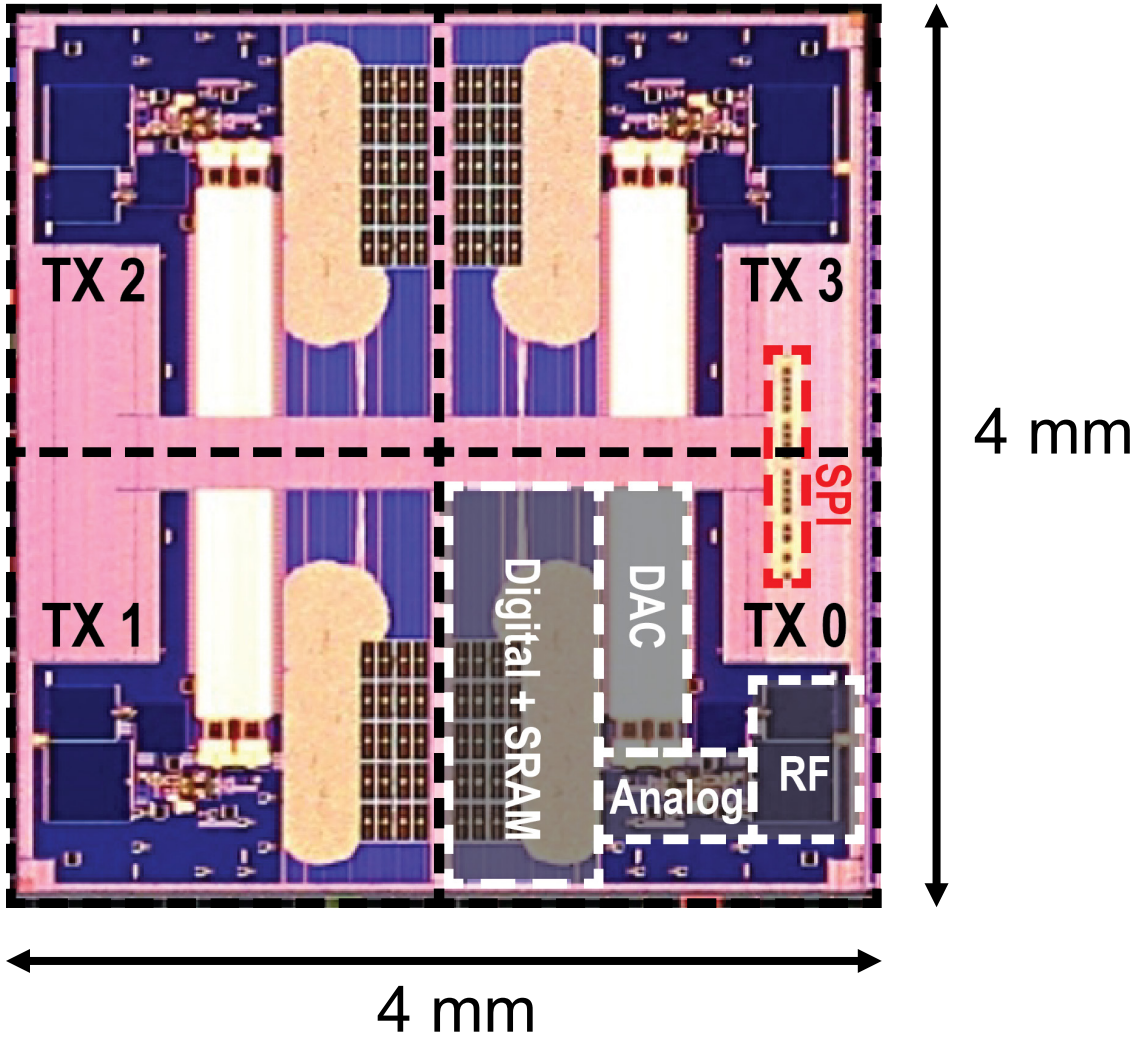
- Intel 22nm FinFET (22FFL) Technology



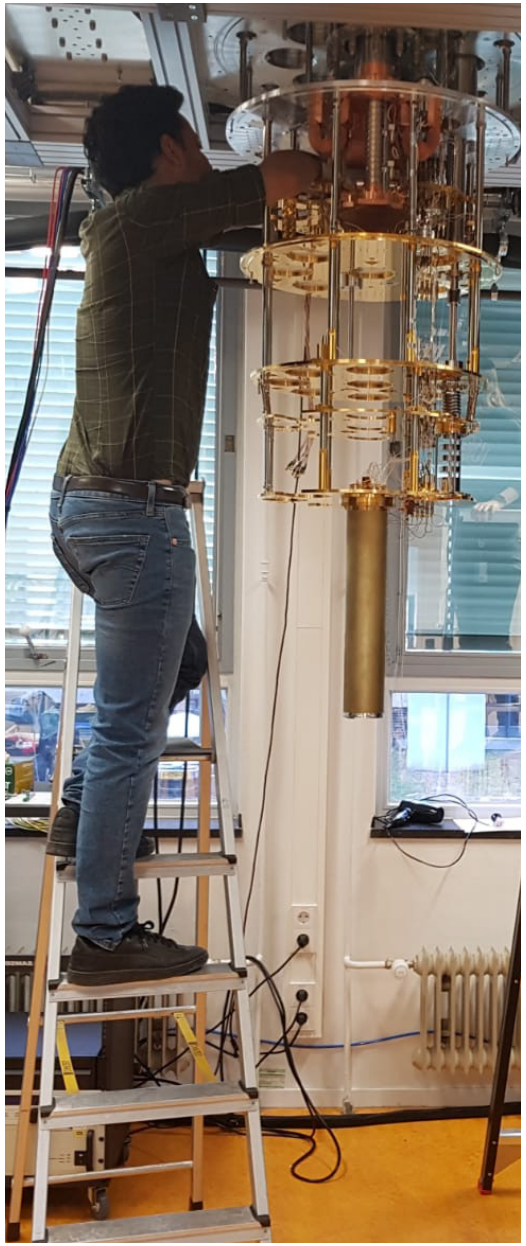


Horse Ridge SoC Die Photo

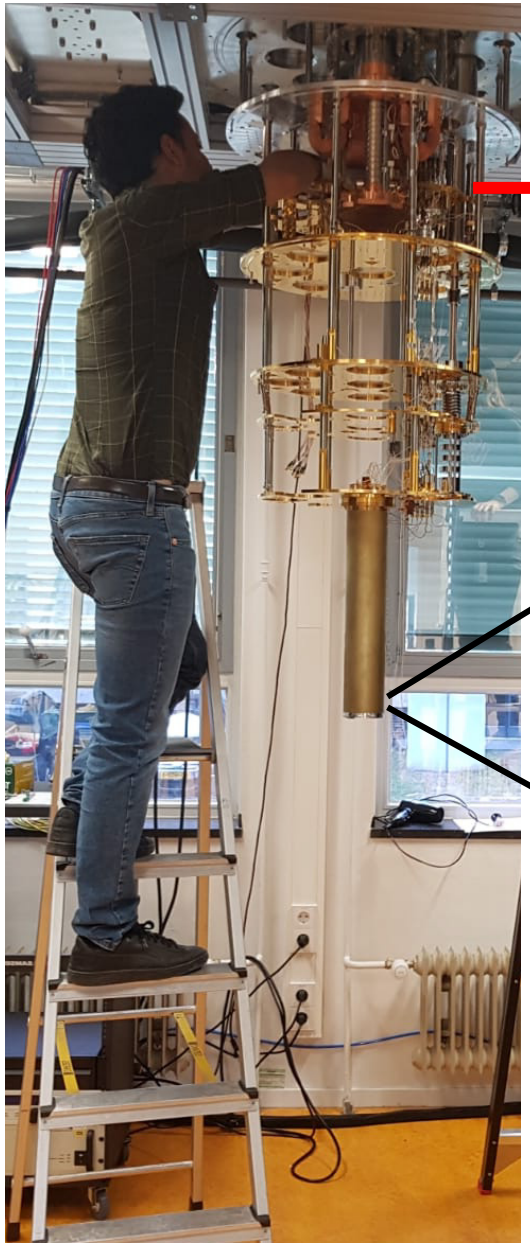
- Intel 22nm FinFET (22FFL) Technology
- 4 Transmitters (TX)
  - 32 channels each
  - 128 qubits



Measurement Setup

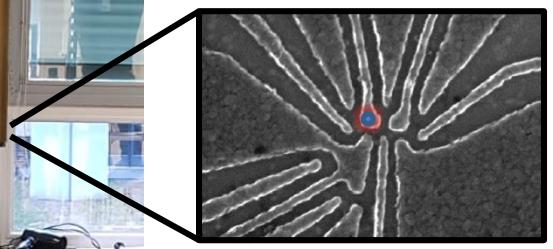


Measurement Setup



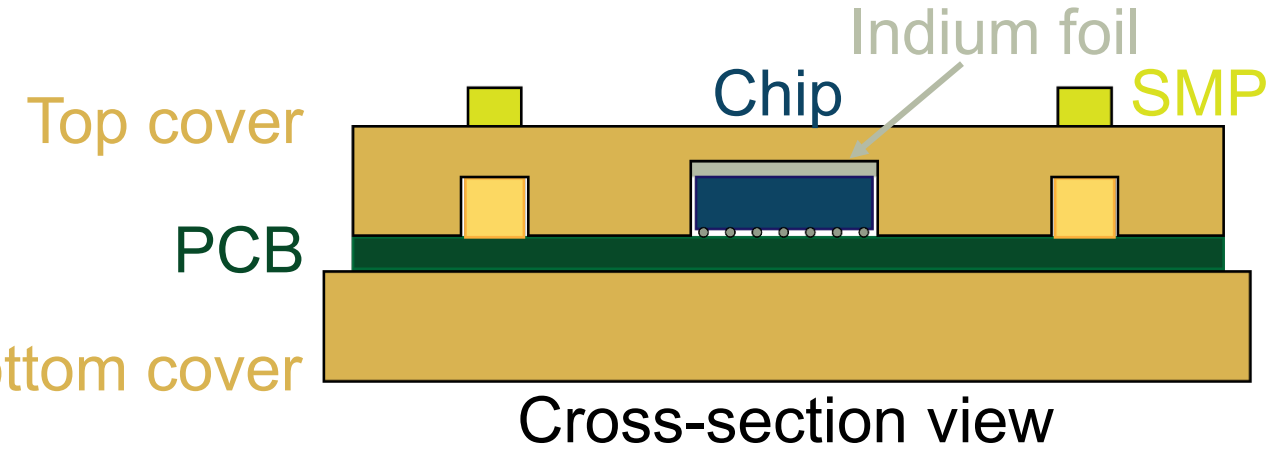
Chip at
3 K plate

60 nm

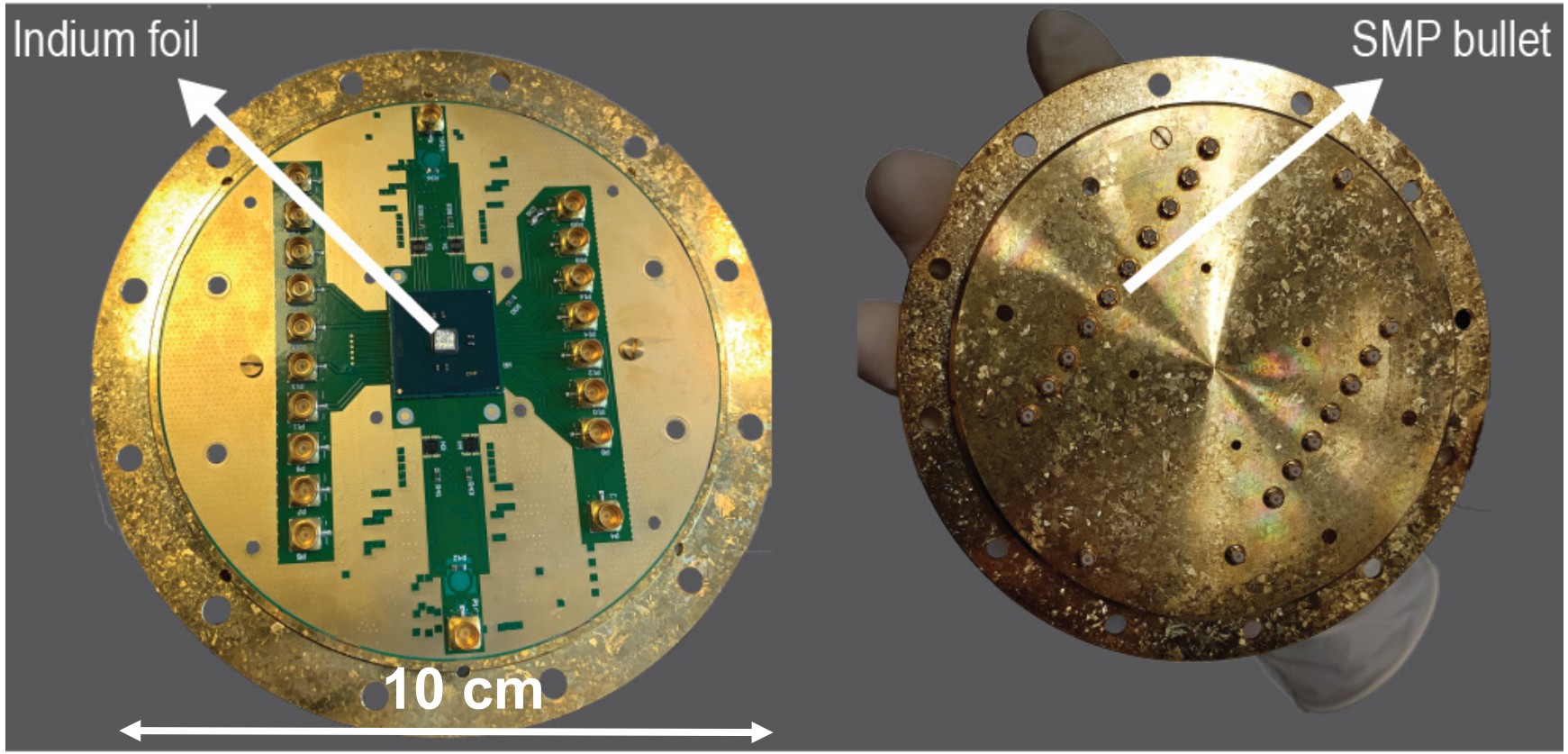


Qubit at
10 mK

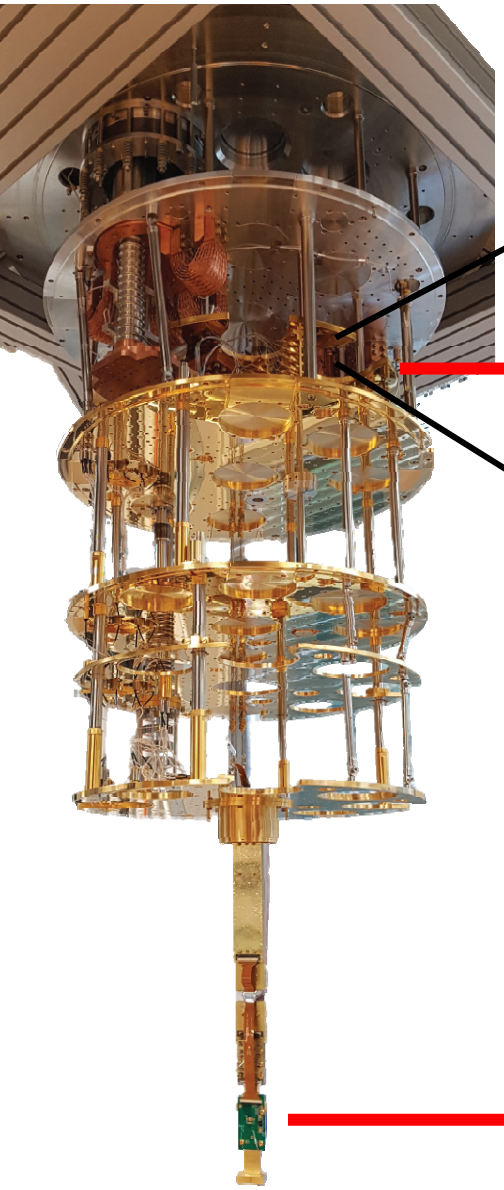
Enclosure



Cross-section view

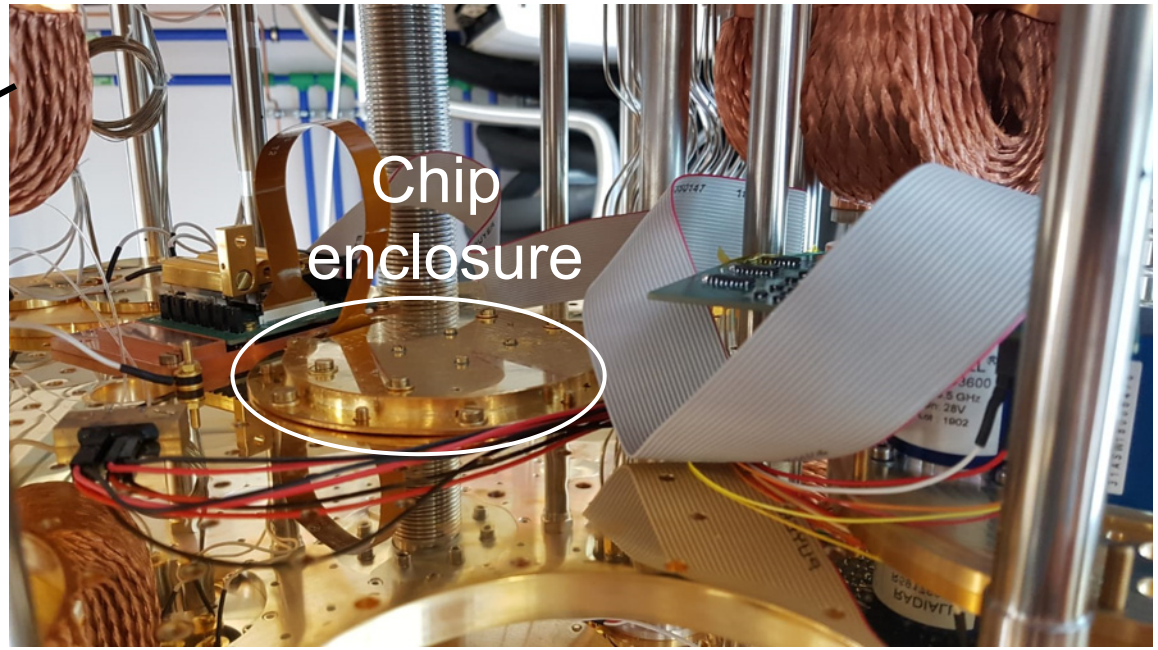


Measurement Setup

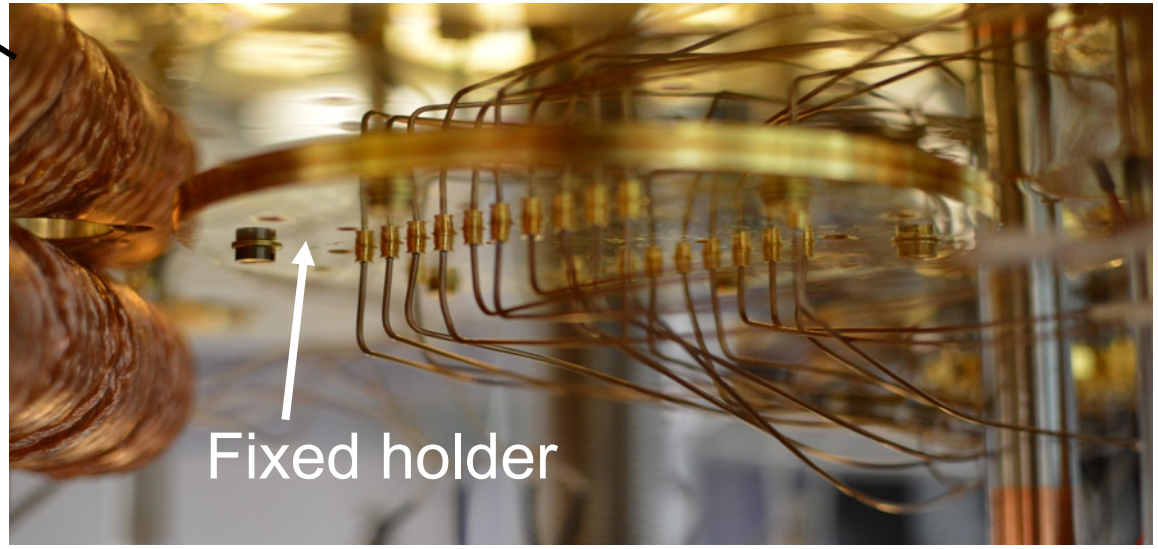


Chip at
3 K plate

Qubit at
10 mK

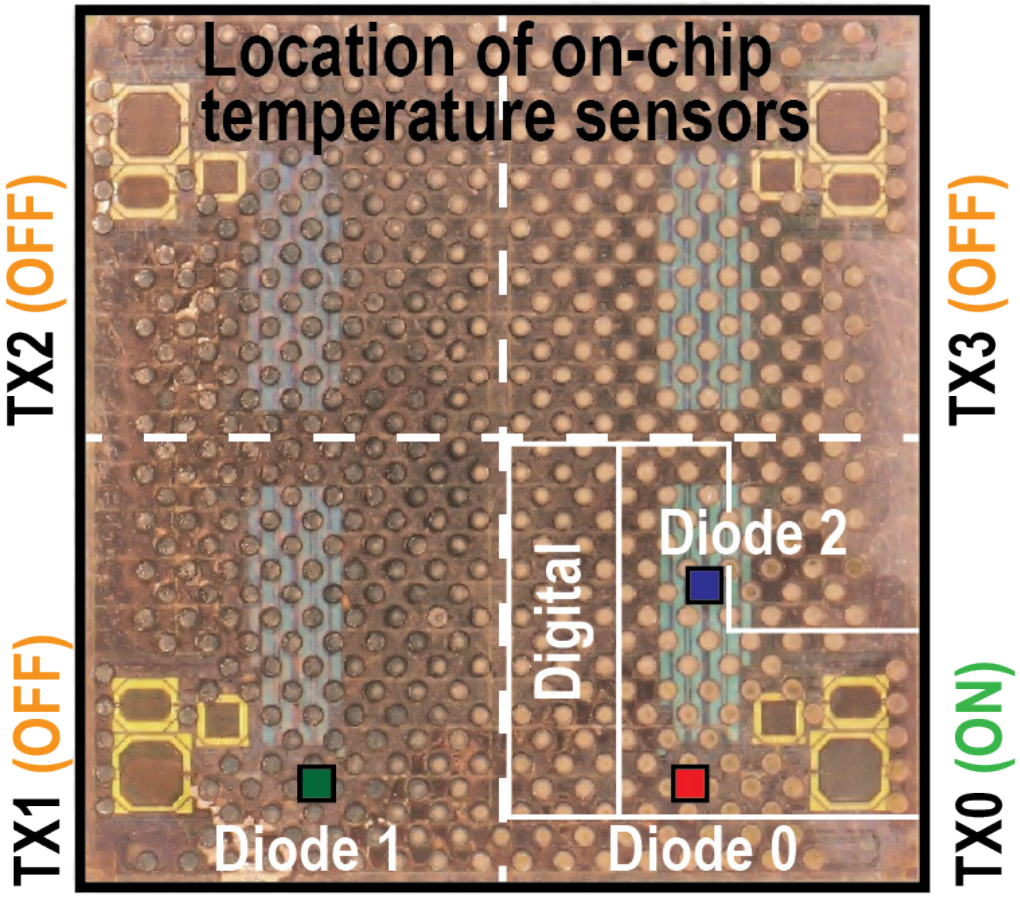


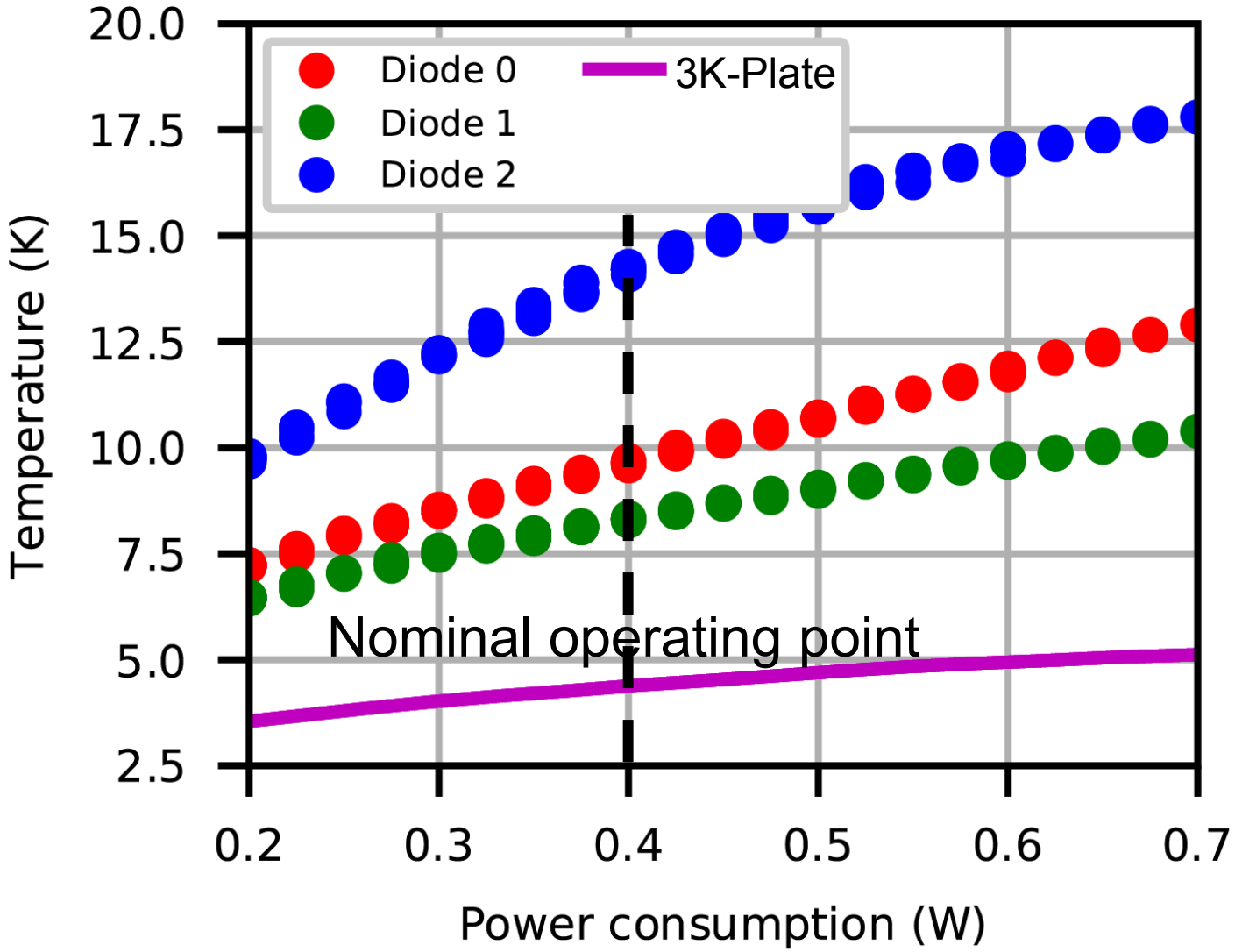
Top view



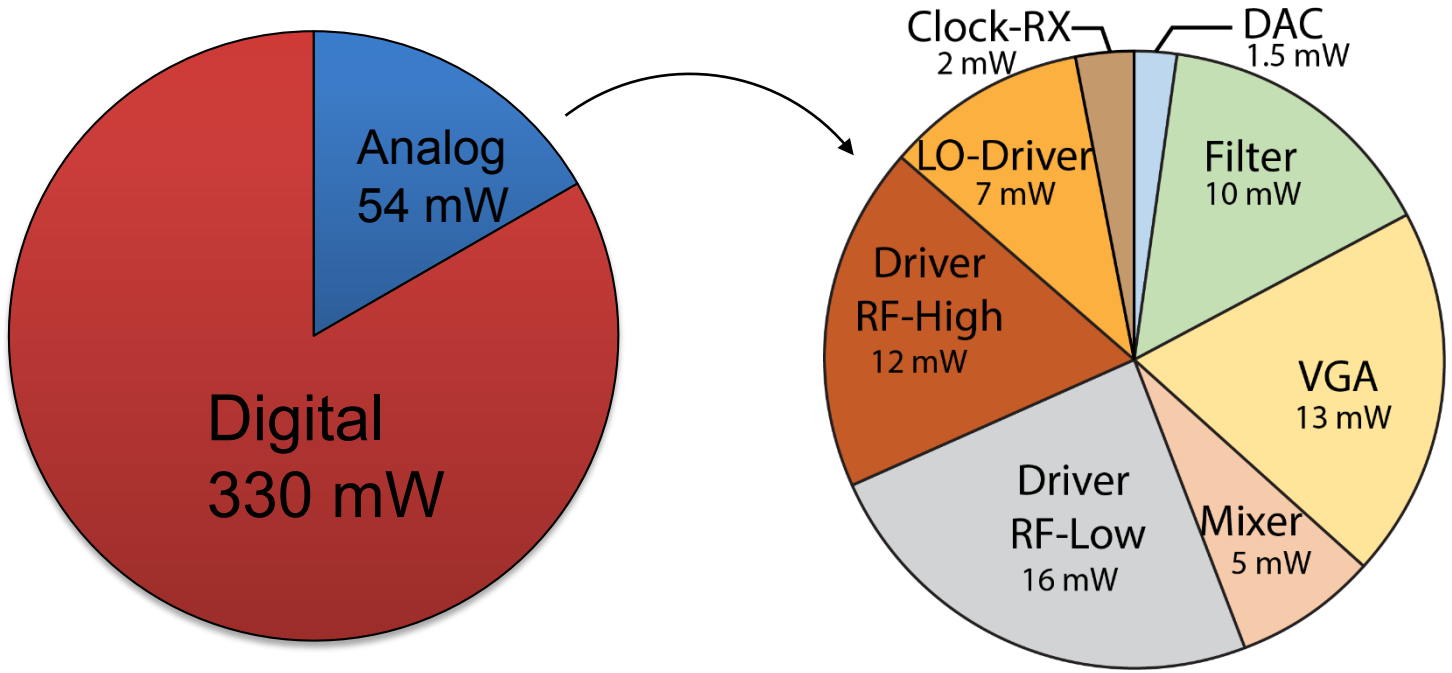
Bottom view

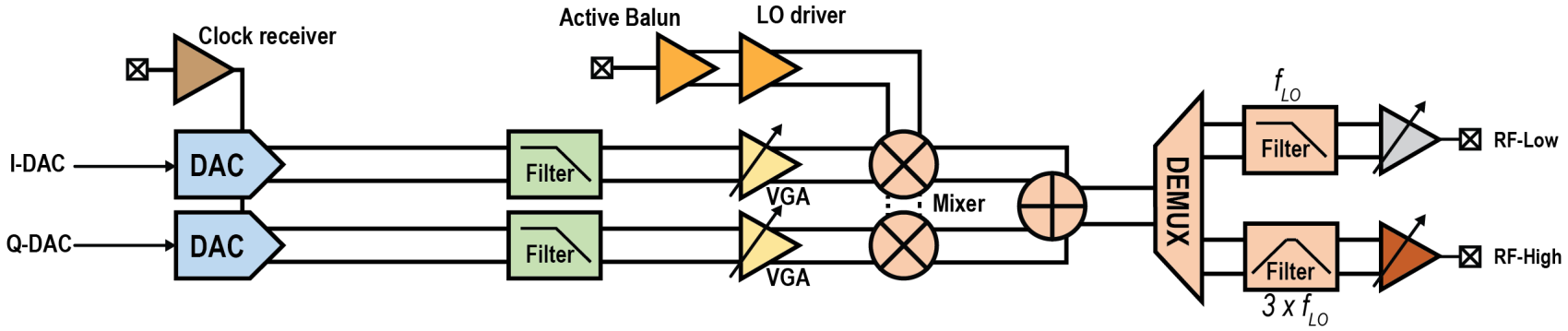
Self heating





Power Consumption @ 3 K



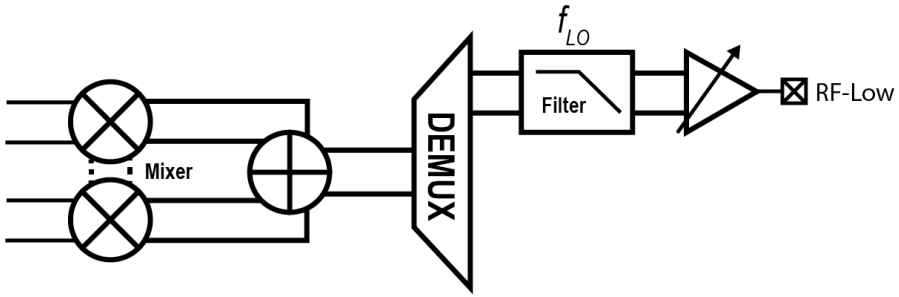


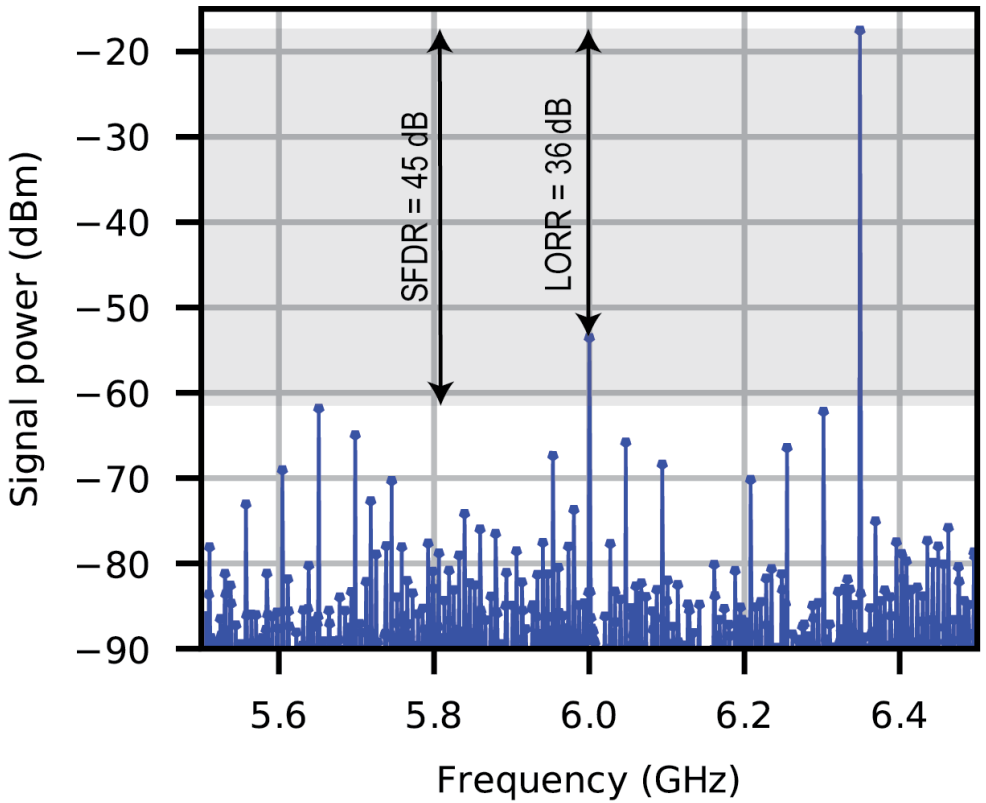
Single-tone output spectrum at 3 K

6 GHz

SFDR > 44 dB

SNR > 48 dB





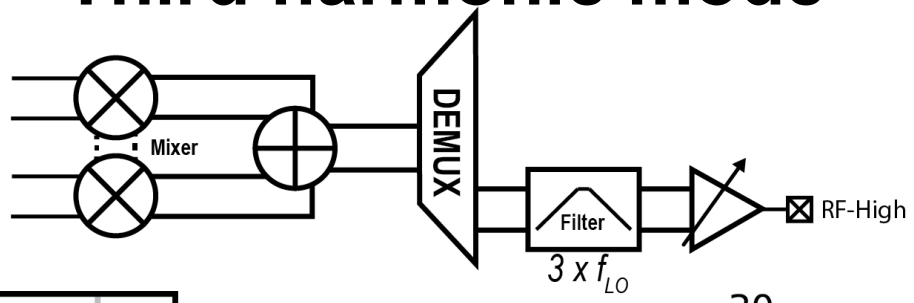
Single-tone output spectrum at 3 K

6 GHz

SFDR > 44 dB

SNR > 48 dB

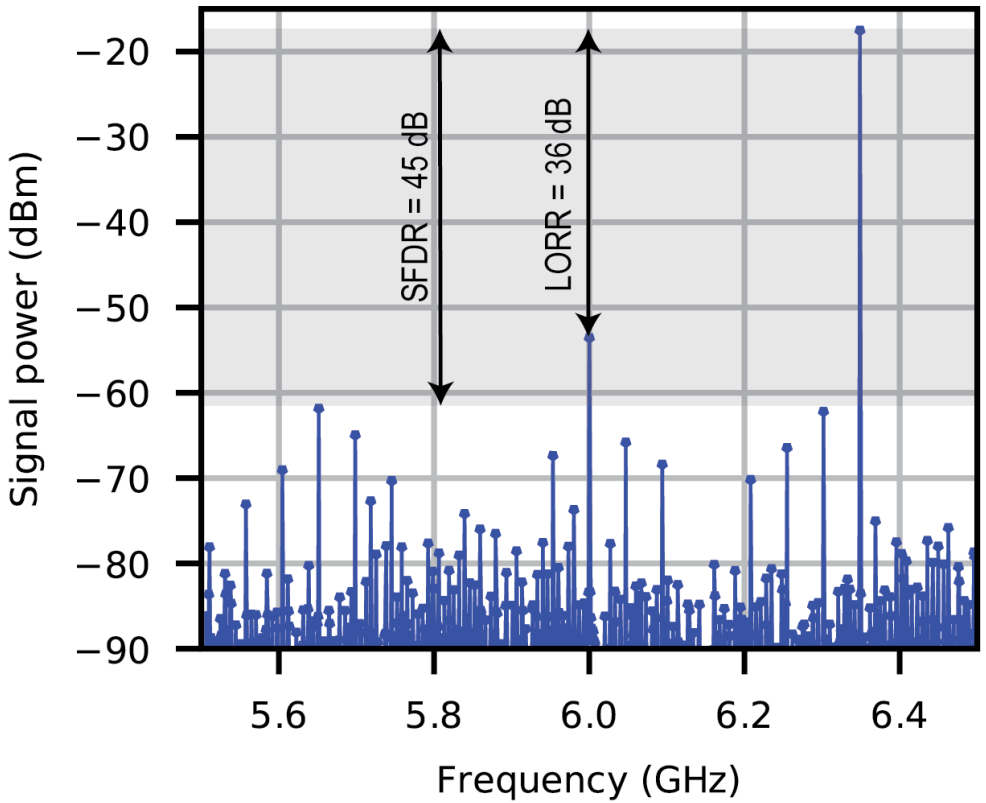
Third harmonic mode

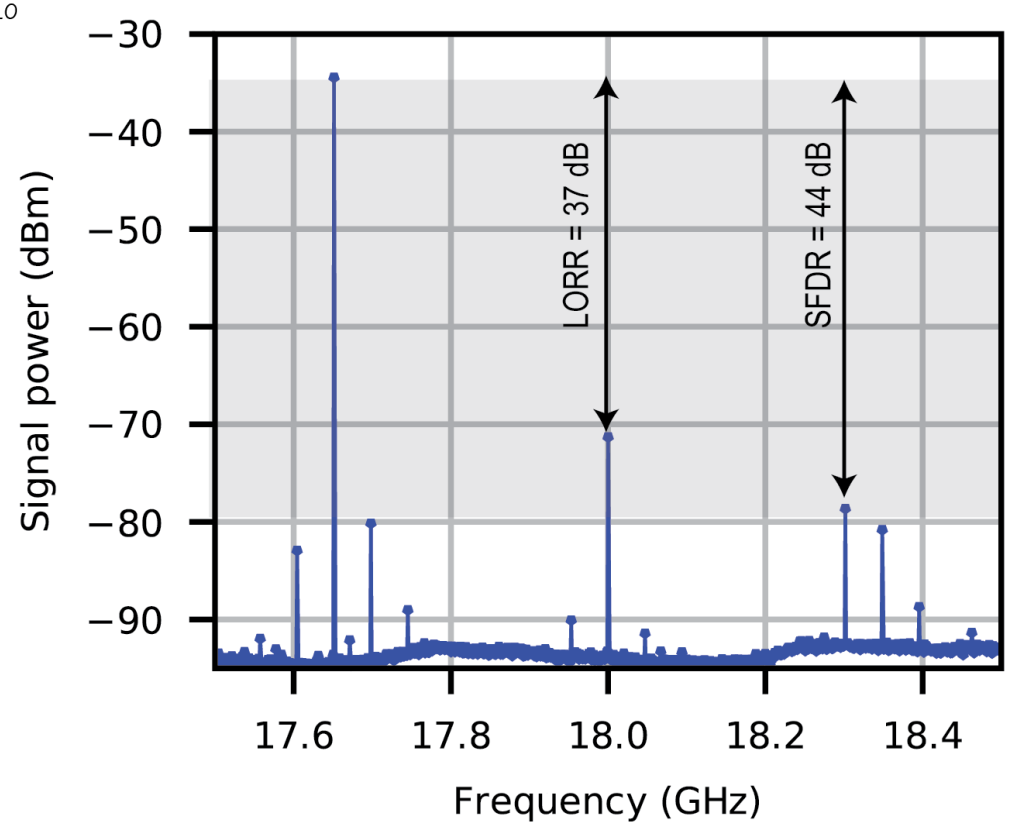


18 GHz

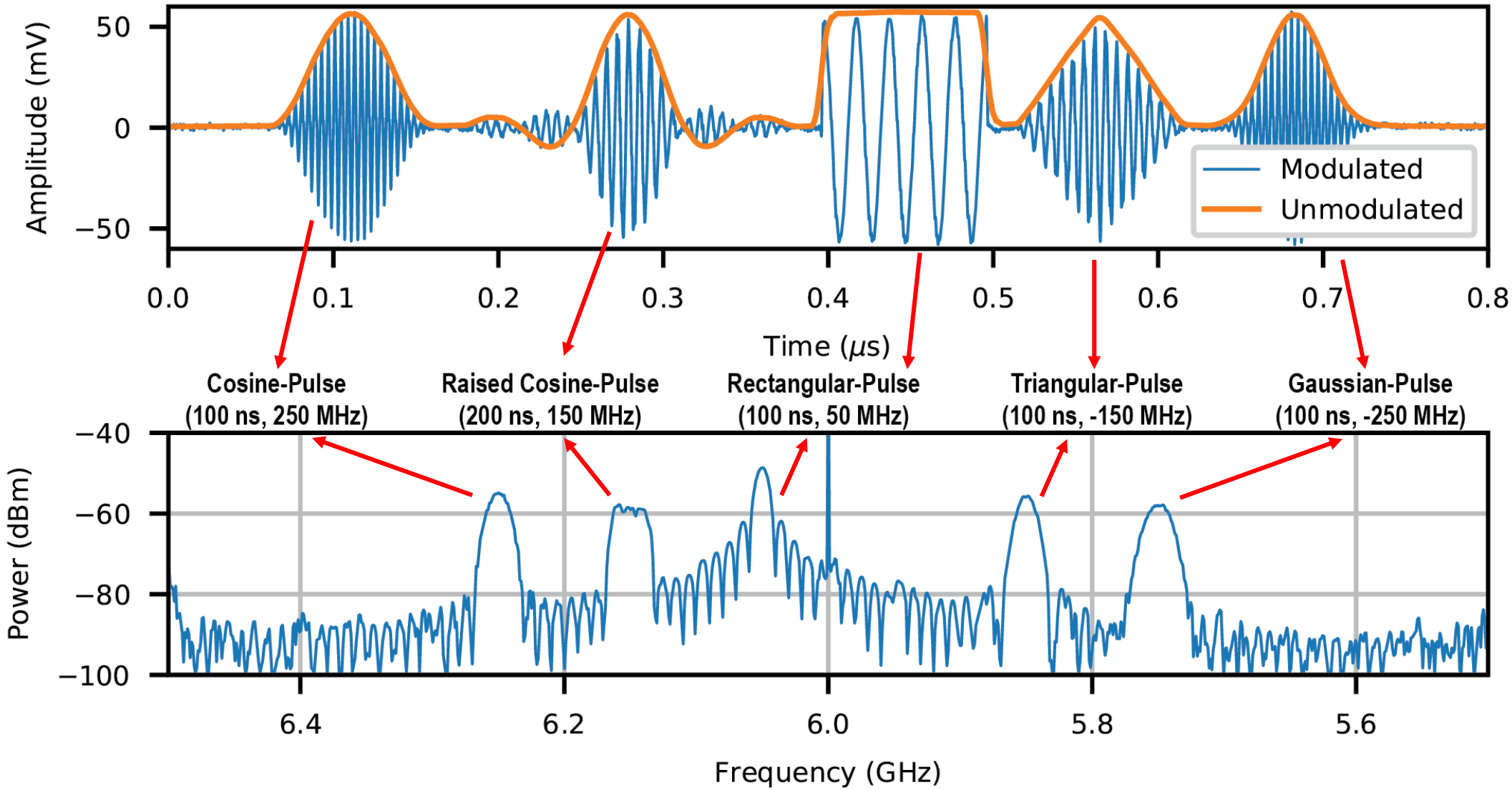
SFDR > 44 dB

SNR > 48 dB



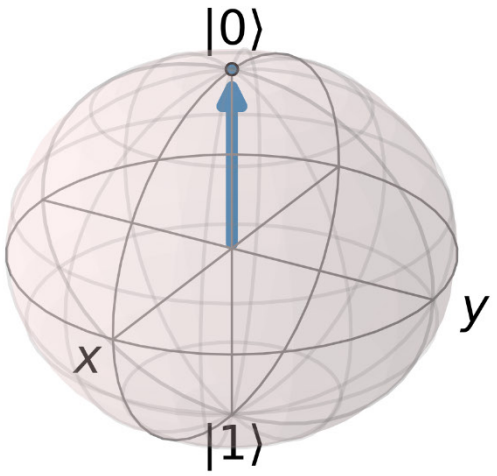


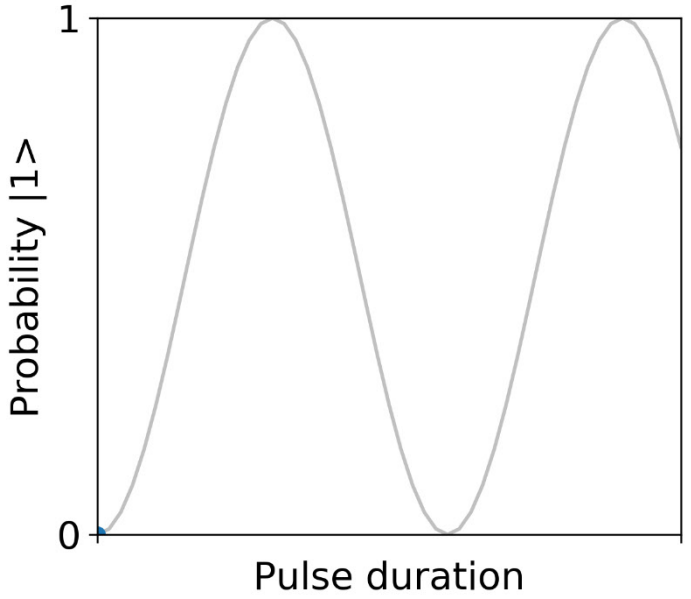
Pulse shaping



Rabi Experiment

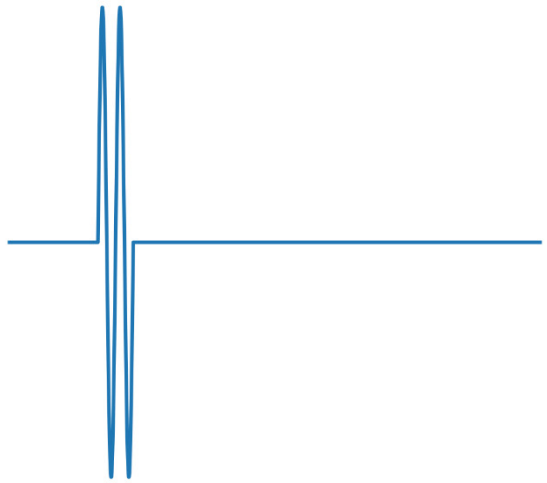
- Increase pulse duration in steps

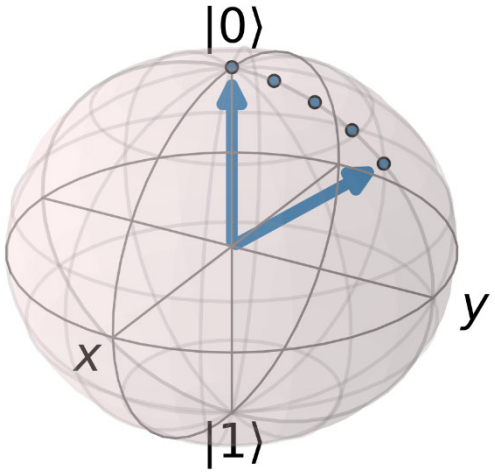


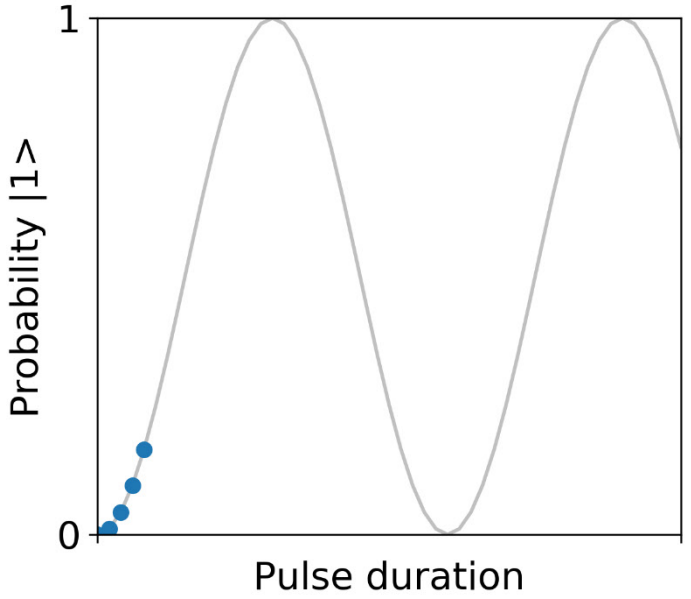


Rabi Experiment

- Increase pulse duration in steps

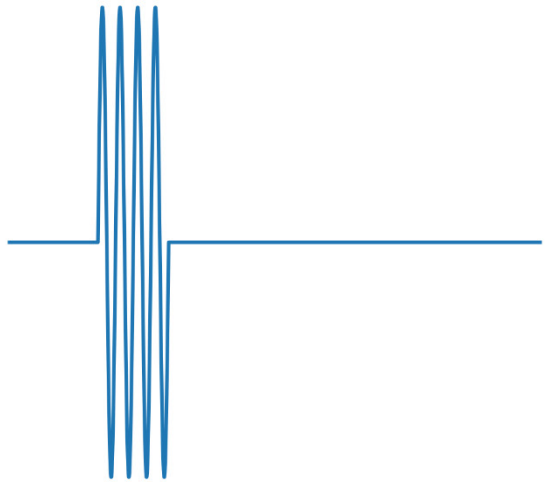


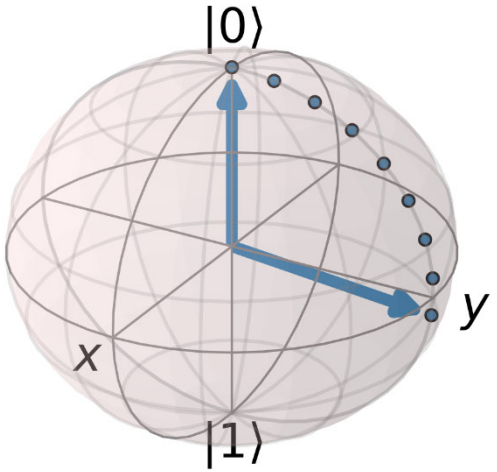


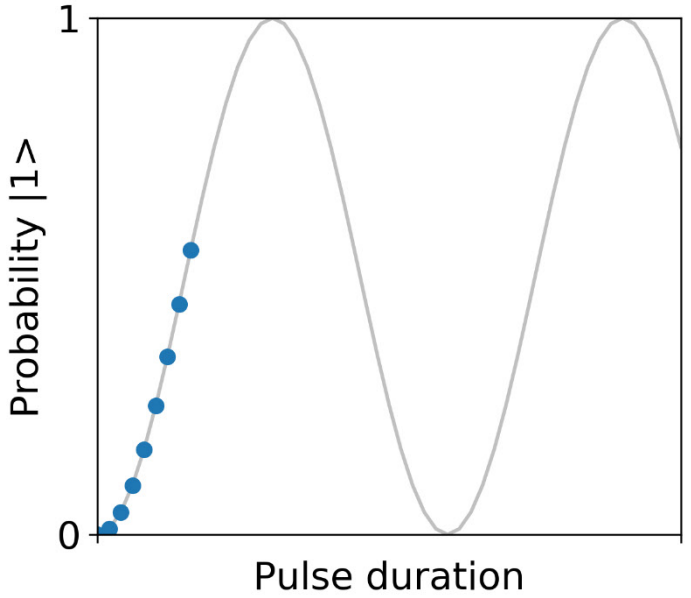


Rabi Experiment

- Increase pulse duration in steps

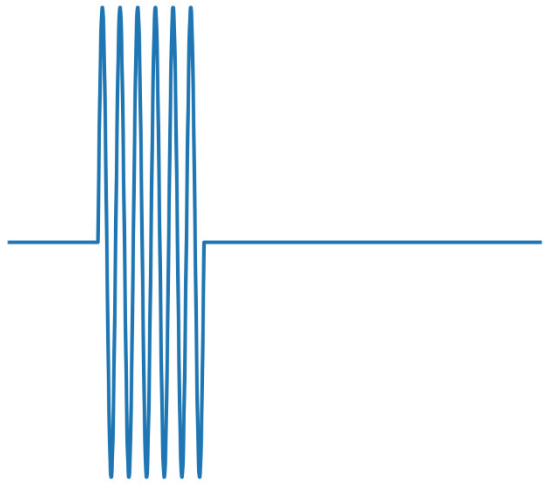


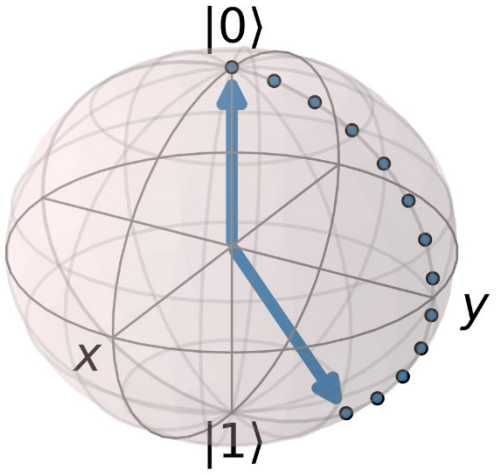


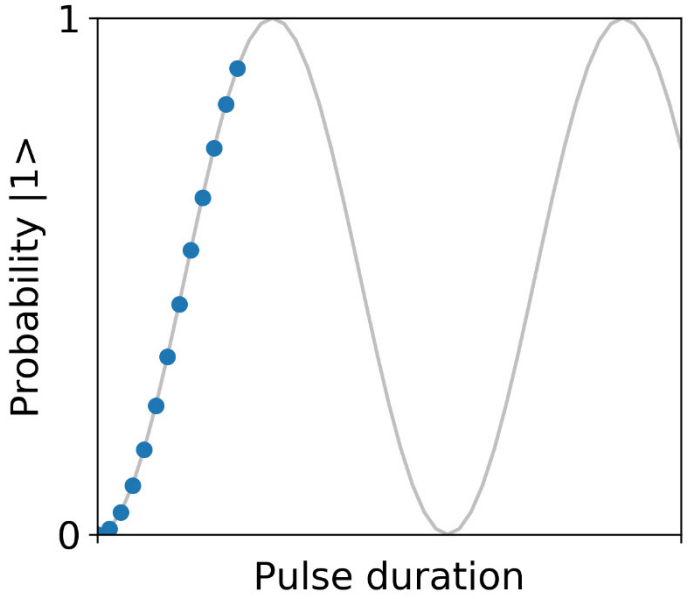


Rabi Experiment

- Increase pulse duration in steps

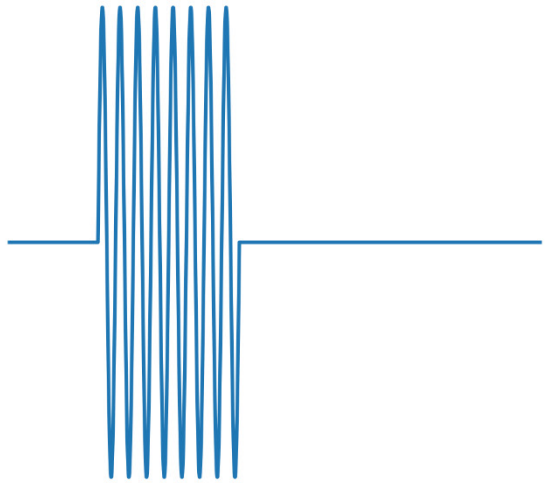


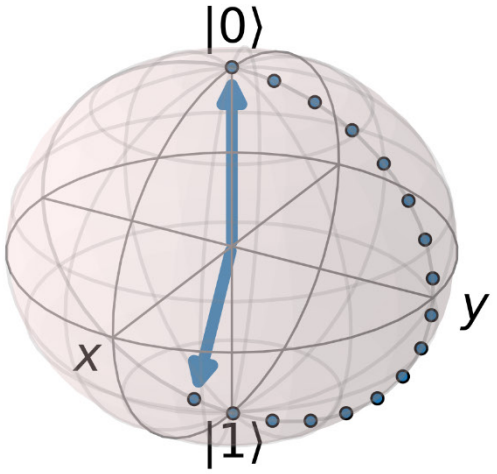


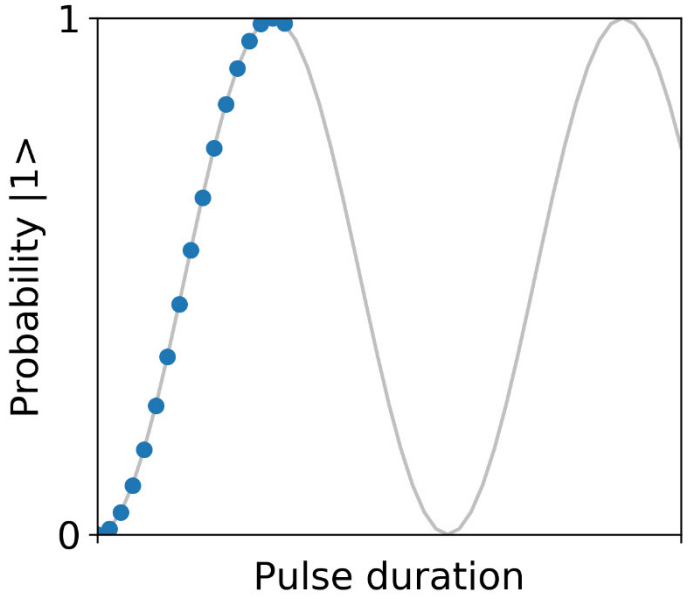


Rabi Experiment

- Increase pulse duration in steps

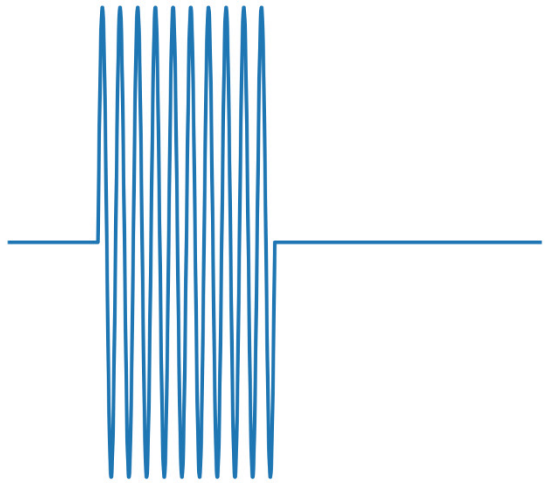


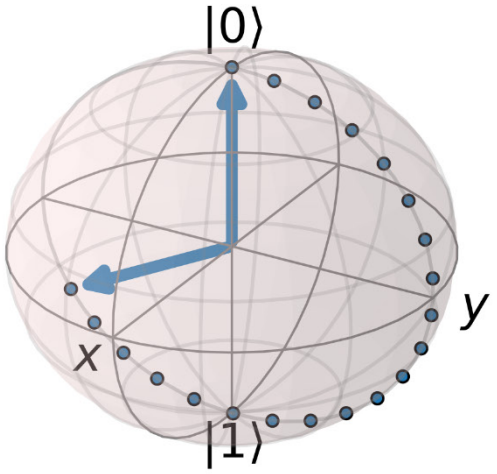


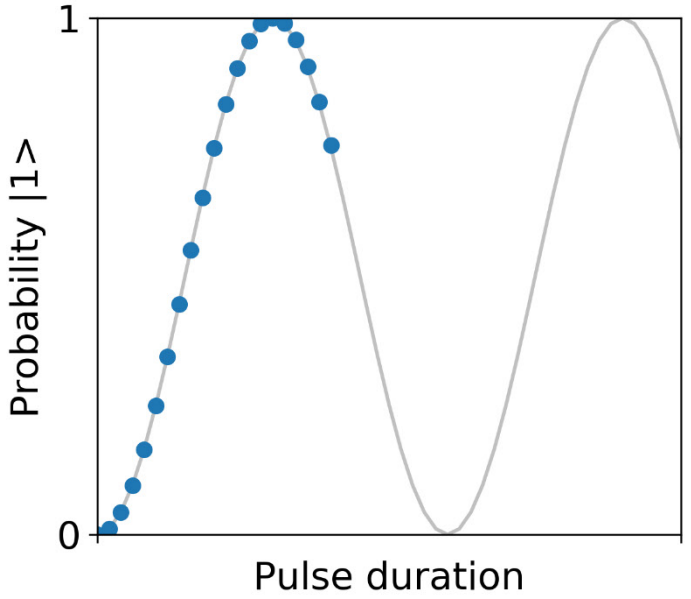


Rabi Experiment

- Increase pulse duration in steps

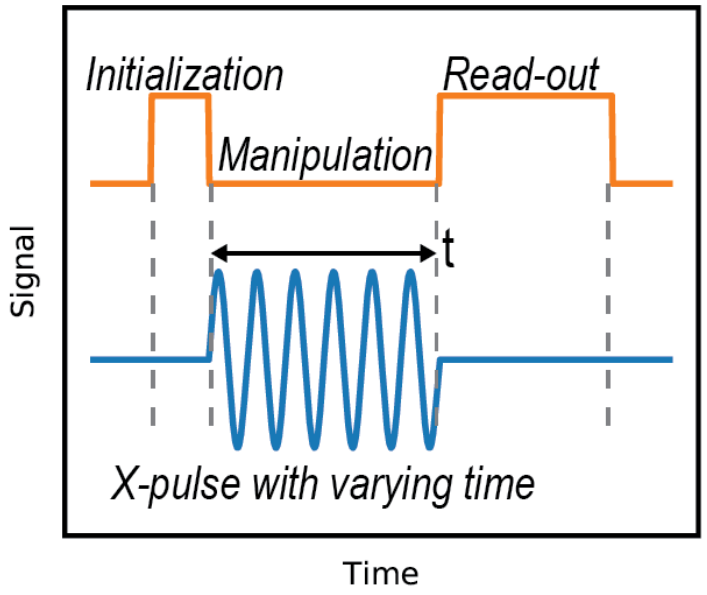


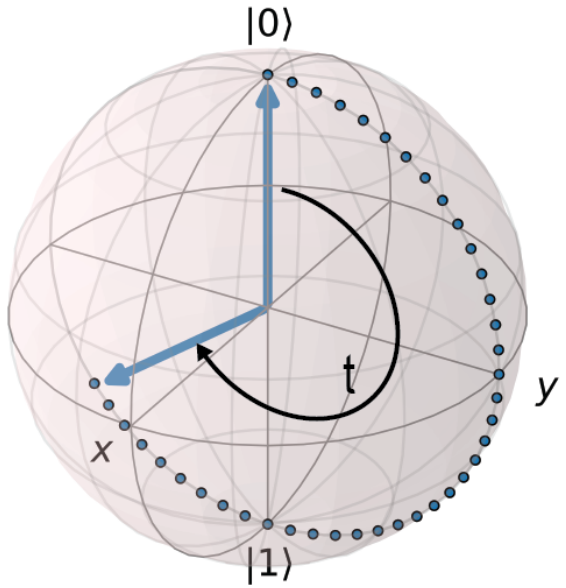


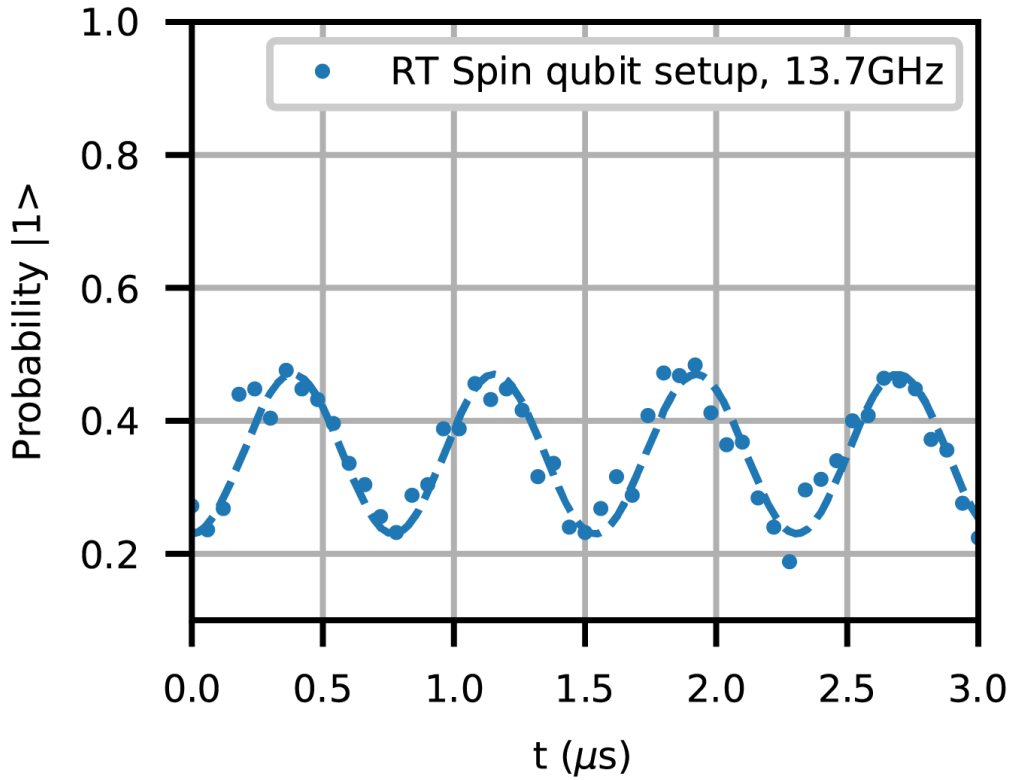


Rabi Experiment @ 13.7 GHz

- Increase pulse duration in steps

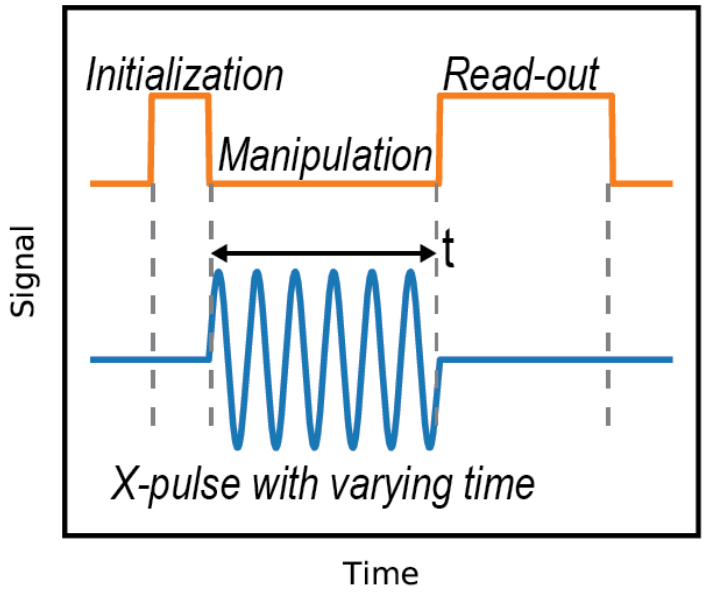


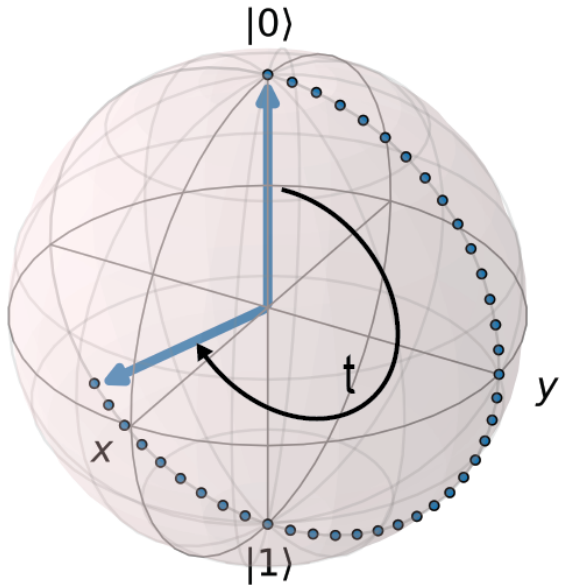


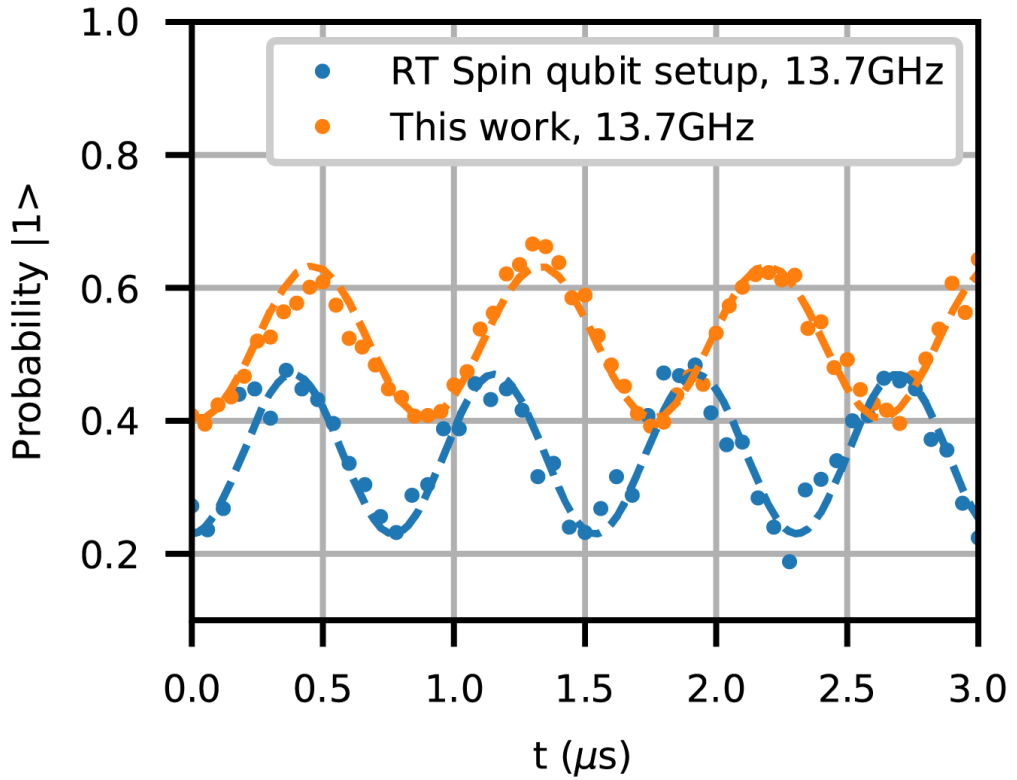


Rabi Experiment @ 13.7 GHz

- Increase pulse duration in steps

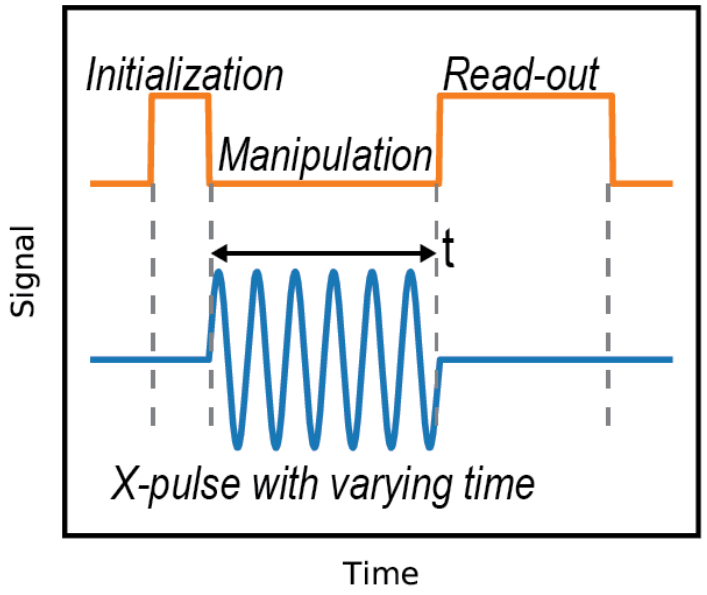


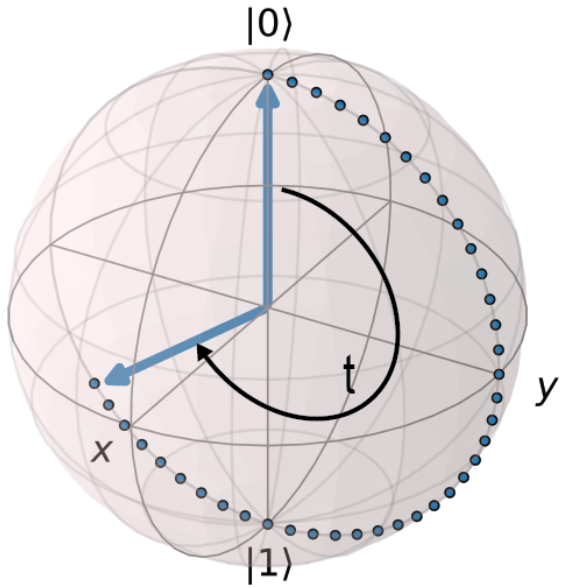


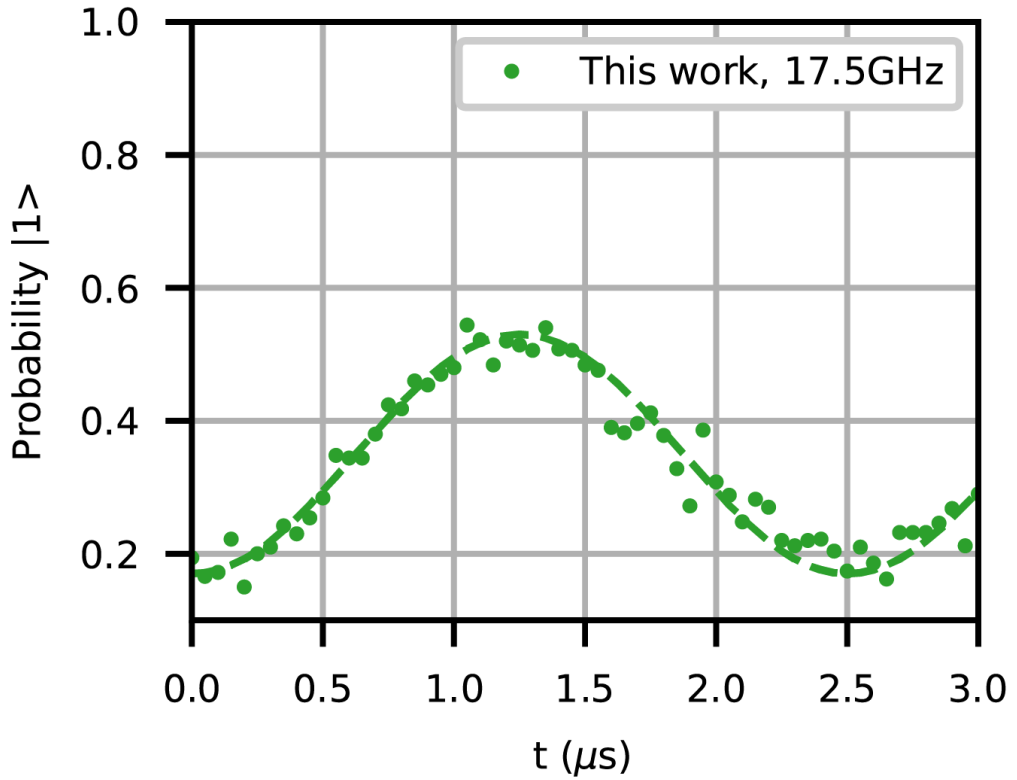


Rabi Experiment @ 17.5 GHz

- Increase pulse duration in steps

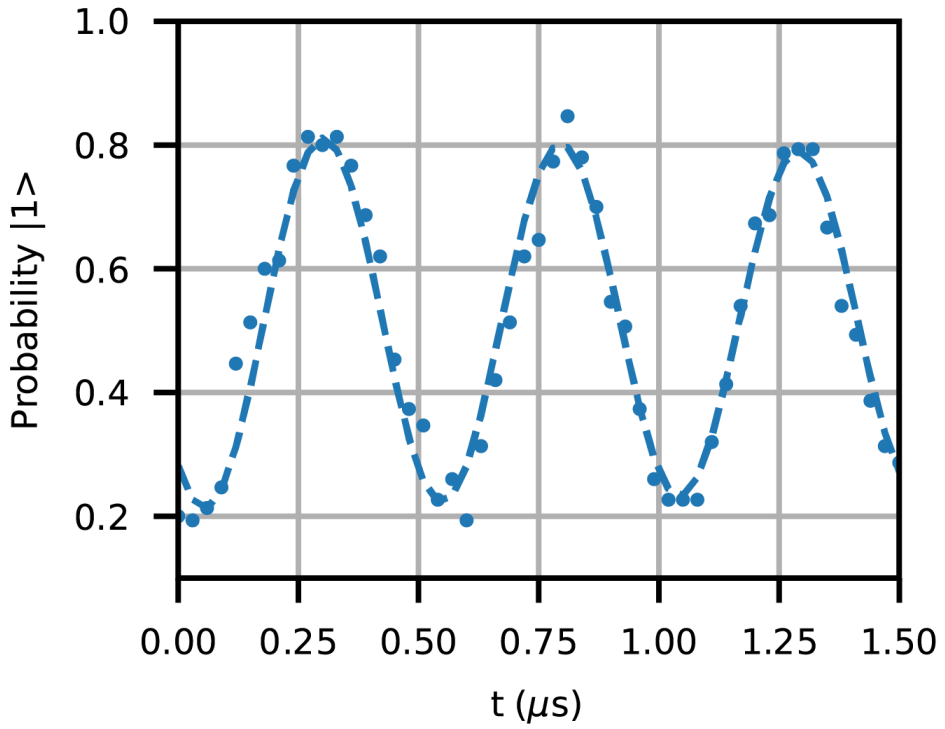




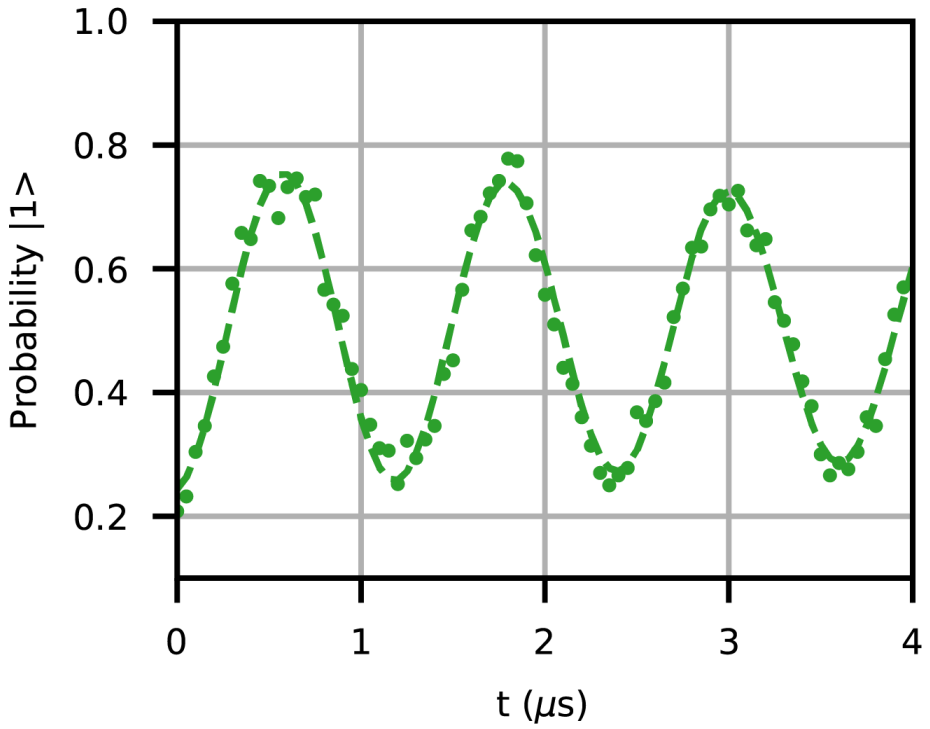


Improved Readout @ 13.4 GHz

Room temperature instrument

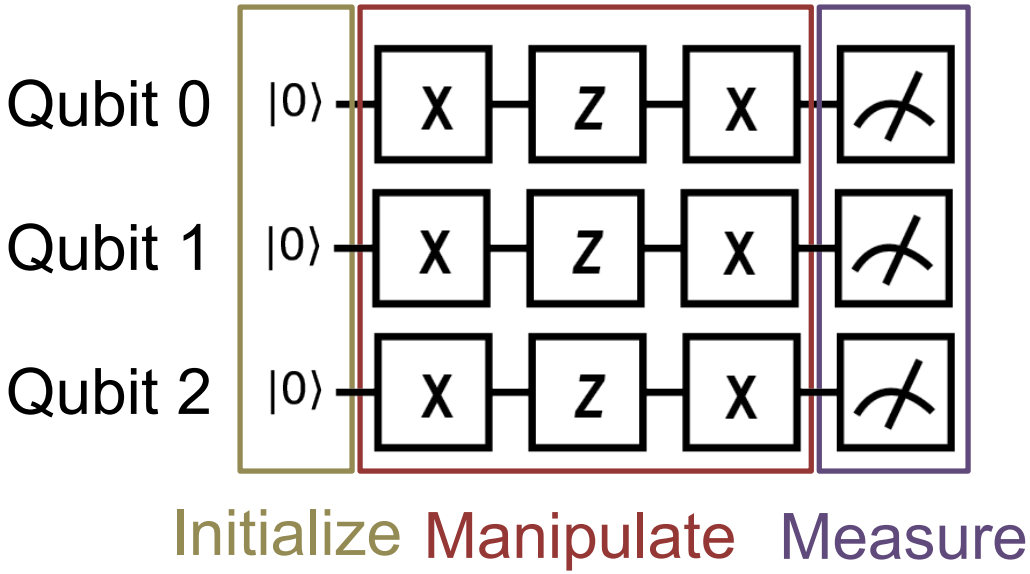


This work



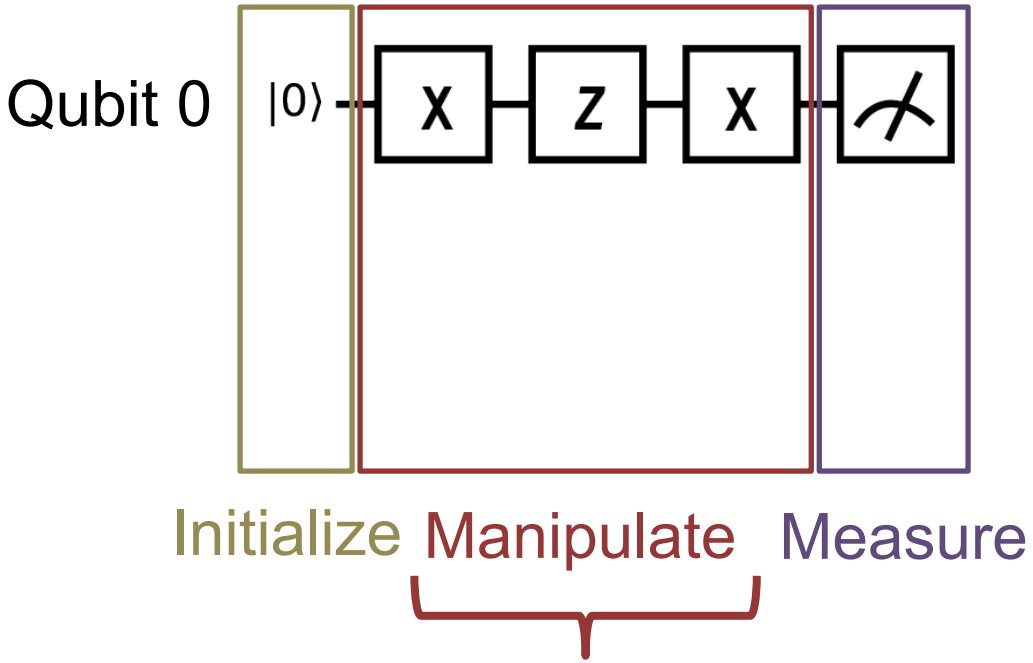
Quantum algorithm execution

- Typical quantum algorithm



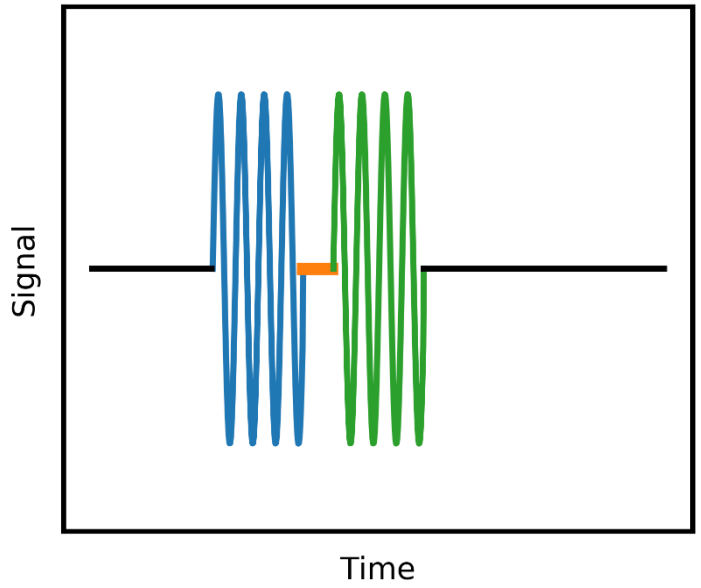
Quantum algorithm execution

- Typical quantum algorithm



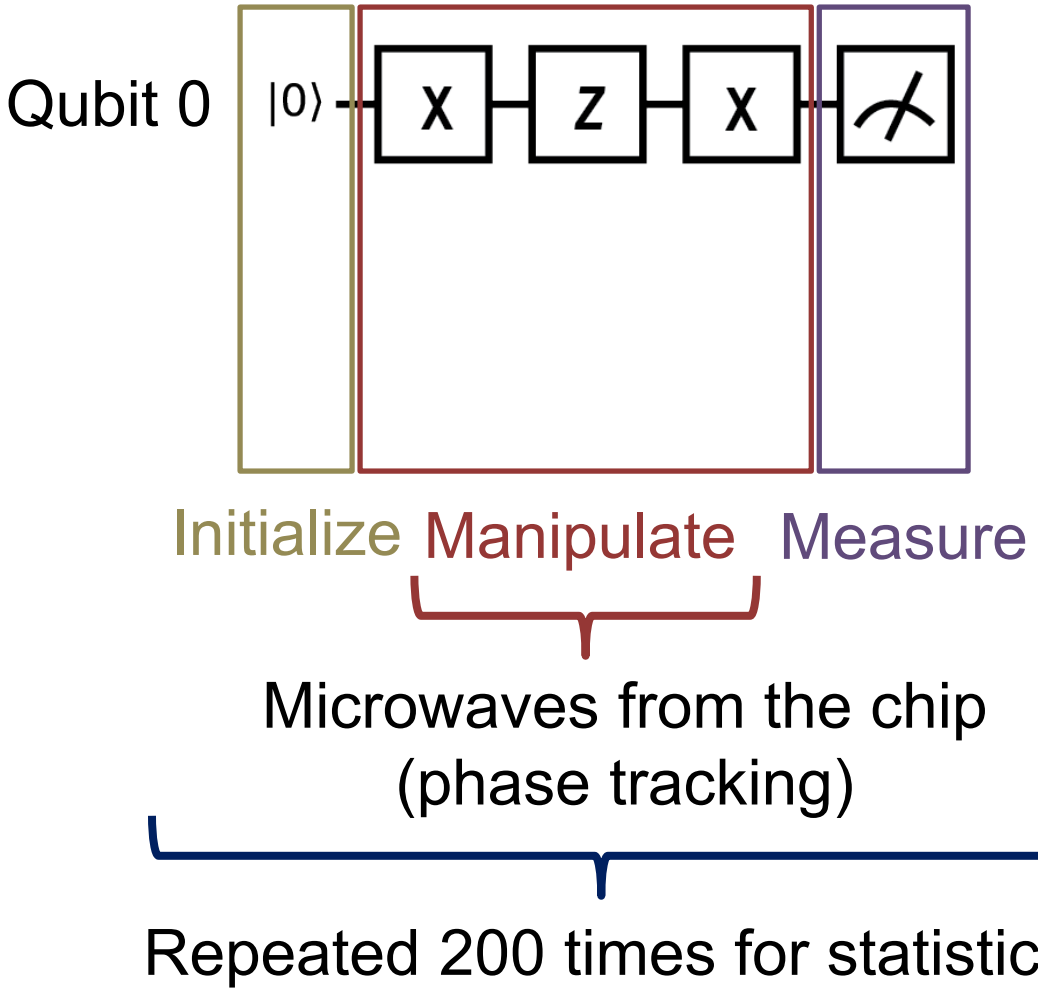
Microwaves from the chip
(phase tracking)

$R_X(\pi/2) \rightarrow R_Z(\theta) \rightarrow R_X(\pi/2)$

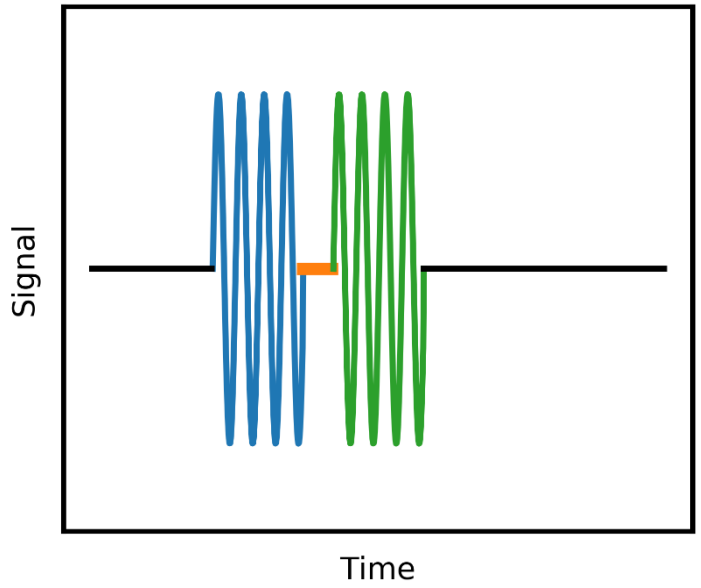


Quantum algorithm execution

- Typical quantum algorithm



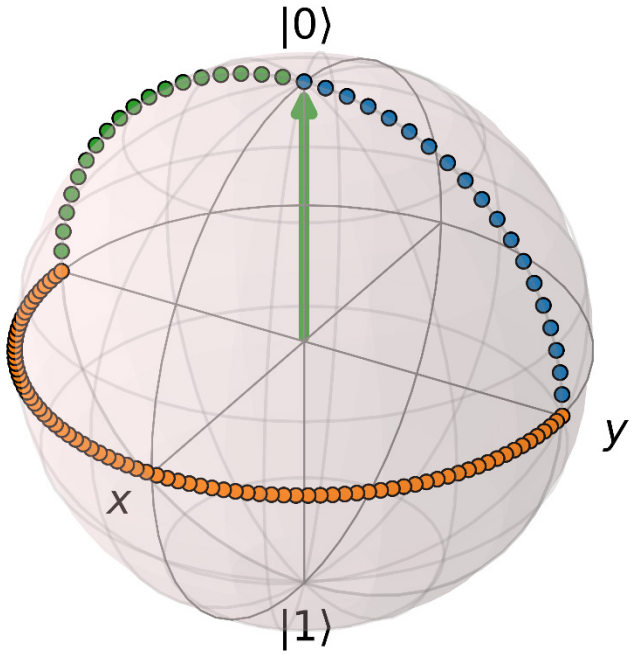
$R_X(\pi/2) \rightarrow R_Z(\theta) \rightarrow R_X(\pi/2)$

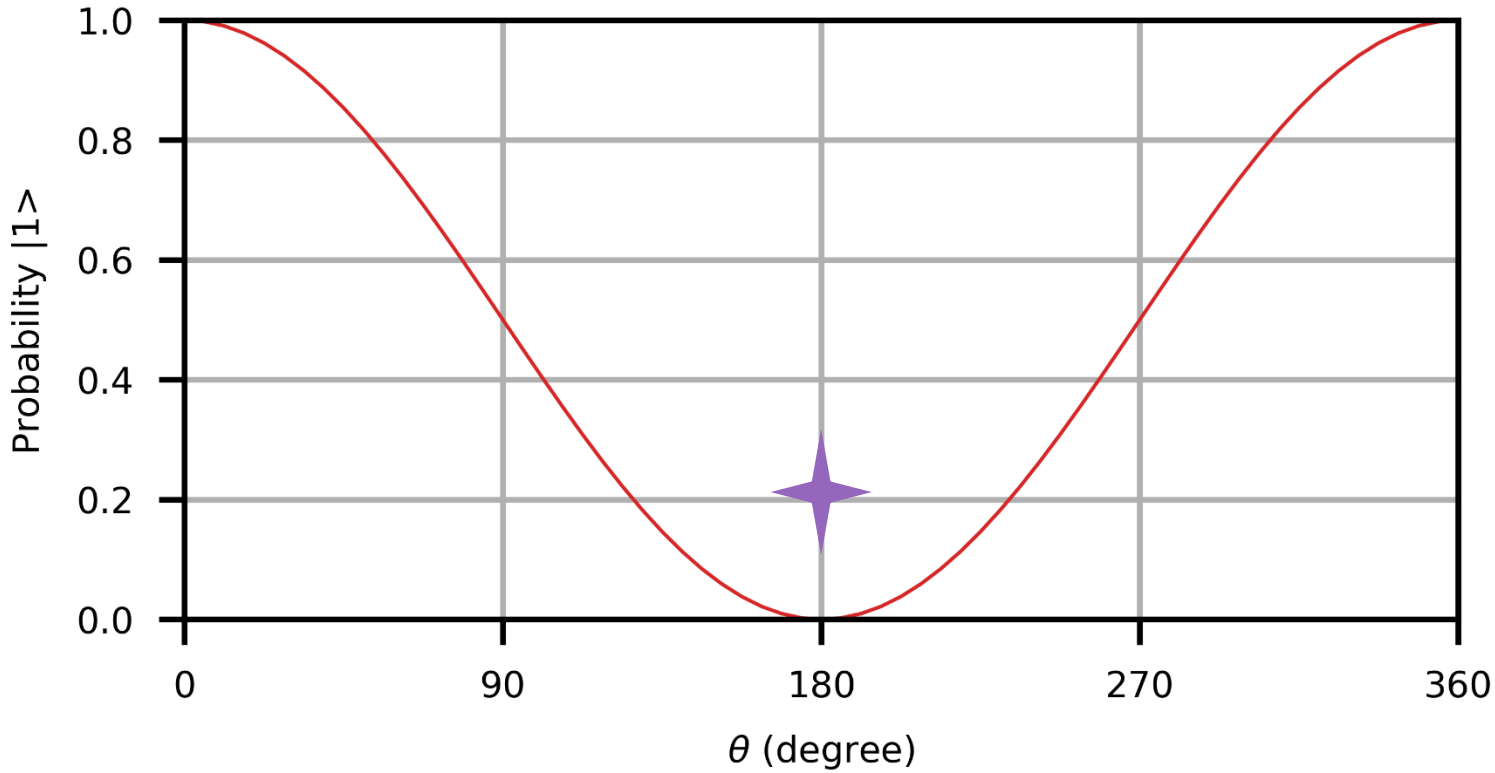


X/θ Experiment @ 13.4 GHz

$\theta = 180^0$

$R_X(\pi/2) \rightarrow R_Z(\theta) \rightarrow R_X(\pi/2)$

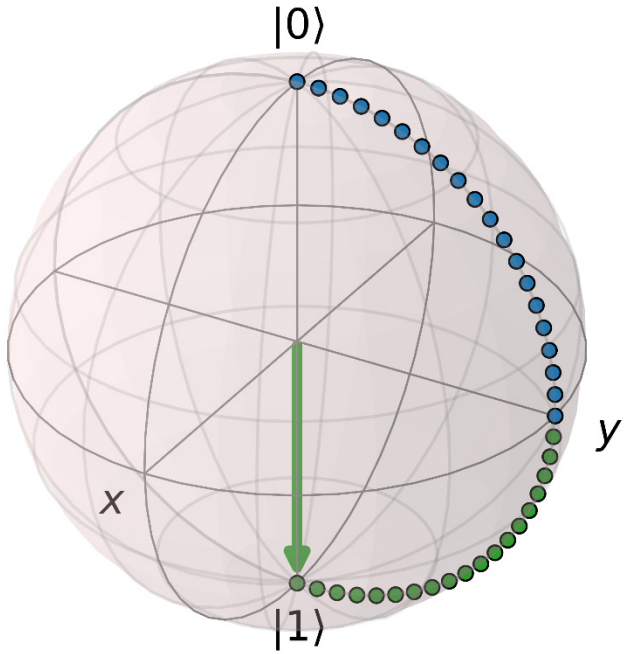




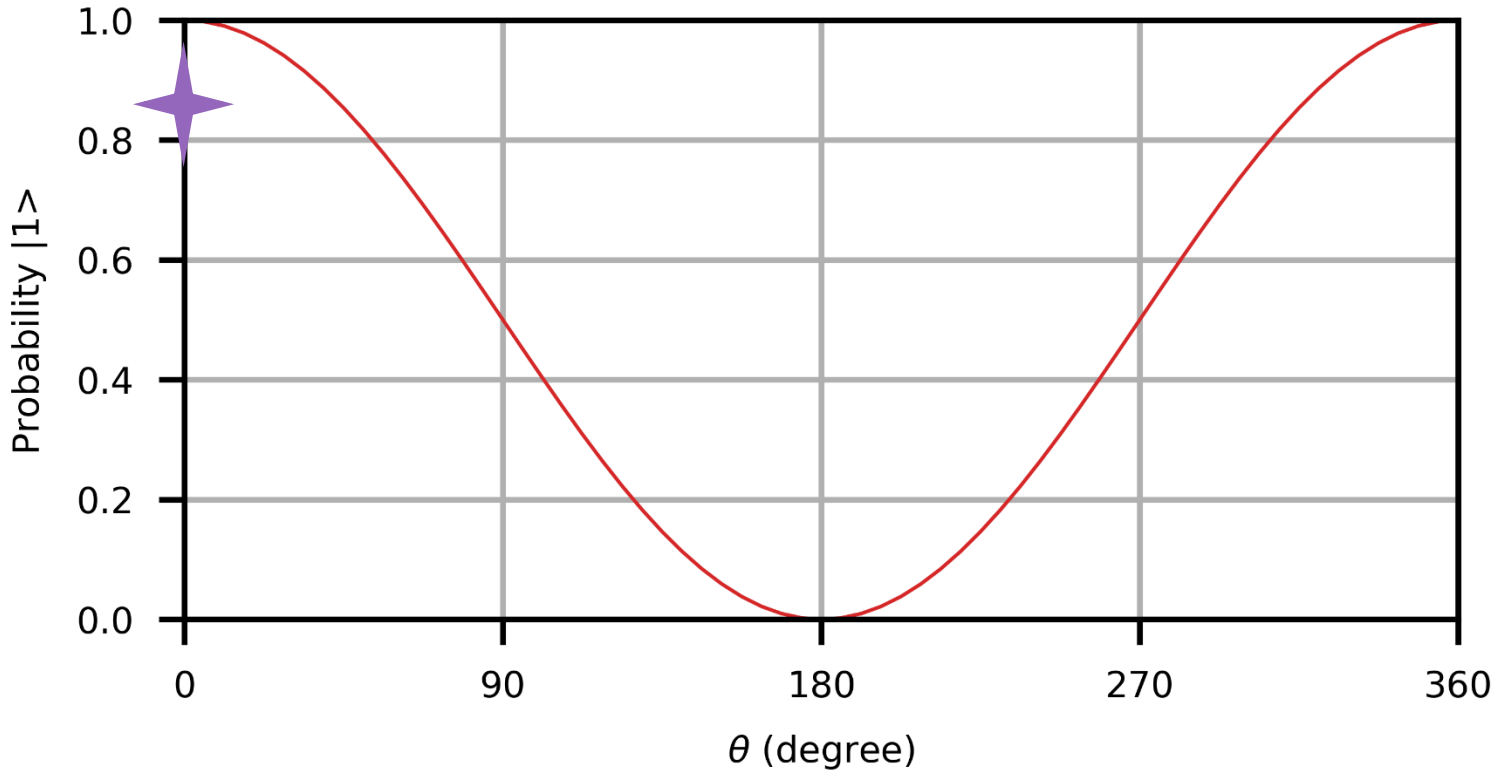
X/θ Experiment @ 13.4 GHz

$\theta = 0^0$

$R_X(\pi/2) \rightarrow R_Z(\theta) \rightarrow R_X(\pi/2)$



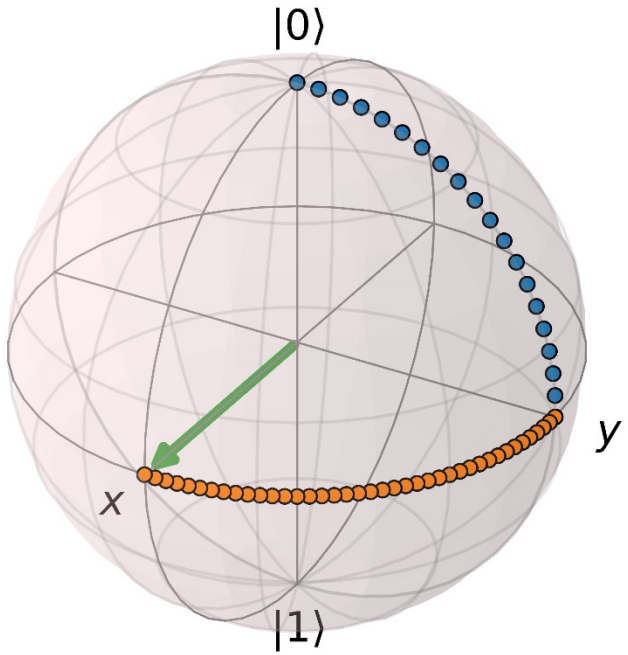
$\theta = 0^0$

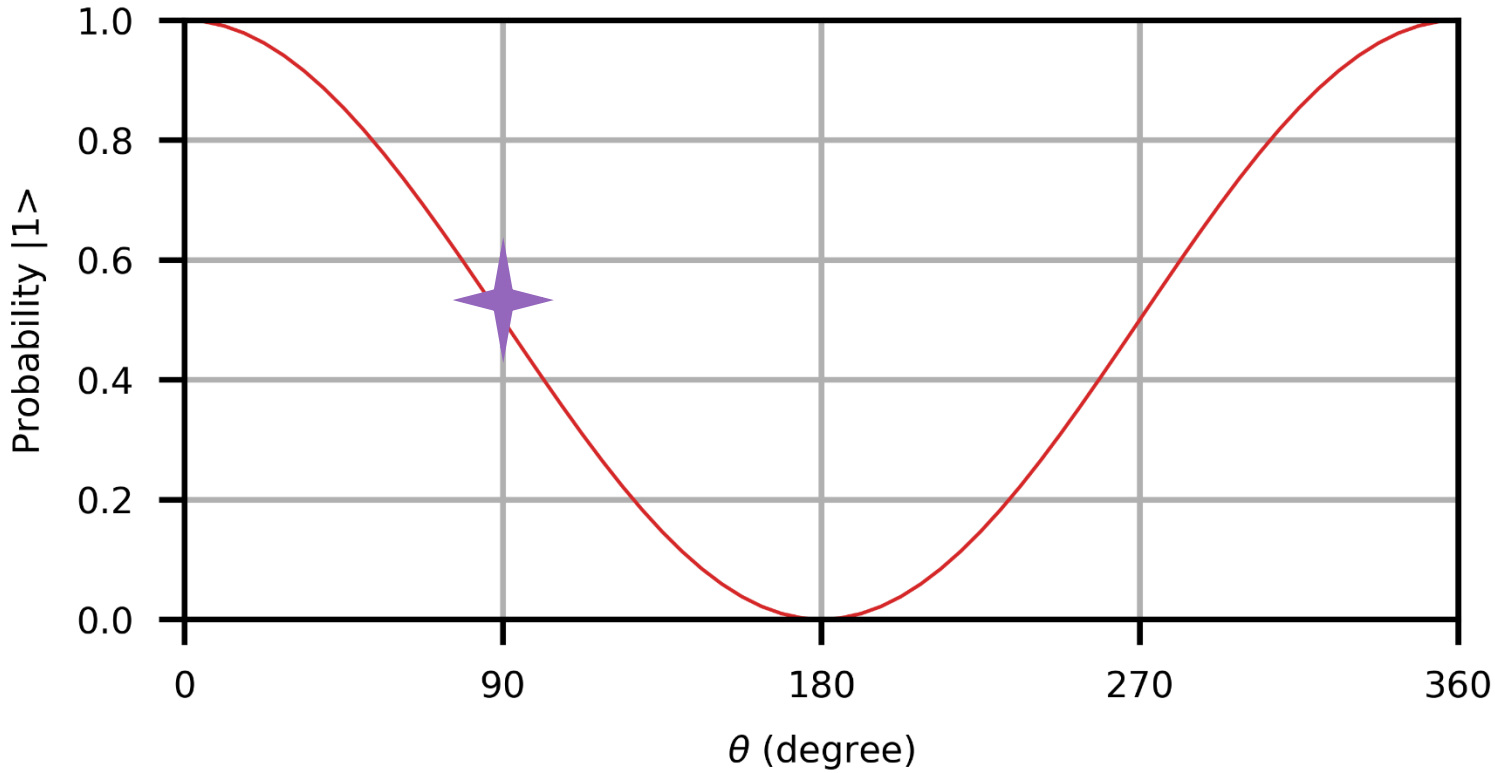


X/θ Experiment @ 13.4 GHz

$\theta = 90^0$

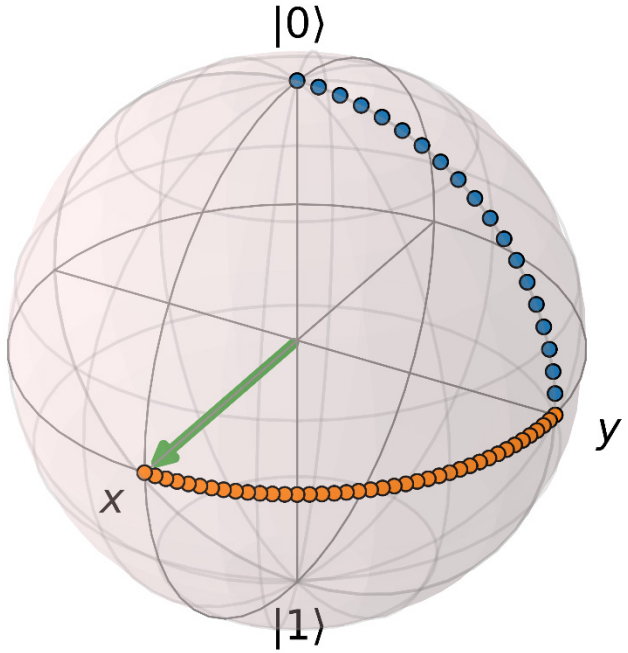
$R_X(\pi/2) \rightarrow R_Z(\theta) \rightarrow R_X(\pi/2)$

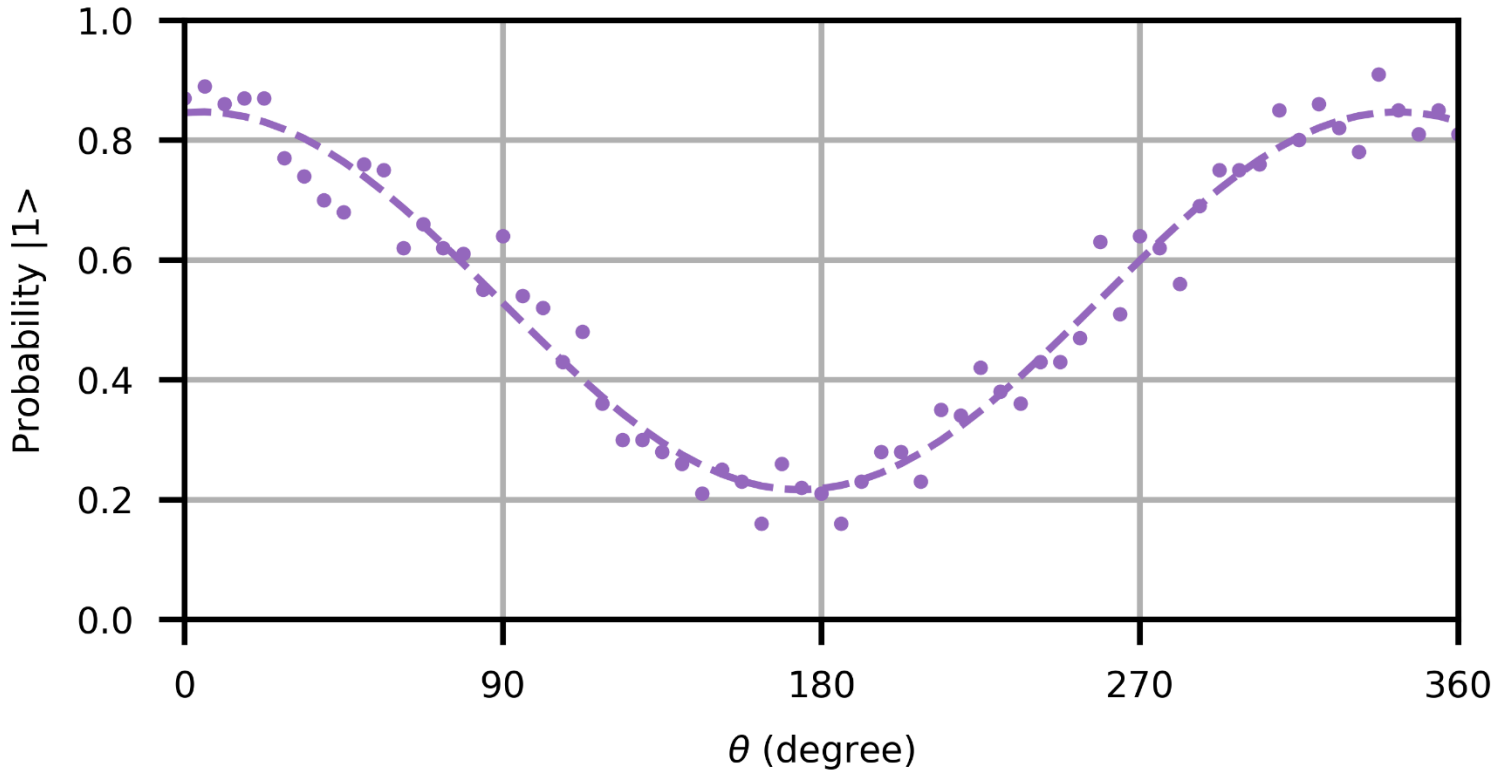




X/θ Experiment @ 13.4 GHz

$R_X(\pi/2) \rightarrow R_Z(\theta) \rightarrow R_X(\pi/2)$





Comparison Table

	This work	ISSCC'19	RSI'17	Spin qubit setup
Operating Temperature	3 K	3 K	300 K	300 K
Qubit platform	**Spin qubits + Transmons**	Transmons	Transmons	Spin qubits
Qubit frequency	**2 – 20 GHz**	4 – 8 GHz		< 20 GHz
Channels	**128 (32 per TX)**	1	4	1
FDMA	**Yes, SSB**	No	Yes, SSB	No
Data Bandwidth	1 GHz	400 MHz	960 MHz	520 MHz
Image & LO leakage calibration	**On chip**	Off chip	Yes	
Phase correction	**Yes**	No	No	No
Fidelity (expected)	**99.99%**	-	-	-
Waveform/Instructions	**Upto 40960 pts AWG**	Fixed 22 pts symmetric		16M pts AWG
Instruction set	**Yes**	No	Yes	Yes
Power / TX	Analog: 1.7 mW/qubit * Digital: 330 mW ‡	Analog < 2 mW/qubit # Digital: N/A		850 W
Chip area / TX	4 mm^2	1.6 mm^2	Discrete components	Rack mount
Technology	22 nm FinFET CMOS	28 nm bulk CMOS		

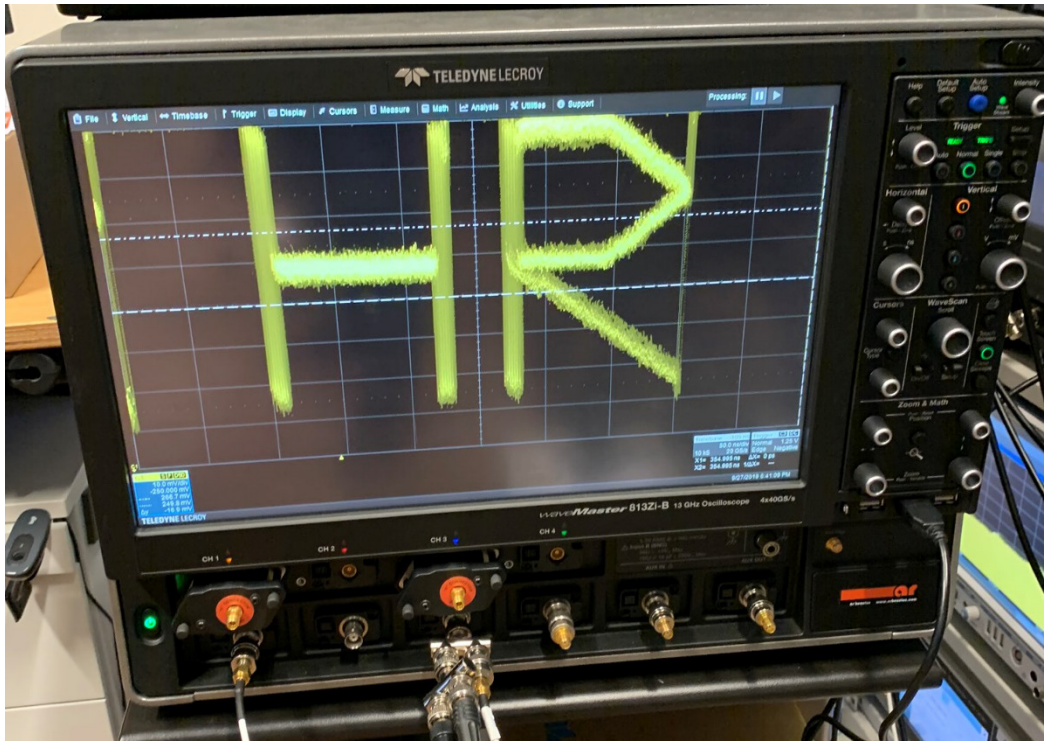
* including LO/Clock driver; only RF-Low active
# does not mention circuits included
‡ can be reduced with clock gating

Conclusions

- Controller for large scale quantum computer
  - ✔ Cryogenic operation
  - ✔ Integrated digital controller
  - ✔ High performance RF signals
  - ✔ Power-efficient architecture
- Most complex cryogenic SoC ever built
  - – Algorithm → microwave signals for qubits
- Enables large scale quantum computing
  - – For a *higher fidelity* (99.99%) than state-of-the-art qubits
  - – Supports *more qubits* (128) than the largest quantum processor

Acknowledgements

- TU Delft: Z. Y. Chang, O. Benningshof, M. Sarsby, N. Alberts, T. Alkemade, B. Bakker, H. Homulle, CoolGroup
- Intel: M. Fredette, C. Le, C. Paulino, R. Lee, R. Mckee, C. Hull, J. Clarke, J. Held, S. Kale, J. Feng, M. Chakravorti, R. Stingel, T. Prabhakaran, J. Lim, S. Suzuki, D. Vemparala, D. Souza, L. Lampert, J. Park, U. Jalan

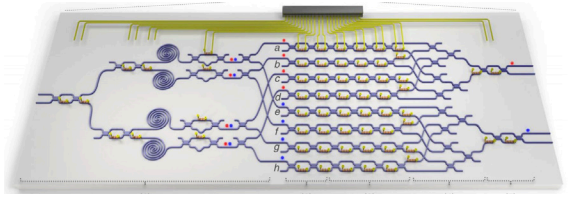
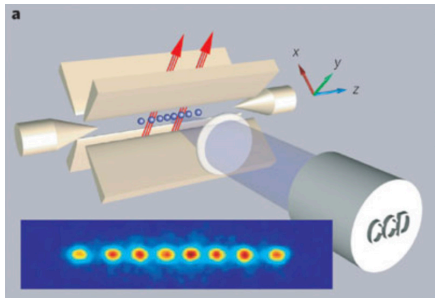
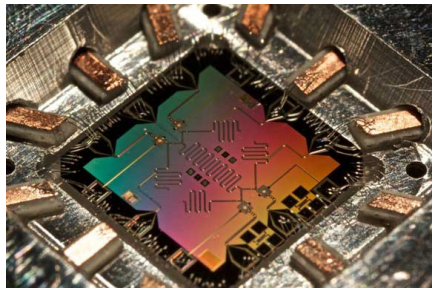
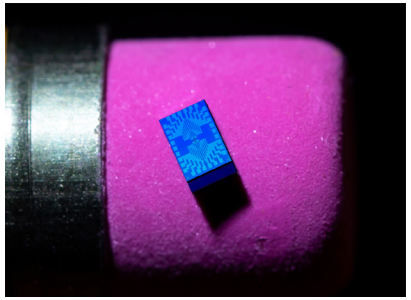


A 110mK 295µW 28nm FDSOI CMOS Quantum Integrated Circuit with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot

Loïck Le Guevel[1,2], Gérard Billiot[1], Xavier Jehl[2], Silvano De Franceschi[2], Marcos Zurita[1], Yvain Thonnart[1], Maud Vinet[1], Marc Sanquer[2], Romain Maurand[2], Aloysius G.M. Jansen[2], Gaël Pillonnet[1]

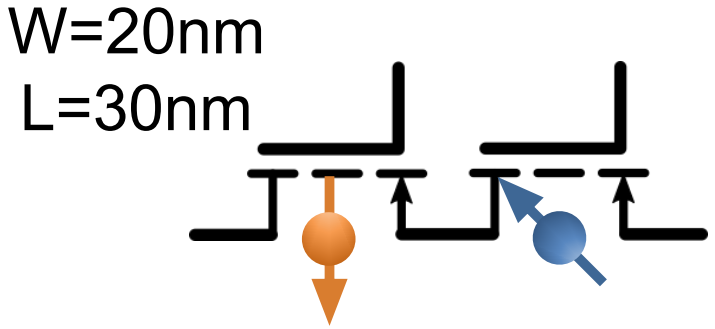
[1]CEA-LETI-MINATEC, Grenoble, France
[2]CEA-IRIG, Grenoble, France

Quantum Processor Technologies

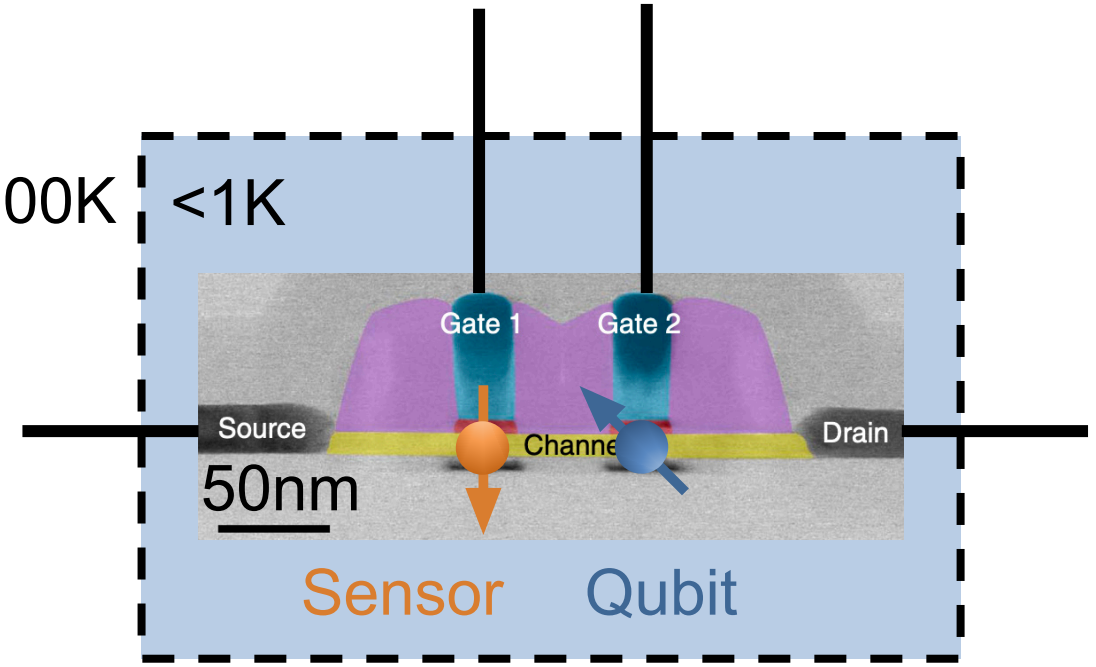
T. Meunier et al. (2019)	 **Photons**	 **Ion Traps**	 **Superconducting Qubits**	 **Semiconductor Qubits**
Fidelity	98%	**99.99%**	99.9%	99.7%
Temperature	**300 K**	**300 K**	0.01 K	0.1 – 1 K
Speed	1ms	100µs	**200ns**	1µs
Variability	0.5%	**0.01%**	3%	0.1-0.5%
Area/qubit	1mm^2	1mm^2	(100µm)^2	**(100nm)^2**
Qubits/mm^2	1	1	10^2	**10^8**

Leveraging the Silicon industry know-how

Silicon nanowire MOSFET
spin qubit on an industrial 300mm wafer



Schematic view of the CMOS spin qubit



R. Maurand et al. (2016)