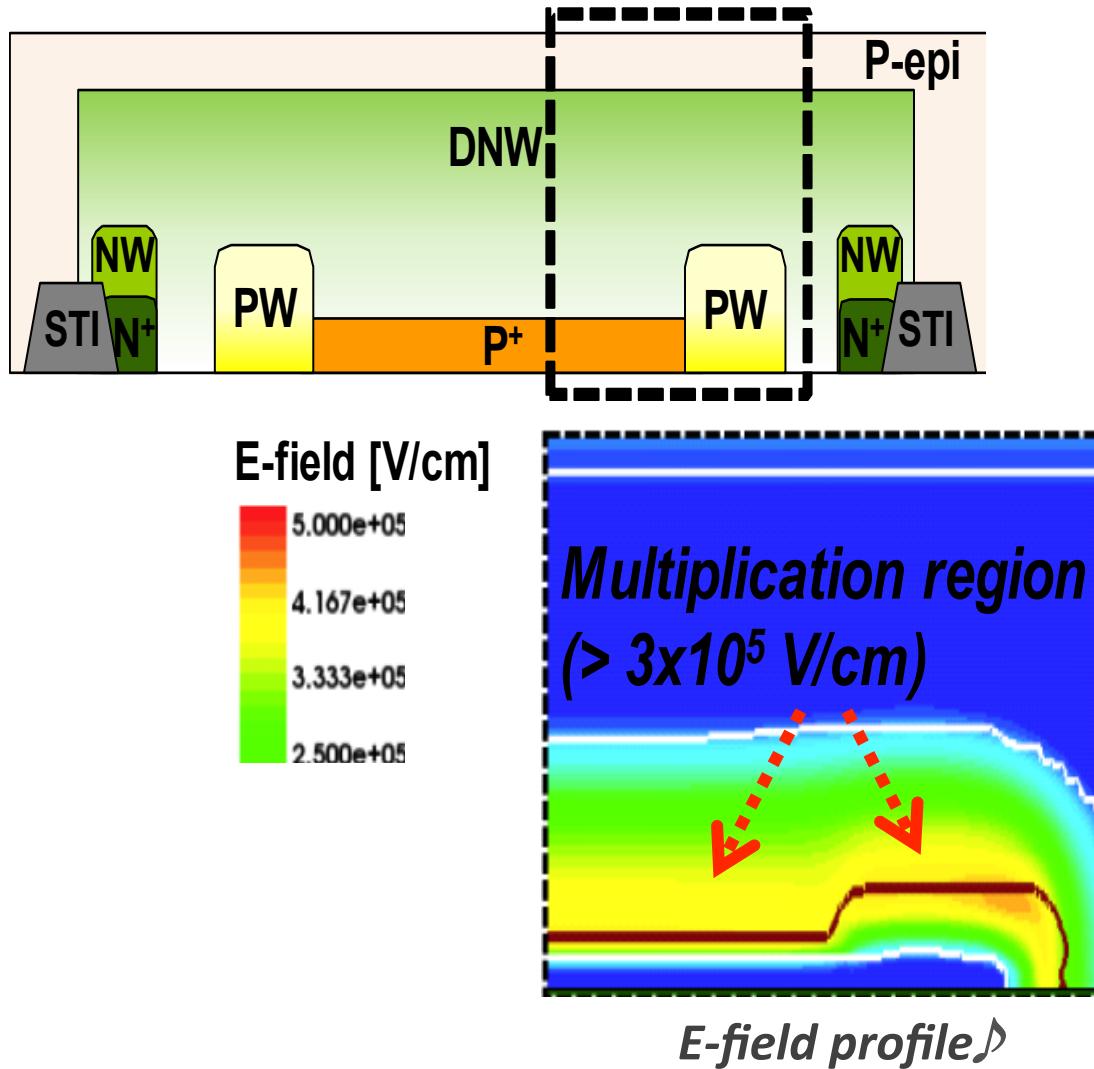
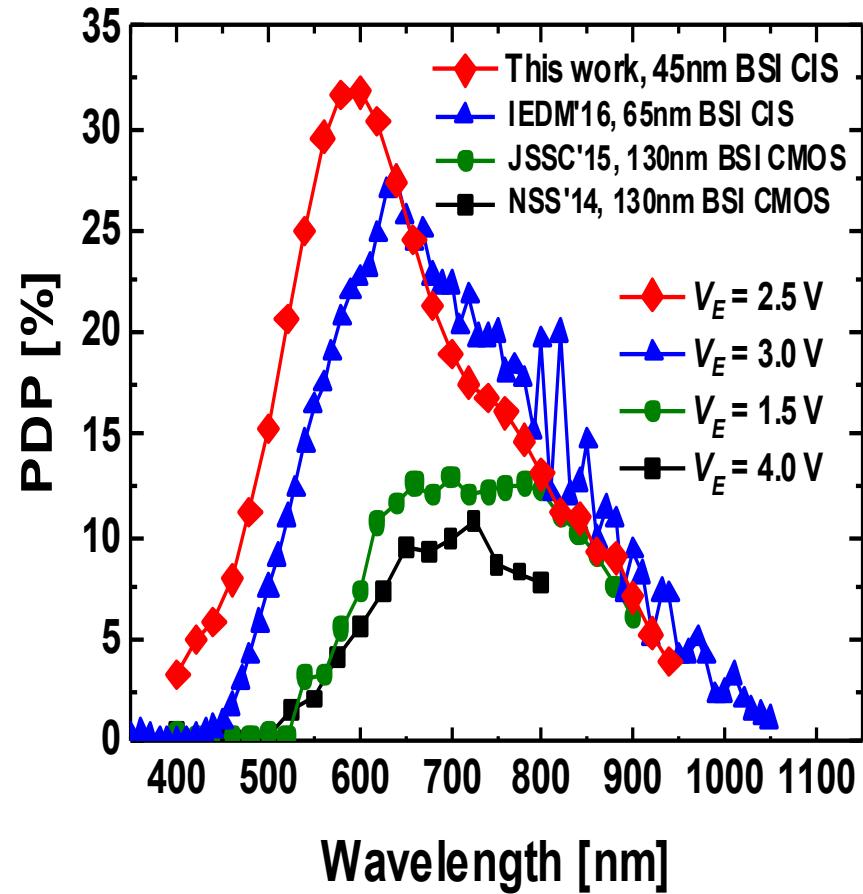
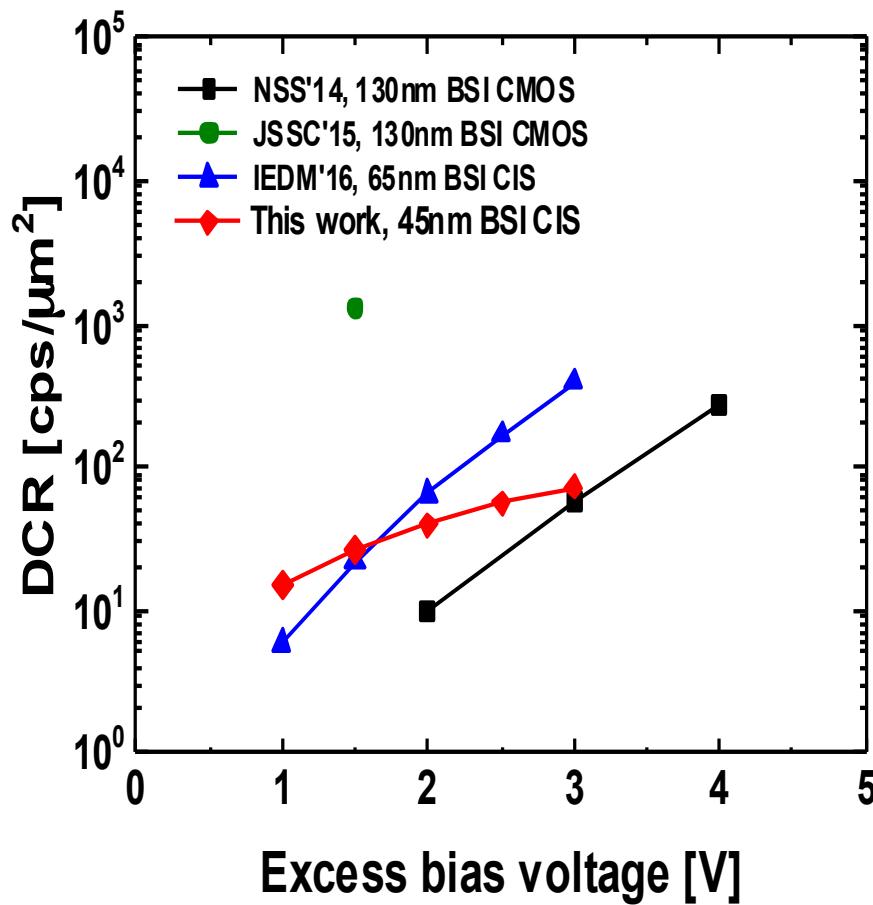


Electrical Microlenses

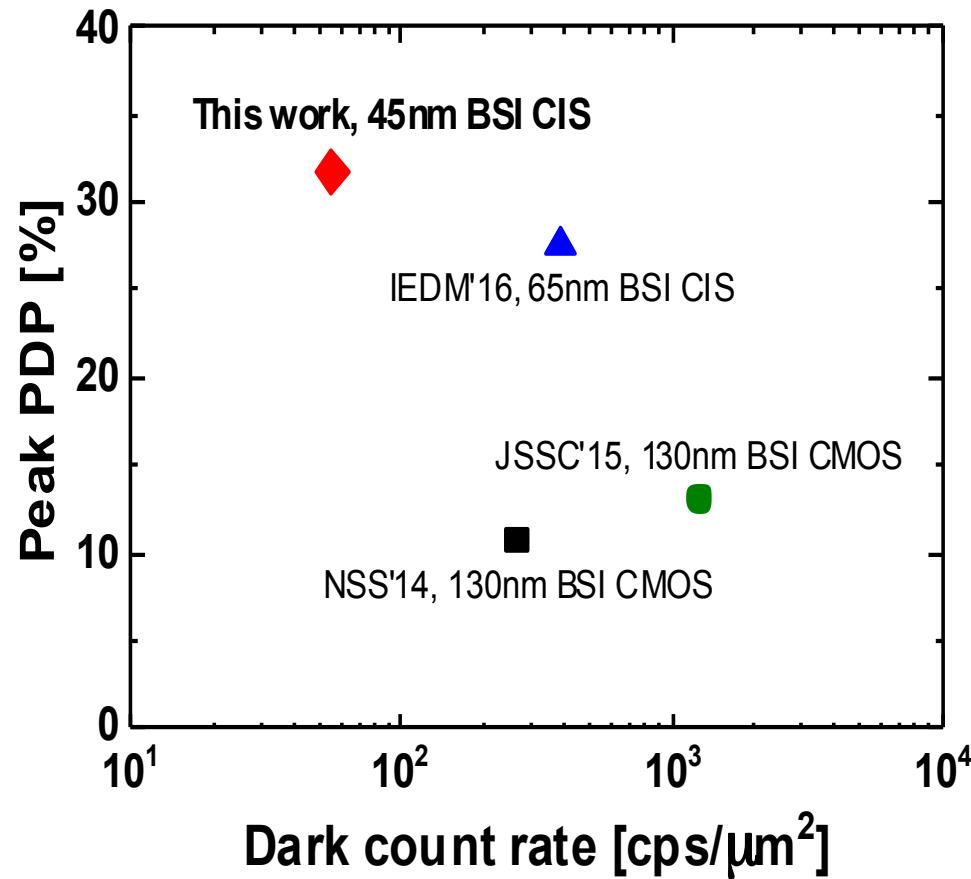


- Extended multiplication region below GR
→ Larger FF

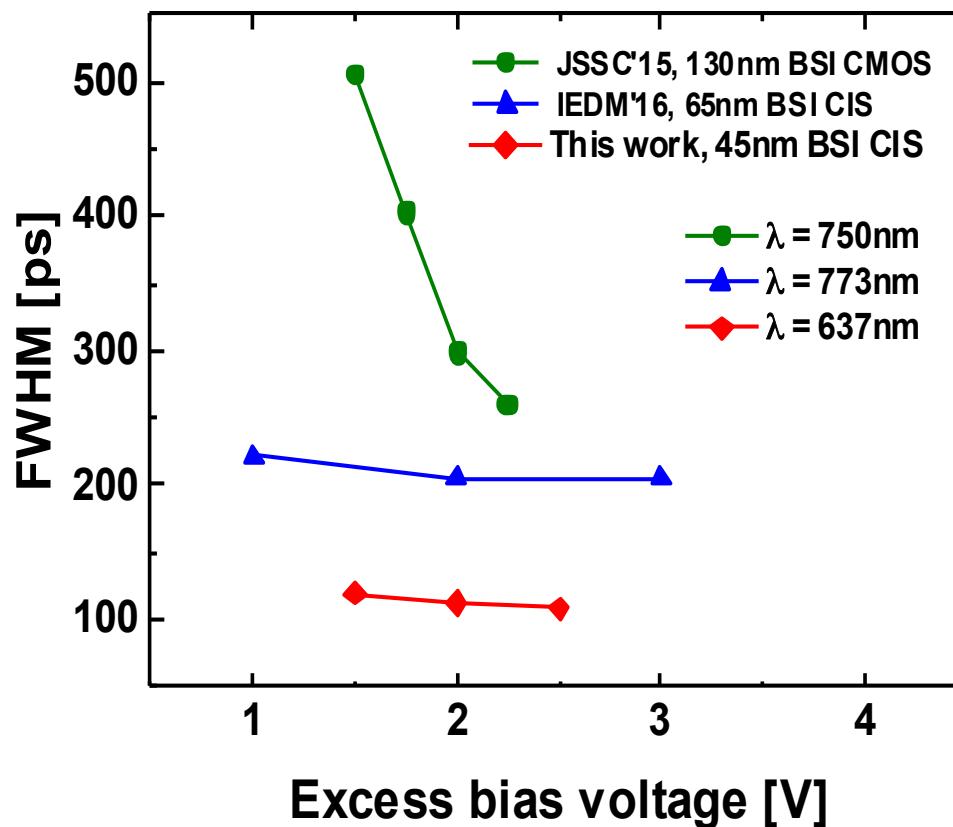
3D-Stacked BSI Comparison: DCR & PDP



3D-Stacked BSI Comparison: DCR & PDP



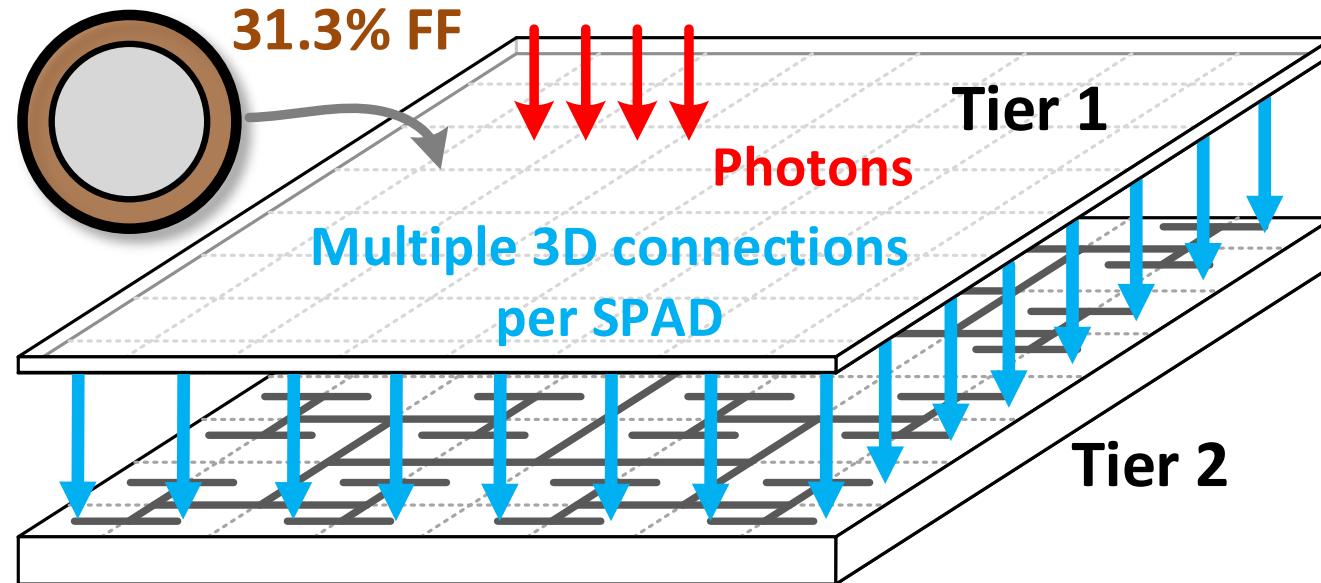
3D-Stacked BSI Comparison: Timing Jitter



3D-Stacked BSI State-of-the-art

	NSS'14	JSSC'15	IEDM'16	This work
Technology (Top/Bottom)	130nm CMOS 130nm CMOS	130nm CMOS 130nm CMOS	65nm CIS 40nm CMOS	45nm CIS 65nm CMOS
Junction GR	P ⁺ /NW PW GR	NLDD/PW NW GR	PW/DNW Virtual GR	P⁺/DNW PW GR
Active area	28.3 μm ²	28 μm ²	27.6 μm ²	122.7 μm²
Fill factor	n.a.	23.3 %	45 %	up to 60.5 %
V_B + V_E	12.3 V + 4 V	16.5 V + 1.5 V	12.0 V + 3 V	28.5 V + 2.5 V
DCR	7.5 kcps 265.3 cps/μm ²	35 kcps 1250 cps/μm ²	10.8 kcps 391.4 cps/μm ²	6.8 kcps 55.4 cps/μm²
PDP peak (@λ)	11 % (@725nm)	13 % (@700nm)	27.5 % (@640nm)	31.8 % (@600nm)
PDP @450nm	0.3 %	0.3 %	0.9 %	6.9 %
FWHM (@λ)	n.a.	505 ps (@750nm)	205 ps (@773nm)	107.7 ps (@637nm)

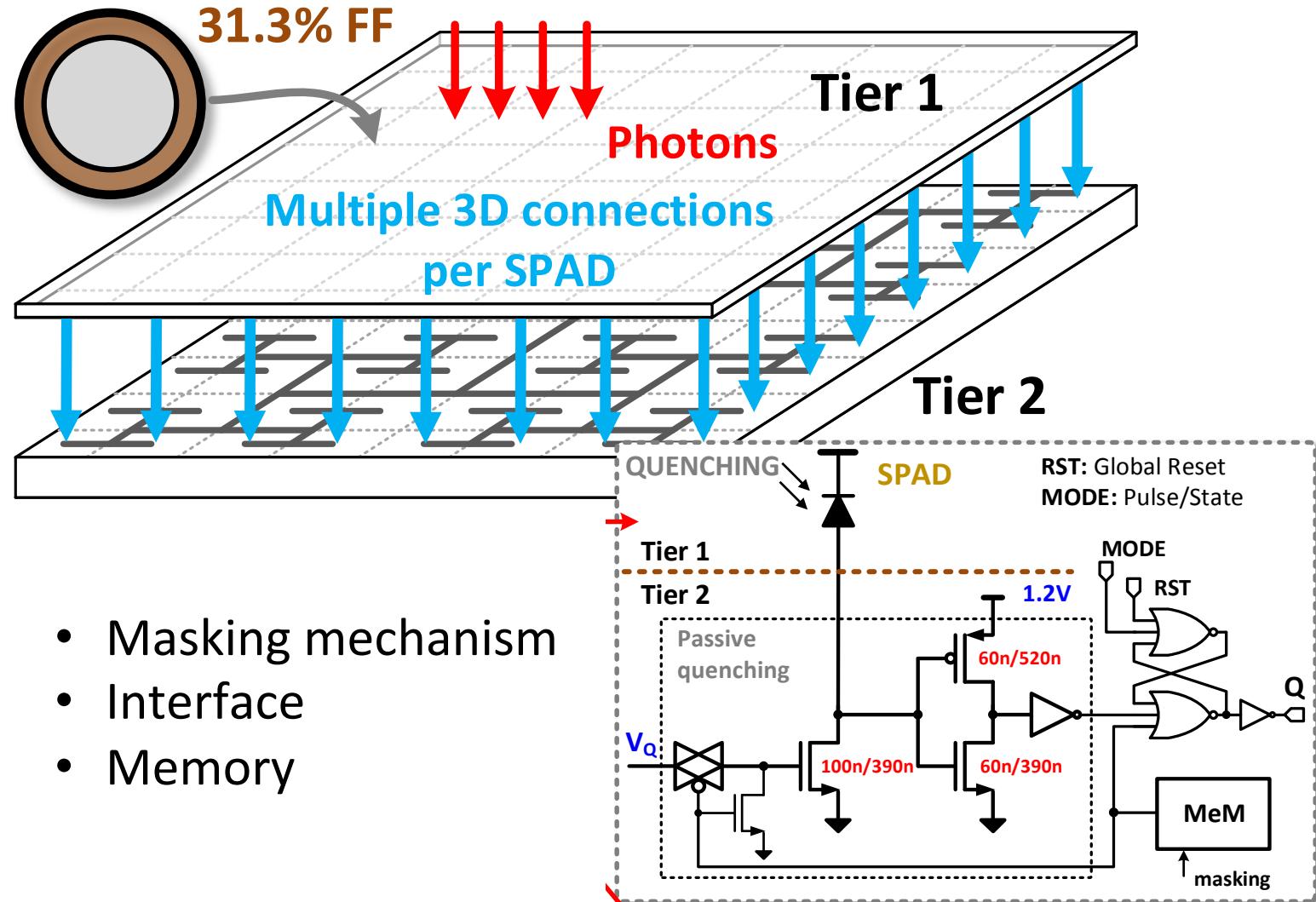
Case Study: LiDAR Sensor



M.J. Lee, A.R. Ximenes, P. Padmanabhan, Y. Yamashita, D.N. Yaung, E. Charbon, IEDM 2017

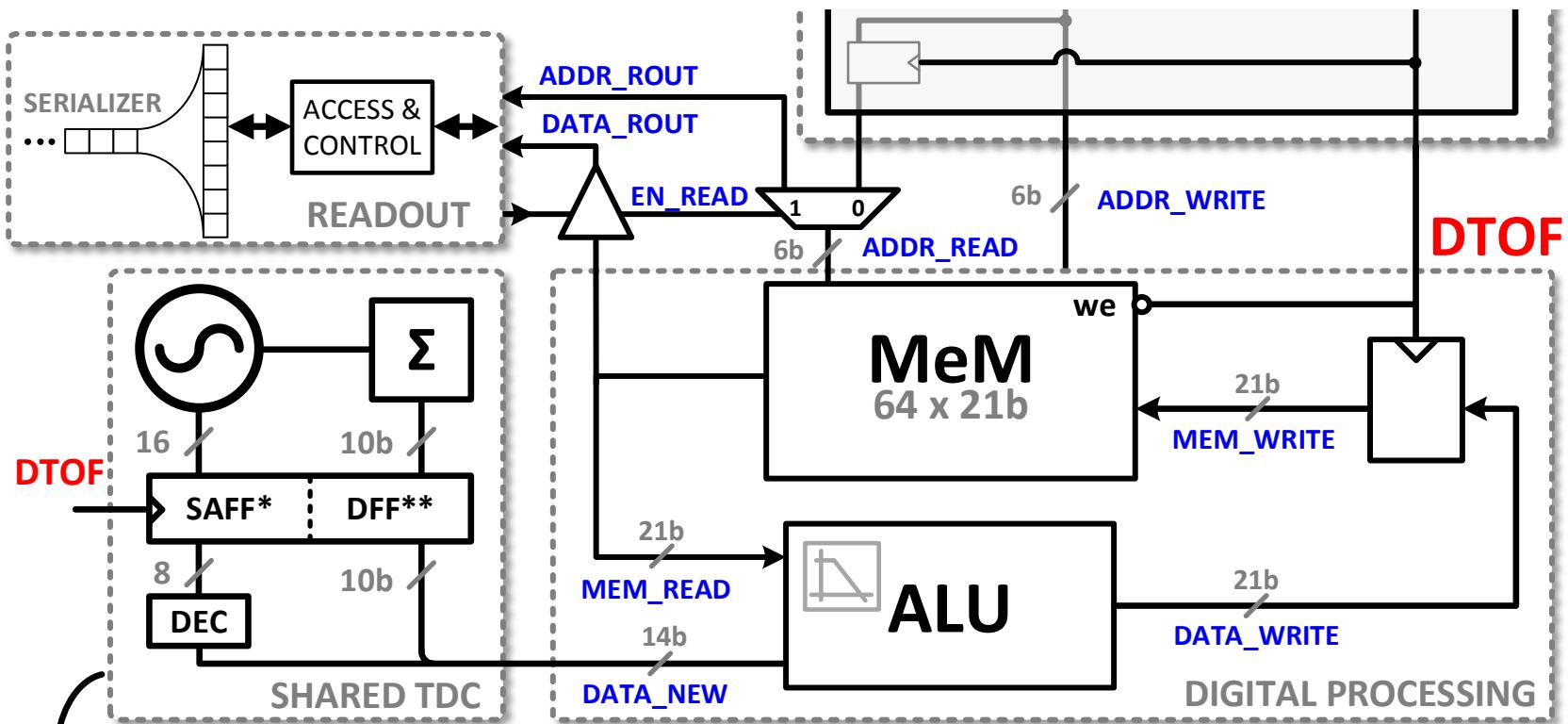
- Tier 1: SPADs + microlenses
- Tier 2: quenching, recharge, TDCs, multi-core, memories, communication unit, I/O

Case Study: LiDAR Sensor



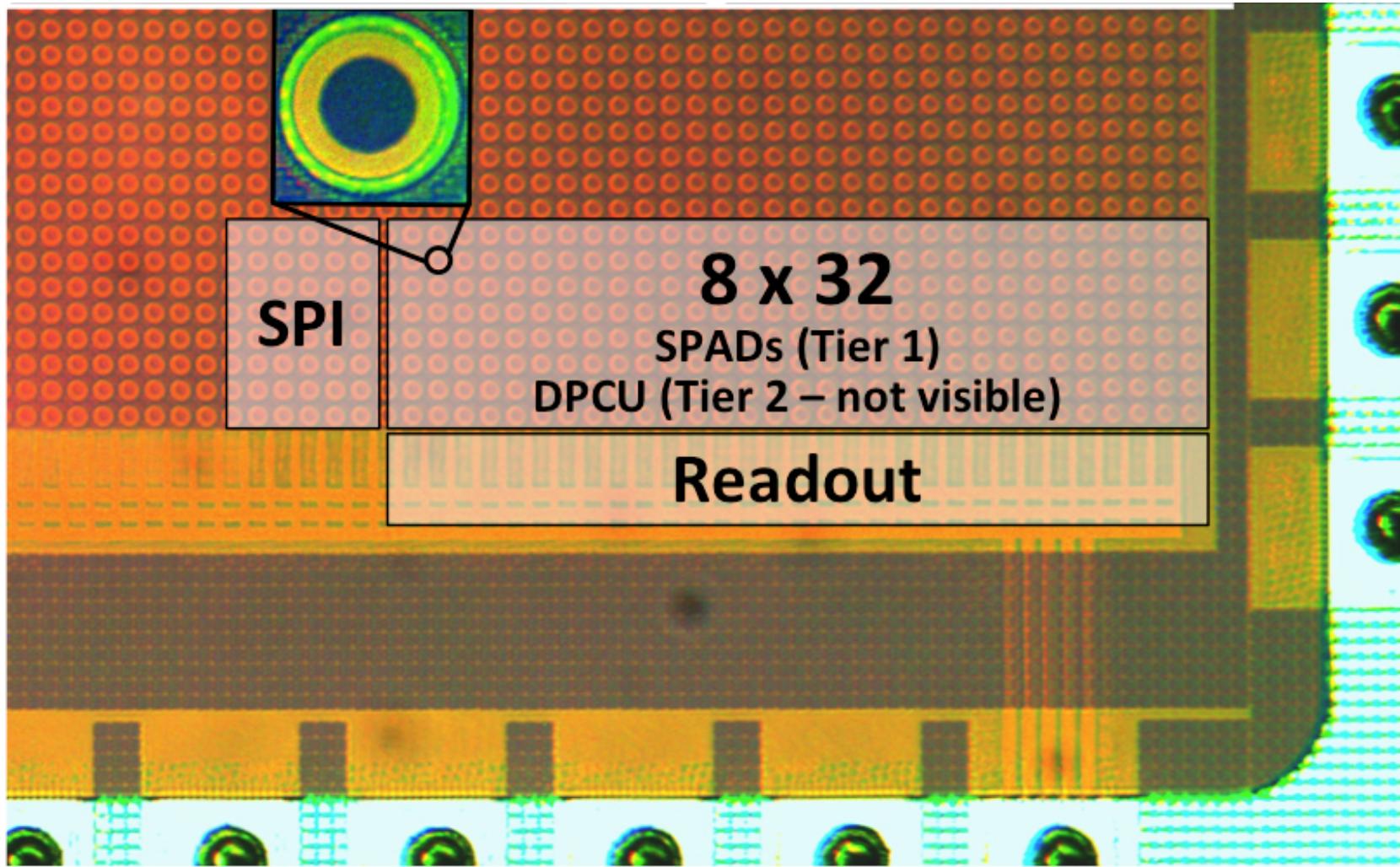
- Masking mechanism
- Interface
- Memory

Case Study: LiDAR Sensor

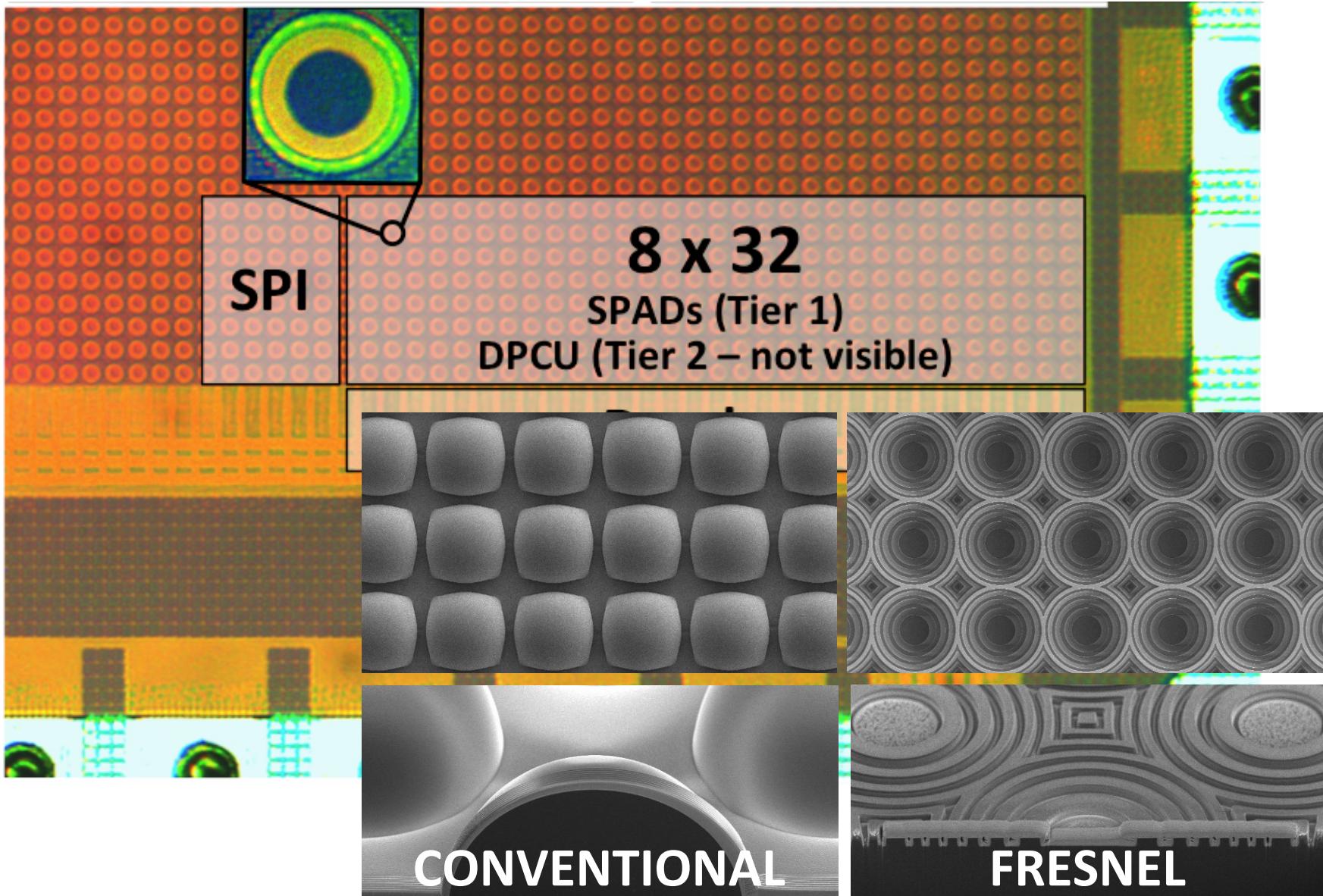


A.R. Ximenes, P. Padmanabhan, M.J. Lee, Y. Yamashita, D.N. Yaung, E. Charbon, ISSCC 2018

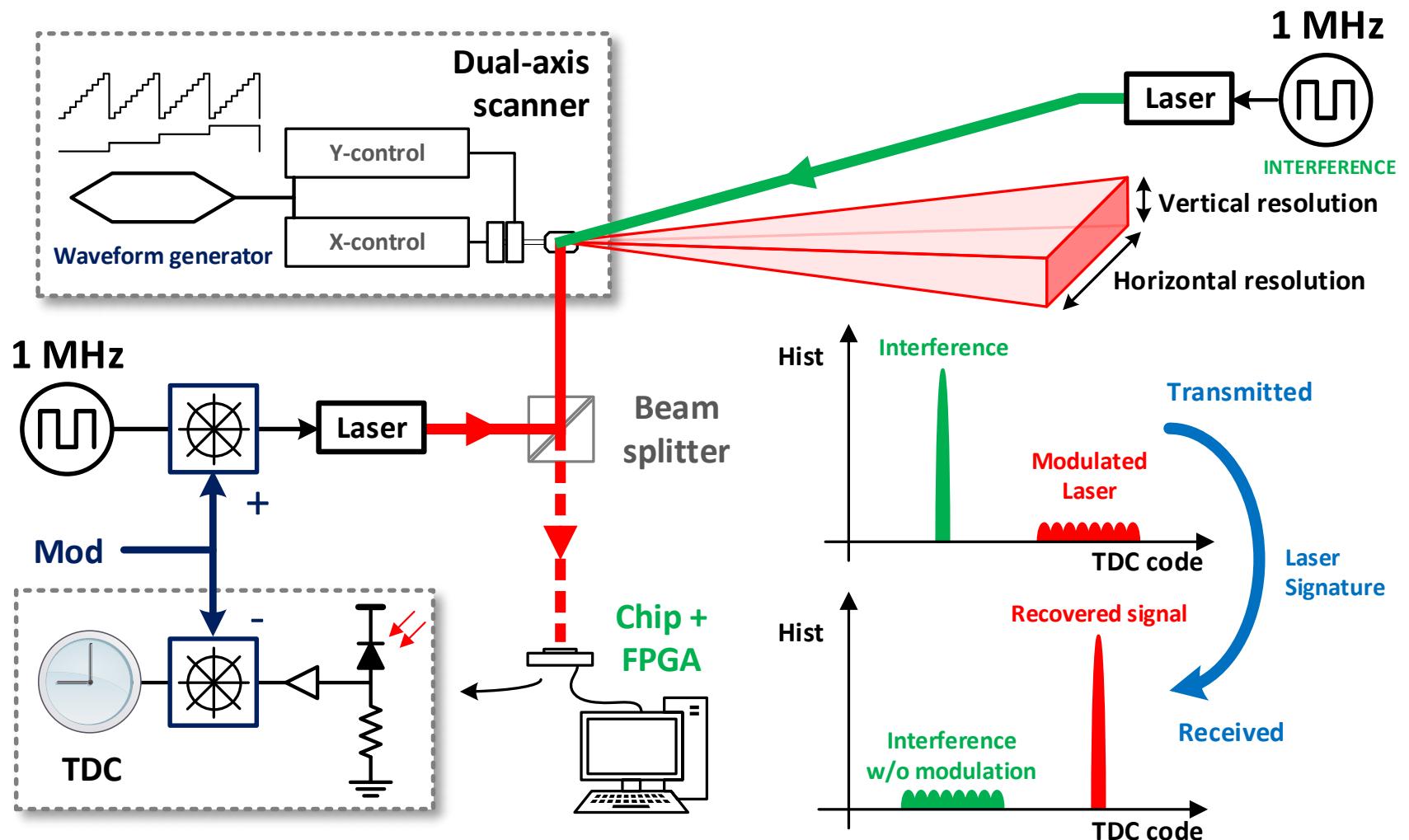
3D-Stacked Chip Micrograph



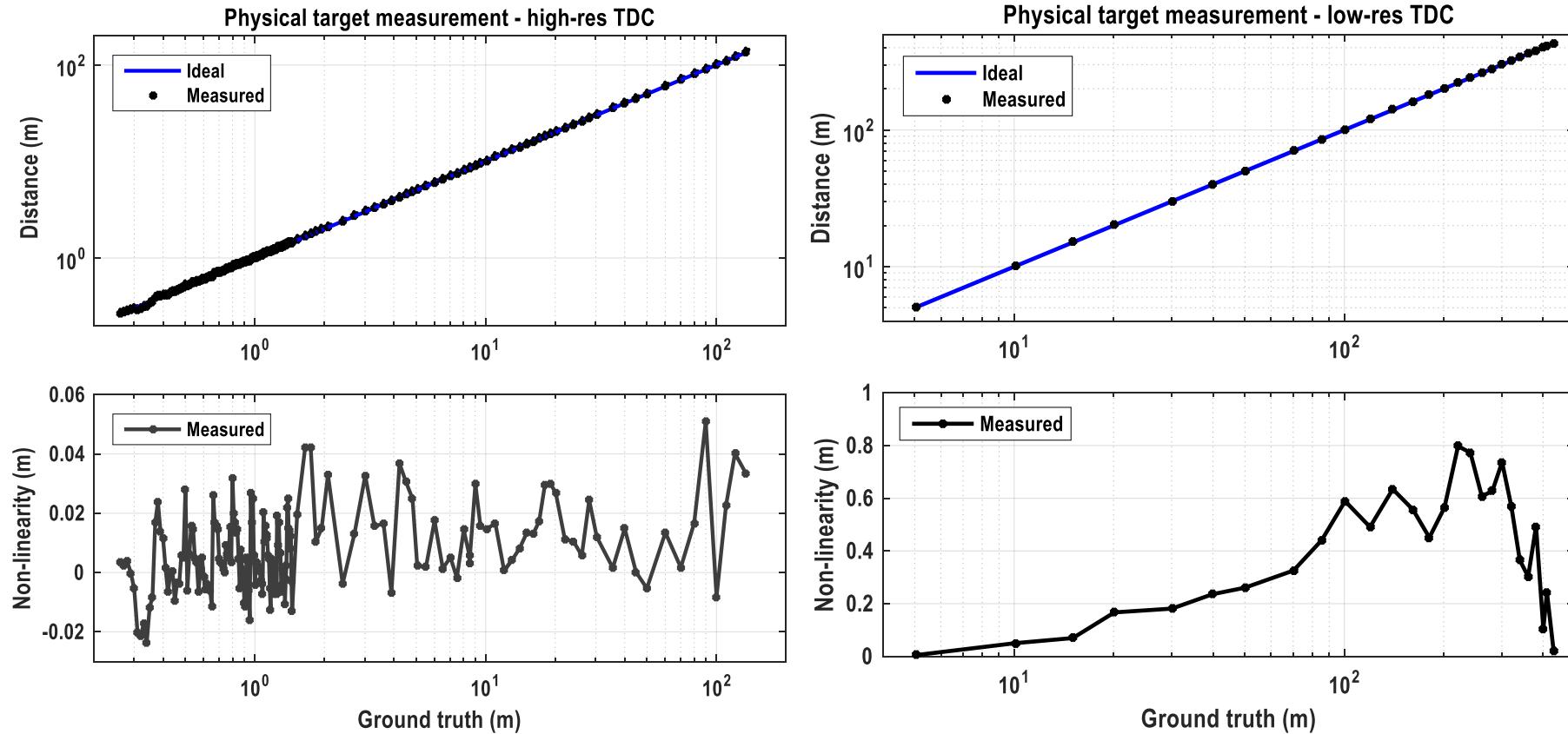
3D-Stacked Chip Micrograph



The LiDAR System

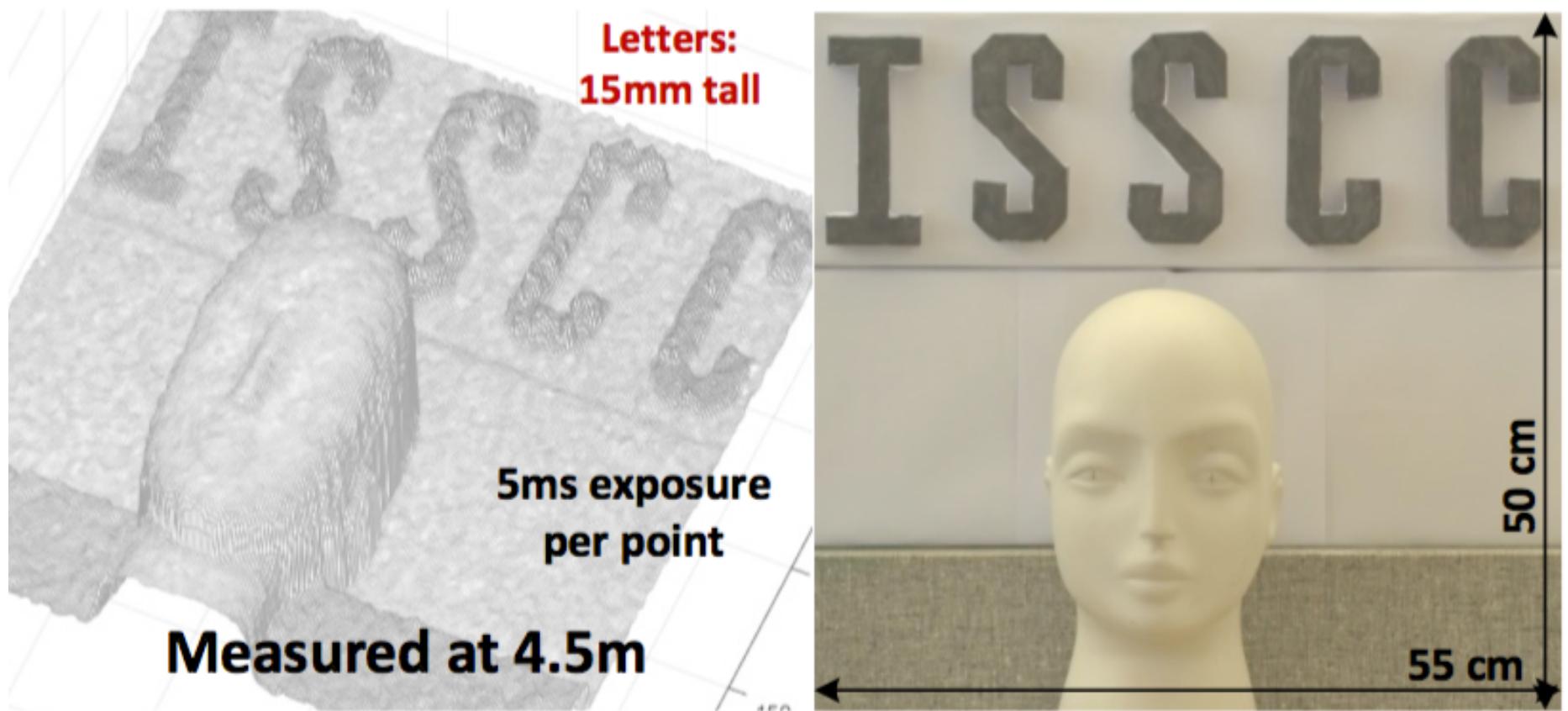


Distance Measurements

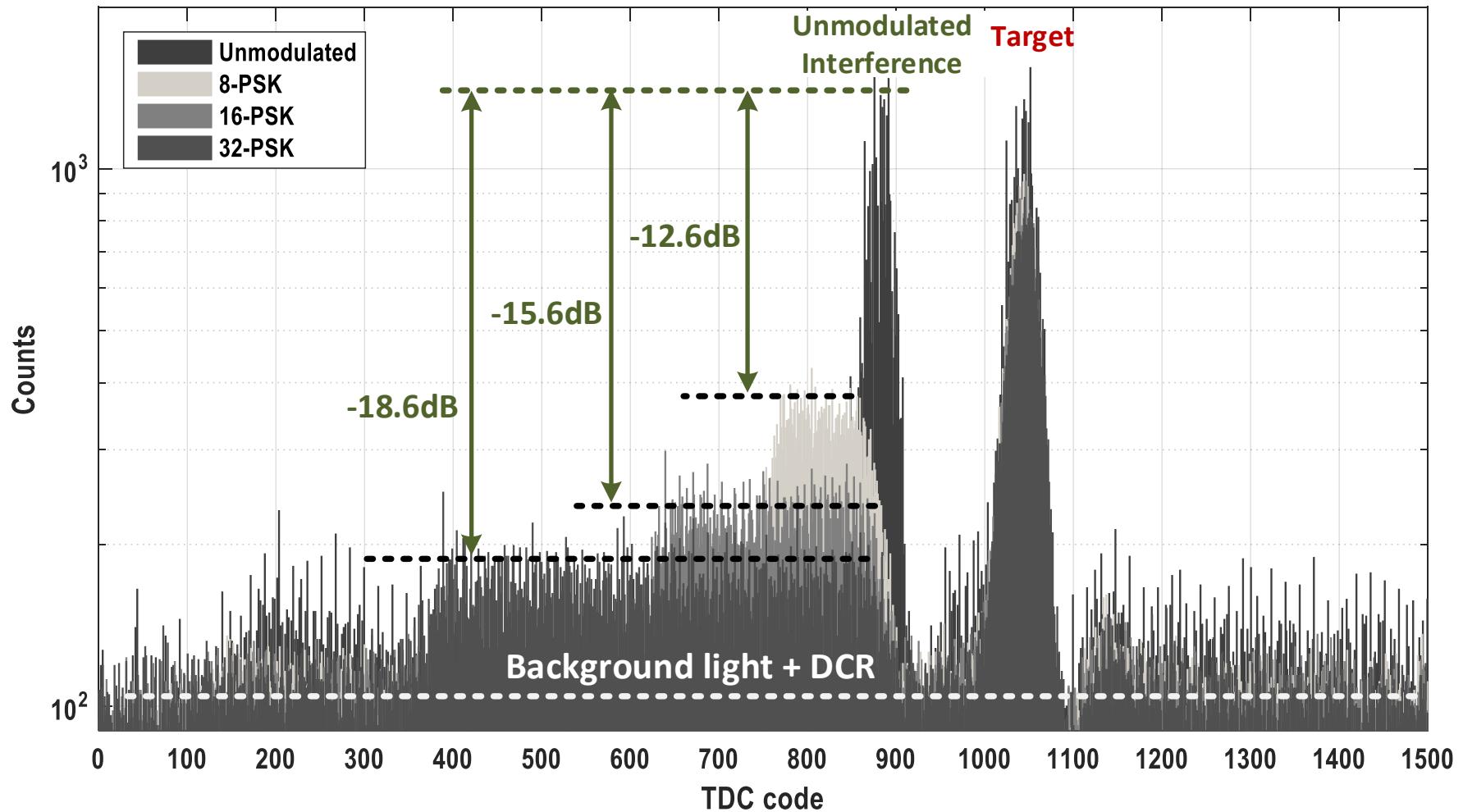


A.R. Ximenes, P. Padmanabhan, M.J. Lee, Y. Yamashita, D.N. Yaung, E. Charbon, ISSCC 2018

256x256 3D Image Reconstruction

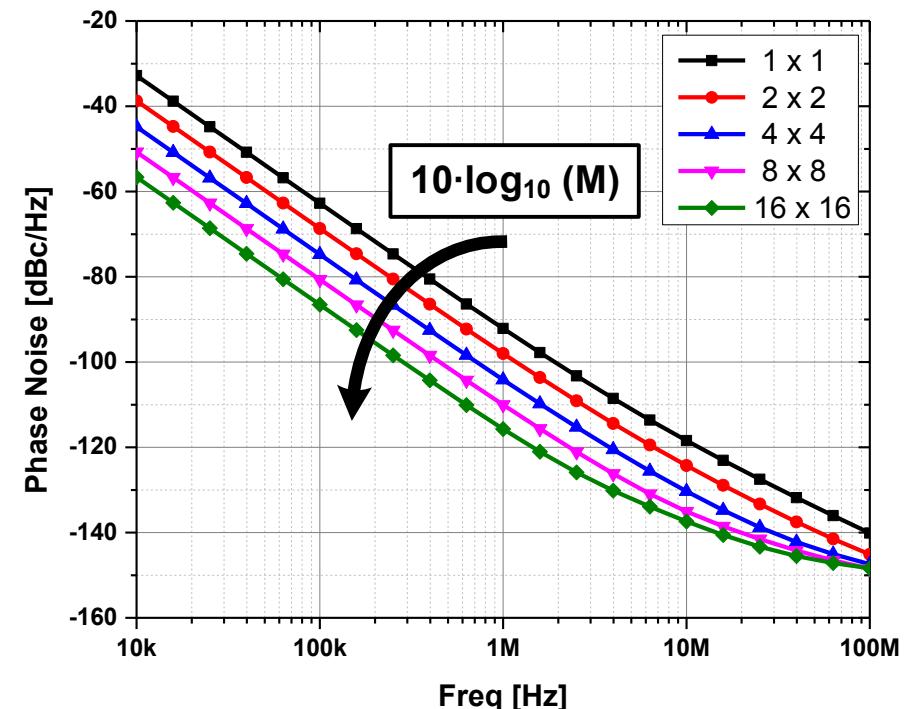
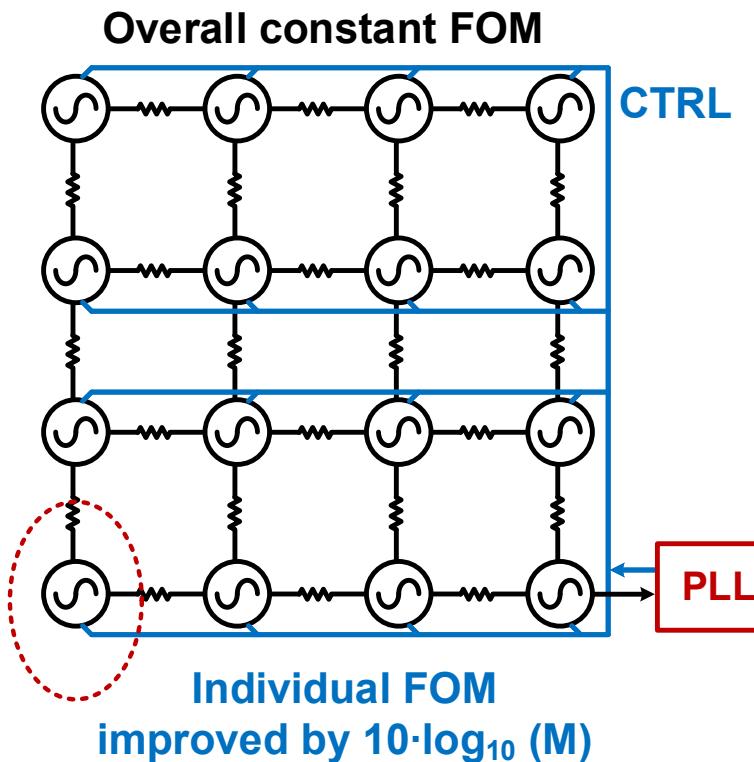


Interference Suppression



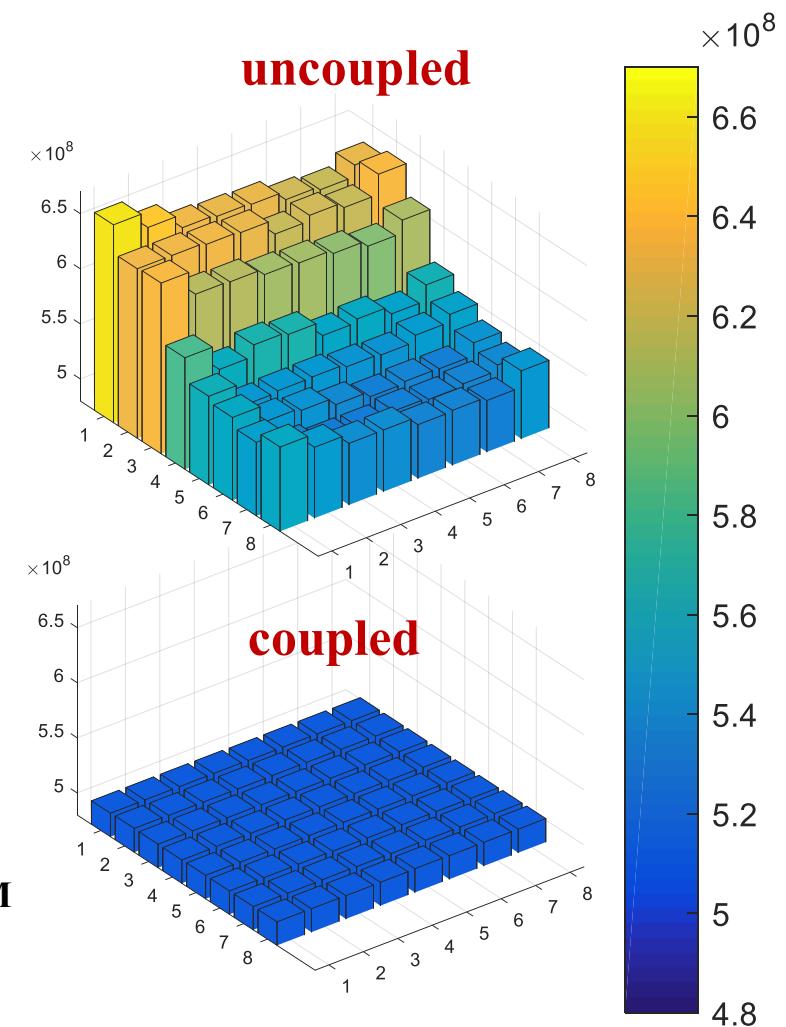
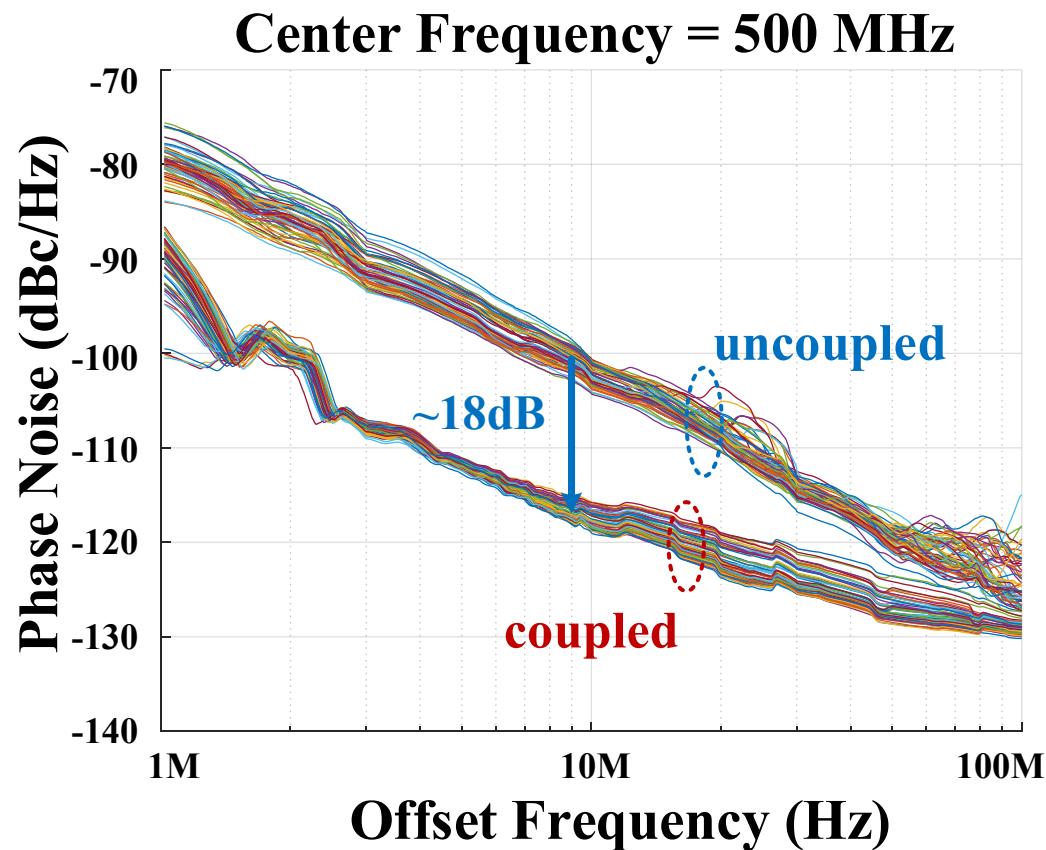
Large Array Synchronization

- Use injection locking for coupling VCOs
- The PLL only forces the desired frequency on the VCOs



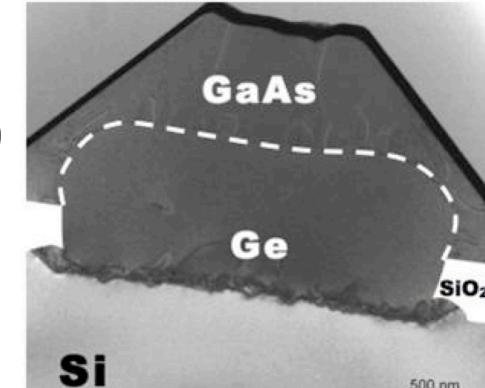
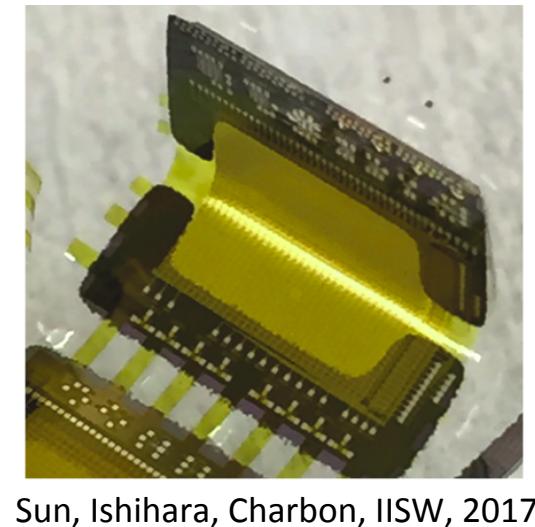
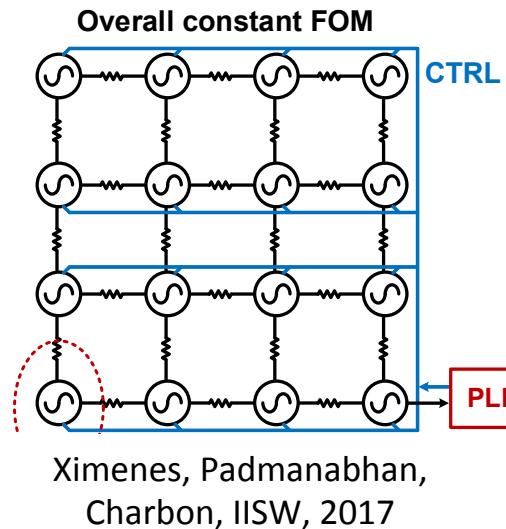
A.R. Ximenes, P. Padmanabhan, et al., IISW 2018

Mutual Coupling Measurements

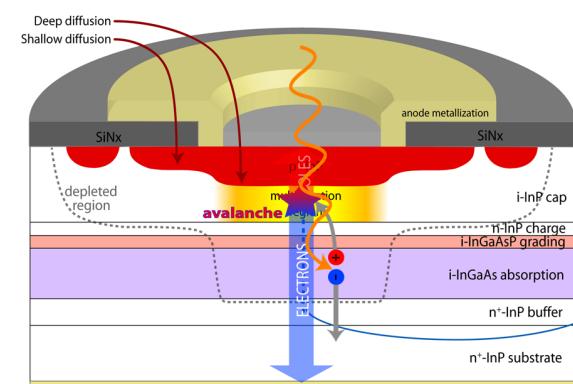


Perspectives for 2020

- Sub-65nm CMOS
- Large, scalable designs (Lego™ approach)
- Backside illumination (BSI) 3D IC
- New Materials (InP, GaAs, Ge, polymers)
- Small pixels, low noise, μ lenses

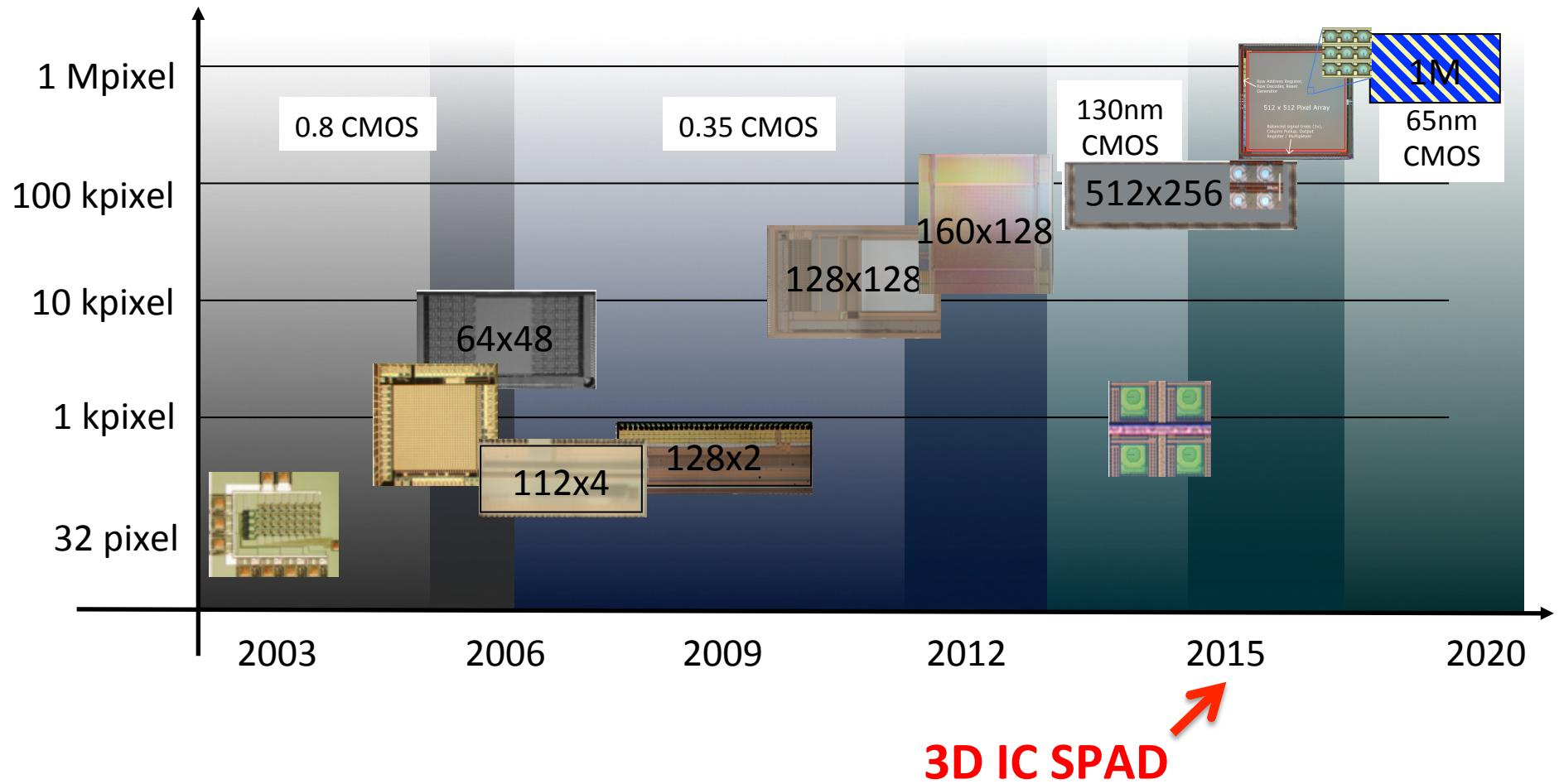


Sammak, Aminian, Charbon,
Nanver, IEDM11



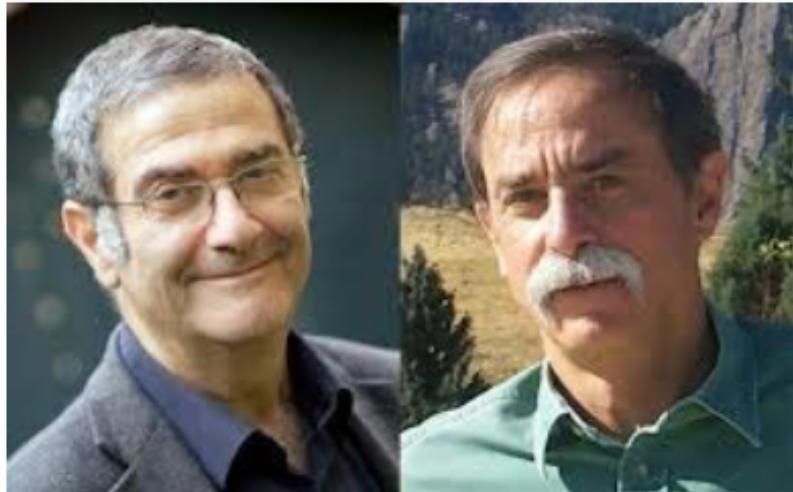
Tosi et al, 2012

Moore's Law for SPADs



SPADs in Quantum Computing

Quantum Computing



Serge Haroche

David Wineland



2012 Physics Nobel Prize

Both Laureates work in the field of quantum optics studying the fundamental interaction between light and matter, a field which has seen considerable progress since the mid-1980s. Their ground-breaking methods have enabled this field of research to take the very first steps towards building a new type of super fast computer based on quantum physics. Perhaps the quantum computer will change our everyday lives in this century in the same radical way as the classical computer did in the last century.

—Announcement 2012 Nobel Prize

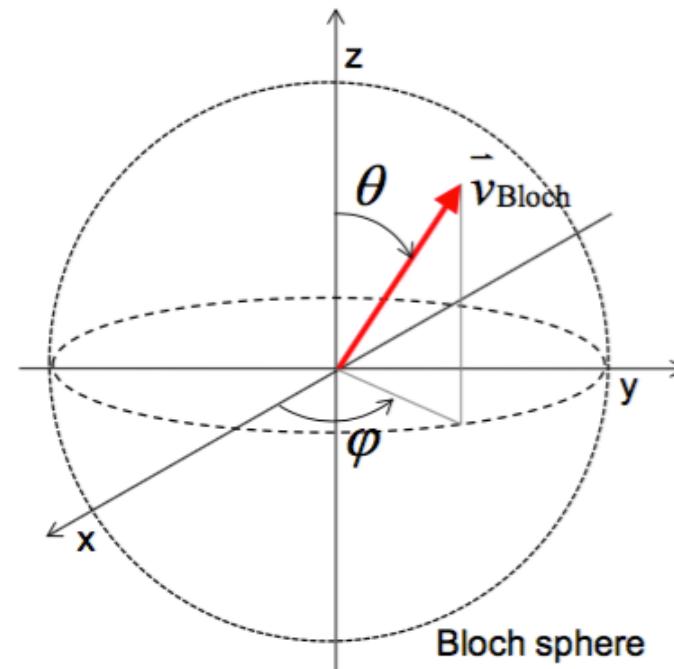
From bits to qubits

- A quantum bit or qubit is a quantum system in which the Boolean states 0 and 1 are represented by a pair of mutually orthogonal quantum states labeled as $|0\rangle, |1\rangle$
- Quantum properties: **superposition** and **entanglement**

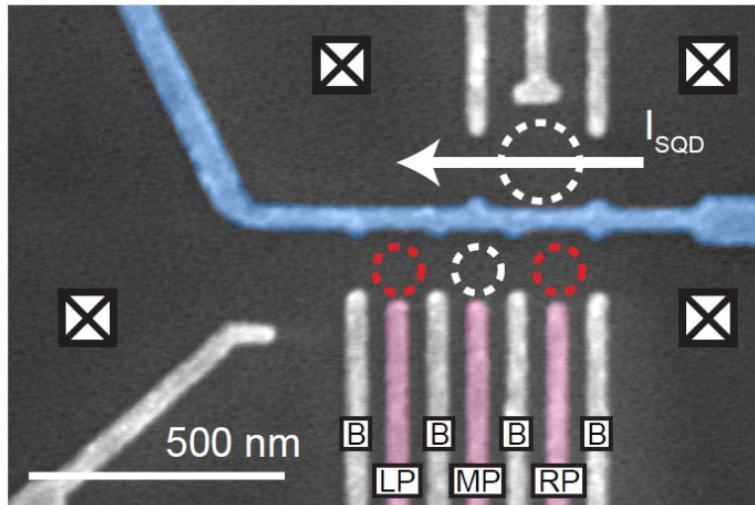
- $\alpha_0, \alpha_1 \in C$
- $|\alpha_0|^2 + |\alpha_1|^2 = 1$

$$|\psi\rangle = e^{i\delta} (\cos(\theta/2)|0\rangle + e^{i\varphi} \sin(\theta/2)|1\rangle)$$

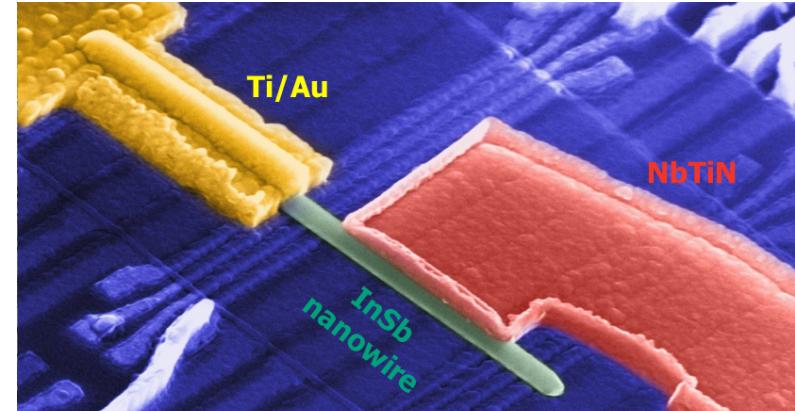
θ is polar angle
 φ is azimuthal angle



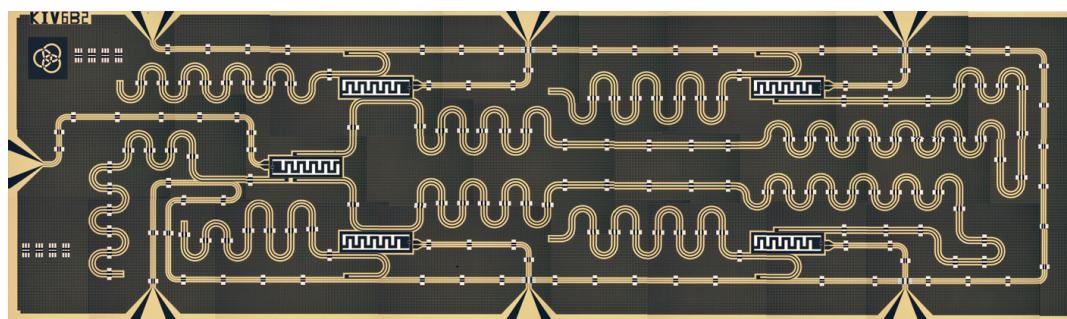
Qbits on a Chip



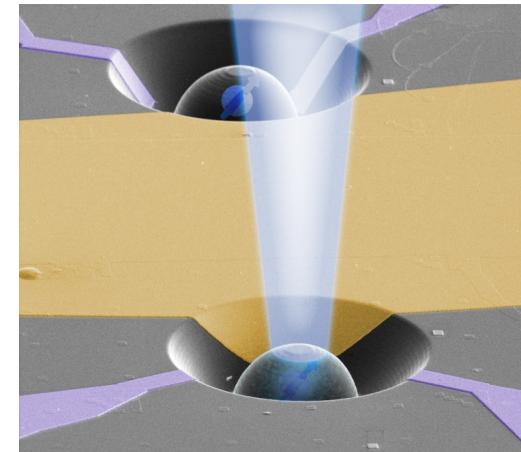
Semiconductor quantum dots



Semiconductor-superconductor hybrids



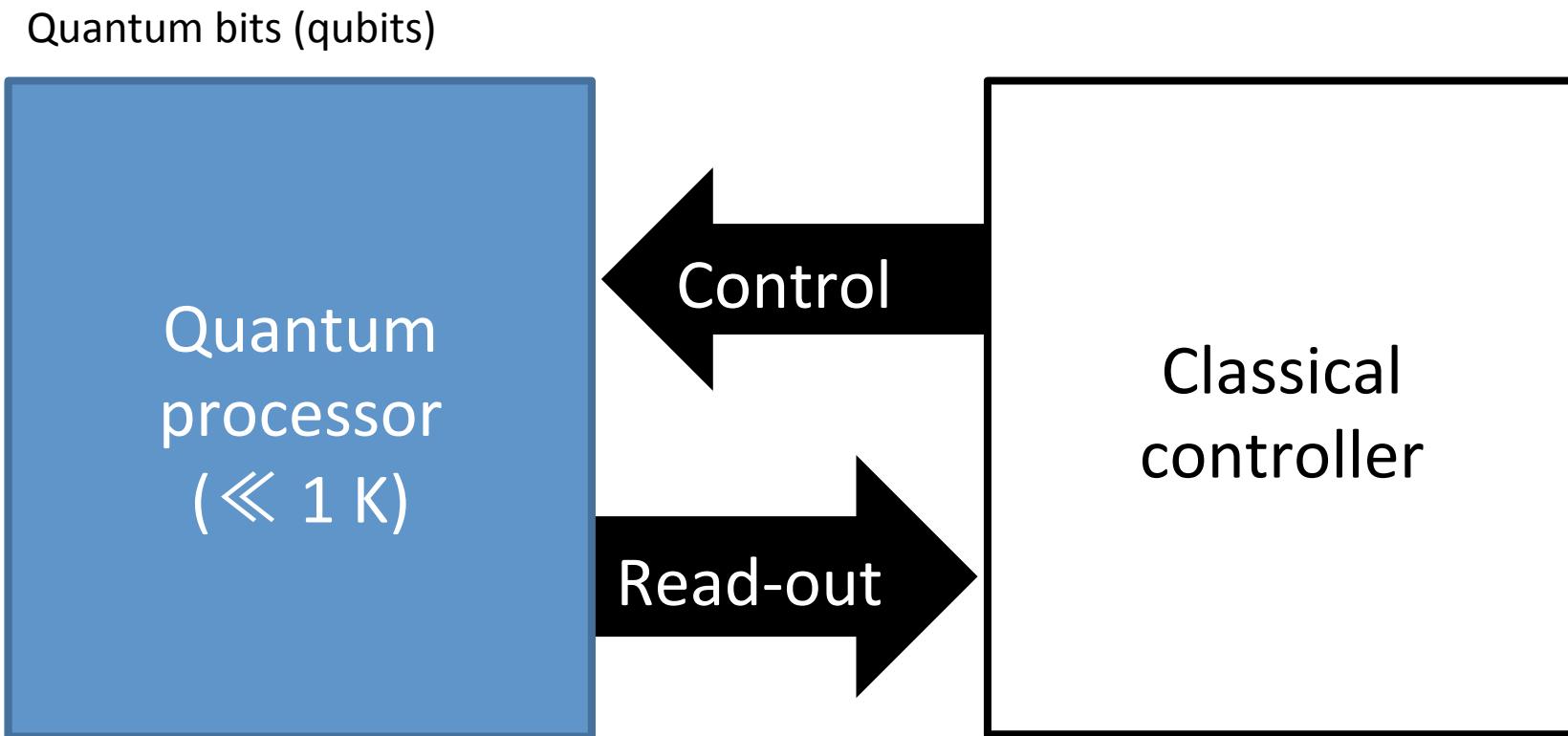
Superconducting circuits



Impurities in diamond or silicon

Source: L. Vandersypen, 2017

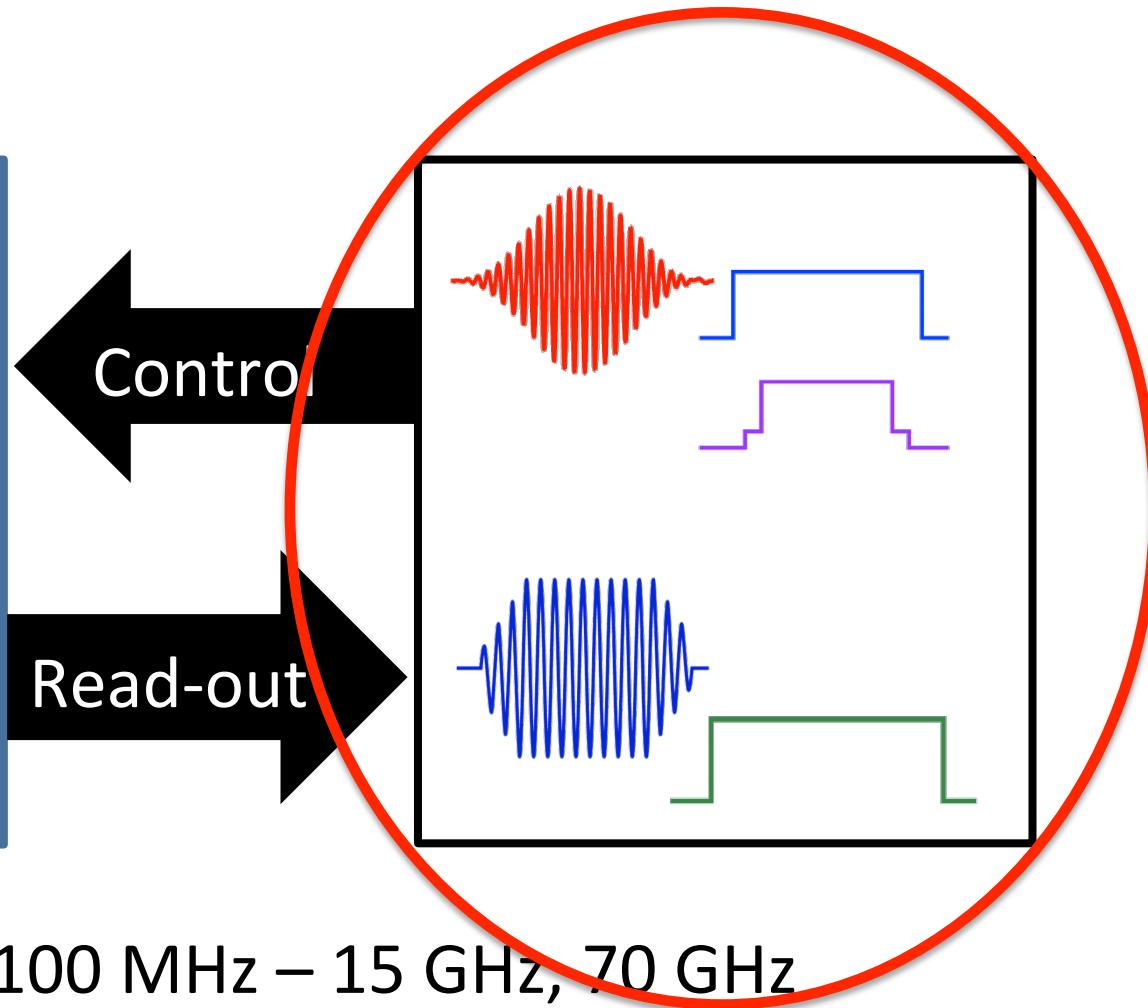
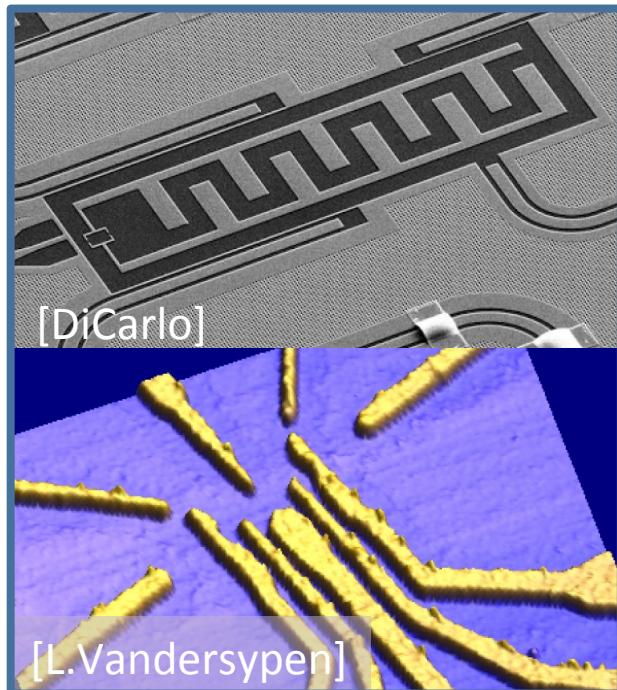
Quantum Computer Architecture



- Carrier frequency: 100 MHz – 15 GHz, 70 GHz
- Pulses: 10 – 100 ns

Quantum Computer Architecture

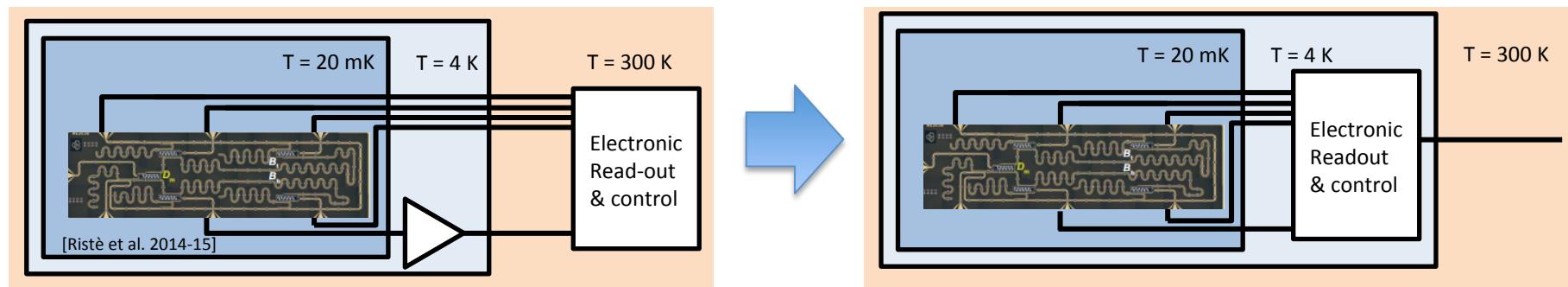
Quantum bits (qubits)



- Carrier frequency: 100 MHz – 15 GHz, 70 GHz
- Pulses: 10 – 100 ns

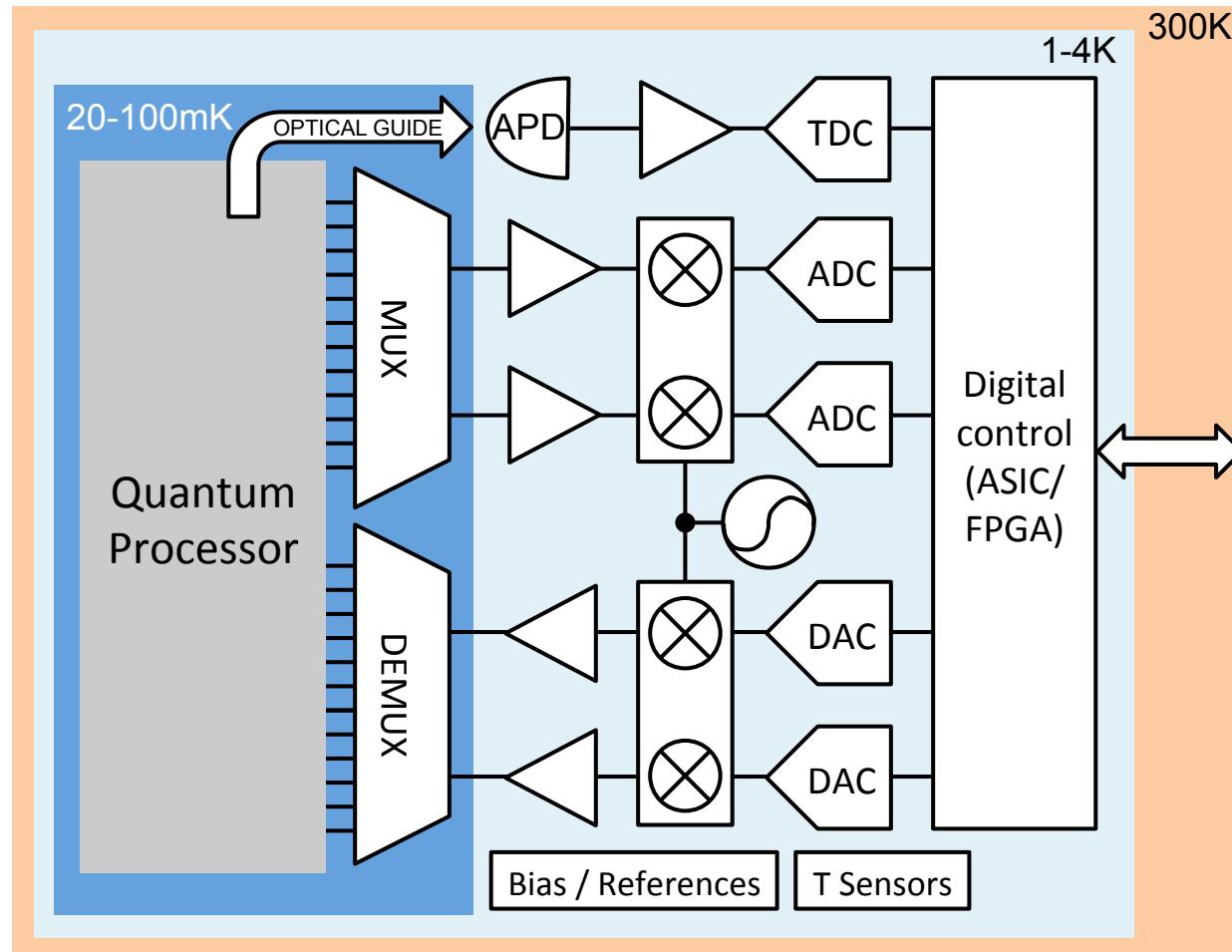
Possible Solutions

- **Proposed solution**
 - Electronics at 4 K
 - Only connections to 4 K to 20 mK are needed



- **Ultimate solution**
 - Qubits at 4 K
 - Monolithic integration

Electronic Readout & Control

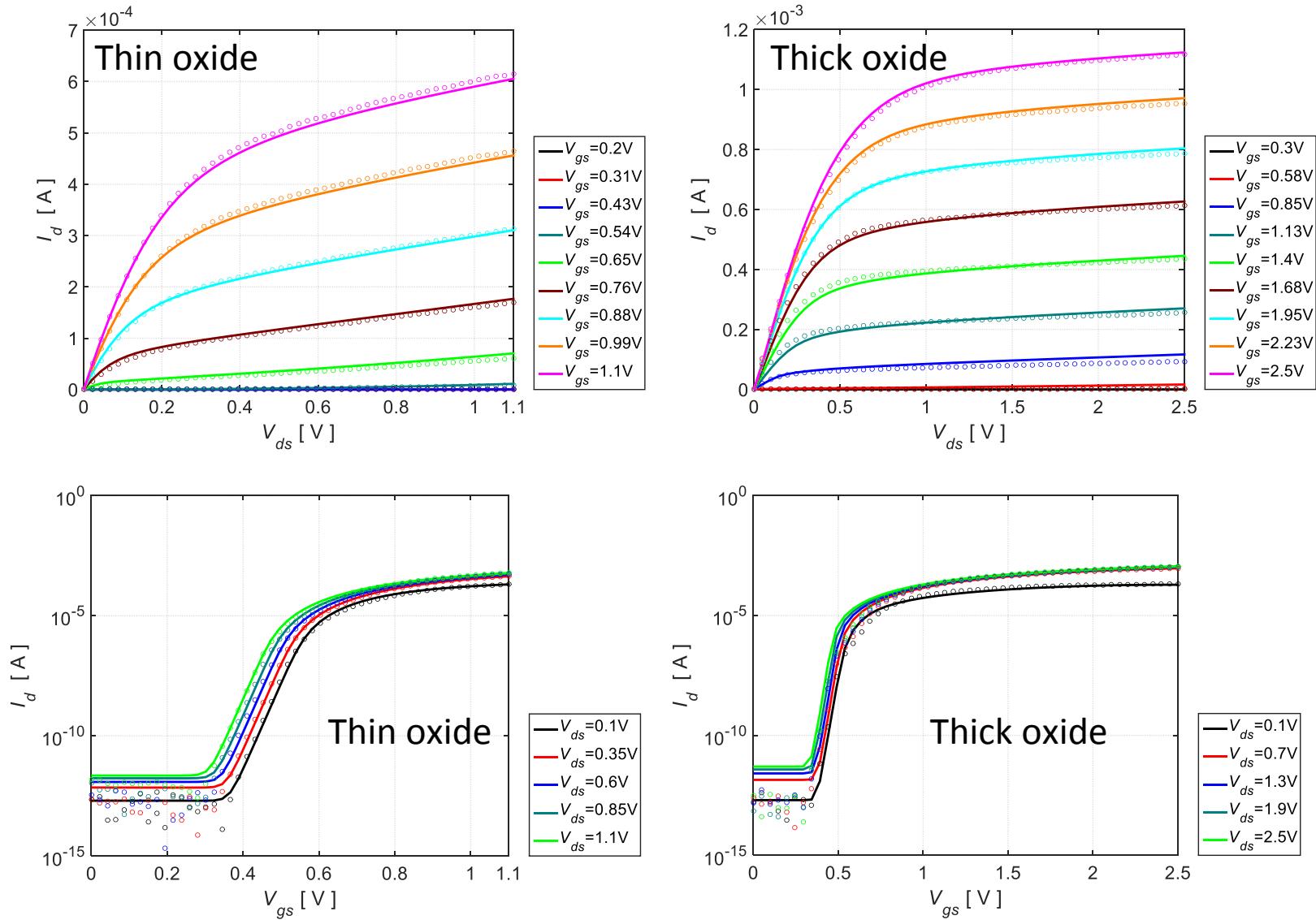


E. Charbon et al., *IEDM 2016*

Cryogenic Electronics

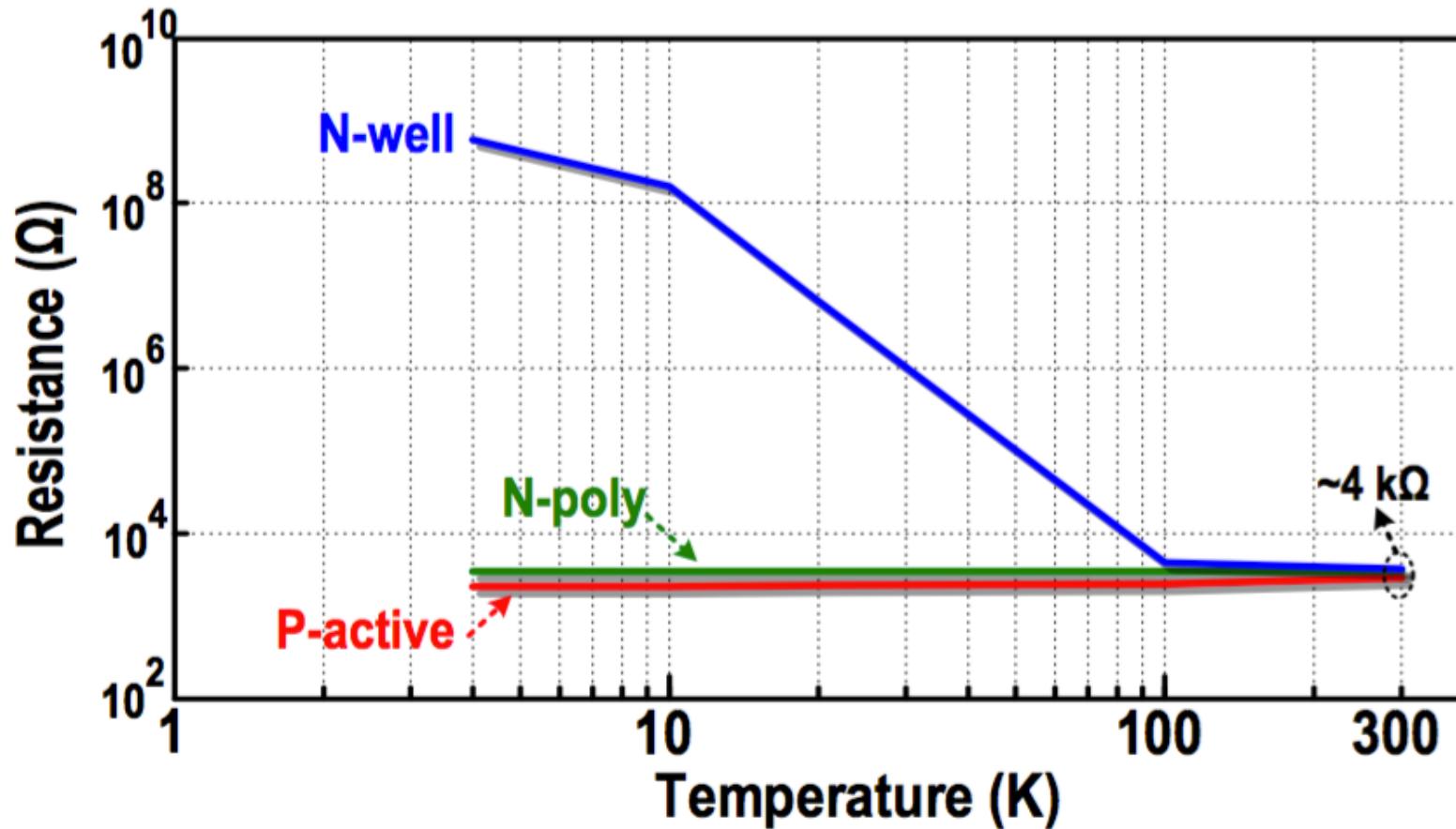
Cryo-CMOS Technologies

40nm MOS at 4K



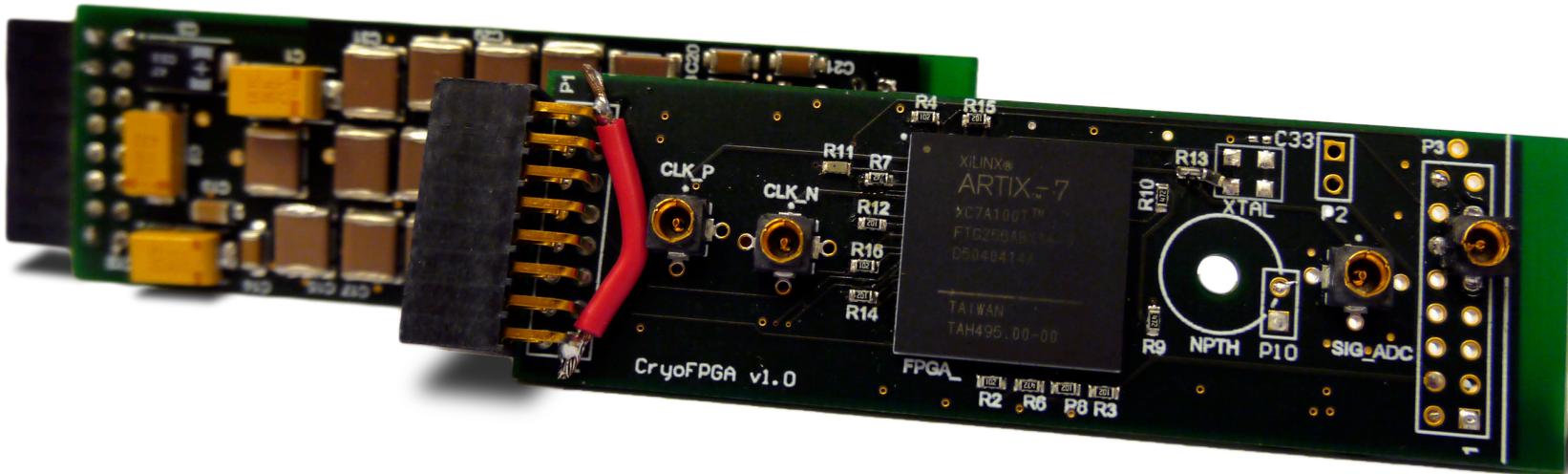
R.M. Incandela et al., ESSDERC 2017, Journal of EDS 2018

Substrate resistivity



B. Patra et al., JSSC 2018

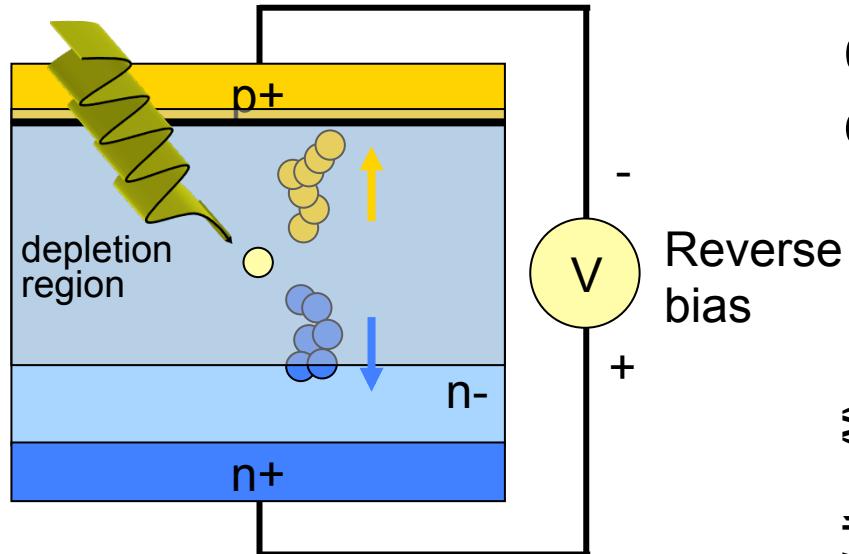
Cryo-FPGAs



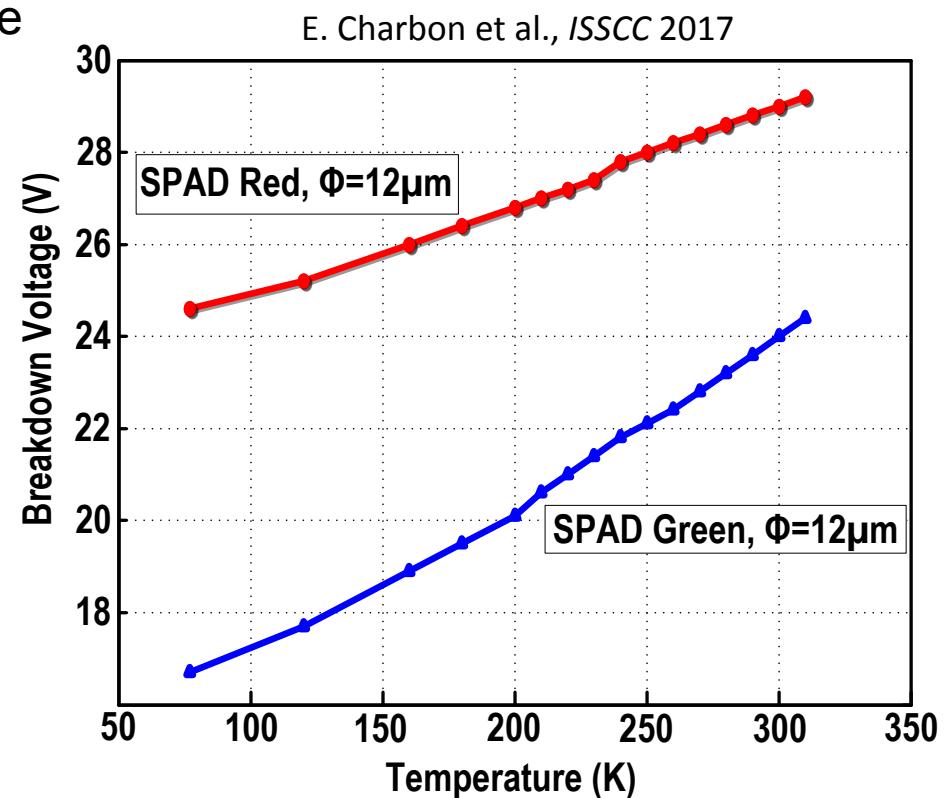
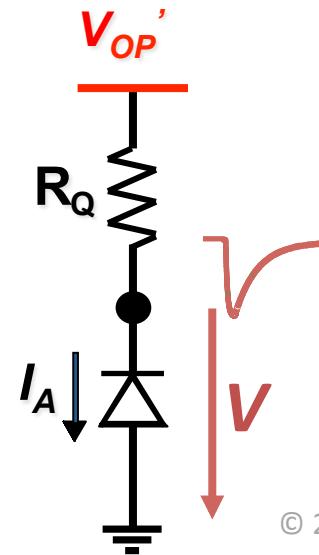
Harald Homulle

- Artix-7 full operation down to 4K
- Other FPGAs only limited to 30K

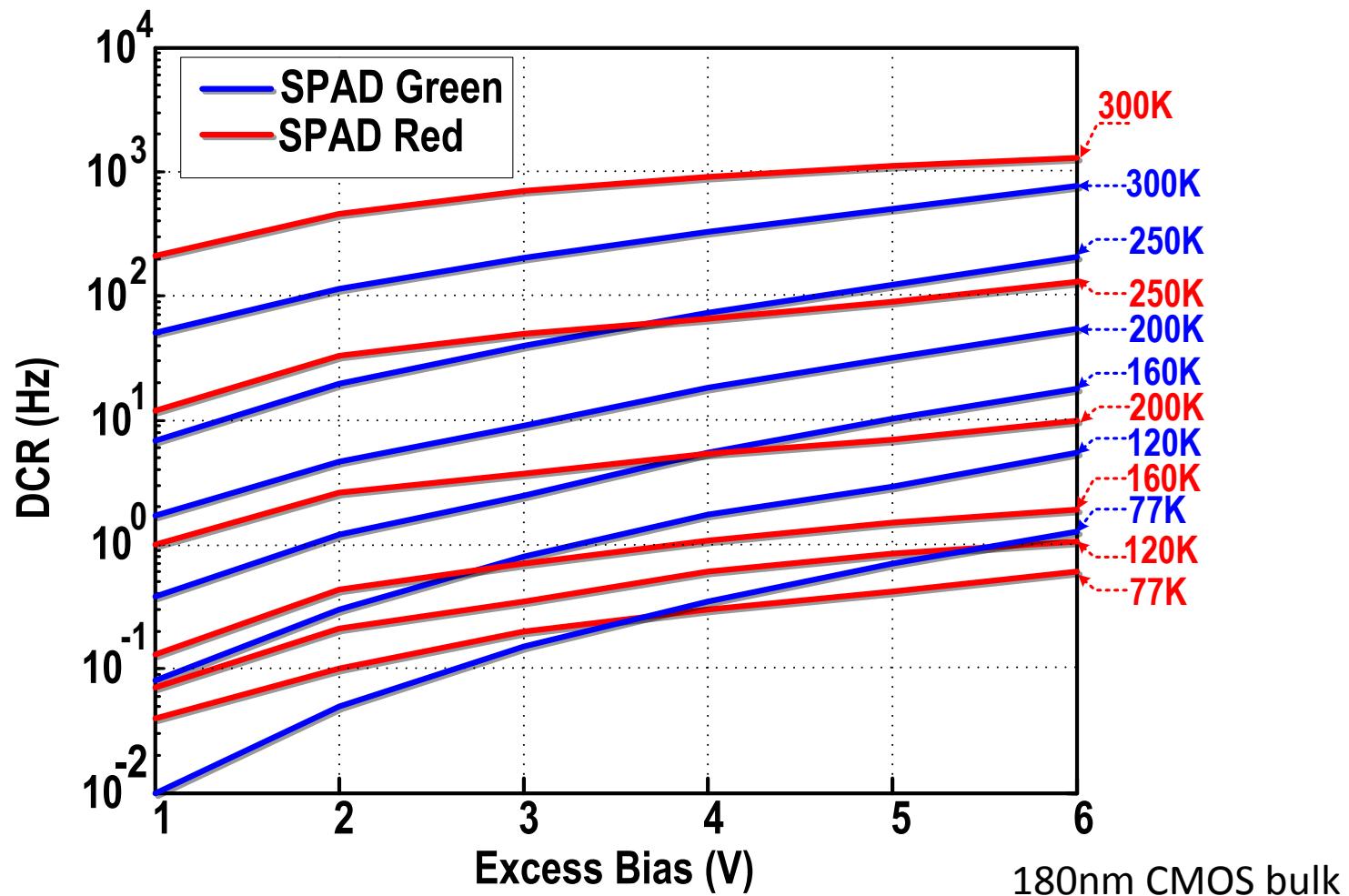
Cryo-SPADs



Operation in proportional and
Geiger mode (SPAD)

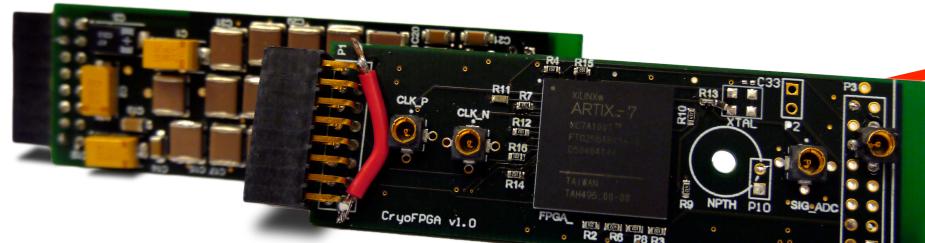


Cryo-SPADs

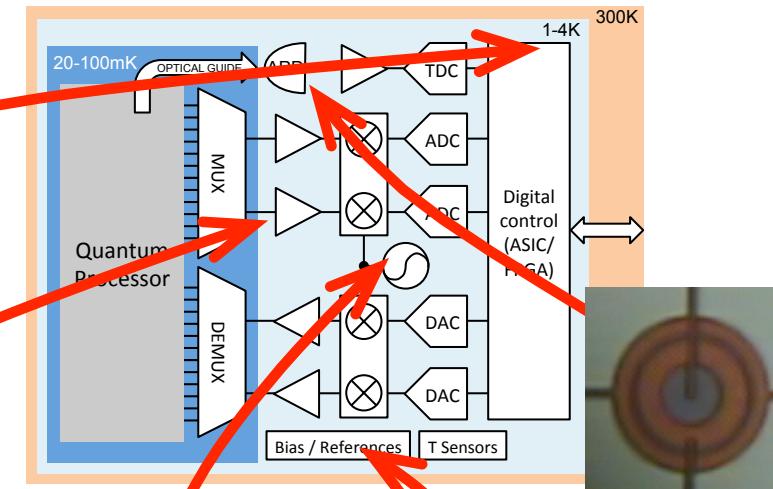


B. Patra et al., JSSC 2018

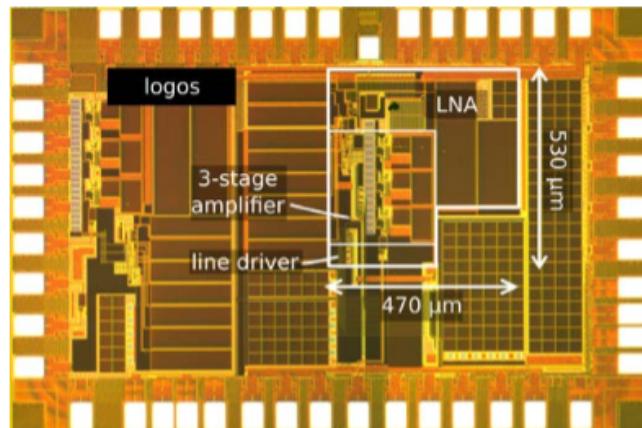
Building up



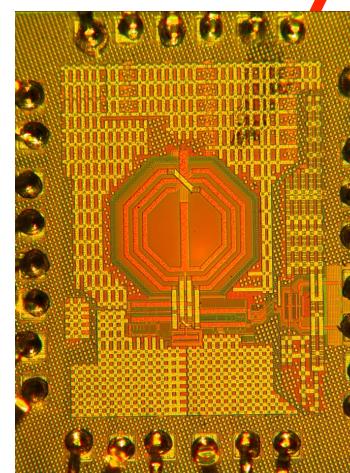
IEEE IEDM 2016



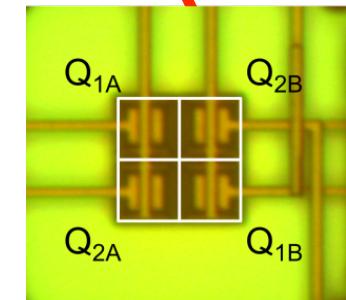
IEEE IEDM 2016
IEEE JSS



IEEE ISSCC 2017
IEEE JSSC 2018



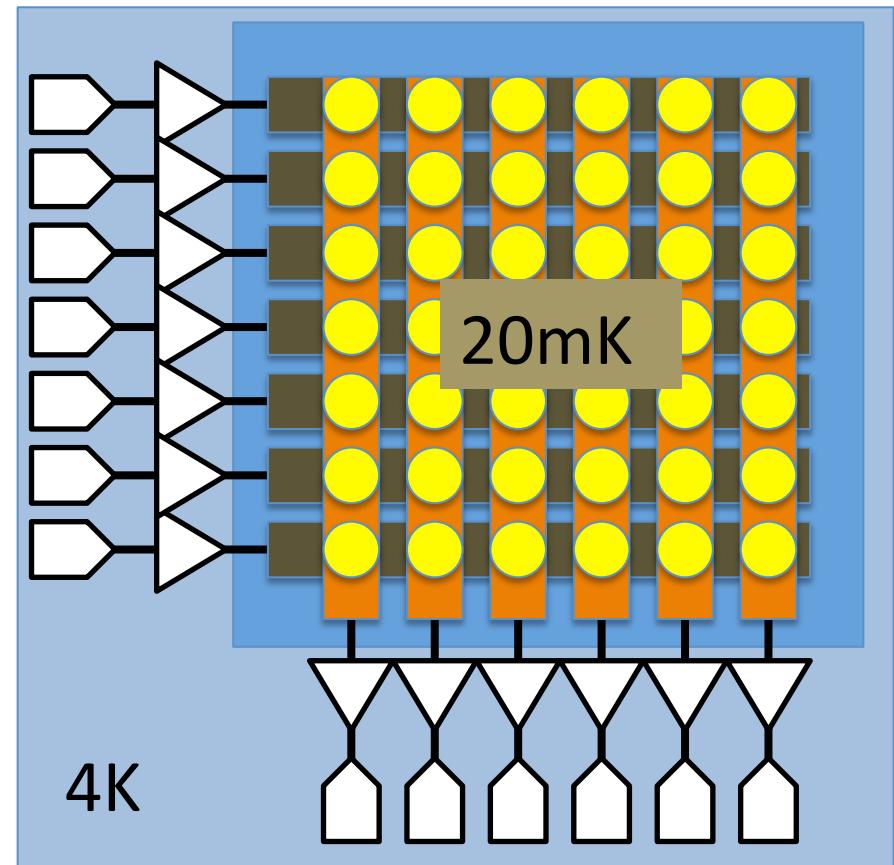
IEEE ISSCC 2017
IEEE JSSC 2018



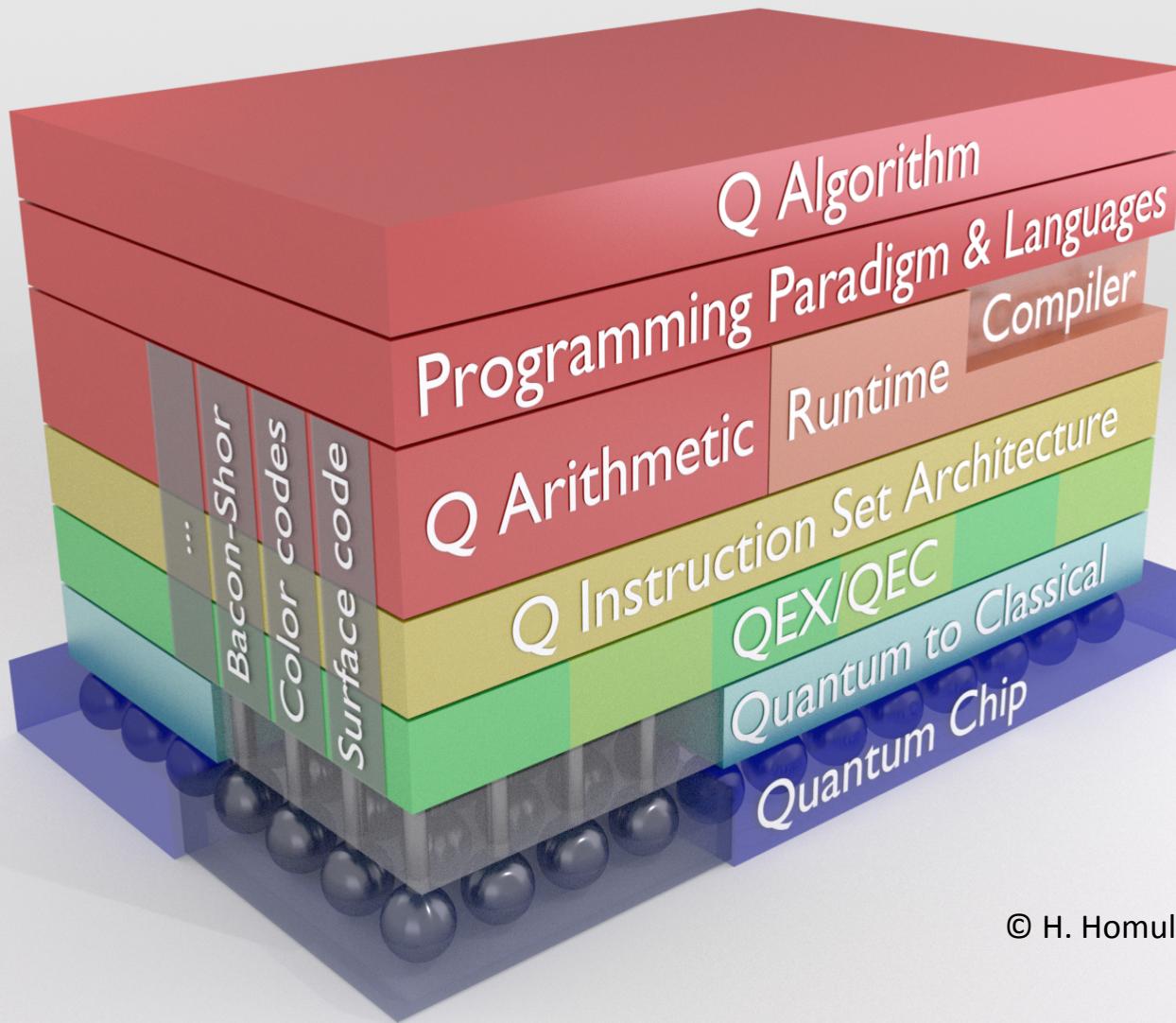
IEEE Sensors 2016

2D readout and control

- Use *imaging sensor* readout as inspiration
- Reduce number of transistors (ideally to zero)
- Use tunneling barriers as selectors
- (limited) use of 3D stacking



Putting things in context



© H. Homulle 2016

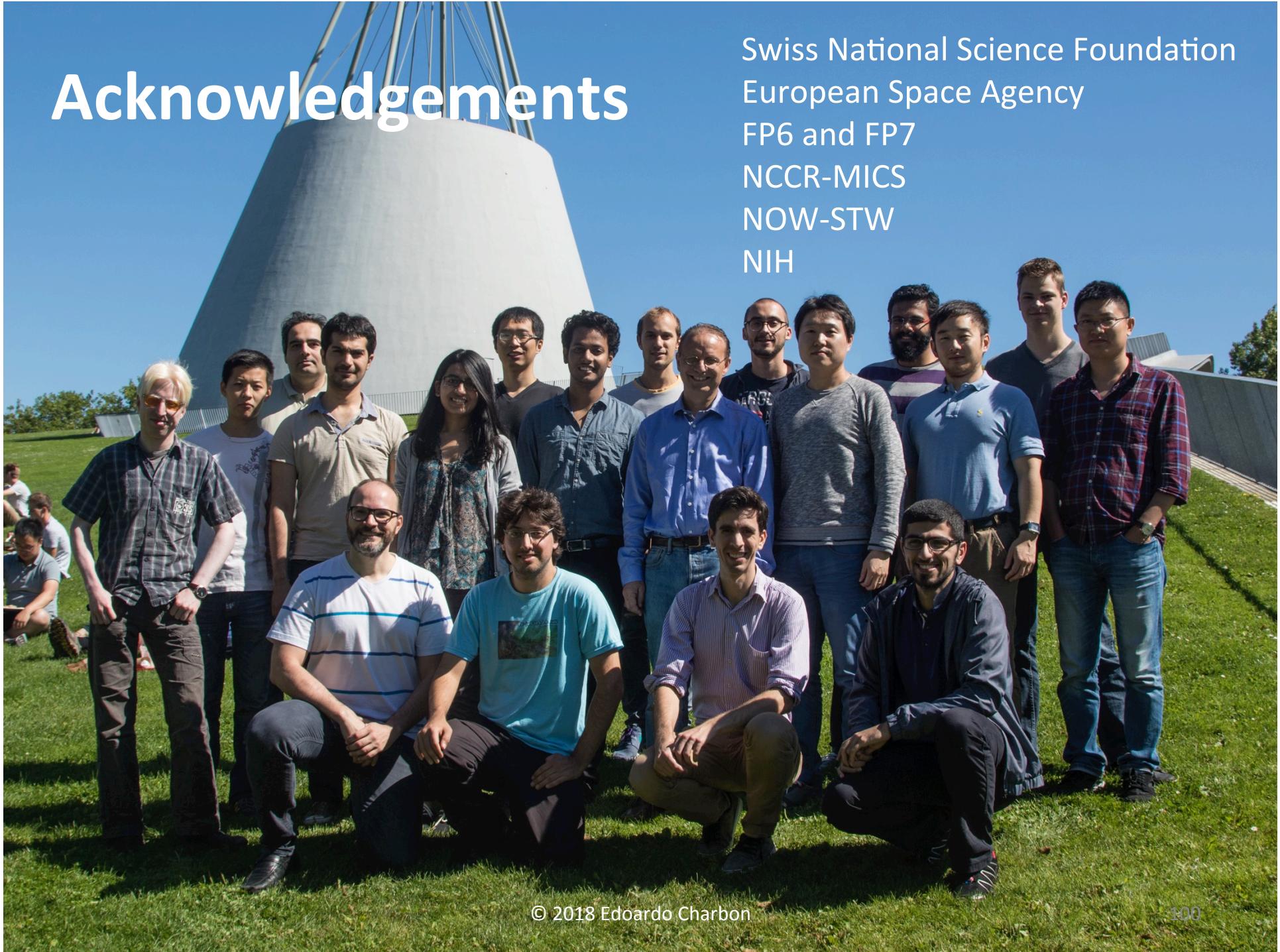
Conclusions

Take-home Messages

- SPADs are quantum devices and that they can be used for quantum applications
- Modularity is an important ingredient to large photonic systems and even the technology of a cellphone camera will do
- One can actually make a product (and money) out of SPADs
- Quantum Computing will need cryo-SPADs and 3D ICs

Acknowledgements

Swiss National Science Foundation
European Space Agency
FP6 and FP7
NCCR-MICS
NOW-STW
NIH



<http://aqua.epfl.ch>

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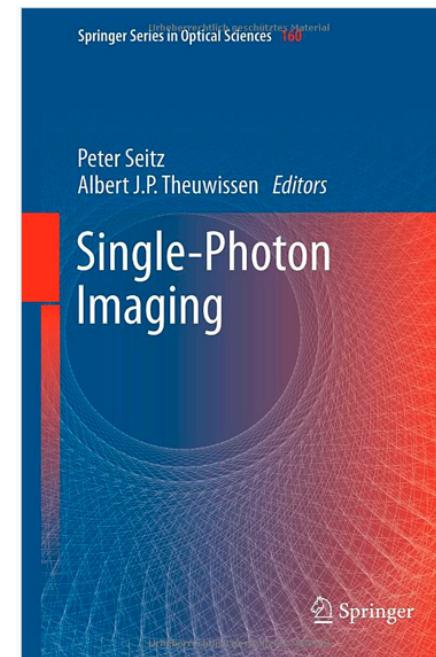
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