VCO-Based ADC for IoT Applications on Google Skywater 130nm OpenSource PDK

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Many open-source hardware projects have gained attention in recent years because anyone can learn from, use, and contribute to them. In addition, recently-published opensource PDKs and EDA tools help to build a complete opensource ecosystem. Contributing to this movement, we designed a VCO-based ADC – a mixed-signal design for Internet-of-Thing (IoT) applications – and implemented this design on Google Skywater 130nm Opensource PDK using purely OpenSource EDA tools and IPs.

Many IoT applications need to collect data from the environment using sensors; therefore, a low-cost and low-power integrated ADC is essential for IoT System-on-Chips (SoCs). A VCO-based ADC architecture has a small hardware area and consumes less power consumption, that is suitable for IoT applications. In addition, most parts of the design are digital, which can be easily reused and ported to new technologies.

Our ADC uses ∑Δ architecture with the first-order noise shaping, as shown in Fig. 1. Firstly, the VCO encodes the voltage level of the input signal into the speed of pulses. After that, a multiphase readout that implements ∑Δ modulators to sample the pulses in each clock. Finally, a third-order Cascaded Integrator Comb (CIC) filter is applied to reduce the sampling rate of the ADC and improve the Signal-to-Noise Ratio (SNR). Our targeted input signal bandwidth is 100KHz which is suitable for low-speed sensor readout and audio applications. The oversampling rate and the oversampling clock are configurable up to 1024 and 50MHz, respectively.

The design has been implemented using open-source EDA tools and Google Skywater 130nm opensource PDK. The main challenge in this work is to design the VCO with high linearity, which affects the overall ADC performance. The VCO are fully customized with eleven cross-coupling inverters specially tuned for high linearity from 2MHz to 10MHz. It has been simulated using an open-source simulator (Ngspice) and laid out in Magic. Additionally, the digital parts, including the phase readout and CIC filter along with a Wishbone bus Interface to read out the captured data in the two SRAMs, are implemented using Openlane – an RTL-to-GDS flow. The VCO occupies a small area of 3520µm^2 while the digital part takes 73,000 µm^2. The post-layout simulation shows that our VCO-based ADC can achieve 10-bit ENOB with the input voltage Vpp = 0.8V and SNDR = 58.6dB with the supply voltage VDD = 1.8V.

This work reused many IPs from the open-source hardware design ecosystem on Skywater 130nm for tapeout to shorten the design time. For example, the pad rings, the management SoC and the PLL are reused from the Caravel Test Harness, while the SRAM macros are from the OpenRAM project. Thanks to the open-source ecosystem, we can complete this project from concept to layout in two months without knowing these EDA tools in advance. Fig. 2 presents the final layout of the Caravel User Project Wrapper, which contains three VCO-based ADC with different configurations for testing. Our project has been public with an open-source license at https://github.com/duyhieubui/caravel_vco_adc. The future works will improve the ADC performance improvement and add more complex architectures.

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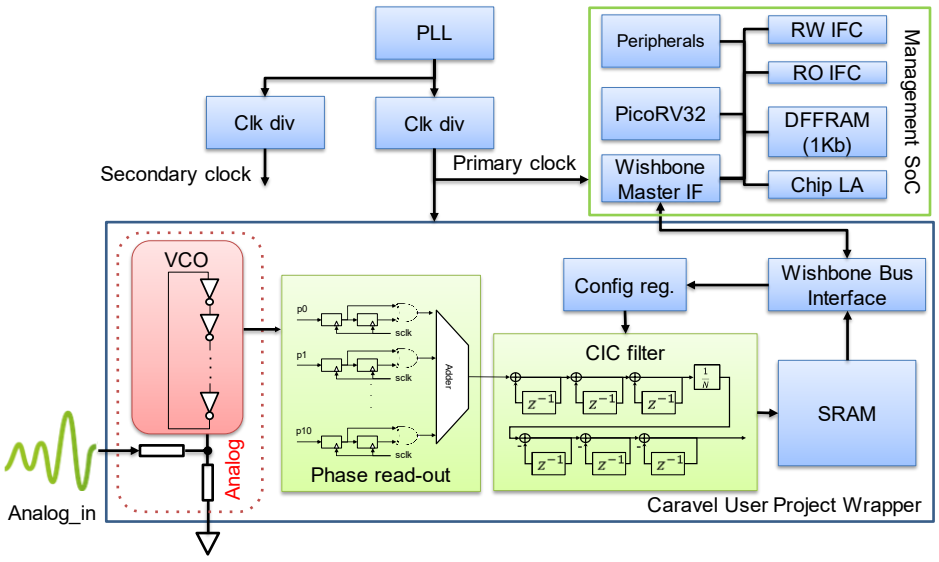

Fig. 1. VCO-based ADC block digram with the test System-on-Chip.

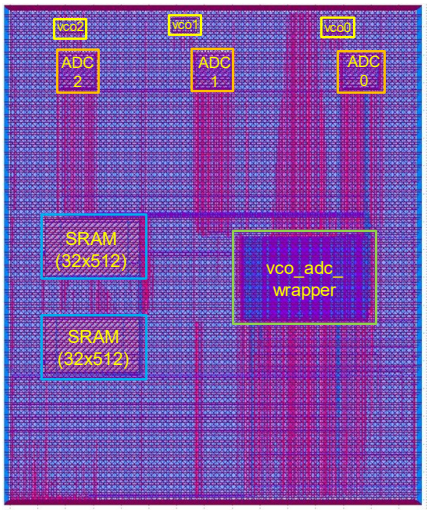

Fig. 2. Layout of the system for tapeout which includes three VCO-based ADCs, a test controller and SRAM for data storage.