Job Descriptions

We, Viettel IC Design Center with an ambition to design world-class Chipsets for 5G and AI applications. These are the very first chipset products of Vietnam.

Chipset (System on chip – SoC) is the most complicated component in every high-tech devices such as mobile phones, cameras, robot, control units in cars, smart TV, computers,…

The trade-war between US and China has raised a big wave of attention in this Chip industry, which has been silently the true core of the high-tech industries for year (the Silicon valey started its own name based on the chip industry). China and Huawei has clearly lost this war due to the chipset sunction from US.

Vietnam has cherished the chipset dream for years. During the hard day after 1975, Vietnam started the first group to do some research about the BJT components. In lately 1980s, a group was found in Hanoi to design the computer from chip level up to the device level. Two of the key members of that team are the founder and the current the CEO of CMC, one of the largest IT companies in Vietnam. During 2000s, ICDIREC was found in HCMC with large amount of government financial support to restart this chipset ambition. However, unfortunately, the result of ICDIREC was not adequated to its original expectation.

There are multiple reasons for the failures in the past. However, following are the main ones:

- No market vision
- So-so or low-end chipset product
- Low-end technologies to design the chip
- No commitment for a longterm investment
- No ecosystem to integrate the chips
- Not intention for commercialization, but for political purpose mainly.

With Viettel SoC, we will leave all these above reasons behind, heading toward the success with a 5G, AI IoT market vision. Our chipset is defined to be of worldclass. We have a very long term investment and a good ecosystem. The target of this project is not only to trigger the semiconductor industry of Vietnam, but also to get money from it.

In order to achieve that goal, we need enthusiastic and ambitious engineers to join us together to make the dream come true. We need people from entry level to senior level for jobs of:

- RTL/FPGA
- Algorithms (5G, AI, communications)
- CPU architecture
- Design For Test
- Firmware
- Verification
- Layout
- Embedded system

Please send email to viettel.vic@gmail.com (we use gmail in case our Vietel emails filter out free emails). Please find more job details as follows:

1. RTL/FPGA
    a. Responsible
        - Design HW (RTL) for FPGA and ASIC for either of the following categories:
            - (5G, AI, communications) algorithms.
            - HW blocks of the chip such as high-speed interface (Ethernet, PCIe, CPRI, JESD,…), controllers, bus system, memory system, security systems,…
            - CPU/DSP subsystem such as caches, MMU, IO interface, interrupt controller, …
        - Optimize the RTL, partition jobs between HW and Software to achieve the desired performance.
    b. Qualification
        - RTL experience (FPGA, ASIC)
        - TOEIC 550 (for those of less than 5 year experience)
        - CPA >2.8 (for newbie)
    c. Opportunities
        - Get trained by top-notch senior engineers.
        - Work on the full chip instead of sub module like in outsourcing companies. This helps engineer to broaden and to deepen skills and knowledge.
        - Opportunities to learn CPU, DSP architecture, to extend knowledge in multiple fields.
        - High-end FPGA and advanced tool flow for development.
        - Open-minded and flatten environment, top 15% income in the industry, many opportunities for long-term developments.
2. Algorithms
    a. Responsible
        - Work on 5G, AI and communications algorithms in Matlab/Python/C. Collaborate with the HW team (RTL/DSP) to validate the algorithms in the system.
        - Optimize the algorithms, partition jobs between HW and Software to achieve the desired performance.
    b. Qualification
        - Good at math (linear algebra)
        - Good at Matlab/Python/C.
        - Eager to think out of the box.
        - TOEIC 550 (for those of less than 5 year experience)
        - CPA >2.8 (for newbie)
    c. Opportunities
        - Challenging jobs with no scope limit.
        - Get trained by top-notch senior engineers in the field.
        - Opportunities to learn DSP architecture, extend knowledge in the field.
        - High-end system for 5G, AI, IoT to speed up the design and validation process.
        - Open-minded and flatten environment, top 15% income in the industry, many opportunities for long-term developments.
3. CPU architecture
    a. Responsible

- Develop CPU/DSP architecture for controlling and signal processing applications (5G, AI,..)
    - Modeling the CPU architect and instruction set.
    - Simulate the Instruction Set.
    - Work on the embedded software to evaluate the performance of the core.
    - Design the IO interface for the core.
    - Design the memory subsystem for the core.
    - Integrate the core into the SoC system.
- Optimize the CPU/DSP core in both the simulation environment and the emulation system.
- HW-SW co-development engagement.

b. Qualification
- Knowlegable in CPU architecture.
- Eager to learn new things.
- Good at C or RTL.
- Knowlegable in both HW and SW.
- TOEIC 550 (for those of less than 5 year experience)
- CPA >2.8 (for newbie)

c. Opportunities
- Work in the world-class CPU/DSP core design flow.
- Get trained by top-notch senior engineers.
- Opportunities to extend knowledge in both the HW and SW world, from compiler to DSP algorithms or Linux.
- Open-minded and flatten environment, top 15% income in the industry, many opportunities for long-term developments.

4. Design for test engineers

a. Responsible
- Work with the system team and the RTL teamd to develop the DFT specifications.
- Develop and implement DFT architecture and infrastructure.
- Develop the debug methodologies.
- Work with the DV team too verify the DFT implementation.
- Generate structural test vectors, analyze and improve the coverage/test time/test cost.

b. Qualification
- Experience in DFT specification development
- Experience in ATPG/MBIST pattern
- Experience in STA constraints for DFT
- TOEIC 550 (for those of less than 5 year experience)
- CPA >2.8 (for newbie)

c. Opportunities
- Work on the full chip instead of sub module like in outsourcing companies. This helps engineer to broaden and to deepen skills and knowledge.
- Get trained by top-notch senior engineers.

- Commercialized DFT full flows from DFT compiler to DV, STA flows.
- Open-minded and flatten environment, top 15% income in the industry, many opportunities for long-term developments.

5. Firmware engineers
    a. Responsible
        - Develop firmware subsytem for the CPU designed by the team.
        - Develop the firmware engines for peripheals to communicate with other chipset (SPI, I2C, UART, interrupt controller, timers, WDT,…, high-speed interfaces such as DDR, PCIe, Ethernet, CPRI,…).
        - Develop the API, SDK for the CPU core.
        - Develop the Linux kernels for the CPU core.
        - Customize the Linux tool chain for the CPU.
        - Work with the CPU compiler to optimize the code.
    b. Qualification
        - Experience in firmware development for micro controllers.
        - Skills in C/C++.
        - Eager to learn new things.
        - TOEIC 550 (for those of less than 5 year experience)
        - CPA >2.8 (for newbie)
    c. Opportunities
        - Work on the full chip instead of sub module like in outsourcing companies. This helps engineer to broaden and to deepen skills and knowledge.
        - Work in the high-end HW-SW codevelopment flows with emulation system.
        - Get trained by top-notch senior engineers.
        - Open-minded and flatten environment, top 15% income in the industry, many opportunities for long-term developments.
6. Verification engineers
    a. Responsible
        - Develop test cases and scenarios for modules and full chip.
        - Build the UVM environements with sequencer, scoreboard and coverage engines.
        - Utilize the VIPs and combine the in-house UVM environment with the commercial VIPs.
        - Work on the emulation system such as HAPS and Zebu to speed up the verification process.
    b. Qualification
        - Experience in UVM.
        - Experience in System Verilog/Verilog.
        - Eager to learn new things.
        - TOEIC 550 (for those of less than 5 year experience)
        - CPA >2.8 (for newbie)
    c. Opportunities
        - Work on the full chip instead of sub module like in outsourcing companies. This helps engineer to broaden and to deepen skills and knowledge.
        - Work in the high-end verification flows with emulation system.

- Get trained by top-notch senior engineers.
- Open-minded and flatten environment, top 15% income in the industry, many opportunities for long-term developments.

7. Layout engineers
    a. Responsible
        - Process technology file management.
        - Physical Implementation Environment Setup.
        - SDC (Synthesis Design Constraints) analysis and debug
        - Netlist analysis and feedback to the design team.
        - Floorplanning for the layout
        - Place cell optimization and timing analysis
        - Clock tree synthesis and timing analysis
        - Routing optimization and timng analysis
        - Timing , power, crosstalk debug and optimization
        - LEC, DRC and LVS checking
        - IO placement, bumping and RDL routing.
    b. Qualification
        - Knowledgable in digital electronics such as Flip Flops, logic gates, clock buffers,....
        - Basic knowledge in CMOS.
        - Basic knowledge in analog circuits is a plus.
        - Interested in script programming (tcl for example).
        - Eager to learn new things.
        - TOEIC 550 (for those of less than 5 year experience)
        - CPA >2.8 (for newbie)
    c. Opportunities
        - Work on the full chip instead of sub module like in outsourcing companies. This helps engineer to broaden and to deepen skills and knowledge.
        - Engaged in one of the most interesting parts in the Chip design process. This part is the final part, which is the most visualized step that allows us to see the full chip design before the manufacturing.
        - Work in the full commercial backend design flow.
        - Get trained by top-notch senior engineers.
        - Open-minded and flatten environment, top 15% income in the industry, many opportunities for long-term developments.
8. Embedded System engineers
    a. Responsible
        - Develop the HW and SW system for the SoC of Viettel. The task includes but not limit to
            - PCB design for the Viettel SoC and other chips to form a completed system.
            - Firmware and debugging enviroment development.
            - Software tool chain for testing automation (PC communicates with the test board, testing equipment like VSA, spectrum analyzer,..).
            - Develop test cases and test scenarios.

- Do the chip characterizations.

b. Qualification
   - Hands-on skills in PCB design.
   - Controller programming experience is a plus.
   - Eager to learn new things.
   - TOEIC 550 (for those of less than 5 year experience)
   - CPA >2.8 (for newbie)

c. Opportunities
   - Work on the full SoC characterization system with multiple fileds involved.
   - Opportunities to broaden and strengthen skills and experiences in the embedded system world involving both HW and SW.
   - Work in advanced design and simulation flows for signal integrity, power integrity check.
   - Get trained by top-notch senior engineers.
   - Open-minded and flatten environment, top 15% income in the industry, many opportunities for long-term developments.