METU Computer Engineering

Ceng 111 – Fall 2021
Week 3a

Digital Computation

Credit: Some slides are from the “Invitation to Computer Science” book by G. M. Schneider, J. L. Gersting and some from the “Digital Design” book by M. M. Mano and M. D. Ciletti.

An example problem: Water Tank

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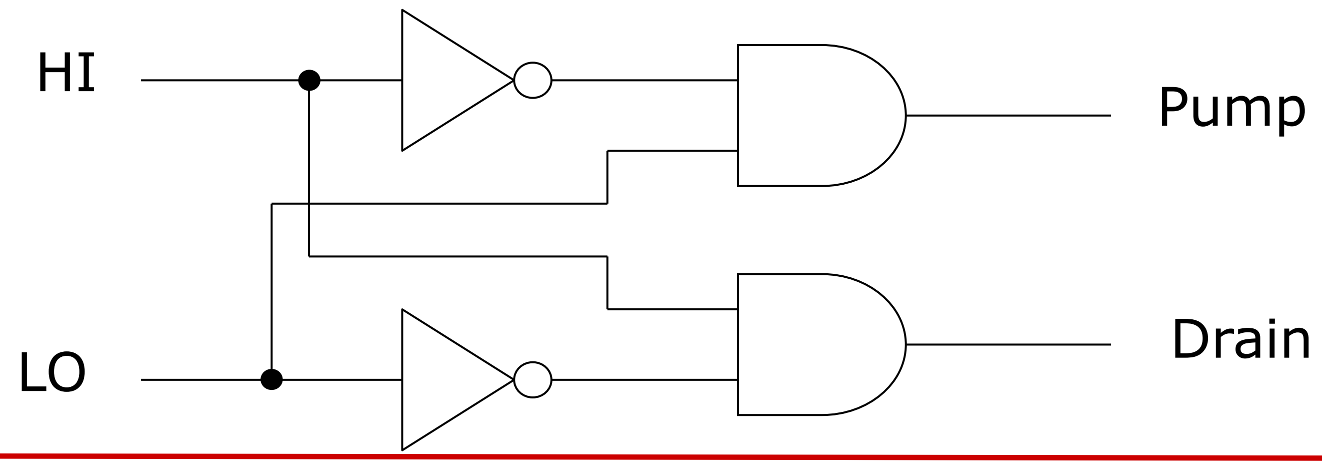
HI	LO	Pump	Drain	
0	0	0	0	Tank level is OK
0	1	**1**	0	Low level, pump more in
1	0	0	**1**	High level, drain some out
1	1	x	x	Inputs cannot occur

Truth Table Representation

Schematic Representation



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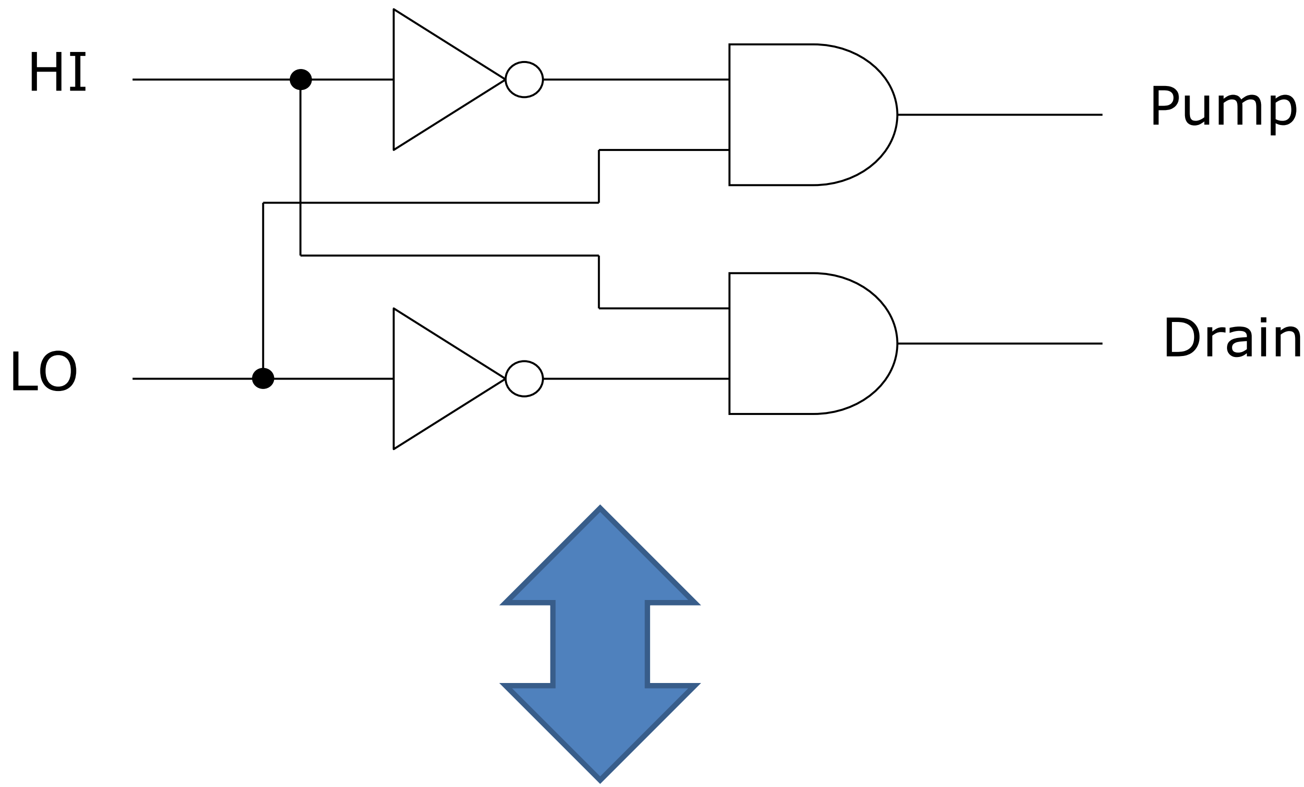
Boolean Logic/Algebra



Pump = HI’.LO
Drain = HI.LO’

Boolean formula describing the circuit.

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The binary addition

$$\begin{array}{r} 0 \\ +0 \\ \hline 0 \end{array} \qquad \begin{array}{r} 1 \\ +0 \\ \hline 1 \end{array} \qquad \begin{array}{r} 0 \\ +1 \\ \hline 1 \end{array} \qquad \begin{array}{r} 1 \\ +1 \\ \hline 10 \end{array}$$

Question (Binary notation) : 111010 + 11011 = ?

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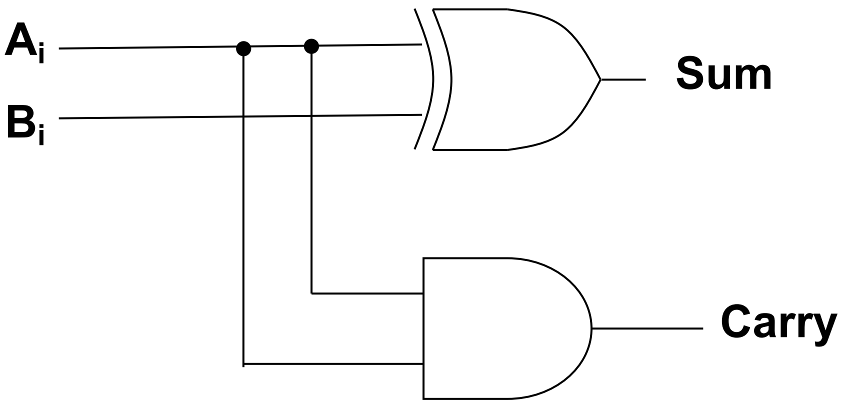
1-bit Half-adder

A_i	B_i	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



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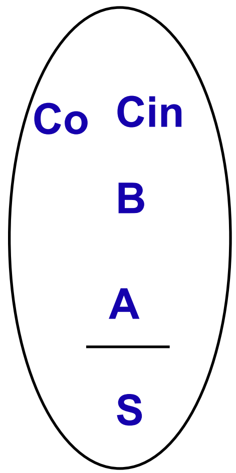
1-bit full-adder

```
      1
    0 0 1 1
+   0 0 1 0
  ---------
    0 1 0 1
```



A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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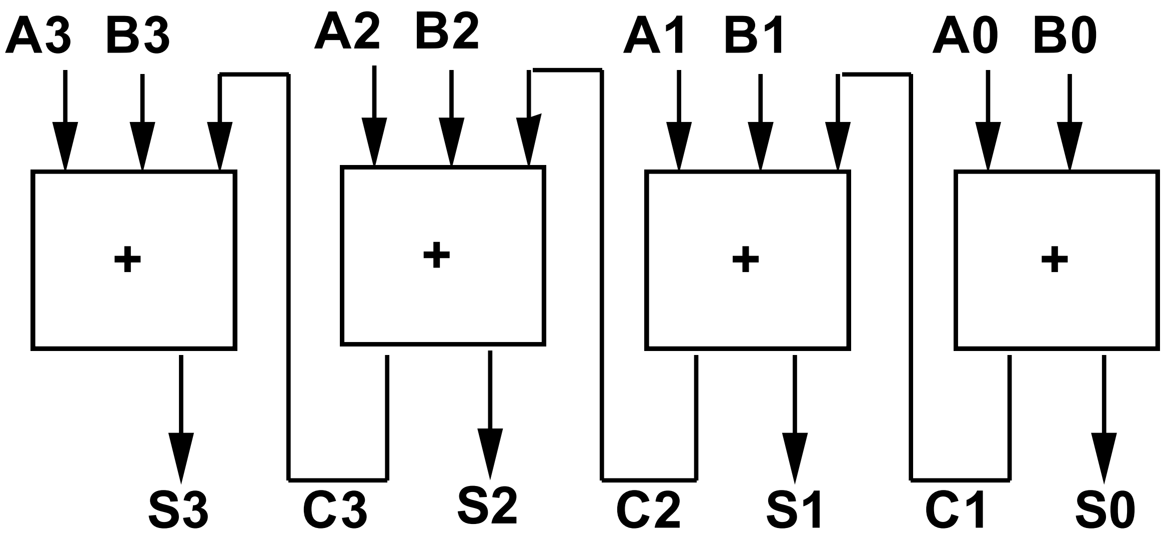
N-bit Adder



Today

- Computer Organization
  - CPU
  - Memory
  - Fetch-decode-execute cycle

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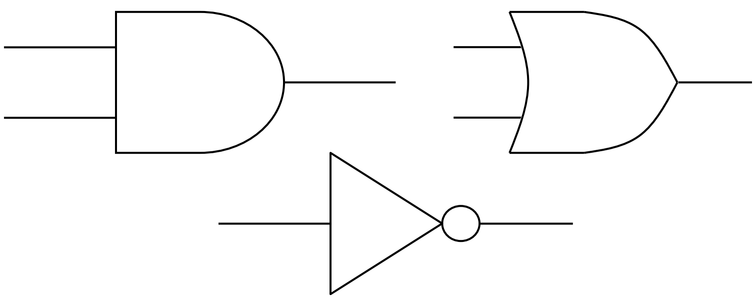
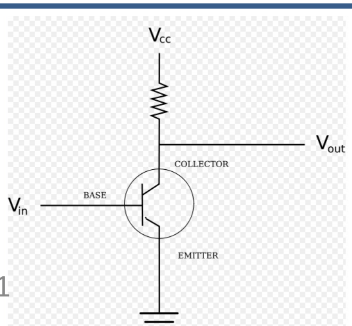
Today

Devices



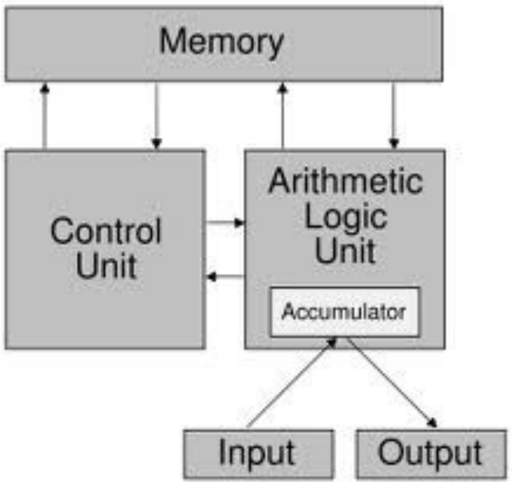
Gates



Transistors

Administrative Issues

- Busy hours for lab schedule
- Quiz



Computer Organization

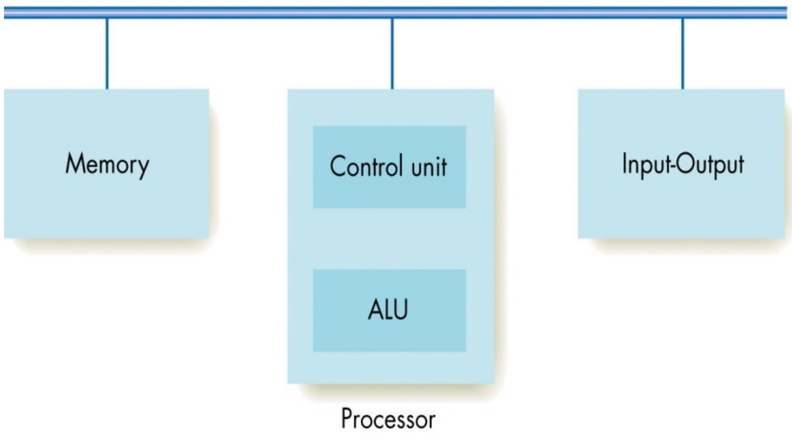
VON NEUMANN ARCHITECTURE & ITS IMPLEMENTATION

Von Neumann Architecture & Its Implementation

- How are instructions coded?
- How are instructions executed?
- How do the different subcomponents interact?
  - Memory
  - ALU
  - The Bus System
  - Registers

The Components of a Computer System

- Von Neumann architecture has four functional units:
  - Memory
  - Input/Output
  - Arithmetic/Logic unit
  - Control unit



- Sequential execution of instructions
- Stored program concept

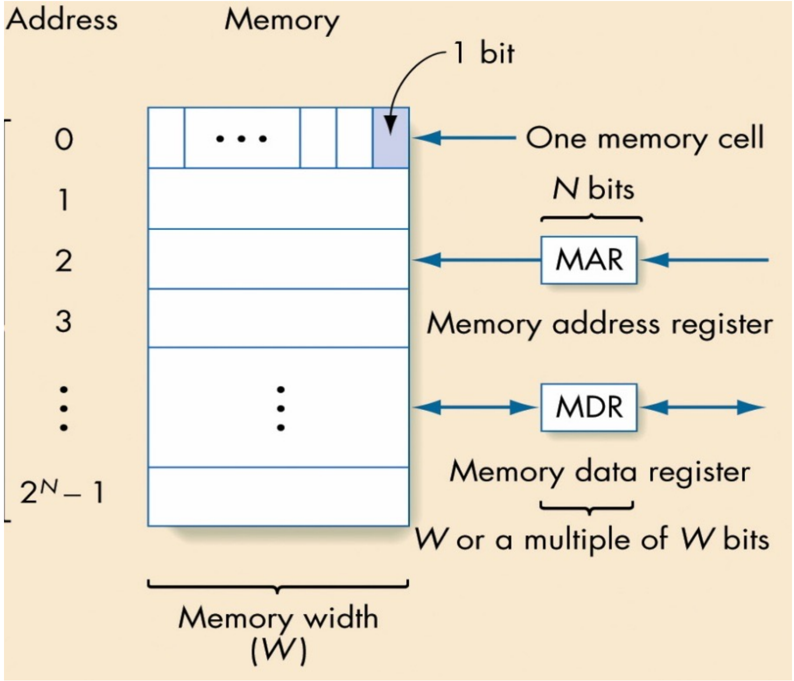
Instruction Execution

Memory and Cache

- Information is stored and fetched from memory subsystem
- Memory maps addresses to memory locations
- Cache memory keeps values currently in use in faster memory to speed access times

Memory and Cache (continued)

- RAM (Random Access Memory)
  Often called *memory*, *primary memory*
  - Memory made of addressable "cells"
  - Cell size is 8 bits
    - Nowadays, it is 32 or 64 bits.
  - All memory cells accessed in equal time
  - Memory address
    - Unsigned binary number with N bits
    - Address space is then 2^N cells



Memory and Cache (continued)

- Rapid access, low capacity “warehouse”
- Retains information entered through input unit
- Retains info that has already been processed until can be sent to output unit

Memory and Cache (continued)

- Parts of the memory subsystem
  - Fetch/store (or Read/Write) controller
    - Fetch: retrieve a value from memory
    - Store: store a value into memory
  - Memory address register (MAR)
  - Memory data register (MDR)

Memory and Cache (continued)

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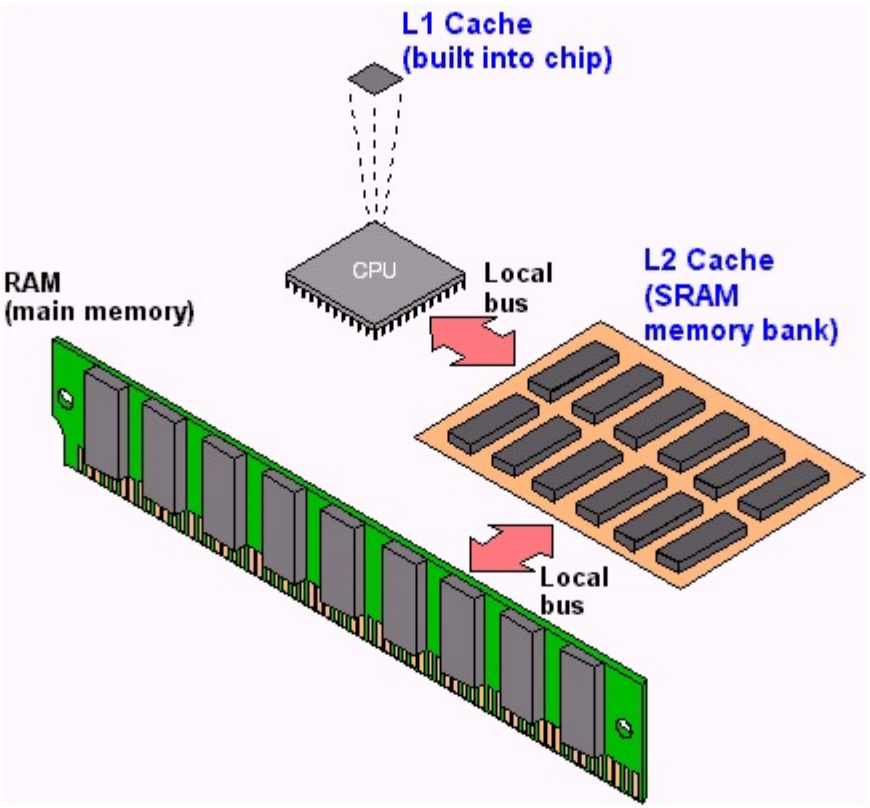
- Fetch operation
  - The address of the desired memory cell is moved into the MAR
  - Fetch/store controller signals a “fetch,” accessing the memory cell
  - The value at the MAR’s location flows into the MDR

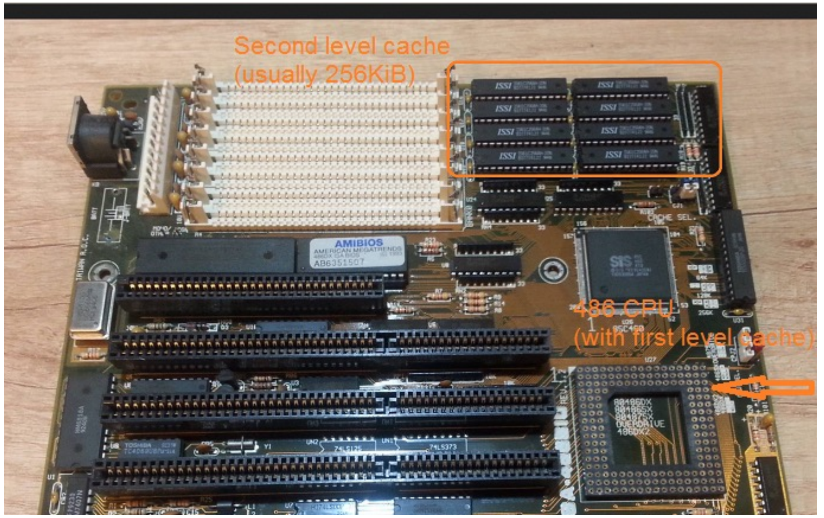
Memory and Cache (continued)

- Store operation
  - The address of the cell where the value should go is placed in the MAR
  - The new value is placed in the MDR
  - Fetch/store controller signals a “store,” copying the MDR’s value into the desired cell

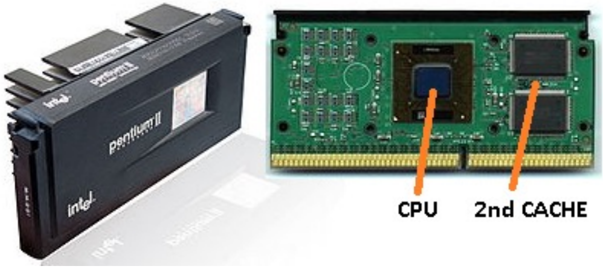
Cache Memory

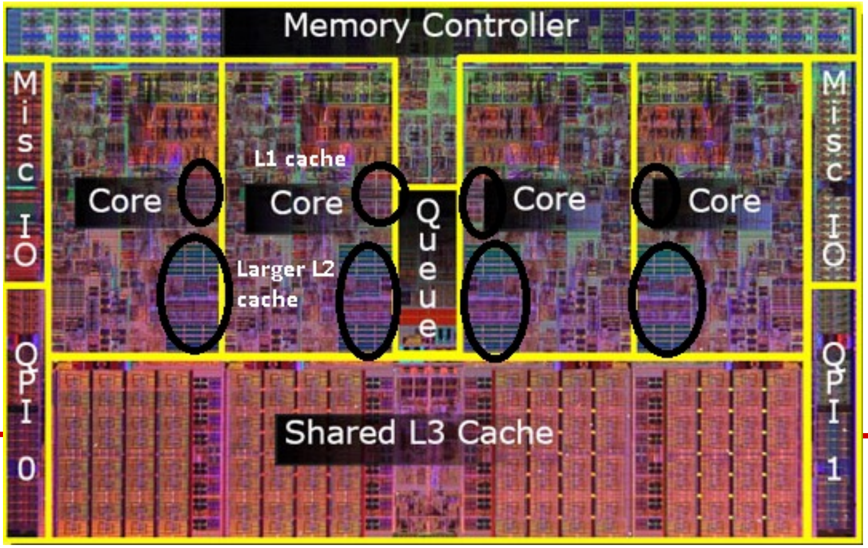
- Memory access is much slower than processing time
- Faster memory is too expensive to use for all memory cells
- Locality principle
  - Once a value is used, it is likely to be used again
- Small size, fast memory just for values currently in use speeds computing time


L1 Cache
(built into chip)
CPU
Local
bus
L2 Cache
(SRAM
memory bank)
RAM
(main memory)
Local
bus


Second level cache
(usually 256KiB)
486 CPU
(with first level cache)

80486: (1989)


CPU
2nd CACHE


Memory Controller
Misc IO
Core
Core
Core
Core
L1 cache
Larger L2 cache
Queue
Misc IO
QPI 0
QPI 1
Shared L3 Cache