EG 301-Q2-April-2024 [#1706]

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Test Start Time	4/17/2024, 2:00:34 PM
Marks Scored	60.0 / 60.0
Total Questions	21
Attempted Questions	21
Correct Questions	20
Incorrect Questions	1
Skipped Questions	0
Pending Evaluation	0

Answer Key

No answer key available for this test. Please contact your exam division/cell.

List of Sections

Section - 1 Marks per question : 3.0 **Marks Scored : 60.0** (20 questions with the highest score selected out of 21) Negative marks per question : 33%

Q No.	Q. Type	Status	Marks	
1	Multiple Choice - Single Answer	✔	3.0	Hide Answer

Consider this code

```
int * p = malloc(sizeof(int));
printf("%p",p);
```

What is printed when this program is run?

- (●) An address in the virtual address space of the process
- ( ) The address in the physical RAM where there memory was allocated
- ( ) The address of the variable p
- ( ) Nothing is printed. This code causes segmentation fault core dumped.

2	Multiple Choice - Single Answer	✔	3.0	Hide Answer

On a modern OS like Linux, a user compiles code so that it's address references

in the compiler output (a.out) are the same as those seen by the *process* when
it is executing. If a.out contains an instruction STORE ax, 0x55f00a (store contents of register ax in address 0x55f00a)

then which of these is true?

- the seen address needs no translation
- the seen address needs to be translated by the MMU
- the seen is the address generated by the MMU
- the seen address is a physical address

3 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

Which of the following is true about the number of page tables in an OS

- It is one per process
- It is one per process group
- It is one per thread
- It is one per user

4 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

In system using paging which of the following is true about the page frame

- Page frame refers to a fixed size of memory in the virtual address space of the process
- The page frame number is used to index the page table and retrieve the PTE
- The frame number is stored in the PTE, hence retrieved from the PTE
- The frame number is available in the compiled executable

5 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

The page table contains

- One entry per cache line
- One entry per per process
- One entry per virtual address used in the program
- One entry per virtual page used in the program

6 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

A TLB is a

- cache for process data
- cache for process code

- ◉ cache for process PTEs
- ○ cache for process run time stack

7 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

TLB is usually located

- ○ In the RAM
- ○ On the disk
- ◉ In the CPU
- ○ In the ALU

8 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

Here is part of a sample session on Linux showing regions or virtual memory areas of a process:
$ pmap `pidof ./address`
8762: ./address
0000abcd12341000 4k r---- address
0000abcd12342000 4k r-x-- address
...
0000abcd12348000 4k rw--- address
...
000055cd123bc000 8k rw--- [anon]
....

Assume pages and frames of size 4k. Which of these is true

- ○ 0000abcd12341000 is the address of a physical location in RAM containing some read only data
- ○ 0000abcd12341 is the frame number for the page containing 0000abcd12341024
- ◉ 0000abcd12341 is the Virtual Page number (VPN) used to index the PTE for the virtual address 0000abcd12341024
- ○ 0000abcd12341000 is a virtual page containing the stack for the process

9 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

The pmap command on Linux reports the memory map of the given process.
In the output of pmap for any process which of the following holds:

- ○ Each region occupies exactly one frame
- ○ Each region has one entry in the PTE
- ◉ There is no indication of which physical frame any address corresponds to
- ○ Successive pages are always in successive frames

10 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

A certain MMU supports simple segmentation with the usual four segments. Which of these hold:

- ◉ The virtual address is split into segment selector and offset

- A base register contains a virtual address and bound register the valid extent of the segment
- Two bits of the physical address are used to select the segment base register
- The contents of the bound register is added to the offset to get the physical address

11 | Multiple Choice - Single Answer | ✔ | 3.0 | Hide Answer

External fragmentation in simple segmentation refers to the fact that:

- The more page frames we have in physical memory, the more fraction of memory remains unusable
- We may have sufficient RAM, but there is difficulty in finding continuous physical address space for a segment
- In most cases not all of the allocated segment for a process is actually used.
- Belady's anomaly is likely to occur as we have more physical frames available.

12 | Multiple Choice - Single Answer | ✔ | 3.0 | Hide Answer

Assume a system uses virtual and physical addresses that are 64bits long. Assume it uses paging with 4k page and frame size. Which of these is true:

- Offset should be 10 bits
- Physical frame number is likely to be 52 bits long
- The least significant 52 bits of the virtual address are used as index to the page table
- The frame number/address is 12 bits long

13 | Multiple Choice - Single Answer | ✔ | 3.0 | Hide Answer

A system uses paging. Consider this instruction: STORE ax, 0x55f00a (store contents of register ax in address 0x55f00a)
Assuming 4K page and frame size, which of the following is true:

- 0x55f00a is the physical location to store the content of ax
- The VPN (virtual page number) is 0x55f
- The PFN (physical frame number) is 0x55f
- The virtual address is 0x55f000 plus the offset returned by the PTE

14 | Multiple Choice - Single Answer | ✖ | -1.0 | Hide Answer

The TLB is often implemented with a fully associative cache / Content-addressable memory and contains:

- Both VPN and PTE for each virtual page
- Only the PTE since the VPN is used as an index to the PTE
- Only the PFN since the VPN is part of the address anyway
- Only the VPN

15 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

When a TLB miss happens, it means that:

- the address accessed is invalid
- the corresponding address has data/instruction that is not cached in the CPU
- that the corresponding PTE is missing from the RAM
- that the corresponding PTE is not cached

16 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

On a system with demand paging, assume a program is correctly written and all virtual address is valid. Which of these is true:

- When a TLB miss occurs, a segmentation fault will also occur
- When a TLB miss occurs, a page of the process is loaded into the TLB
- When a page fault occurs, a page of the process will be loaded from the disk and TLB updated
- When a page fault occurs, the TLB will be updated but no page loaded from the disk

17 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

When we say a system supports demand paging we mean

- The system prioritizes those processes to run that demand pages more often
- Whenever the process demands more memory (like using malloc) then it gets the memory immediately
- Most process pages are brought into memory only when their content is accessed
- Page frames are not initially allocate to a process, it needs to execute a system call demanding more memory before it gets it

18 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

Belady's anomaly says that for a given process and a simple page replacement strategy like FIFO:

- More physical frames on the system always reduce the number of page faults that occur
- More physical frames can sometimes increase the number of page faults that occur
- More physical frames always increase the number of page faults that occur
- If the number of frames is larger than the number of pages then it increases the possibility of page faults

19 Multiple Choice - Single Answer ✔ 3.0 Hide Answer

The dirty bit (or modified bit) in the PTE helps so that:

- The cost of swap-in is reduced

- [x] We incur the cost of swap-out only when the bit is set to dirty
- [ ] Pages which have the dirty bit set are only loaded into the frame
- [ ] When the dirty bit is not set, then we are sure the PTE is in the MMU so we don't have to update the TLB

20 | Multiple Choice - Single Answer | ✔ | 3.0 | Hide Answer

Linear page table storing is not preferred because

- [ ] Accessing linear page tables is complicated and needs sophisticated hardware support
- [ ] Linear page tables are slow
- [ ] The memory regions of a process are in contiguous(continuous) pages
- [x] Linear page tables are too large and waste a lot of space in the RAM

21 | Multiple Choice - Single Answer | ✔ | 3.0 | Hide Answer

Which of these is an example of something common in an OS like Linux, but NOT supported by the CPU

- [x] CPU support for notion of a file descriptor
- [ ] CPU support for memory management using MMU
- [ ] CPU support for traversing the page table hierarchy during a TLB miss
- [ ] CPU support for kernel vs user mode execution