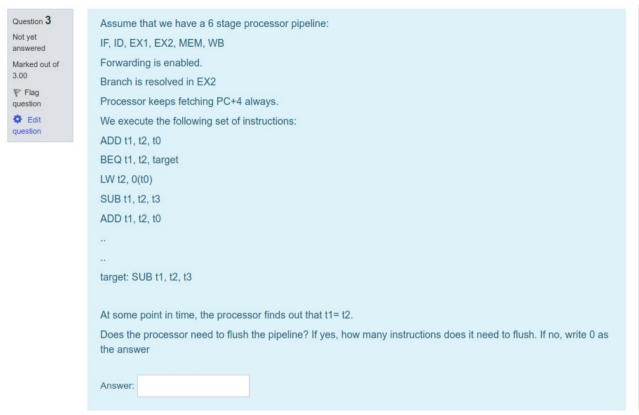
Quiz 5 Show the working in rough sheet for all questions



Question 2 Not yet answered Marked out of 4.00 Flag question	Assume that we are running the following instructions on a 5 stage MIPS pipeline. Assume that we can write and read registers in the same clock cycle. ADD t4, t2, t3 SW t4, 0(t2) BEQ t1, t4, target
Edit question	Which of the following statements are true? Select one or more:
	 a. No data forwarding required to Instruction 3 b. With forwarding, data needs to be forwarded from MEM of Instruction1 to MEM of Instruction3 c. With forwarding, data needs to be forwarded from EX of Instruction1 to MEM of Instruction2 d. With forwarding, data needs to be forwarded from MEM of Instruction1 to EX of Instruction3 e. No data forwarding required between any instructions f. With forwarding, data needs to be forwarded from EX of Instruction1 to EX of Instruction2 g. With forwarding, data needs to be forwarded from EX of Instruction2 to EX of Instruction3

Show the working in rough sheet



Show the working in rough sheet

```
Q4: (10 marks)
```

We have a six stage processor pipeline: IF, ID, EX, Mem1, Mem2, WB.

The data fetched from memory is available only after the Mem2 stage (for Loads). Branches are resolved in the EX stage. By default, the next instruction (PC+4) is always fetched.

The processor supports forwarding.

There are no structural hazards

The following instructions are executed on this processor in the same order.

```
LW R1, 0(R2)
BEQ R1, R2, target
ADD R2, R3, R4
Instr 6
Instr 7
Instr 8
```

Instr 9

Instr 10

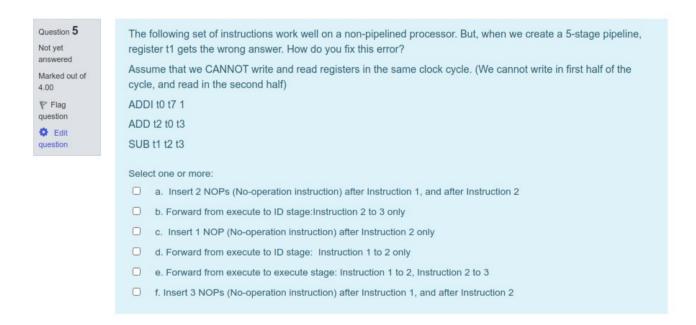
...

target: LW R1, 0(R2)

- - -

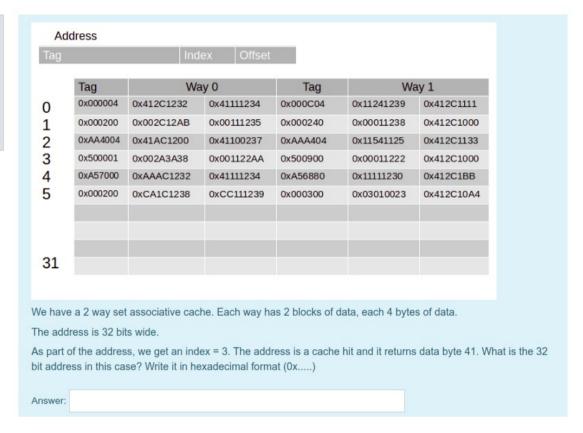
Question:

- a. Write the pipeline diagram for these instructions assuming that R1= R2 when BEQ executes. Assume that Instructions 6 to 10 are independent of each other with no hazards (5 marks)
- b. Indicate which register is forwarded, Indicate the from and to instruction. Indicate the from and to pipeline stage for forwarding (2 marks)
- c. If it needs a pipeline flush, how many instructions need to be flushed and which instructions are flushed (3 marks)

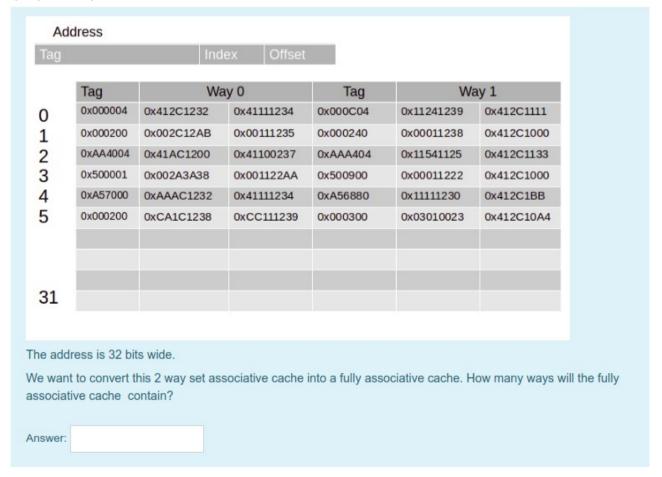


Question 6	We have a 5 stage MIPS processor pipeline with forwarding enabled.	
Not yet answered	Fill up the blank such that, the instruction will create one stall between Instruction 1 and 2	
Marked out of	Instruction 1:	
3.00	ADD t2, t4, t0	
√ Flag question	SUB t2, t2, t0	
\$ Edit	Select one or more:	
question	□ a. ADD t1, t4, t0	
	□ b. BEQ t4, t0, loop	
	□ c. LW t0, 0(t4)	
	☐ d. LW t4, 0(t0)	
	□ e. SW t4, 0(t0)	
Question 7	Assume that we have a 4-stage pipeline: IF, ID, EX/MEM, WB. All stages take 1 cycle to execute	÷.
Not yet	Assume that we are NOT allowed to write/read the registers in the same clock cycle.	
answered Marked out of	Does any hazard exist between the following set of instructions? If yes, identify the type of hazar	d.
3.00	ADDI to x0 1	
V Flag	SUB t1 t5 t3	
question Edit		
question	SW t2 0(t5)	
	BEQ t3, t5, target	
	"	
	Select one or more:	
	a. Control hazard	
	□ b. No hazard	
	□ c. Structural hazard	
	☐ d. Data hazard	
	O d. Data nazara	





Q9: (2 marks)



Q10: (2 marks)

	Way0	Way1	Way 2	Way3
)	M[0]	M[4]	M[8]	M[10]
,				

Assume the 4 way set associative cache. Tag is not shown in the cache. The Sequence of memory accesses are shown below in the same order. Addresses 0,4,8,10 and so on are in hexadecimal.

M[0]

M[4]

M[8]

M[10]

M[8]

M[8]

At this point, if the processor issues a load for memory address 0x18, which is, M[18] or M[11000], which of the following is true?

Let us assume a LRU replacement policy for this cache.

Select one or more:				
	a. M[18] is a cache miss			
	b. M[18] goes into Way 3			
	c. M[18] replaces M[0] and goes into Way 0			
	d. M[18] goes into Way 2			
	e. M[18] replaces M[4] and goes into Way 1			
	f. M[18] goes into a different index other than 0			
	g. M[18] is a cache hit			