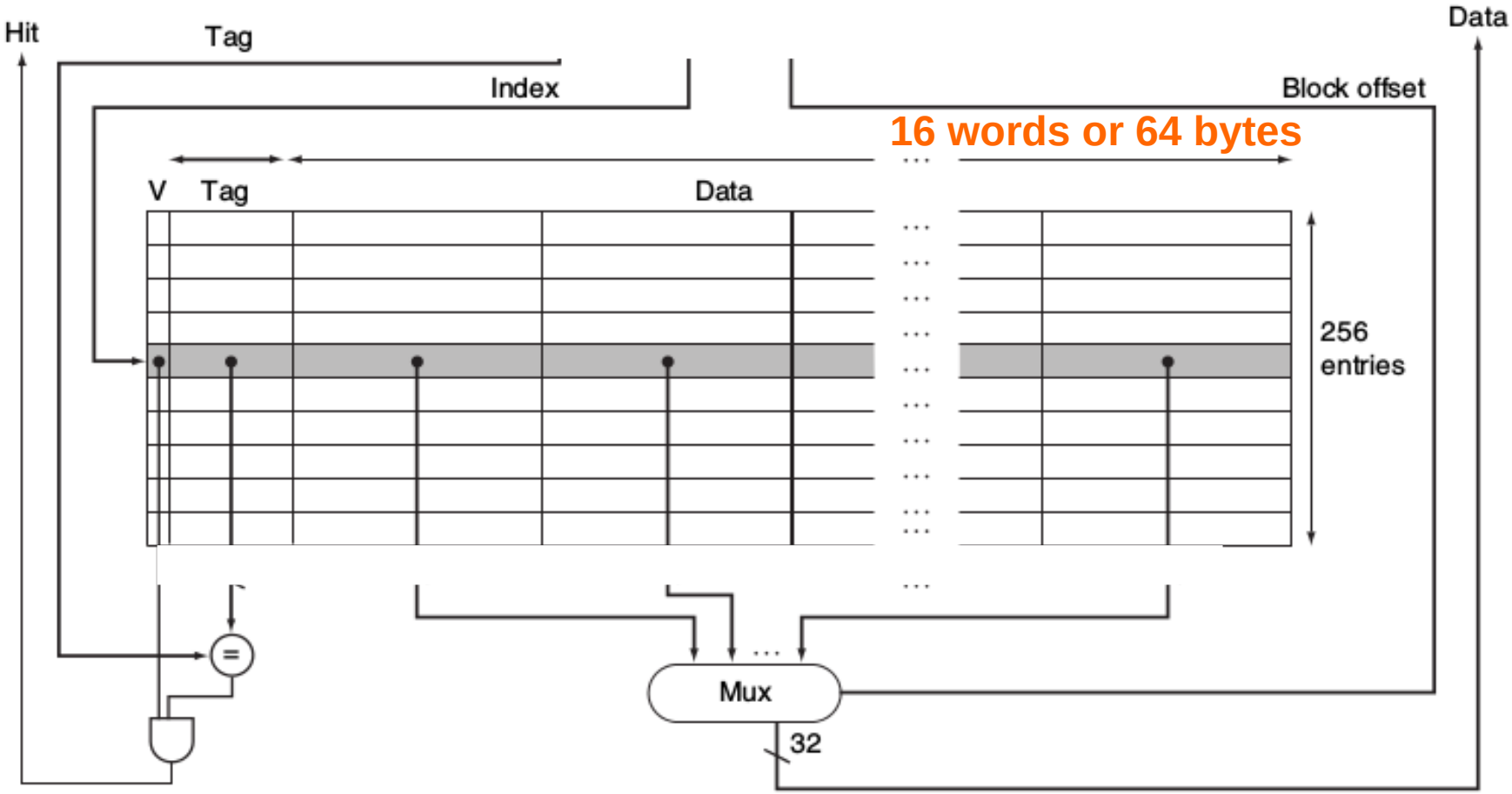
Q1: In this direct mapped cache, each block contains 64 bytes or 16 words.
How many bits does the following contain:
- Byte offset
- Index
- Tag



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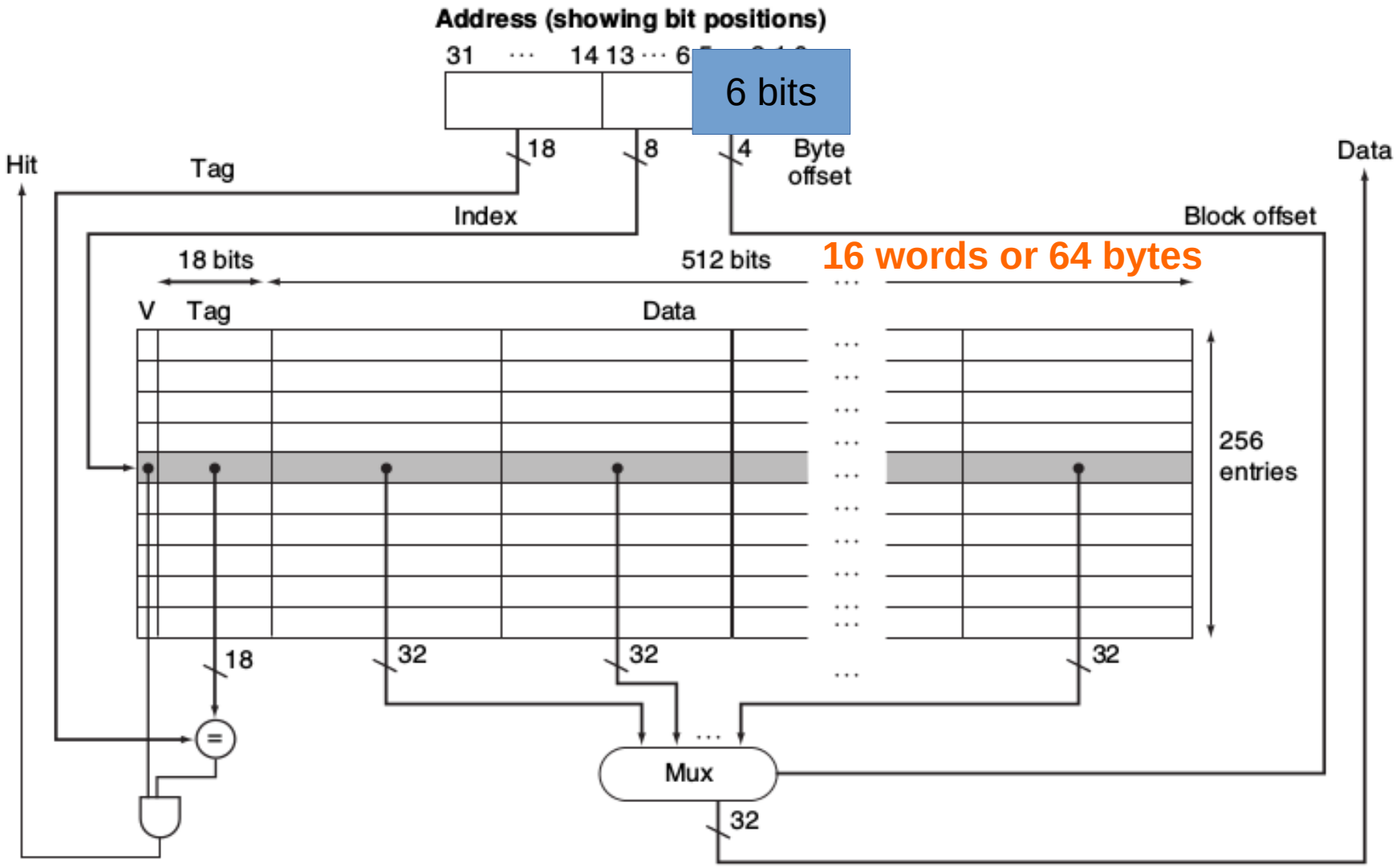
Solution



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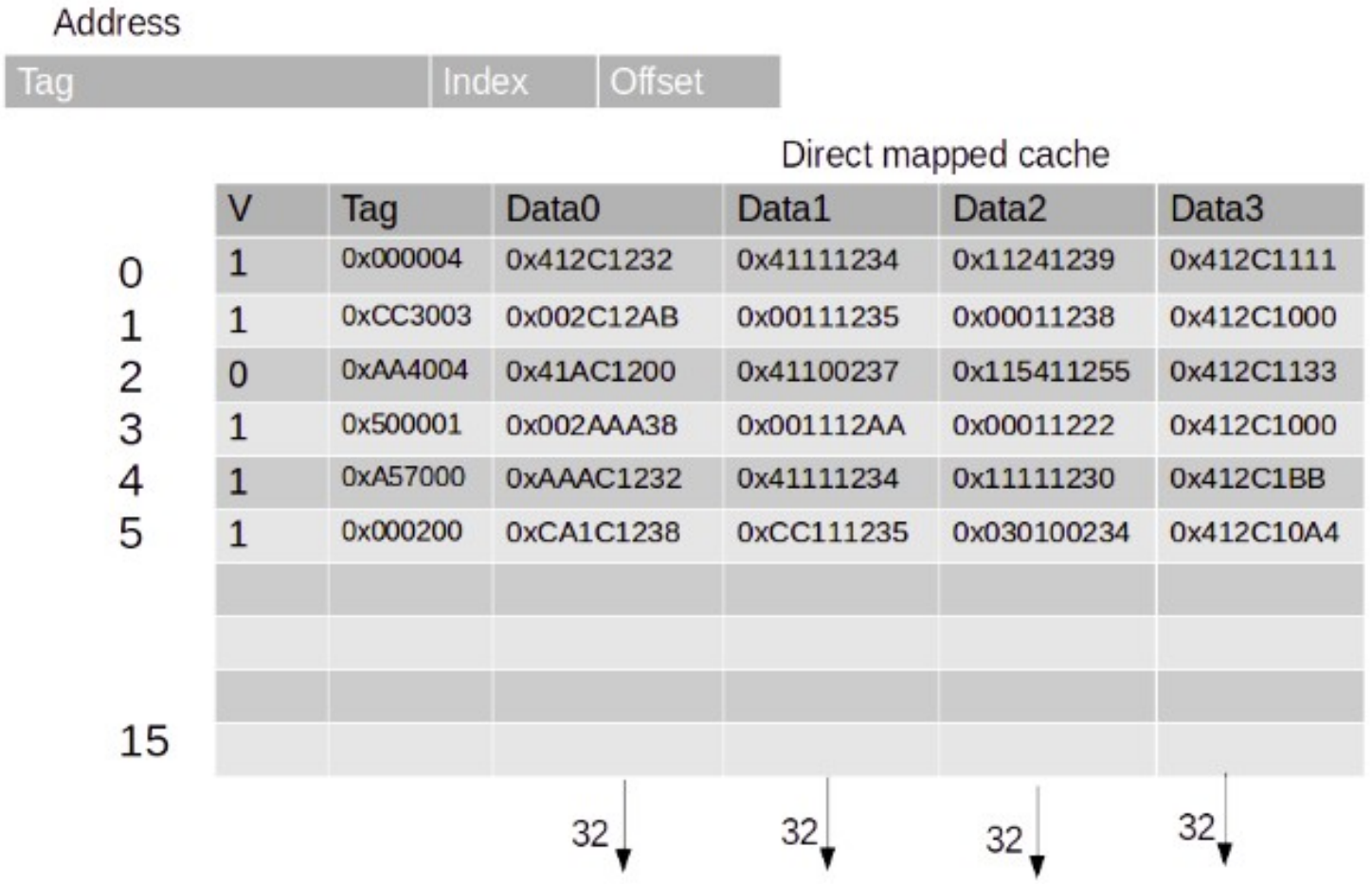


Q2 Consider a direct mapped cache which uses 4-word blocks, 32-bit data words (4 bytes) and 32-bit addresses.

Say you are trying to read data from memory location 0x00020013. Assume you are reading the bytes individually. What would be the:

Tag field value

Offset value

The cache line or block in which the data should be found

Is it a cache hit? If yes, what is the data that is read assuming a byte read?

Direct mapped cache

	V	Tag	Data0	Data1	Data2	Data3
0	1	0x000004	0x412C1232	0x41111234	0x11241239	0x412C1111
1	1	0xCC3003	0x002C12AB	0x00111235	0x00011238	0x412C1000
2	0	0xAA4004	0x41AC1200	0x41100237	0x115411255	0x412C1133
3	1	0x500001	0x002AAA38	0x001112AA	0x00011222	0x412C1000
4	1	0xA57000	0xAAAC1232	0x41111234	0x11111230	0x412C1BB
5	1	0x000200	0xCA1C1238	0xCC111235	0x030100234	0x412C10A4
15						

32 32 32 32

Soln:

Consider a direct mapped cache which uses 4-word blocks, 32-bit data words (4 bytes) and 32-bit addresses.

Address: 0000 0000 0000 0010 0000 0000 **0001** 0011 (0x00020013)

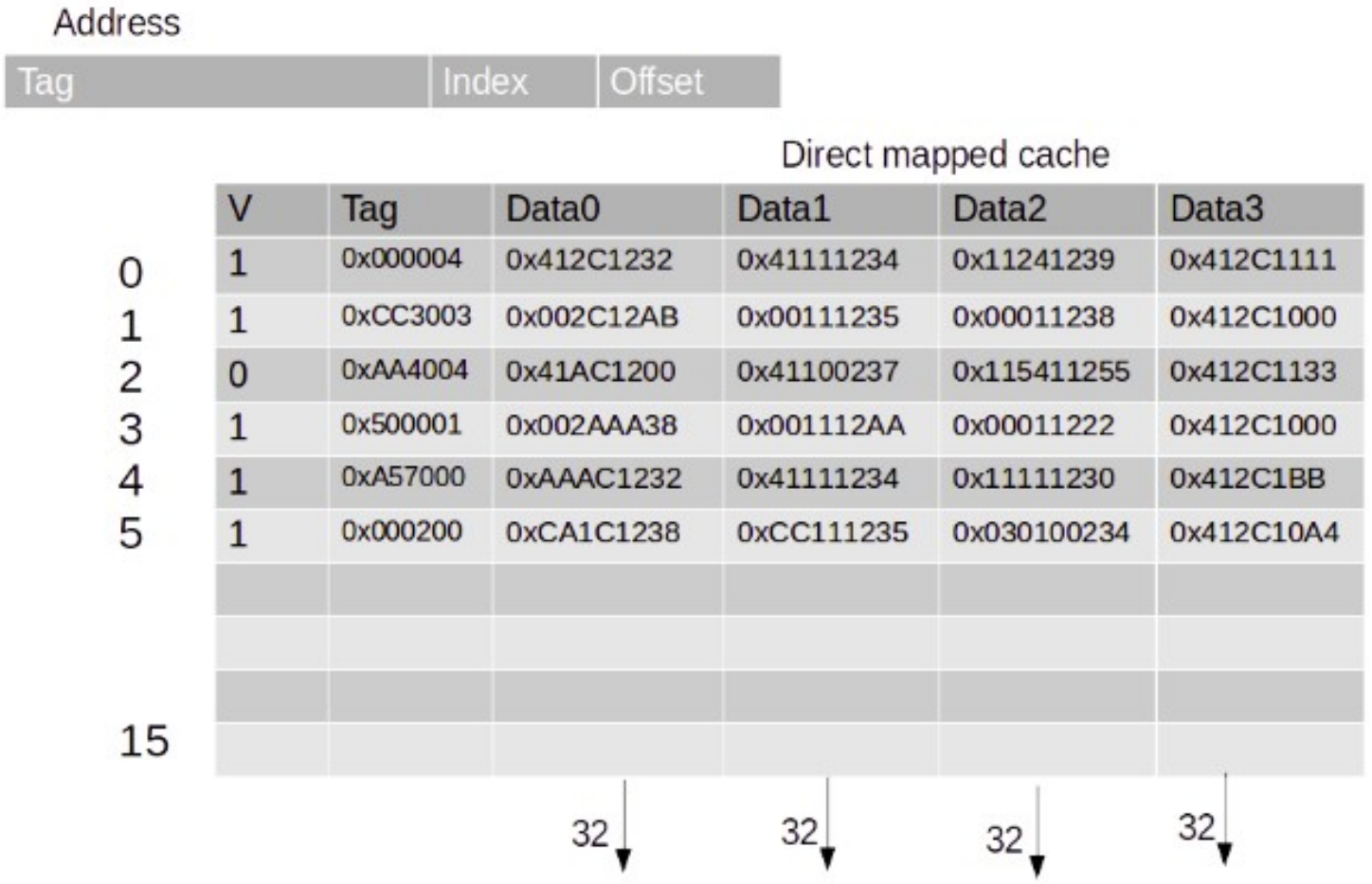
16 lines → 4 index bits. Each block or line has 4 words i.e., 16 bytes. To address each byte, we need 4 bits of offset. Remaining 24 bits are tag bits.

Tag field value → 0x000200

Block offset value →3 or 0011

The cache line in which the data will be found →Index 0001 -- Line 1

Is it a cache hit? →Cache miss.



Q3 Consider a direct mapped cache which uses 4-word blocks, 32-bit data words (4 bytes) and 32-bit addresses.

Say you are trying to read data from memory location 0x00020053. Assume you are reading the bytes individually. What would be the:

Is it a cache hit? If yes, what is the data that is read assuming a byte read?

Address

Tag	Index	Offset

Direct mapped cache

	V	Tag	Data0	Data1	Data2	Data3
0	1	0x000004	0x412C1232	0x41111234	0x11241239	0x412C1111
1	1	0xCC3003	0x002C12AB	0x00111235	0x00011238	0x412C1000
2	0	0xAA4004	0x41AC1200	0x41100237	0x115411255	0x412C1133
3	1	0x500001	0x002AAA38	0x001112AA	0x00011222	0x412C1000
4	1	0xA57000	0xAAAC1232	0x41111234	0x11111230	0x412C1BB
5	1	0x000200	0xCA1C1238	0xCC111235	0x030100234	0x412C10A4
15						

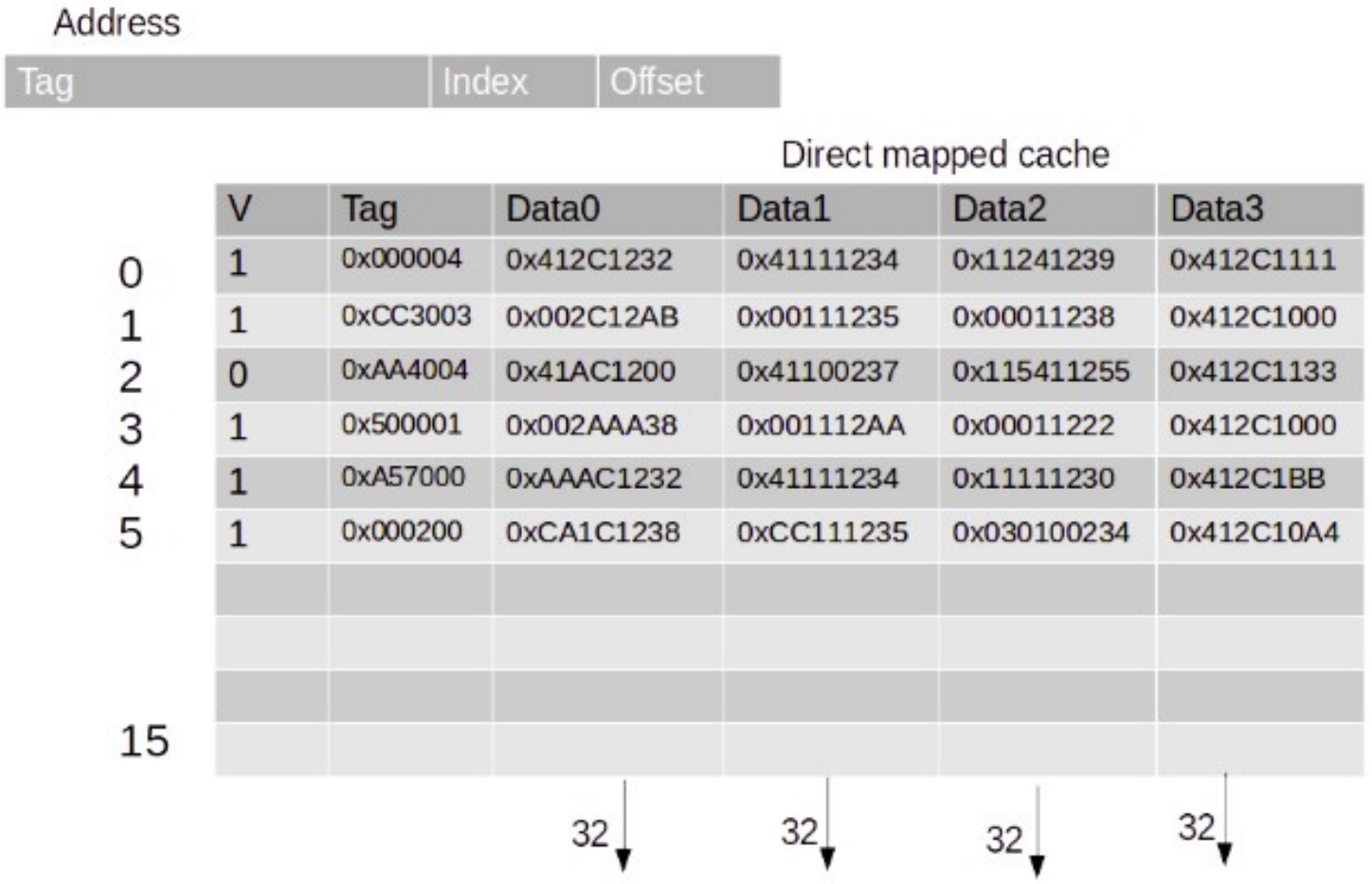
32 32 32 32

Soln:

Consider a direct mapped cache which uses 4-word blocks, 32-bit data words (4 bytes) and 32-bit addresses.

Address: 0000 0000 0000 0010 0000 0000 **0101** 0011 (0x00020053)

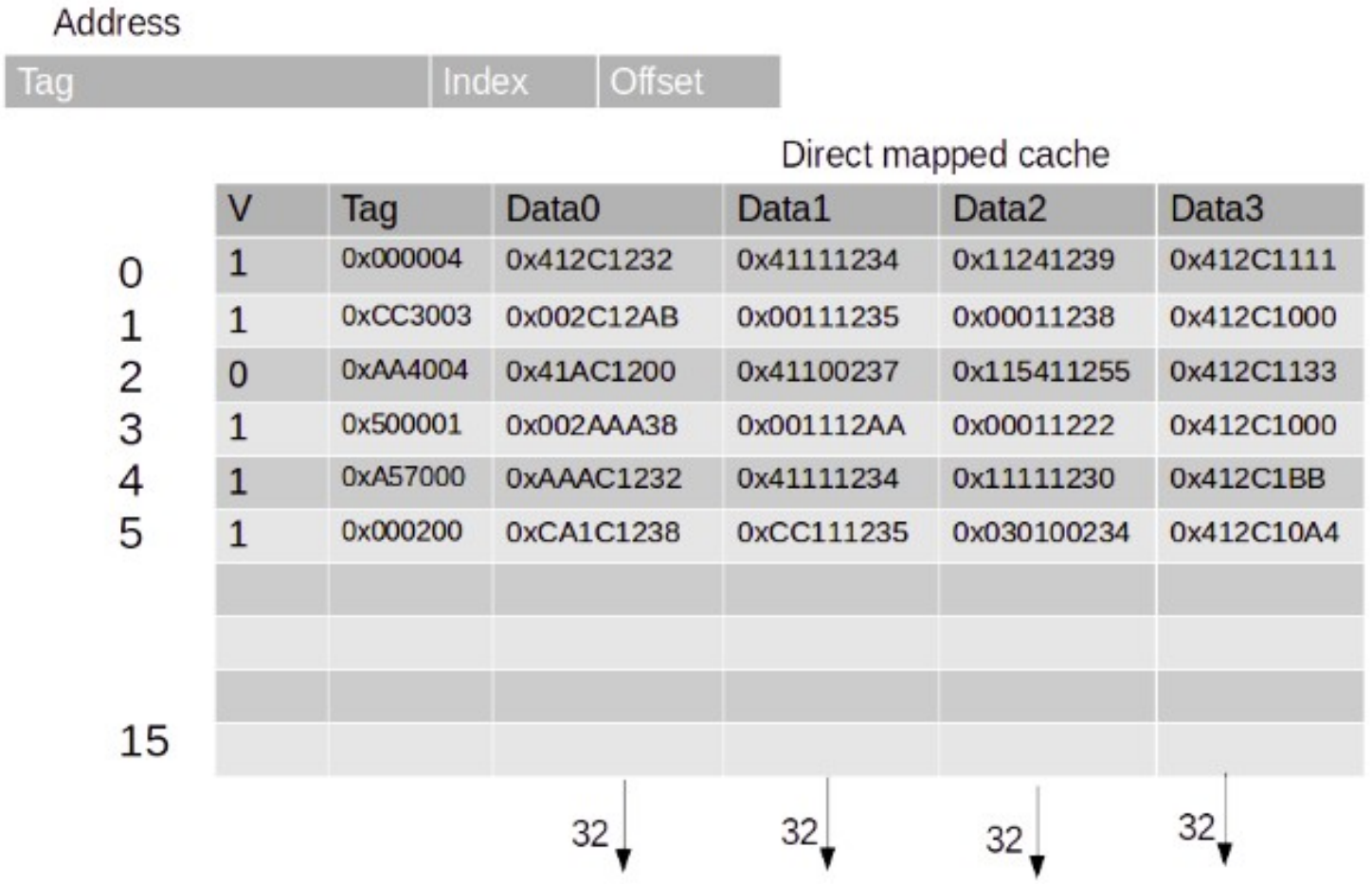
Hit: Data read is 38



Q4

Consider a direct mapped cache which uses 4-word blocks, 32-bit data words (4 bytes) and 32-bit addresses.

Can data from locations 0x00012329 and 0x00322FF9 be present in the cache at the same time? Explain.



Q4

Consider a direct mapped cache which uses 4-word blocks, 32-bit data words (4 bytes) and 32-bit addresses.

Soln: Index for 0x00012329 is 2. Index for 0x00322FF9 is F.

Line 2 and F are different indices and index to different cache lines. So, they can be present.

Q5: This is a 2 way set associative cache whose index number, tag and data are shown in the following table.
The address we obtain is:
1010 1010 0100 11 0111 0000
Assume no byte offset. What is the data fetched, if it is a cache hit?

Tag (14 bits)	Index or Set ID	Data
10100001001001	01101101	00_{16}
11100001100100	01101101	10_{16}
11001011010110	01101110	20_{16}
11100101101011	01101110	30_{16}
11110110110100	01101111	40_{16}
10100111010101	01101111	50_{16}
10101010111110	01110000	84_{16}
10101010010011	01110000	94_{16}
01110001001000	01110001	$A4_{16}$
00001101101101	01110001	$B4_{16}$
01011010010010	01110010	$C4_{16}$
10101111001011	01110010	$D4_{16}$

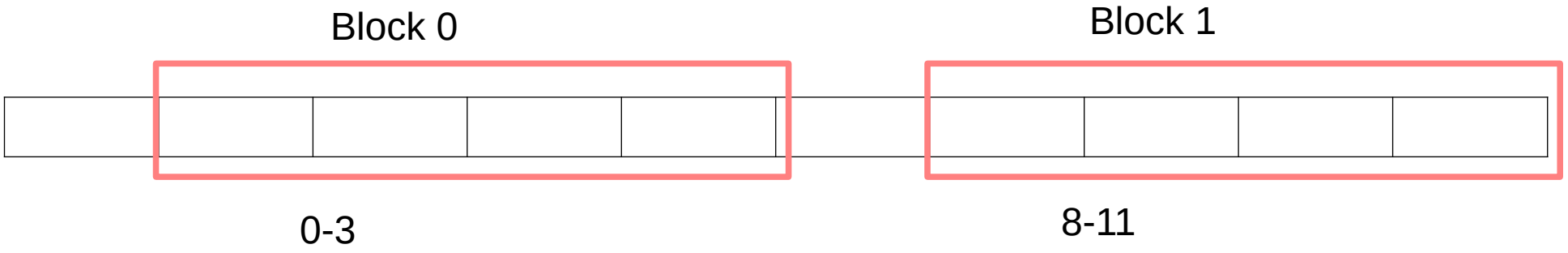
This is a 2 way set associative cache whose index number, tag and data are shown in the following table.
The address we obtain is:
1010 1010 0100 11 0111 0000
Assume no byte offset. What is the data fetched, if it is a cache hit?

Tag (14 bits)	Index or Set ID	Data
10100001001001	01101101	00_{16}
11100001100100	01101101	10_{16}
11001011010110	01101110	20_{16}
11100101101011	01101110	30_{16}
11110110110100	01101111	40_{16}
10100111010101	01101111	50_{16}
10101010111110	01110000	84_{16}
10101010010011	01110000	94_{16}
01110001001000	01110001	$A4_{16}$
00001101101101	01110001	$B4_{16}$
01011010010010	01110010	$C4_{16}$
10101111001011	01110010	$D4_{16}$

Q6

- Show the hits and misses and final cache contents for a fully associative cache with four-word blocks and a total size of 8 words. Assume LRU replacement.
  - Assume the sequence: 2,3,10,11,0,21,16

Solution



- 2: Miss: 0-3
- 3: Hit
- 10: 8-11, 0-3
- 11: Hit
- 0: Hit
- 21: 20-23 (replace 8-11), 0-3
- 16: miss