# Geng-You CHEN (陳庚佑)

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## **Work Experiences**

Synopsys, Inc. Senior R&D Engineer, Verdi Hsinchu City, Taiwan (R.O.C)

Nov 2019 ~ Present

I'm a backend engineer developing algorithms & data structures inside the graph database of our Verdi debugger tool.

- I proposed a Dynamic Programming algorithm of wildcard path matching on the call graph of modules in large-scale user designs.
   ✓Latency of each query is improved by 7.8x ~ 35x, compared with our existing backtracking algorithm.
   ✓Scaled out by porting my algorithm to Synopsys CDPL (our in-house distributed computing library) or Apache Spark GraphX.
- I adapted the idea of Persistent Binary Search Tree to do reconfiguration on the call graph of modules in large-scale user designs.

  ✓ Made every existing DP algorithm work even if users want to change their designs' hierarchy at runtime (without recompilation).

MediaTek, Inc. Taipei City, Taiwan (R.O.C.)

Principal Engineer, Set-top Box SoC

Senior Engineer, TV SoC

Jan 2019 ~ Mar 2019

After merged into MediaTek, I became the USB software owner of every STB SoC platform.

MStar Semiconductor, Inc. (merged with MediaTek, Inc.) Principal Engineer, TV SoC Taipei City, Taiwan (R.O.C.)

Jun 2018 ~ Dec 2018 Nov 2014 ~ May 2018

I was an embedded engineer improving Linux Kernel's USB core, EHCI driver (USB 2.0 host), and USB Mass Storage driver.

- I made the idea of Lazy Initialization workable for delayed resuming slow USB HDDs to shorten the system wake-up latency. 

  ✓ System wake-up latency is improved by up to 10x (measured when a slow USB HDD is plugged into the TV system).
- I rewrote entire USB layer for non-OS applications to help customers get way from GPL license.
   ✓ 6+ of our TV SoC platforms can be used in secure applications (for customers who want to keep their source codes closed).

### **Researches & Publications**

Exploiting Write Heterogeneity of Morphable MLC/SLC SSDs in Datacenters with Service-Level Objectives

USA

Published in IEEE Transactions on Computers (TC)

Mar 2017

In this paper, we optimized the usage of SLC mode in SSDs (speed up by sacrificing lifetimes) based on the latency SLO in data centers.

- I proposed an adaptive algorithm: Given a latency SLO (e.g. 99% of I/O requests need to be completed within 100ms), it guides SSDs to temporarily operate at SLC mode only when it predicts our latency SLO cannot be met.
  - √ For a set of real workloads which typically requires over-provisioning 2.4x storage nodes to meet our SLO, I can meet the same SLO without over-provisioning by sacrificing only 2.8% of SSD lifetime.

DuraCache: A Durable SSD Cache Using MLC NAND Flash

USA

Published in ACM/EDAC/IEEE Design Automation Conference (DAC)

May 2013

In this paper, we improved 19.6x lifetime of SSD caches by exploiting the fact that many SSDs are write-through caches in data centers.

I helped the first author to build a test platform for wearing out MLC Flash chips, and researching how the BER (bit error rate) grows.
 ✓ My result inspired us that if we can treat the data corruptions in SSD caches as regular cache misses, we can improve 1.7x lifetime of SSD caches by sacrificing less than 1% of cache hit count.

#### **Educations**

Dept. of CSIE, National Taiwan University

M.S., Computer Science, Overall GPA: 4.28/4.30 (ranking: 3/144)

Taipei City, Taiwan (R.O.C.) Sep 2012 ~ Jun 2014

Undergraduate Program of EECS, National Tsing Hua University B.S., Electrical Engineering

Hsinchu City, Taiwan (R.O.C.)

Sep 2008 ~ Jun 2012

#### Technical Skills

- · Languages: C/C++ (proficient), C#, Java, Scala, SQL, Shell script, HTML, CSS, JavaScript, PHP, Verilog, SystemC
- · Domain expertises:
  - Algorithms and distributed computing (as an algorithm developer at Synopsys)
  - Linux Kernel device drivers (as an USB expert at MediaTek with 4+ years of experience)
  - Non-volatile memory systems / SSDs for data centers (as a Computer Architecture researcher with 2 papers earning 47 citations)