Geng-You CHEN (陳庚佑)

gengyouchen@gmail.com | +886 931472408 | linkedin.com/in/gengyouchen | github.com/gengyouchen

Work Experiences

MediaTek, Inc. **Taipei City, Taiwan**
Principal Software Engineer, Set-top Box *Jan 2019 ~ Mar 2019*
Principal Software Engineer, USB team, TV SoC (former MStar Semiconductor, Inc.) *Jun 2018 ~ Dec 2018*
Senior Software Engineer, USB team, TV SoC (former MStar Semiconductor, Inc.) *Nov 2014 ~ May 2018*

- I improved Linux Kernel's USB host driver by discovering and eliminating more than 200 3rd-party device compatibility issues
  - ✓Annual # of USB compatibility issues is reduced by up to 84% (measured in my Korea customer's project)
- I achieved an innovative "Lazy Resuming" idea in Linux Kernel's DPM (device power management)
  - ✓System wake-up time is improved by up to 10x (measured when a slow USB hard disk is plugged into the system)
- I re-wrote entire USB layer from the ground in U-Boot to help customers get way from GPL license
  - ✓More than 6 models of SoCs can be completely GPL-free, and used by China customers for security applications
- I worked oversea with customers (5 weeks in a year), and helped our IC designers improve/validate their next generation TV SoCs
  - ✓I became the USB software owners for more than 15 models of major TV SoCs (more than 50% global market share)

TinnoTek, Inc. (Closed. It's a startup founded by Prof. Shi-Yu Huang) **Hsinchu City, Taiwan**
Software Intern, EDA (Electronic Design Automation) *Jul 2011 ~ Dec 2011*

- I developed a tool which scans customer's Verilog source codes, and generates & routes our power monitoring modules into them
  - ✓With the help of FPGA, the SoC power simulation time is improved by 10x (compared with simulation using pure software tools)

Educations

Dept. of CSIE, National Taiwan University **Taipei City, Taiwan**
M.S., Computer Science (Advisor: Prof. Chia-Lin Yang) *Sep 2012 ~ Jun 2014*

- Overall GPA: 4.28/4.30 (ranking: 3/144)
  - ✓I was elected as a Honorary Member of the Phi Tau Phi Scholastic Honor Society of the Republic of China
- Research on Computer Architecture, especially on optimizing the NAND Flash memory (i.e. SSD) in data centers

Undergraduate Program of EECS, National Tsing Hua University **Hsinchu City, Taiwan**
B.S., Electrical Engineering *Sep 2008 ~ Jun 2012*

Researches & Publications

Exploiting Write Heterogeneity of Morphable MLC/SLC SSDs in Datacenters with Service-Level Objectives **USA**
Published in IEEE Transactions on Computers (TC), a top journal in Computer Architecture *Mar 2017*

- I proposed an online algorithm which smartly guides MLC SSDs to temporarily operate at SLC mode in order to meet the data center's SLO requirement (e.g. 99% of I/O requests should be completed within 100ms) without over-provisioning more storage nodes
  - ✓For real workloads requiring 2.4x over-provisioning to meet their SLO, I can meet the same SLO without any over-provisioning, by just sacrificing less than 2.8% of SSD's lifetime (due to using SLC mode)

DuraCache: A Durable SSD Cache Using MLC NAND Flash **USA**
Published in ACM/EDAC/IEEE Design Automation Conference (DAC), a top conference in Computer Architecture *May 2013*

- I used FPGA to build a test platform for wearing out MLC NAND Flash chips and measuring how their BER (bit error rate) grow
  - ✓ My experiment result inspired us that if we design our data center to treat the data corruptions in SSD as regular cache misses, we can improve the SSD lifetime by more than 1.7x, by just sacrificing less than 1% of cache hit count

Technical Skills

- Programming: C/C++ (proficient), Verilog (for FPGA prototyping), SystemC (for simulator development)
- Domain expertise
  - Linux Kernel's device driver (as an USB expert in MediaTek with 4 years of experience)
  - NAND Flash memory system (as a Computer Architecture researcher with 2 top papers earning more than 40 citations)

Other Projects

- **SSDSim**: I developed a scalable and flexible SSD simulator written in SystemC, pure C (for firmware), and C++
  - ✓ When simulating SSD clusters, it can be 5x ~ 10x faster than other two popular open-source SSD simulators in the academia
- **EECS2002**: I designed a series of hand-on programming labs for people who want to learn system prototyping using FPGA
  - ✓ Selected by Prof. Shi-Yu Huang in his class Introduction to SoPC (System on Programming Chip) as his students' home-works