

31	25	24	20	19	15	14	12	11	7	6	0	
funct7		rs2		rs1		funct3		rd		opcode		R-type
imm[11:0]				rs1		funct3		rd		opcode		I-type
imm[11:5]		rs2		rs1		funct3		imm[4:0]		opcode		S-type
imm[12 10:5]		rs2		rs1		funct3		imm[4:1 11]		opcode		B-type
imm[31:12]								rd		opcode		U-type
imm[20 10:1 11 19:12]								rd		opcode		J-type

imm[31:12]					rd	0110111	LUI
imm[31:12]					rd	0010111	AUIPC
imm[20 10:1 11 19:12]					rd	1101111	JAL
imm[11:0]			rs1	000	rd	1100111	JALR
imm[12 10:5]	rs2	rs1	000	imm[4:1 11]	1100011	BEQ	
imm[12 10:5]	rs2	rs1	001	imm[4:1 11]	1100011	BNE	
imm[12 10:5]	rs2	rs1	100	imm[4:1 11]	1100011	BLT	
imm[12 10:5]	rs2	rs1	101	imm[4:1 11]	1100011	BGE	
imm[12 10:5]	rs2	rs1	110	imm[4:1 11]	1100011	BLTU	
imm[12 10:5]	rs2	rs1	111	imm[4:1 11]	1100011	BGEU	
imm[11:0]			rs1	000	rd	0000011	LB
imm[11:0]			rs1	001	rd	0000011	LH
imm[11:0]			rs1	010	rd	0000011	LW
imm[11:0]			rs1	100	rd	0000011	LBU
imm[11:0]			rs1	101	rd	0000011	LHU
imm[11:5]	rs2	rs1	000	imm[4:0]	0100011	SB	
imm[11:5]	rs2	rs1	001	imm[4:0]	0100011	SH	
imm[11:5]	rs2	rs1	010	imm[4:0]	0100011	SW	
imm[11:0]			rs1	000	rd	0010011	ADDI
imm[11:0]			rs1	010	rd	0010011	SLTI
imm[11:0]			rs1	011	rd	0010011	SLTIU
imm[11:0]			rs1	100	rd	0010011	XORI
imm[11:0]			rs1	110	rd	0010011	ORI
imm[11:0]			rs1	111	rd	0010011	ANDI
0000000	shamt	rs1	001	rd	0010011	SLLI	
0000000	shamt	rs1	101	rd	0010011	SRLI	
0100000	shamt	rs1	101	rd	0010011	SRAI	
0000000	rs2	rs1	000	rd	0110011	ADD	
0100000	rs2	rs1	000	rd	0110011	SUB	
0000000	rs2	rs1	001	rd	0110011	SLL	
0000000	rs2	rs1	010	rd	0110011	SLT	
0000000	rs2	rs1	011	rd	0110011	SLTU	
0000000	rs2	rs1	100	rd	0110011	XOR	
0000000	rs2	rs1	101	rd	0110011	SRL	
0100000	rs2	rs1	101	rd	0110011	SRA	
0000000	rs2	rs1	110	rd	0110011	OR	
0000000	rs2	rs1	111	rd	0110011	AND	
0000	pred	succ	00000	000	00000	0001111	FENCE
0000	0000	0000	00000	001	00000	0001111	FENCE
000000000000			00000	000	00000	1110011	ECALL
000000000001			00000	000	00000	1110011	EBREAK
001100000010			00000	000	00000	1110011	MRET
csr			rs1	001	rd	1110011	CSRRW
csr			rs1	010	rd	1110011	CSRRS
csr			rs1	011	rd	1110011	CSRRC
csr			zimm	101	rd	1110011	CSRRWI
csr			zimm	110	rd	1110011	CSRRSI
csr			zimm	111	rd	1110011	CSRRCI

0000001	rs2	rs1	000	rd	0110011		MUL
0000001	rs2	rs1	001	rd	0110011		MULH
0000001	rs2	rs1	010	rd	0110011		MULSU
0000001	rs2	rs1	011	rd	0110011		MULU
0000001	rs2	rs1	100	rd	0110011		DIV
0000001	rs2	rs1	101	rd	0110011		DIVU
0000001	rs2	rs1	110	rd	0110011		REM
0000001	rs2	rs1	111	rd	0110011		REMU

1513	12	11 10	9 8 7	6	5 4 3	2 1 0		
func4		Rd/rs1			rs2		op	CR-type
func3	imm	rd/rs1			imm		op	CI-type
func3	imm			rs2		op	CSS-type	
func3	Imm				rd'		op	CIW-type
func3	imm		rs1'		imm	rd'	op	CL-type
func3	imm		rs1'		imm	rs2'	op	CS-type
func6			rd'/rs1'		func2	rs2'	op	CA-type
func3	offset		rs1'		offset		op	CB-type
func3	jump target						op	CJ-type

1513	12	11	10	9	8	7	6	5	4	3	2	1	0	
000	0								0			00		Illegal
000	nzuimm[5:4 9:6 2 3]								rd'			00		C.ADDI4SPN
001	-											00		Reserved
010	uimm[5:3]			rs1'			uimm[2 6]		rd'			00		C.LW
100	-											00		Reserved
110	uimm[5:3]			rs1'			uimm[2 6]		rs2'			00		C.SW
000	nzimm[5]	0				nzimm[4:0]				01			C.NOP	
000	nzimm[5]	rs1/rd != 0				nzimm[4:0]				01			C.ADDI	
001	Imm[11 4 9:8 10 6 7 3:1 5]											01		C.JAL
010	imm[5]	rd != 0				imm[4:0]				01			C.LI	
011	nzimm[9]	2				nzimm[4 6 8:7 5]				01			C.ADDI16SP	
011	nzimm[17]	rd != {0,2}				nzimm[16:12]				01			C.LUI	
100	0	00	rs1'/rd'			nzimm[4:0]				01			C.SRLI	
100	nzimm[5]	01	rs1'/rd'			nzimm[4:0]				01			C.SRAI	
100	imm[5]	10	rs1'/rd'			imm[4:0]				01			C.ANDI	
100	0	11	rs1'/rd'			00		rs2'			01		C.SUB	
100	0	11	rs1'/rd'			01		rs2'			01		C.XOR	
100	0	11	rs1'/rd'			10		rs2'			01		C.OR	
100	0	11	rs1'/rd'			11		rs2'			01		C.AND	
100	1	11	-			-		-			01		Reserved	
101	Imm[11 4 9:8 10 6 7 3:1 5]											01		C.J
110	imm[8 4:3]			rs1'			imm[7:6 2:1 5]					01		C.BEQZ
111	imm[8 4:3]			rs1'			imm[7:6 2:1 5]					01		C.BNEZ
000	nzuimm[5]	rs1/rd != 0				nzuimm[4:0]				10			C.SLLI	
010	uimm[5]	rd != 0				uimm[4:2 7:6]				10			C.LWSP	
100	0	rs1 != 0				0				10			C.JR	
100	0	rd != 0				rs2 != 0				10			C.MV	
100	1	0				0				10			C.EBREAK	
100	1	rs1 != 0				0				10			C.JALR	
100	1	rs1/rd != 0				rs2 != 0				10			C.ADD	
110	uimm[5:2 7:6]					rs2				10			C.SWSP	