HT9170B/HT9170D
DTMF Receiver

Features

- Operating voltage: 2.5V~5.5V
- Minimal external components
- No external filter is required
- Low standby current (on power down mode)
- Excellent performance
- Tristate data output for MCU interface
- 3.58MHz crystal or ceramic resonator
- 1633Hz can be inhibited by the INH pin
- HT9170B: 18-pin DIP package
  HT9170D: 18-pin SOP package

General Description

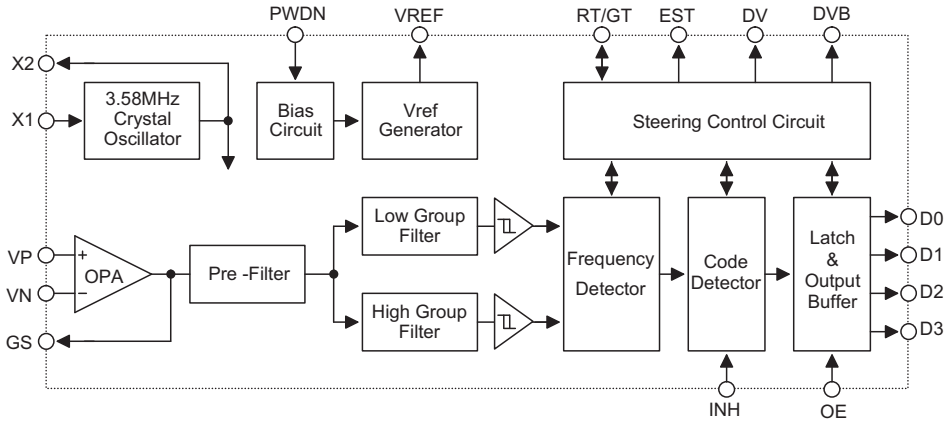
The HT9170B/D are Dual Tone Multi Frequency (DTMF) receivers integrated with digital decoder and bandsplit filter functions as well as power-down mode and inhibit mode operations. Such devices use digital counting techniques to detect and decode all the 16 DTMF tone pairs into a 4-bit code output.

Highly accurate switched capacitor filters are implemented to divide tone signals into low and high group signals. A built-in dial tone rejection circuit is provided to eliminate the need for pre-filtering.

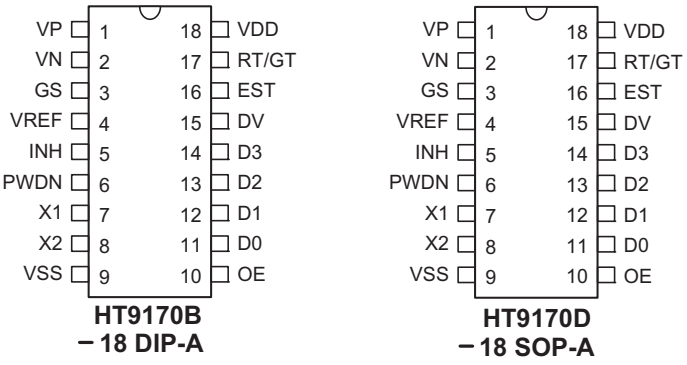
Selection Table

Function / Part No.	Operating Voltage	OSC Frequency	Tristate Data Output	Power Down	1633Hz Inhibit	DV	DVB	Package
HT9170B	2.5V~5.5V	3.58MHz	√	√	√	√	—	18 DIP
HT9170D	2.5V~5.5V	3.58MHz	√	√	√	√	—	18 SOP

Block Diagram



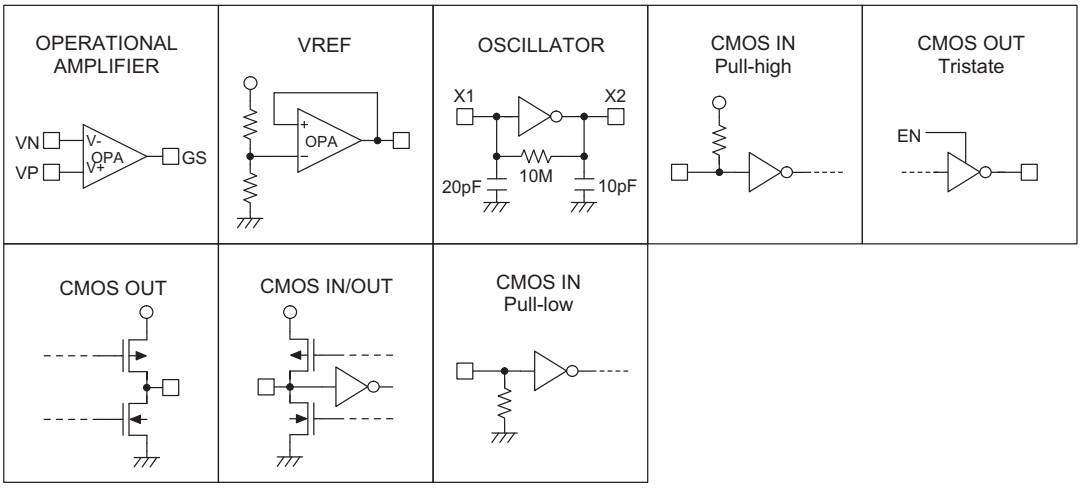
Pin Assignment



Pin Description

Pin Name	I/O	Internal Connection	Description
VP	I	Operational Amplifier	Operational amplifier non-inverting input
VN	I		Operational amplifier inverting input
GS	O		Operational amplifier output terminal
VREEF	O	VREF	Reference voltage output, normally $V_{DD}/2$
X1	I	oscillator	The system oscillator consists of an inverter, a bias resistor and the necessary load capacitor on chip. A standard 3.579545MHz crystal connected to X1 and X2 terminals implements the oscillator function.
X2	O		
PWDN	I	CMOS IN Pull-low	Active high. This enables the device to go into power down mode and inhibits the oscillator. This pin input is internally pulled down.
INH	I	CMOS IN Pull-low	Logic high. This inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
VSS	—	—	Negative power supply, ground
OE	I	CMOS IN Pull-high	D0~D3 output enable, high active
D0~D3	O	CMOS OUT Tristate	Receiving data output terminals OE="H": Output enable OE="L": High impedance
DV	O	CMOS OUT	Data valid output When the chip receives a valid tone (DTMF) signal, the DV goes high; otherwise it remains low.
EST	O	CMOS OUT	Early steering output (see Functional Description)
RT/GT	I/O	CMOS IN/OUT	Tone acquisition time and release time can be set through connection with external resistor and capacitor.
VDD	—	—	Positive power supply, 2.5V~5.5V for normal operation

Approximate internal connection circuits



Absolute Maximum Ratings

Supply Voltage .....–0.3V to 6V

Input Voltage.....V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature .....–50°C to 125°C

Operating Temperature.....–20°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.5	5	5.5	V
I_{DD}	Operating Current	5V	—	—	3.0	7	mA
I_{STB}	Standby Current	5V	PWDN=5V	—	10	25	μA
V_{IL}	"Low" Input Voltage	5V	—	—	—	1.0	V
V_{IH}	"High" Input Voltage	5V	—	4.0	—	—	V
I_{IL}	"Low" Input Current	5V	V_{VP}=V_{VN}=0V	—	—	0.1	μA
I_{IH}	"High" Input Current	5V	V_{VP}=V_{VN}=5V	—	—	0.1	μA
R_{OE}	Pull-high Resistance (OE)	5V	V_{OE}=0V	60	100	150	kΩ
R_{IN}	Input Impedance (VN, VP)	5V	—	—	10	—	MΩ
I_{OH}	Source Current (D0~D3, EST, DV)	5V	V_{OUT} =4.5V	–0.4	–0.8	—	mA
I_{OL}	Sink Current (D0~D3, EST, DV)	5V	V_{OUT} =0.5V	1.0	2.5	—	mA
f_{OSC}	System Frequency	5V	Crystal=3.5795MHz	3.5759	3.5795	3.5831	MHz

A.C. Characteristics

f_{OSC}=3.5795MHz, Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
DTMF Signal							
	Input Signal Level	3V		–36	—	–6	dBm
		5V		–29	—	1	
	Twist Accept Limit (Positive)	5V		—	10	—	dB
	Twist Accept Limit (Negative)	5V		—	10	—	dB
	Dial Tone Tolerance	5V		—	18	—	dB
	Noise Tolerance	5V		—	–12	—	dB
	Third Tone Tolerance	5V		—	–16	—	dB
	Frequency Deviation Acceptance	5V		—	—	±1.5	%
	Frequency Deviation Rejection	5V		±3.5	—	—	%
t_{PU}	Power Up Time (See Figure 4.)	5V		—	30	—	ms
Gain Setting Amplifier							
R_{IN}	Input Resistance	5V	—	—	10	—	MΩ
I_{IN}	Input Leakage Current	5V	$V_{SS}<(V_{VP},V_{VN})<V_{DD}$	—	0.1	—	μA
V_{OS}	Offset Voltage	5V	—	—	±25	—	mV
P_{SRR}	Power Supply Rejection	5V	100 Hz $-3V<V_{IN}<3V$	—	60	—	dB
C_{MRR}	Common Mode Rejection	5V		—	60	—	dB
A_{VO}	Open Loop Gain	5V		—	65	—	dB
f_T	Gain Band Width	5V	—	—	1.5	—	MHz
V_{OUT}	Output Voltage Swing	5V	R_L>100kΩ	—	4.5	—	V_{PP}
R_L	Load Resistance (GS)	5V	—	—	50	—	kΩ
C_L	Load Capacitance (GS)	5V	—	—	100	—	pF
V_{CM}	Common Mode Range	5V	No load	—	3.0	—	V_{PP}
Steering Control							
t_{DP}	Tone Present Detection Time			5	16	22	ms
t_{DA}	Tone Absent Detection Time			—	4	8.5	ms
t_{ACC}	Acceptable Tone Duration			—	—	42	ms
t_{REJ}	Rejected Tone Duration			20	—	—	ms
t_{IA}	Acceptable Inter-digit Pause			—	—	42	ms
t_{IR}	Rejected Inter-digit Pause			20	—	—	ms
t_{PDO}	Propagation Delay (RT/GT to DO)			—	8	11	μs
t_{PDV}	Propagation Delay (RT/GT to DV)			—	12	—	μs
t_{DOV}	Output Data Set Up (DO to DV)			—	4.5	—	μs
t_{DDO}	Disable Delay (OE to DO)			—	300	—	ns
t_{EDO}	Enable Delay (OE to DO)			—	50	60	ns

Note: DO=D0~D3

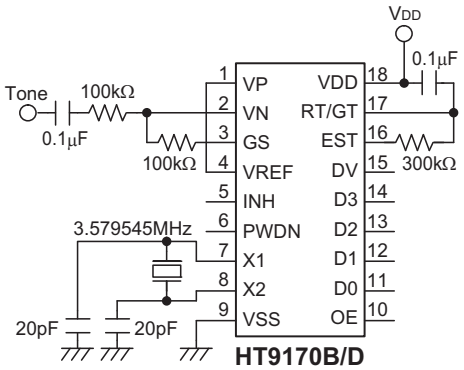


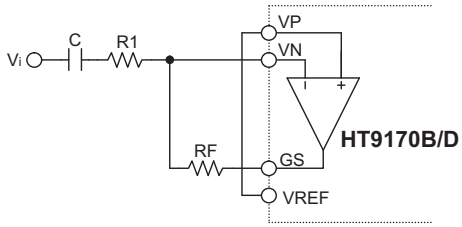
Figure 1. Test circuit

Functional Description

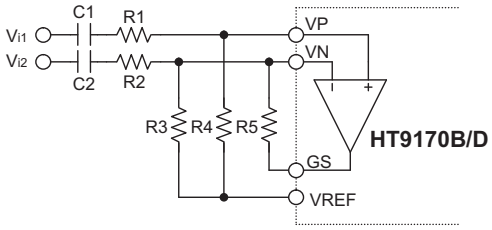
Overview

The HT9170B/D tone decoders consist of three band pass filters and two digital decode circuits to convert a tone (DTMF) signal into digital code output.

An operational amplifier is built-in to adjust the input signal (refer to Figure 2).



(a) Standard input circuit



(b) Differential input circuit

Figure 2. Input operation for amplifier application circuits

The pre-filter is a band rejection filter which reduces the dialing tone from 350Hz to 400Hz.

The low group filter filters low group frequency signal output whereas the high group filter filters high group frequency signal output.

Each filter output is followed by a zero-crossing detector with hysteresis. When each signal amplitude at the output exceeds the specified level, it is transferred to full swing logic signal.

When input signals are recognized to be effective, DV becomes high, and the correct tone code (DTMF) digit is transferred.

Steering control circuit

The steering control circuit is used for measuring the effective signal duration and for protecting against drop out of valid signals. It employs the analog delay by external RC time-constant controlled by EST.

The timing is shown in Figure 3. The EST pin is normally low and draws the RT/GT pin to keep low through discharge of external RC. When a valid tone input is detected, EST goes high to charge RT/GT through RC.

When the voltage of RT/GT changes from 0 to V_{TRT} (2.35V for 5V supply), the input signal is effective, and the correct code will be created by the code detector. After D0~D3 are completely latched, DV output becomes high. When the voltage of RT/GT falls down from VDD to V_{TRT} (i.e.., when there is no input tone), DV output becomes low, and D0~D3 keeps data until a next valid tone input is produced.

By selecting adequate external RC value, the minimum acceptable input tone duration (t_{ACC}) and the minimum acceptable inter-tone rejection (t_{IR}) can be set. External components (R, C) are chosen by the formula (refer to Figure 5.):

$t_{ACC}=t_{DP}+t_{GTP}$;

$t_{IR}=t_{DA}+t_{GTA}$;

where t_{ACC}: Tone duration acceptable time

t_{DP}: EST output delay time (″L″→″H″)

t_{GTP}: Tone present time

t_{IR}: Inter-digit pause rejection time

t_{DA}: EST output delay time (″H″→″L″)

t_{GTA}: Tone absent time

Timing Diagrams

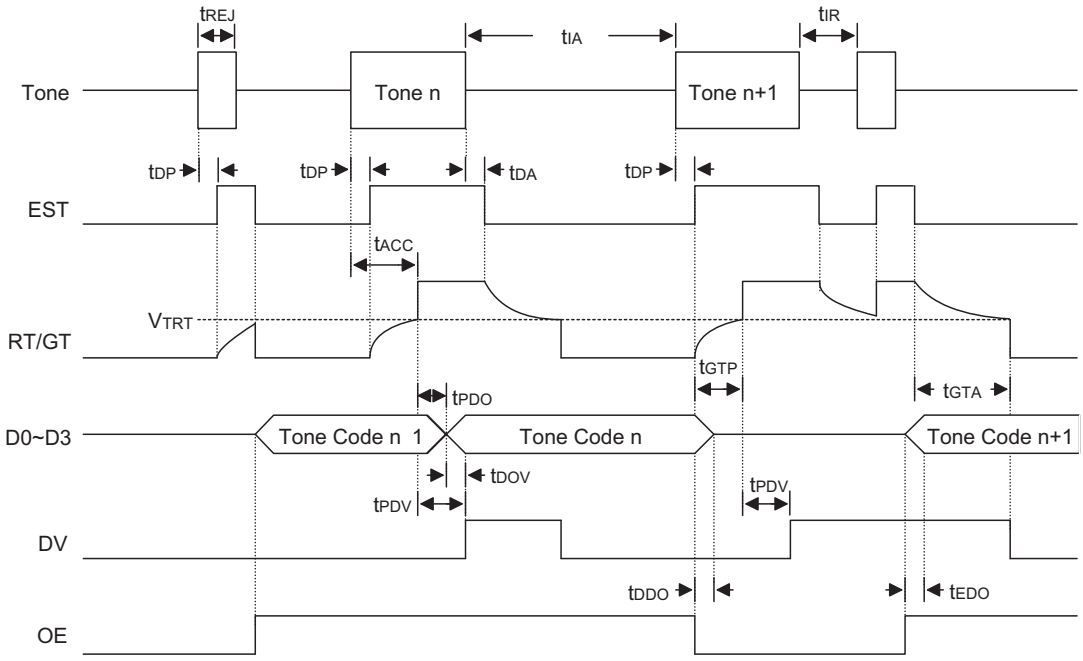


Figure 3. Steering timing

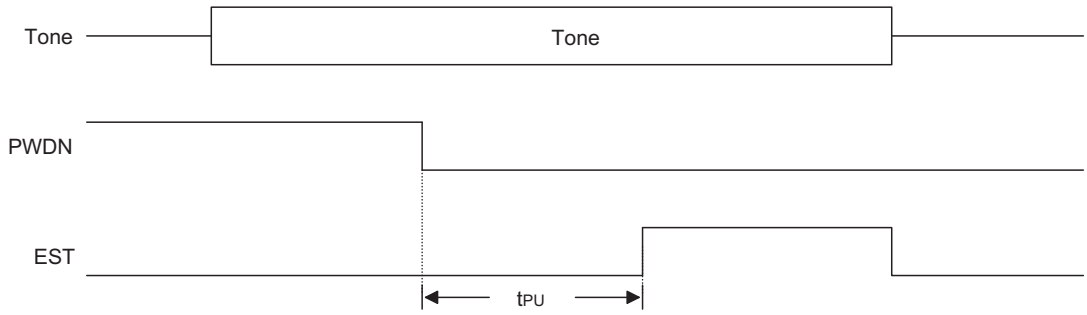
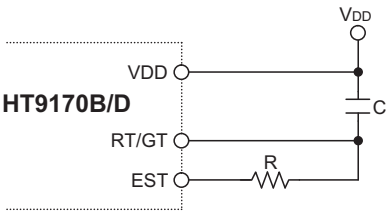


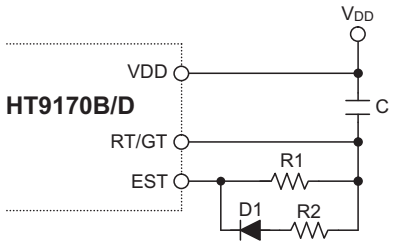
Figure 4. Power up timing



(a) Fundamental circuit:

$t_{GTP} = R \times C \times Ln (V_{DD} / (V_{DD} - V_{TRT}))$

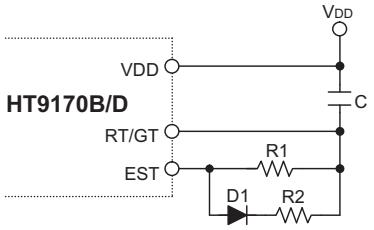
$t_{GTA} = R \times C \times Ln (V_{DD} / V_{TRT})$



(c) $t_{GTP} > t_{GTA}$:

$t_{GTP} = R1 \times C \times Ln (V_{DD} / (V_{DD} - V_{TRT}))$

$t_{GTA} = (R1 // R2) \times C \times Ln (V_{DD} / V_{TRT})$



(b) $t_{GTP} < t_{GTA}$:

$t_{GTP} = (R1 // R2) \times C \times Ln (V_{DD} - V_{TRT}))$

$t_{GTA} = R1 \times C \times Ln (V_{DD} / V_{TRT})$

Figure 5. Steering time adjustment circuits

DTMF dialing matrix

	COL1	COL2	COL3	COL4
ROW1	1	2	3	A
ROW2	4	5	6	B
ROW3	7	8	9	C
ROW4	*	0	#	D

DTMF data output table

Low Group (Hz)	High Group (Hz)	Digit	OE	D3	D2	D1	D0
697	1209	1	H	L	L	L	H
697	1336	2	H	L	L	H	L
697	1477	3	H	L	L	H	H
770	1209	4	H	L	H	L	L
770	1336	5	H	L	H	L	H
770	1477	6	H	L	H	H	L
852	1209	7	H	L	H	H	H
852	1336	8	H	H	L	L	L
852	1477	9	H	H	L	L	H
941	1336	0	H	H	L	H	L
941	1209	*	H	H	L	H	H
941	1477	#	H	H	H	L	L
697	1633	A	H	H	H	L	H
770	1633	B	H	H	H	H	L
852	1633	C	H	H	H	H	H
941	1633	D	H	L	L	L	L
—	—	ANY	L	Z	Z	Z	Z

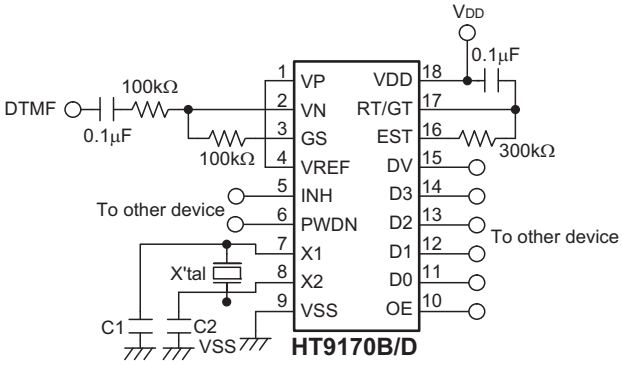
Note: "Z" High impedance; "ANY" Any digit

Data output

The data outputs (D0~D3) are tristate outputs. When OE input becomes low, the data outputs (D0~D3) are high impedance.

Application Circuits

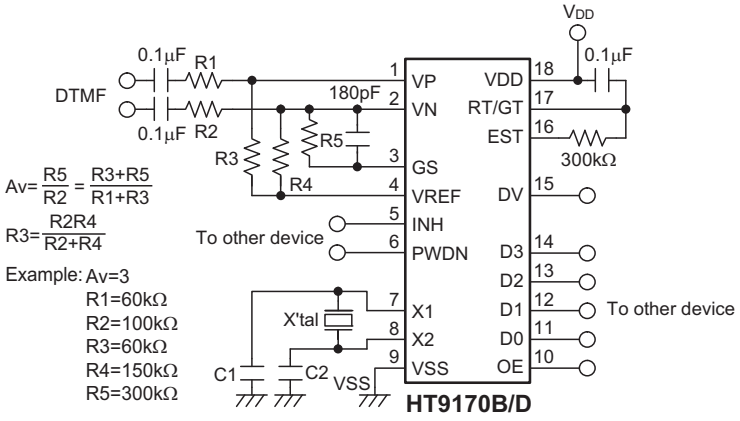
Application Circuit 1



Note: X′tal = 3.579545MHz crystal
C1 = C2 ≅ 20pF

X′tal = 3.58MHz ceramic resonator
C1 = C2 ≅ 39pF

Application Circuit 2



Note: X′tal = 3.579545MHz crystal
C1 = C2 ≅ 20pF

X′tal = 3.58MHz ceramic resonator
C1 = C2 ≅ 39pF

Package Information

18-pin DIP (300mil) Outline Dimensions

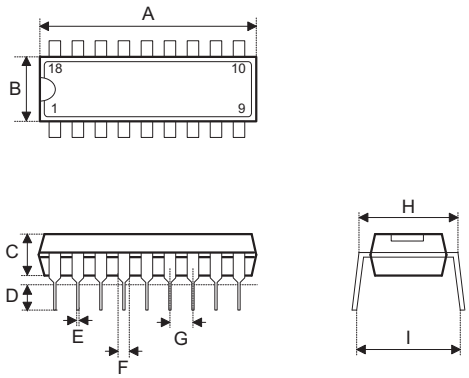


Fig1. Full Lead Packages

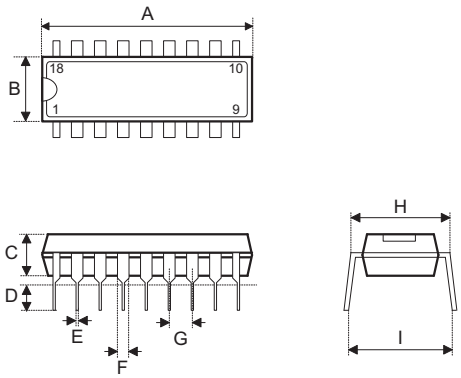


Fig2. 1/2 Lead Packages

• MS-001d (see fig1)

Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	880	—	920
B	240	—	280
C	115	—	195
D	115	—	150
E	14	—	22
F	45	—	70
G	—	100	—
H	300	—	325
I	—	—	430

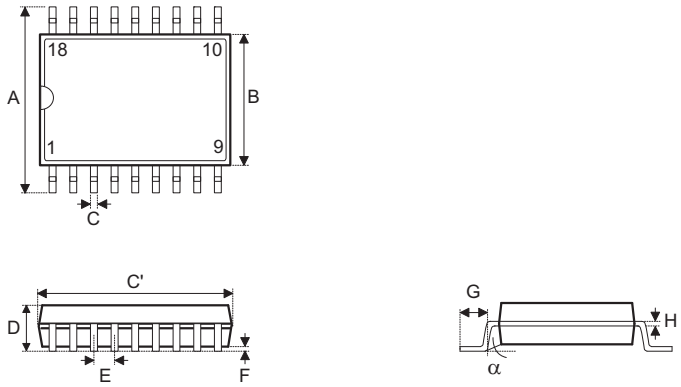
• MS-001d (see fig2)

Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	845	—	880
B	240	—	280
C	115	—	195
D	115	—	150
E	14	—	22
F	45	—	70
G	—	100	—
H	300	—	325
I	—	—	430

• MO-095a (see fig2)

Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	845	—	885
B	275	—	295
C	120	—	150
D	110	—	150
E	14	—	22
F	45	—	60
G	—	100	—
H	300	—	325
I	—	—	430

18-pin SOP (300mil) Outline Dimensions

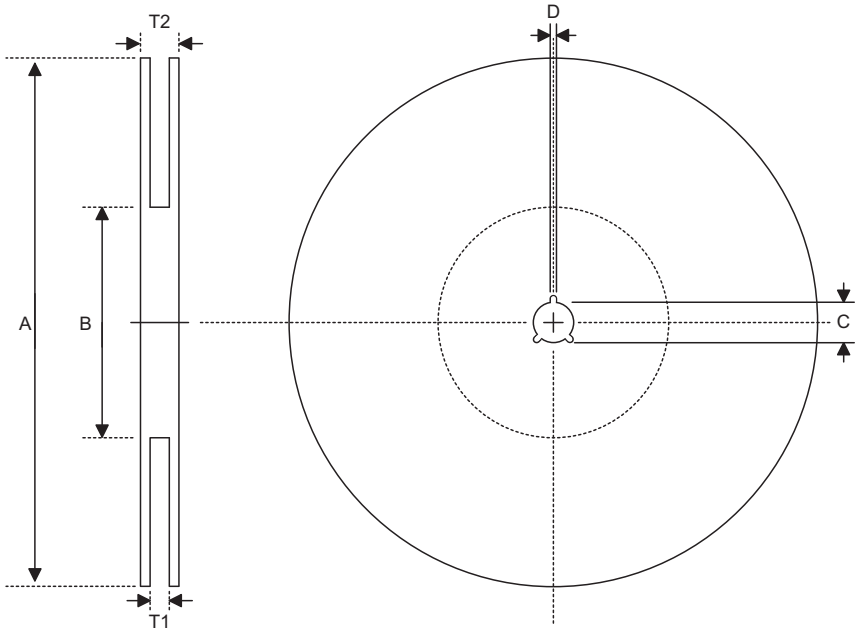


• MS-013

Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	393	—	419
B	256	—	300
C	12	—	20
C′	447	—	463
D	—	—	104
E	—	50	—
F	4	—	12
G	16	—	50
H	8	—	13
α	0°	—	8°

Product Tape and Reel Specifications

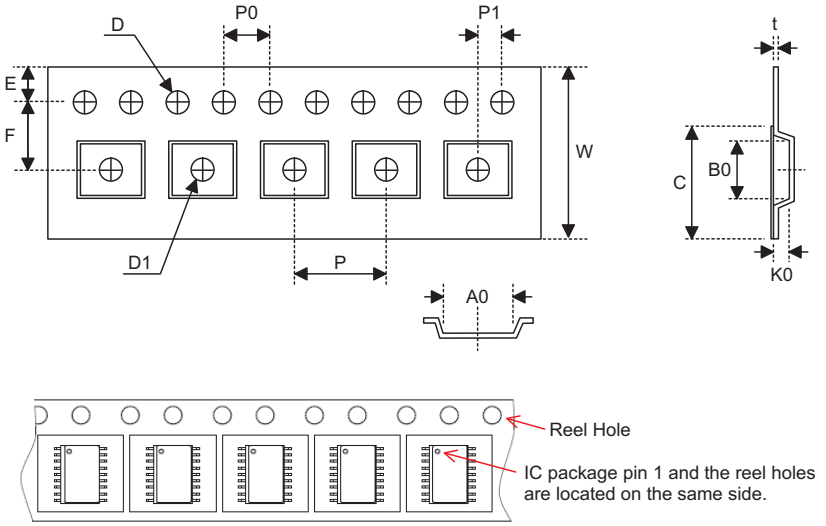
Reel Dimensions



SOP 18W

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	24.8 $^{+0.3/-0.2}$
T2	Reel Thickness	30.2±0.2

Carrier Tape Dimensions



SOP 18W

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0 $^{+0.3/-0.1}$
P	Cavity Pitch	16.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	1.5±0.1
D1	Cavity Hole Diameter	1.50 $^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	10.9±0.1
B0	Cavity Width	12.0±0.1
K0	Cavity Depth	2.8±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	21.3±0.1

Holtek Semiconductor Inc. (Headquarters)
No.3, Creation Rd. II, Science Park, Hsinchu, Taiwan
Tel: 886-3-563-1999
Fax: 886-3-563-1189
http://www.holtek.com.tw

Holtek Semiconductor Inc. (Taipei Sales Office)
4F-2, No. 3-2, YuanQu St., Nankang Software Park, Taipei 115, Taiwan
Tel: 886-2-2655-7070
Fax: 886-2-2655-7373
Fax: 886-2-2655-7383 (International sales hotline)

Holtek Semiconductor Inc. (Shanghai Sales Office)
G Room, 3 Floor, No.1 Building, No.2016 Yi-Shan Road, Minhang District, Shanghai, China 201103
Tel: 86-21-5422-4590
Fax: 86-21-5422-4705
http://www.holtek.com.cn

Holtek Semiconductor Inc. (Shenzhen Sales Office)
5F, Unit A, Productivity Building, Gaoxin M 2nd, Middle Zone Of High-Tech Industrial Park, ShenZhen, China 518057
Tel: 86-755-8616-9908, 86-755-8616-9308
Fax: 86-755-8616-9722

Holtek Semiconductor Inc. (Beijing Sales Office)
Suite 1721, Jinyu Tower, A129 West Xuan Wu Men Street, Xicheng District, Beijing, China 100031
Tel: 86-10-6641-0030, 86-10-6641-7751, 86-10-6641-7752
Fax: 86-10-6641-0125

Holtek Semiconductor Inc. (Chengdu Sales Office)
709, Building 3, Champagne Plaza, No.97 Dongda Street, Chengdu, Sichuan, China 610016
Tel: 86-28-6653-6590
Fax: 86-28-6653-6591

Holtek Semiconductor (USA), Inc. (North America Sales Office)
46729 Fremont Blvd., Fremont, CA 94538, USA
Tel: 1-510-252-9880
Fax: 1-510-252-9885
http://www.holtek.com

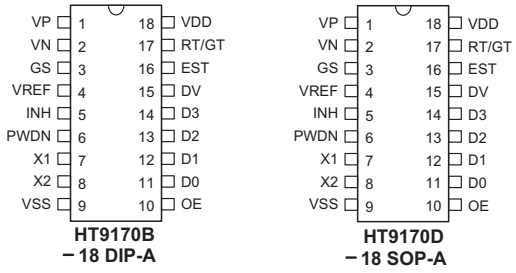
HT9170 雙音多頻(DTMF)信號接收器使用說明

文件編碼：HA0038T

簡介

HT9170 是一個具有數位解碼和濾波功能的雙音多頻(DTMF)信號接收器。HT9170B 和 HT9170D 可進入省電模式。HT9170 系列都利用數位計數的方法對 16 種 DTMF 輸入進行解碼，並產生 4bit 的代碼輸出。高速轉換的濾波電路將 DTMF 信號分解爲高頻和低頻信號。

HT9170B 的封裝形式爲 18-pin DIP
HT9170D 的封裝形式爲 18-pin SOP

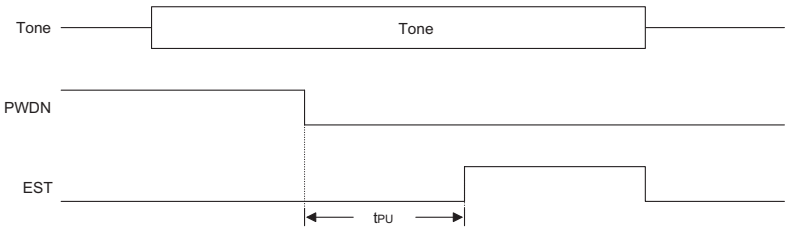


功能描述

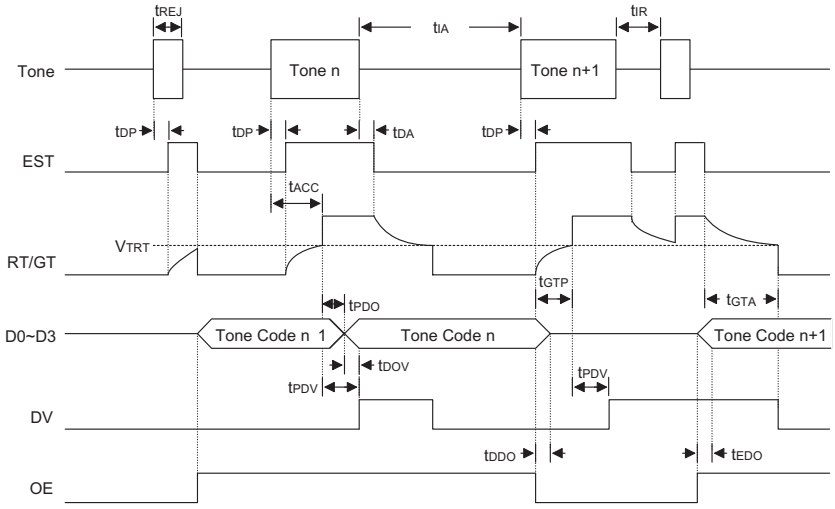
HT9170 系列通過三次濾波和兩次數位解碼電路將 DTMF 信號輸入轉換爲數位信號輸出。它有一個內置的放大電路對輸入信號進行調整。其預置濾波電路可將 350Hz~400Hz 的信號濾掉，再通過低通濾波電路和高通濾波電路將信號分解成低頻信號和高頻信號。

當 HT9170 接收到有效的 DTMF 信號時，其 DV 引腳被置爲高準位，並且這個 DTMF 信號被送至內部電路進行解碼。將 OE 引腳置爲高準位後，其 D0~D3 引腳就會產生解碼輸出。

時序圖



開機時序



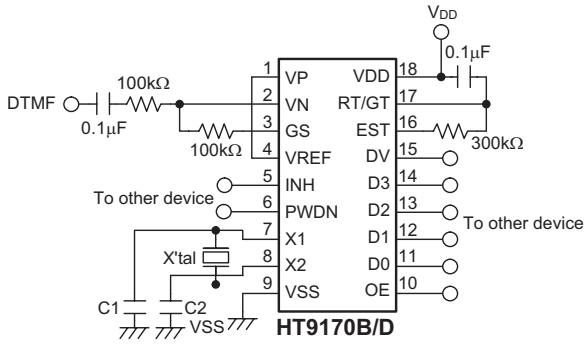
操作時序

DTMF 輸入與解碼輸出表

低頻(Hz)	高頻(Hz)	數碼	OE	D3	D2	D1	D0
697	1209	1	H	L	L	L	H
697	1336	2	H	L	L	H	L
697	1477	3	H	L	L	H	H
770	1209	4	H	L	H	L	L
770	1336	5	H	L	H	L	H
770	1447	6	H	L	H	H	L
852	1209	7	H	L	H	H	H
852	1336	8	H	H	L	L	L
852	1447	9	H	H	L	L	H
941	1336	0	H	H	L	H	L
941	1209	*	H	H	L	H	H
941	1447	#	H	H	H	L	L
697	1633	A	H	H	H	L	H
770	1633	B	H	H	H	H	L
852	1633	C	H	H	H	H	H
941	1633	D	H	L	L	L	L
—	—	ANY	L	Z	Z	Z	Z

註：Z 表示高阻狀態

應用電路



程式清單

```
include ht48r10a-1.inc
;----------------------------------------------------------------
;定義引腳
D0   EQU  PA.0
D1   EQU  PA.1
D2   EQU  PA.2
D3   EQU  PA.3
OE   EQU  PB.0
DV   EQU  PB.1
INH  EQU  PB.2
PWDN EQU  PB.3
；----------------------------------------------------------------
data .section 'data'
out_code db ?                          ;解碼資料輸出暫存器
;----------------------------------------------------------------
code .section at 0 'code'
         org     00h
         jmp     start
         org     04h
         reti
         org     08h
         reti
;----------------------------------------------------------------
start:
         clr     intc
         set     pac                   ;設置 PA 爲輸入口
         clr     pbc                   ;設置 PB 爲輸出口
         set     pbc.1                 ;設置 PB.1 爲輸入口
         mov     a,offset out_code
         mov     mp0,a
         mov     a,18h
         mov     count,a
         clr     PWDN                  ;啓動 9170 的晶振
         clr     OE
         CLR     INH
scan:    snz     DV                    ;檢測是否收到 DTMF 信號
         jmp     scan
         set     OE                    ;收到 DTMF 信號，則置位元 OE
                                       ;允許解碼信號輸出
         set     pa
         mov     a,pa                  ;將解碼信號讀入微控制器
         and     a, 0fh
         mov     [00h],a
scan1:
         sz      DV
         jmp     scan1
         clr     OE
```

```
                inc     mp0
                sdz     count
                jmp     scan                    ;檢測下一個 DTMF 信號
                jmp     start
        end
```