KU LEUVEN

FACULTEIT INGENIEURSWETENSCHAPPEN

Error bound analysis of sum product networks using posit representation number over FPGA

Antoine GENNART

Thesis submitted for the degree of
Master of Science in
Electrical Engineering, option
Electronics and Integrated Circuits

Thesis supervisor:
Prof. dr. ir. Marian VERHELST

Assessor:
Ir. TO FILL

Mentor:
Ir. Nimish SHAH

Academic year 2019 – 2020

Preface

TODODODOD I would like to thank everybody who kept me busy the last year, especially my promoter and my assistants. I would also like to thank the jury for reading the text. My sincere gratitude also goes to my wive and the rest of my family.

Antoine Gennart

Contents

Abstract

TODODODODO The `abstract` environment contains a more extensive overview of the work. But it should be limited to one page.

Chapter 1

Introduction

The first contains a general introduction to the work. The goals are defined and the modus operandi is explained.

Chapter 2

State of the art

2.1 Sum product networks

2.2 Floating point represenation

2.3 Posit representation

Chapter 3

Error bound

3.1 Error bound for Posit

3.1.1 Encoding error

3.1.2 Addition error

3.1.3 Multiplication error

3.2 Error bound for Float

3.2.1 Encoding error

3.2.2 Addition error

3.2.3 Multiplication error

3.3 Error bound for sum product networks

Chapter 4

Hardware implementation

4.1 Posit representation

4.1.1 Adder

4.1.2 Multiplier

4.2 Sum product networks

Chapter 5

Results and experiments

5.1 Error bound

5.2 Hardware implementation

Chapter 6

Conclusion

Bibliography

Master's thesis filing card

Student: Antoine Gennart

Title: Error bound analysis of sum product networks using posit representation number over FPGA

UDC: 621.3

Abstract:

Here comes a very short abstract, containing no more than 500 words. LaTeX commands can be used here. Blank lines (or the command `\par`) are not allowed!

Thesis submitted for the degree of Master of Science in Electrical Engineering, option Electronics and Integrated Circuits

Thesis supervisor: Prof. dr. ir. Marian Verhelst

Assessor: Ir. TO FILL

Mentor: Ir. Nimish Shah