OLLSCOIL NA hÉIREANN, CORCAIGH
THE NATIONAL UNIVERSITY OF IRELAND, CORK

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

Examination Session and Year	Summer 2018
Module Code	CS2507
Module Title	Computer Architecture
Paper Number	
External Examiner	Prof. Omer Rana
The Head of the Department	Prof. Cormac Sreenan
Internal Examiners	Dr. Ahmed Zahran
Instructions to Candidates	**Answer all questions.**
Duration of Paper	90 minutes
Special Requirements	**Clearly write the question number in the answer sheet.** **All written text must be legible to be graded.** **Calculators are NOT allowed.**

PLEASE DO NOT TURN THIS PAGE UNTIL INSTRUCTED TO DO SO

THEN ENSURE THAT YOU HAVE THE CORRECT EXAM PAPER

Question 1: [20 marks]

A. **[7 marks]** Name two key performance metrics used to determine the performance of computer systems. What does each metric measure? Explain how these metrics would be affected by replacing the processor with two processors identical to the original one.

B. **[7 marks]** Explain what is meant by the power wall.
Explain how the power wall changed the adopted approach for improving the performance of microprocessors.

C. **[6 marks]** Consider the following C statements.

int x1=10;

float x2=10.25;

Write down the corresponding binary value stored for x1and x2 in MIPS registers.

Question 2: [20 marks]

A. **[8 marks]** Explain what is meant by the following design principles and illustrate using an example how MIPS integrates them into its instruction set design.
   a. Make the common case fast
   b. Simplicity favours regularity

B. **[12 marks]** Consider the MIPS code below and answer the following questions.

```
L1:     addi $t0, $0, 0
L2:     addi $t1, $0, 0
L3:     ori $t2, $0, 4
L4:     addi $t3, $0, 1000
L5:     slt $t4, $t0, $t2
L6:     beq $t4, $0, L12
L7:     lw $t4, 0($t3)
L8:     add $t1, $t1, $t4
L9:     add $t0, $t0, 1
L10:    add $t3, $t3, 4
L11:    j L5
L12:    ……
```

a. **[2 marks]** What would be the value of registers $t0, $t1, $t2, $t3, $t4 when these instructions are executed for the first time?

b. **[2 marks]** How many times would the instructions at L5, L6, and L7 be executed?

c. **[2 marks]** If every memory location X stores the same value X (e.g., memory location 1000 contains 1000), what would be the value of the registers $t0, $t1, $t2, $t3, $t4 when the instruction at L12 is executed?

d. **[2 marks]** Rewrite the code between L1 and L11 as a procedure in which the values 4 in L3 and 1000 in L4 are passed as arguments, write this procedure after making the necessary changes.

e. **[1 marks]** In the procedure, do we need to store the return address register ($ra) in the stack? Why?

f. **[1 marks]** In the procedure, how many registers should be moved to the stack? Why?

g. **[2 marks]** Consider a single clock cycle processor, how many clock cycles would be needed to execute the shown instructions before executing L12?

Question 3: [20 marks]

A. **[8 marks]** Name hazard types in pipelined processor architectures and identify the cause of each of them. What is the most challenging type to handle? Explain one technique that is used to reduce the impact of this hazard.

B. **[6 marks]** Consider the code shown in Question 2.B, running in a five-stage pipelined MIPS. Which lines are prone to pipelining hazards? Can any of these completely hazards be avoided in this code? If yes, how? If No, why?

C. **[6 marks]** Assume that individual stages of the MIPS processor datapath have the following latencies

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

Also, assume that instructions executed by the processor are broken down as follows:

ALU	beq	lw	sw
45%	20%	20%	15%

a. (1 mark) What is the clock cycle time in a pipelined and non-pipelined processor?
b. (1 mark) What is the total latency of an LW instruction in a pipelined and non-pipelined processor?
c. (1 mark) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?
d. (1 mark) Assuming there are no stalls or hazards, what is the utilization of the data memory?
e. (1 mark) Assuming there are no stalls or hazards, what is the utilization of the write-register port of the register file?
f. (1 mark) Assuming there are no stalls or hazards, what is the utilization of the sign extender?

Question 4: [20 marks]

A. **[6 marks]** Reducing the miss rate and miss penalty are essential goals to improve the cache performance. Explain two techniques that are used to achieve these goals.

B. **[4 marks]** Calculate the parity bits of the Hamming SEC for the following byte [0x77].

C. **[4 marks]** What is the role of Translation Look-aside Buffer (TLB) in virtual memory systems? How does TLB impact the performance of virtual memory systems? What is the difference between a TLB miss and a page fault?

D. **[6 marks]** For a MIPS direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-5	4-0

1. (2 marks) What is the cache block size (in words)?
2. (2 marks) How many entries does the cache have?
3. (2 marks) To which block in the cache does the address 3000 belong?

PLEASE DO NOT TURN THIS PAGE UNTIL INSTRUCTED TO DO SO

THEN ENSURE THAT YOU HAVE THE CORRECT EXAM PAPER