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Thin-film Silicon Solar Cells

Bhushan Sopori

National Renewable Energy Laboratory, Golden, CO, USA

8.1 INTRODUCTION

Because silicon (Si) is an indirect band gap material, it is generally perceived that the thickness of Si required to absorb usable sunlight should be larger than $(\alpha_{\text{bandedge}})^{-1}$, where α_{bandedge} is the absorption coefficient for wavelength (λ) of light corresponding to the near-bandedge. Using this simple rule of thumb, on the basis of absorption due to a single pass of light, and using the mid-point of the bandedge ($\lambda = 1.05$ μm), one gets $\alpha^{-1} \sim 700$ μm. This implies that the wafer thickness for sufficient absorption of the solar spectrum is >700 μm. This is quite a large thickness for a Si wafer and is not desirable for commercial production of solar cells for two reasons: the wafer cost can be very high and its effectiveness for collection of photogenerated carriers will be small because it is difficult to have a minority-carrier diffusion length (MCDL) comparable to such a large wafer thickness. Thus, for practical reasons, wafer thickness must be less than this value. Furthermore, detailed models that take into account surface characteristics and the multireflections within the wafer show that absorption can be greatly enhanced; thus, the need for such a thick wafer is diminished. Later in this chapter, we will show that by employing an appropriate structure, a very thin layer of Si can offer a high degree of absorption of the solar spectrum – nearly as much as a thick wafer. The physics and modeling capabilities for analyses of solar cell structures have taken two decades to develop and have been responsible for the majority of the improvements in Si solar cell efficiency.

As an introduction, it is necessary to have a general understanding of the requirements for a thin-film Si solar cell and the problems that emerge when the thickness of a Si solar cell is reduced. Clearly just reducing the cell thickness will result in reduced absorption, and thus, a reduced photocurrent. To get a quantitative feel of such a reduction in the photocurrent, consider a planar solar cell. Figure 8.1 is a plot of maximum achievable current density (MACD) generated by a planar solar cell, with an optimum antireflection (AR) coating, for different values of the cell thickness. These calculations are

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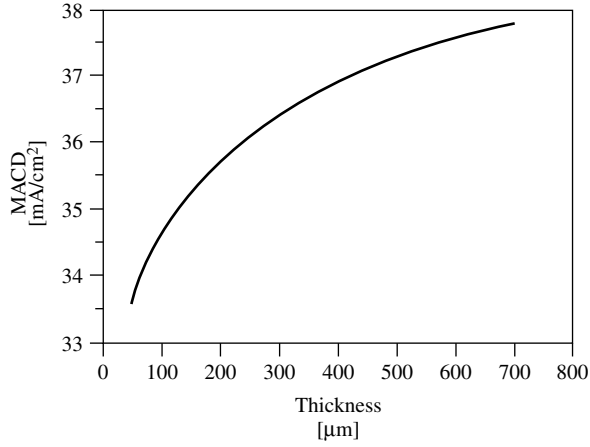


Figure 8.1 Maximum achievable current density (MACD) from a planar, AR-coated Si solar cell as a function of cell thickness. These calculations assume an optimized AR coating and AM1.5 incident spectrum. These results are obtained with *PV Optics*

performed using *photovoltaic* (*PV*) *Optics* software, which assumes the generation of one electron-hole pair per photon and a collection efficiency of unity. These assumptions are tantamount to a zero surface-recombination velocity and absence of other electronic loss mechanisms. Thus, the photocurrent in Figure 8.1 corresponds to a maximum achievable current density for the AM1.5 solar spectrum. Figure 8.1 shows that the photocurrent increases with an increase in thickness and saturates at a thickness of about 700 μm. At a thickness of ~300 μm, the current density is within 5% of the saturation value, which implies that a thickness of 300 μm is suitable for fabricating high-efficiency solar cells on planar substrates. This is fortunate because a similar demand on wafer thickness comes from requirements for maintaining a high yield in handling and processing other semiconductor devices.

The PV industry has traditionally borrowed technological know-how of device handling and processing from the semiconductor industry, which traditionally uses thick wafers to prevent breakage through mechanical handling or generation of thermal stresses by high-temperature processing. Concomitantly, the PV community found it compelling to use wafers of similar thickness for Si solar cells. The choice of thick wafers permitted the PV community to focus on the material and device-processing issues, which helped develop the science and technology of Si solar cells to the current level.

Recently, however, there have been many advances in wafer handling and in the development of gentler processing methods to accommodate high throughput. These advances have sparked interest in using thinner substrates for two reasons: (1) To reduce the amount of Si for each watt of PV energy generation. Because the PV industry has gone through periods of Si shortage, an efficient use of Si can minimize such hardships; and (2) To improve the efficiency of solar cells fabricated on low-cost substrates using improved cell designs.

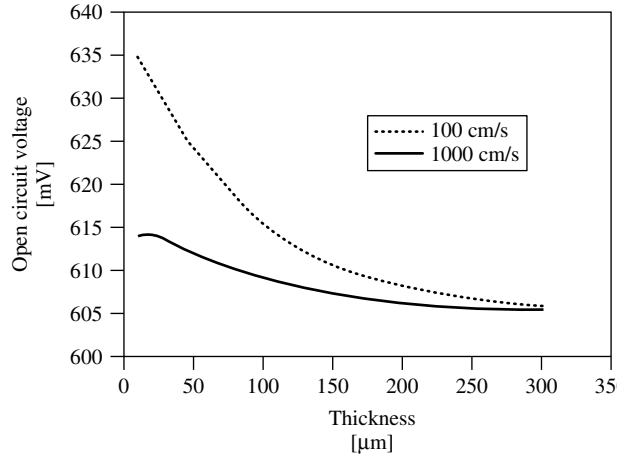


Figure 8.2 V_{OC} of a Si solar cell as a function of thickness for high and low surface-recombination velocities. These calculations were performed with PC1D

One approach to simultaneously accomplish these demands is to use thinner wafers. Thinner wafers conserve material and also offer a performance advantage by decreasing the bulk-carrier recombination within the solar cell. Hence, for a given material quality of the substrate, a reduction in the cell thickness can result in improving the open-circuit voltage (V_{OC}) and the fill factor (FF) of the solar cell. However, as the cell thickness is reduced, the surface recombination becomes an increasingly important component of the total recombination. In particular, surface recombination can severely degrade V_{OC}. This can be seen in Figure 8.2, which shows V_{OC} as a function of thickness (for a rather simple solar cell) for two different values of surface-recombination velocity, $S = 100$ cm/s and $S = 1000$ cm/s. In the calculations for Figure 8.2, we have used a front-textured cell with $S_f = S_b$, where S_f and S_b are the recombination velocities at the front and back surfaces, respectively. The important conclusion is that although a reduction in thickness can lead to an increase in V_{OC}, it can have the opposite effect if surface recombination is not reduced simultaneously. Clearly, the full advantage of reducing the volume recombination by thinner wafers can be achieved only if the device has built-in features to generate and reflect minority carriers away from interfaces using electronic reflectors (such as high–low fields), and optical reflectors. These are important considerations for thin solar cells.

Thus, thinner cells can yield higher voltages and higher fill factors if the surface recombination demands are met. However, they may suffer a loss in the photocurrent unless the optical losses associated with thickness reduction are compensated through superior light-trapping design. If these conditions are met, thinner cells can be more efficient than their thicker counterparts. Thin-film cells can also offer a direct cost advantage associated with the use of less Si and by employing thin-film technologies that (in principle) are deemed to be low-cost methods. It is clear that thinner cells can offer significant reduction in the PV energy cost. The photovoltaic industry is planning to reduce the wafer thickness incrementally from its current value of about 350 μm to less than 100 μm within

the next ten years, staying within the realm of the existing technologies at each major step of thickness. However, the arguments above provide motivation for a major reduction in thickness – to a new generation of Si solar cells using Si films less than 10 μm thick. Such a thin-film Si (TF-Si) solar cell offers many advantages that can lower the cost of generating solar electricity. A TF-Si cell offers (1) reduced bulk recombination leading to lower dark current, higher V_{OC} and higher FF of the device. Compared to a thick cell, a thin cell of the same material quality can yield higher device performance. Likewise, for a comparable performance, TF-Si solar cell requires lower material quality than a thick cell. It also offers (2) potential for low-cost cells/modules, (3) potential for lightweight photovoltaics, (4) lower energy consumption for device fabrication, and (5) potential for flexible solar cells.

These advantages of TF-Si solar cells, in concurrence with the performance advantage, make them very attractive for the future. Practical realization of solar cells with the above advantages poses many challenges in both the design and device fabrication. These challenges include an efficient method for light-trapping to compensate for reduced thickness, and a low-cost substrate to support the thin film. Low-cost substrates generally imply materials that may not be compatible with the high temperatures required for formation and processing of Si film. This incompatibility can arise because of impurities in the substrate that can diffuse into the Si film, softening of the substrate, thermal mismatch, and less desirable electronic properties of the interface leading to high S_b.

This chapter will discuss current efforts to develop a new technology (or set of technologies) that can achieve the potential performance of very thin Si solar cells. In the last few years, a number of R&D groups around the world have embarked on the design and fabrication of TF-Si solar cells. These efforts have already led to some exciting results. However, the design and fabrication of high-efficiency TF-Si solar cells continue to present a host of challenges. We review the salient aspects of the current research on TF-Si cells, and we present a systematic approach to the analysis, design, and fabrication of such devices.

8.2 A REVIEW OF CURRENT THIN-FILM SI CELLS

Many basic concepts of thin-film Si solar cells were suggested decades ago [1, 2]. It was apparent then that thinner cells would require a means of enhancing optical absorption. As early as 1975, it was proposed that enhanced optical absorption accompanying light-trapping can help lower the cell thickness required for efficient generation of photocurrent to a few microns. The proposed approach used a prismatic configuration to deflect light into a thin film at oblique incidence, so that the light would be total internally multireflected within the thin cell. This approach is similar to launching guided waves in integrated optics. Although this approach did not flourish because of evident drawbacks, other cell configurations that would support the use of very thin Si films for solar cell applications were later suggested [3, 4]. Some simple (approximate) calculations showed that cell efficiencies approaching 10% could be obtained with polycrystalline Si films of 10-μm thickness with 1-μm grain size [3]. These calculations only considered bulk recombination arising from grain boundaries (GBs) in polycrystalline Si and planar cell structures. Although the possibility of the thin-film Si solar cell was envisioned long ago, a practical realization has begun only recently. The path to TF-Si cells has

awaited some understanding of how to improve optical losses through enhanced absorption and the recognition and mitigation of electronic losses because of carrier recombination at interfaces.

Initial theoretical analysis based on thermodynamic considerations [5] suggested that rough surfaces and an asymmetric cell structure would effectively enhance optical absorption in the cell. Surface texturing, which was initially introduced to reduce surface reflectance for broadband illumination, also resulted in an increase in the optical path of light transmitted into a Si wafer [6–10]. Following the initial success, texture etching became a standard process step for fabricating Si solar cells, both in the laboratory and commercially. Figure 8.3 shows calculated short-circuit current density (J_{SC}) values as a function of thickness for different texture structures including planar, standard chemical texture, pyramids, inverted pyramids, and perpendicular slats. The surface structures are illustrated in Figure 8.4. However, only the laboratory cells, fabricated on high-quality wafers and with high-reflectance back contacts, realized the advantage of light-trapping. Although commercial cells also use texturing, its usefulness was perhaps largely limited to lowering the surface reflectance, rather than enhancing light-trapping. This is because the typical commercial solar cells use an Al-alloyed back contact that develops a rough interface, which has very low reflectance and allows most of the light to be transmitted into the metal where it is absorbed. The light absorbed in the metal constitutes an optical loss.

Surface texture has been successfully produced by anisotropic chemical etching in solutions of KOH or NaOH. It is known that texturing involves exposition of (111) crystallographic planes, which yield pyramids on (100) wafers. However, good texturing requires tedious process steps of developing a chemical composition containing silicates [11]. It was fortunate that texture etching could be combined with saw-damage removal for a low cost process. Recently, other texturing techniques have been developed that include reactive-ion etching, mechanical scribing of grooves, and acid etching [12–14]. However, none of these methods are suitable for thin-film solar cells because they produce deep

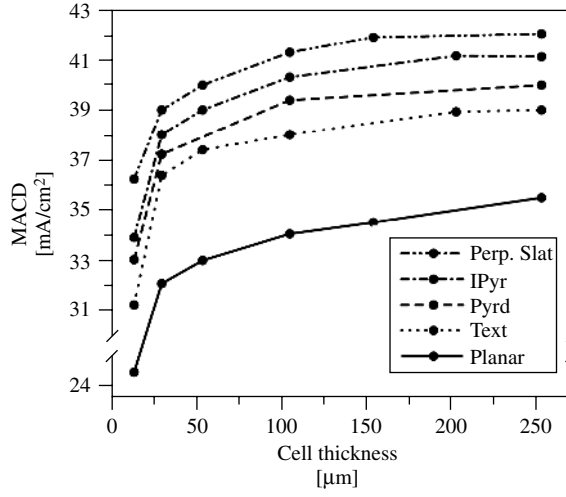


Figure 8.3 Calculated MACD for Si solar cells with different texture shapes: perpendicular slats, inverted pyramids, uniformly textured pyramids, chemically textured random pyramids and planar

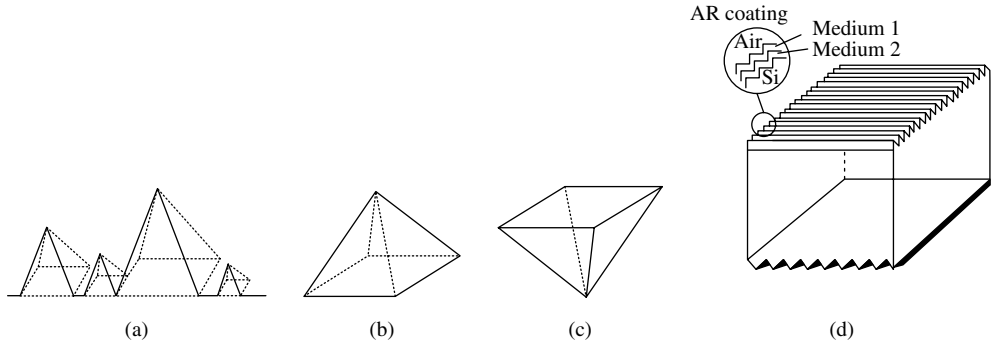


Figure 8.4 Sketches of various surface structures used in calculations shown in Figure. 8.3: (a) chemically textured random pyramids; (b) uniformly textured pyramids; (c) inverted pyramids; and (d) perpendicular slats

texture. A suitable approach for producing texture in TF-Si may be intrinsic to the use of polycrystalline material. This method has worked well for transparent conducting oxides used in thin-film a-Si.

Surface texturing naturally occurs in polycrystalline films deposited from a Si-bearing gas phase, as well as in thin and thick films grown at or near the melting point. Although exact mechanisms are not well established, texturing appears to be a grain-boundary effect. In a gas-phase growth, the high-energy grain-boundary sites allow migration of Si atoms away from the grain-boundary regions into the main grains, leading to a loss of material (thickness of the Si film) in the vicinity of the grain boundary [15, 16]. In a melt regime, such as in the growth of Si ribbons, there are local variations in the solidification temperature between the intragrain and grain-boundary regions. Because the surface tension of liquid Si or Si at high temperatures is quite high, it has the tendency to ball up at the free surfaces. This process results in grooving at the grain boundaries [17, 18]. Texturing is also observed in Si thin films crystallized by metal-induced crystallization [19]. A natural formation of texture in a Si film can play an important role in cost-effectiveness of TF-Si solar cells by obviating the need for a separate layer to enhance light-trapping. Because texturing is related to the growth or deposition process, it is important to note that texture shape and depth can change with a change in grain size. Brief discussions of the effects of texture height and texture angle are given in the next section. One of the drawbacks of texturing is that it greatly increases the surface area, thereby increasing dark current and reducing V_{OC}.

As pointed out in the previous section, interfaces (surfaces) attain a particularly significant role in a TF-Si solar cell because, for a given solar spectrum, a thinner cell has higher-generated carrier density near the surface due to enhanced light trapping. A simple way to envision increased sensitivity to surface recombination is to examine the distribution of absorbed photon flux in a thick wafer and a thin film. Figures 8.5(a) and 8.5(b) compare the distribution of absorbed photon flux in a 300-μm wafer and a 10-μm thin film of Si, respectively. Both cells have front and back texture, with an Al back-reflector. The texture heights for thick and thin cells are 3 μm and 0.6 μm, respectively. It is seen that the thin cell has an absorbed photon flux density about 3

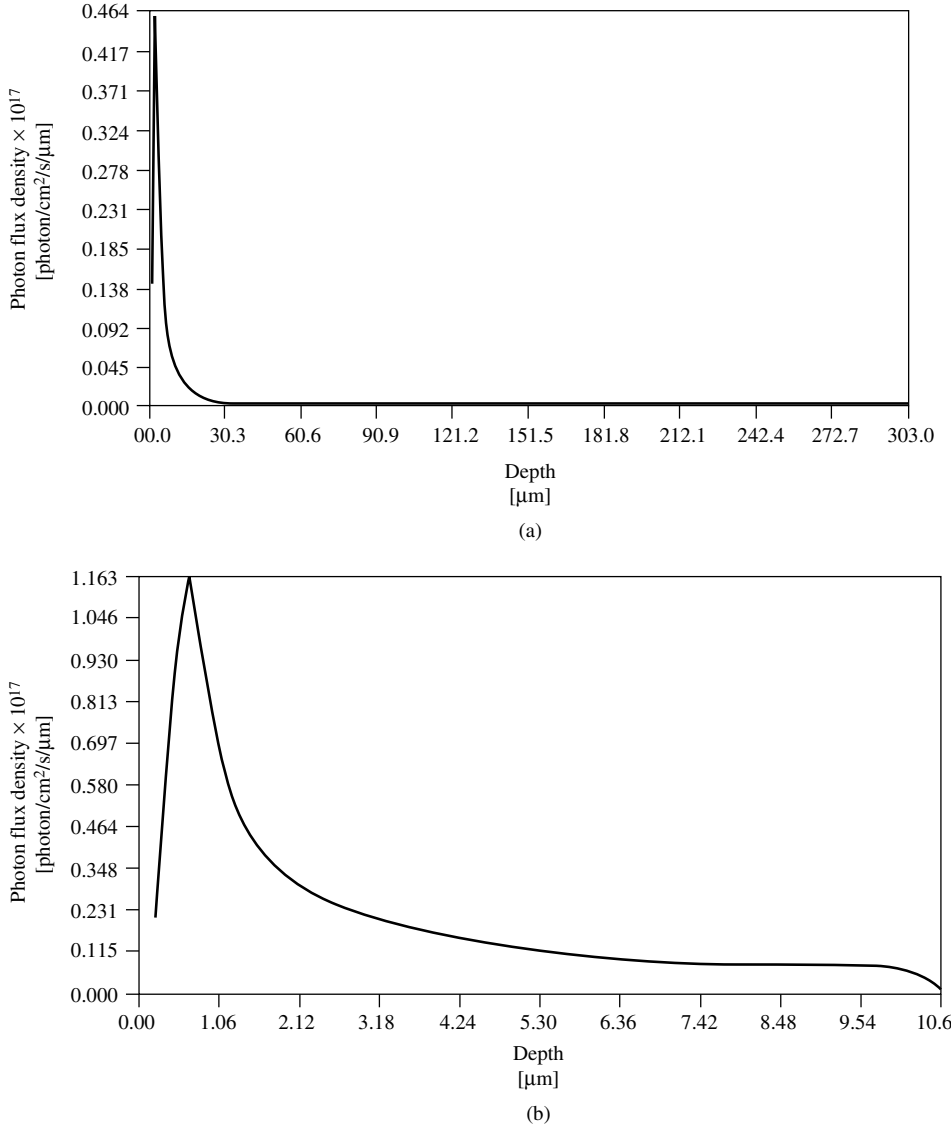


Figure 8.5 Calculated photon flux absorbed within the thickness of a (a) 300-μm wafer; and (b) 10-μm thin film. Both structures have double-sided texture and an Al back-reflector

times higher at each interface; implying that carrier generation at the interfaces of the thinner cell is about three times higher. Consequently, for the same surface-recombination velocity, the carrier recombination for the thinner cell will be 3 times higher. Therefore, it is imperative that an efficient TF-Si cell design will minimize contributions from all components of surface-related recombination.

It is important to recognize that there can be several contributions to the surface recombination in a solar cell (in addition to that from the cell-air interface). These

contributions include Si-metal (Si-M) interface(s) and edge leakage (e.g. from the mesa edge). Many approaches are used to minimize the effective surface recombination at each surface. A prudent approach to minimize the Si-M contact area (both at the front and back) is through appropriate grid design. This consideration has led to the design of point-contact and buried-contact cells [20, 21]. This feature will also minimize the shadow loss for the incident light (except for back-contact cells). Another means of reducing the effect of Si-M interaction on the carrier loss is to employ a minority-carrier reflector consisting of a high–low field (such as n^+/n or p^+/p) under the metal. Several schemes have been developed for forming the back contact of wafer-based cells that include either a partial or total diffusion of the back surface. For a TF-Si cell fabricated by deposition, these features can be accomplished by tailoring the dopant profile during deposition.

Surface passivation of unmetallized regions can be further improved by oxidation. It has been shown that such passivation can reduce the surface-recombination velocity to about 100 cm/s [22, 23] – values that are essential for high-efficiency TF-Si cells. In wafer-based cells, passivation schemes are embodied in various configurations called *passivated emitter rear locally diffused* (*PERL*) and *passivated emitter rear totally-diffused* (*PERT*) as described in Chapter 7. Application of wafer-based passivation methods to TF-Si solar cells may not be straightforward. For example, oxide growth at conventional temperatures ($>1000^\circ$C) is not feasible for cells deposited on low-cost substrates like glass. However, it has been shown that low-temperature oxides grown by rapid thermal processing (RTP)-like processes can have excellent passivation properties [24]. Another approach to produce effective surface passivation can be the use of low-temperature plasma-enhanced chemical vapor deposition (PECVD) nitride. It is now well known that SiN (or oxy nitrides) produces a positive charge at the Si interface that results in excellent passivation characteristics for *p*-type Si [25, 26].

It is fruitful to briefly review some preliminary work that was instrumental in establishing the advantages of TF-Si solar cell structures and promoting further research. The capability of a thin cell to yield high performance with effective incorporation of light-trapping and surface passivation was demonstrated by a number of researchers. Table 8.1 compares the cell parameters of three devices of different thickness. One of them is a typical high-efficiency thick cell with light-trapping and surface passivation; the other two are thin cells fabricated by different processes. These cells include light-trapping, as well as oxide passivation. Figure 8.6 illustrates the structure of the devices.

The first device is a 44-μm-thick cell with n^+pp^+ structure [27]. Its surfaces are not well passivated, but include a good light-trapping design. The second device is a PERL cell fabricated on a 47-μm single-crystal, float-zone (FZ), wafer. The wafer was chemically thinned, and NF_3 was used during the oxidation step to reduce wafer-bending

Table 8.1 Parameters of two types of thin cells and comparison with a thick cell

Structure	Thickness [μm]	V_{OC} [mV]	J_{SC} [mA/cm^2]	Fill Factor [%]	Efficiency [%]
n^+pp^+	44	643	35.3	75.8	17.2
PERL	47	698	37.9	81.1	21.5
PERL	400	702	41.2	81.2	23.5

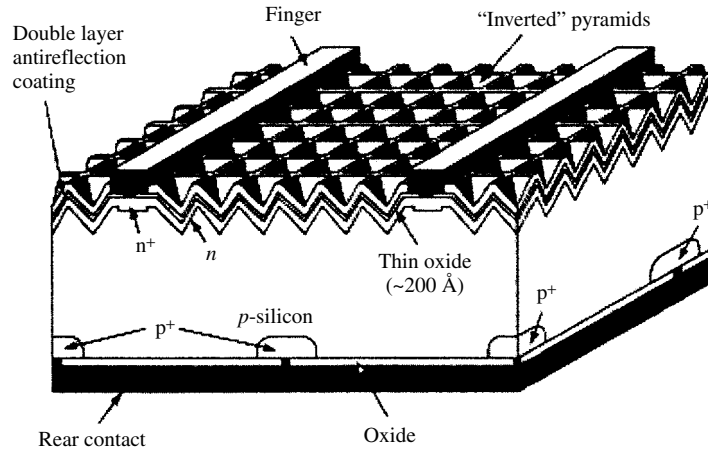


Figure 8.6 Structure of the test cells whose parameters are given in Table 8.1

due to oxide stress. The third device is also a PERL cell, but was fabricated on a 400-μm FZ wafer, and its device structure is similar to the 47-μm device. Figure 8.6 shows the structure of these devices. They include excellent passivation and light-trapping using the PERL process and inverted pyramids, respectively. The performance of the 44-μm n^+pp^+ cell is considerably lower than that of the other two cells, primarily due to inadequate passivation. Chapter 7 further discusses Si wafer–based solar cell technology. The results shown in Table 8.1 clearly demonstrate the potential of thin Si cells.

The table shows that light-trapping in the 47-μm cell can yield a J_{SC} that is only 3.3 mA/cm^2 lower than that of the 400-μm cell. Comparing the two PERL cells shows that it is possible to reduce the thickness by a factor of 10, and yet reduce the efficiency only by 10% (23.5% vs. 21.5%). It is interesting to note that the J_{SC} values of these cells are very close to the theoretical values, indicating very efficient light-trapping and carrier collection. From Figure 8.3, it is seen that inverted pyramids can produce J_{SC} values of 38 and 39 mA/cm^2 for cells having thicknesses of 44 and 47 μm, respectively. It is also seen that beyond a 250 μm cell thickness, the J_{SC} saturates at about 42 mA/cm^2.

Another cell that illustrates the high performance capability of thin cells was fabricated on a crystalline Si film made by zone-melting recrystallization (ZMR) [28]. Figure 8.7 illustrates the structure and processing sequence for ZMR cells. To minimize substrate issues, a single-crystalline Si wafer was used as a support. A thin layer of SiO_2 was deposited on the Si substrate as a stopping layer for impurity diffusion, and then a 60-μm-thick layer of poly-Si was deposited by a chemical vapor deposition (CVD) technique. The sample was then heated in vacuum by a line-shaped carbon strip, located just above the sample, to about 1200°C to recrystallize the poly-Si layer. A (100)-dominated surface was obtained with a growth speed of 0.2 mm/s, and grain sizes of millimeter to centimeter were reached. They achieved a high conversion efficiency of more than 14% for a 10 × 10-cm cell with $V_{OC} = 608$ mV, $J_{SC} = 30$ mA/cm^2, and $FF = 78.1\%$, and 16% for a 2 × 2-cm^2 cell with $V_{OC} = 608$ mV, $J_{SC} = 35.1$ mA/cm^2, and $FF = 77.1\%$. These results are quite impressive for solar cells fabricated on the poly-Si thin film obtained by ZMR technology.

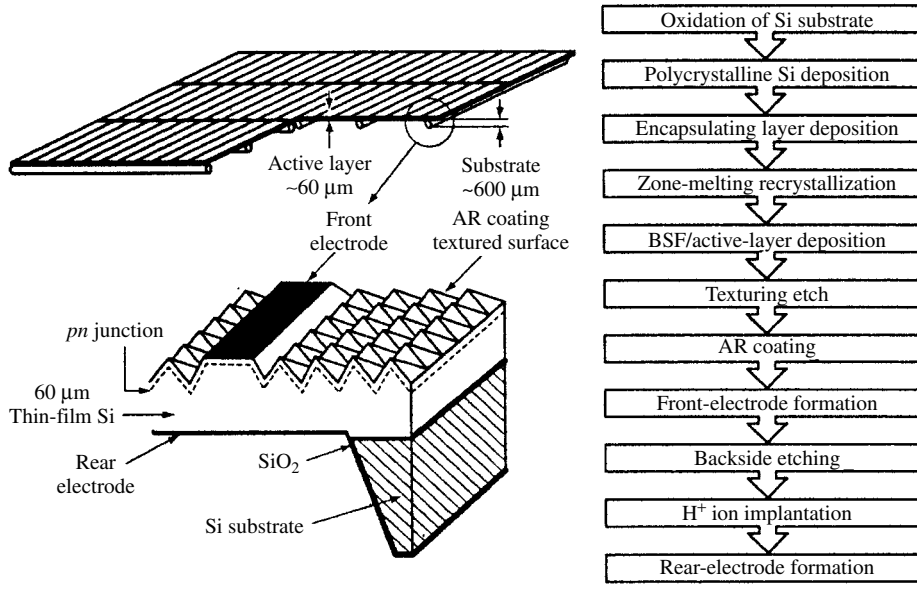


Figure 8.7 A schematic of the structure of the ZMR solar cell with a 60-μm poly-Si active thickness, and an illustration of the process steps involved in cell fabrication

Following the success of researchers who fabricated thin cells using conventional technology of wafer thinning and device processing, several laboratories began investigating alternate methods to produce thin films of Si in which production of Si film and cell processing are compatible. Some of the considerations that went into the qualitative cell design are identified below.

Efficient carrier generation. Thin Si films have an inherent drawback of being weakly absorbing in a significant region of the solar spectrum. A well-known solution to this issue is to incorporate light-trapping by creating surface roughness or texture. The initial attempts at fabricating TF-Si cells relied heavily on this approach. In most cases, back reflections were expected to come from refractive-index discontinuity at the backside of the film and the film support. Some of the approaches resemble those used in a-Si technology. But there are many issues that still remain unresolved about the light trapping in thin films. Some of the details of light-trapping and its applications to thin cells are discussed in the next section.

Efficient carrier collection. Although TF-Si cells are expected to perform well with poor material quality, the minority-carrier diffusion length must still be longer than the film thickness. An approach that can circumvent this restriction is to use a pin structure or multiple junctions, in a manner similar to that in a-Si solar cells.

Mechanical support. A thin Si film, less than 10 μm thick, is not a self-standing structure; it needs a support. Typically, two approaches may be used for supporting thin-film solar cells: (1) the cell is fabricated on a temporary substrate that has suitable properties to participate in the device processing, and it is then transferred or lifted off to a permanent support. In this case, the cell fabrication itself can be done using conventional processes,

and the permanent support can be a rather inexpensive material. The temporary support can be a Si wafer, which is reusable for growing other Si films. A liftoff CLEFT (cleavage of lateral epitaxial films for transfer) technique was originally developed for Ge- and GaAs-based cells using zone-melting recrystallization [29–32]. This technique is very successful, but is not warranted for a low-cost device. (2) A thin film of Si is deposited on a permanent substrate and is then processed into a solar cell. To use conventional processes, such a substrate must withstand high-temperature processing. For example, several laboratories have investigated development of high-temperature glass, thermally matched to Si [33, 34]. Alternately, newer processing methods must be developed that are compatible with low-cost substrates.

The current techniques for TF-Si solar cell fabrication are diverse and use single-crystalline, large-grain multicrystalline, or fine-grain microcrystalline Si films. Although this distinction appears to be related to grain size, in reality, it separates the technologies related to the growth of the film itself. The single- and multicrystalline Si films require high temperature $>800^{\circ}$C, use of a Si substrate, some type of epitaxial growth, and/or separation from the substrate. The fine-grain films (μ-crystalline) are deposited on a low-cost substrate typically at $<600^{\circ}$C. Thus, the approaches currently used in thin-film Si solar cell fabrication can be categorized on the basis of processing temperature and substrates used for depositing the thin film. These approaches include using a single-crystalline wafer for deposition of a thin-Si layer, which is subsequently separated from it (or removing a thin layer from a single-crystal wafer and transferring it to another substrate), depositing thin films on a multicrystalline Si wafer, and using a non-Si substrate. Table 8.2 summarizes various substrate types, processing approaches, and the cell efficiencies obtained in the laboratory. Recently, a number of papers have reviewed approaches for TF-Si solar cells [35–37]. Here, we have selected some approaches for further discussion and to illustrate general requirements for design and processing of thin-film Si solar cells.

8.2.1 Single-crystal Films Using Single-crystal Si Substrates

This approach involves separating a single-crystal thin film from a single-crystal substrate. Three techniques are currently being followed. One approach consists of generating a porous-Si layer on a single-crystal substrate, which is then followed by epitaxial growth of a thin film. The thin film is then separated from the substrate by chemically etching the porous-Si interface. Figure 8.8 illustrates various process steps used for this approach [38, 39]. The best efficiency attained by such cells is about 12.5%. The parameters for the best cell (4 cm^2) are $V_{OC} = 623$ mV, $J_{SC} = 25.5$ mA/cm^2, and $FF = 79\%$.

The second approach that has been suggested is similar to the "smart cut" method used in the microelectronics field for wafer-bonding [40, 41]. It involves implanting a Si wafer with hydrogen and creating a defect interface below the surface, followed by a separation of the surface layer. This technique has been used successfully to separate thin (<1 μm) layers of Si, but may not be cost-effective for making the 10-μm-thick, separable layers needed for solar cells. For the hydrogen atoms to penetrate such a thick layer required for PV applications, requires a very high-energy implant. No single-junction cells have been made using this approach. Recently, however, this approach has been used for making stacked multijunction solar cells that use GaAs-based and Si-based devices.

Table 8.2 A summary of various TF-Si solar cells [35–37]

Technique	Institution	Temperature [°C]	Substrate	Processing	Efficiency	Remarks
ZMR	Mitsubishi Electric Co.	>1300	SiO_2 on MG-Si	LPCVD 50–60 micron active layer, alkaline wet etching, P in diffusion, H passivation by ion implantation, DARC, backside etching for rear electrode	4.2%, 100 cm^2 (1993) 16.4%, 4 cm^2	Recrystallization speed = 1 mm/s
	FhG-ISE	>1300	Perforated SiO_2 on Si	No seeding, no texture, no defect passivation, interdigitated grid, 30 micron by thermal CVD	6.1%, 4 cm^2 (1996)	9.3% by Large-Area Recrystallisation (LAR)
		>1300	Graphite	Interdigitated grid, reactive ion etching	11.0%, 4 cm^2 (1997)	9.3% on ceramic, >17% expected for screen printing
SPC	Sanyo Electric Co.	600	Metal	PECVD *p*-type a-Si:H (SiH_4), ITO sputtering, evaporation of Ag finger contacts	9.2%, 1 cm^2 (1994)	10-um a-Si, 10–600 min annealing
LPE	Astropower Inc.	~1000	Graphite cloth	Gas phase P in diffusion, PECVD H passivation, photolithographic contacts, DARC	13.4%, 1 cm^2 (1994)	Si directly deposited on substrate, active layer = 80 μm
			n/r	$POCl_3$, Al gettering, H passivation, PECVD SiO_2 as ARC	14.6%, 1 cm^2 (1996)	Film thickness unknown
			n/r	n/r	16.6%, 1 cm^2 (1997)	Record thin-film Si on foreign substrate, no vacuum process

CVD	Univ. de Neuchatel	200	Textured TCO/glass	3.6-μm, μc-Si by PECVD at 100 MHz (SiH_4), doping by PH_3 and B_2H_6, ZnO/Ag back contact	8.5%, 1 cm^2 (1999) 13.1% a-Si:H/μc-Si 10.7% (1999)	Deposition rate <2 A/s, unstabilized, stabilized (other substrates possible)
	IMEC	>1000	p^+ SILSO	20-μm film by thermal CVD, DARC, no texture, SiN passivation, evaporated contacts	13.7%, 4 cm^2 (1997)	No H passivation 11.6%, 7.6% on SSP, 10.3% on RGS, 13.2% on EFG
	FhG-ISE	>1000	Silicon Sheets from Powder (SSP)	First deposition BSF, 30 micron by thermal CVD, no texture, no H passivation, SiN coating	8.00%, 4 cm^2 (1997)	Dep. Rate >l0 μm/min., 11.1% on SiLSO, 17.4% on FZ (inverted pyramids, local emitter, thermal oxide)
	Ecole Polytechnique	150	Textured TCO/glass	Polymorphous standard *p-i-n*, 0.4–0.8 micron *i*-layer.	9.30%, 0. 1 cm^2	Mixed a-Si:H/μc-Si matrix
	Canon Co	200–400	n/r	Standard *n-i-p* structures, Ag/ZnO back contact, >1 micron thick *i*-layer, VHF PECVD.	7.4%, 0.25 cm^2 (1999) 11.5% a-Si:H/μc-Si	Stabilized results
Excimer laser crystallization	Kaneka Co.	<550	Glass	Laser crystallization of 100-nm a-Si by PECVD (B_2H_6/SiH_4), followed by *n*- and *p*-type μc-Si and 6 micron intrinsic poly-Si (all PECVD), ITO front contact and Ag fingers.	10.1% 0.25 cm^2 (1997) 12.8% a-Si:H/μc-Si (1997)	Efficiency >14% expected

Note: n/r = not reported (proprietary reasons); BSF: back surface field; LPCVD: low pressure CVD; TCO: transparent conducting oxide; RGS: ribbon grown on substrate; EFG: edge-defined film-fed growth; ARC: antireflection coating; DARC: double layer ARC; SPC: solid phase crystallization; LPE: liquid-phase epitaxy

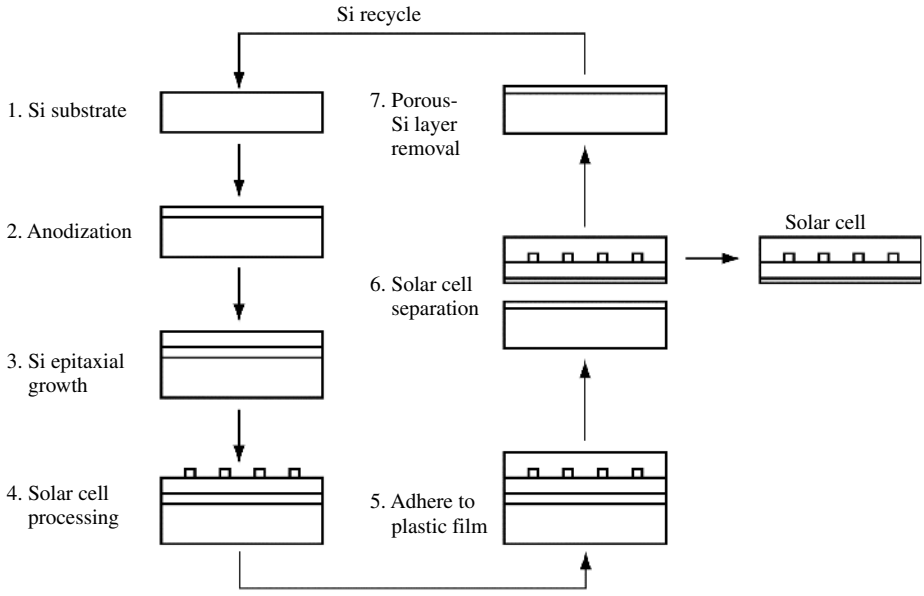


Figure 8.8 A schematic of various process steps involved in the use of porous Si as a separation layer

The third technique, called *epilift*, consists of depositing an epilayer on a patterned single-crystal wafer through a mask with openings along <110> directions [42]. The masking layer is exposed in a mesh pattern; the lines are 2 to 20 μm wide and spaced 50 to 100 μm apart. The growth faces have an (111) orientation, and the layer has a diamond cross-section giving it an antireflection texture. Figure 8.9 is a schematic of the cell configuration. Although this approach appears to have been commercialized, to date no cell performance has been reported.

8.2.2 Multicrystalline-Si Substrates

Thin Si films can be deposited on a multicrystalline Si (mc-Si) substrate by an epitaxial process. The general objective is to use a low-cost, large-grain, cast-Si wafer, such as a metallurgical grade feedstock, as the substrate and to deposit a high-quality thin layer on it. The epitaxially grown layer would be low in impurity content, as well as in crystallographic defects [43, 44]. There is interest in the use of liquid-phase epitaxy, as well as other vapor-phase deposition techniques for high-growth-rate. Some of the issues in this method include impurity contamination from the low-cost substrate, different growth rates of different grains, and prevention of substrate defects from propagating into the film.

One of the major problems in this method is that the solar cell is not amenable to efficient light-trapping designs because the backside becomes a Si–Si interface with little or no discontinuity in the refractive index for high reflectance from this interface.

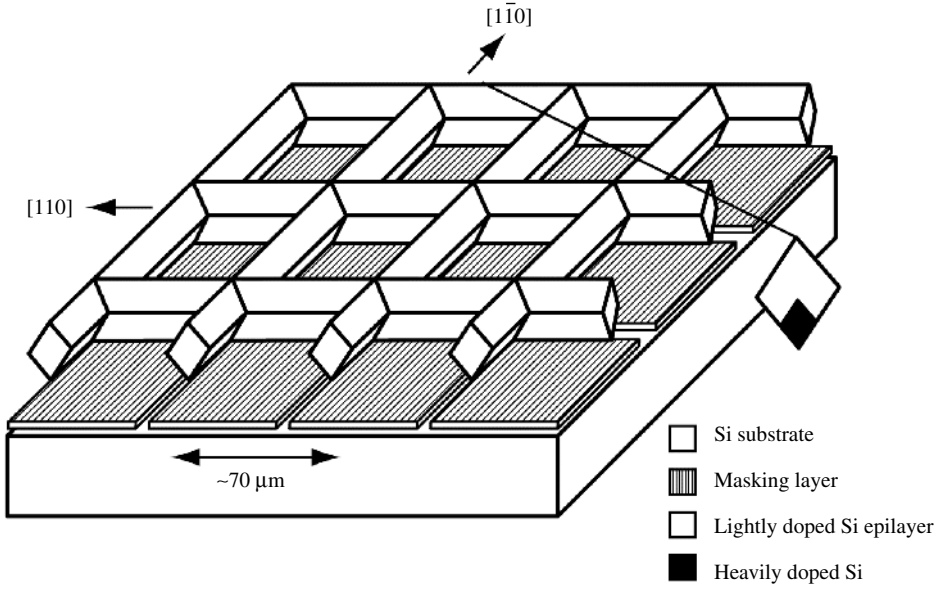


Figure 8.9 A schematic of the epilift process. Masking layer – Si_3N_4; epi layer is grown by LPE process. Typical epi thickness = 20 μm

8.2.3 Non-Si Substrates

The cost advantages of thin-film Si are likely to be realized if the support for the thin film consists of a low-cost substrate. Clearly, in this case, it is not possible to directly deposit a crystalline or mc-Si film. Use of a non-Si substrate has gained some prominence because of the recent success in depositing μc-Si on glass substrates at reasonably low temperatures. However, there are a number of challenges in making such a device. These challenges are related to both the design and the fabrication process(es) of the device. A major issue in the device design is identifying method(s) for efficient light-trapping that are compatible with a low-cost cell design. Theoretical calculations show that film thicknesses of about 10 μm are sufficient to yield photocurrent densities of 35 mA/cm^2 in fairly simple thin film device structures [19]. Other issues of device design are related to the carrier-collection approaches, such as the nature of junction(s), electrode geometry, and electronic and optical reflectors. Finally, all of these aspects must be achieved compatible with low-cost methods of cell fabrication.

A recent advance in Si-based thin-film technology has led to a new realm of thin-film μc-Si solar cells. The Kaneka group has developed a cell configuration called ***S**urface Texture and enhanced Absorption with a back Reflector* (STAR) [45, 46]. Figure 8.10 shows a sketch of the STAR cell. It consists of a glass substrate with a back-reflector on which an *n*-type μc-Si film is deposited by the plasma CVD process. Next, an *i*-type poly-Si film (typically 2 to 4 μm thick) is deposited at substrate temperature <550°C; this layer has no intentional doping, but is slightly *p*-type and has a carrier concentration

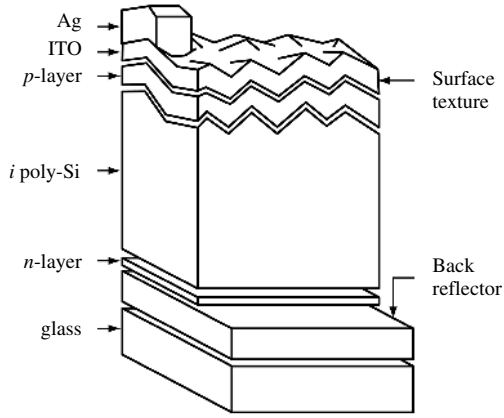


Figure 8.10 Illustration of the structure of a STAR cell. The μc-Si I-layer is typically 2 to 3 μm in thickness

Table 8.3 Measured $I-V$ parameters of STAR cells of different film thickness. The efficiencies are measured as the *Aperture efficiency*, which includes metallization, and *inside efficiency*, which excludes metallization area

Cell thickness	J_{SC} [mA/cm^2]	V_{OC} [mV]	FF [%]	Total area efficiency [%]	Active area efficiency [%]
1.5	22.9	526	77.2	9.3	–
2.5	24.39	510	75.5	9.4	9.8
3.5	26.12	480	74.8	9.4	9.8

of about 10^{15} to 10^{16}/cm^3. This layer is followed by depositions of a p-type Si film, a layer of ITO and an Ag-grid electrode. Some of the results obtained on the STAR devices are given in Table 8.3. This approach has shown astounding progress, manifested in a cell of about 10.4% efficiency, in a very short time. Initial theoretical calculations indicate that 16 to 18% cell efficiencies are possible with moderate grain size and some novel cell designs. It is important to note that the main part of the device uses an intrinsic material based on an nip structure. As pointed out earlier, the drift field within the i-layer can greatly increase the effective minority-carrier lifetime. However, because GBs exist within this region, the structure is prone to shunting effects that can limit the V_{OC} and FF. It is interesting to note that although the J_{SC} values increase with thickness, the V_{OC} values of the STAR cells decrease with increasing thickness. This behavior was explained in the previous section in Figures 8.1 and 8.2.

A novel approach for obtaining high V_{OC} could be to use thin-film material consisting of a mixture of a-Si and μc-Si. Although the physics of the μc-Si phase within an a-Si matrix is only beginning to be studied, it is likely that properties of such a composite phase can be tailored to exhibit behavior of either species. Thus, an a-Si-rich phase in the I-region can display higher V_{OC}, whereas a μc-Si-rich phase can yield higher J_{SC}. Indeed, there appears to be some evidence of this behavior. Researchers from Institut fur

Photovoltaic have fabricated TF-Si solar cells with a $V_{OC} = 600$ mV and an efficiency of 10.2%, using a two-phase material with a ratio of a-Si: μc-Si of 4:6 [47, 48].

Recently, a new structure has been proposed at the National Renewable Energy Laboratory (NREL) that integrates several processing advantages in the cell design and overcomes many of the substrate problems [49–51]. Figure 8.11 is a sketch of the cell, which consists of a *p*-type Si film, about 10 μm thick, deposited on a metal-coated glass substrate. An *n*-type junction can be made by any conventional method, followed by an AR coating and front metallization. As illustrated in the figure, the cell has texture on both the back (Si-metal) interface and the front surface. Some other important features of the cell are: (1) the thickness of the Si film is about 10 μm, with a preferred grain size in the range of 10 to 50 μm; (2) it is double-side textured with an AR coating on the front side, and the texture height is about 1 μm; and (3) the substrate material is low-cost glass, which is isolated by a metal layer from the Si layer. The back metal (at the Si-glass interface) has multiple functions – it serves as an optically reflecting back-electrode, a gettering medium, and an interface layer to relieve the stress resulting from thermal mismatch between the glass and Si.

Many cell designs use textured interface(s) and a reflecting back-electrode that is directly located on the thin cell. A disadvantage of the reflecting metallic or conducting oxide back-electrode is that it can lead to significant losses due to optical absorption. However, this loss decreases with an increase in the film thickness. The mechanism of metallic loss is discussed in detail later in Section 8.3.

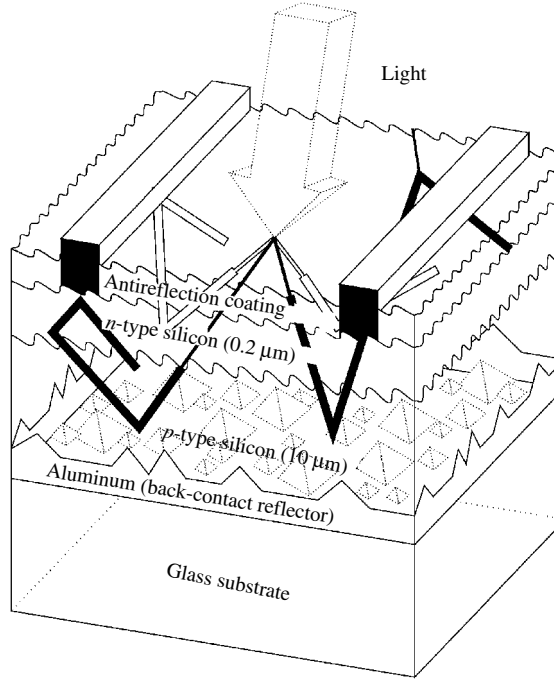


Figure 8.11 A schematic of the proposed thin silicon solar cell

The primary aim of exploiting a thin cell is to lower the bulk recombination losses that can lead to higher *FF* and V_{OC}. However, this must be done in a way that promotes good carrier generation and collection. Carrier collection can be a particularly difficult problem in a μc-Si cell because of carrier recombination at the GBs and the small grain size. The University of New South Wales (UNSW) has developed a multijunction cell approach to overcome this problem. The multijunction approach, reminiscent of a-Si cell designs, can circumvent the effect of poor material quality (i.e. short minority-carrier diffusion length) by providing closely spaced collecting junctions. Although the details of the cell material are not known, it is expected that the semiconductor film will consist of hydrogenated microcrystalline silicon. Such a film consists of polycrystalline Si with grain size typically <1 μm, hydrogenated grain boundaries, and material that contains a significant amount of amorphous tissue in the film. Recently, UNSW group reported 7.2% efficiency using this approach. Details of the device structure and processing methods were not disclosed. However, it is believed that a PECVD technique is used for Si deposition [52]. This type of material, deposited by plasma-assisted deposition, has been used by the Neuchatel group in Switzerland [53], which has reported an efficiency of 12%.

8.3 DESIGN CONCEPTS OF TF-SI SOLAR CELLS

Like any other emerging technology, the fabrication of TF-Si solar cells has, to date, followed empirical optical and electronic designs. The optical design aims at a high degree of light-trapping, such that the effective optical thickness of the absorber is similar to that of a much thicker wafer-based cell. It is generally known that one or more interfaces must be rough or textured to produce effective light-trapping. The electronic design of a TF-Si cell, particularly one using small-grain Si, is very difficult because such a structure has three-dimensional nonuniformity. Later in this chapter, we will illustrate some preliminary calculations using a software package that is currently being developed. However, qualitative designs can be derived using lumped material parameters such as effective minority-carrier lifetime, effective surface-recombination velocity, and absence of local shunting.

The material quality of a TF-Si cell should be such that the volume recombination is significantly lower than its thick-cell counterpart. In a thin-Si cell, the carrier recombination is expected to arise primarily from impurities, grain boundaries, and interfaces. Impurity effects can be minimized by the use of Al gettering, whereas a large ratio of grain size/Si thickness can minimize shunting effects of grain boundaries. A more difficult task is that of interface passivation, particularly if the Si film is in contact with a substrate material that may be conducting.

Unfortunately, cell design and processing are intimately connected. We will, however, attempt to consider a representative cell structure (that has nearly all the elements of any TF-Si cell) and illustrate optical and electronic design concepts. The emphasis will be on the physics and methods of designs. The cell structure we consider is illustrated in Figure 8.12. It consists of a glass substrate coated with a layer of a metal such as Al. A thin layer of *p*-type amorphous or fine-grained μc-Si film is deposited on the Al-coated substrate. The deposited film may be grain-enhanced by using one of the techniques described in the next section describing deposition techniques. In particular, it must employ a technique that allows the substrate temperature to remain below its softening point. The grain-enhanced film forms the base region of the cell. The method of

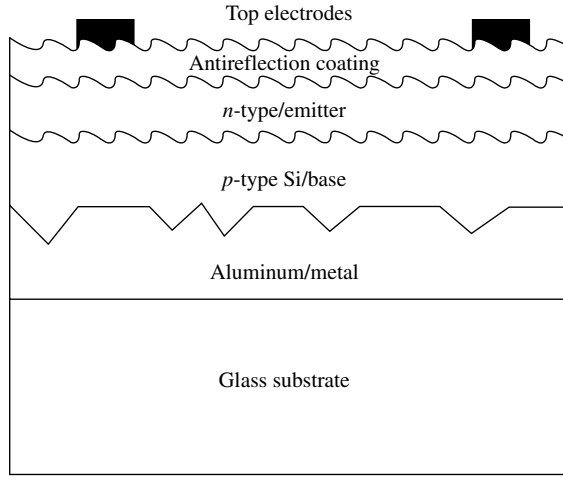


Figure 8.12 A sketch of the generic device structure used for cell design discussion

deposition for amorphous or μc-film is not critical to the grain-enhancement process, and can be done by any technique that can produce high throughput and good material quality. Thus, a variety of film-deposition techniques such as sputtering, PECVD, hot-wire CVD, and photo-CVD can be used for Si deposition. The junction is expected to be fabricated by a low-temperature process, such as the deposition of an n-type, μc-Si layer. Use of low-temperature deposition technologies is a major difference between TF-Si and the conventional wafer-based Si solar cells. In addition to maintaining the integrity of the substrate and rear metal layer, a low-temperature process can minimize the diffusion of dopant along grain boundaries. Other techniques that can exploit defect-engineering concepts also have the potential of forming an n/p junction at low temperatures. An important feature of the device configuration of Figure 8.12 is the interfacial Al film. This layer functions as a multipurpose buffer layer. It participates in grain enhancement, acts as an ohmic back contact, serves as an impurity-gettering layer, and provides back reflection for effective light-trapping.

Qualitatively, one can identify various built-in features of the cell structure that potentially can make it a high-efficiency design. These include the following:

1. An interfacial texture to promote light-trapping. Some details on the nature of the texture, such as shape, height, and location(s) of the texture, are determined in the next section.
2. The use of a backside optical reflector to enhance light-trapping.
3. A large grain-size-to-film-thickness ratio compatible with high V_{OC} and FF. Large grain size is obtained by solid-phase grain growth using photo-excitation (e.g. IR (infrared) lamps, lasers, RTA).
4. A built-in impurity-gettering mechanism that can improve the material quality of the deposited Si. It is common for thick Si wafer-based solar cell processing to require advanced techniques, such as impurity gettering and hydrogen passivation. The proposed structure offers a simple means of using Al gettering. As discussed in

the next section, phosphorous diffusion and Al alloying are very effective impurity-gettering methods.

8.3.1 Light-trapping in Thin Si Solar Cells

As pointed out earlier, a thin-film Si solar cell requires highly efficient light-trapping designs to absorb a significant fraction of the incident sunlight and to minimize reflection. Light-confinement approaches have been discussed in detail for wafer-based cells [54]. Here, we will concentrate only on thin cells. A true optical confinement (or light-trapping) implies that once the light is transmitted into a wafer, the structure sustains the light without transmission from the surfaces. In electromagnetic devices, this is referred to as a *guided wave*. In thin dielectric films used as waveguides in integrated optics, the guided waves use total internal reflection and some specific coherent features to achieve this condition. In a solar cell structure, such modes are not possible. The modes of the structure are radiation modes. Thus, light-trapping as used in solar cells is a misnomer. However, it is supposed to imply relative enhancement of optical absorption over the planar configuration. This necessitates two features of the structure: (1) capability of increasing the optical path of the light transmitted into the cell, and (2) making the structure asymmetrical, such that reflectance at two surfaces is different. An additional requirement in a solar cell is to minimize the reflectance of the illuminating sunlight.

Antireflection (AR) coatings and front-side texturing can be used to fulfill this goal. Choosing appropriate materials for AR coatings and designing the configuration of the front-side texture are among the tasks for optical design of solar cells [55]. The only way to enhance light-trapping in a terrestrial (completely illuminated) solar cell is to use rough surfaces/interfaces instead of planar structures. An analysis of light-trapping concepts using thermodynamic equilibrium conditions suggested that a semiconductor slab with rough surfaces can produce an effective increase in the optical path by a factor of $2n^2$, where n is the refractive index of the semiconductor [5]. The shape of the surface/interface of the device will play a critical role in the light-trapping process. Finding the most appropriate surface configuration that can maximize light-trapping is one of the major goals of optical design of the solar cell. Depending on its morphology, a rough surface can be either Lambertian reflective (a random roughness that causes scattering to follow a $(\cos\theta)^2$ distribution) or geometric reflective (textured surface having a feature size larger than the wavelength of light). Only the surface/interface structure that is geometric reflective will be investigated in this chapter. A number of software packages are available for calculating absorption in a solar cell. These include Sun Rays, Texture, and PV Optics [56–58]. Of these, *PV Optics* is the most general and allows investigation of many features as will be shown later.

One of the important issues in a thin-film solar cell that is seldom considered for thick cells is the metallic absorption loss. All solar cells need contacts, and in many cases, contacts may be expected to serve as optical reflectors. For example, a-Si solar cells use Al or Ag as part of the back-reflector. Unfortunately, a metal surface is not totally reflective. Typical reflectance at an air–metal interface may be quite high, ~90% for Al and 95% for Ag. However, when such a metal is used in a solar cell, the metal loss is enhanced. The reflectance at the semiconductor metal interface is lower than that at the air–metal interface; the light that is transmitted into the metal is absorbed there,

contributing to the enhanced loss. Furthermore, if the interface is rough or textured, the area of the metal is increased contributing to a higher loss. In a good light-trapping cell design, the light at the weaker end of the spectrum can encounter many reflections within the cell. At each reflection, a part of the light incident on the metal will be absorbed instead of being reflected back to the semiconductor. The photon loss due to metal will become a severe problem when the thickness of the cell decreases and the number of passes increases. Minimization of the metal loss is also an important task in the design of the solar cell.

In this chapter, the optical-modeling software, *PV optics*, is used to discuss the optical design of TF-Si cells. We use the example of a single-junction thin-film solar cell illustrated in Figure 8.12. The results of a series of calculations will be presented to provide information on the influence of various features of the cell configuration on the optical properties of the device, which can help select the best configuration for single-junction Si thin-film solar cells. It should be emphasized again that the optical design of the cells is only an optimization process of the cell structure which was itself determined by other design criteria. The results of the optical design can be very different for different structures.

8.3.2 Description of PV Optics

PV Optics is an optical-modeling software developed by Sopori *et al*. at NREL [59]. This software can calculate a variety of optical parameters for multilayer devices operating in air or within an encapsulated module. These parameters include reflectance, transmittance, distribution of absorbed photons in each layer, and integrated absorbance weighted with an AM1.5 spectrum to determine the MACD for each layer. The method is the numerical equivalent to shining a beam of light on the sample that has an arbitrary surface morphology. This beam is split into a large number of beamlets that impinge on a small region of the surface. Each beamlet is permitted to propagate within the sample, and we keep track of its entire path while it undergoes reflection, transmission, and absorption. In this manner, each beamlet bounces back and forth within the sample. The net energy absorbed at each plane within the sample is determined. This procedure is continued for each beamlet until the energy in the beam is reduced to nearly zero. This process yields the net reflection, transmission, and absorption in the device structure. *PV Optics* uses a combination of ray and wave optics to suitably address thin and thick media, and metal optics.

In our calculations, MACD is used to evaluate the ability of the device to absorb photons in the semiconductor layers. It is defined as the current density that could be generated if every photon (in AM1.5 spectrum) absorbed in the semiconductor layer would generate an electron-hole pair and this pair would contribute to current that is collected by the external circuit. Another parameter, metal loss, is used to estimate the amount of photons lost at the semiconductor/metal interface. Metal loss is defined as the current density that could be generated if every photon (in AM1.5 spectrum) lost at the semiconductor/metal interface would generate an electron-hole pair and this pair would result in a current that is collected by the external circuit. Thus, better devices have higher MACD and lower metal loss.

It should be pointed out that a metallic back-reflector requires a careful design, because such a reflector is accompanied by a loss of photon flux caused by free-carrier

absorption. The amount of the absorption loss depends on the texture parameters, the thickness of the film, and on the metal itself. The approach for minimizing the reflector loss in thin amorphous-silicon solar cells is discussed in several papers [60, 61]. Here we use a similar approach to optimize parameters for the cell structure shown in Figure 8.12.

Figure 8.13(a–d) shows the calculated optical properties of the cells with the basic structures shown in the inserts of these figures. The MACD and metal loss under different conditions are also denoted in these figures. In this calculation, the thickness of the cell considered is 10 μm and the back-contact metal is Al. The texture height is 1.0 micron. From this figure, it can be seen that as long as either surface is textured, the MACD of the device will be higher than that of double-side planar cells, even if metal loss is higher in some cases. Another observation that can be made from these figures is that the MACD will be improved more (about 30%) in double-sided textured or front-side textured/backside planar cells. Double-sided textured cells will yield the highest MACD. This conclusion suggests that double-sided textured or front-side textured structures should be used in the design of solar cells. The important point is that it is more effective to

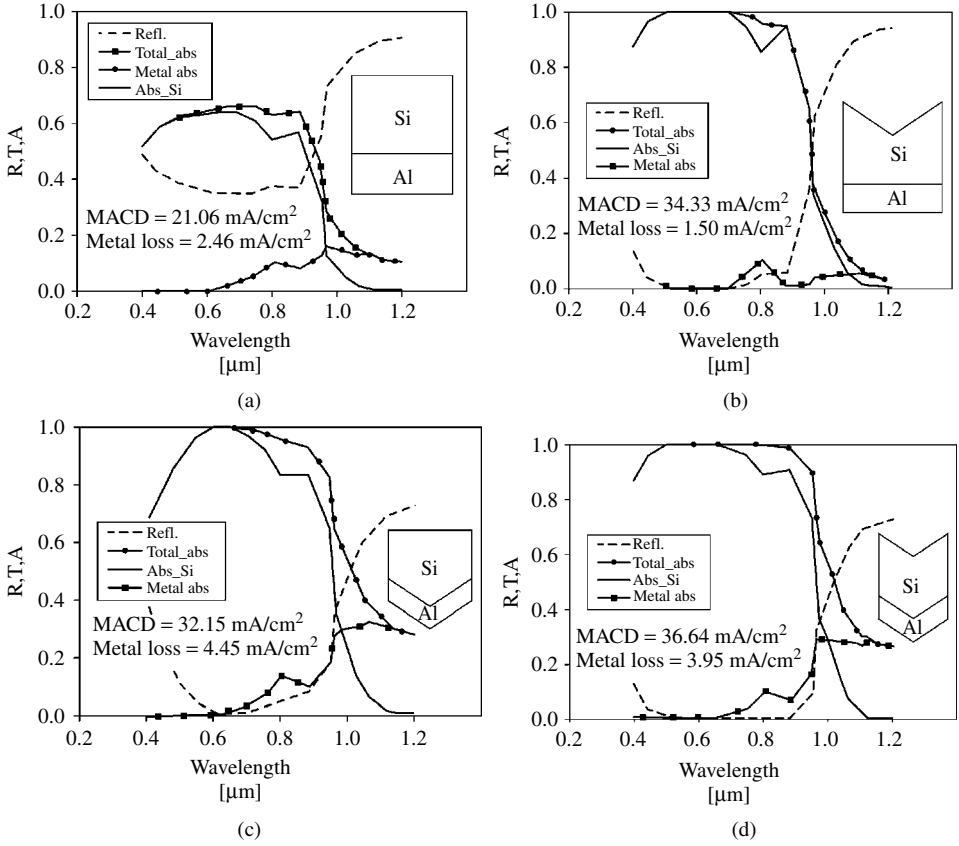


Figure 8.13(a–d) Calculated reflectance (R), transmittance (T), and absorbance (A) of a single-junction cell under different surface configurations. The cell structures are shown in the inset of the figures. Absorber thickness = 10 μm. (a) Planar, (b) FTBP, (c) FPBT, and (d) DT

scatter light entering the cell than at the back-reflection. The same conclusion has been reached by other a-Si solar cell researchers [62, 63]. Another key observation is that any textured surface, front or back, drastically reduces the reflection losses (note how high they are in Figure 8.13(a) between 400 and 1000 nm).

Figure 8.14 shows calculated metallic loss (as mA/cm^2) arising because of the Al back-reflector as a function of the film thickness for three cases of the texture: (1) front-polished and back-textured (FPBT), (2) front-textured and back-polished (FTBP), and (3) double-sided textured (DT). These calculations assume an AR coating consisting of 710 Å Si_3N_4 and 100 Å of SiO_2. It is seen that the metallic absorption is lowest for back-polished configuration for all film thicknesses, and that all losses decrease as the Si thickness increases because less light reaches the back contact.

To further understand the effect of thickness on various optical losses, Figure 8.15 shows the calculated values of reflectance, the Si absorbance, and the metallic loss as a function of wavelength for two different values of the cell thickness. The cell structure, depicted in the inset, consists of front-polished and back-textured surfaces; the cell thicknesses are 5 μm and 15 μm. From this figure, we can conclude that an increased absorbance in the thicker Si film results not only from increased single-path absorption but also because of a reduction in the metal loss associated with reduced energy impinging at the back semiconductor/metal interface.

The details of light-trapping presented in Figures 8.13 to 8.15 provide insight into various mechanisms that control dependence of J_{SC} on the absorber thickness, and the losses arising from metal contacts, for different texture configurations. We can now examine the influence of thickness of a single-junction Si cell on the MACD for different texture configurations. Figure 8.16 shows the calculated MACD as a function of the Si-film thickness for three surface configurations: FTBP, FPBT, and DT. The texture height used in these calculations is 1 μm. It is seen that in all cases the MACD nearly saturates after

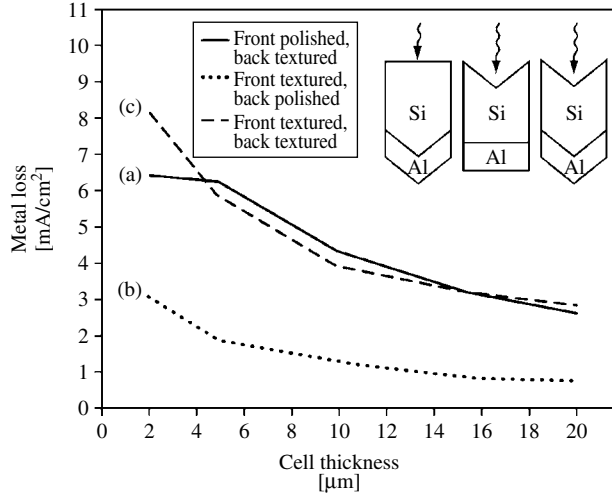


Figure 8.14 Metal loss due to absorption by an Al back-reflector as a function of thickness for three different cell structures. Texture height was 1.0 μm

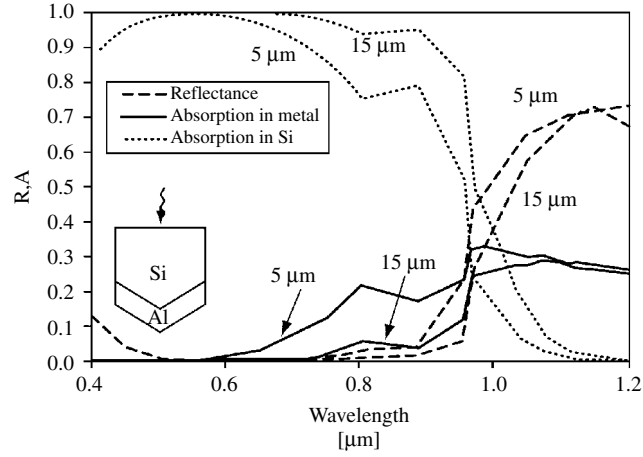


Figure 8.15 Calculated values of reflectance, Si absorbance, and metal absorbance for two cells, 5 μm and 15 μm thick, showing mechanisms of the enhanced absorption. The cells have front-polished and back-textured configuration. Texture height was 1.0 μm

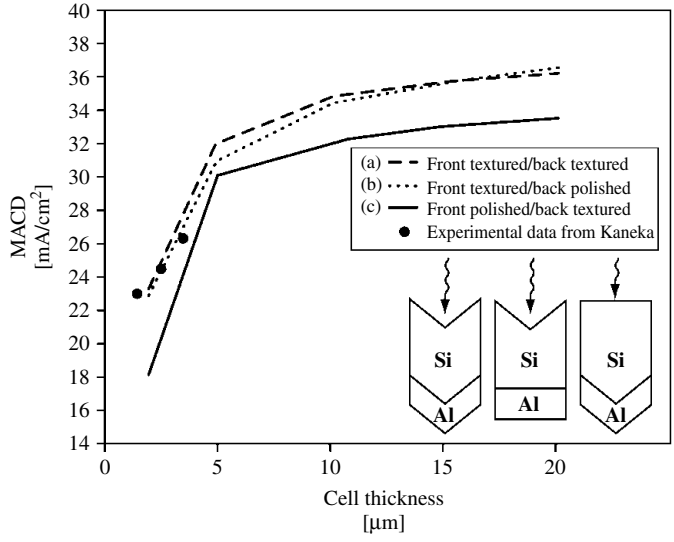


Figure 8.16 Calculated maximum photocurrent generated in a cell with light-trapping involving a metal reflector

the film thickness has reached about 10 μm. Furthermore, texturing at both interfaces appears to be the most suitable cell configuration. Figure 8.16 includes experimental data from Kaneka [45, 46]; the solid points show excellent agreement with calculated results. One can deduce the effect of light-trapping by comparing J_{SC} values in Figures 8.1 and 8.3 for the same thickness of the cell. In Figure 8.1, the thickness required to generate a J_{SC} of 34 mA/cm^2 is 80 μm. However, the structures of Figure 8.16 can produce the same values of J_{SC} for a thickness of about 10 μm – a factor of 8 thinner.

Figure 8.16 shows that the MACDs in FTBP and DT cells are much higher than that of FPBT cells, although the metal loss of DT cells is not too different from those of FPBT cells. It can be seen that, with proper optical design, the MACD tends to saturate when the cell is in excess of 10 ~ 15 μm. Thus, from the view of the optical designer, the thickness of thin-film solar cells should be around 10 ~ 20 μm to obtain maximum benefit. Indeed, it is expected that 10 ~ 20-μm-thick cells with proper light-trapping will generate the same J_{SC} as 300-μm-thick cells.

Several processing techniques that can produce texturing in the silicon solar cells were mentioned earlier. They can produce texture with vastly different shapes. We will now briefly discuss the influence of different texture shapes on the properties of thin-film solar cells. For the pyramid-shaped texture pits, three parameters will control the properties of the texture structure: the depth, the bottom angle, and the density of the texture pits. A set of calculations is performed on the cell structure shown in Figure 8.13 using different texture configurations. The terminology used in the text is as follows: the pyramid-shaped pits on the textured surface are simply called *texture pits*. The geometry parameters of the texture pits, such as the depth and the bottom angle, are illustrated in Figure 8.17. When the density of the texture pits is investigated, the ratio between the area of the textured part and the whole area is called area ratio (in which the "area" of a region is actually the length of the corresponding region).

8.3.2.1 Influence of the texture height on MACD

As pointed out earlier in this chapter, texture is typically generated by exposure of (111) crystallographic planes that subtend an angle of 70.4° with each other. To investigate the effect of the texture height on the photocurrent generation, we will assume that pits, having a texture angle of 70.4°, cover the whole surface of the cell. Calculated MACD for a solar cell having a 10-μm-thick Si absorber is about 31 mA/cm^2. This value is nearly independent of the texture height (between 0.1 and 2 μm), when the bottom angle remains unchanged. This indicates that very shallow texture pits can be used in the device without degrading performance. This conclusion is important to the thin-film cell structure, which will not accommodate deep pits.

8.3.2.2 Influence of the bottom angle of the texture pits on MACD

In a previous section, we mentioned that texturing produced by chemical etching will result in a fixed texture angle. Many other ways of texturing have been developed recently for

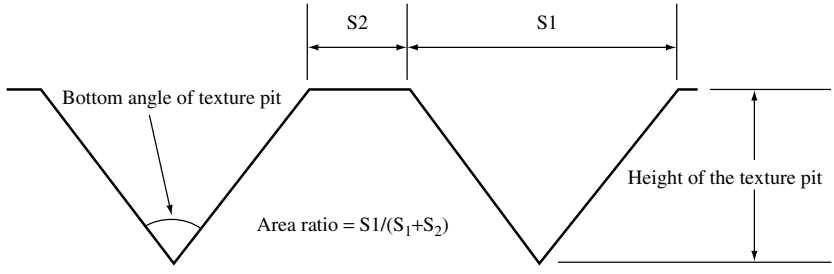


Figure 8.17 The geometry and the terminology used in the texture shape study [19]

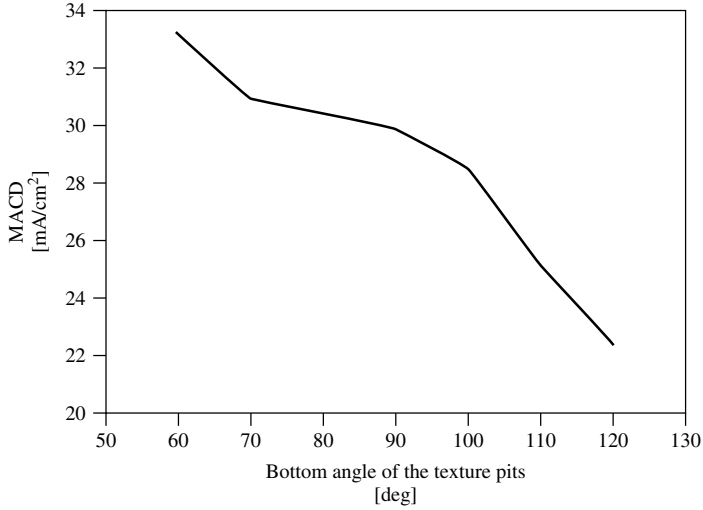


Figure 8.18 The calculated MACD as a function of the bottom angle of texture pits. Si thickness = 10 μm

wafer-based solar cells that use mechanical grooving and surface-shaping techniques. We have also indicated that in deposited films, the texture angle can be related to the grain size. It is useful to investigate the influence of the texture angle of the pits on the cell performance. Here, we show results of calculations performed with *PV Optics* to study the influence of texture angle on the cell current. We assume a 10-μm-thick absorber layer, having a texture pit 1 μm deep on the front side while the backside is planar, and we change the bottom angle from 60 to 120 degrees. Figure 8.18 shows the calculated MACD as a function of the bottom angle of the texture pits. From these results, it can be seen that MACD will drop by about 30% when the bottom angle changes from 60 to 120 degrees. It is important to point out that the dominant effect of changing the bottom angle is to change the reflectance. Analysis of the reflectance spectra shows that the reflectance increases with an increase in the texture angle (i.e. as the surface becomes smoother) in the wavelength range of 0.4 μm to 0.9 μm. In this wavelength range, the reflectance is primarily from the front surface. Therefore, to get better performance, "sharper" texture pits should be used in the cell design. In wafer-based Si solar cell processing, sharp texture is produced by reactive-ion etching (RIE). In the past, RIE texturing has resulted in cells with lower V_{OC} due to shunting. Such shunting results from breakage of the peaks and (or) penetration of metal through the junction during processing. However, this technology is now used commercially by some solar cell manufacturers.

8.3.2.3 Influence of density of the pits

In some processing techniques, the texture pits cannot cover the surface totally. This example will investigate the relation between the optical properties of the cells and the density of the pits.

Figure 8.19 evaluates the influence of pit density on MACD and metal loss. The MACD increases as the fraction of texture pit area increases.

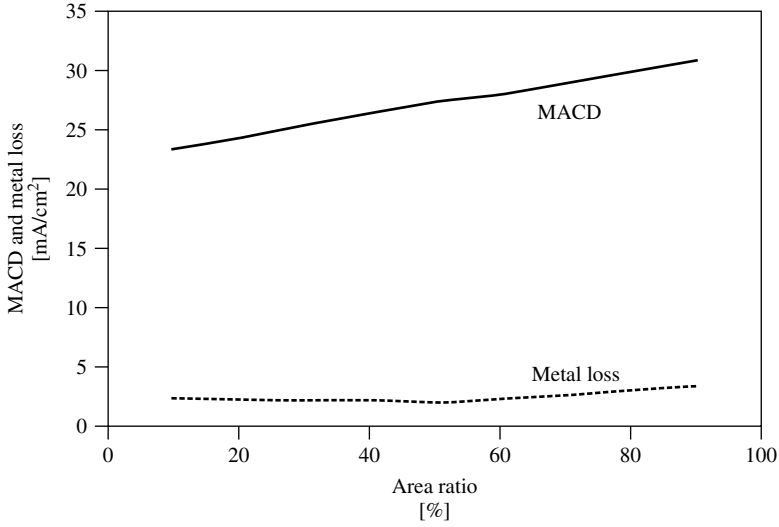


Figure 8.19 Calculated MACD and metal loss as functions of area ratio for a Si cell with 10-μm-thick absorber

8.3.2.4 Summary from optical modeling

From the analysis performed in the preceding sections, we can make some conclusions about the structure of the thin-film solar cells:

1. The thickness of the cell should be 10 to 20 μm in order to get satisfactory J_{SC}.
2. The best structure will be front-surface-textured/backside-polished or front-surface textured/backside-textured.
3. The texture pits should be as sharp as possible, and should occupy the entire surface of the cells.

8.3.3 Electronic Modeling

A generalized electronic model of a TF-Si solar cell should address features such as nonuniformities arising from grain boundaries (GBs) and intragrain defects, as well as detailed optical generation resulting from light-trapping, as illustrated in the previous section. Clearly, this requires a 3-D modeling capability. 3-D modeling is also needed to include metal contacts appropriately. Unfortunately, no modeling package suitable for this purpose is available at this time.

There are two major problems in building an appropriate modeling software for a polycrystalline Si device. First, it is difficult to model electrical fields, recombination, and boundary conditions at GBs and other crystal defects (later we will show one approach to handle fields associated with defects). Second, it is difficult to assign values to parameters associated with defects and GBs. This is because the grain-boundary parameters depend strongly on the interactions of these defects with impurities. For example, clean GBs have been found to have very little electron beam–induced current (EBIC) contrast

which implies very little recombination. The contrast increases with increased impurity segregation.

A good deal of preliminary understanding of the design of a TF-Si solar cell can be acquired through modeling a single-crystalline TF-Si cell. Such a cell may be considered to have uniform material properties, but inclusion of metallization can introduce large spatial nonuniformities (because shadowing effects can be more pronounced in a thinner cell). However, for a first approximation, 1-D analysis can yield reasonably accurate results. In the beginning of the chapter, we used *PV Optics* and PC1D to show dependence of J_{SC} on the cell thickness and V_{OC} on the thickness and the surface-recombination velocity, respectively [64, 65]. Another electronic modeling package, used by most a-Si cell designers, is AMPS (analysis of microelectronic and photonic structures) [66]. To date, PC1D is only a 1-D package and is valid for uniform, homogeneous material without GBs or intragrain defects. Because PC1D does not include detailed light-trapping, a good 1-D modeling would still require a combination of an optical model like *PV Optics* and PC1D.

Accurate modeling of a polycrystalline TF-Si solar cell is complicated not only because of GB issues but also because of a recently observed phenomenon known as *defect-clustering*. It is observed that polycrystalline Si exhibits segregation of intragrain defects into grains of some specific orientations. Thus, one is able to find grains of zero-defect density adjacent to very heavily defected grains (defect clusters). The formation of defect clusters in polycrystalline Si is attributed to relief of thermal stress (produced during crystal growth or deposition) through dislocation generation by grains having certain preferred orientations. These orientations have the lowest-yield stress for the growth or deposition conditions [67]. When the defects are clustered, it is expected that the potentials introduced by different defects may couple with each other if they are close enough spatially, so that some second-order extra energy levels, or even an energy-band-like structure, will be generated. But, unfortunately, there is so far no study on this subject. As a result, modeling of TF-Si cells must include laterally nonuniform material.

A first-order approximate (but simple to handle) model for a polycrystalline TF-Si solar cell is to regard cell performance as being controlled by the spatial variations arising from changes in the grain-to-grain properties such as dislocation density. Each grain can be assumed to be uniform. In this approximation, one can embed GB effects into lumped series resistance that interconnects various grains through a network model. This model was developed at NREL to predict the effects of spatial nonuniformities in a large-area solar cell [68, 69]. Here, the total cell consists of a parallel combination of a large number of smaller cells (in this case, each cell corresponding to a different grain). The characteristics of each cell are determined by the local properties of that grain.

Figure 8.20 illustrates the network model. The solar cell is divided into an array of diodes, where each diode is small enough to assume a uniform distribution of defects. Each node in the matrix depicts a local cell, connected to other cells by a resistor representing the series resistance. The series resistance arises from a number of sources that include the sheet resistivity of the emitter in an n/p device.

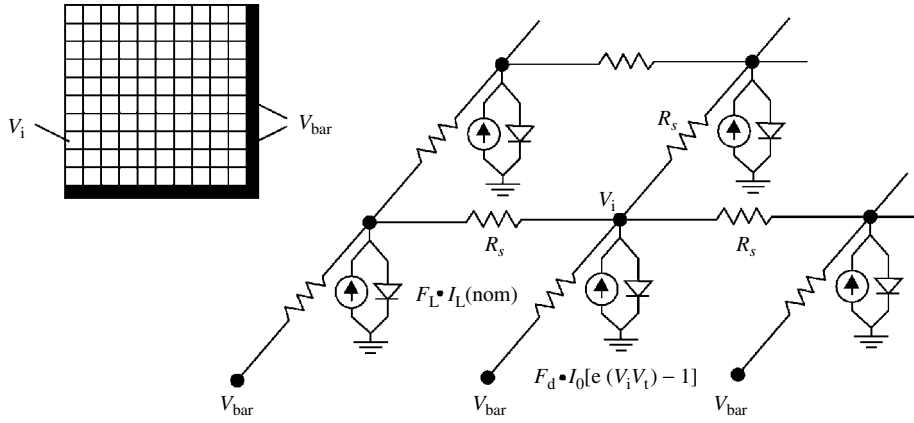


Figure 8.20 A network model of a solar cell showing voltage and current sources corresponding to dark (indicated by subscript d) and illuminated (indicated by subscript L) conditions, and the resistive components due to the sheet resistivity of the emitter

Current–voltage (I–V) curves of a cell are synthesized using diode equations for individual cells. For each cell, we can write the total current density, J, as

$$J = J_{ph} - J_{dark}(V)$$

where J_{ph} and $J_{dark}(V)$ are the photogenerated and the dark-current densities, respectively. The dark current of each local region of a known defect density, is described by

$$J_{dark} = J_{01}\{\exp(eV/kT - 1)\} + J_{02}\{\exp(eV/2kT - 1)\} + J_{03}\{\exp(\beta V - 1)\} \qquad (8.1)$$

The first two terms in the above equation are well-known expressions for representing band-to-band and midgap defect recombination respectively in a p-n junction (see Chapter 3). The last term is added to include tunneling currents (as a generalized expression) that occur in heavily defected regions. These tunneling currents arise because of a carrier-hopping mechanism, which is independent of temperature; here β is a constant needed to fit the specific voltage dependence. Hence, a local cell element (i, j) in the matrix is represented by a current source comprising J_{01ij}, J_{02ij}, J_{03ij}, and a corresponding light-induced current density $J_{ph,ij}$. For room temperature operation, the tunneling current can be neglected. One can represent all current components of cell elements in terms of nominal currents of defect-free devices. Accordingly,

$$J_{01ij} = J_{01} \bullet A_{ij} \bullet \exp(eV/kT - 1) \text{ and}$$
$$J_{02ij} = J_{02} \bullet B_{ij} \bullet \exp(eV/2kT - 1) \qquad (8.2)$$

where J_{01} and J_{02} represent dark-saturation current densities in the nominal "defect-free" device element. A_{ij} and $B_{i'j}$ are the factors representing the ratio of dark current

normalized by the nominal "defect-free" current for each component device. A finite-element computer code, written in Microsoft Excel, is used to analyze the network.

$$V_{ij} = \frac{F_{\mathrm{phi}j} I_{\mathrm{ph}nom} - [A_{ij} I_{01nom}(\mathrm{e}^{V_{ij}/a\,kT} - 1) + B_{ij} I_{02nom}(\mathrm{e}^{V_{ij}/b\,kT} - 1)] + \left(V_{\mathrm{neighbors}}\right)/R_s}{N/R_s} \tag{8.3}$$

where
V_{ij}: Voltage at a node ij
$F_{\mathrm{phi}j}$: Fraction of short-circuit current at the node compared to nominal defect-free short circuit current (<1)
I_{01nom}, I_{02nom}: Nominal short-circuit current per node
A_{ij}, B_{ij}: Fraction of dark currents at the node (>1)
$V_{\mathrm{neighbors}}$: Voltage of the nearest-neighbor cells
N: Number of nearest-neighbor cells
R_s: Electrical resistance between cells.

This above network model allows the synthesis of the I–V characteristics of the total cell. Here we will use this model to illustrate the influence of crystal defects on the cell performance. We first consider a spatially uniform, defect-free solar cell; the cell performance is limited by the material properties such as impurity content and the minority-carrier lifetime. The values of various current components are assumed to be: $J_{\mathrm{ph}} = 35$ mA/cm^2, $J_{01} = 3.6 \times 10^{-6}$ mA/cm^2, $J_{02} = 4.5 \times 10^{-10}$ mA/cm^2. Because this cell is uniform, all device elements in the network model of this cell are identical. Figure 8.21 shows the I–V curve (dotted line) of the total cell. The parameters of the total cell are $V_{\mathrm{OC}} = 650$ mV, $J_{\mathrm{SC}} = 34.5$ mA/cm^2, $FF = 81\%$, and Efficiency $= 18.4\%$. Now, we consider another cell with same material properties but having 20% of the area covered by heavily dislocated regions. The network model of this cell consists of two kinds of device elements. One similar to those of the defect-free cell, and the other representing defected regions. The parameters for the defected device elements are determined from

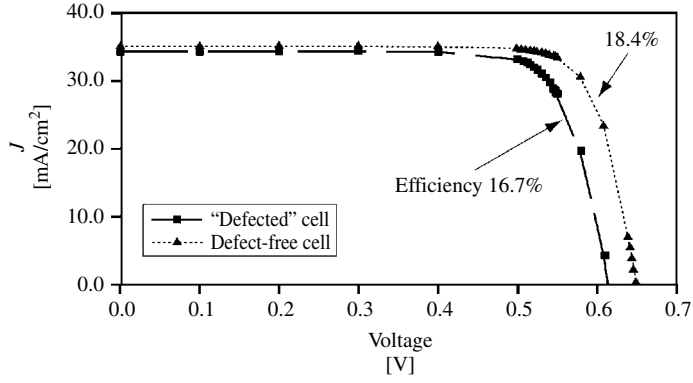


Figure 8.21 Calculated I–V curves of defect-free and defected cells (20% area with defects) showing degradation due to defected regions

experimental measurements, as $J_{ph} = 24.5$ mA/cm^2, $J_{01} = 3.6 \times 10^{-5}$ mA/cm^2, $J_{02} = 4.5 \times 10^{-8}$ mA/cm^2 [...]. These low-performing devices, constituting 20% of the total device elements, are now randomly distributed in our network model. The resultant I–V curve for the total cell is also shown in Figure 8.21 (solid line). The parameters of the total cell with defects are $V_{OC} = 620$ mV, $J_{SC} = 32.7$ mA/cm^2, $FF = 75.8\%$, and Efficiency = 16.7%.

It is seen that all the parameters of the "defected" cell are lower than that of the "defect-free" cell. However, the major reduction is in the V_{OC} and the FF. The reduction in V_{OC} is 30 mV whereas J_{SC} is reduced by 1.45 mA/cm^2. It should be pointed out that in a "defect-free" cell, a reduction of 30 mV in V_{OC} would require a large reduction in J_{SC} (in accordance with the cell equation). This disproportionate reduction in the voltage is caused by increased recombination, which manifests as shunting, due to defected regions. Such shunts represent sources of internal power dissipation within the cell. The network model is directly applicable to multigrain solar cells, if the distribution of defects in various grains is known.

The extent of influence of a GB on the photovoltaic properties of the grains constituting the GB depends on several parameters of the grains themselves. These parameters include density of defects, barrier height, and the carrier density of the grains. In a small-grain material, the grain size can be of the same order as the size of "influence" of a GB. Thus, grains and GBs are modeled as regions with different properties. It is important to note that each region (whether a grain or a GB) is characterized by defects. All grains and the boundaries between adjacent grains can be modeled using categorization developed by Chen [19]. This categorization of various grains (or regions) is based on the properties of defects, summarized below.

Type I: These regions have very low defect densities and may be considered as standard regions where the recombination of the majority carriers can be neglected, and the density of extra charges introduced by defect levels is negligibly small.

Type II: The recombination of majority carriers can be neglected, but the extra charges introduced by defect levels in these regions cannot be.

Type III: These are heavily defected, effectively "dead" regions in which almost all the carriers (both majority and minority carriers) will recombine. In the modeling, the details of carrier distribution inside this type of region are ignored because these regions do not contribute any free carriers to the system. This type of region can include GBs or other defect-rich regions such as heavily diffused emitters.

Type IV: A highly defected region in which a significant fraction of the majority carriers recombine. As a result, the Fermi levels in this region will be different from the Type I regions with the same doping concentrations. Because of the high density of defect levels, it is likely that these regions also have extra charges.

In Type I regions, the electric field $E(x, y)$ is 0. But in the regions of Type II or Type III, which have extra charges, these charges will induce internal electric fields; hence, $E(x, y)$ will not be 0.

An important feature of the characterization of regions into four types is that it includes defect-free regions, defected regions, as well as GBs. In particular, one can appropriately define GB in terms of the properties of adjacent grains (see a later part of this Section 8.3.3.1).

Here, we will present some preliminary results of this model to illustrate the influence of material parameters, such as grain-size and grain-boundary recombination, on cell performance. This model can also be used to study effects of material parameters on the minority-carrier lifetime and carrier transport. We consider a sample with a columnar (two-dimensional) grain structure, which may have many regions of different lifetimes due to different defect distributions, separated by GBs. The sample is illuminated with light to generate photocarriers. The procedure for solving the 2-D continuity equation, subjected to appropriate boundary conditions, is discussed in References [19, 70, 71]. However, some physical insight can be gained by addressing the boundary conditions involving different region types.

8.3.3.1 Boundary/interface conditions

Because we are dealing with multiregion samples, there are two different boundaries: the surfaces of the entire sample and the boundaries between adjacent regions (grains) in the sample. These will be referred to as *boundary condition* and *interface condition*, respectively.

At the surface of the sample, the boundary condition is

$$D\frac{\partial n}{\partial \vec{n}} = Sn, \tag{8.4}$$

where S is the surface-recombination velocity, $\vec{n}$ is a unit vector, n is the concentration of electrons, and D is the diffusion coefficient.

At the interfaces between different regions, the boundary conditions depend on the types of the regions. The GBs between Type I or II regions can be treated as a surface with specific recombination velocities. At the interfaces, the following interface condition applies

$$n_1 = n_2 \tag{8.5}$$

$$D_1\frac{\partial n_1}{\partial \vec{n}} - D_2\frac{\partial n_2}{\partial \vec{n}} = Sn_{1or2} \tag{8.6}$$

Here, S is the "effective" surface-recombination velocity. However, if one of the grains is heavily defected, Type III, its boundary will have a finite width due to the field extending into the adjacent grain. This condition is illustrated in Figure 8.22. If the lifetimes of electrons and holes are τ_e and τ_h, respectively, in the Type III region, we can extend the algorithm of Fossum and Lindholm to the bulk region to express the electron current (in p-type samples) at the edge of the interface space-charge region [72].

The interface between a Type IV and a Type I (or Type II) region can be treated as a high–low junction because of their Fermi levels.

Because a solar cell involves an n/p junction for carrier collection, we must also consider how the junction is influenced in different region types. The fabrication of such a junction will influence the nature of the depletion regions, but all the equations developed earlier, including boundary conditions, still apply in the quasi-neutral region (QNR) of

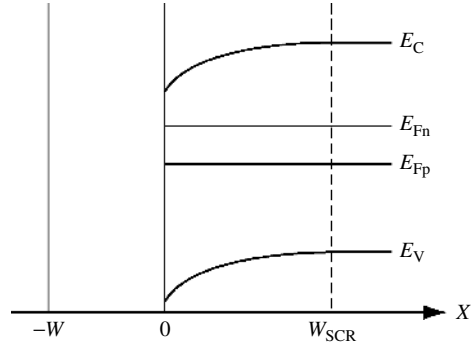


Figure 8.22 The energy band model used for boundary-condition analysis around a Type III region

the n/p junction. However, the depletion space charge region (SCR) region in different types of material need to be treated differently: SCR inside Type I regions should have the same behavior as the SCR in a normal n-p junction. In Type II or Type III regions, because there are extra charges (other than the dopant ions) and they are opposite to the charges of dopant ions, the net total charge should be less than that in the region without extra charges. The most apparent effect of the charges trapped in the p-n junctions may be the change of the width of the depletion region. This change can be easily determined by the Shockley model

$$W_{SCR} = \sqrt{\frac{2\varepsilon_{si}(N_A + N_D - 2N_x)(V_{bi} - V)}{e(N_A - N_x)(N_D - N_x)}} \tag{8.7}$$

where N_x is the extra charge density trapped in the Si. This value is the same for n-type and p-type regions, because we assume that the density of defect-related energy levels is the same in these two regions.

The calculation of the recombination current inside the space-charge region due to the Type IV can also be done following the Fossum and Lindholm algorithm.

The resultant band configurations used for device analysis are illustrated in Figure 8.23. The finite element method is used in this model. To limit the number of variables in this calculation, we assume that all the grains are similar. This assumption also brings other benefits to the calculation – since all the grains are similar, no net carrier flow will exist between grains at steady state. Therefore, the current collected by the device is just the summation of the current collected by each grain in the sample.

First, we will examine dependence of cell parameters, V_{OC} and J_{SC}, on the grain size of μc-Si thin-film solar cells. Figures 8.24(a) and 8.24(b), show the calculated values of J_{SC} and V_{OC} for two values of the GB interface recombination velocity, 100 cm/s and 1000 cm/s. The S-value of 100 cm/s corresponds to "clean" GBs. In practice, such a low value of S is hard to achieve. The μc-Si for PV applications is likely to contain impurities, which segregate at the GBs resulting in higher S-values. Thus, $S = 1000$ cm/s represents a more realistic μc-Si. The other parameters used in these calculations are given in Table 8.4. Here, G is the generation rate due to incident light and α is the

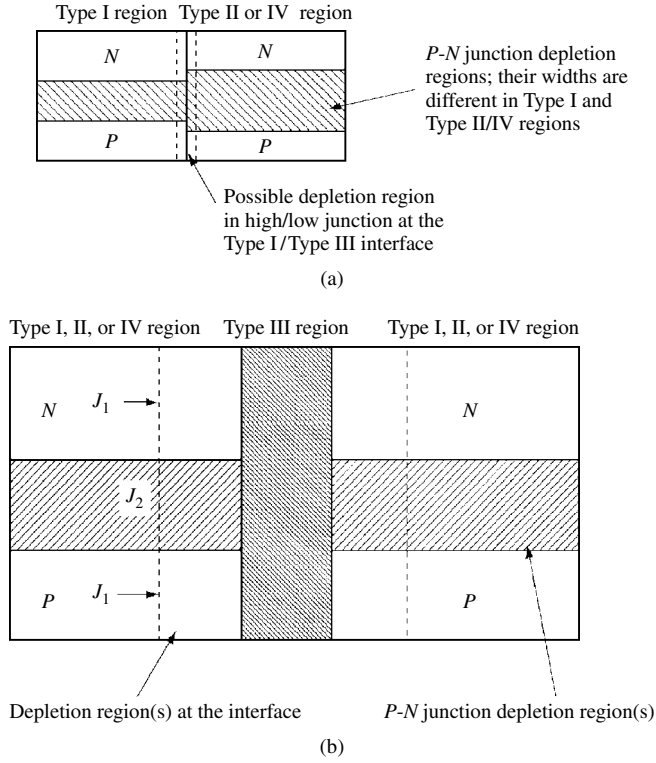


Figure 8.23 The proposed model of different regions in an n-p junction built on imperfect material. (a) The model of Type I, II, and IV regions, and the relationship among them inside a device. (b) The junction at the interface of Type I, II, IV region, and Type III region. J_1 and J_2 are current flows discussed in Reference [19]. The distribution of carriers inside the Type III region is not considered

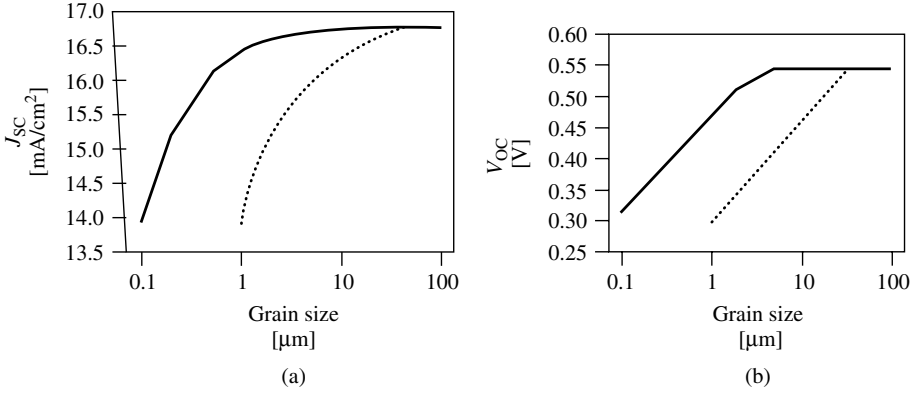


Figure 8.24 Calculated dependence of (a) J_{SC}; and (b)V_{OC} on the grain size of the 10-μm-thick cell for two values of interface recombination velocity, 100 cm/s (solid lines) and 1000 cm/s (dotted lines)

Table 8.4 The parameters used in calculating the solar cell characteristics

G [s^{-1}]	α [cm^{-1}]	D [cm·s]	Junction depth	n-doping	p-doping
10^{18}	100	50	0.5 μm	10^{18}	10^{17}

absorption coefficient. $G = \alpha \times$ number of photons incident at the surface (photons/unit area-second).

Calculated J–V curves, depicting the influence of grain-boundary recombination, are shown in Figure 8.25. Figure 8.25(a) is for a 5-μm-grain-size sample, and Figure 8.25(b) is for a 0.5-μm-grain-size sample. It can be seen that, for larger grain size, the recombination at the GBs will mainly degrade V_{OC}, and not J_{SC}. From Figures 8.24 and 8.25, it can be seen that the larger the grain size, the better the performance of the device. However, the interface recombination has a strong influence on each parameter. For low interface recombination velocity, when grain size is large (~1 μm), a decrease in the grain size will primarily degrade V_{OC} and not J_{SC}. However, for small grain size (<0.5 μm), J_{SC} will also decrease rapidly with a decrease in grain size. Because interface recombination has a very strong influence on the device performance, passivation of the GBs is very important for μc-Si thin-film solar cells. Furthermore, it can also be concluded that, to get a device with satisfactory J_{SC} and V_{OC}, the grain size of a μc-Si thin solar cell should be several microns.

8.3.4 Methods of Making Thin-Si Films for Solar Cells

The deposition techniques for Si films run the gamut from single-crystal deposition using crystalline substrates to microcrystalline Si thin films on glass or steel foil. A variety of techniques are now used for the deposition of thin films for solar cells [73, 74]. These include RF and DC glow-discharge techniques such as plasma-enhanced CVD (PECVD), hot-wire CVD (HWCVD), the electron cyclotron resonance CVD (ECRCVD), and other microwave- and plasma-beam deposition methods. Of these, the PECVD system is well suited to large-area depositions. Some of the newer techniques, such as ECRCVD, remote plasma-assisted CVD, and HWCVD have produced materials with interesting properties such as lower defect density, greater minority-carrier diffusion length, and lower hydrogen concentration. Some of these techniques may hold promise for the future.

Today, commercial a-Si:H solar cells are mostly deposited in multichamber reactors. Hydrogen incorporation is an important issue in the deposition of a-Si:H cells. A Si-bearing gas, typically silane, is used as the process gas in a DC or an RF (13.56–200 MHz) plasma in a pressure range of 0.1 to 1 torr. Typically, the deposition rates are 1–5 Å/s. A material with good electronic quality requires a dense and a homogeneous network of amorphous Si with minimum void density. These conditions dictate low deposition rates. Hydrogen dilution appears to have a strong influence on the properties of a-Si. However, a high hydrogen dilution rate is accompanied by a reduction in the deposition rate. Typically, VHF plasma excitation involves a source in the vicinity of 50 MHz. Operation

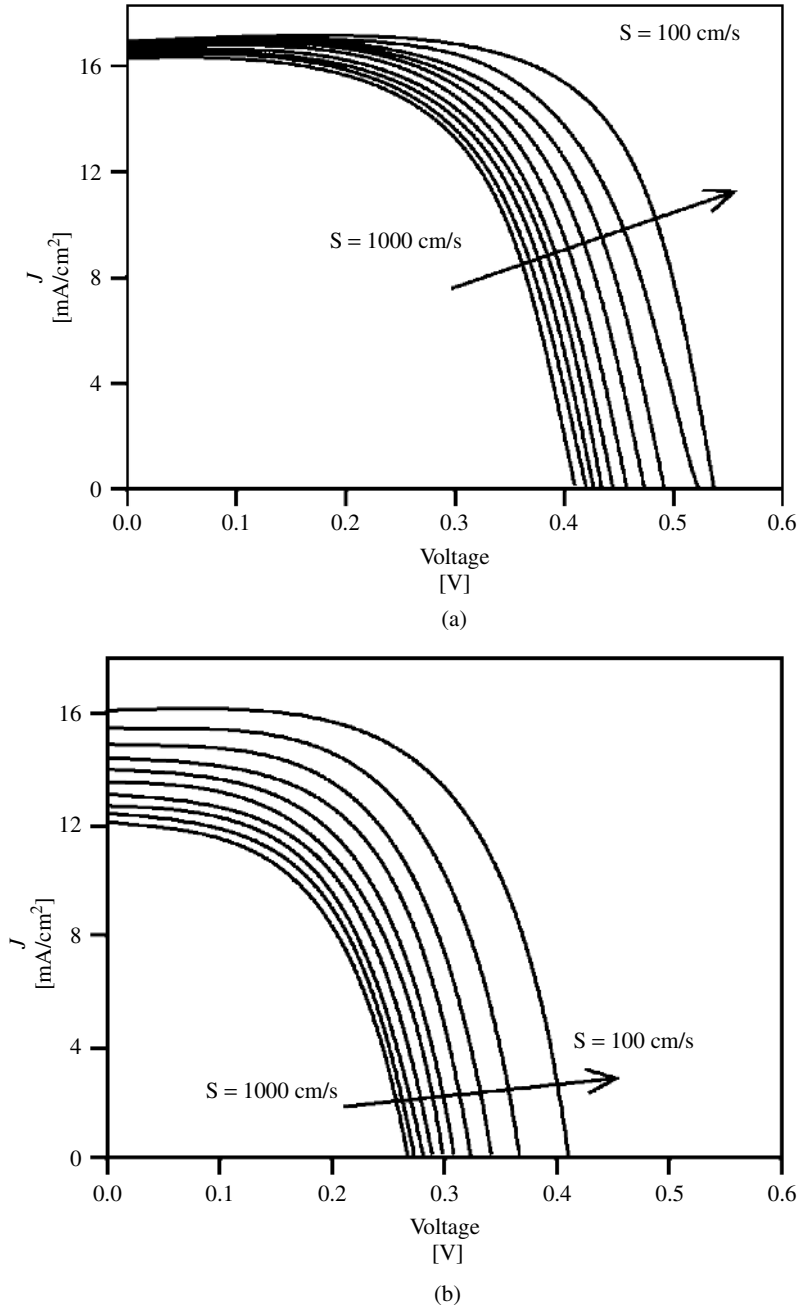


Figure 8.25 The calculated $J-V$ curves for different grain boundary interface recombination velocities (S). In the figures, S changes from 1000 cm/s to 100 cm/s in steps of 100 cm/s. Other parameters are given in Table 8.4. The grain sizes used in the calculations are: (a) 5 μm; (b) 0.5 μm [19]

Table 8.5 Grain-enhancement methods for already-deposited amorphous or fine-grain Si films. Temperature >600°C cannot be applied to low-cost glass substrates

Method	Processing temp. [°C]	Processing time	Metal contamination
CVD growth	1000	>10 h	No
Annealing	500	20–40 h	No
ZMR	1200	Quick	No
MIC	<500	Quick	Severe
LIC	>1000	Quick	No

LIC – laser induced crystallization; MIC – metal induced crystallization

in such a frequency range leads to higher deposition rates. See Chapter 12 for a more complete discussion of a-Si materials and deposition techniques.

It is known that typical, low-temperature (<400°C) CVD methods generally yield fine-grain (<0.1 μm) Si films. The solar cells fabricated on such films exhibit shunting, low V_{OC}, and poor carrier collection. Thus, it is imperative that a fine-grain (or amorphous) Si film on a glass or some other low-cost substrate be grain-enhanced by a low-temperature process. Table 8.5 gives a summary of the grain-enhancement techniques currently used in thin-film μc-Si formation. The grain enhancement involves the movement of GBs in an attempt to minimize the overall energy. A simple approach for accomplishing this is to perform a high-temperature anneal. However, high temperature (>600°C) processing is not compatible with low cost substrates like glass. The processing temperature can, however, be significantly lowered by a suitable choice of film properties and processing conditions.

8.3.5 Methods of Grain Enhancement of a-Si/μc-Si Thin Films

The grain-growth phenomenon in a crystal is caused by the material's effort to minimize its excess Gibbs free energy from the presence of GBs by minimizing the total grain-boundary area. GBs are a higher energy, nonequilibrium condition compared to a single-crystal structure. Thus, any technique that applies sufficient energy to mobilize GBs will cause grain enhancement.

(a) Annealing

When an a-Si film deposited on glass substrate is subjected to a thermal anneal for an extended period of time, crystallization of the film occurs leading to an increase in the grain size. The thin film remains in the solid phase during the whole process, which is why this kind of process is also called *solid-phase crystallization*. The grain enhancement in this process results from a movement of GBs activated by the heating. An increase in the time or temperature, or both, can further promote the grain growth. The major drawback of the thermal annealing process is that it requires a long time. A typical annealing process will take 20 to 40 h [75]. The annealing time can be reduced somewhat if a surface-textured substrate or doped a-Si layers are used. These methods accelerate the

velocity of grain enhancement, either by introducing some kind of seeds or by activating the grain-boundary movement.

(b) Metal-induced crystallization (MIC)

MIC of a-Si can be used to produce μc-Si with grains larger than those achievable either by thermal annealing of a-Si or by direct deposition of μc-Si by plasma or HW processes. If a-Si is deposited at low temperatures on substrates coated with certain metals, and then heated to a temperature >300°C, the a-Si film can be converted to μc-Si. Alternatively, if the deposition of a-Si can be carried out at such higher temperatures on these metals, one can obtain large-grain μc-Si films directly. Here the metal acts as a catalyst to induce crystallization. The effects of several kinds of metals, such as Sb, Au, Al, and In (which form eutectics with Si), and those of Pd, Ti, and Ni (which form silicides with Si), have been studied. Al is a particularly interesting metal for solar cell because it can offer other advantages, as described in this chapter. Earlier studies on very thin (<1 μm) a-Si films found that Al-induced crystallization of a-Si could occur as low as 167°C [76]. However, the grain size of the crystallized films was very small and the annealing time required was between 10 and 60 min. This led to a conclusion that MIC involves intermixing of metal with Si and the formation of a high concentration of metal alloy in the amorphous/crystalline interface. Furthermore, it was found that the growth of the crystalline phase would stop when no more metal is available.

Although the mechanism(s) involved in MIC are not well understood, it is generally believed that nucleation requires a strong interaction between metal and Si [77–79]. These interactions may involve a solid-phase diffusion or formation of an alloy or eutectic. For solar cell applications, each of these mechanisms must be highly controlled. Incorporation of high metal concentrations into the crystallized Si film poses a major limitation on MIC technique. Typically, MIC-formed Si films have very low minority-carrier lifetime. Solar cells fabricated on them can have severe shunting effects because some of the metal segregates at the GBs. Two approaches have been attempted to overcome these drawbacks in MIC films. One, use of metal-induced lateral crystallization (MILC), in which crystallization is started from a metallized region and then extended laterally into a metal-free area. Typically, Pd and Ni, have been used for MILC which yielded films with a grain size up to several microns [80]. However, it is found that crystallized regions away from the initial metal also have large concentration of metal.

The second approach is to use optical excitation instead of furnace annealing to crystallize an a-Si film deposited on a metallic layer. Because the absorption of optical energy within a Si film is not uniform, optical excitation can be tailored to produce an absorption profile favorable for MIC. In particular, infrared excitation of an a-Si film, deposited on an Al layer, will result in a peak in the energy dissipation near the a-Si-metal interface. Thus, optical processing can initiate nucleation at the interface followed by a grain-enhancement process. Initial work comparing thermal processing and optical processing to achieve MIC of a thin layer of a-Si [81] showed that crystallization by optical excitation occurs very rapidly and at temperatures as low as 200°C – features important for TF-Si solar cell fabrication. Optical excitation can initiate nucleation at the interface and the crystallization propagates into the a-Si film. This process is also accompanied by injection of point defects that promotes grain enhancement. Thus, optical processing is a two-step process – a higher-temperature alloying to produce nucleation,

followed by a lower-temperature vacancy injection to enhance the grain size and continue conversion of amorphous to crystalline phase. Optical processing of the TF-Si samples is done in a quartz furnace, with tungsten-halogen lamps fitted on one side. The sample is illuminated from the a-Si side. The intensity of the light is controlled to provide a predetermined intensity versus time profile including a slow ramp-up and ramp-down of temperature.

Figure 8.26(a) is an XRD (x-ray diffraction) spectrum of a 3-μm film, deposited by HWCVD at $<100^{\circ}$C on a Al/Cr-coated 7059 glass substrate, showing absence of crystalline structure in the Si film. Only Al peaks are seen in the spectrum [82]. It may be pointed out that it is necessary to deposit a thin layer of Cr on glass prior to deposition of Al to improve the adhesion of Al. Figure 8.26(b) is the XRD spectrum of this sample after optical processing at $\sim 480^{\circ}$C for 3 min. An important feature of Figure 8.26(b) is the presence of two preferred orientations – (220) and (111). One can also notice the existence of a large Al peak due to unused Al. The initial Al thickness was 2 μm. Longer times can also help increase grain size, however, because optical processing is a transient process, its advantages diminish (approaching a thermal process), if the process times are too long. This indicates that the crystallization of a-Si can happen very rapidly with optical excitation processing technique.

If the deposition of a-Si on Al/Cr-coated substrates is carried out at temperatures in excess of 300°C, some crystallization and some (or total) consumption of Al can occur during the deposition itself. Figure 8.27(a) is an XRD spectrum of a 2-μm, Si film deposited by HWCVD at 500°C showing the crystallization was strongly textured in (220) direction. However, optical processing can further enhance crystallization. Figure 8.27(b) shows an XRD spectrum of the same sample after optical processing at 480°C for 3 min. The intensity of the (111) peak becomes much stronger, and the intensity of (220) peak increases more than 200%. The increase in (111) and (220) peaks could result from formation of new grains of the preferred orientations, and/or (more likely) by enlargement of the original grains during processing.

Additional results show that an increase in process time and/or temperature leads to enhancement of grain size, while crystallization spreads over the entire thickness of the a-Si film with two preferred orientations. However, there appears to be an "incubation temperature" at which the grain enhancement begins. We have carried out studies to investigate crystallization at different temperatures. The samples were optically processed to change the maximum light intensity while keeping the process time constant. Figures 8.28(a) and 8.28(b) show the intensity of XRD peaks for (111) and (220) orientations as a function of process temperature. These results are shown for three (3 μm, 6 μm, and 10 μm) thicknesses of a-Si films deposited by HWCVD. The deposition temperatures for these films are as follows: 3 μm at $<100^{\circ}$C, 6 μm at $<250^{\circ}$C, and 10 μm at $\sim 500^{\circ}$C. Each of the XRD measurements was made after calibrating the system with standard reference samples. Hence, the intensities of the XRD peaks are representative of the extent of crystallization in those specific orientations. From these plots, one may also infer that thinner films can be crystallized more readily than thicker ones. Despite the fact that the 6 and 10 μm films had some crystallization occuring during the deposition itself, the incubation temperature is lower for thinner films. This conclusion is also supported by TEM (transmission electron microscope) results, which show that the initial part of the optical process leads to a nucleation occurring over the entire interface. Then a

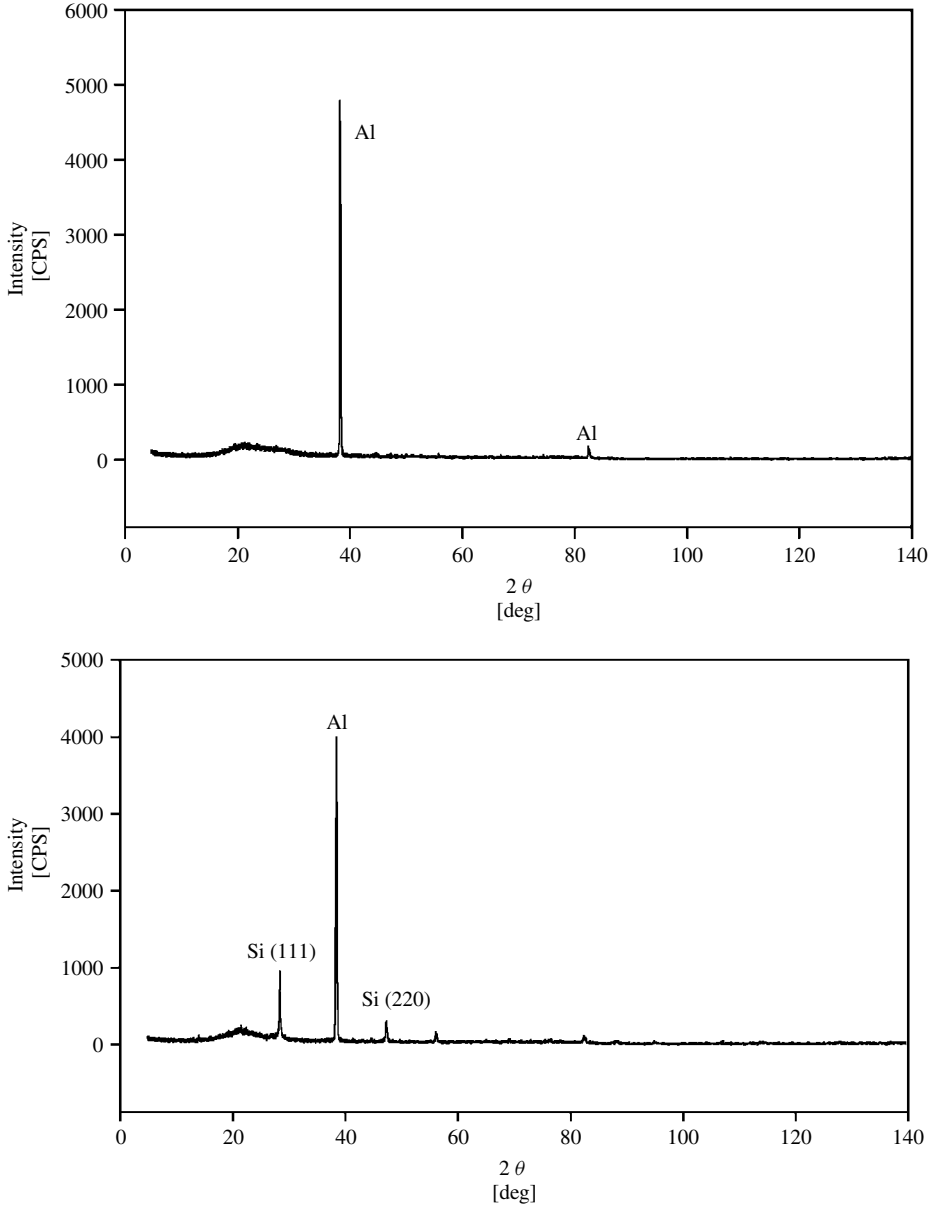


Figure 8.26 XRD spectrum of a 3-μm-thick HWCVD a-Si film, deposited on Al/Cr/glass at about 100°C (a) before optical processing; and (b) after optical processing at ~480°C for 3 min

crystallization front propagates away from the interface converting a-Si into crystalline Si. These features can be seen in Figure 8.29(a), which is a TEM cross-section of a partially crystallized Si film on a glass substrate. The film, 6 μm thick, was deposited at 250°C and processed for 3 min at 460°C. The various regions of the structure are identified in the figure. The largest grain size near the Al interface is about 0.1 μm and decreases

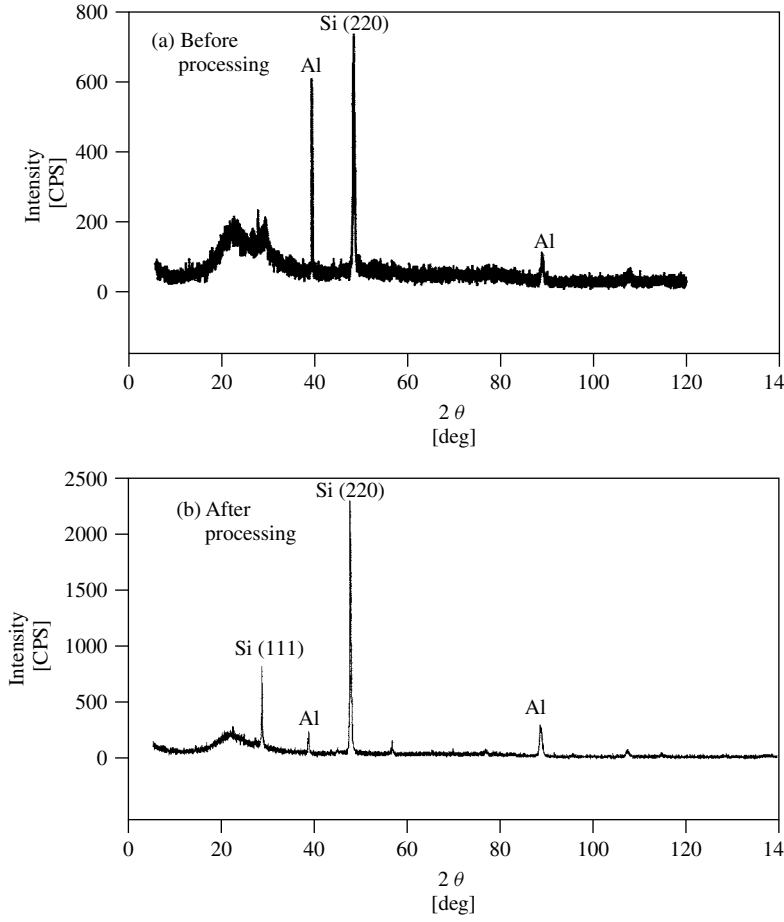


Figure 8.27 XRD spectrum of a 2-μm-thick HWCVD Si film, deposited on Al/Cr/glass at about 500°C (a) before optical processing; and (b) after optical processing at ~480°C for 3 min. A significant increase in Si (220) compared to Si (111) orientation can be seen in (b)

toward a-Si. From this figure, it is clear that 3 min of optical processing time was not sufficient to crystallize the entire film at 460°C. Figure 8.29(b) is a TEM plan view of the film showing distribution of grain sizes near the Si–Al interface.

Detailed profiling of Al across the crystallized films, done by SIMS (secondary ion mass spectroscopy) and micro-X-ray, showed that in optically crystallized films the Al concentration dropped by several orders of magnitude within about 1 μm from the Al-Si interface [81, 83]. These results indicate that Al is required only for the initiation of crystallization. After the nucleation, the crystallization front propagates into a-Si while grain enhancement occurs in the crystallized film. It is believed that vacancy injection from Al-Si interface is responsible for grain enhancement.

Investigation of the possibility of applying optically assisted MIC showed that crystallization of a-Si can start at about 200°C in less than 3 min. This crystallization

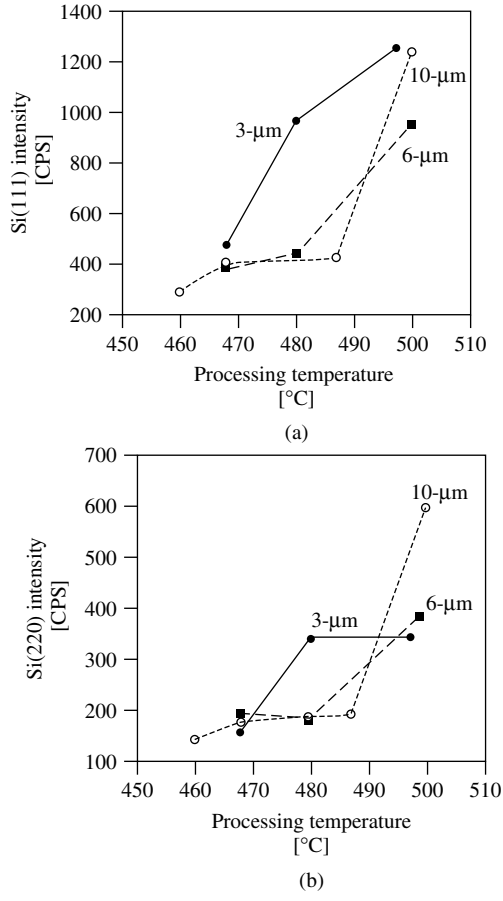
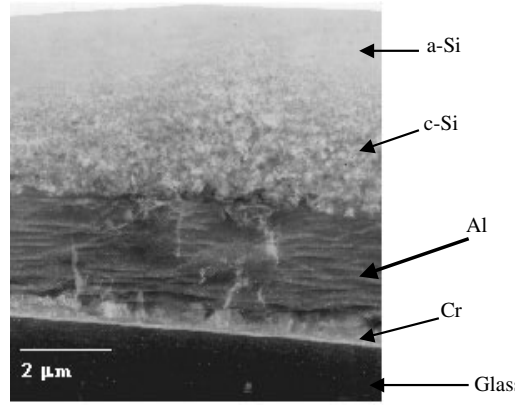


Figure 8.28 Intensity of (a) Si (111) and (b) Si (220) peaks in the XRD spectra of processed samples as functions of processing temperature. A "jump" of peak intensity around 490°C can be observed for the 10-μm-thick sample

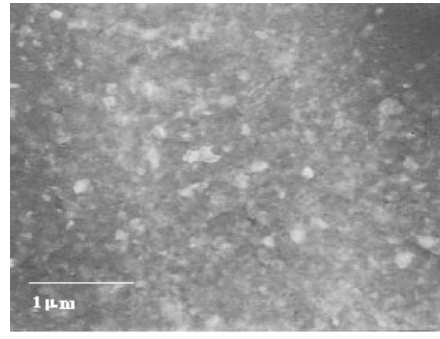
becomes much stronger at temperatures close to 450°C. By controlling the process conditions, it is possible to confine Al to the vicinity of the Si–Al interface, leaving the crystallized film (away from the interface) with a low Al concentration. In contrast, thermally crystallized films have nearly uniform and high concentration of Al. Some films, thermally processed at higher temperatures, may exhibit lateral nonuniformities because of segregation into Si-rich and Al-rich phases.

The proposed explanation of the optically assisted, Al-induced crystallization and grain enhancement of thick samples is as follows:

- Optical processing generates a nonuniform temperature distribution within the film structure, especially at the Al-Si interface where energy can be locally absorbed, producing a higher temperature spike.
- In high-temperature (>450°C) optical processing, although the monitored film surface temperature is lower than the eutectic point of an Al-Si system, melting in the local



(a)



(b)

Figure 8.29 TEM photos of a partially crystallized Si film showing (a) start of nucleation and grain growth from the Al interface in cross-section; and (b) grain size distribution near the Si–Al interface in plan view

regions around the Al/Si interface may still occur. This local melting will induce crystallization at the interface area, and this crystallization can be much stronger than the crystallization caused by Al-Si intermixing at a solid phase.

- For thick samples, once the initial crystallization has occurred, it is possible to continue crystallization and grain enhancement via injection of defects. It is believed that in this process vacancies are injected into Si, especially when temperature is below 450°C, which can promote grain growth. This could suggest that following a high-temperature dwell, the optical power could be reduced to stimulate grain enhancement.

One may think that a preferred approach for crystallization would be to deposit the a-Si film at a higher temperature and then use optical processing. However, results to date seem to indicate that the effect of optical processing is somewhat diminished, if the film is deposited at higher temperatures. Thus, contrary to intuition, low-temperature deposition appears to favor crystallization during optical processing. One may explain this behavior by assuming that the formation of thick Al-rich alloyed layer retards vacancy injection. More research needs to be done to understand behavior of point-defect injection.

(c) Zone-melting recrystallization (ZMR)

In zone-melting recrystallization, a narrow zone on the surface of the sample is melted with heating. The film is recrystallized by moving this melted zone around the surface. A range of energy sources, including strip heaters, electron beams, and radio-frequency (RF) heaters, have been used. Because the thin film is heated to the temperature around the melting point of silicon ($\sim$1200°C), this method is not suitable for the crystallization of an a-Si film on a normal glass substrate. For the other kinds of low-cost substrate (such as metallurgical Si and carbon), preventing the impurity diffusion from the substrate to the film is also a major issue. Ishihara *et al*. reported impressive results for solar cells fabricated on poly-Si thin films obtained by ZMR technology [84].

(d) Laser-induced recrystallization

XeCl excimer laser recrystallization (ELR) and annealing (ELA) of a-Si has been studied extensively in recent years. Although most works are concentrated on the use of this method for thin-film transistor (TFT), it is also used for solar cells. The focused short-pulsed laser beam is scanned over the a-Si or μc-Si thin film to heat the sample. In laser recrystallization, depending on the power of the incident light, the part of the thin film under illumination can be either in liquid phase (melted totally) or in liquid + solid phase (partly melted), which will result in different grain sizes. It is interesting that the grain size does not increase even though the temperature in the thin film is around the melting point of Si. Because short-pulse laser is used, the temperature of the substrate can be much lower than that of the film; this is a major difference between ZMR and ELR. By placing a thin oxide and/or nitride layer between the substrate and a-Si, both heat transfer from the thin film to the substrate and impurity diffusion from the substrate to the thin film can be dramatically reduced. Other alternatives such as using prepatterned a-Si and multiple-step laser processing can improve the quality of the film. TFTs fabricated on ELR films have yielded excellent overall performance [85]. At present, solar cells fabricated on laser-crystallized Si have achieved conversion efficiencies close to 9%.

Solid-phase crystallization processing using ELA combined with RTP is also reported [86]. The ELA treatment can be at a temperature of 550°C. Poly-Si thin films with a grain size as large as several microns have been obtained.

8.3.6 Processing Considerations for TF-Si Solar Cell Fabrication

The performance of crystalline Si solar cells is strongly controlled by impurities and defects in the material [87]. Although the quality of the starting material used for wafer-based commercial Si solar cells is quite poor, the PV industry has developed solar cell fabrication methods that improve the material quality during the cell fabrication. As explained in the previous sections, one of the advantages of the TF-Si solar cell is its partial immunity to the quality of the material. However, high-efficiency device fabrication does require material quality and processing procedures that may not be compatible with low cell costs unless careful consideration is given to minimizing impurities and defects. It is prudent to include a brief discussion of the processing approaches used to ameliorate deleterious effects of impurities and defects in the design and processing of TF-Si cells.

Thus, it may be important to include impurity gettering and hydrogen passivation in TF-Si solar cell fabrication [88–92].

The impurities of most interest in PV-Si are the transition metals (TM), particularly Fe, Cr, and Ni. They are typically present in concentrations as high as $10^{14}/\text{cm}^3$ in the as-grown substrates. In the dissolved state, these impurities are highly mobile with diffusivities close to 10^{-6} cm^2/s at typical process temperatures [93]. They produce deep level electronic states within the bandgap which act as efficient recombination sites. For example, at room temperature, the interstitial iron (Fe_i) introduces a donor level at $E_\text{T} \approx E_\text{V} + (0.375 \pm 0.015)$ eV. The hole capture cross section of interstitial iron can be written as (in cm^{-2})

$$\sigma_p(\text{Fe}_\text{i}) = (3.9 \pm 0.5) \times 10^{-16} \times \exp\left(-\frac{0.045 \pm 0.005 \text{ eV}}{k_\text{B}T}\right), \tag{8.8}$$

where k_B stands for the Boltzman constant and T is the temperature. The electron-capture cross-section of Fe at room temperature was measured as $\sigma_n = 4 \times 10^{-14}/\text{ cm}^2$. Because of near-mid gap energy and a large-capture cross-section, it is expected that Fe will produce high-recombination or low minority-carrier lifetime.

TMs in Si also have the ability to form complexes with each other. For example, B can form Fe–B and B–O pairs. B–Fe forms a donor level at $E_\text{v} + 0.1$ eV ($\sigma_n = 4 \times 10^{-13}/\text{cm}^2$ at the room temperature) and an acceptor level at $E_\text{c} - 0.29$ eV. At low injection levels, the recombination rate caused by the Fe–B pair is lower than that of interstitial Fe. Recent studies have also shown that B–O pair formation occurs in some solar cells. This effect is manifested as a decrease in the minority-carrier diffusion length (MCDL) of the cell under sunlight. This mechanism has a pronounced effect of reducing the efficiency of a Si solar cell.

Impurity gettering is used in microelectronic device fabrication to trap impurities away from the active region of the device by oxygen precipitates. This leaves a very clean, denuded surface region, while the impurities are driven into the bulk. For this reason, it is often referred to as *internal gettering*. Because microelectronic devices use only the near-surface region of the wafer, internal gettering works well for them. Solar cells, being minority-carrier devices, use nearly the entire thickness for the device. Hence, it is necessary to apply external gettering techniques to clean up the bulk of the material. In external gettering, a surface region serves as a sink for impurities. Fortunately, phosphorous diffusion and Al alloying are some of the processes that have worked well for efficient gettering in solar cells. Because these processes are extensively used in solar cell fabrication for junction and contact formation, all Si solar cells experience a certain degree of gettering. In a typical junction formation or Al alloying process, the Fe concentration can be reduced by two orders of magnitude. Theoretical and experimental details of P and Al gettering are reviewed in several papers [94, 95]. For a typical multicrystalline Si wafer, P diffusion for formation of an n^+p solar cell can lead to an improvement in the average MCDL from a value of about 50 μm to 75 μm. This increase in the MCDL is caused by removal of fast-diffusing transitional metal impurities from the bulk of the substrate into the P diffused region. Similar results are obtained with the Al-alloying used for formation of the backside p^+ region and back metallization.

Impurity gettering can also play an important role in fabrication of high-efficiency TF-Si solar cells. The Si as deposited for TF-Si cells also contains high concentrations of impurities. Although it is possible to deposit high-purity a-Si or poly-Si for laboratory purposes, it is difficult to maintain "cleanliness" in a high-throughput deposition system. In addition, low-cost substrates such as glass or ceramics will release impurities through desorption or diffusion, which can contaminate the deposition system and the Si film. Because of the small thickness of the Si film, gettering times can be short and/or process temperatures can be low. A unique way to provide for impurity gettering in a TF-Si solar cell is to include a layer of Al in the device structure (see Figure 8.12). Another approach for low-temperature gettering may be to inject vacancies. Because the impurities that kill minority-carrier lifetime are typically interstitial transition metals, a region of vacancy injection can be a "sink" for the impurities. Sources of interstitial sinks can also be interfaces (such as heterointerfaces), GBs, and other crystal defects. However, it has been observed that such sites can lead to precipitation of metallic impurities. Because it is very difficult to getter precipitated impurities, it is desirable to maintain impurity concentrations below the saturation levels. Precipitated impurities form local shunts which can severely degrade V_{OC} and FF of the device.

Similar to impurities, defects are sites for high-carrier recombination, causing degradation in solar cell performance. In a polycrystalline TF-Si solar cell, the dominant defects are GBs and intragrain dislocations. In both mc-Si and poly-Si, one often finds that intragrain defects segregate in certain preferred grains. Most solar cell processing does not change the nature or density of crystal defects because these defects are generally tangled, which prevents them from gliding. Like impurities, defects introduce energy levels in the band gap. The nature of the levels in a real material is quite complex, because the defects represent a host of defect configurations. Crystal defects always appear to have detrimental effects on material quality.

Typical solar-cell processes do not fully remove impurities from Si. Even the impurities that are readily gettered remain in the solar cell in significant levels and produce strong harmful effects on solar cell performance. In addition to residual impurities, many crystallographic defects are stable at the processing temperatures used. It is often observed that defect concentrations remain essentially unaltered by solar cell processing. Therefore, it is important to identify methods of dealing with the residual impurities and defects. Fortunately, hydrogen passivation has proven to be a very valuable process to deal with residual impurities and defects.

H is known to be electronically very active in Si, and it interacts with nearly all impurities and defects. H saturates dangling bonds at interfaces, and at point and extended defects, thereby reducing the carrier recombination and improving device characteristics. H can also interact with impurities in Si. The nature of such interactions depends on the type of impurities. For example, it can deactivate shallow dopants, both acceptor and donor types, leading to changes in the resistivity of the wafer. Although this effect is an undesirable feature for most cases, it can be used to reversibly alter dopant activity and to form erasable p/n junctions in some future applications. Atomic H can interact with metallic impurities such as Fe, Cr, Ni, Cu, and Au to reduce their effectiveness for carrier recombination in Si. H interactions with O exhibit a very interesting behavior – it appears that H diffusivity is lowered by the O, whereas the diffusivity of oxygen donors is greatly enhanced.

Introduction of H after impurity gettering can help improve solar cell efficiency by as much as 3 to 4 absolute points. Generally, such a passivation results in a significant decrease in the dark current and an improvement in the illuminated cell parameters. However, the degree of improvement can vary significantly over the wafer in a manner very similar to impurity gettering [96–98]. It has been determined that better-performing regions improve more than the poorer regions. This behavior can be explained by the dependence of H diffusion on the structure of defects, such as defect clusters and impurity precipitation. The defects and impurities act as trapping centers for atomic H, reducing its effective diffusivity [99–102].

Several methods have been used for incorporating H in solar cells. These include ion implantation, plasma processing, and, more recently, a process in which hydrogenation is combined with deposition of a Si_3N_4 layer by a PECVD process. The nitride layer is used as an AR coating. Another advantage of the nitride coating is that the front metal can be fired through the nitride using an RTP-like process, typically 800 to 850°C for about 10 s.

In a wafer-based cell, passivation of impurities and defects requires a deep diffusion of H into the bulk of the solar cell. In addition, it is important that H interacts with only those impurities that degrade device performance. For example, H should not deactivate dopants because that would lead to a change in the resistivity of the device. These considerations dictate a careful design of a hydrogenation process. A deep diffusion of H may appear to be quite trivial because a high value of diffusivity of H in Si is often assumed. However, the effective diffusion of H in Si is primarily controlled by its defects and impurities. H can associate with impurities and defects to form complexes, leading to "trapping" of H during its diffusion into Si – causing a greatly reduced diffusivity of H at low temperatures (e.g. $<400^{\circ}C$ typically used for hydrogenation by plasma or ion implantation). To minimize the effects of trapping, it is necessary to use a high-temperature process step. At higher temperatures, the complexes begin to dissociate, causing the H to diffuse with intrinsic lattice diffusivity.

Trapping of H is also expected in poly TF-Si solar cells because of the abundance of GBs. However, by incorporating suitable process design, the trapped H can be released for impurity-defect passivation. This feature may be valuable for TF-Si solar cells because many a-Si or poly-Si deposition techniques result in copious amounts of H in the thin film.

8.4 CONCLUSION

The thin-film Si solar cell was envisaged during the infancy of solar-cell technology as a potential candidate to reduce the amount of Si needed for an efficient solar cell. Although it was recognized that the quality of the material needed for a TF-Si solar cell does not have to be very high, experimental work on cell fabrication had to await technologies in two different areas – a lift-off type of technology for making single-crystal cells, and low-temperature processing of large-grain polycrystalline deposition to make thin films on low-cost substrates. Clearly, this is just the beginning of thin-film Si solar-cell technology, but there has been astounding progress in a very short time frame. In addition to vigorous research, there is also interest in commercial production of such

devices. Like any other technology, many methods for TF-Si solar cell production will emerge. The lift-off approaches for potentially high-efficiency single-crystal cells are very attractive. However, there are questions about the reliability of a technique that involves mechanical transfer from one substrate to the other. Likewise, reuse of the single crystal substrate is another issue.

The use of μc-Si seems to have a large potential because of being a true thin-film technology that can use some established thin-film processes. Furthermore, it can also derive benefits from ongoing R&D within the a-Si community. Because μc-Si is now used in traditional a-Si cells for junction formation, there is considerable added interest in studying deposition kinetics, phase transformation, and electronic and optical properties of μc-Si. To date, the performance of μc-Si is clearly limited by the grain size (controlling V_{OC} and *FF*). The highest efficiencies are obtained by using nip structure, which offers the advantage in achieving high currents. Higher voltages have been obtained using a mixture of a-Si and μc-Si phases. Because of the similarities in a-Si cells and μc-Si TF cells, there may be common features in module technology, too.

TF-Si solar cell technology will eventually compete with other thin-film technologies based on polycrystalline thin films of CdTe or CIGS ($Cu(UnGa)Se_2$). It may be argued that Si is a simpler material system and that its processing can be low cost compared to compound semiconductors. On the flip side, it is believed that GBs in poly thin films are "benign," making these material systems easy to process. Clearly, there is much more work to be done before such arguments can be resolved.

The TF-Si solar cell is an excellent solution to reduction in the use of Si and achievement of high efficiency at low cost. Many problems need to be solved before this technology can compete with existing solar cells, but the future looks very bright for TF-Si solar cells.

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