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Crystalline Silicon Solar Cells and Modules

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7.1 INTRODUCTION

Crystalline silicon solar cells and modules have dominated photovoltaic (PV) technology from the beginning. They constitute more than 85% of the PV market today, and although their decline in favor of other technologies has been announced a number of times, they presumably will retain their leading role for a time, at least for the next decade.

One of the reasons for crystalline silicon to be dominant in photovoltaics is the fact that microelectronics has developed silicon technology greatly. On the one hand, not only has the PV community benefited from the accumulated knowledge but also silicon feedstock and second-hand equipment have been acquired at reasonable prices. On the other hand, Microelectronics has taken advantage of some innovations and developments proposed in Photovoltaics.

For several decades, the terrestrial PV market has been dominated by *p*-type Czochralski silicon substrates. Continuous improvements in performance, yields and reliability have allowed an important cost reduction and the subsequent expansion of the PV market. Because of the lower cost of mc-Si wafers, multicrystalline (MC) silicon cells emerged in the 1980s as an alternative to single-crystal ones. However, their lower quality precluded the achievement of similar efficiencies to those of Cz, so that the figure of merit \$ W^{-1} has been quite similar for both technologies over a long time (see Table 7.1).

Deeper understanding of the physics and optics of the mc-Si material led to improved device design, which allowed a wider spread of the technology. A combination

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Table 7.1 Breakdown of costs of fabrication of single-crystalline (SX) and multicrystalline (MC) solar cells (corresponding to year 1990) [1]

Item	SX	MC
Pure Si	38	38
Ingot formation	115	35
Sawing	77	77
Wafer cost	**230**	**150**
Cell fabrication	80	80
Total components	310	230
Yield	0.95	0.9
Cell cost	**326**	**256**
Module assembling	75	75
Lamination	75	75
Module cost (Euro m^{-2})	**476**	**406**
Efficiency	0.14	0.12
Module cost (Euro Wp^{-1})	**3.40**	**3.38**

Table 7.2 Market share of monocrystalline and multicrystalline solar cells [2]

Year	Cz-Si solar cells		MC-Si solar cells	
	Output [MW]	Market share [%]	Output [MW]	Market share [%]
1996	48.7	55	28.4	32
2000	92.0	32	146.7	51

of improved material quality and material processing has allowed higher efficiencies at a still lower cost, increasing the share of MC in the PV market, well ahead of monocrystalline. Recent evolution of the market can be seen in Table 7.2 [2].

This chapter offers an overview of silicon solar cell and module technology. First, Si properties justifying its use as photovoltaic material are presented. Then, design of Si solar cells is reviewed, highlighting the benefits and limits of different approaches. Manufacturing processes are described, paying special attention to technologies that are currently implemented at the industrial level, mostly based on screen-printing metallization technology. Considerations of ways of improving solar cell technology are also specified. Peculiarities of multicrystalline material are explained in Section 7.6, while other approaches that are already in industrial production are also described briefly. Next, crystalline Si modules are reviewed, pertaining to electrical performance, fabrication sequence and reliability concerns.

7.2 CRYSTALLINE SILICON AS A PHOTOVOLTAIC MATERIAL

7.2.1 Bulk Properties

Crystalline silicon has a fundamental indirect band gap $E_G = 1.17$ eV and a direct gap above 3 eV [3] at ambient temperature. These characteristics determine the variation of optical properties of Si with wavelength, including the low absorption coefficient for carrier generation for near band gap photons [4]. At short ultraviolet (UV) wavelengths in the solar spectrum, the generation of two electron–hole pairs by one photon seems possible, though quantitatively this is a small effect [5]; at the other extreme of the spectrum parasitic free-carrier absorption competes with band-to-band generation [6]. The intrinsic concentration is another important parameter related to the band structure; it links carrier disequilibrium with voltage [7].

At high carrier densities, doping- or excitation-induced, the band structure is altered leading to an increase in the effective intrinsic concentration: this is one of the so-called heavy doping effects that degrade the PV quality of highly doped regions [8].

Recombination in Si is usually dominated by recombination at defects, described with Shockley–Read–Hall (SRH) lifetimes. The associated lifetime τ (which can also be described in terms of diffusion length L) increases for good quality materials. Auger recombination, on the contrary, is a fundamental process that becomes important at high-carrier concentration [9]. The Auger coefficients are reported to be higher at moderate carrier densities due to excitonic effects [10]. Band-to-band direct recombination is also a fundamental process but quantitatively negligible (it is instructive, however, to notice that record-efficiency solar cells have such extraordinarily low SRH recombination levels that they perform as 1%-efficient light-emitting diodes, that is, radiative recombination is significant [11]).

At low and moderate doping, electrons present mobilities about three times higher than holes, both limited by phonon scattering. Impurity scattering dominates for higher doping densities [12, 13]. Carrier–carrier scattering affects transport properties in highly injected material [14].

7.2.2 Surfaces

7.2.2.1 Contacts

Contacts are structures built on a semiconductor surface that allow charge carriers to flow between the semiconductor and the external circuit. In solar cells, contacts are required to extract the photogenerated carriers from the absorbing semiconductor substrate. They should be selective, that is, should allow one type of carrier to flow from Si to metal without energy loss while blocking the transport of carriers of the opposite type.

Direct Si-metal contacts, in general, do not behave this way. As an exception, good hole contacts to highly doped p-Si substrates with aluminum are possible. But the

most used approach is to create heavily doped regions under the metal, *p*-type for hole extraction and *n*-type for electron extraction. Majority carriers in this region can flow through the contact with low voltage loss. The transport of minority carriers is described by a surface recombination velocity (SRV), *S*. Although the SRV is high, limited only by thermal diffusion so that $S \cong 10^6$ cm·s^{-1} [15], the concentration of minority carriers, for a given *pn* product, is suppressed by the high doping and the flow is reduced.

As will be seen later on, the contact for the minority carriers is usually placed at the front (illuminated) face of the substrate, and the corresponding heavily doped layer is usually called *emitter*. The doped region under the majority carrier contact at the back is called a *Back Surface Field* (BSF).

Recombination at these heavily doped regions is described by the saturation current density J_0 that includes volume and true contact recombination. Their thickness w should be much higher than the minority-carrier diffusion length L so that few excess carriers reach the contact, and the doping level must be very high to decrease contact resistance and the minority-carrier concentration, although heavy doping effects may limit the doping level advisable for such regions. The recombination activity of BSF layers is often described in terms of an effective SRV instead of the saturation current density.

Typical 10^{-13} to 10^{-12} A·cm^{-2} J_0 values are achieved [16, 17]. Diffused phosphorus is used for *n*-contacts. Aluminum alloying has the advantages over boron for *p*-contacts that very thick p^+ layers can be formed in a short time at moderate temperatures and that gettering action is achieved [18]. As a shortcoming, the p^+ layer is nonhomogeneous and can even be locally absent; the obtained J_0 is larger than expected for a uniform layer. In comparison to aluminum, boron offers higher doping levels because of a larger solubility [19] and transparency to light so that it can also be used at illuminated surfaces.

Other structures have been tested to obtain selective contacts: metal-insulator-semiconductor (MIS) contacts [20], polysilicon contacts [21] and heterojunction to a-Si or other wide band gap material [22].

7.2.2.2 Noncontacted surfaces

Because of the severe alteration of the bonding of Si atoms, a large number of band gap states exist at a bare Si surface which, acting as SRH recombination centers, make the SRV very large, around 10^5 cm·s^{-1} [23, 24]. In order to reduce surface recombination, two main approaches are followed [25].

In the first one, the density of electron surface states in the gap is decreased. This is accomplished by depositing or growing a layer of an appropriate material that partially restores the bonding environment of surface Si atoms. This material must be an insulator.

Thermal SiO_x is grown in an oxygen-rich atmosphere at the expense of substrate Si atoms at high temperatures around 1000°C. SiN_x is deposited by plasma-enhanced chemical vapor deposition (PECVD) [26] at low temperatures between 300 and 400°C range. The quality of both techniques is very sensitive to subsequent treatments, with hydrogen playing a major role in obtaining low SRV values below 100 cm·s^{-1}.

As a general rule, *S* increases with the doping of the substrate [23, 24]. It also depends on the injection level and doping type, because the interfaces contain positive

charges that affect the number of carriers at the surface, and because the capture probability for electrons and holes is different [27]. N-type or intrinsic surfaces are usually better than p-type ones. Stability under UV exposure is another fundamental concern.

In the second approach, the excess carrier density at the interface is decreased relative to the bulk. This effect has already been commented upon with respect to contacts and results in a reduced effective SRV at the bulk edge of the corresponding space charge region. It can be produced by charges in the surface layer, by the electrostatics associated to a MOS structure [28] or by doping.

The surface layer can be accumulated or inverted, or, correspondingly, doped with the same or the opposite type of the substrate. Its recombination activity is better described by a constant saturation current density, J_0, whose minimization follows the same rules as mentioned for the contacts if S at the surface is high. On the contrary, if S is low when compared to D/L for minority carriers (with D the diffusion constant and L the diffusion length in the substrate) in the surface layer, it is better for it to be thin or "transparent" to minority-carrier flow ($w < L$). The optimum doping level is a compromise between reduction of the excess carriers, and heavy doping effects and the increase of the SRV with doping. Moderate doping levels are favored in this case. Under passivated surfaces, J_0 values around 10^{-14} A·cm^{-2} are achievable, with phosphorus-doped substrates giving better results than boron-doped ones [16, 17].

In conclusion, recombination at a noncontacted surface can be made much smaller than at a metallized one, and this has a deep influence in the evolution of Si solar cell design.

7.3 CRYSTALLINE SILICON SOLAR CELLS

7.3.1 Cell Structure

Several studies have been carried out to find the limiting efficiency and the optimum structure of a-Si solar cell [29–31]. All avoidable losses are assumed to be suppressed:

1. no reflection losses and maximum absorption as achieved by ideal light-trapping techniques,
2. minimum recombination: SRH and surface recombination are assumed avoidable and only Auger recombination remains,
3. the contacts are ideal: neither shading nor series resistance losses,
4. no transport losses in the substrate: the carrier profiles in the substrate are flat so that recombination is the minimum possible for a given voltage.

The optimum cell should use intrinsic material, to minimize Auger recombination and free-carrier absorption, and should be around 80-μm thick, the result of the trade-off between absorption and recombination. It could attain nearly 29% efficiency at one sun AM1.5 Global, 25°C [30].

This ideal case does not tell us where to put the contacts. To realize Condition 4 mentioned above, the contacts should be located at the illuminated or the front face, closest to photogeneration (Figure 7.1a). Because of metal shading losses this threatens

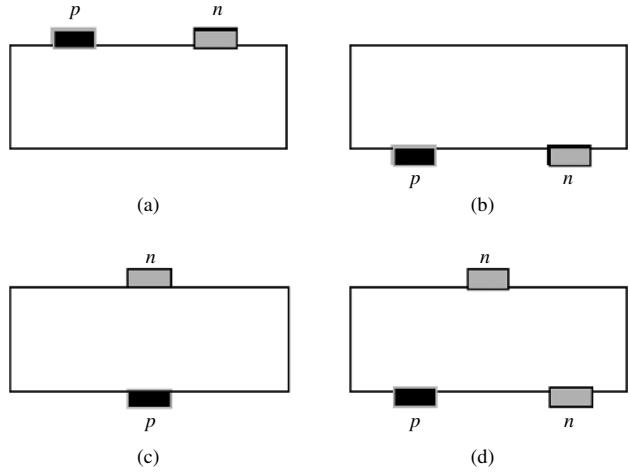


Figure 7.1 Contacting structures: (a) both contacts at the front; and (b) at the back; (c) both faces contacted; and (d) one carrier extracted at both faces. The structures with interchanged *n*- and *p*-types are also possible

Condition 3 mentioned above. This solution is being considered for concentration [32]. Putting both contacts at the back works the other way round (Figure 7.1b). Back-contacted cells exhibit record efficiencies under concentration and demonstrate very high values near 23% at one sun [33].

In most cells, each contact is placed on a different face, which is technologically simpler (Figure 7.1c). Minority carriers in the substrate are usually collected at the front since their extraction is more problematic because of their low density. The diffusion length describes the maximum distance from where they can be collected. Majority carriers can drift to the back contact with low loss. Several designs extract minority carriers both at the front and at the back (Figure 7.1d) [34], thus increasing the volume of profitable photogeneration.

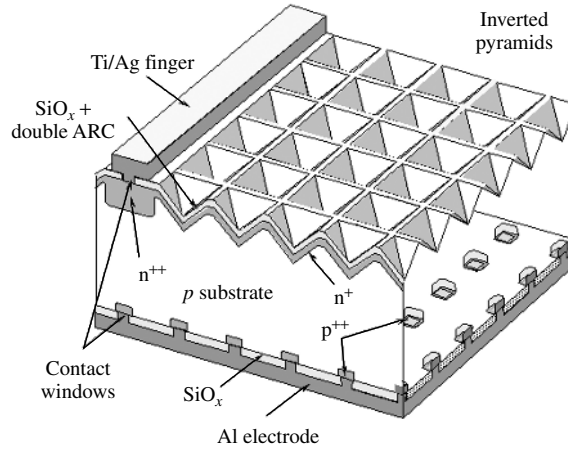
Bifacial cells are designed to collect light incident at both faces, which allows a boost in output power if there is a significant albedo component. They can be implemented with any structure in Figure 7.1 on the condition that both surfaces allow light through [35].

Both 24.7% record-efficiency laboratory solar cells [36] (Figure 7.2a) and mass-produced industrial devices (Figure 7.2b), typically 15% efficient, display the contacting structure in Figure 7.1(c). They will be described in the paragraphs that follow with the aim of illustrating the amplitude and the reasons for the performance gaps between the ideal and the best Si cell, and between this cell and industrial cells.

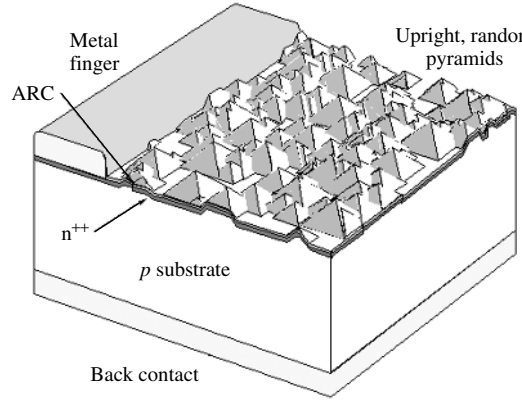
7.3.2 Substrate

7.3.2.1 Materials and processing

Highest efficiencies are achieved with monocrystalline float zone (FZ-Si) material, which in addition to extreme crystalline perfection shows the lowest contamination levels of both



(a)



(b)

Figure 7.2 (a) Passivated emitter and rear locally diffused (PERL) cell; and (b) industrial cell with screen-printed contacts. (Not to scale)

metallic and light (O, C, N) impurities. This translates into the longest post-processing SRH lifetimes in the millisecond range, but still shorter than the Auger limit. Magnetic Czochralski (MCz) material contains much less oxygen than conventional Czochralski and also allows very high efficiencies to be obtained [36].

Industrial cells use Czochralski (Cz-Si) wafers because of their availability. Cz wafers are also perfect crystals but they contain a high concentration of oxygen that affects lifetime in several ways [37]. Some commercial devices are made on multicrystalline (mc-Si) substrates grown in blocks or ribbons with procedures specially developed for photovoltaics. In addition to crystal defects, such as grain boundaries and dislocations, the potential content of metallics is higher because of lower segregation to the melt during the faster solidification process. As a result, the lifetime of mc-Si is lower.

But lifetime is important at the end of solar cell fabrication during which it can undergo strong variations. This issue is handled in different ways in a laboratory and a factory environment. In the laboratory, measures are taken to maintain long initial lifetimes by avoiding contamination during high-temperature steps: furnace cleaning, ultra pure chemicals and so on. In a rough, industrial environment and with defect-containing (Cz- and mc-Si) materials, the problem is more complex: in addition to contamination from the surroundings, impurities and defects in the substrate move, interact and transform at high temperature. The solution is to integrate gettering steps [38] in the fabrication flow that reduce the impact of contamination, and to tailor the thermal treatments to the peculiarities of the material. Final substrate lifetimes of industrial cells range from 1 to 10 μs.

Gettering techniques eliminate or reduce contaminant impurities in a wafer, and so neutralize the effect of lifetime reduction. Although gettering processes are not always well understood, it is admitted, in general, that in a gettering process a sink region is formed, which is able to accommodate the lifetime-killing impurities in such a way that they are not harmful to the device being manufactured, or at least they are where they can be easily removed.

In solar cell fabrication, we take advantage of the fact that phosphorus and aluminum diffusions, appropriate candidates for emitter and BSF layers, respectively, produce gettering in certain conditions [39]. Other techniques have been explored [40, 41], but their integration in a solar cell process is not so straightforward.

P gettering effect has been proved for a wide variety of P diffusion techniques (spin-on, $POCl_3$, PH_3 etc), provided diffusion is done in supersaturation conditions (i.e. over its solid solubility in silicon). Unfortunately, this leaves a "dead layer" of electrically inactive phosphorus near the surface, which reduces UV response of the cells in case it is not etched away [42]. Another phenomenon related to this supersaturated P is the injection of silicon self-interstitials to the bulk of the material, which is responsible for an enhancement of the gettering effect [43].

When Al is deposited on Silicon (by different techniques such as sputtering, vacuum evaporation or screen printing) and annealed over the eutectic temperature (577°C), a liquid Al-Si layer is formed, where impurities tend to segregate because of their enhanced solubility [44]. They will remain in this gettering layer while cooling, so that bulk lifetime will improve after the process.

Another approach to improve material quality is "bulk passivation", a treatment with hydrogen, for example, during SiN_x deposition, to which some defected materials respond very well [45].

7.3.2.2 Doping level and type

Both laboratory record-efficiency and industrial cells use boron-doped substrates. Rather than fundamental advantages [46], there are practical (properties of P diffusion, easiness of Al alloying) and historical reasons for this preference [47]. However, the situation may change once the role of boron in the degradation of Cz-Si cells under illumination has been established [48].

The optimum substrate doping depends on the cell structure and dominant recombination mechanism. Though intrinsic substrates present the advantage of highest Auger-limiting lifetimes, higher doping is favored when SRH recombination is present, since recombination is proportional to the excess density that decreases, for a given voltage, as doping increases [29]. This is balanced with a reduction of the lifetime itself.

A high doping also helps in minimizing the series resistance losses associated to the transport of carriers to the back face in thick cells with the majority carrier contact at the back.

Doping levels in the 10^{16} cm^{-3} range are found in the substrate of industrial cells. Very high efficiencies have been obtained with both low (1 Ω·cm for PERL cells) and high substrate resistivities, as in the point-contact cells [33].

7.3.2.3 Thickness

From the point of view of electrical performance, the choice of the optimum substrate thickness also depends on the structure and the quality of the materials and involves several considerations. In cells with diffusion lengths longer than the thickness, the most important issue is surface recombination: if S at the back is higher than D/L for the minority carriers in the substrate (around 250 $cm \cdot s^{-1}$ for the best cells), thinning the cell increases recombination at a given voltage, and vice versa. Thinner cells always absorb less light as well, which is attenuated by light-trapping techniques. Passivated emitter and rear locally diffused (PERL) cells were reported to improve when going from 280- to 400-μm thickness because of a (relatively) high rear surface recombination and nonideal light-trapping [49].

The losses associated with the transport of carriers extracted at the nonilluminated face decrease with thinning: in conventional structure cells; this leads to decreased series resistance. In back-contacted cells, both types of carriers benefit from thinning and the trade-off in absorption leads to lower w values, around 150 to 200 μm.

The diffusion length of industrial cells (around 100 μm) is generally lower than thickness. These cells are rather insensitive to thinning because they collect only the generation near the contact and are not affected by rear surface recombination. The driving criteria are cost and fabricability. A thickness in the 200- to 300-μm range is usually employed but there is a clear trend toward thinner wafers for saving expensive silicon material [47], and advanced wafering techniques and procedures to process very thin, large-area substrates without breaking are being developed: light-trapping and back recombination will become increasingly important.

7.3.3 The Front Surface

7.3.3.1 Metallization techniques

Metal grids are used at the front face to collect the distributedly photogenerated carriers. The compromise between transparency and series resistance requires metallization technologies able to produce very narrow but thick and highly conductive metal lines with

a low contact resistance to Si. Laboratory cells use photolithography and evaporation to form 10- to 15-μm metal fingers. Ti/Pd/Ag structures combine low contact resistance to *n*-Si and high bulk conductivity. These processes are not well suited to mass production that relies on thick-film technologies. Ag pastes are screen printed, resulting in over 100-μm wide lines with higher bulk and contact resistance. Laser-grooved buried-grid (LGBG) industrial cells implement a finer metallization technology [50], which will be presented in Section 7.7.3.

Coarser metallization techniques imply higher shading and resistance losses, and restrict the efficiency enhancement that could be achieved by internal cell design.

7.3.3.2 Homogeneous emitters

Under the metal lines, the substrate must be heavily doped to make the contact selective. Usually the doped region, the emitter, extends all across the front surface, acting as a "transparent electrode" by offering minority carriers in the substrate a low resistance path to the metal lines.

When the exposed surface is not passivated (Figure 7.3a), the emitter should be as thin as possible, because the high SRV makes the light absorbed in this region poorly collected, and also highly doped to decrease recombination. On the other hand, a sufficient low-sheet resistance is to be achieved. The solution is to make very thin and highly doped emitters.

If the surface is passivated (Figure 7.3b), the collection efficiency of the emitter can be raised by lowering the doping level thus avoiding heavy doping and other detrimental

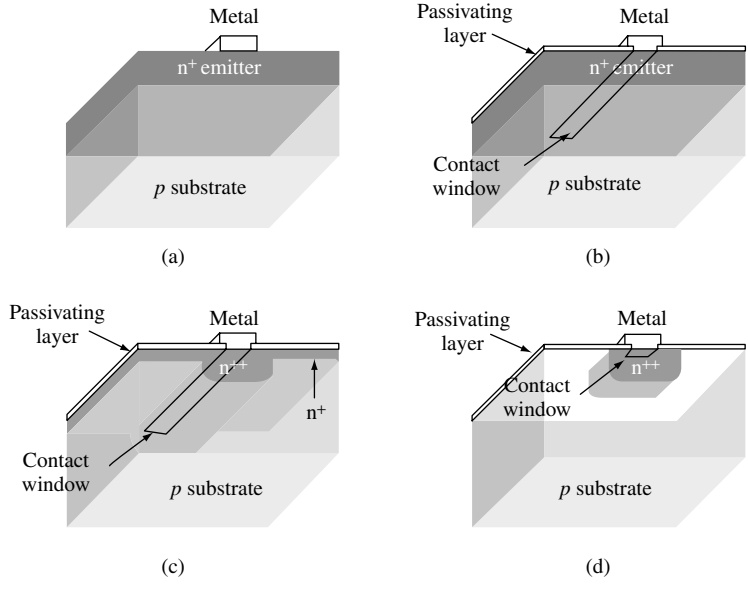


Figure 7.3 Different emitter structures: (a) homogenous emitter without surface passivation; (b) homogenous emitter with surface passivation; (c) selective emitter; and (d) localized emitter

effects. This must be balanced with contact resistance. Etching off of the passivating layer before metallization is usually needed (not in screen-printed cells). To maintain low sheet resistance and diminish recombination at the metallized fraction, the emitter is deep (around 1 μm). Note that the collection of carriers near the surface implies that the emitter is thin in terms of the minority-carrier diffusion length ($w < L$) and so it is very sensitive to surface recombination. Recombination is further reduced, by making the contact window narrower than the finger width, as illustrated in Figure 7.3 [51].

Control of both the surface concentration and the depth of the emitter, is achieved by depositing, in a thermal step, the desired amount of phosphorus or boron (predeposition) and then diffusing it into the substrate (drive-in) during subsequent furnace steps. The MIS solar cell, on the contrary, uses no diffusion for the n region, which is electrostatically induced by charges on top of the surface [20].

The J_0 of the emitter is the average, weighted by the contacted area, of the J_0 of contacted and noncontacted portions.

7.3.3.3 Selective and point emitters

A further improvement involves making separate diffusions for the different regions since the requirements are so different (Figure 7.3c) [52]: a heavily doped and thick region under the contacts, a thin and lowly doped region under the passivating layer. These structures, known as "selective emitters", come at the expense of more complicated processing usually involving photolithographic delineation and alignment of the diffusions (not in LGBG cells to be seen later).

If a very low SRV is possible, it would be best to have no emitter at all since doping always degrades bulk lifetime (Figure 7.3d). Examples are the back point-contact solar cell and the point-emitter design with bifacial contact [53], originally designed for concentration but capable of very high one-sun efficiency as well.

With localized contacts, surface recombination decreases with the penalty of an increase in transport losses in the substrate: deeper gradients for minority carriers, or increased series resistance for majority carriers, because of current crowding near the contacts. The trading is more favorably solved as the contact size shrinks [54]. Light and/or localized diffusions also have the drawback of decreased gettering action.

7.3.3.4 Industrial cells

Screen printing drastically affects the design of the emitter: it must be very highly doped to decrease the high-contact resistance and not very shallow so that it is not perforated during paste firing, which would short-circuit the junction [55]. Besides, the wide metal lines must be placed well apart; and in order to keep shading losses moderate, the emitter lateral conductance must be high, which also advises deep and highly doped regions. These characteristics are good to decrease recombination at the contacts, but are far from optimum at the exposed surface.

Industrial phosphorus emitters, typically, feature surface concentrations over 10^{20} cm^{-3} and 0.4-μm depth, and result in a sheet resistance around 40 Ω. As already

mentioned, the very highly doped region exhibits almost no photovoltaic activity due to the presence of precipitates ("dead layer"). As a result, the collection of short-wavelength light is very poor and the J_0 large, irrespective of a hypothetical surface passivation is therefore not implemented. The advantage is that heavy phosphorus diffusions produce very effective gettering. Some ways of incorporating selective emitters to screen-printed cells are being considered, SiN_x appearing very well suited for surface passivation [55]. This, however, must be accompanied by a decrease in the finger width so that lower sheet resistances are tolerated.

7.3.4 The Back Surface

The majority carrier, back p-contact of industrial solar cells is usually made by printing, and subsequently, firing an aluminum-containing Ag-conducting paste.

The p^+ layer would be useful in decreasing contact recombination, as explained, but this is immaterial to the electrically thick ($w > L$) present industrial cells and it is not optimized for this purpose.

For high-efficiency cells, contact passivation is essential. A BSF is a first step (Figure 7.4a). Localized contacts, as shown in Figure 7.4(b), further reduce recombination. This structure is presented by some of the bifacial cells [56].

If the surface passivation is good, the BSF is restricted to point contacts, some microns in size, as in PERL and similar cells (Figure 7.4c) [57]. The back face of bifacial cells passivated with SiN_x is shown in Figure 7.4(d).

A shallow and light diffusion helps in decreasing surface recombination (Figure 7.4e). The diffusion can be the same type of the substrate, or the opposite one: so-called PERT (Passivated emitter rear totally diffused) [36] and PERF (Passivated emitted rear floating junction) [58] cells demonstrate these concepts. The latter structure benefits from the lower J_0 values of n^+ layers, and it is essential that no electron flow is injected from the n region to the p contact: the junction must be in open-circuit (a "floating" junction). Note that this structure has nothing to do with structures sometimes found at the back of industrial cells (Figure 7.4f) where a coarse metal mesh is fired through the parasitic n^+ layer formed during front diffusion. A mesh is preferred to a continuous layer for mechanical reasons. The junction is shorted and presents to the substrate a high SRV.

7.3.5 Size Effects

Substrate edges are highly recombining surfaces that adversely affect cell performance, especially for small size, large diffusion length devices. For laboratory cells, efficiency is defined on the basis of a design area. The emitter is limited to it by planar masking or mesa etching. The true edge is thus placed far away from the cell limit, and then recombination is reduced. For real applications, on the contrary, only the substrate area counts, and edge optimization is more complex. Advanced passivation schemes such as edge diffusions are being considered [59, 60]. In large industrial cells, this recombination is much less important.

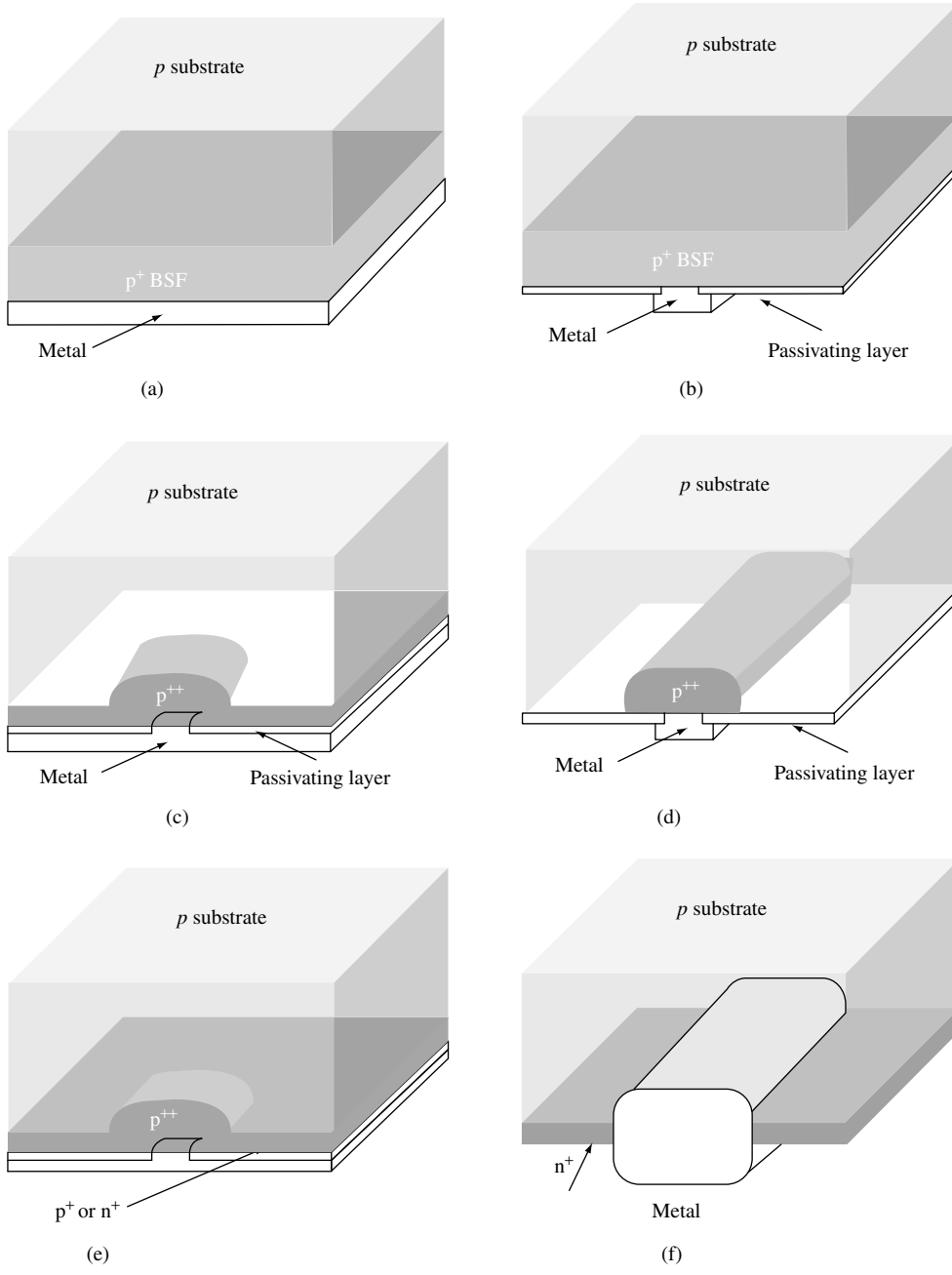


Figure 7.4 Rear contact structures: (a) continuous BSF; (b) bifacial cell; (c) local BSF; (d) local BSF, bifacial cell; (e) selective emitter or floating junction passivation; and (f) shorted junction at the back face of industrial cells

Large cell sizes are preferred by the industry, 10×10 cm^2 or 12.5×12.5 cm^2 being standard. Apart from fabricability concerns, a bigger cell means that more current must be collected at the terminals, making Joule losses grow: the longitudinal resistance of the metal lines increases quadratically with their length. This problem, more severe for coarser metallization techniques, decreases efficiency with increasing size. To alleviate series resistance at the price of increased shading, terminals are soldered to metal bus bars inside the cell's active area, thus decreasing the distance from where current must be collected along the fingers.

7.3.6 Cell Optics

Flat plate solar cells in operation are illuminated from a large portion of the sky, not only because of the isotropic components of radiation, but also because of the sun's apparent motion over the day and the year. So, with regard to angular distribution, these cells must accept light from the whole hemisphere. The spectral distribution also varies with time, weather conditions, and so on. For calibration purposes, a standard spectral distribution AM1.5 Global is adopted as a representative condition, usually specified at 0.1 W·cm^{-2}.

A solar cell should absorb all useful light. For nonencapsulated cells, the first optical loss is the shading by the metal grid at the illuminated face, if any. This loss can amount to more than 10% for industrial cells while for laboratory cells using fine metallization it is much lower. Though several techniques have been proposed to decrease the effective shading, such as shaped fingers, prismatic covers, or cavities [61], their efficacy depends upon the direction of light and so they are not suited to isotropic illumination.

7.3.6.1 Antireflection coatings

Next, loss comes from the reflectance at the Si interface, more than 30% for bare Si in air due to its high refraction index. A layer of nonabsorbing material with a lower refraction index (n_{ARC}) on top of the Si substrate decreases reflectance: this is a step toward the zero-reflection case of a smoothly varying refraction index. If the layer is thick in terms of the coherence length of the illumination, around 1 μm for sunlight, there are no interference effects inside it. The encapsulation (glass plus lamination) belongs to this category.

Antireflection coating (ARC) means an optically thin dielectric layer designed to suppress reflection by interference effects. Reflection is at a minimum when the layer thickness is (an odd multiple of) $n_{ARC}\lambda_0/4$, with λ_0 the free space wavelength, since in this case reflected components interfere destructively. At other wavelengths reflection increases, but is always below the value with no ARC or, at most, equal [62]. The ARC is usually designed to present the minimum at around 600 nm, where the flux of photons is a maximum in the solar spectrum. For reflection to become zero at the minimum, the coating index should be the geometric average of those of air and silicon, that is, 2.4 at 600 nm for nonencapsulated cells.

The industry uses TiO_x deposited by chemical vapor deposition (CVD). PECVD SiN_x is very interesting since it also serves as a passivating layer, as explained earlier.

By using double layer coatings with $\lambda/4$ design, with growing indices from air to silicon, the minimum in reflection is broader in wavelength. Evaporated SZn and MgF_2

are used in laboratory high-efficiency cells. The low index of passivating SiO_x in contact with Si degrades the performance of the ARC. The SiO_x layer is then made as thin as is compatible with efficient passivation [63].

7.3.6.2 Texturing

Alkaline (KOH or NaOH-based) solutions etch anisotropically a-Si crystal exposing {1 1 1} planes on which the etching rate is lowest. On [1 0 0]–oriented wafers, randomly distributed, square-base pyramids are formed, whose size is adjusted to a few microns by controlling etching time and temperature. In a textured face, a ray can be reflected toward a neighboring pyramid (Figure 7.5a) and hence absorption is enhanced. Though calculation of reflection requires ray tracing, a rough estimate of near-normal incidence can be derived, by assuming that each ray strikes twice the Si surface so that reflection is the square of the untextured case.

Texturing is incorporated into both industrial and laboratory Si solar cells, and, in combination with antireflection (AR) coating, reduces reflection losses to a few percent. In the latter case, in order to better control the pyramid geometry and to allow delineation of fine features on the surface, photolithographic techniques are used to define inverted or upright pyramids at the desired positions. It has to be noted that in this case the reflectivity is similar to that of a random texture [64].

Light entering the substrate at a textured surface is tilted with respect to the cell normal. This means that photogeneration takes place closer to the collection junction, which is very beneficial for low-diffusion length cells, by enhancing the collection efficiency of medium- to long wavelengths (Figure 7.5a). The effect is equivalent to an increase of the absorption coefficient. As a drawback, textured surfaces present higher SRVs.

7.3.6.3 Light-trapping

Long-wavelength photons are weakly absorbed in silicon, and, unless internal reflectances are high, they will escape the substrate without contributing to photogeneration. The aim of light-trapping or light confinement techniques is to achieve high internal reflectances.

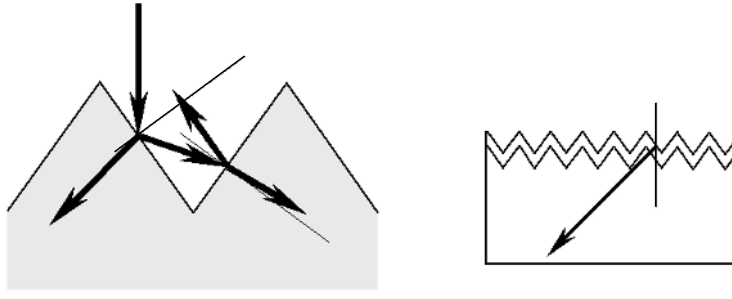


Figure 7.5 Effects of surface texturing: (a) decreased reflection; and (b) increased photogeneration in the base

Practical back mirrors that are fully compatible with the cell electrical design, can be implemented, such as those schematized in Figure 7.4. A metal can make a good reflector, but Al, especially after heat treatment, gives low reflectance. The Si-oxide-metal structure in Figure 7.4(c) can present a high reflectance by capitalizing on interference effects [65].

At the front, the metal mirror is not applicable because the ray paths must be kept open for the entering light. Still, high front reflectance can be achieved because of total internal reflection [61]. Rays striking the surface at angles larger than the critical air-Si one are totally reflected. Texturing one or both surfaces with macroscopic or microscopic features serves this purpose by tilting the rays. Even in the case of geometric texturing with well-defined surface orientations, after a few internal reflections, the direction of rays inside the wafer is randomly distributed: this is the lambertian case, useful analytic approximation to light-trapping. Bifacial structures in Figure 7.4 can, for the same reason, be very efficient at confining the light [66].

Light-trapping increases the effective thickness of the wafer for absorption. In the geometrical optics regime, it has been shown that for one-side isotropic illumination the maximum enhancement factor (though perhaps not realizable) is 4 $(n_{Si}/n_{air})^2$, that is, each ray traverses 50 times the cell thickness before escaping [67]. The corresponding enhancement in photogeneration will be lower because of the competition of the absorption by free carriers at long wavelength.

Light-trapping is essential for thin cells. Even in the thick PERL design it can suppose around 1 $mA \cdot cm^{-2}$ enhancement in short-circuit current with respect to the case where the internal reflectances were zero.

7.3.7 Performance Comparison

For illustration purposes, Table 7.3 collects relevant parameters of the Auger-limited ideal Si solar cell [30], the best one-sun PERL cell [36] and a typical screen-printed, industrial cell on Cz-Si. The different concepts behind each set of data must be accounted for when comparing the figures. For instance, the ideal cell is assumed as being isotropically illuminated, while measurements are made for near-normal incidence.

Table 7.3 Cell performance (25°C, AM1.5 Global 0.1 $W \cdot cm^{-2}$)

Cell type	Ideal (calculated)	PERL (measured)	Industrial (typical)
Size (cm^2)	–	4	100
Thickness (μm)	80	450	300
Substrate resistivity ($\Omega \cdot cm$)	Intrinsic	0.5	1
Short-circuit current density, J_{SC} ($A \cdot cm^{-2}$)	0.0425	0.0422	0.034
Open-circuit voltage, V_{OC} (V)	0.765	0.702	0.600
Fill factor, *FF*	0.890	0.828	0.740
Efficiency, η (%)	28.8	24.7	15.0

The most striking difference between the best and the ideal solar cell is the difference in design: thick and low injection *versus* thin and high injection. The PERL cell is surely the best design for the currently achievable levels of surface recombination, which limit open-circuit voltage and shift the optimum thickness to high values. The low resistivity follows then from transport considerations for the chosen structure. The very high fill factor of the ideal cell is characteristic of high injection, Auger-limited operation.

Reduction of surface recombination in the best laboratory cells relies on surface passivation and the restriction of very heavily doped regions to a minimum. In the end, this is possible because of the possibility of defining and aligning very small features on the surfaces.

The very heavily doped emitter, along with lower substrate lifetimes, is responsible for the reduced short-circuit current and open-circuit voltage in the industrial cell. The fill factor is affected by the large device area in conjunction with the limitations of the metallization technique, which further reduces the current because of shading.

Continuous improvement in material quality and cost-driven thinning of the substrates will increase the need for industrial cells to implement surface passivation schemes. This will require the refinement of the metallization technique; another issue is that substrate lifetimes in an industrial environment depend on the gettering action of very heavy diffusions, which are not compatible with optimum surface performance. The PERL approach – high-temperature processes and delineation of fine features – is the most successful path to high efficiency, but it is not the only one that can inspire the forthcoming developments in industrial cells. It is worth noting, in this respect, that heterojunction with intrinsic thin-layer (HIT) solar cells have entered the exclusive club of more than 20% efficiency with a different approach (see Section 7.7.2).

7.4 MANUFACTURING PROCESS

7.4.1 Process Flow

Figure 7.6 shows the main steps of a simple process for solar cell fabrication based on screen printing. With more or less minor modifications, this process is currently used by many manufacturers. The main virtues of this 30-year-old PV technology are easy automation, reliability, good usage of materials and high yield. The drawback, as explained in preceding sections, is the efficiency penalty derived from the coarse and aggressive metallization technique. Some specific treatments worked out for mc-Si will be explained in Section 7.6.

Each step is briefly described in the following text with illustrative purposes: values of temperature, time and so on will only be indicative.

1. *Starting material*: The industry uses so-called solar grade Cz-Si wafers, round in origin but very often trimmed to a pseudo-square shape, or multicrystalline square wafers. Wafer dimensions are between 10- and 15-cm side and between 200- and 350-μm thickness. Doping is *p*-type (boron) to a resistivity of around 1 Ω·cm.
2. *Saw damage removal*: The sawing operation leaves the surfaces of "as cut" wafers with a high degree of damage. This presents two problems: the surface region is of

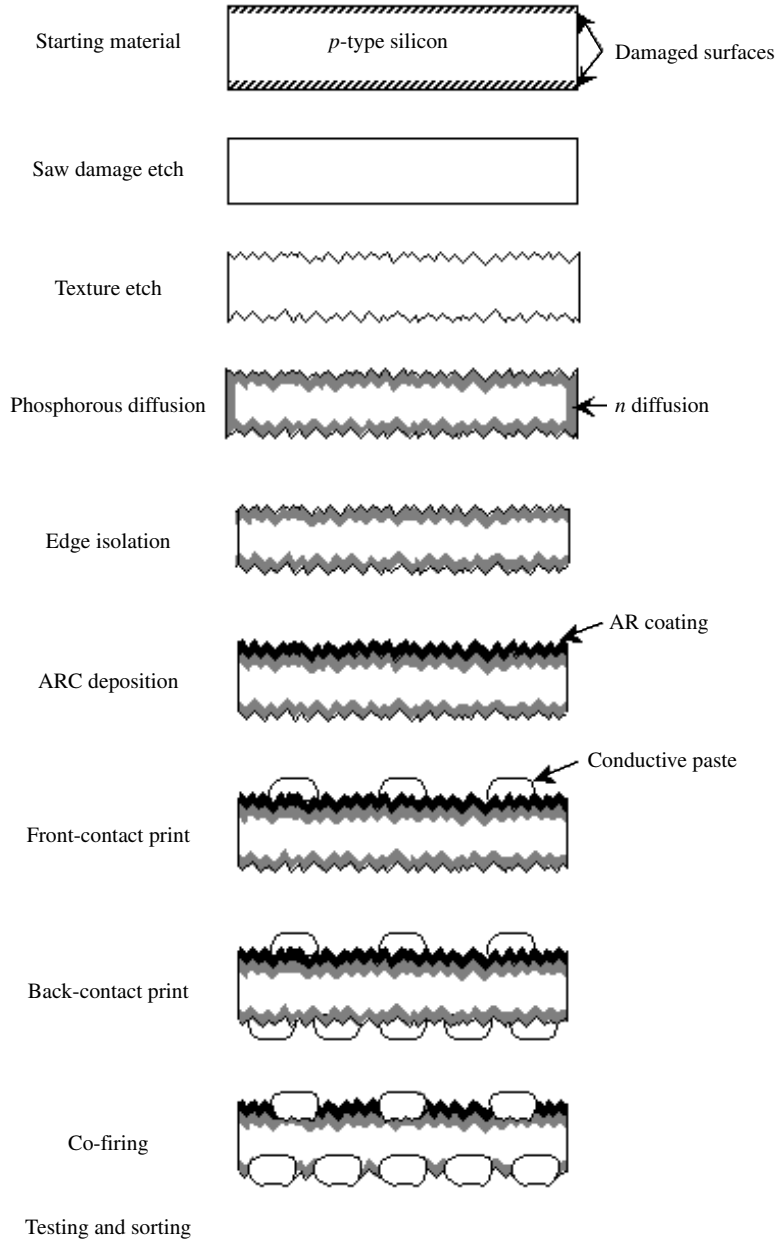


Figure 7.6 A typical processing sequence with schematic illustrations of the resulting structures

a very bad quality and the defects can lead to wafer fracture during processing [68]. For this reason, about ten microns are etched off from each face in alkaline or acid solutions. The wafers, in Teflon cassettes, are immersed in tanks containing the solution under temperature and composition control. Alkaline etches are preferred to acid solutions due to considerations of waste disposal.

3. *Texturization*: NaOH etching leading to microscopic pyramids is commonly employed. Their size must be optimized, since very small pyramids lead to high reflection, while very large ones can hinder the formation of the contacts. To ensure complete texturing coverage and adequate pyramid size, the concentration, the temperature and the agitation of the solution and the duration of the bath must be controlled (in fact NaOH at a higher concentration and at a higher temperature is commonly used as an isotropic etch for saw damage removal). Alcohol is added to improve homogeneity through an enhancement of the wettability of the silicon surface. Typical parameters are 5% NaOH concentration, 80°C and 15 min [69].
   Texturing alternatives for multicrystalline material are presented in Section 7.6.
4. *Phosphorus diffusion*: Phosphorus is universally used as the *n*-type dopant for silicon in solar cells. Since solid-state diffusion demands high temperature, it is very important that the surfaces are contamination-free before processing. To this end, after the texturing the wafers are subjected to acid etch to neutralize alkaline remains and eliminate adsorbed metallic impurities.
   The industry uses a number of procedures to perform the phosphorus diffusion. The following classification is based on the type of furnace in which the high-temperature step takes place:
   Quartz furnaces: The cells to be diffused, loaded in quartz boats, are placed in a quartz tube with resistance heating and held at the processing temperature (Figure 7.7a). The cells enter and exit the furnace through one end, while gases are fed through the opposite one. Phosphorus itself can be supplied in this way, typically by bubbling nitrogen through liquid $POCl_3$ before injection into the furnace. Solid dopant sources are also compatible with furnace processing. Five to fifteen minutes at temperatures in the range from 900 to 950°C can be considered representative. As suggested in Figure 7.6, both surfaces and the edges of the wafer will be diffused.

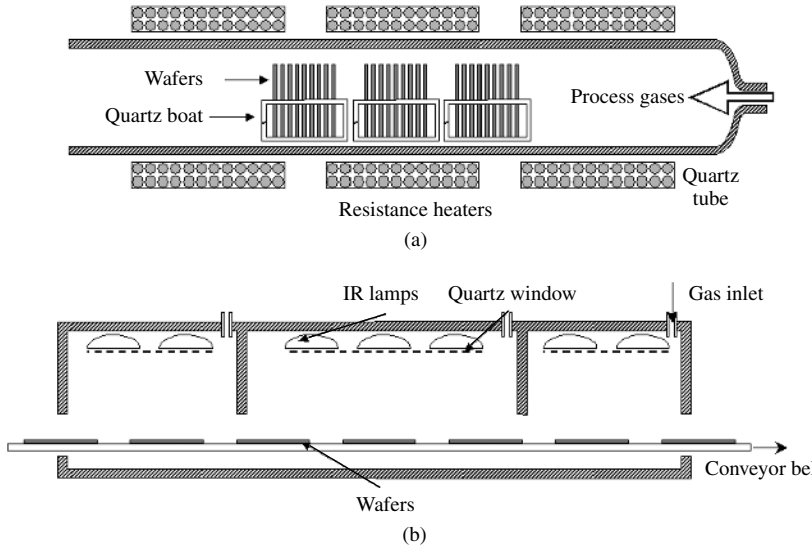


Figure 7.7 (a) A quartz furnace; and (b) a belt furnace for the diffusion of phosphorus

Belt furnaces: In this case, solid phosphorus sources are used: screen printed, spun-on or CVD pastes containing phosphorus compounds are applied on one wafer face and, after drying, placed in a conveyor belt passing through the furnace (Figure 7.7b). The temperature inside it can be adjusted in several zones and, though the furnace is open, gases can be supplied. The temperature cycle undergone by the wafer will mimic the temperature profile along the furnace with the time scale set by the advancing speed of the belt. A cycle begins with several minutes at around 600°C with clean air to burn off the organic materials of the paste, followed by the diffusion step in nitrogen at 950°C for 15 min. Only one face of the wafer is diffused, but the parasitic junction formed at the edges is also present in this technique due to diffusion from the gas phase. Resistance or infrared heating can be employed, the latter offering the possibility of faster heating–cooling rates of the wafer.

The main benefit of the quartz furnace is cleanliness, since no metallic elements are hot and no air flows into the tube. Though this is a batch step, high throughput can be achieved since many wafers can be simultaneously diffused in each tube, commercial furnaces consisting of stacks of four tubes. In a belt furnace, the ambient air can get into the furnace and the hot conveyor belt is a source of metallic impurities. The assets of belt furnaces are found in automation and in-line production, throughput and the ability to implement temperature profiles. New designs try to reconcile the advantages of both types of equipment [70].

After diffusion, an amorphous glass of phospho-silicates remains at the surface that is usually etched off in diluted HF because it can hinder subsequent processing steps.

5. *Junction isolation*: The *n*-type region at the wafer edges would interconnect the front and back contacts: the junction would be shunted by this path translating into a very low shunt resistance. To remove this region, dry etching, low temperature procedures are used.

   For the widely employed etch with plasma, the cells are coin-stacked and placed into barrel-type reactors. In this way, the surfaces are protected and only the edges remain exposed to the plasma. This is obtained by exciting with an RF field a fluorine compound (CF_4, SF_6), which produces highly reactive species, ions and electrons that quickly etch the exposed silicon surface [71]. Though this is a batch step, a large number of wafers can simultaneously be processed allowing high throughput. Laser cutting of the wafer edges is an alternative in industrial use.

6. *ARC deposition*: Titanium dioxide (TiO_2) is often used for creating the antireflecting coating due to its near-optimum refraction index for encapsulated cells. A popular technique is atmospheric pressure chemical vapor deposition (APCVD) from titanium organic compounds and water: the mixture is sprayed from a nozzle on the wafer held at around 200°C and the compound is hydrolyzed on the surface [72]. This process is easily automated in a conveyor-belt reactor. Other possibilities include to spin-on or screen print appropriate pastes.

   Silicon nitride is also used as AR coating material with unique properties that will be described in Section 7.6.

7. *Front contact print and dry*: The requirements for the front metallization are low contact resistance to silicon, low bulk resistivity, low line width with high aspect ratio, good mechanical adhesion, solderability and compatibility with the encapsulating

materials. Resistivity, price and availability considerations make silver the ideal choice as the contact metal. Copper offers similar advantages, but it does not qualify for screen printing because subsequent heat treatments are needed during which its high diffusivity will produce contamination of the silicon wafer.

Screen printing compares very unfavorably with vacuum evaporation in the first three requirements. It has been already commented how this affects the cell design and leads to a significant efficiency gap between laboratory and commercial cells. But throughput and cost compensate for it.

Screen printing will be described in more depth in the following section. It is used to stick a paste containing silver powder to the front face of the wafer in the comblike (fingers plus bus bars) pattern. Automatic screen printers are available that are capable of in-line, continuous operation with high throughput. These machines accept wafers from packs, cassettes or a belt line, place them with sufficient accuracy under the screen and deliver the printed wafers to the belt line. The paste is a viscous liquid due to the solvents it contains; these are evaporated in an in-line furnace at 100 to 200°C. The dried paste is apt for subsequent processing.

8. *Back contact print and dry*: The same operations are performed on the backside of the cell, except that the paste contains both silver and aluminum and the printed pattern is different.

   Aluminum is required because silver does not form ohmic contacts to p-Si, but cannot be used alone because it cannot be soldered. The low eutectic temperature of the Al-Si system means that some silicon will be dissolved and then recrystallize upon cooling in a p-type layer.

   Though in principle a continuous contact will give better electrical performance (lower resistance), most commercial wafers feature a back contact with a mesh structure: apart from paste-saving considerations, this is preferred to a continuous layer because the different expansion coefficients would produce warp of the cell during the subsequent thermal step.

9. *Cofiring of metal contacts*: A high-temperature step is still needed: organic components of the paste must be burnt off, the metallic grains must sinter together to form a good conductor, and they must form an intimate electric contact to the underlying silicon. As Figure 7.6 shows, the front paste is deposited on an insulating layer (the AR coating) and the back contact on the parasitic n-type rear layer.

   Upon firing, the active component of the front paste must penetrate the ARC coating to contact the n-emitter without shorting it: too mild a heat treatment will render high contact resistance, but too high a firing temperature will motivate the silver to reach through the emitter and contact the base. In extreme situations, this renders the cell useless by short-circuiting it. In more benign cases, small shunts appear as a low shunt resistance or dark current components with a high ideality factor that reduces the fill factor and the open-circuit voltage.
   The back paste, in its turn, must completely perforate the parasitic back emitter to reach the base during the firing.
   In order to comply with these stringent requirements, the composition of the pastes and the thermal profile of this critical step must be adjusted very carefully.

10. *Testing and sorting*: The illuminated $I-V$ curve of finished cells is measured under an artificial light source with a spectral content similar to sunlight (a sun simulator)

at a controlled temperature of 25°C. Defective devices are then rejected, and the rest are classified according to their output. The manufacturer establishes a number of classes attending, typically, to the cell current at a fixed voltage near the maximum power point. Modules will subsequently be built with cells of the same class, thus guaranteeing minimal mismatch losses. If, for instance, cell currents within a class must be equal within 5%, the accuracy and stability of the system must be better than that. Automatic testing systems that meet the very demanding requirements of high throughput processing are available.

7.4.2 Screen-printing Technology

Screen printing is a thick-film technology, a terminology that opposes it to the usual microelectronic procedures of evaporation of thin films. It consists in translating a layer of a material in a desired pattern to the surface of the wafer. Though it can be employed for virtually any step in solar cell manufacturing, contact formation constitutes the most demanding, frequent and conspicuous application of screen printing. Screens and pastes are the essential elements of this technology [68].

1. *Screens*: Screens are tight fabrics of synthetic or stainless steel wires stretched on an aluminum frame, as sketched in Figure 7.8. The screen is covered with a photosensitive emulsion, which is treated with photographic techniques in such a way that it is removed from the regions where printing is desired.

   For printing fine and thick layers, as is needed for the front contact of a solar cell, the wires must be very thin and closely spaced [73]. On the other hand, the opening of the reticule must be several times larger than the largest particle contained in the paste to be printed. Screens for solar cell production typically feature 200 wires per inch, wire diameter around 10 μm, mesh opening around 30 μm, corresponding to

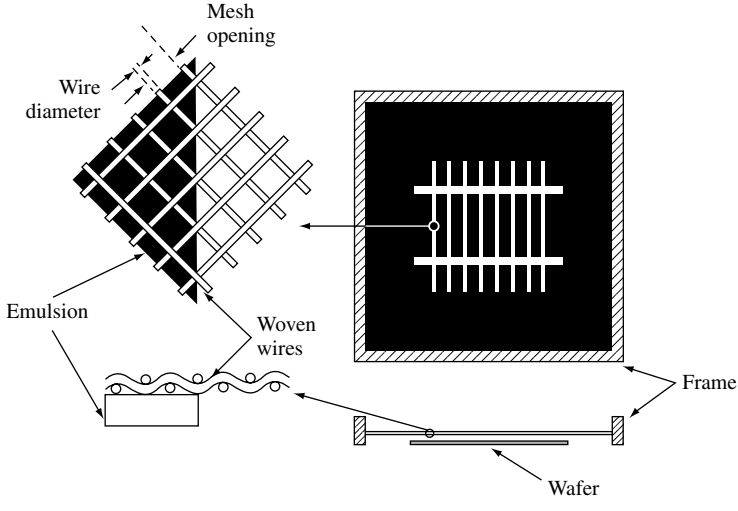


Figure 7.8 A screen for transferring the top contact pattern to a solar cell

nearly 50% open surface, that is, not intercepted by wires and a total thickness (woven wires plus emulsion) of around 100 μm.

2. *Pastes*: The pastes are the vehicles that carry the active material to the wafer surface. Their composition is formulated to optimize the behavior during printing. A paste for the metallic contacts of the solar cell is composed of the following:

   Organic solvents that provide the paste with the fluidity required for printing
   Organic binders that hold together the active powder before its thermal activation
   Conducting material, which is a powder of silver composed of crystallites of a size of tenths of microns; for the *p*-contact, aluminum is also present. This amounts to 60 to 80% in weight of the paste
   Glass frit, 5 to 10% in weight, a powder of different oxides (lead, bismuth, silicon etc.) with a low melting point and high reactivity at the process temperature, that enables movement of the silver grains and etches the silicon surface to allow intimate contact.

   The paste composition is extremely important for the success of the metallization and is critically linked to the heat treatment.

3. *Printing*: Figure 7.9 illustrates the process of printing a paste through the patterned emulsion on a screen. The screen and the wafer are not in contact, but a distance apart called the *snap-off*. After dispensing the paste, pressure is applied to the squeegee, which can be made of metal or rubber: this puts the screen in contact with the wafer. The squeegee is then moved from one side of the screen to the opposite one, dragging and pressing the paste in front of it. When an opening is reached, the paste fills it and sticks to the wafer, remaining there after the squeegee has passed and the screen has elastically retired.

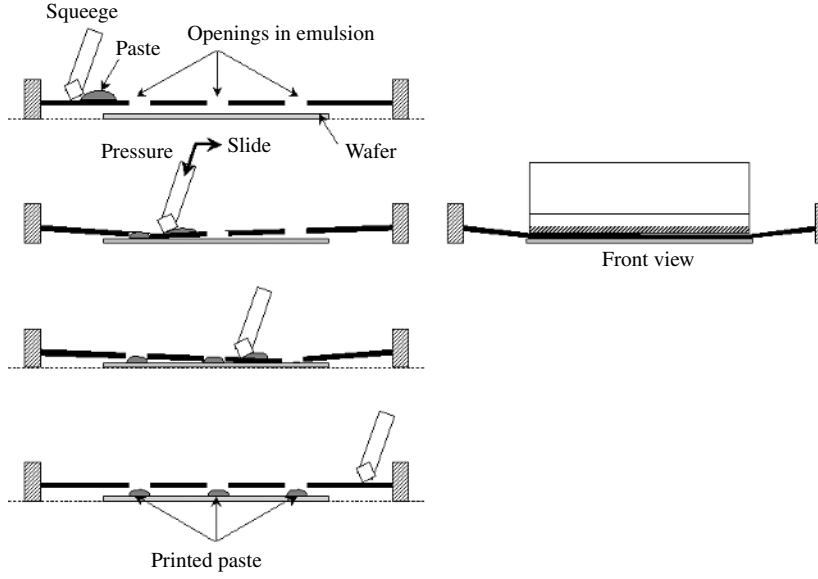


Figure 7.9 Illustration of a printing sequence

The amount of printed paste depends on the thickness of the screen material and the emulsion and the open area of the fabric. It also depends on the printed line width.

The viscous properties are of utmost relevance: when printing, the paste must be fluid enough to fill without voids all the volume allowed by the fabric and the emulsion, but after being printed it must not spread over the surface.

Critical parameters of this process are the pressure applied on the screen, the snap-off distance and the velocity of the squeegee.

4. *Drying*: Solvents are evaporated at 100 to 200°C right after printing so that the wafer can be manipulated without the printed pattern being damaged.

5. *Firing*: Firing of the pastes is usually done as a three-step process in an IR belt furnace. In the first step, when heating up, the organic compounds that bind the powder together are burnt in air. In the next step, the highest temperature between 600 and 800°C is reached and maintained for a few minutes. Higher temperatures are needed if an AR coating must be penetrated; crystal orientation and paste composition must be considered too. In the last step, the wafer is cooled down.

   The phenomena that take place during firing are very complex and not completely understood. The oxides forming the glass frit melt, enabling silver grains to sinter and form a continuous conductor so that the layer can present low sheet resistance. Neither the silver melting point nor the silicon–silver eutectic temperature is reached, sintering consisting of the intimate contact of solid silver crystallites. At the same time, the reactive molten glass etches some silicon and silver grains are allowed to form intimate contact with the substrate. The amount of etched silicon is on the order of 100 nm. When a layer of TiO_2 or SiN is present, the glass frit is able to etch through it. In fact, the quality of the contact improves because of a better homogeneity.

   The picture of the contact after cooling down shows two zones [74]. In the inner one, crystallites of silver are plugged into silicon forming crystalline interfaces and presumably very good electrical contact in a sort of "point contact". These grains are embedded in a compact amorphous glass. The outer zone is more porous and contains silver grains and glass frit: this porosity explains why the resistivity of silver paste is much higher than that of pure silver.

   Besides, the contact resistance of printed contacts is much higher than that of an evaporated contact to *n*-Si of the same doping. It seems that, although enough silver grains make good contact with silicon, not all them are connected to the grains in the outer layer; many remain isolated by the glass.

   When the paste, in the case of the back metallization, contains aluminum as well as silver, the Al-Si eutectic formed and recrystallized ensures a good contact. With dielectric layers the contact appears to be localized as well, and some beneficial role is attributed to the metal atoms in the frit [75].

6. *Limitations and trends in screen printing of contacts*: As explained in former sections, the high contact resistance and the etching action of the glass frit require the front emitters to be highly doped and not very thin if screen printing is used. Only improved paste formulation and processing can overcome this limitation.

   Narrow but thick fingers with good sheet conductance are also needed. Well-defined lines must be much wider than the pitch of the woven fabric; 60-μm lines seem achievable, with 100-μm ones being standard (see Figure 7.10). Incrementing the amount of transferred paste implies increasing the thickness of the emulsion or the

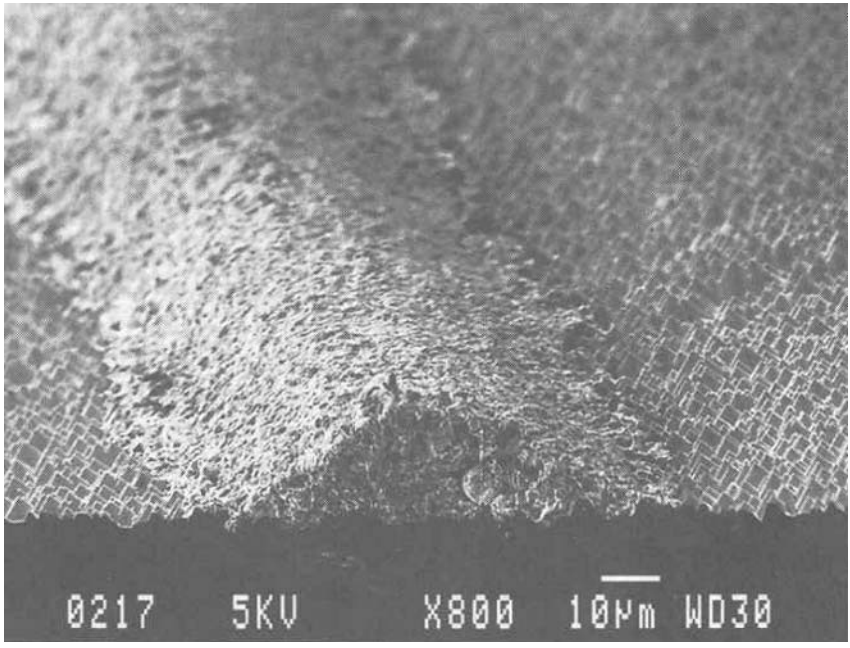


Figure 7.10 Screen-printed contact finger; texture pyramids are also visible. (Reprinted from *Solar Energy Materials and Solar Cells*, **41/42**, Nijs J, Demesmaeker E, Szulfcik J, Poortmans J, Frisson L, De Clerq K, Ghannam M, Mertens R, Van Overstraeten R, "Recent improvements in the screen-printing technology and comparison with the buried contact technology by 2D-simulation", 101–107, (1997), with permission from Elsevier Science)

pitch-to-diameter ratio of the wires, which are both limited. Besides, screens become deformed with usage and a continuous deterioration of printed patterns is observed.

Metal stencils [76] can outperform screens: they produce finer lines with better aspect ratio, endure more printing operations without degradation and need less cleaning and maintenance.

In screen printing, the wafer is subjected to considerable pressure. This can pose a problem with very thin or irregular wafers, such as those obtained by sheet growth of silicon, which can break down. Metallization alternatives have been developed, some of which are used in industries. They will be presented in Section 7.7.

7.4.3 Throughput and Yield

Because of the rapidly growing demand, photovoltaic factories are quickly expanding their production volumes so that there is a strong driving force to increase the throughput of processes and equipment. Automation is being extensively applied to the fabrication of solar cells and in-line, continuous processing tends to displace batch steps: in the process outlined above, only chemical etches, tube diffusion and edge isolation are batch steps. Automation and large-scale production lead to reduced costs [77].

Most processes described above have been borrowed from the electronic industry: diffusion, plasma etching, and so on are standard in microelectronics, while screen printing

was extensively used by thick-film technology in hybrid circuits. The character of the industries being different, their requirements for equipment differ, and it is to be expected that substantial improvements of photovoltaics will take place, now that the business volume makes it attractive for equipment manufacturers to get involved in.

A modern fabrication line is capable of processing around 1000 wafers h^{-1}, that is, an operation in a cell takes 2 to 3 s. Of course, the slowest operation along the flow line will limit the overall throughput. In order to get an estimate of how this translates into yearly production, let us consider 10×10 cm^2 cells with 15% efficiency (1.5 Wp power per cell). If the line operates without interruption and all wafers are successfully processed, during one year it will produce

$$1.5 \text{ Wp/cell} \times 1000 \text{ cells/h} \times 24 \text{ h/day} \times 365 \text{ days/year} \cong 13 \text{ MWp/year}$$

This number has to be decreased by (1) the downtime of the equipment due to maintenance, repair, and so on and (2) the yield, that is, the percentage of defective or broken wafers. Allowing for both would give a throughput in the range of 5 to 10 MWp/year per production line with available, commercial equipment.

Yield is a most important parameter for cell production: it can be defined as the ratio of successful finished cells to starting wafers. Since PV technology is material-intensive, yield has a strong influence on cost. Breakage and poor electrical performance are the causes of low yield, which is, generally speaking, benefited by automation. In this respect, in-line quality control acquires a great relevance to quickly detect and amend problems affecting yield.

For a given time per operation per cell, the throughput increases if the power of the cell increases. This is achieved by increasing the cell's area and the efficiency, which also helps in decreasing the cost. The standard wafer size is shifting from 10×10 cm^2 to 12.5×12.5 cm^2 and 15×15 cm^2. Series resistance and the uniformity of the obtained layers (emitter, AR coating), that may compromise the electrical performance, become important issues. Besides, larger cells are more difficult to handle without breaking and the yield may be affected.

There is a lot of room for efficiency improvement of industrial solar cells and the processes to realize it are proved in the laboratory. The question is how to implement them in an industrial environment so that they are cost-effective.

7.5 VARIATIONS TO THE BASIC PROCESS

This section introduces some variations to the basic process described above that aims at improving the efficiency, the throughput or the cost. While some modifications are already in production, most of these improvements are still being developed at the laboratory.

7.5.1 Thin Wafers

Wafering and sheet-growth techniques improve and produce thinner substrates, with wafer thickness below 200 μm being envisaged for the near term [78]. When processing these thin cells, several relevant issues appear.

The probability of fracture of the wafer during handling increases, especially in conjunction with a larger size. Adequate handling tools must be designed. Some steps appear to be critical: for instance, in chemical baths convection can exert significant torque on the wafers. This issue is fostering the study of the mechanical properties of silicon [79, 80] and even the development of new crystallization procedures.

The behavior during heat treatments is modified due to a decreased thermal mass. On the other hand, wafers can more easily become bent. Processes need to be specifically optimized for thin cells [81].

Thin cells largely depend on surface passivation and optical confinement. If attained to reasonable degrees, efficiency improvement comes as a bonus for thin cells, but otherwise the performance is degraded. New optimal structures must be developed.

7.5.2 Back Surface Passivation

The enhancement of material quality and the decrease of wafer thickness will make it necessary to passivate the back surface. Several approaches are feasible to be incorporated to the basic screen-printing process [55, 82]:

- *Aluminum back surface field*: With the benefit of gettering action, a highly doped *p*-type region at the back can easily be formed by screen-printing aluminum paste on the entire surface followed by high-temperature alloying. Several manufacturers implement aluminum BSF in their production lines. It can be integrated in the process flow (1) before metallization, possibly at the same time as phosphorus diffusion, and (2) by printing the aluminum paste after the front contact print so that the alloy forms during paste firing, though in this case lower temperatures are possible leading to worse properties.

  In either case, a back, silver-based contact is still needed for solderability. Bending of the wafers is an issue for thin cells.
- *Boron back surface field*: Like phosphorus, boron can be diffused from solid sources, so that it can easily be integrated into the basic process. Though it would be very attractive to diffuse both phosphorus and boron during the same thermal step, it appears that the obtained profiles are far from optimum and that a two-step diffusion seems necessary.
- *Silicon nitride passivation*: The surface and bulk passivation properties of silicon nitride are explained below. This replaces AR coating deposition and does not alter the basic process, though the parasitic junction must not be allowed to form in this case. This structure, as well as boron BSF, is compatible with the bifacial operation of the solar cell.

7.5.3 Improvements to the Front Emitter

Quantitative improvements in both recombination currents and spectral response will be derived from front surface passivation only when better paste formulations and finer line prints allow more resistive emitters – thinner and/or less doped – to be used [83]. In that case, tube oxidation and silicon nitride deposition appear as good candidates for industrial use.

Selective emitters are being developed at the laboratory level for screen-printed solar cells. A number of techniques have been proposed [84] that are compatible with the screen-printing process; none of them is at present implemented in production lines:

- Two separate diffusions for metallized and unmetallized regions, the heavy diffusion being restricted to the regions to be metallized by a screen-printed mask.
- A homogeneous and thick emitter is diffused by conventional means; a screen-printed mask is applied to protect the regions to be metallized from the plasma etch that follows. In this way, in the unprotected regions the emitter is thinner and less doped.
- Self-aligned selective emitter by diffusion from a patterned solid dopant source: under the dopant source a highly doped emitter is formed, while a much lighter diffusion from the gas phase takes place at the uncovered regions.
- First a high sheet resistance emitter is formed to which self-doping pastes containing phosphorus as well as silver are applied. Firing is performed above the silver–silicon eutectic temperature, thus leading to the formation of an alloyed layer heavily doped with phosphorus [85].

Except the last one, all the techniques require some kind of pattern aligning to print the front contact fingers on the heavily doped regions. Automatic screen printers feature enough accuracy to perform this task.

Obviously, the unmetallized part of these emitters is sensitive to surface passivation, which must thus be implemented by oxidation or nitride deposition.

7.5.4 Rapid Thermal Processes

In conventional furnaces of the closed-tube or conveyor-belt types, not only are the wafers heated to the process temperature but also the equipment itself: chambers, substrates or boats and so on. This brings about (1) long heating–cooling times, due to the large thermal masses involved, (2) a high potential for contamination, since a lot of parts, some of them metallic, are held at a high temperature and (3) high-energy consumption.

On the other hand, the microelectronic industry has developed in the last years, so-called *rapid thermal processes* (RTP), whereby only the wafers, and not their environment, are heated up to high temperature. Selective heating is accomplished by intense UV illumination of the semiconductor. The interest of RTP for solar cell fabrication comes from very short thermal cycles down to a few minutes including heating and cooling, so that throughput can be boosted. Besides, the absence of hot parts in the equipment diminishes potential contamination and energy consumption.

At the laboratory scale rapid thermal diffusion of very thin emitters (which is beneficial from the electrical point of view) has been demonstrated. Rapid thermal firing of screen-printed contacts and aluminum alloying have also been successfully implemented, along with other promising techniques such as rapid thermal nitridation and oxidation of the surfaces for passivation purposes [86, 87]. It can be said that every thermal step in the solar cell process can be made by RTP.

A possible drawback of the technique is a degradation of substrate lifetime as compared to conventional processing of some materials, due to the formation and quenching-in

of defects because of the very fast heating and cooling cycles and possibly also due to precluded gettering action [88].

A hurdle to industrial deployment of RTP is the lack of suitable equipment, since Microelectronics uses one-wafer reactors while Photovoltaics would need large capacity batch reactors or, better, in-line continuous equipment. It seems possible to furnish conveyor-belt furnaces with UV lamps to obtain these industrial RTP reactors, but some problems such as temperature uniformity must be solved [89].

7.6 MULTICRYSTALLINE CELLS

It has already been pointed out that the peculiarities of mc cells may prevent, in some cases, the use of standard processing technologies. Some of the proposed alternatives are not yet so cost-effective as to be incorporated in an industrial production line, but others are finding their way. Two main differences with single-crystalline silicon can be highlighted:

- Mc-material quality is poorer because of crystalline defects (such as grain boundaries, dislocations, etc) and metallic impurities (dissolved or precipitated), giving lower bulk lifetimes and hence lower cell efficiencies. To address this problem, two main strategies are followed: implementation of gettering steps and defect passivation with hydrogen.
- Texturing is more difficult because of different exposed crystallographic planes, so that standard alkaline solutions are not appropriate. To improve light-trapping and absorption, other techniques have to be implemented.

7.6.1 Gettering in mc Solar Cells

As already explained, gettering processes are also used in monocrystalline Si processing, but in the case of mc-Si they are even more important to improve material quality. P and Al gettering steps are routinely integrated in mc solar cell processing. Gettering conditions (temperature, process duration etc) differ from those of single crystal, because of the interaction among metal impurities, crystalline defects and other impurities present in mc-materials (mainly O and C).

It has been realized that gettering efficiency is strongly material dependent [90, 91]. This is explained by the fact that different techniques to grow mc-Si ingots produce wafers with different number and distribution of defects. Differences are even found in regions of the same ingot [92].

Additionally, a single mc wafer may exhibit nonuniform properties, both areal and in-depth, so that response to a gettering process can be inhomogeneous, affecting the final electrical performance of the solar cell [93, 94].

7.6.2 Passivation with Hydrogen

Silicon nitride is widely used as masking film in microelectronics [95]. For solar cells, it presents the advantage of performing as an effective antireflection coating. Films can

be deposited by several techniques, but the most commonly used process is chemical vapor deposition (CVD), involving the reaction of silane gas and ammonia. Plasma-Enhanced Chemical Vapor Deposition (PECVD) is preferred to other CVD technologies (atmospheric pressure CVD or low pressure CVD) because it is a low temperature process ($T < 500^{\circ}C$), and this means reducing complexity and preventing lifetime degradation.

But the most outstanding property of PECVD for mc-material is that it produces hydrogenation, and its benefits for silicon are well known [96, 97]. Atomic H interacts with impurities and defects in the bulk of Si, neutralizing their recombination properties to a certain extent, a phenomenon that is usually expressed as "bulk passivation". In the case of PECVD, amorphous silicon nitride films are produced with up to 40 atomic % of hydrogen (i.e. although these films are usually referred to as SiN_x they are really a-SiN_x:H). A subsequent thermal step is needed to activate hydrogenation, and in an industrial process the metal firing step fulfills this objective [98].

Additionally, surface passivation due to SiN_x deposition by PECVD has also been reported [99]. Achievable surface recombination velocity on a phosphorus-doped emitter is similar to that of a high-quality oxide passivated one, and a value as low as 4 $cm\,s^{-1}$ has been obtained on a polished 1.5 Ω·cm FZ p-type silicon wafer [100].

These three different properties (AR coating, bulk passivation and surface passivation) cannot be varied independently, an optimization of processing parameters (temperature, plasma excitation power and frequency, gas flow rate) is necessary, and a compromise should be reached [101, 102]. Furthermore, there are different PECVD techniques giving different results.

The state of the art of the industrial PECVD equipments today is the "direct" PECVD, schematized in Figure 7.11(a). The processing gasses are excited by means of an electromagnetic field, and the wafers are located within the plasma. Bulk is effectively passivated, but surface damage is sustained due to direct exposure of wafers to plasma, precluding the achievement of good surface passivation. Furthermore, surface passivation degrades with exposition to UV light.

There is a high frequency direct PECVD (13.56 MHz) and a low frequency one (in the range of 10–500 kHz), the former being better in terms of surface passivation and UV stability. On the other hand, it is more difficult to obtain uniform layers.

A different approach is the "remote" PECVD, where wafers are located outside the region in which the plasma is formed. Surface damage is avoided in this way, so that

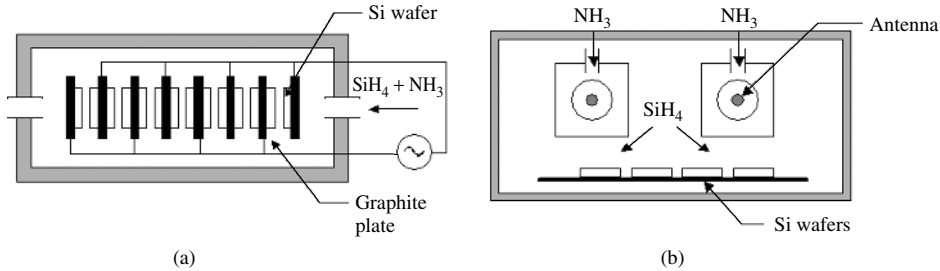


Figure 7.11 Industrial PECVD reactors: (a) direct-plasma reactor; and (b) remote-plasma system

better surface passivation is achieved. On the other hand, bulk passivation is reduced. This technique has been developed at the laboratory level in the last decade, and is currently being introduced into the industry. Figure 7.11(b) shows a sketch of an industrial remote PECVD. It implements a continuous feed of wafers, an advantage that should be compared to the batch-type direct PECVD.

7.6.3 Optical Confinement

Anisotropic texture with alkaline solutions (NaOH or KOH), standard in single crystal solar cells, is also applied to multicrystalline wafers, but with much poorer results, which is one of the reasons for their reduced performance. Reflectance of the textured wafers is relatively high because for randomly oriented grains the etch rate is not the same as that of (100) crystals. Another drawback is the existence of steps between grains, which may cause interruption in the screen-printed metal contacts.

That is why new alternatives are being considered. Their evaluation should take into account not only gains in reflectivity, but also surface damage and compatibility with metallization. In any case, the potential of some of these have been proved, and they are now being developed for industrial applications. Others need more research. The surface features produced by some of these are comparable in size or smaller than the wavelength, and geometrical optics is no longer applicable. They act as diffraction gratings, as scattering media or, in the limit of very small feature size, as graded index layers.

7.6.3.1 Chemical texturing

Several chemical techniques have been proposed. Some of them result in an inverted pyramid structure, but need photolithography patterning, which is a serious drawback for compatibility with the industry [103]. The result of nearly 20% for a mc-Si solar cell relies on an oxide-forced acidic texturing scheme [104]. A simpler approach is based on isotropic etching with an acidic solution containing nitric acid, hydrofluoric acid and some additives. The resulting etch pits of 1–10 μm in diameter are uniformly distributed, giving a homogeneous reflectance over the surface of the wafer and the absence of steps between grains (see Figure 7.12). An increase of short-circuit current of about 1 $mA \cdot cm^{-2}$ is reported for solar cells processed on isotropic textured wafers when compared to cells processed on anisotropic textured wafers [105]. Some technical difficulties, such as depletion of the solution and exothermic effects, can be encountered to come to an industrially compatible processing step. An automatic wet-bench, with temperature control of the etching solution and automatic replenishment of chemicals, has been designed recently.

Reduction in reflection, by forming porous silicon, is also being developed [106]. A detailed analysis taking into account the sum of reflectance and absorption within the porous Si layer shows an optimum of about 5 to 6% total optical loss. Besides its potential, the compatibility of the porous Si formation with screen-printed contacts still needs to be addressed.

7.6.3.2 Mechanical texturing

V-grooves about 50-μm deep can be formed in Si wafers by mechanical abrasion using conventional dicing saws and beveled blades, followed by an alkaline etching to reduce

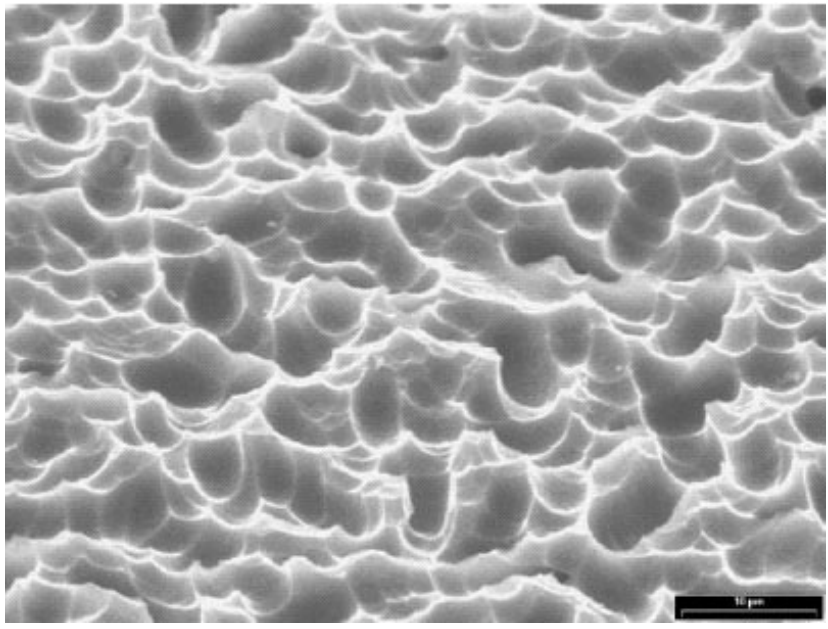


Figure 7.12 Mc-Si surface after acid etching. (Reprinted from *Solar Energy Materials and Solar Cells*, **74**, Szulfcik J, Duerinckx F, Horzel J, Van Kerschaver E, Dekkers H, De Wolf S, Choulat P, Allebe C and Nijs J, "High-efficiency low-cost integral screen-printing multicrystalline silicon solar cells", 155–164, (2002), with permission from Elsevier Science)

surface damage. With this technique, efficiency gains of 5% (relative) after encapsulation have been reached [107]. Contact fingers should be screen printed parallel to the grooves, on plateaus left untextured to ensure easy printing, so that some kind of alignment is maintained. Other contacting alternatives can be implemented, such as roller printing [108] or buried contact [109]. Currently, automated systems are being developed to check industrial feasibility.

Another approach is scribing grooves by laser [110]. Upright pyramids of 7-μm height can be created by two orthogonal sets of parallel grooves, followed by a chemical etch to remove the silicon residues. Combined with a single layer ARC, laser texturing can reduce weighted reflectivity to 4%, half of that given by anisotropic etching and the same AR coating. Adjustments have been made to obtain smoother and smaller grooves, in order to adapt the technique to a screen-printed process.

7.6.3.3 Reactive ion etching (RIE)

Reactive ion etching (RIE) texturization of silicon in chlorine plasma is a dry isotropic etching process that creates a surface with a high density of steep etching pits, with typical dimensions below 1 μm (see Figure 7.13) [111]. Increases of up to 1.4 $mA \cdot cm^{-2}$ in short-circuit current compared to anisotropic texture have been reported with a maskless technique [112]. RIE can also be performed in conjunction with a masking layer to produce more regular features [113]. The main obstacle in industrial implementation is too

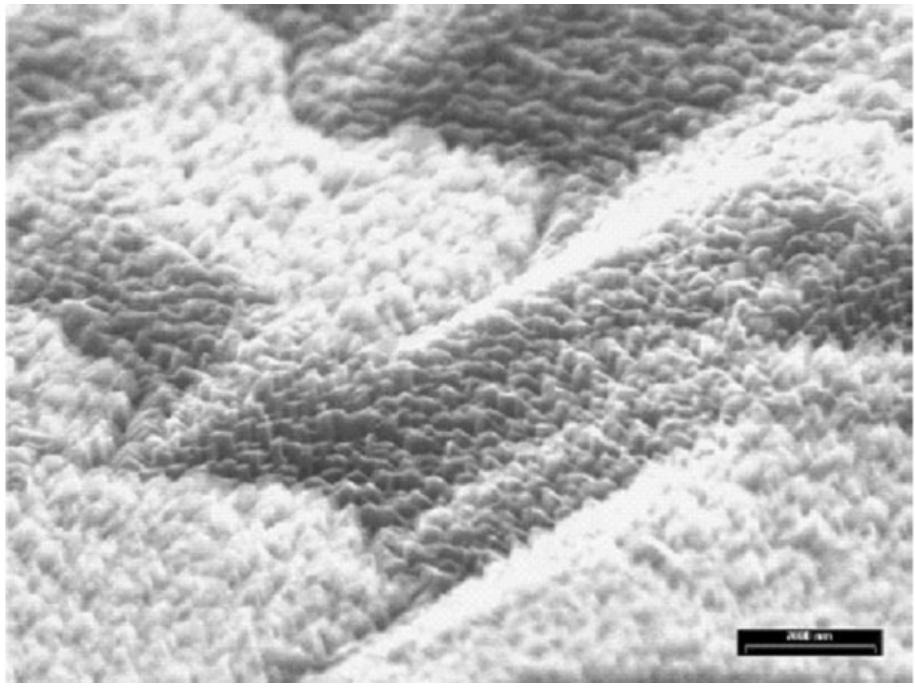


Figure 7.13 Mc-Si surface after RIE. (Reprinted from *Solar Energy Materials and Solar Cells*, **74**, Szulfcik J, Duerinckx F, Horzel J, Van Kerschaver E, Dekkers H, De Wolf S, Choulat P, Allebe C and Nijs J, "High-efficiency low-cost integral screen-printing multicrystalline silicon solar cells", 155–164, (2002), with permission from Elsevier Science)

low process throughput. Alternatives to the use of toxic and corrosive Cl_2 are also being investigated [114].

7.6.3.4 AR coating and encapsulation

It has to be taken into account that cell reflection properties differ from those of texturing because it is usually complemented by AR coating (typically, by atmospheric pressure CVD deposition of TiO_2 or TiO_2/SnO_2 or by PECVD of SiN_x), and cell encapsulation, so that the relative difference between several texturing methods normally reduces, as can be noticed in Table 7.4.

Table 7.4 Comparison of weighted AM1.5 reflectivities for mc-Si wafers with several surface treatments [115]

Reflectivity [%]	Alkaline textured	Acidic textured	Maskless RIE
Bare	34.4	27.6	11.0
With SiN AR coating	9.0	8.0	3.9
SiN & encapsulated	12.9	9.2	7.6

7.7 OTHER INDUSTRIAL APPROACHES

Other commercially available technologies will be described in this section. They all look for a decrease in the \$ W^{-1} figure of merit, following different approaches:

- using ribbons, presented in Chapter 6, as substrates;
- implementing techniques that do not need high-temperature processes: HIT, based on a-Si/*x*-Si heterojunction emitter;
- substituting screen-printing metallization by a more efficient technique: LGBG, based on the buried contact concept;

These only cover a small fraction of the PV market today, but they all have big expansion plans for the next few years.

7.7.1 Silicon Ribbons

Ribbon technologies offer a cost advantage over crystalline silicon, thanks to the elimination of the slicing process. They cover at the moment around 5% of the PV market, Edge-defined-Film-fed Growth (EFG) being the most mature of them, while string ribbon (STR) and dendritic web (WEB) are also into industrial production.

A specific solar cell process is needed for ribbon substrates, to account for the high density of defects (dislocations, grain boundaries, impurities, etc). Al paste is usually printed to create a deep BSF and to benefit from gettering, and silicon nitride is deposited by PECVD for bulk defect passivation and anti-reflection coating.

For EFG solar cells, the uneven surface of the sheets precludes the use of screen-printing metallization, and back and front contact formation is done by pad-printing and direct writing (extrusion) of silver pastes and inks. Efficiencies exceeding 14% on an average have been produced in the manufacturing line, achieving more than 14.7% in some cases [116]. Further reduction of production costs is expected by the growth of large-diameter EFG cylinders, which reduce thermoelastic stresses and can result in thinner and more uniform wafers. Thin curved wafers will require new technology for solar cell processing.

In the case of STR, 14.7% efficiencies have been reported for a process including screen-printed contacts fired with RTP [117], and 50 and 100 W modules are commercially available [118]. Regarding dendritic web, an $n^+ np^+$ structure (phosphorus front diffusion and rear Al alloyed emitter) is implemented on a high-resistivity antimony-doped substrate. Because of the low substrate thickness (100 μm), it can benefit from the location of the *p-n* junction at the back, performing an effective front surface field, enabling a high diffusion length and immunity to light-induced degradation. Using only production-worthy, high-throughput processes, dendritic web cells have been fabricated with efficiencies of up to 14.2% [119].

7.7.2 Heterojunction with Intrinsic Thin Layer

A new structure called HIT has been developed recently, which makes use of the cheaper amorphous silicon (a-Si) technology, depositing a-Si layers on crystalline silicon by

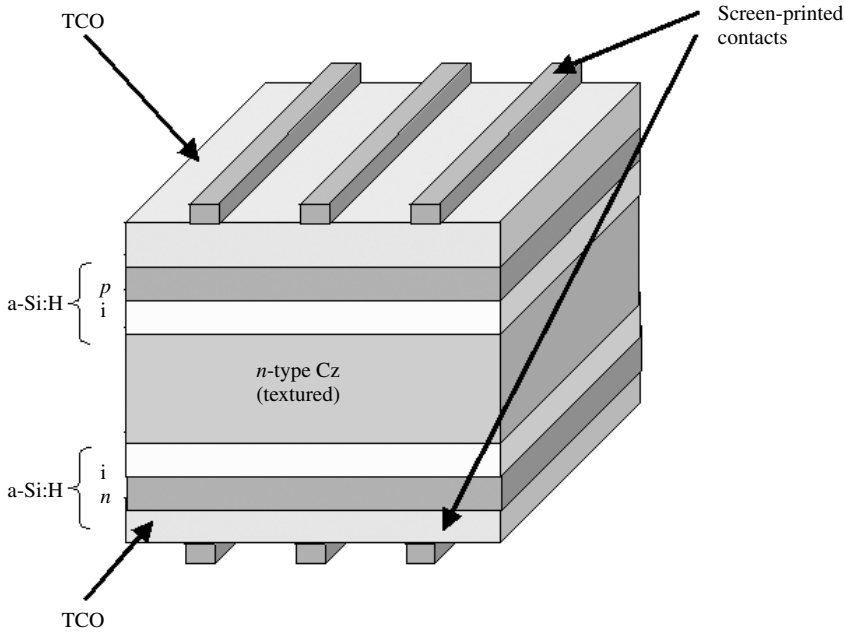


Figure 7.14 Structure of the HIT cell

PECVD [120]. It provides an excellent surface passivation with very low temperature processes (below 200°C), avoiding lifetime degradation of the bulk material. Figure 7.14 shows the structure of the HIT cell. A textured *n*-type Cz-Si substrate is used. The emitter and BSF are made of *p*-type and *n*-type a-Si layers, respectively. Very thin intrinsic a-Si layers are inserted between a-Si and the crystalline substrate, to improve the characteristics of the a-Si/c-Si interface. Thickness of these amorphous layers is on the order of 10 to 20 nm. On both doped layers, transparent conductive oxide (TCO) layers are formed, by sputtering, and metal fingers are screen printed. Back metallization is also comblike to reduce thermal and mechanical stresses, making the cell symmetrical and enabling it to perform as a bifacial cell.

In 1994, 20% efficiency was achieved with a similar HIT structure on a 1 cm^2 cell. Mass production of HIT cells started in 1997, with conversion efficiencies of 17.3% on 100 cm^2 substrates. 180 W modules are fabricated, and special modules exist for roof-tile and bifacial applications.

7.7.3 Buried Contact Technology

The buried contact solar cell process was developed at the University of New South Wales [50]. It is based on forming grooves in the silicon surface, where the metal is deposited by electroless plating, so that high aspect ratios and low metal shading losses are achieved. Several techniques have been proposed for groove formation, laser scribing being the most attractive for large-scale production. A metallized groove, typically 40-μm deep and 20-μm wide, is presented in Figure 7.15. Additionally, other high-efficiency

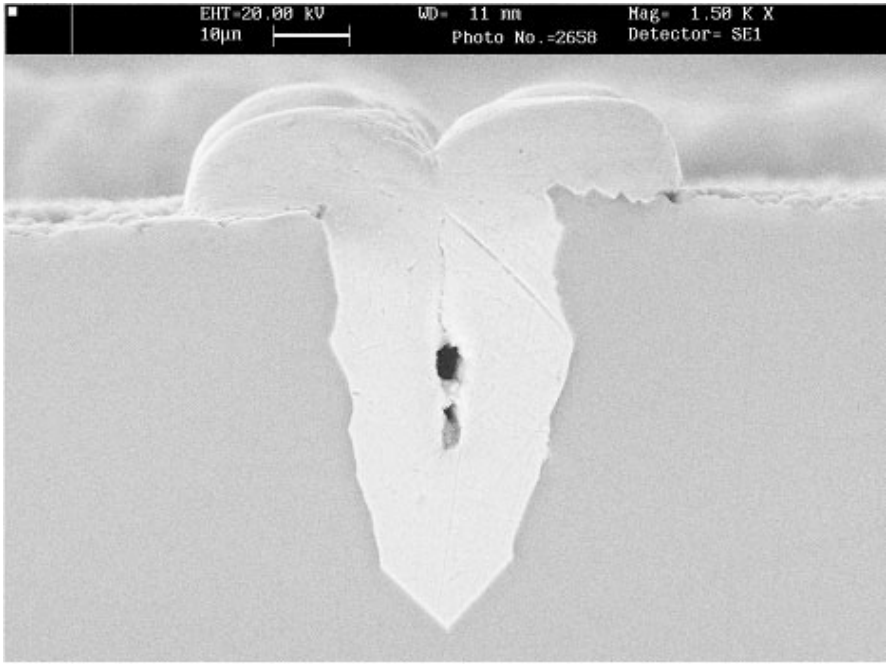


Figure 7.15 Cross-section of a buried contact. (Reprinted with permission from BP Solar)

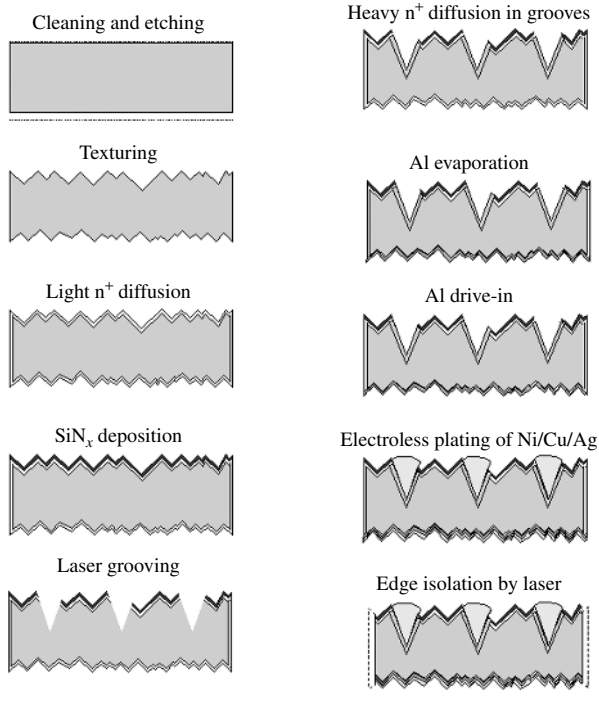


Figure 7.16 Laser-grooved buried-grid solar cell process

features are implemented, such as a selective emitter (highly doped under the metal fingers and low-doped and surface-passivated in the active area) and a Back Surface Field by Al evaporation and alloying, which also produces gettering effect.

The buried contact solar cell has been licensed to many manufacturers, but for the moment only one of them has implemented it at the industrial level, commercializing it as the LGBG solar cell. The LGBG process is sketched in Figure 7.16. Three high-temperature steps are needed, and a number of wet steps must be performed. A key element is the silicon nitride layer, which serves as a masking layer for heavy phosphorus diffusion and plating, and also performs as an antireflection coating and surface passivator. Efficiencies of 17% are routinely achieved with Cz-Si [121], and improvements are being researched and implemented to further increase cell efficiency [122].

The buried contact approach relies on compensating the increase in process complexity as compared to screen-printed technology with an increase in cell efficiency. A midway is proposed with a simplified buried contact solar cell process, with only one high-temperature step, TiO_2 antireflection coating and screen-printed Al BSF [123].

7.8 CRYSTALLINE SILICON PHOTOVOLTAIC MODULES

The power of a single solar cell being small, several of them must be electrically associated to make a practical generator. The module is the building unit for generators that can be purchased in the market, that is, it is the real PV product. Performance and lifetime of PV systems depend on the protection that module construction offers to the active photovoltaic devices.

The basic module fabrication procedure used by most manufacturers was developed three decades ago and is described below briefly. Modules for special applications (building integration, marine operation, etc) require slight modifications of the process and the materials.

7.8.1 Cell Matrix

In a module, the cells are usually arranged in series. After cell finishing, tinned copper ribbons (tabs) are soldered to the bus bars at the front (Figure 7.17a). It has to be noted that tabs must overlap a long distance along bus bar length since the conductance of the printed bus bars is too low. Conductive epoxies can replace conventional solder alloys and illumination used instead of iron heating.

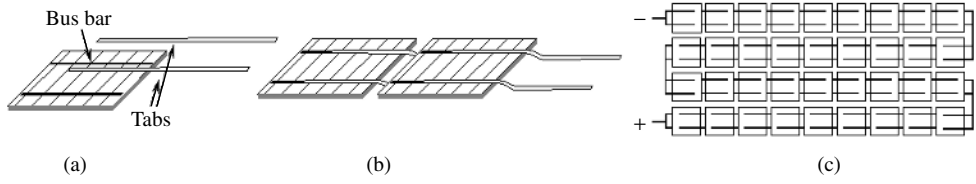


Figure 7.17 (a) Cell interconnection with tabs; (b) two cells in series; and (c) layout of 36 series-connected cells

Two tabs per cell are employed thus providing redundancy that allows current to flow in case electrical continuity is broken because of some failure [124]. Besides, the effective length of grid fingers is one-fourth the cell side and series resistance is alleviated. Tabs provide a nonrigid link between cells that allow thermal expansions to be accommodated.

Series interconnection of strings by soldering the tabs to the rear side of another cell follows (Figure 7.17b). The strings are interconnected with auxiliary tabs to form the cell matrix. This can consist of a single series string or several strings (Figure 7.17c). If the strings are not internally paralleled, their terminals are brought outside the module to permit flexible circuit configuration.

A common module configuration uses 36 series-connected cells, which, under operating conditions, would produce around 15 V at maximum power, appropriate for 12 V battery charging [125]. As building-integrated, grid-connected applications grow, modules with different electrical configurations enter the market.

A few years ago these operations were performed manually, but current factories use sophisticated equipment that performs most of the operations automatically. Both throughput and yield benefit from automation since the connected cells are very fragile and difficult to handle.

7.8.2 The Layers of the Module

The array of cells must be properly encapsulated for reliable outdoor operation for more than 20 years, paying attention to factors like rigidity to withstand mechanical loads, protection from weather agents and humidity, protection from impacts, electrical isolation for the safety of people and so on.

The different layers that the module is made up of are then stacked. A common structure is sketched in Figure 7.18.

A 2- to 3-mm thick soda lime glass is used as a superstrate that provides mechanical rigidity and protection to the module while allowing light through. It must have low iron content or otherwise the light transmission will be low. Modern modules use glass with cerium that absorbs UV radiation to enhance reliability [126]. Tempered glass must be employed to increase the resistance to impacts.

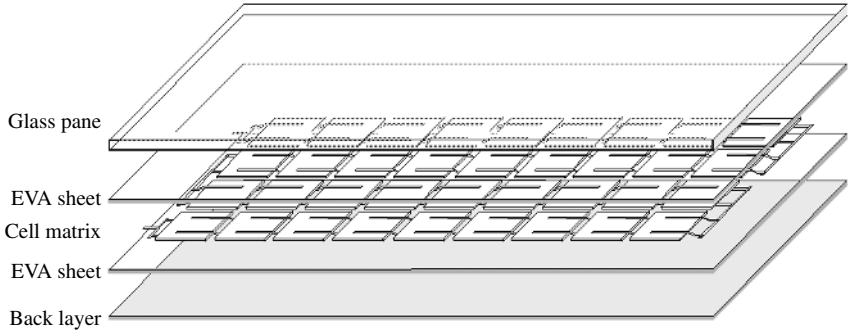


Figure 7.18 Stack of materials to be laminated

The cell matrix is sandwiched between two layers of the encapsulant or pottant material. The most popular encapsulant is the copolymer ethylene-vinyl-acetate (EVA), a plastic composed of long molecules with a backbone of carbon atoms with single covalent bonding. EVA is a thermoplastic, that is, shape changes made under heating are reversible. It is sold in rolls of extruded film around 0.5-mm thick. Along with the polymer, the film contains (1) curing agents and (2) stabilizers whose role will be described later.

The outer layer at the nonilluminated module side is usually a composite plastic sheet acting as a barrier for humidity and corroding species. Some manufacturers use another glass, which increases protection.

7.8.3 Lamination and Curing

These steps are carried out in a laminator, a table that can be heated and furnished with a cover that closes the edges tightly. The cover has an internal chamber and a diaphragm that separates this from the chamber containing the module. Both chambers can be independently evacuated: this configuration allows the module to be kept in a vacuum while mechanical pressure is exerted on it.

In the lamination stage, both chambers are evacuated while temperature is raised above the EVA melting point at around 120°C. Vacuum is important to extract air – to prevent voids from forming – and moisture and other gases. The EVA flows and embeds the cells. After a few minutes, with the module chamber still in vacuum, the upper chamber is filled with air so that the diaphragm presses the laminate. The temperature is increased to 150°C and the curing stage begins: the curing agents induce cross-linking of the EVA chains, that is, chemical bonds are formed transversely among the long molecules that before curing are only weakly linked to one another. The plastic then acquires elastomeric, rubberlike properties and indeed the curing step is analogous to the vulcanization of rubber. This stage takes up to 60 min for standard cure EVA [127]. After cooling down, the laminates are unloaded from the laminator.

Lamination used to be a bottleneck in the module fabrication process. To improve throughput several solutions have been followed by the industry: (1) commercial fast-curing EVA formulations allow drastic reductions of curing time to less than 10 min [128], (2) performing the curing step in a separate oven decreases the residence time in the laminator and (3) a large lamination area – up to several square meters – enables simultaneous process of several modules or very large ones.

Another polymeric material, poly vinyl butyral (PVB), was used in early times of module fabrication. It is processed in a similar way to EVA and can present some advantages over EVA [129] but it requires low temperature storing. For modules using two glass panes, resin fill-in is an alternative to EVA with reliability advantages. A sealed cavity is formed between the glass panes with the cells in-between and the liquid resin is poured into it. Care must be taken to ensure that no bubbles form [125]. Resins do not require heating to cure. Silicone resins are expensive but very stable and some modules for building integration use them. Yet curing can be inhibited by the module sealant so that they are difficult to handle. Acrylic resins with UV curing are being investigated.

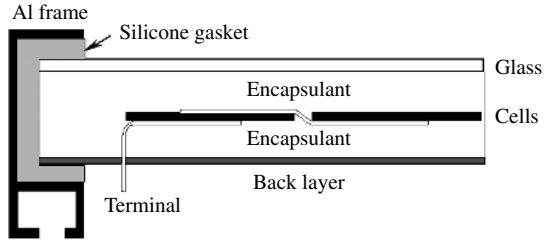


Figure 7.19 Cross-section of a standard module

7.8.4 Postlamination Steps

These include (1) trimming the edges of the laminate to remove spread-out encapsulant, (2) sealing them with silicone rubber to close this potential path of moisture penetration in the module, (3) sticking the plastic junction box at the back of the laminate and performing the connections and (4) when required, installing the anodized aluminum frame (Figure 7.19). The frame must be electrically insulated from the active cell circuit so that high-voltage differences can be sustained between the electrical terminals and the frame without current flow.

Besides, among other final tests, the $I-V$ curve of all modules under standard conditions is measured in a solar simulator to check if they fulfill specifications. Flash simulators are commonly utilized to save energy, with the electronic equipment able to record a complete $I-V$ curve in a fraction of a second. They must have a spectral content matched to the AM1.5 standard, or else, they must be calibrated with a calibrated cell of the same technology.

7.8.5 Special Modules

7.8.5.1 BIPV products

Building integration of PV modules (BIPV) has emerged as one of the most important – by volume – applications of Photovoltaics. Modules perform two tasks: as constructive materials as well as power generators. Modules can be incorporated to a building in a number of ways and special products are being developed so that the typical framed module is no longer the only PV product. Very large modules with special fixing for roof or façade integration, roof tiles with cells and semitransparent modules allowing light through are available. Visual appearance is enhanced by module shape, encapsulation and cell color [130]. Besides, these products must comply with building normative such as fire resistance.

7.8.5.2 Bifacial modules

Several cell structures have been presented that can operate with bifacial illumination. By encapsulation between two glass panes, bifacial modules offering increased power output per unit cell area can be produced without technology changes. In spite of their potential, their presence in the market is very small at the moment.

7.8.5.3 Modules with back contact cells

Several cell structures have been proposed that bring both contacts to the back face, which is usually accomplished by implementing phosphorus diffusions at both faces that are internally connected through processing. They fit the scheme in Figure 7.1(d) [131]. Back contact cells are interconnected without tabs by soldering them to a layer with the connection paths printed, similar to PCB practice in electronic circuits. These experimental designs offer simplified module fabrication and enhanced visual appeal.

7.9 ELECTRICAL AND OPTICAL PERFORMANCE OF MODULES

7.9.1 Electrical and Thermal Characteristics

The voltage of the module is, in principle, the number of series-connected cells times the voltage of the single cell, and the module current the number of paralleled cells times the single cell current. Whatever the combination, the module power equals the power of a single cell times the number of them. Mass-produced modules offered in the catalogues of manufacturers show power ratings that typically range from 50 to 200 Wp, delivered at current levels between 3 and 8 A and at voltages between 20 and 40 V. Lower and higher values are possible for special applications.

The manufacturer usually provides values of representative points (short-circuit, open-circuit and maximum power) of the module $I-V$ curve measured at standard cell conditions (STC), that is, 1 kW·m^{-2} irradiance (=0.1 W·cm^{-2}), AM1.5 spectral distribution and 25°C cell temperature. The maximum power of the module under STC is called the peak power and given in watts-peak (Wp). While efficiency has the greatest importance for a solar cell, for a module it has the less relevant meaning since part of the area is not occupied by the expensive solar cells.

The conditions in real operation are not the standard ones; instead, they vary strongly and influence the electrical performance of the cell, causing an efficiency loss with respect to the STC nominal value. This loss can be divided into four main categories [132]:

1. *Angular distribution of light*: Because of the movement of the sun and the diffuse components of the radiation, light does not fall perpendicular to the module, as is the case when measurements are done and the nominal efficiency is determined.
2. *Spectral content of light*: For the same power content, different spectra produce different cell photocurrents according to the spectral response. And the solar spectrum varies with the sun's position, weather and pollution and so on, and never exactly matches the AM1.5 standard.
3. *Irradiance level*: For a constant cell temperature, the efficiency of the module decreases with diminished irradiance levels. For irradiances near one sun, this is primarily due to the logarithmic dependence of open-circuit voltage on photocurrent; at very low illumination the efficiency loss is faster and less predictable.
4. *Cell temperature*: The ambient temperature changes and, because of the thermal insulation provided by the encapsulation, light makes cells in the module heat over it;

higher temperature means reduced performance. This is usually the most important performance loss.

But, prediction of the module response under different conditions is required to correctly assess the yearly production of a PV system in the field. The physical mechanisms of influence of temperature and irradiance on cell performance are well known, so that, in principle, prediction of module output could be rooted in physical models. This is however unpractical and would be a different approach if followed by PV system engineers.

Instead, very simple methods are used for translating the $I-V$ performance to different operating conditions and standardized procedures have been developed for PV modules of industrial technologies [133]. These methods are applicable within a limited range of temperature and irradiance conditions that are not very far from those met when testing the module and which require a small number of easily measurable parameters. The module datasheets from the manufacturers used to include some of these, allowing simplest estimates to be made, such as:

1. The steady-state power balance determines cell temperature: the input is the absorbed luminous power, which is partially converted into useful electrical output and the rest is dissipated into the surroundings. Convection is the main mechanism for heat dissipation in terrestrial, flat plate applications, and radiation is the second nonnegligible mechanism of heat dissipation. A common simplifying assumption is made that the cell-ambient temperature drop increases linearly with irradiance. The coefficient depends on module installation, wind speed, ambient humidity and so on, though a single value is used to characterize a module type. This information is contained in the Nominal Operating Cell Temperature (*NOCT*), which is defined as the cell temperature when the ambient temperature is 20°C, irradiance is 0.8 kW·m^{-2} and wind speed is 1 m·s^{-1}. *NOCT* values around 45°C are typical. For different irradiance values G, this will be obtained by

$$T_{\text{cell}} = T_{\text{ambient}} + G \times \frac{NOCT - 20^{\circ}\text{C}}{0.8\ \text{kW}\cdot\text{m}^{-2}}$$

2. The module short-circuit current is assumed strictly proportional to irradiance. It slightly increases with cell temperature (this stems from a decrease in band gap and an improvement of minority-carrier lifetimes). The coefficient α gives the relative current increment per degree centigrade. By combining both assumptions, the short-circuit current for arbitrary irradiance and cell temperature is calculated as

$$I_{\text{SC}}(T_{\text{cell}}, G) = I_{\text{SC}}(\text{STC}) \times \frac{G}{1\ \text{kW}\cdot\text{m}^{-2}} \times [1 + \alpha(T_{\text{cell}} - 25^{\circ}\text{C})]$$

   For crystalline Si, α is around 0.4% per degree centrigrade.

3. The open-circuit voltage strongly depends on temperature (the main influence is that of the intrinsic concentration), decreasing linearly with it. Knowledge of the coefficient, called β, allows the open-circuit voltage to be predicted by

$$V_{\text{OC}}(T_{\text{cell}}, G) = V_{\text{OC}}(\text{STC}) - \beta(T_{\text{cell}} - 25^{\circ}\text{C})$$

   The irradiance dependence is buried in T_{cell}. For crystalline Si, β is around 2 mV/°C per series-connected cell.

4. A lot of factors affect the variation of the maximum power (or, equivalently, the efficiency) with irradiance and temperature. The parameter γ is defined as the relative decrease in module efficiency per degree centigrade of cell temperature increase

$$\eta(T_{\text{cell}}, G) = \eta(\text{STC}) \times [1 - \gamma(T_{\text{cell}} - 25^{\circ}\text{C})]$$

Usual γ values are near 0.5% per degree centrigrade.

7.9.2 Fabrication Spread and Mismatch Losses

So-called mismatch losses arise when cells with different $I-V$ characteristics are interconnected because of the fewer degrees of freedom left to bias the devices, so that the array output is less than the sum of the powers that the individual cells could deliver. The differences come from the unavoidable fabrication spread or from nonuniform irradiance or working temperature within the array.

To minimize mismatch losses, finished cells are measured and sorted in the factory. For series connection, the important parameter is the current at the maximum power point (mpp). It is the common practice to measure the current before encapsulation at a fixed voltage close to the mpp and to classify the cells accordingly, though other classification criteria are possible [134]. Within each class all devices present similar currents within the specified tolerance that ensures that, when connected in series to form the module, the mismatch loss will be below the desired limit [135]. Depending on the class being processed, the power rating of the resulting module will vary and this explains why manufacturers offer different module families though they are built in exactly the same way.

7.9.3 Local Shading and Hot Spot Formation

Because of local shading or failure, one or several solar cells can present a much smaller short-circuit current than the rest of devices in the series string. If the defected cells are forced to pass a current higher than their generation capabilities, they become reverse-biased, even enter the breakdown regime, and sink power instead of sourcing it.

Figure 7.20 illustrates this behavior for an 18-cell string with one cell shaded so that its short-circuit current is half that of the remaining devices. String short-circuit is marked with a horizontal line, showing that in this condition the shaded cell is strongly reverse-biased and dissipates the power produced by the unshaded cells. This effect of course severely degrades the efficiency of the module, but more important is the fact that it can get damaged.

Avalanche breakdown is characterized by a nonuniform distribution of current across the junction, breakdown occurring preferentially at localized regions, possibly correlated to damage during processing. Intense local heating can produce very high temperatures (a hot spot). If a temperature of around 150°C is reached, the lamination material becomes degraded and the module irreversibly deteriorated [136, 137]. Because of the localized nature of the process solar cells show large scattering in their reverse characteristics so that the module behavior under partial shading is not accurately predictable.

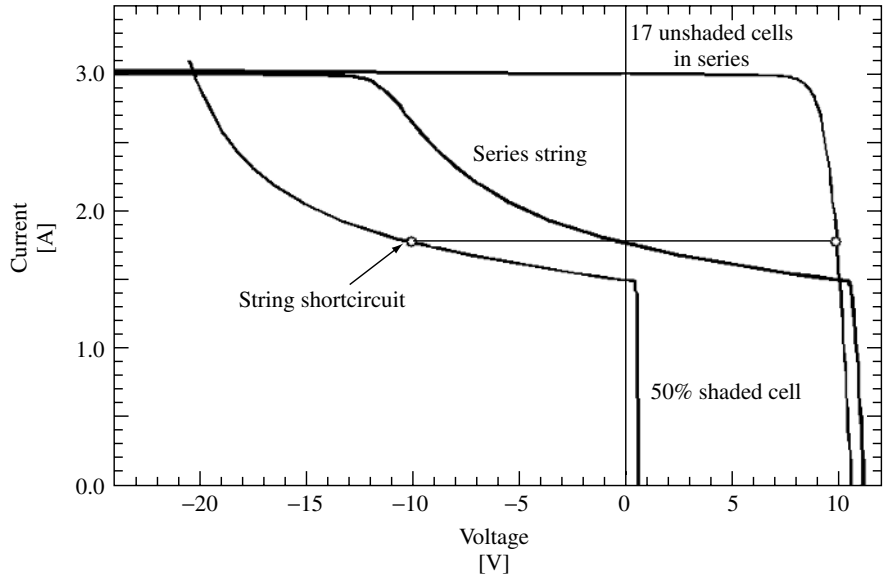


Figure 7.20 Computer simulation of the $I-V$ curves of a 50% shaded cell, showing the typical "soft" reverse breakdown, and of 17 identical cells, unshaded, in series. When series-connected with the shaded cell, the curve labeled "series string" is obtained

In order to devise the means of preventing hot spot failure from occurring, the worst case is considered. This occurs when the N-cell series string is short-circuited and a shaded solar cell is reverse-biased with the voltage of the remaining $N-1$ good devices, as shown in Figure 7.20. The minimum N that will lead to hot spot formation (i.e. the maximum N for safe operation) depends on rather uncontrollable factors, as explained. For Si solar cells of standard technology, it is around 15 to 20.

Since larger series strings are generally used, the approach followed is to put a diode (bypass diode) in parallel, but in opposite polarity, with a group cells. The number of cells in the group is chosen so that hot spots cannot be formed. When one or several cells are shaded, they are reverse-biased only to the point where the diode across the group starts forward conduction. The diode carries away the necessary current to keep the group near short-circuit.

Figure 7.21 illustrates the operation of the bypass diodes. When the current forced through the shaded substring is such that the reverse bias equals the diode threshold voltage, the bypass diode sinks all necessary current to keep the string at this biasing point thus preventing the power dissipated in the shaded cell to increase. It is also apparent that the bypass diode leads to a significant increase of output power allowing the module to keep delivering the power generated by the unaffected groups.

It is clear then that the smaller the number of cells per bypass diode, the lower the efficiency loss for a shading condition, but this means a higher cost and more complex fabrication. It has been proposed to integrate a bypass diode in each cell so that these effects will be minimized at the expense of more complicated cell processing [138].

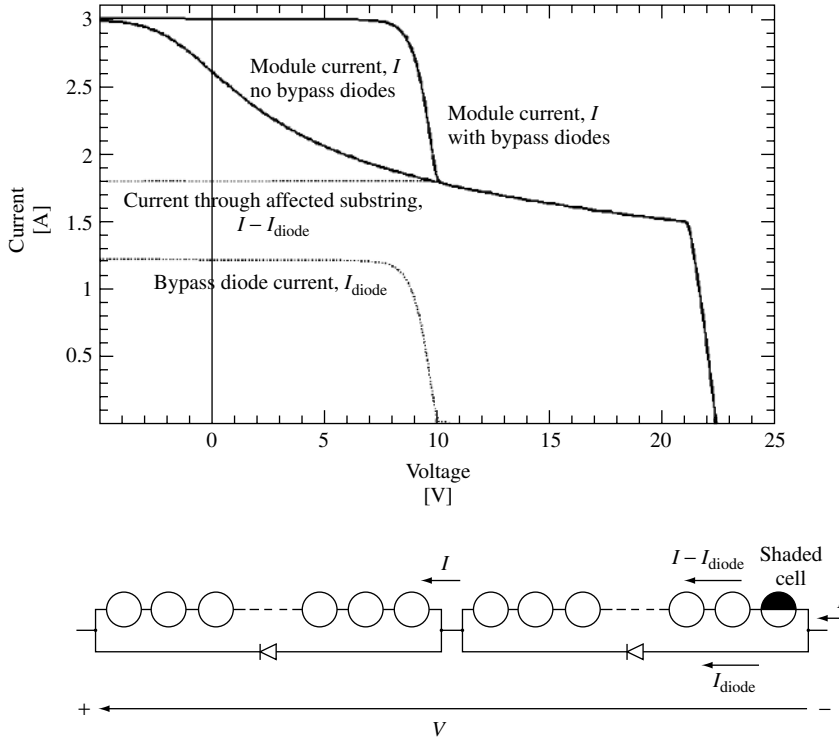


Figure 7.21 Computer simulation of the $I-V$ curves of a 36-cell series string without and with two bypass diodes, connected as shown in the bottom of the figure, when one cell is 50% shaded. The currents through the shaded substring and its bypass diode are also shown

The practice is to take electrical terminals outside the encapsulation not only for the extremes of the series string, but also for intermediate points as well, so that bypass diodes are connected in the junction box 12 or 18 cells each (Figure 7.22). Endurance to shading is a standard test for module qualification.

The influence of local shading on the module output depends on the details of the $I-V$ curve of the cells as well. Under certain circumstances of partial shading, it is beneficial that the cells show some shunt resistance. However, tight control of leakage currents by processing is not easy.

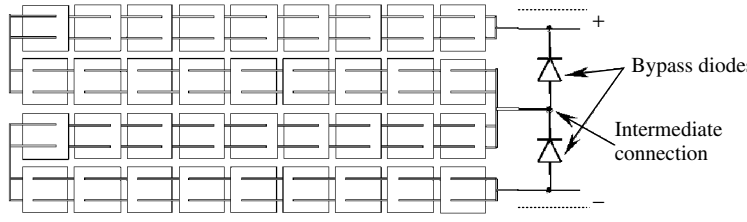


Figure 7.22 Two bypass diodes in a 36-cell module. The connections are done in the junction box

7.9.4 Optical Properties

The encapsulation affects the optical properties of the cells in several ways. The optical properties of the cells must be optimized attending to cost and performance after encapsulation.

Some effects of encapsulation are [139] as follows:

- The refraction index of glass and EVA is similar, around 1.5, between those of air and Si. Encapsulation acts, then, as a thick AR. For well textured Si solar cells, this antireflection action is enough and sometimes no thin ARC is used.
- The design of the ARC coating must account for the fact that the cell is illuminated from a medium with this index. The optimum ARC refractive index is larger than in air.
- Glass and EVA absorb some light in the short-wavelength range.
- Typically, 4% reflection occurs at the air–glass interface [Figure 7.23 (1)]. ARC coatings and texturing can be applied to decrease this loss.
- The light reflected by the metal fingers and the cell surface, if the reflected rays are tilted with respect to the normal to the glass surface, can be partly recovered by total internal reflection at the glass–glass interface [Figure 7.23 (2)]. This effect could be enhanced by texturing the cell surface with tilted pyramids, instead of the upright pyramids obtained by alkaline etching of (1 0 0) surfaces [140].
- Though the trapping capabilities of the cell, due to the lower difference in refractive index, appear to worsen with encapsulation, the escaped rays are trapped in the glass so that the absorption enhancement in the ideal case is not affected.
- For cells without a back metal mirror, the transmitted light can be recovered by putting a reflector, detached from the cell, at the back of the module [Figure 7.23 (3)]. The back plastic layer, if white, serves this purpose.
- The same white layer, since it reflects diffusively, allows some of the light incident between the cells to be collected [Figure 7.23 (4)].

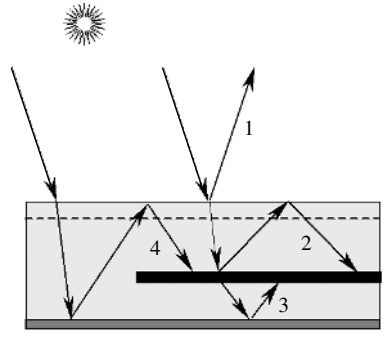


Figure 7.23 Optical effects of encapsulation: (1) glass reflection; (2) trapping of cell reflectance; (3) trapping of cell transmittance; (4) collection of peripheral light

7.10 FIELD PERFORMANCE OF MODULES

7.10.1 Lifetime

Long lifetime is claimed as one of the main virtues of PV and some manufacturers currently offer warranty for more than 20 years, with 30-year lifetime being the objective for short-term development. This should mean that for this period of time the module will keep working, that is, producing electrical power with an efficiency similar to the starting efficiency and without deterioration that compromises the safety or the visual appearance. Two factors determine lifetime: reliability, that refers to premature failure of the product, and durability, that attends to slow degradation that eventually decreases production to unacceptable levels. Cost effectiveness, energy payback balance and public acceptance of photovoltaic energy strongly rely on the reliability and the long lifetime of modules.

PV systems worldwide have been working for more than 20 years, and this allows us to gather information concerning degradation mechanisms. Modules in the field are subjected to static and dynamic mechanical loads, thermal cycling, radiation exposure, ambient humidity, hail impact, dirt accumulation, partial shading and so on. Common failure modes [124, 141] are related to the action of weather agents in combination with deficiencies in fabrication.

Location-dependent steady degradation of module output is also observed, with short-circuit current and fill factor being the most affected parameters. In many cases, this has been proved to correlate with degradation of EVA encapsulation [127]. EVA, like most polymers, is known to undergo photothermal degradation: UV radiation breaks molecular chains. Diffusion of chemical species is also relatively easy through it, so that moisture and corroding agents can enter while absorbers and stabilizers can out-diffuse.

Yellowing or browning of EVA reduces its optical transmission affecting module current. For this reason, EVA incorporates UV absorbers in its formulation. Cerium-containing glasses alleviate this problem. Degradation also decreases the strength of the encapsulant, leading to loss of adhesion to the cells and even detachment of the layer (delamination). This is promoted by the shear stress that accompanies different expansion coefficients upon diurnal thermal cycles. Delamination brings about optical and thermal degradation. Besides, the degraded encapsulant can be penetrated more easily by moisture and chemicals. Among these, sodium from the glass and phosphorus from the cell emitter are known to precipitate at the cell surface, corroding solder joints and increasing series resistance [141]. Encapsulant formulations are being continuously improved to address these problems.

7.10.2 Qualification

Several organisms, such as the International Electrotechnical Commission (IEC), the Institute of Electrical and Electronic Engineers (IEEE) and so on, have designed tests aimed at guaranteeing the quality of PV products [142]. Test procedures have been defined that, if successfully passed by a product, should guarantee the reliability of the PV module.

Manufacturers voluntarily submit their products for qualification tests in an accredited laboratory. These include verification of the module performance claimed in the datasheets as well as reliability tests. The certifications obtained are intended as a quality assurance for the customer.

Qualification tests consist in verifying the module integrity by visual inspection, measurement of the electrical performance at STC and of the electrical isolation before and after treatments that simulate, in an accelerated manner, real operation conditions. For instance, the IEC Standard 61 215 [143] specifies the following:

- Ultraviolet exposure using xenon lamps.
- Thermal cycling (-40°C to 50°C, 50 cycles) in climatization chamber.
- Humidity freeze cycling (thermal cycling with 85% relative humidity).
- Damp heat (1000 h at 85°C and 90% relative humidity).
- Twist test for testing resistance to torques.
- Pressure is applied to the module to test resistance to static mechanical loads.
- Hail impact test, where the module is stricken by 25 mm diameter ice balls at 23 m seg^{-1}.
- Outdoor exposure.
- Hot spot tests, where the module is selectively shaded.

Different test combinations are applied to a sample of a few modules. The modules will qualify if no major failures are found and the visual inspection reveals no damage, the electrical power is within 90% of specifications, and isolation is maintained.

7.11 CONCLUSIONS

This chapter has reviewed current state of crystalline silicon solar cells and modules. The main lines defining the structure of the described situation can be summarized as follows:

- *Changing scale*: The current booming of the markets enables and fosters technological and processing improvements.
- *Laboratory-industry gap*: There is a mature technology at the laboratory that has led to impressive performance levels, on the one hand, and a reliable, fast, 30-year-old industrial process producing modest efficiency, on the other hand. Closing this gap is the key to a lower \$ Wp^{-1} figure of merit.
- *Novel silicon materials*: Market growth and the threat of silicon shortage stimulates new materials and very thin substrates that demand new technological solutions.
- *Technology diversification*: These two challenges are to be faced by solar cell production technology in the coming years. Intensive preindustrial research is being conducted and solutions are being developed along several different lines.
- *Quality*: Product reliability and durability and environmental and aesthetical friendliness are as important as cost for the growth of PV industry and this also influences technology.
- *Long-term scenario*: Alternatives to crystalline silicon technology are being researched thoroughly and presumably some of them will succeed in reducing photovoltaic costs to competitive ones. Nevertheless, for these so-called "leapfrogs" to take place, a mature PV market should consolidate, for which silicon technology is essential at least for the next decade.

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