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Bulk Crystal Growth and Wafering for PV

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6.1 INTRODUCTION

The workhorse of the photovoltaics industry is silicon. More than four out of five amperes of solar-module produced current come from crystalline silicon modules. Of this amount, over 50% is produced by a steadily increasing share from multicrystalline silicon material.

Silicon solar cells first were made about 50 years ago from Czochralski (Cz)-pulled monocrystals with technology adapted from the microelectronics industry. Subsequently, world-record cell efficiencies have been achieved at a very high cost on a laboratory scale with Float Zone (FZ) monocrystals.

Cost pressures have forced the development of multicrystalline material solidification processes for production of very large silicon ingots (blocks), which have reached typical sizes of 250 kg in 2000. A good theoretical understanding of growth processes, together with numerical simulations of the entire process down to a microstructural defect level in the crystal today has resulted in the economical production of high-quality material. Sawing of silicon crystal into the thin wafers required for the best performance in solar cells wastes about 50% of expensive, pure silicon feedstock and is very costly. This has led to the development of several crystalline silicon foil, that is, ribbon production processes, and these are now in various stages of R&D and commercialization.

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6.2 BULK MONOCRYSTALLINE MATERIAL

The dominant issue of the photovoltaic industry is to fabricate solar cells in large volumes that are both highly efficient and cost-effective. An overall industrial goal is to significantly lower the costs per watt. The dominant absorber material used today for the majority of the commercially produced solar cells is the Czochralski-grown crystalline silicon (c-Si) in monocrystalline and block-cast material in multicrystalline form (mc-Si). Up to now, a lot of effort has been undertaken to increase the electrical efficiency of solar cells reproducibly towards and even above 20% [1], whereas much higher efficiencies were indeed claimed [2] but were most probably never reached [3]. Unfortunately, efficiency improvements are often reached only with the help of cost-intensive process steps so that most steps cannot be directly implemented into industrial products but have to be reengineered for low-enough cost. Hence, there still remains a significant efficiency gap between monocrystalline laboratory cells with efficiencies up to 24% and cost-effective, commercial Cz solar cells that are presently produced and sold in high volume at approximately 14 to 17% efficiency.

While some years ago the cost of a module was driven almost equally by the cost of the wafer (33%), the cell process (33%) and the module making (33%), this well-known ratio has changed significantly – both for C-Si and mc-Si. Today, in most products the wafer attributes to sometimes more than 50% (!) of the module cost, whereas the cell process and the module process attribute to the rest with similar portions of ~25%. The main reason for this is on one hand a steady cost reduction in the cell and module processes and on the other hand a significant increase in feedstock price together with an almost unchanged wafer thickness of 250 to 350 μm in production.

One way to meet today's demand of lower wafer cost is to (1) reduce the cost of crystal growth by improvement of productivity and material consumption at constant wafer quality, (2) reduce the cost of the wire-sawing process and (3) cut thinner wafers. While commercial Si solar cells still have a present wafer thickness of 250 to 350 μm for reasons of mechanical stability, a thickness of only 60 to 100 μm has been calculated to be the physical optimum thickness for silicon solar cells [4]. In this thickness regime the maximum theoretical efficiency for c-Si solar cells can be reached. In this optimum thickness regime, however, monocrystalline silicon becomes very fragile so that not only the electronic but also the mechanical properties of the wafer as well as the handling and processing techniques become of utmost importance for a good overall fabrication yield. Besides the mere mechanical wafer stability, manufacturing processes have to be adapted, redesigned or newly developed to avoid bending and breaking of ultra-thin wafers. With reduced wafer thickness, the necessity for surface passivation has to be taken into account. Since this cannot be done without adding to the cost, any added process step has to add adequate efficiency to remain cost-effective. Other important issues to get as much efficiency as possible out of the "valuable" wafer are improvements in anti-reflection (AR) coating, grid shadowing, "blue" response of the emitter and both surface and volume passivation.

The demand for high-quality polysilicon feedstock in the world market grew quickly not only in the microelectronic but also in the photovoltaic industry. In 1980 the worldwide production of single-crystal silicon amounted to approximately 2000 metric tons per year. This number was equivalent to ~100 000 silicon crystals every year

by either the Czochralski technique (80%) or the floating-zone technique (20%). The PV industry used both the high-quality tops and tails of the microelectronic crystals for less than 5$/kg to fit the feedstock demand and the depreciated Cz pullers of the "big brother" microelectronic industry. Since the microelectronic industry was and is still driven by continuously increasing ingot diameters, the "small" Cz machines became available for the PV-industry at interesting prices. During the last expansion phase of the microelectronic industry (1993–99), the PV industry had to struggle with a severe shortage of affordable feedstock. To reach the production volume, even pot scrap Si material had to be used. New and demanding techniques were developed in a hurry to separate the Si from the quartz crucible parts and to pre-select and pre-clean this material. Also, fine grain material had to be made usable. However, the annual world requirement for solar quality silicon in 2010 is estimated at 8000 to 10 000 metric tons for PV use, that is, the silicon demand will be roughly as high in volume as today's world production for microelectronics. A dedicated Si feedstock supply only for PV is therefore a necessity.

It can no longer be denied that the growing of silicon crystals has matured from an art into a scientific business. In today's PV-business, some of the bigger companies convert more than ~1 to 2 tons of silicon per day into solar grade Cz crystals and solar cells. Since PV has different main requirements for crystal growing from the microelectronic industry, the focus of machine and process development differ.

6.2.1 Cz Growth of Single-crystal Silicon

Solar cells made out of Czochralski (Cz)-grown crystals and wafers play – together with multicrystalline cells – a dominant part in today's PV industry. This is due to the following advantages.

Cz crystals can be grown from a wide variety of differently shaped and doped feedstock material. This enables the PV industry to buy cost-effective feedstock Si with sufficient quality even on spot markets. Since the feedstock is molten in a crucible, the shape, the grain size and the resistivity of the different feedstock materials can be mixed for the required specifications, although a given feedstock alone would fail. However, special care must be taken to avoid any macroscopic particles (SiO_2, SiC) that would not be dissolved in the melt especially when pot scrap material is used.

The Cz process acts as a purification step with respect to lifetime-limiting elements. The effective distribution coefficients of the most dominant lifetime-limiting metals (Fe, Ni, Au, Ti, Pt, Cr) are in the range of 10^{-5} or below. Together with appropriate gettering steps during cell processing, highly efficient commercial solar cells can even be made out of ingots grown from low-grade pot scrap material. The targeted iron equivalent concentration in the finished cell must be $<10^{12}$ atoms/cm^3 to achieve a minority carrier diffusion length well above ~150 μm.

The Cz process itself acts as a quality control step since proper crystallisation, that is, dislocation-free growth of an ingot, can only take place in a well-defined process window. The homogeneity of a well-grown solar grade Cz ingot for PV application is excellent with respect to the bandwidth of electronic and structural properties, whereas mc-Si block casting produces specifications with higher variances in most parameters. Cell

processes with Cz-Si can therefore use high-efficiency processes with smaller process windows that require well-defined starting material.

Cz technology is mature and cost-effective. Equipment and processes for semi-automated growing of crystals are commercially available so that several Cz pullers can be run by a single operator. Owing to the robust making of the machines, many Cz growers more than 20 years age are still in production.

The ingot can be pulled in a defined <100> orientation. This is a big economic advantage since the solar cell process can use this crystallographic property to homogeneously texture solar cells with a very cost-effective wet chemical etching step. By anisotropic etching, a surface structure with random pyramids is built that couples the incoming light very effectively into the solar cell. This effect together with the usually higher diffusion length of Cz crystals gives rise to the increased efficiency of Cz-Si solar cells compared to similarly processed mc-Si cells.

There exists a high potential for increasing the net pulling speed, that is, the productivity of a puller by a clever design of the hot zone, by sophisticated recharging concepts of Si in the hot crucible and by tuning the growth recipe to the optimum pull speed. Here the PV industry is in the novel position that it can neglect most specifications that are required in the microelectronic industry.

This is possible since the PV specifications are strongly reduced in the number of required parameters in contrast to microelectronic material. A PV specification "simply" focuses on the maximum productivity, a minority-carrier diffusion length of the material that should be exceeding the cell thickness and a shallow p-type doping that leads to a specific resistivity between 0.3 and 10 Ωcm, depending on the fabricated solar cell type.

One of the main disadvantages of Cz crystallisation of silicon is the fact that square cells are best suited to built a highly efficient solar module, whereas Cz ingots have a round cross section. In order to use both the crystal and the module area in the best manner, the ingots are usually cut into a pseudosquare cross section before they are cut into wafers. Additionally, the tops and tails of the ingots cannot be used for wafer production. The cropped and slapped materials, that is, tops and tails and so on, are then fed back into the growth process again.

The equipment and the basic principle for Cz pulling is shown in Figure 6.1. The Cz equipment consists of a vacuum chamber in which feedstock material, that is, polycrystalline silicon pieces or residues from single crystals, is melted in a crucible and a seed crystal is first dipped into the melt. Then the seed is slowly withdrawn vertically to the melt surface whereby the liquid crystallises at the seed. High vacuum conditions can be used as long as the melt weight is small (<1–2 kg), but with larger melts (often more than 30 kg) only pulling under argon inert gas stream is practicable. Owing to the reduced argon consumption, the argon pressure is set in the 5 to 50 mbar regime in the PV industry, whereas in the microelectronic industry, atmospheric pressure is also used.

After the silicon is completely molten, the temperature of the melt is stabilised to achieve the required temperature to lower the seed into the melt. The temperature must be chosen so that the seed is not growing in diameter (melt too cold) or decreasing in diameter (melt too hot). In PV the seed is usually <100>-oriented, is monocrystalline and

(a) (b)

Figure 6.1 Cz pullers in a PV-production environment (a) and growing Cz crystal (b) in a quartz crucible

is pulled upwards to grow a "crystal neck". Since dislocations propagate on (111) planes that are oblique in an <100>-oriented crystal, the dislocations grow out of the crystal neck after a couple of centimetres so that the rest of the crystal grows dislocation-free even if the growth was started from a dislocated seed. The dislocation-free state of the grown crystal manifests itself in the development of "ridges" on the crystal surface. If this state is achieved, the diameter of the crystal can be enlarged by slower pulling until it reaches the desired value. The transition region from the seed node to the cylindrical part of the crystal has more or less the shape of a cone and is therefore called the "seed cone". This cone can be pulled differently, either flat or steep.

Shortly before the desired diameter is reached, the pulling velocity is raised to the specific value at which the crystal grows with the required diameter. Owing to the seed rotation, the crystal cross section is mostly circular. In general, the pulling velocity during the growth of the cylindrical part is not kept constant, but is reduced towards the bottom end of the crystal. This is mainly caused by the increasing heat radiation from the crucible wall as the melt level sinks. The heat removal of the crystallisation thus becomes more difficult and more time is needed to grow a certain length of the crystal. Standard pull speeds in the body range from 0.5 to 1.2 mm/min. The diameter of the crystal in PV is often chosen between 100 and 150 mm. This is due to the short-circuit current of big solar cells where values of 6 A per cell are exceeded. It is difficult to provide a proper contacting scheme in screen print technology that can handle such high currents in the front contacts without high series-resistance losses. With even larger cell sizes, this effect becomes more problematic.

To complete the crystal growth free of dislocations, the crystal diameter has to be reduced gradually to a small size, whereby an end cone develops. For this purpose, the pulling speed is raised and the crystal diameter is decreased. If the diameter is small enough, the crystal can be separated from the melt without a dislocation forming in the cylindrical part of the crystal. The withdrawal of the crystal from the residual melt can be done with a rather high velocity, but not too fast, because thermal shock would cause plastic deformation called "slip" in the lower part of the crystal. The final crystal length is dependent on the crucible charge and varies between 40 and 150 cm.

Nowadays, the seed crystals used for Cz crystal growth are usually dislocation-free. However, each time the seed crystal is dipped into the melt, dislocations are generated by the temperature shock and by surface tension effects between the melt and the crystal. Normally these dislocations are propagated, or move into the growing crystal, particularly if the crystals have large diameters. The movement of dislocations is affected by cooling strain and faulty crystal growth.

The strain that occurs as a result of different cooling rates between the inner and the outer parts of the crystal is probably the main reason for the dislocation movement in the case of large crystals. At the usual <100>-crystal orientation, no (111) lattice plane, that is, no main glide plane, extends parallel to the crystal axis. All (111) glide planes are oblique to the crystal axis and as a result all dislocations that move only on one glide plane are conducted out of the crystal at some time. For movement in the pulling direction, the dislocations have to move downwards in a zigzag motion using at least two of the four different (111) glide planes. Dislocation-free crystal growth is relatively stable even for large crystal diameters, in spite of the higher cooling strain. This is so because it is difficult for a perfect crystal to generate a first dislocation. However, if a first dislocation has been formed, it can multiply and move into the crystal. In this way, numerous dislocations are generated and spread out into the crystal until the strain becomes too low for further movement of dislocations. Therefore, if a dislocation-free growing crystal is disturbed at one point, the whole cross section and a considerable part of the already-grown good crystal are inundated with backward-moving slip dislocations. The length of the slip-dislocated area is approximately equal to the diameter. Wafers and cells that show these types of dislocations can easily be hydrogen-passivated.

After losing the dislocation-free state, the crystal continues to grow with a high density of dislocations that usually are irregularly arranged. They are partly grown-in into the crystal and partly generated later by strain-induced processes. At high temperatures, climb processes take place that distort the dislocation array even more. This further increases the irregular shape and the distribution of the dislocations. In contrast to simple "slip" dislocations, these "grown-in" dislocations cannot be passivated well by a hydrogen-passivation step later in the solar cell processing. With crystal diameters above 30 mm, the monocrystalline but dislocated growth is not stable and in most cases changes to polycrystalline growth because of the tendency of a Si crystal to form twins in the presence of strain and dislocations. These twins also multiply and form higher-order twins and thus rapidly form a polycrystal. This fine-grained poly-Si material is not usable for solar cell production. Known causes for the generation of the critical first dislocation are either solid particles in the melt that move to the solidification front, gas bubbles that are trapped at the solidification front, impurities that exceed the solubility limit in the melt, vibrations of crystals and melt, thermal shocks or a too high cooling strain.

The growth of the seed cone is the most critical stage in the pulling of the Cz crystal. For productivity reasons very flat seed cones are preferable since the time for the making of the cone is not productive. However, the probability of introducing dislocations in the seed cone is lowest for tapered cones, although this means an increase in the pulling time by 15 to 25% for the same body length and additional loss in usable material. The loss of time and material gets worse for larger ingot diameters.

Owing to the reaction between the liquid Si and the quartz crucible, the crucible is of considerable importance to the growth. The silica of the crucible supplies considerable amounts of oxygen to the melt and, owing to the high purity of the silica, only small amounts of other impurities. However, the crucible tends to dissolve after a long-standing time so that the risk for particles in the melt from the crucible is increased with increased pulling time. The oxygen of the melt adds up to 10^{18} oxygen atoms/cm^3 to the growing crystal, whereas carbon is usually $<10^{17}$/cm^3 and has only little impact on the solar cell performance. Oxygen effects like thermal donors and precipitates can be well controlled in Cz cell processing.

6.2.2 Tri-crystalline Silicon

The mechanical properties of tri-crystalline silicon (tri-Si) allow slicing of ultra-thin wafers with higher mechanical yield than monocrystalline silicon (see [5, 6]). Tri-Si is a crystal compound consisting of three mutually tilted monocrystalline silicon grains [5, 6]. The crystal compound has a (110) surface orientation in all grains in contrast to the standard (100) orientation of wafers for today's solar cell production. While two of the grain boundaries in a tri-crystal are $\sum 3$ classified, that is, first-order twins, the third grain boundary is a $\sum 9$ structure, that is, a second-order twin. All boundaries are perpendicular to the (110) wafer plane and meet at the ingot centre forming a characteristic tri-star. Tri-Si growth is fully compatible with standard Cz monocrystalline growth, but it is faster. Using a tri-crystal seed that contains the complete generic information, tri-Si ingots of 100 to 150 mm diameter and up to 700 mm length are grown in standard commercial crystal pullers using optimised growth parameters for neck, crown and body (see Figure 6.2).

As the pulling axis is parallel to the common <110> orientation of all three grains, the dislocations often cannot be completely eliminated during necking, resulting in ingots that are not dislocation-free. The maximum local dislocation densities are about 105/cm^2 in the ingot top and about 107/cm^2 in the ingot bottom. The dislocations are often arranged

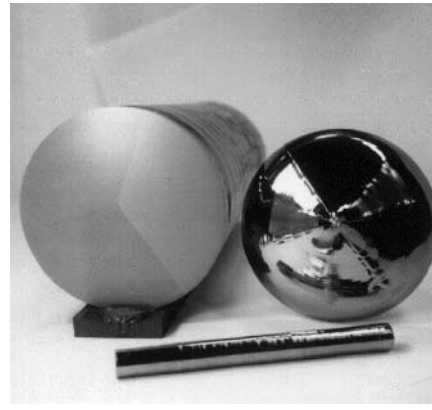


Figure 6.2 Tri-crystal seed (front), tri-crystal with cropped crown (left) and tri-crystal crown (right) with typical facets

in a streetlike geometry, while the dislocation density is significantly reduced in between the streets. However, despite the presence of dislocation from the very beginning (!), ingots of up to 700-mm length can be Cz-grown with multiple recharges at increased pull speed (see Figure 6.3). This is in fundamental contrast to the traditional c-Si growth with (100) orientation where dislocations must be completely avoided because otherwise the crystalline structure is totally lost after only a few centimetres of dislocated growth due to rapid dislocation multiplication. This peculiar structural stability of tri-Si, studied in detail through a geometrical stress model, is attributed to a reduction of cross slip in the tri-Si structure [7, 8].

Regarding electrical properties, ELYMAT mappings [9] show that there is a good spatial correlation between dislocation density and minority-carrier diffusion length: areas of high dislocation density show low diffusion length values. For dislocation lean ingots with 4- to 10-Ωcm resistivity, diffusion length values of more than 1000 μm (see Figure 6.4) can be obtained before light-induced degradation (LID).

The LID of the diffusion length of Cz-Si has recently been investigated extensively by several groups [1, 10, 11]. Although the identification of the defect structure is yet

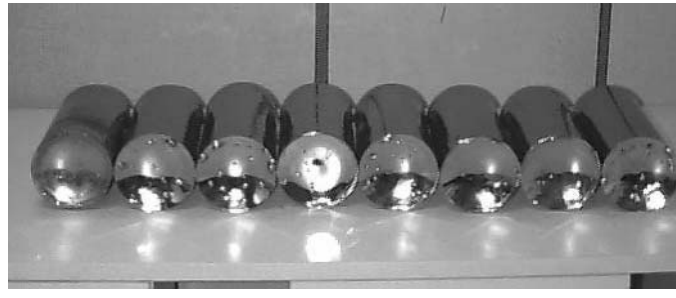


Figure 6.3 Tri-Si ingots (Ø140 mm) from quasi-continuous pulling

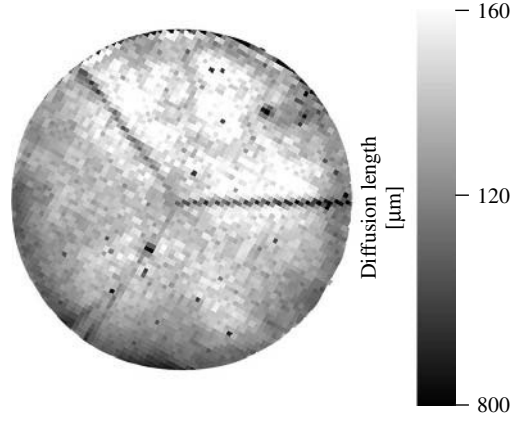


Figure 6.4 Diffusion length map of a 10-Ωcm as-grown wafer cut from the top of a dislocation lean tri-Si ingot. Lateral average diffusion length is 1300 μm

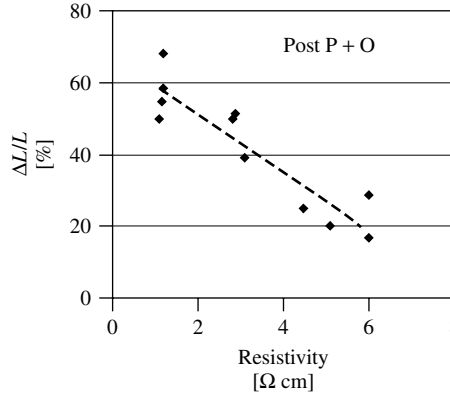


Figure 6.5 Relative degradation of diffusion length versus base resistivity for tri-crystalline silicon, measured after a standard P-diffusion and oxidation process

to be accomplished, a strong correlation of the effect with boron and oxygen is well established. Because tri-Si is grown with boron doping using standard Cz technology, an impact of LID on electrical quality is also present. Figure 6.5 shows a plot of the relative degradation as a function of base resistivity after a standard P-diffusion and oxidation process. Relative degradation values of less than 30% can be reached with 4- to 6-Ωcm material.

Tests on Si crystals fabricated from virgin poly-feedstock material with gallium, indium or aluminium as doping material have been performed to study LID. Best results have been obtained for Indium-doped material, for which the LID effect is reduced to almost below 3% of the diffusion length, which is within the accuracy limit of the ELYMAT measurements. With this material, light stable diffusion length values above 1 mm (!) can be achieved. This material is therefore best suited for high-efficiency cell processes.

In order to test the tri-Si material with standard solar cell processes, test cells are manufactured with a modified "Siemens Solar Boron Back Surface Field" (BSF) process with screen-printed contacts, as described in [12]. The final cell thickness was between 120 and 250 μm. A boron-BSF process was chosen since the BSF is crucial for high efficiency at reduced wafer thickness and beneficial for material with high diffusion length. SiN deposited with a commercial low pressure chemical vapour deposition (LP-CVD) method was applied as an AR coating, that is, no volume passivation can be expected since no molecular hydrogen was present during SiN deposition. In this case no complicated passivation or activation effects of hydrogen in Si must be taken into account [13–16]. In order to eliminate the effect of the different surface orientations and in order to focus on the pure material response, the wafers were *not* textured.

Table 6.1 shows that the efficiencies reach 15.5% in a lab-scale average. This efficiency compares well and slightly exceeds the results of corresponding solar cells from *solar-grade* <100> mono-material that was grown in standard production. The champion tri-Si cell efficiency without surface texturing was 15.9% using this cost-effective process.

Table 6.1 AM1.5 cell efficiencies for non-textured BSF cells on tri-Si and mono-Si substrates. Cell area is 103 × 103 mm^2 pseudo square

Material (non-textured)	Thickness average [μm]	Average efficiency [%]	V_{OC} [mV]	I_{SC} [mA/cm^2]	FF [%]	Rho [ohm cm]
Tri-Si	140	15.5	615	33.4	75.5	4
Mono-Si	200	15.2	612	32.7	76	1

6.3 BULK MULTICRYSTALLINE SILICON

Multicrystalline silicon besides monocrystalline silicon represents the basis of today's photovoltaic technology. Multicrystalline silicon offers advantages over monocrystalline silicon with respect to manufacturing costs and feedstock tolerance at, however, slightly reduced efficiencies. Another inherent advantage of multicrystalline silicon is the rectangular or square wafer shape yielding a better utilisation of the module area in comparison to the mostly round or pseudosquare monocrystalline wafers. The efficiencies of multicrystalline silicon solar cells are affected by recombination-active impurity atoms and extended defects such as grain boundaries and dislocations. A key issue in achieving high solar cell efficiencies is a perfect temperature profile of both ingot fabrication and solar cell processing in order to control the number and the electrical activity of extended defects. Moreover, the implementation of hydrogen-passivation steps in solar cell processing turned out to be of particular importance for multicrystalline silicon. With the introduction of modern hydrogen-passivation steps by Si_3N_4 layer deposition, the efficiencies of industrial multicrystalline silicon solar cells were boosted to the 14 to 15% efficiency range and consequently market shares were continuously shifted towards multicrystalline silicon as the standard material of photovoltaics.

6.3.1 Ingot Fabrication

Two different fabrication technologies for multicrystalline silicon, the Bridgman and the block-casting process (see illustrations in Figures 6.6 and 6.7) are employed. In both processes the solidification of high-quality multicrystalline silicon ingots with weights of 250 to 300 kg, dimensions of up to 70 × 70 cm^2 and heights of more than 30 cm have been successfully realised. While the Bridgman technology is a quite commonly used technique, the only two companies mainly employing the casting technology are Kyocera (Japan) and Deutsche Solar GmbH (Germany) [17, 18].

The main difference between both the techniques is that for the melting and crystallisation process only one crucible (Bridgman) is used, whereas for the crystallisation process a second crucible (block casting) is used.

In the case of the Bridgman process, a silicon nitride (Si_3N_4)-coated quartz crucible is usually employed for melting of the silicon raw material and subsequent solidification of the multicrystalline ingot. The Si_3N_4 coating thereby serves as an anti-sticking layer preventing the adhesion of the silicon ingot to the quartz crucible walls that owing to the volume expansion during crystallisation of the silicon material would inevitably lead to a destruction of both the silicon ingot and the crucible. Concerning the block-casting

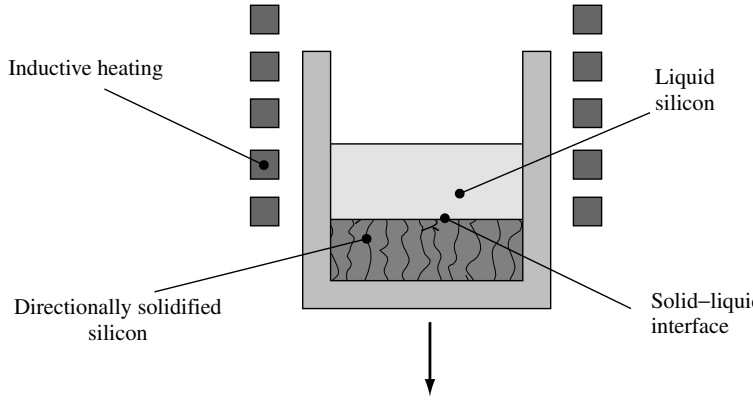


Figure 6.6 Conventional Bridgman technique that still is mainly used for the fabrication of multicrystalline ingots. Both melting and crystallisation of the silicon is performed in a Si_3N_4-coated quartz crucible. Crystallisation is realised by slowly moving downward the liquid silicon-containing crucible out of the inductively heated hot zone of the process chamber

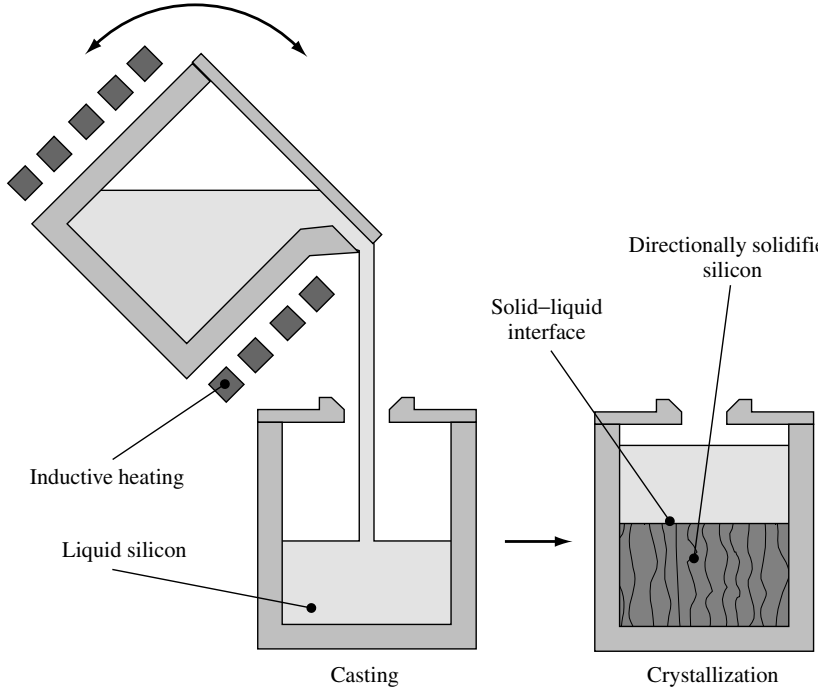


Figure 6.7 Block-casting process for the fabrication of multicrystalline silicon. After melting the silicon in a quartz pot, the silicon is poured into a second quartz crucible with a Si_3N_4 coating. The heating elements of the crystallisation crucible are not shown in the figure. In comparison with the Bridgman technique (see Figure 6.6), shorter crystallisation and cooling times can be realised by employing a more variable heater system

process, the melting is performed in a quartz crucible without a coating, whereas – after pouring the molten silicon into a second crucible – for the crystallisation also a Si_3N_4-coated one is used.

Usually, in both production technologies, crystallisation starts at the bottom of the crucible by lowering the temperature below the melting temperature (1410°C) of silicon. Within the Bridgman process the temperature reduction is achieved by simply descending the liquid silicon-containing crucible out of the hot area of the crystallisation furnace. Contrarily, the temperature control during the block-casting process is achieved by a corresponding adjustment of the heaters, whereas the crucible itself is not moved during solidification.

After solidification starts in the bottom region, the crystallisation front, that is, the liquid–solid interphase, moves in a vertical direction upwards through the crystallisation crucible. This so-called directional solidification results in a columnar crystal growth and consequently adjacent wafers fabricated out of the ingots show nearly identical defect structures (grain boundaries and dislocations).

Common crystallisation speeds used for the Bridgman technology are in a range of about 1 cm/h (corresponding to a weight of approximately 10 kg/h for large ingots). With regard to the increase in crystallisation speed, that is, productivity, mainly cooling of the already crystallised fraction of the ingot has to be taken into account. Too high process speeds cause large thermal gradients within the solidified silicon that may result in cracks or even destruction of the ingot. For the block-casting technology, however, owing to the more versatile and sophisticated heater system, considerably higher crystallisation speeds can be achieved [18].

6.3.2 Doping

Standard multicrystalline silicon is a boron-doped p-type material with a specific electrical resistivity of about 1 Ωcm, which corresponds to a boron concentration of about $2 \times 10^{16}/cm^3$. The specific resistivity is adjusted in a way such that optimal solar cell performance is guaranteed. Naturally, the boron concentration can be varied according to the requirements of specific solar cell processes. Specific resistivities in a range of 0.1 to 5 Ωcm have been used for solar cell fabrication so far. The boron concentration is normally adjusted by adding the equivalent amount of B_2O_3 to the silicon raw material prior to melting of the silicon. Considering alternative doping elements like gallium (p-type) or phosphorous (n-type) first, the segregation coefficient governing the resistivity decrease with increasing block height has to be considered. With a segregation coefficient of 0.8, boron nearly always is the optimal doping element giving only a small resistivity change over the silicon ingot (see Figure 6.8), whereas gallium and phosphorous with segregation coefficients of 0.008 and 0.35, respectively, are less favourable.

For phosphorous as an n-type dopant, additionally the disadvantage of a lower minority charge carrier (i.e. holes) mobility and a more complicated solar cell process using, for example, higher process temperatures for boron instead of phosphorous diffusion is encountered. However, recent results indicate that the activity of extended defects in n-type multicrystalline silicon is unexpectedly low, which could render n-type material nevertheless an attractive new feedstock source for photovoltaics.

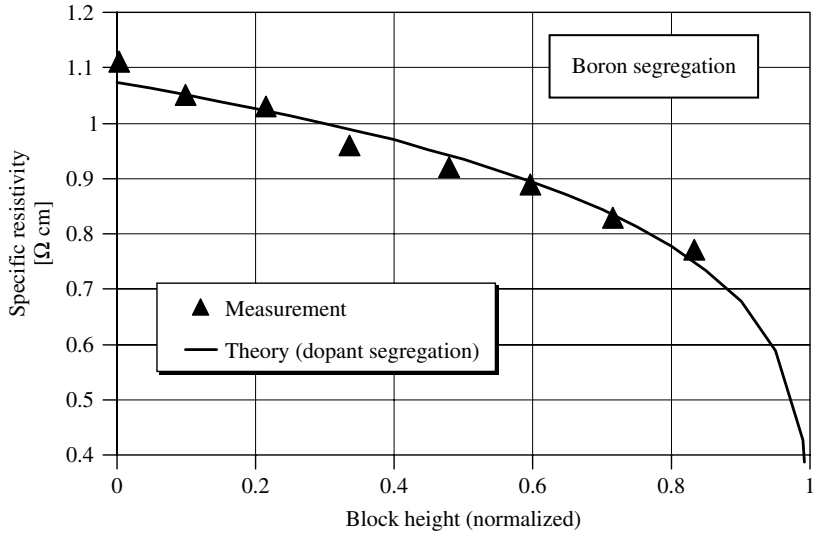


Figure 6.8 Decrease in the specific resistivity of *p*-type multicrystalline silicon due to segregation of the doping element boron

6.3.3 Crystal Defects

The main crystal defects in multicrystalline silicon are grain boundaries and dislocations. Concerning the attainable efficiencies of solar cells, not only the concentration of these defects but also their electrical activity is considered as crucial.

With respect to the grain boundaries and the grain size, basically smaller grains are observed at the beginning of the crystallisation process in the ingot bottom part. With increasing block height, individual grains prevail at the expense of surrounding grains and thus give rise to an increase in the mean grain size. This increase of grain size, however, depends on the crystallisation speed (see Figure 6.9). A higher crystallisation speed also means higher temperature gradients and thus an increased probability for the formation of crystal seeds in the melt that in turn lead to a limitation of the grain size. This is also the reason for faster crystallised block-cast material usually exhibiting smaller grains than conventional Bridgman-type multicrystalline silicon.

On the other hand, the grain sizes achieved with modern block-cast material are still large enough to not degrade solar cell efficiencies provided that the electrical activity of the grain boundaries is low enough. Grain boundaries and dislocations, if electrically charged, effectively attract minority charge carriers and consequently represent highly active recombination centres for photo-generated charge carriers. The electrical activity of grain boundaries and dislocations is determined by their impurity decoration (specifically by transition metals) and strongly increases with higher impurity concentrations.

Moreover, it was discovered that the shape of the crystallisation front during solidification also has considerable influence on the grain boundary activity [19]. Preserving a strictly planar solidification front clearly leads to a reduced grain boundary activity.

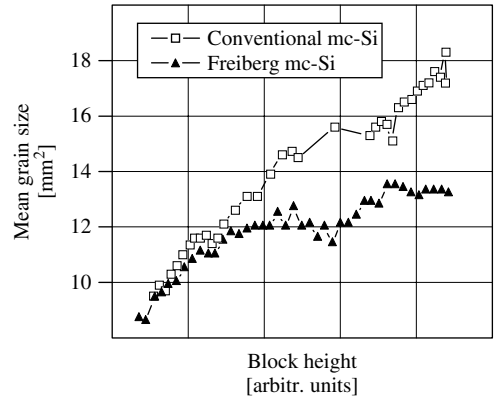


Figure 6.9 Mean grain size as a function of the block height for conventional Bridgman-type multicrystalline silicon (mc-Si) and the faster crystallised block-cast material from the Freiberg production facility of Deutsche Solar GmbH. Reduced crystallisation times lead to slightly lower grain sizes of the Freiberg mc-Si

Because also in modern high-throughput production processes a nearly perfectly planar solidification front is kept throughout the crystallisation process, grain boundaries show only weak electrical activities and therefore are generally considered as less important for solar cell efficiencies.

Crystal dislocations, however, turned out to be the most efficiency-relevant defects in multicrystalline silicon for solar cells. The dislocation density that is experimentally accessible by counting micrometer-small etch pits after appropriate chemical etching steps nearly shows a perfect correlation to the wafer lifetime and diffusion length (Figure 6.10) that are closely linked to solar cell performance. Dislocations are induced and multiplied

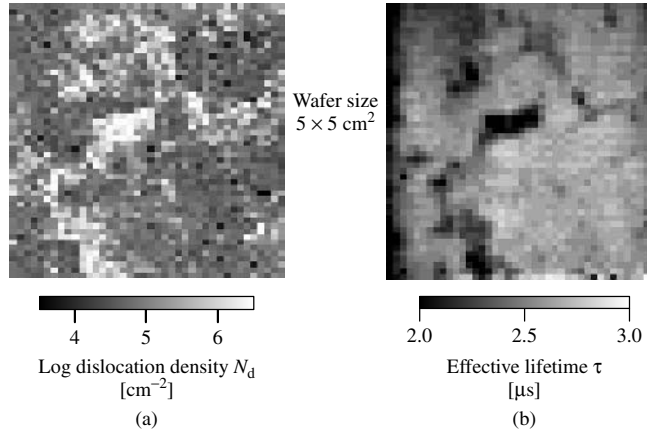


Figure 6.10 Topographies of the dislocation density N_d (a) and the effective lifetime τ_{eff} (b) of a typical multicrystalline silicon wafer showing the excellent correlation of both parameters. The effective lifetime measurements were conducted out without any surface passivation and thus are limited to less than approximately 3 μs by surface recombination processes

by thermal stress that is originated from temperature non-homogeneities during crystallisation and cooling of the ingot. The reduction of these temperature variations while keeping high process speed is therefore considered one of the most important issues for the further improvement of multicrystalline silicon.

An optimal process scenario for the production of multicrystalline silicon from both the crystal defect and the productivity point of view starts with a small crystallisation speed and minimal temperature gradients in order to secure a low-defect density bottom region of the ingot. After that, crystallisation speed should be largely increased for productivity reasons while keeping the solidification front planar and thermal gradients within the solidified silicon low.

6.3.4 Impurities

Despite boron being the standard dopant and thus an intentionally introduced impurity, even higher impurity concentrations in multicrystalline silicon are observed for both oxygen and carbon.

The interstitial oxygen concentration in multicrystalline silicon is affected by two processes, which are oxygen incorporation via the quartz crucible during melting and oxygen loss through evaporation of SiO, that is, the evaporating gaseous silicon monoxide that is stable at high temperatures only.

Because the segregation coefficient >1, the oxygen content decreases with increasing block height. Typical concentrations of the interstitial oxygen content of Bridgman and block-cast material are given in Table 6.2. Obviously, although the silicon melt never stays in direct contact with the quartz crucible, lower oxygen concentrations with Bridgman-type material compared to silicon from the block-casting process are not feasible. We therefore conclude that there also has to exist an oxygen release from the Si_3N_4 coating (containing some percentage of oxygen) into the silicon melt during the Bridgman process. In addition, we observe a much more rapid decrease of the oxygen concentration with increasing block height for block-cast material, which is attributed to the normally employed lower ambient pressure and enhanced gas exchange during this process.

Table 6.2 Typical concentrations of interstitial oxygen $[O_i]$ for block-cast material from the Freiberg production plant of Deutsche Solar GmbH and for typical material coming from a Bridgman process. For the determination of the oxygen concentration by Fourier Transform Infrared Spectroscopy (FTIR), a conversion factor of $2.45 \times 10^{17}/cm^2$ was used

Ingot position	Interstitial oxygen concentration $[O_i]$ $[10^{17}/cm^3]$	
	Block-casting process	Bridgman process
Bottom	6.5	6
Middle	0.9	3.5
Top	0.5	2

Although oxygen residing on interstitial lattice sites is not electrically active, recombination-active oxygen complexes such as thermal donors [20–22], new donors [23, 24] and oxygen precipitates may be formed after annealing steps, specifically in the high oxygen concentration bottom part of the ingot (see an example of the donor activity in Figure 6.11).

Specifically, thermal donors turned out to be mainly responsible for a broad low-lifetime region with a width of 4 to 5 cm in the bottom part of Bridgman-type ingots [25]. Owing to the instability of the thermal donors in high-temperature steps during solar cell processing, these low lifetimes, however, does not lead to low efficiencies. It is worth noting that the width of this low-lifetime region in the bottom part of the ingots is largely reduced for material from the block-casting process. The most likely explanation for this is the shorter process times that consequently give less time for the formation of oxygen complexes out of interstitial oxygen atoms.

Similar to metals, oxygen segregation at grain boundaries and dislocations enhances the recombination strength of these extended defects. Oxygen precipitates may also getter metal impurities during crystallisation, which are released afterwards during solar cell processing as highly recombination-active point defects.

Generally, the manifold involvement of oxygen in efficiency-relevant microscopic processes makes the reduction of the oxygen incorporation into multicrystalline silicon one of the most important targets of material improvement efforts.

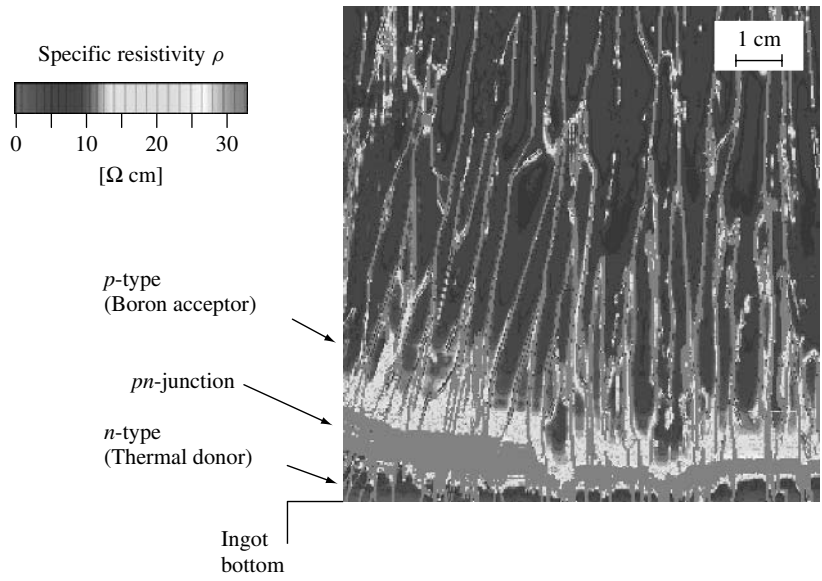


Figure 6.11 High resolution map of the specific resistivity (van-der-Pouw measurement technique) of a vertically cut wafer from a special high resistivity *p*-type multicrystalline silicon test ingot. Owing to the increased oxygen content, the formation of thermal oxygen donors changes the conductivity to *n*-type in the bottom part. The *pn*-junction can be identified by a remarkable increase in the specific resistivity

Like oxygen, carbon in multicrystalline silicon appears in concentrations considerably higher than those of the boron dopant concentrations. Typical concentrations of substitutional carbon are in the range of $2-6 \times 10^{17}/cm^3$ generally increasing with increasing block height. The incorporation of carbon into the silicon melt takes place via gaseous CO formation inside the crystallisation chamber by SiO chemically reacting with the graphite heaters. The main problem that is caused by an increased carbon concentration is the formation of needle-shaped SiC crystals (often associated with oxygen and nitrogen, see Figure 6.12) within the silicon material. SiC representing an electrically conductive semiconductor material effectively shorts the solar cell *pn*-junction, thereby leading to drastically reduced efficiencies. The problem of SiC formation, however, usually occurs only in the uppermost region of the ingot that is anyway rejected because of segregation of metallic impurities.

Despite oxygen and carbon being present in much higher concentrations, transition metals like iron or titanium are considered as much more important with regard to solar cell efficiencies with the exception of the outer edges (width 5–10 mm) of an ingot where in-diffusion from the Si_3N_4 coating may occur and the top segregation region metal point defects in high-quality multicrystalline silicon are present in concentration levels below the detection limit of Deep Level Transient Spectroscopy (DLTS) measurements,

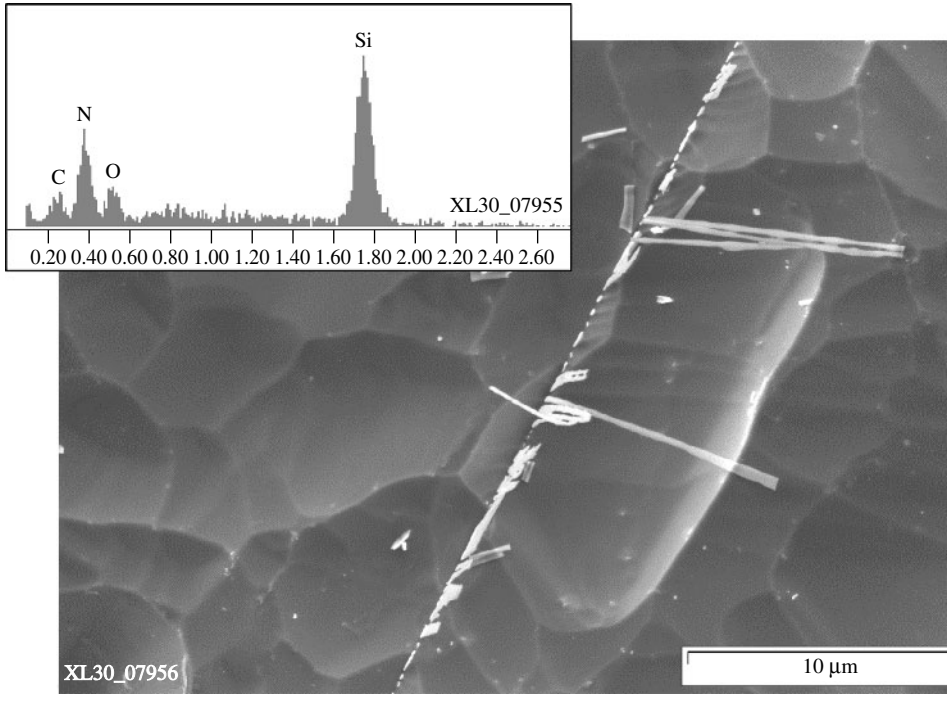


Figure 6.12 SEM (Scanning Electron Microscope) image of a heavily shunted solar cell region. The microscopic investigations reveal needle-shaped structures containing silicon, nitrogen, oxygen and carbon. The shunting mechanism is assumed to be due to electrically conductive SiC that short-circuits the solar cell *pn*-junction

that is, below approximately $10^{12}/cm^3$. The importance of metal impurities for multicrystalline silicon solar cells is, however, based on metal impurities controlling the activity of extended defects, specifically that of crystal dislocations.

We anticipate that metallic impurities are, for example, responsible for the observed systematic changes of the lifetime of multicrystalline silicon wafers after high-temperature steps in the range of 800 to 1000°C (e.g. the phosphorous diffusion step for fabrication of the solar cell *pn*-junction). The wafer lifetime quite commonly decreases in annealing steps above 900°C, where this decrease is even more significant at enhanced cooling speeds after the anneal. The proposed mechanism behind this lifetime degradation is a release of metal atoms from extended defects like dislocations into the wafer bulk material and a subsequent quenching of the metal atoms as highly recombinative point defects.

Another hint of an extensive interaction between extended defects and metal impurities is given in Figure 6.13 that depicts the theoretical segregation profile of iron in an intentionally contaminated multicrystalline ingot (mean iron concentration: $7.9 \times 10^{17}/cm^3$) as compared to the experimental one. We clearly can state a reduced experimentally determined segregation effectiveness most probably caused by iron segregation into extended defects competing with the segregation process in the liquid silicon phase during crystallisation.

In order to prevent such defect–metal interaction processes leading to enhanced recombination activity, a very effective segregation of metallic impurities into the ingot top region has to be assured. This segregation effectiveness, however, decreases with both increasing crystallisation speed and increasing concentration of extended defects.

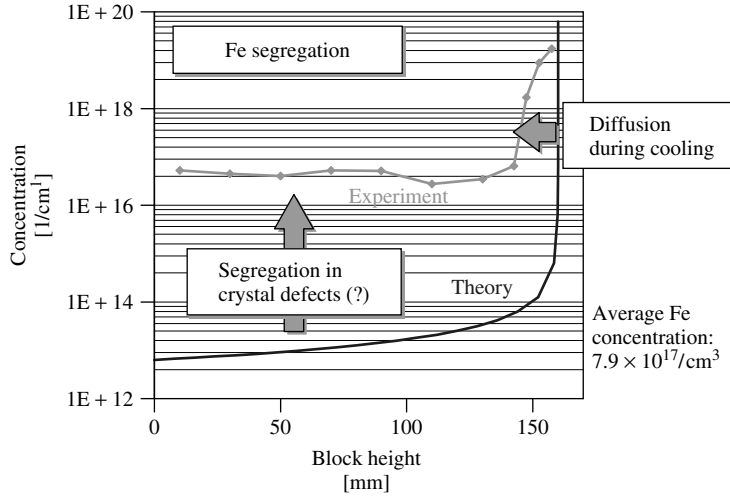


Figure 6.13 Experimentally determined iron concentration of an intentionally contaminated multicrystalline silicon test ingot (mean Fe concentration: $7.9 \times 10^{17}/cm^3$). The experimental data is given as a function of the block height and in comparison to the theoretically expected profile. The much higher than theoretically predicted concentration in the bottom and middle part of the ingot is attributed to a segregation not only into the silicon melt but also into extended crystal defects during solidification

This in turn verifies the importance of a properly adjusted and controlled crystallisation speed. In order to assure an effective impurity segregation for high-quality multicrystalline silicon, specifically in regions with increased defect densities (e.g. ingot bottom part), solidification at a low crystallisation speed is essential.

6.4 WAFERING

More than 80% of the current solar cell production requires the cutting of large silicon crystals. Multicrystalline ingots grown by the Bridgman or gradient freeze technique now reach cross sections of more than 50×50 cm^2 and weigh over 250 kg; monocrystalline Cz crystals have diameters of up to 20 cm today. While in the last few years the cost of solar cell processing and module fabrication could be reduced considerably, the sawing costs remain high.

Figure 6.14 shows that the sawing costs are a substantial part (29%) of the wafer production cost and thus contribute considerably to the total module cost. Since the sawing of the crystals is connected with high material losses (about 50%), ribbon growth techniques or the thin film technology, which avoid the sawing step, have a high potential for developing cheaper solar cells. However, both technologies still have to overcome serious difficulties and their development will probably take another 5 to 10 years. The present task is therefore to optimise the sawing technique for further cost reduction in mass production.

At the beginning of the PV industry, the available sawing technology of the microelectronic industry was used. The ingots were mainly cut by inner diameter (ID) saws. This technology is, however, relatively slow and not economical for mass production [26]. It was therefore gradually replaced by the multi-wire slicing technology [27]. The advantages are the higher throughput of about 500 to 700 wafers per day and per machine, a smaller kerf loss of about 180 μm and almost no restrictions on the size of the ingots. Currently, wafers between 250 and 350 μm are usually cut, but a wafer thickness down to about 100 μm can be achieved by the technique. Since the technology is relatively new and still under development, most wafer manufacturers have to optimise the sawing process by their own experience. The sawing process depends on several variable parameters as will be described next, which makes it difficult to optimise the process in view of throughput, material losses, reduction of supply materials and wafer quality.

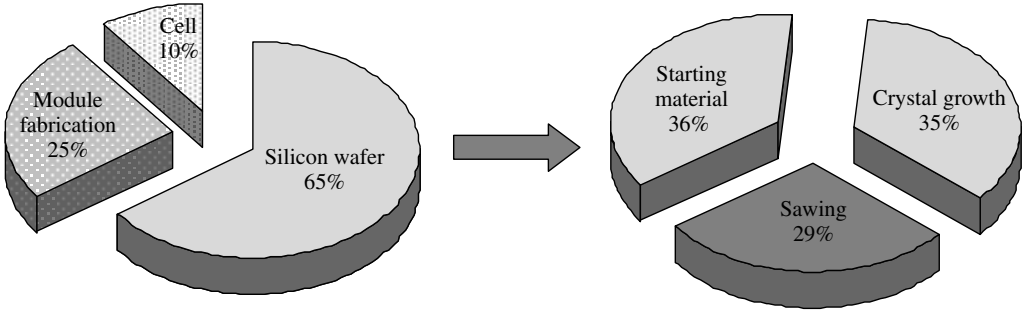


Figure 6.14 Cost distribution for modules and silicon wafers

Basic knowledge about the microscopic details of the sawing process is required in order to slice crystals in a controlled way. In the following section, the principles of the sawing process will be described as far as they are understood today.

6.4.1 Multi-wire Wafering Technique

After crystal growth the silicon ingots are cut in a first step by band saws into columns with a cross section that is determined by the final wafer size. Standard sizes are about 10×10 cm^2, but larger wafers sizes up to 15×15 cm^2 are increasingly used in the solar cell technology. The columns are glued to a substrate holder and placed in a multi-wire saw that slices them into the final wafers. The principle of the multi-wire technology is depicted in Figure 6.15. A single wire is fed from a supply spool through a pulley and tension control unit to the four wire guides that are grooved with a constant pitch. Multiple strands of a wire net (known as a web) are formed by winding the wire on the wire guides through the 500 to 700 parallel grooves. A take-up spool collects the used wire. The wire is pulled by the torque exerted by the main drive and slave as shown in the figure. The tension on the wire is maintained by the feedback control unit at a prescribed value. The silicon column on the holder is pushed against the moving wire web and sliced into hundreds of wafers at the same time. The wire either moves in one direction or oscillates back and forth. Solar cell wafers are mainly cut by a wire that is moving in one direction, whereas wafers for the microelectronic industry are cut by oscillating wires. Cutting in one direction allows higher wire speeds between 5 and 20 m/s, but yields less planar surfaces. Smoother and more even surfaces are obtained by oscillating sawing. Depending on the pulling speed, the wires have a length between 150 and 500 km in order to cut a single column in one run. The wire material is usually stainless steel.

Cutting is achieved by an abrasive slurry, which is supplied through nozzles over the wire web and carried by the wire into the sawing channel. The slurry consists of a

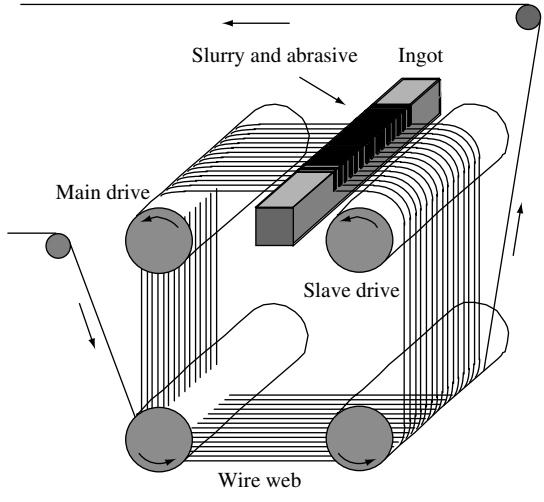


Figure 6.15 Schematic diagram depicting the principle of the multi-wire sawing technique

suspension of hard grinding particles. Today, SiC and diamond are the most commonly used abrasives. Both materials are very expensive and account for 25 to 35% of the total slicing cost. The volume fraction of solid SiC particles can vary between 20 and 60% and the mean grain size between 5 and 30 μm. For polishing smaller grain sizes below 1 μm are used. The main purpose of the slurry is to transport the abrasive particles to the sawing channels and to the crystal surface. It also has to keep the particles apart and must prevent their agglomeration. The entry of the slurry is a result of the interaction between the wire and the highly viscous slurry. Normally, only a small amount of slurry enters the cutting zone. The factors that are important here are the viscosity and the wire speed, but to understand the fluid mechanical problems that are involved a complex physical modelling is required. First attempts of a description have been reported recently [28–31].

Most of the commercial slurries are based on oil, but water-based or water-washable slurries based on ethylene glycol have been tested as well. Oil slurries have several drawbacks. The wafers can stick together and are difficult to separate after sawing. This problem will become even more severe when the wafer thickness will be reduced in the future. The removal of oil from the wafer surfaces requires comprehensive cleaning procedures. Since large quantities of slurry and SiC are used during sawing and recycling is not possible at present, the disposal of these materials has to be considered as well. The disposal causes, however, environmental hazards and is therefore complicated and expensive. On the contrary, water-based slurries or slurries that are very hygroscopic have the problem that hydrogen gas is generated from the interaction of water and silicon, which can cause the hazard of explosion. From the environmental point of view, water-washable slurries may be the choice of the future.

Material is continuously removed through the interaction of the SiC particles below the moving wire and the silicon surface. The abrasive action of the SiC depends on many factors such as wire speed, force between wire and crystal, the solid fraction of SiC in the suspension, the viscosity of the suspension, the size distribution and the shape of the SiC particles. The viscosity of the slurry depends on the temperature and the solid fraction of particles. Since the temperature rises as a result of the cutting process, the suspension has to be cooled and the temperature controlled during sawing. The viscosity of the slurry also changes because of the continuous abrasion of silicon and iron from the wire. This gradually deteriorates the abrasive action and the slurry has to be replaced or mixed with new slurry after some time.

The kerf loss and surface quality are determined by the diameter of the wire, the size distribution of the SiC particles and the transverse vibrations of the wire. The amplitude of vibration is mainly sensitive to the tension of the wire, but it also depends on the damping effect of the slurry. Increasing the tension will reduce the amplitude of vibration, hence the kerf loss [32]. Typical wire diameters are around 180 μm and the mean size of active particles can vary between 5 and 30 μm. This yields kerf losses around 200 to 250 μm per wafer.

The objective of efficient sawing is to slice with a high throughput, with a minimum loss of slurry and silicon and with a high quality of the resulting wafers. Since many parameters can be changed, the optimisation of sawing becomes a difficult task and today it is mainly done by the wafer manufacturers. They are mostly guided by experience. In

the following section, the main results of investigations are summarised, which describe the current understanding of the microscopic details of the wire sawing and yield some guidelines to optimise the process.

6.4.2 Microscopic Process of Wafering

Figure 6.16 shows schematically a cross section of the wire in the cutting zone. The space between the wire and the crystal surface is filled with slurry and SiC particles. The pressure of the wire on the particles varies along the contact area. The forces are maximal directly below the wire and decrease towards the side faces. Because of the transverse vibrations, the wire also exerts forces sideward, which determines the surface quality of the sliced wafers. The interaction between the abrasive SiC particles and the silicon crystal yields a distinct damage pattern on the surface that can be analysed by microscopic techniques. A typical surface structure as seen under an optical microscope is shown in Figure 6.17. Similar structures are obtained along the entire contact zone, which shows that the abrasive process is the same in all directions.

The surface structure consists of local indentations with a mean diameter of a few micrometers. Such a uniform structure can be explained by the interaction of loose, rolling particles that are randomly indented into the crystal surface until small silicon pieces are chipped away. Since SiC particles are facetted and contain sharp edges and

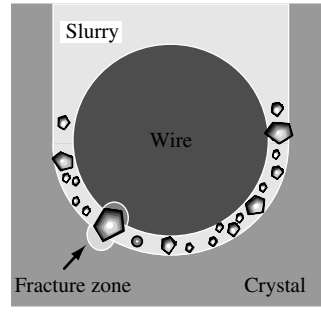
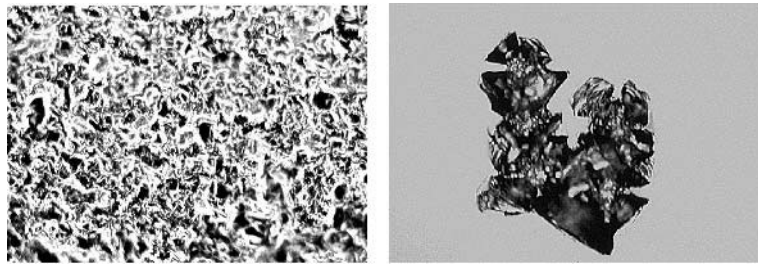


Figure 6.16 Cross section of wire, slurry with abrasive and crystal in the cutting zone



(a) (b)

Figure 6.17 Optical micrograph of the surface of an as-cut silicon wafer (a) and several micro-indentations on a polished silicon surface (b)

tips, they can exert very high local pressures on the surface. This "rolling grain" model forms the physical basis of the wire sawing process. Similar surface structures also form after lapping semiconductor surfaces with loose abrasive particles.

The individual process of the interaction of a single particle with sharp edges and the surface of a brittle material can be studied by micro-indentation experiments. This is shown in Figure 6.17(b) for a silicon surface. The damage structure of several overlapping micro-indentations with a Vickers diamond indenter resembles the structure of an as-cut wafer. Numerous micro-indentation experiments on monocrystalline silicon have been carried out in the past to investigate the damage structure quantitatively (e.g. [33–37]). The main results are summarised schematically in Figure 6.18 for a "sharp" Vickers indenter with pyramid geometry. Loading by sharp indenters first leads to the generation of a remnant plastic impression in the surface known as the elastic–plastic zone. Recent Raman investigations of this region have shown that under high pressures the silicon lattice transforms into other crystal structures. Several phase changes have been observed directly under the indenter, in particular a metallic high-pressure phase [38, 39]. Under loading at 11.8 GPa an endothermic transformation to metallic silicon (Si II) occurs ($\Delta G = 38$ kJ/mol), which partly transforms back to another high-pressure phase (Si III at 9 GPa, $\Delta G = -8.3$ kJ/mol). In the metallic state the silicon can plastically deform and

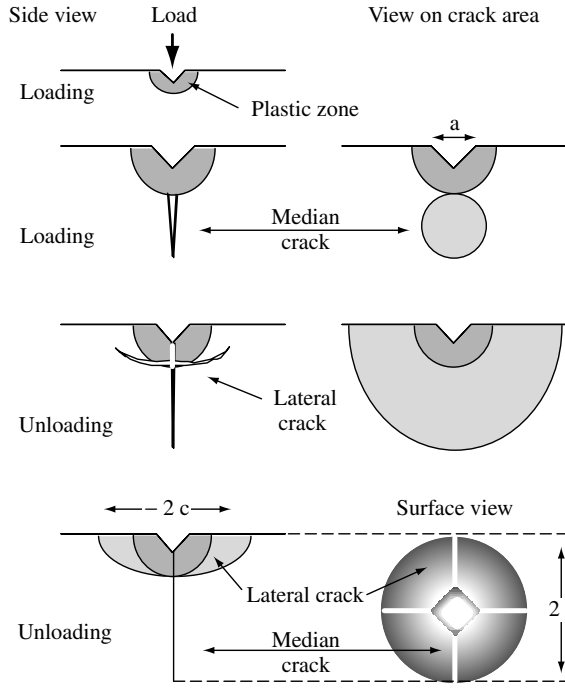


Figure 6.18 Schematic diagram of the development of the crack system below a sharp indenter upon loading and unloading. Dark gray areas indicate the plastic zone below the indenter. The dotted areas are the crack planes of the halfpenny-shaped median crack system. They are viewed from end-on (left side) or perpendicular to the plane (right side). In case radial cracks also occur, they may coalesce with the median crack and form a similar crack pattern

the material can be removed by processes known for ductile metals. This is, however, a slow but moderate process.

With increasing pressure the material begins to break and cracks are generated parallel to the load axis emanating from the plastic zone. Median cracks are generated beneath the plastic zone, where the tensile stresses are maximal, in the form of full or truncated circles. At a critical size they become unstable and extend towards the surface. In addition, shallow radial cracks may be generated at the edges of the plastic zone. Both radial and median cracks may coalesce to form halfpenny-shaped cracks that are visible at the surface (as shown in Figure 6.19). Upon unloading, residual stresses from the elastic–plastic zone can lead to lateral cracks parallel to the surface. When these lateral cracks reach the surface, material is chipped away. This is the main process for material removal during sawing. Chipping requires a certain minimum load to occur (chipping threshold). Above the limit when material is removed only the median and radial cracks remain. They are finally part of the saw damage.

A quantitative model based on the rolling grain interaction described above has been developed. Results have been compared with experimental investigations of the sawing process on commercial multi-wire saws, allowing for the extraction of useful conclusions. Details can be found in Reference [40].

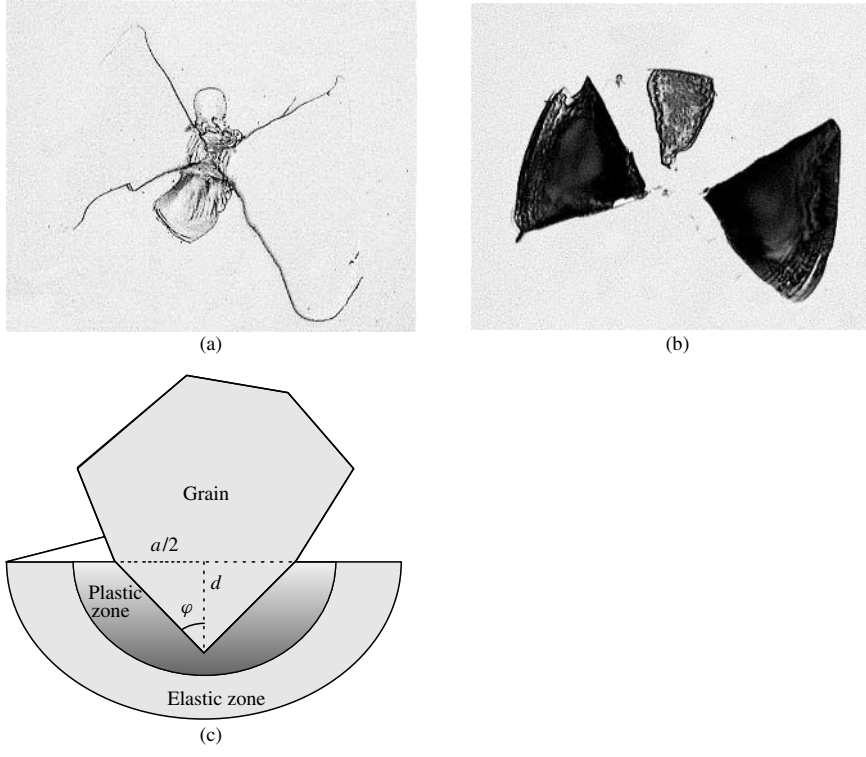


Figure 6.19 (a) Optical micrograph of median and (b) lateral cracks (below the surface) at a Vickers indentation. (c) Schematic representation of the impression of a sharp grain into a surface

6.4.3 Wafer Quality and Saw Damage

Several factors are currently considered to determine the quality of the wafers: fracture behaviour, crack density, thickness variations, surface roughness and cleanness. After sawing the surface of the wafer is damaged from the fracture processes and contaminated with organic and inorganic remnants from the slurry. Therefore, the wafers have to be cleaned and the saw damage removed by etching before a solar cell can be fabricated. In addition, the thickness and surface roughness of the wafer may vary, which may be detrimental for some of the further processing steps. All factors are related to the sawing process. Figure 6.20 shows an example of the topology of an as-cut surface. It consists of thickness variations on different length scales. On the scale of millimetres, one can observe grooves parallel to the direction of the wire. They occur particularly under higher loads and can be caused by a deficit of slurry, mechanical vibrations or inhomogeneities of the material. Mostly a large number of parallel wafers are then affected. Grooves on wafers cannot be removed by etching and thus reduce the quality of a wafer.

On a length scale of about 100 μm, the surface may have a wavy topology that is not detrimental unless sharp steps occur. On the micrometer-length scale the surface shows a certain roughness, which is directly related to the microscopic sawing process as described before. The extent of saw damage, which has to be etched away before solar cell processing, lies typically in the range of 5 to 10 μm.

Saw damage also occurs in the abrasive grains and the wire itself. Although the fracture strength of the SiC particles is higher than that of silicon, the grains eventually lose their sharpness owing to breakage that reduces their sawing performance. To reduce the abrasion of the grains, sawing should be done in a stress range where the load on the individual grains lies above the fracture strength of silicon but below that of SiC.

Typically, the wires have diameters between 150 and 180 μm and a length of about 150 to 500 km. They are made of stainless steel and coated with a brass layer.

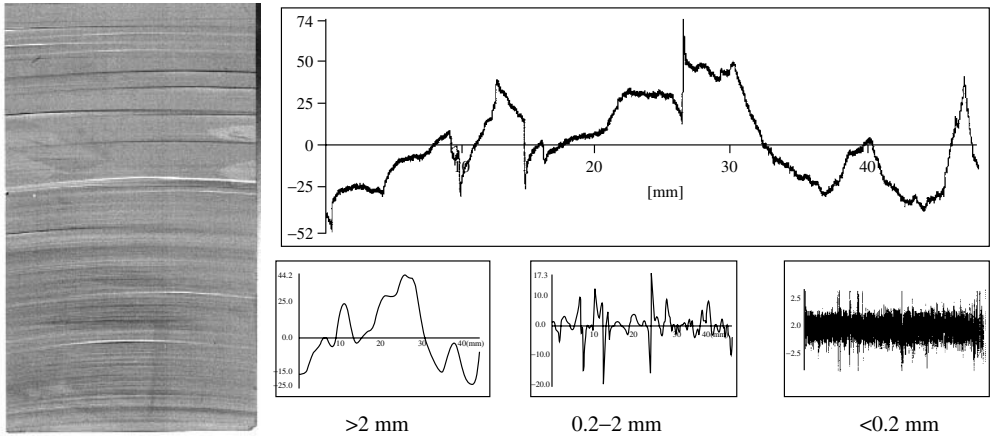


Figure 6.20 Surface structure of a wafer with grooves resulting from uneven cutting. It also shows the bowing of the wire under load during sawing. The surface profile measured by a laser scanner profiler is depicted on the right. Different wavelengths filtered from the profile are shown below

It is important that the thickness is very uniform over the entire length, because sudden changes in the diameter can lead to fracture of the wire or damage to the wafer surface. The abrasion of the steel wires is also due to the interactions with the grains. Excessive wear can lead to breakage, which is undesirable during sawing because it is very time consuming to build up the wire web inside the machine. Some manufacturers are beginning to develop *in situ* detection systems to control the sawing process and thus prevent the wire breakage.

6.4.4 Cost and Size Considerations

The investigations of the microscopic processes of wire sawing have laid the basis for the selection of the best range of parameters and for further modifications. It allows one to increase the sawing performance, to reduce the consumption of slurry, SiC powder, wire material and etchant, and hence directly the costs of slicing. Furthermore, the quality of the wafers such as roughness, flatness and saw damage of the surfaces can be improved. This is important in view of the development of thinner wafers for solar cells, which will reduce the consumption of expensive silicon. The current sawing technique in production allows the sawing of wafers with thickness down to about 200 μm. The goal is to further reduce the thickness to about 100 to 150 μm in production. Sawing of thinner wafers is possible but at present still at the expense of more breakage. The problem becomes even more severe when the wafer size increases at the same time to 15×15 cm^2 or more. In mass production such a development will only become possible by a careful selection of the parameter range and an *in situ* control of all the factors that determine the slicing process.

6.5 SILICON RIBBON AND FOIL PRODUCTION

Research and development on crystal growth technologies for production of crystalline silicon ribbon have been under way for three decades. Interest in methods of crystalline silicon wafer production was initiated during the oil crises of the mid-1970s. Out of this period arose the first large-scale efforts in R&D to develop low-cost methods of producing substrates for solar cell manufacture. A seminal program was conducted in the US, which was led between 1975 and 1985 by the Jet Propulsion Laboratory (JPL) Flat Plate Array Project [41]. It was the activity in this project in this time period, combined with larger investments from the private sector both in the US and internationally, that developed the seeds of the technology of crystalline silicon ribbon and foil production methods being commercialised today.

The past decade of R&D on crystalline silicon materials has culminated in the expansion of wafer manufacturing at an unprecedented pace. While established methods of production based on Cz growth, directional solidification and ingot casting have flourished, a new generation of ribbon technologies has moved past the R&D stage into large-scale manufacturing and is in competition with these conventional approaches. Ribbon technologies, some of which had entered R&D already in the early 1970s, and have now reached maturity with the start up of manufacturing on a megawatt (MW) scale, include Edge-defined Film-fed Growth (EFG), String Ribbon (STR) and Silicon Film^{TM} (SF).

Dendritic Web (WEB) production and the Ribbon Growth on Substrate (RGS) technique are moving to pilot demonstration phases. A summary of the changes in the status of leading ribbon/foil technologies over the past decade and projections for manufacturing capacities are given in Table 6.3. It is anticipated that the ribbon production will contribute in excess of 30 MW of wafers to world solar energy markets by the end of 2001.

Development has not been continuous for most of the methods listed above. The R&D has been interrupted and then restarted in several cases when the technological status changed to generate new opportunities for cost-effective production. EFG development has the longest continuous history. After initial technology development on EFG started at Tyco Laboratories in 1971, it was subsequently augmented with funding from Mobil Oil, starting in 1974. In the time span from 1971 to the present, pilot lines using five different variations of the EFG process have been evaluated, starting with single ribbons in 1971 to the octagonal crystal tube now being commercialised. Ownership transferred to ASE Americas in 1994, at which time the transition to manufacturing was initiated. After periods of decreased activity, WEB, STR and RGS have all been strengthened with R&D in the past several years subsequent to being revitalised by new owners. WEB development was initiated with funding from Westinghouse in the 1970s, but now is being carried out by EBARA Solar. STR technology underwent an R&D phase in the early 1980s under the name of Edge-Stabilised Ribbon (ESR) and Edge-Supported Pulling (ESP) at the National Renewable Energy Laboratory and at Arthur D. Little, respectively, before being taken up in 1994 by Evergreen Solar. RGS development was initiated at Bayer, but is currently continuing with ECN of the Netherlands. If successful, a future commercialisation is anticipated by Deutsche Solar in Germany and Sunergy in the Netherlands.

Ribbon and foil technologies must meet the challenges of the photovoltaic marketplace and overcome a number of existing technical barriers if they are to continue to expand manufacturing and to position themselves to remain competitive in the next decade. Challenges to be met are productivity increases on a per furnace basis to drive down labour and overhead (capital) costs, improved mechanical and electronic quality of ribbon wafers together with the development of low-cost solar cell designs that will raise efficiencies to 18 to 20% and reduction of wafer thickness while maintaining high yields in order to reduce demand on silicon feedstock. Achievement of these goals in the next decade can lead to cost decreases, which will drive additional volume expansion for

Table 6.3 Historic record on R&D and manufacturing status of leading ribbon/foil technologies of the past decade

Wafer process/ year started	1990 status level		2000	2001	Schematic
WEB/1967	R&D	<0.1 MW	R&D <0.2 MW	Pilot −0–1 MW	Figure 6.20
EFG/1971 (Ribbon); 1988 (Octagon)	Pilot	1.5 MW	Production −12 MW	Production −20 MW	Figure 6.21
ESP (STR)/1980	R&D	–	Pilot <0.5 MW	Production <5 MW	Figure 6.23
SF/1983	–	–	Pilot −1–2 MW	Production >5 MW	–
RGS/1983	R&D	–	R&D	Pilot <1 MW	Figure 6.24

ribbon and foils and allow these new-generation technologies to become market leaders in silicon wafer production. Technology description, the status of each of the growth approaches and the barriers for each of the technologies to overcome in order to remain competitive are the topics of the following sections.

6.5.1 Process Description

The ribbon technologies that have been proposed over the past three decades and that have survived till the commercial manufacturing and R&D phases (Table 6.3) may be grouped into two basic approaches: "vertical" and "horizontal" growth (pulling) methods. The latter category is further subdivided into methods in which either a substrate is used to assist in the formation of the crystal or foil or those that do not use any substrate material. The horizontal methods refer not so much to the geometrical aspects related to the ribbon-pulling direction as to the disposition of the temperature gradients, which act at the interface and influence growth characteristics. The EFG, WEB and STR methods are examples of the vertical method category, while both the RGS foil and the SF methods grow crystals in a horizontal-pulling configuration with the aid of a substrate. The term "foil" is used interchangeably with wafer, but here we use it to refer more specifically to the RGS wafer to distinguish a unique aspect: the wafer is crystallised upon contact with a substrate, and is then detached and the substrate material recycled.

Ribbon/foil growth techniques have historically been evaluated in a number of variants and modifications of the techniques listed in Table 6.3. Successes and failures in many of these variants often spawned new processes or led to evolution and modifications in old variants. A bibliography and descriptions of the techniques and a detailed historical perspective of the many variant ribbon technologies that have been pursued can be found in the endnote [42] and in References [43, 44].

Fundamental differences exist in the heat transfer and the interface temperature gradients during growth for these two general categories of ribbon and foil production methods. These lead to very different process limits in several important areas: the capacity, or throughput potential in a single furnace configuration, crystallite or grain nucleation characteristics and the pulling speed. The speed is constrained as a consequence of the thermoelastic stress acting on the crystal during growth. The pull speed and stress affect the defect density and electronic quality. For example, for the vertical techniques – WEB, EFG and STR – the crystal growth direction and dominant heat transfer of latent heat from the interface are both parallel to the pulling axis of the ribbon and essentially perpendicular to the growth interface. The latent heat conducted along the ribbon is radiated to the environment. The pulling speed and the interface growth velocity are the same. For RGS and SF, crystals nucleate on the substrate and grow nearly perpendicular to the substrate-pulling direction, while the growth interface tends to be angled towards the pulling axis of the substrate. Thermal conduction of latent heat from the growth interface is augmented in the direction perpendicular to the pulling axis, that is, through the thickness of the ribbon, because of conduction into the substrate. This augmented heat removal allows very high ribbon production rates, whereby low interface growth rates, v_I, are realised with high pull rates, v_P, that is,

$$v_P = v_I / \cos(\theta)$$

where θ is the angle between the normal to the interface and the pull direction and is close to 90°. The low interface growth rate, in turn, reduces the need for the high interface temperature gradients required to maintain growth stability in vertical ribbon growth. The gradients in the vertical methods are the cause of high thermoelastic stresses and set practical productivity limits when low defect densities and flat ribbon are required. Details on the process limits affecting the horizontal growth techniques may be found in other publications [45, 46]. We next give a description of each of the techniques listed in Table 6.3.

WEB. WEB is grown directly from melted silicon in a crucible with no shaping device (Figure 6.21) [47]. A dendritic seed or button is lowered into a supercooled melt. The seed spreads laterally to form a button. When the seed is withdrawn, two secondary dendrites propagate from the ends of the button into the melt, forming a frame to support the freezing ribbon. The dendrites grow into the melt that has been supercooled by several degrees. Very accurate melt temperature control is required in order to maintain the supercooled interface condition and prevent "pull-out", whereby the growth terminates by voiding of the meniscus. The width of the ribbon is controlled by the position of the two dendrites that support the liquid film. The growth velocity is determined by the rate of removal of the latent heat into the ribbon and of the heat conducted through the melt through the meniscus. Typical growth rates are from 1 to 3 cm/min.

In vertical ribbon growth, the meniscus contains the suspended melt volume that connects the bulk melt to the growth interface and crystal. Its shape and the heat conduction taking place within it critically affect impurity segregation and the crystallisation

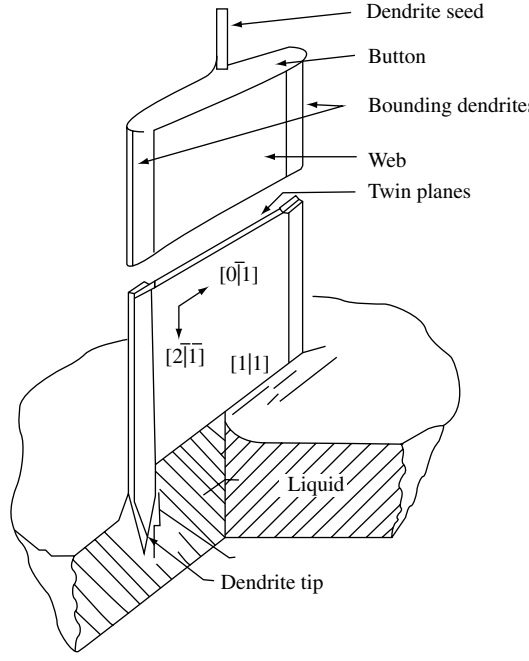


Figure 6.21 Schematic of Dendritic Web (WEB) growth process for ribbon

conditions and shape of the crystal. The meniscus height, h, away from the influence of the dendrites, is fixed by the surface tension, liquid-silicon contact angle and liquid density. This can be calculated from the solution of the Young–Laplace equation requiring a contact angle of $\Theta = 11^\circ$ at the liquid–solid interface that gives

$$h = a[1 - \sin(\Theta)] \quad \text{where} \quad a = (2\sigma/\rho g)^{1/2}$$

where $\sigma = 720$ dyne/cm is the surface tension, $\rho = 2.53$ g/cm^3 is the density of liquid silicon and g is the gravitational acceleration. Because thermal radiation dominates the heat flow from the ribbon, the geometry of the heat shields and the susceptor lid controls the isotherms in the melt and the ribbon.

Accurate temperature control, within a few tenths of one degree, is necessary to ensure a uniform ribbon width and thickness. The temperature of the melt surface must be constant over the width of the growing web to prevent the dendrites from growing in or out. The dominant impurity in the WEB in production today is oxygen since a quartz crucible is used. Typical WEB thicknesses range from 100 to 150 μm and widths up to 8 cm have been grown. Growth lengths between seedings in pilot production extend to many tens of meters.

EFG. In this technique, the geometry of the ribbon is controlled by a slotted graphite die through which silicon is fed via capillary action (Figure 6.22) [48]. A seed crystal is

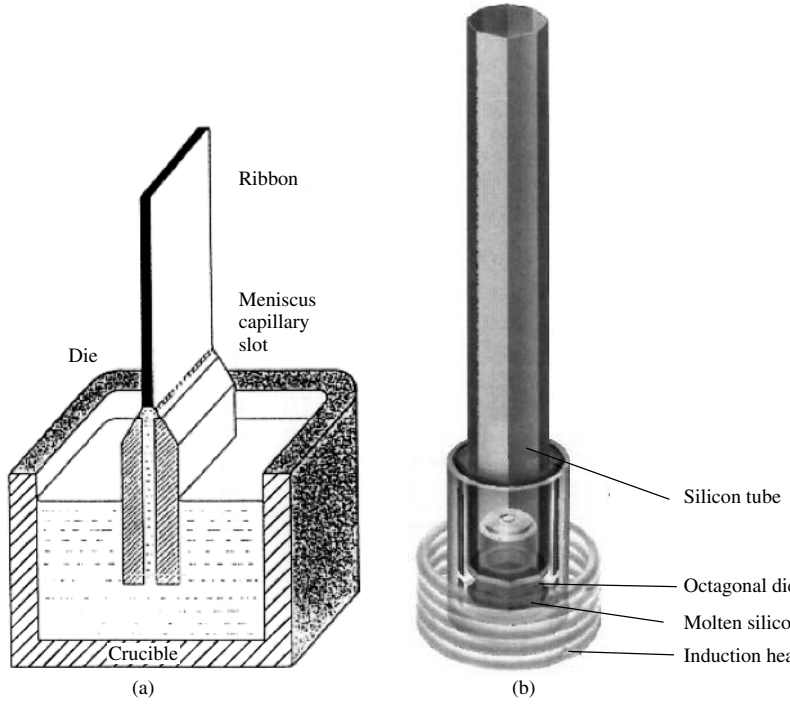


Figure 6.22 Schematics of Edge-defined Film-fed Growth (EFG) growth process: (a) ribbon die and crucible configuration and (b) octagon configuration

lowered until it contacts the liquid in the capillary. The liquid spreads out over the top of the die to the edges where it is pinned by surface tension. The seed is withdrawn, pulling the liquid up while more liquid flows upward through the capillary. As the ribbon is withdrawn, the liquid freezes on the solid crystal. The die and the crucible are integral, that is, made of the same piece of graphite. The thickness of the sheet material is fixed by the width of the die top, distance between the die tip and melt level, meniscus shape, heat loss from the sheet and the pull rate. The shape of the liquid–gas interface, or meniscus, which connects the die to the solidifying ribbon, is described by the Young–Laplace or the capillary equation. As with WEB, the growth rate is controlled by how fast heat can be conducted away from the interface and lost by radiation or convection from the solid crystal. Growth is self-stabilising because the meniscus height increases with an increase in pull rate. The curvature of the meniscus causes the thickness of the crystal to decrease. This increases the rate of heat removal per unit area of the interface, thus increasing the growth rate until it is again equal to the pull rate.

The dominant impurity in EFG ribbon is carbon, which is in supersaturation. Temperature control of a few degrees along the interface is sufficient to prevent ribbon pull-out or freezing of a growing ribbon to the die top. Over time, the die becomes eroded affecting ribbon properties and leading to a non-uniform ribbon thickness and growth difficulties.

Ribbons with thicknesses from 400 μm to as little as 100 μm have been grown. Rather than a single flat ribbon, hollow EFG polygons are grown to enhance the rate of throughput. The favoured geometries for commercial development today are octagons with 10-cm- or 12.5-cm-wide faces, equivalent to growth of up to a 100-cm-wide ribbon from a single furnace. Various closed geometries, including nonagons with 5-cm faces, and large-diameter cylinders have been grown. Growth velocities for the EFG octagon are 1.7 cm/min. The relationships between the EFG process parameters and the silicon ribbon characteristics, including thermal stress and the influence of impurities and defects on the quality of the material, have been extensively examined and are reviewed in Reference [49].

An extension of the EFG process to growth of 50-cm-diameter cylinders has recently been demonstrated [50]. An example of such a cylinder 1.2 m in length is shown in Figure 6.23. The cylindrical geometry offers some relief from the large thermoelastic stresses generated in plane ribbon. This allows consideration of higher productivity furnaces from a combination of larger perimeters and potentially higher growth speeds. Growth of EFG cylinders with average wall thickness down to 100 μ has been demonstrated, and solar cells have been made on this material [51].

STR. In this technique, ribbon growth takes place directly from a pool of melted silicon without a die (Figure 6.24) in a process mirroring the WEB geometrically. Rather than dendrites, as with WEB, the position of the ribbon edges in STR is maintained by two strings fed through holes in the bottom of the crucible. The strings are drawn upward out of the melt to support the meniscus and the ribbon, and their pull rate determines the growth speed of the ribbon. The thickness of the ribbon is controlled by surface tension, heat loss from the sheet and pull rate. An important difference of the STR process from WEB growth is that the constraints of maintaining propagating dendrites and a supercooled melt are eliminated, and this relaxes the high degree of temperature control required in the WEB furnace. The high meniscus, 7 mm (see Equation 2), allows simple control of

Figure 6.23 Experimental 50-cm-diameter EFG cylinder exiting from furnace

the growth process and maximises its stability to mechanical and thermal fluctuations. Depending upon the wetting qualities of the strings and their diameter, the meniscus height at the strings near the edges differs from that at the centre, and it is usually much lower at the edges [52, 53].

For comparable thicknesses, the growth velocities of STR are similar to EFG and WEB. Careful adjustment of the growth parameters can allow very thin ribbon, down to 5 μm, to be grown [54]. Generally passive after heaters are used, but some work on an active after heater has been carried out to allow low-stress, 100-μm-thick ribbon to be grown. This material was sufficiently flat to be made into solar cells. Because of the concave downward meniscus curvature at the string, any grains nucleated at the strings can propagate into the ribbon.

RGS. In this growth technique, the silicon melt reservoir and die are placed in close proximity to the top surface of a substrate, on which the ribbon/foil grows. The substrate may be graphite or ceramic (Figure 6.25) [55]. The principle is to have a large wedge-shaped crystallisation front. The die contains the melt and acts to fix the width

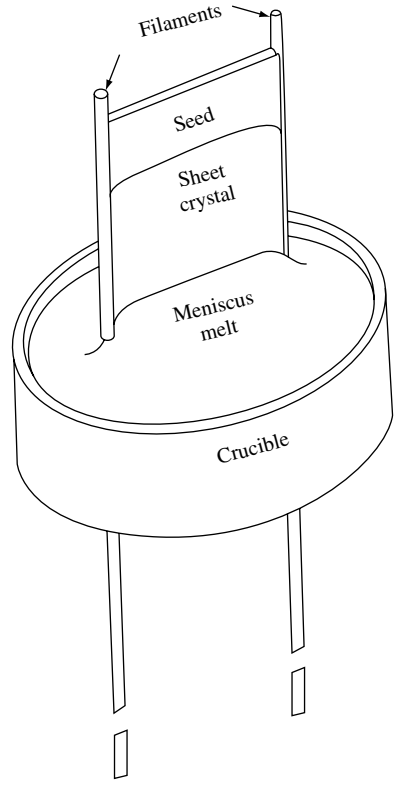


Figure 6.24 Schematic of String Ribbon (STR) growth system

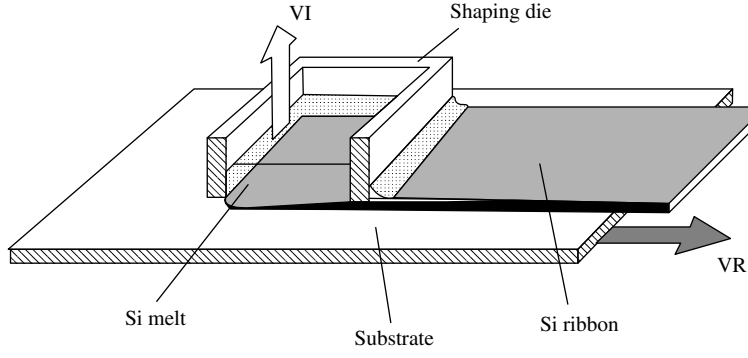


Figure 6.25 Schematic of Ribbon Growth on a Substrate (RGS) configuration

of the foil. The thickness of the foil is controlled by the heat-removal capacity of the substrate, pull rate and surface tension. The direction of crystallisation and growth are nearly perpendicular. The area of the growth interface now can be very large compared to the foil thickness. The latent heat is extracted by conduction into the substrate. The thermal gradients near the interface are small, thus reducing thermally induced stress in

the wafer. Growth rates from 4 to 9 m/min have been demonstrated. One example was an 8.6-cm-wide foil, 300-μm thick, grown at 6.5 m/min.

An important goal in the R&D phase of RGS has been to make a substrate that can be reused. After cooling, the silicon foil may be separated from the substrate by stresses arising from differences in thermal expansion between substrate and silicon. Experimentation with coated foils is in progress and offers the most promise in providing a cost-effective reusable substrate. Thicknesses between 100 and 500 μm have been grown. By working with the lower thermal gradients in the foil thickness direction, but still large enough for rapid growth, fluctuations in the pulling speed and gradient only affect the foil thickness slightly [55].

SF. The details of the SF process are proprietary. The silicon crystal is grown in a thin layer directly upon either an insulating or a conducting substrate, with a barrier layer that promotes nucleation [56]. In the case of an insulating substrate, the barrier layer must also act as a conductor to collect the current generated in the cell. In the case of a conducting substrate, the substrate can also act as an electrical conductor if *vias*, or holes, are provided to connect the thin silicon crystal layer and the substrate. The SF thin film and barrier layer do not separate from the substrate on cooling as in RGS, but become the active part of the solar cell. The grown polycrystalline silicon layer is made very thin ($\ll$100 μm), thus reducing the amount of silicon required. Currently, layers of 20-μm thickness are under development. A variety of substrate materials have been used including steel, ceramics and graphite cloth [56, 57]. It is necessary that the barrier layer prevent the transport of impurities from the substrate into the silicon. The barrier layer allows wetting and nucleation during growth. It should also act to electrically passivate the back surface and have a high optical reflectivity.

An insulating barrier layer has been reported that promotes growth of large columnar grains (greater than 1 mm) through the thickness of the grown SF silicon film [56]. As-grown films on coated ceramic substrates exhibit very low diffusion lengths of less than 10 μm. The new barrier layer and the substrate result in longer diffusion lengths, 20 to 40 μm, and the silicon has an improved response to phosphorous gettering.

6.5.2 Productivity Comparisons

Ribbon crystal growth technology for production of silicon wafers has been historically faced with the evaluation of the trade-off between bulk electronic quality and throughput (productivity per furnace). The choice of crystal growth conditions is made on the basis of wafer cost parameters and the premium imposed by the marketplace on solar cell efficiency. Material quality that can translate into high solar cell efficiencies has always been a primary market driver guiding ribbon growth process development. Ribbon wafers have inherently lower wafer production costs than those obtained from directionally solidified and cast ingots, or Cz boules, because ribbon growth avoids the large material losses due to sawing, which exceed 50% of the starting feedstock. The ribbon geometry has an additional cost advantage in that high levels of radiative cooling allow very rapid pulling rates. On the other hand, the higher wafer cost for the cast ingot or Cz boule production methods demand that these products maintain an advantage in bulk electronic quality, and higher solar cell and module efficiencies, in order to stay competitive with respect

Table 6.4 Single-furnace performance metrics for ribbon technologies under development and in commercialisation

Method/ parameter	Pull speed [cm/min]	Width [cm]	Throughput [cm^2/min]	Furnaces per 100 MW[a]
WEB	1–2	5–8	5–16	2000
EFG Octagon	1.65	8 × 12.5	165	100
STR	1–2	5–8	5–16	1175
SF	[b]	15–30	[b]	[b]
RGS	600–1000	12.5	7500–12 500	2–3

[a] Furnace data are taken from Reference [58], where throughput is normalised for comparison purposes to an overall yield of 90% and cell efficiency of 15% for all processes
[b] Pulling rate parameters for the SF process are not available

to ribbon technology. Superior electronic quality is generally achieved at the expense of throughput in bulk crystal growth from the melt.

A summary of performance metrics for ribbon technologies currently under development is given in Table 6.4. A critical driving parameter in technology development of ribbon methods for large-scale manufacture and commercialisation is the productivity per furnace. Productivity governs the capital cost of installed capacity and direct labour costs, which constitute significant barriers to ongoing commercialisation on a large scale for all ribbon technologies.

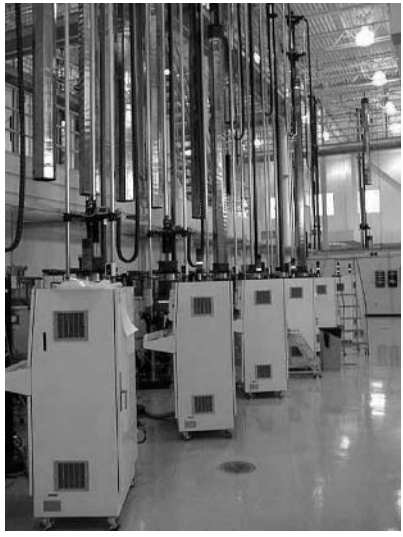
6.5.3 Manufacturing Technology

Table 6.4 shows that development of ribbon technologies is proceeding along two distinct paths. WEB and STR rely on low furnace cost to remain competitive in wafer costs. Development of SF and RGS technologies is focused on achieving superior throughput per furnace.

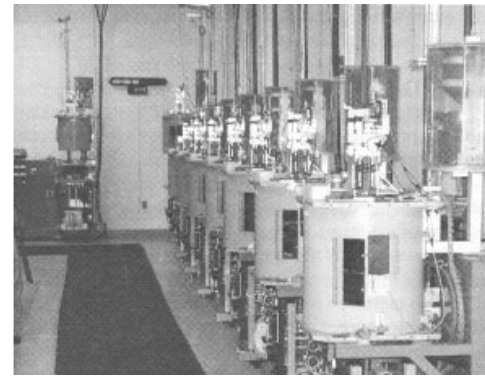
Scaling of ribbon factories significantly beyond the manufacturing levels practised now, for example, 100 MW, poses different challenges for technology development in these two cases. The low throughput ribbon furnace (WEB, STR) requires a simple and low-cost furnace design, a high level of automation and low infrastructure costs. In contrast, high reliability and uptime of furnaces and the growth process are most critical for the high throughput technologies SF and RGS. EFG technology development is moving in a direction that is trending towards the middle of these two extremes.

Examples of commercial installations and equipment now in manufacturing for EFG and STR technologies are shown in Figure 6.26. Figure 6.26(a) pictures a group of furnaces in the EFG octagon manufacturing line, with a high bay area to accommodate the 5.4-m octagon growth lengths. EFG wafers of 10-cm width and of 10- or 15-cm lengths are standard products and are cut from the octagon tubes using high-speed lasers (not shown). More detail on this technology is given in Reference [59].

Single ribbon furnaces for the growth of 8-cm-wide ribbon of the STR manufacturing line are shown in Figure 6.26(b). Ribbon sections up to a meter long are scribed



(a)



(b)

Figure 6.26 Manufacturing crystal growth equipment in commercialisation for (a) EFG and (b) STR technology

from the ribbon while it is growing, and then further cut into wafers of 10-cm length prior to processing.

WEB, SF and RGS ribbon technologies all are in various stages of R&D and pilot demonstrations leading to commercialisation. SF is perhaps the closest to successfully scaling up the technology, as a wider (20 cm) and higher throughput furnace is reaching the final demonstration phase. WEB is basing its expansion to a 1- to 2-MW pilot operation on a single ribbon furnace for producing 5-cm-wide wafers. RGS is moving towards the use of 12.5-cm-wide ribbon in which high sustained throughput technology and consistent high material quality needs to be demonstrated.

6.5.4 Ribbon Material Properties and Solar Cells

Except for WEB, all the growth processes produce multicrystalline ribbon. WEB ribbon grows with (111) crystallographic faces (see Figure 6.21). It typically does not have any grain boundaries, but has a single multiple-twin boundary located about mid-way through the ribbon thickness. Each (111) surface is made up of a single grain, and the dislocation density is the lowest of any ribbon, 10^3 to $10^4/cm^2$.

For the other two vertical ribbon growth cases, EFG and STR, extraneous crystals are generated most often at the sides of the ribbon (i.e. octagon tube corners) and propagate along the growth axis of the ribbon. These crystals form elongated grains often many centimetres in length along the growth axis, and which extend through the ribbon thickness. In EFG, the grains are interspersed with numerous twin boundary arrays. The grains at the ribbon edge in STR are generally smaller than in the centre. Because the meniscus near each string is concave downward, the grains nucleated at the string can

propagate into the ribbon centre. In both EFG and STR, the grain dimensions typically are large compared to the ribbon thickness and the as-grown diffusion length, and the charge collection and solar cell efficiency are minimally influenced by grain boundary recombination.

For SF and RGS, the substrates provide the dominant nucleation sites for crystals. The grains usually are columnar and extend through the ribbon thickness with dimensions that can be made large compared to the diffusion length with proper adjustments of the pulling speed and interface inclination.

Fast movement of the solid–liquid interphase reduces the ability of the freezing process to segregate impurities to the melt. This is represented in Table 6.5 together with the crystalline aspect and the dislocation density of the different technologies.

Stresses produced by thermal gradients during growth generate most of the intragranular dislocations in ribbon material. In the best quality EFG material, it has been shown that the loss in background current is highly correlated with the dislocation density and not grain boundaries [60]. It is not clear if the intrinsic qualities of the dislocations act as recombination centres or if the associated impurity cloud is responsible. Dislocations decorated with SiO_x precipitates have been reported to limit the lifetime in WEB [61] and RGS material [62]. Recent photoluminescence studies suggest similar causes for dislocation recombination activity in EFG material [63].

A critical parameter for solar cell efficiency is the ribbon thickness. As shown by Bowler and Wolf [64], an optimum thickness for peak efficiency occurs. This thickness is dependent on the fabrication technique and material properties, including front and back surface recombination velocities, minority-carrier lifetime and base resistivity among other parameters. For a "typical" $n^+ pp^+$ structure with a 200-μm diffusion length, L_d, a back surface field and a single layer anti-reflection coating, the optimum thickness region consists of a broad peak near 80 μm (Figure 6.27) as calculated using PC-1D [65]. For a 100-μm L_d the optimum thickness peaks at about 50 μm and for a 400-μm L_d it is near 120 μm. A front surface recombination velocity of 10^5 cm/s is assumed.

Table 6.5 Comparison of silicon ribbon material characteristics. In all cases the columnar grains extend through the thickness of the ribbon. An equilibrium segregation coefficient of $k_0 \sim 10^{-5}$ is typical of the most detrimental impurities for ribbon bulk lifetime

Material	Crystallinity	Dislocation density [1/cm^2]	Effective segregation	Thickness [μm]
EFG	Columnar grains in growth direction	10^5–10^6	$k_0 < k_{eff} < 10^{-3}$	250–350
WEB	Single (111) face central twin planes	10^4–10^5	$k_0 < k_{eff} < 10^{-3}$	75–150
STR	Columnar grains in growth direction	5×10^5	$k_0 < k_{eff} < 10^{-3}$	100–300
SF	Columnar grains through thickness	10^4 to 10^5	$k_{eff} < 1$	50–100
RGS	Columnar grains through thickness	10^5–10^7	$k_{eff} < 1$	300–400

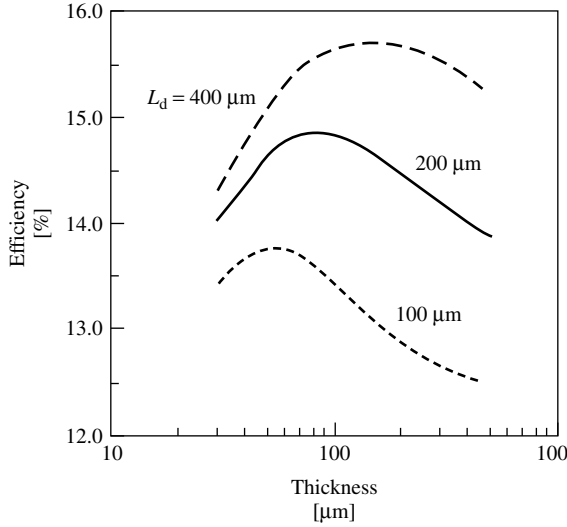


Figure 6.27 Solar cell efficiency versus thickness. (See the text for a description of the solar cell parameters)

The thickness of WEB and SF is closer to the optimum than the other three ribbon growth techniques. Light trapping will move the optimum to a thinner base, but such optical structures on multicrystalline ribbon are not yet practical. For growth on a substrate, it is possible to texture the substrate to trap light. This has been shown on SF wafers [57].

Solar cell fabrication processes used for conventional Cz and cast material wafers are commonly applied to silicon ribbon. If the ribbon is doped *p*-type with boron, the *n*-type emitter typically is formed by phosphorus diffusion either from $POCl_3$, PH_3 or a spin-on source. Front contacts are usually screen-printed or evaporated with diffused or alloyed aluminium as back contact to produce a back surface field. A double or single layer anti-reflection coating may be used. For SF grown on an insulating substrate, contact with the back surface requires etching holes to allow contact with the conducing barrier layer. Table 6.6 summarises material characteristics and solar cell performance potential of the various forms of ribbon material. Boron dopes the ribbon *p*-type. Antimony can be used to produce *n*-type material as reported for WEB.

Table 6.6 Some "best" solar cell efficiency levels for various ribbon technologies

Material	Resistivity [Ω cm]	Carbon [1/cm^3]	Oxygen [1/cm^3]	Efficiency [%]
EFG (Reference [66])	2–4, *p*-type	10^{18}	$<5 \times 10^{16}$	15–16
WEB	5–30, *n*-type	Not detected	10^{18}	17.3
STR	1–3, *p*-type	4×10^{17}	$<5 \times 10^{16}$	15–16
SF (Reference [67])	1–3, *p*-type	5×10^{17}	5×10^{17}	16.6
RGS (Reference [68])	2, *p*-type	10^{18}	2×10^{18}	12.0

Ribbon cell processing, nevertheless, needs to recognise the unique growth constraints of all of the techniques. As noted above, a common material characteristic for ribbon materials historically has been the compromised as-grown bulk electronic quality, dictated by the development of desired high-throughput growth configurations. This strategy has its base in a commercial demand for very low cost wafers that must compete at relatively low volumes with already established dominant products based on single-crystal Cz wafers or directionally solidified and cast ingots. As-grown ribbon diffusion lengths most often are less than 100 μm. To obtain the maximum cell efficiency on this ribbon, with higher dislocation densities and contaminating impurities than in competitor wafers, a solar cell processing strategy was devised early in the history of ribbon technology development that incorporates special bulk lifetime upgrading steps. For example, bulk lifetime upgrading via aluminium alloying and hydrogen is particularly effective for EFG material [69, 70]. Another approach is to use plasma-enhanced chemical vapour deposition (PECVD) of silicon nitride to generate hydrogen for passivating the silicon bulk [71].

6.5.5 Ribbon/Foil Technology – Future Directions

Ribbon/foil wafer production is poised to move on to face a new round of challenges in the construction of large (50–100 MW) manufacturing facilities for crystalline silicon ribbon wafers. The RGS foil technology, with the greatest potential of all ribbon methods for cost reduction on the basis of a high throughput per furnace, is entering a pilot demonstration phase. This process faces challenges in process and equipment development before it can enter high-volume manufacturing of wafers. In the next pilot phase, we may expect that RGS will demonstrate a consistent material quality sufficient for improving cell efficiency to greater than 12% from the current 10 to 11%; process control capable of reproducibly producing a low stress, regular structure, with a shaped 12.5-cm-wide wafer suitable for high-yield cell processing at about a 300-μ thickness and a reliable prototype furnace with melt replenishment to enable continuous production, which will gain full benefit from the high throughput growth concept.

The future focus of WEB and STR ribbon development is on process automation and capital cost reduction for furnaces and infrastructure based on a concept of a low throughput (per furnace) process. Production will probably grow to between 1 and 10 MW for each of these approaches over the next several years. Process parameters that will be practised in this next round of manufacturing equipment expansion for both of them are narrowed down to a single ribbon per furnace concept with similar throughput parameters – a ribbon width of about 8 cm and a pull speed in the 1 to 2 cm/min range. The WEB ribbon technology is embarking on its pilot expansion with a unique process for the growth and manufacturing of solar cells at a 100-μm wafer thickness. STR is expanding its manufacturing with a 300-μm-thick wafer. Although wafer bulk quality is demonstrated on an R&D level to be capable of achieving 15 to 16% cell efficiencies for STR, and over 17% for WEB, quality and cell efficiency levels on a multi-megawatt scale are yet to be established. Both approaches will attempt to demonstrate the cost-effectiveness of operating on a multi-MW level in the next few years. R&D directions, which would appear to have the most potential for the reduction of wafer material costs for these techniques, are growth of wider ribbons and more ribbons per furnace.

EFG and SF ribbon technology have successfully completed their initial scale up of wafer production to the multi-megawatt level. Process control and equipment reliability improvements, which can drive throughput and yield higher, become increasingly more dominant in determining the manufacturing cost. As throughput per furnace increases, capital cost impact on variable manufacturing costs from the growth furnace decreases. There is pressure on all ribbon technologies to concentrate on reducing the capital cost of the wafer production equipment if the transition to large-scale wafer manufacturing of 50- to 100-MW annual capacity factories is to be sustained.

Process variable ranges are firmly established for the EFG process. Octagon tube length, throughput and wafer thickness parameters will remain within the ranges given in Table 6.4 for the next generation of equipment, while octagon face width, and hence the EFG wafer dimension, will increase from 10 to 12.5 cm. The major thrust in R&D on the EFG process in this phase will be on process control and process and equipment automation.

The benefits of the savings in silicon feedstock and potential gains in cell efficiency with a reduction of the ribbon/foil thickness are well understood for all these technologies. However, the pressure to carry out R&D in this direction for the case of wafers made from ribbons is not as acute as for conventional crystalline silicon wafer manufacturing methods because of the large benefit in feedstock savings already realised for ribbons on account of their favourable geometry. The R&D for the next generation of vertical ribbon technology beyond about five years will target the demonstration of production methods for very thin wafers. A strong motivator driving thickness reduction will be the pressure to increase the cell efficiency, which is seen to be capped in the 16 to 17% range (see Table 6.6) for current cell designs and wafer bulk quality. Low-cost cell designs, which can break this barrier and achieve desired targets of 18 to 20% for ribbon, are most easily found for thinner wafers, but this also requires improvements in bulk electronic quality to be achieved concurrently.

The major problem in this development for all vertical growth techniques will be to find methods to reduce the effects of thermal stress. At present, the only means by which this can be done is to reduce the pull speed. The cylinder geometry has the potential to offer some relief to the EFG process at the expense of having to work with thin curved wafers in cell and module processing. Although thermal stress is not a problem with substrate-assisted growth techniques, there probably will be a trade-off between good bulk quality with large grains and throughput.

6.6 NUMERICAL SIMULATIONS OF CRYSTAL GROWTH TECHNIQUES

Commercial finite element simulation tools for structural analysis in computer-aided engineering started to develop at the beginning of the seventies. Today, simulation tools are an essential part in various industry productions; see crash test simulation for automobile development or airflow simulations in the aerospace industry. As an advanced application the descriptions of whole production processes are the goal of the strategies for simulations. If these strategies are successful, computer modelling opens the opportunity to shorten development time for production facilities, to reduce the costs for the

engineering and to speed up process optimisation. In this chapter we will report on those simulation tools, various thermal models and examples of numerical simulations of silicon crystallisation processes.

6.6.1 Simulation Tools

Numerical simulation tools can be distinguished in universal and special-purpose programs. Examples of commercial universal-purpose programs are ABAQUS [72], ANSYS [73] and MARC [74] with a wide range of applications in structural analysis, thermal and fluid-flow simulations or electromagnetic field simulations. The number of special-purpose programs cannot be estimated seriously. Many universities and companies are working with specially developed software tools to obtain solutions of their specific problems. Recently, the large commercial programs both compromise and enable the user to add their specific subroutines to a program run.

The main structure of most of the simulation tools is similar: A pre-processing is designed to define the initial and boundary conditions of a simulation run and includes the generation of the simulation domain (finite element mesh) as well as a set of physical data that describes the material properties. The main-processing is normally not interactive and contains the solver of the mathematical formulations. The post-processing visualises the simulation results.

The demand for simulation tools depends on the complexity of the physical problem or on the technical process that the user wants to simulate. In general, the description of all physical relationships is reachable only in relatively simple and well-known problems. The full description of an industrial production facility by numerical simulations is not possible today, and neither is it reachable in the near future because too many details are too complex to be described by the numerical models. Therefore, the development of useful simplifications is one of the important keys to a successful simulation. This demand requires an integrated teamwork between the user of a simulation tool and the operators at the production facility and other process specialists.

Not the another important requirement is the validation of simulation results by experimental data. At least two experiments are necessary to validate simulation results concerning the process behaviour of a production facility. This means that the simulation model should be validated by measurements during a standard process and in a worst-case scenario to ensure the correctness of the results in an enlarged area of validity. Normally, these experiments are expensive and difficult to realise during a running production, but otherwise, running a non-optimised production would be quite more expensive. Anyhow, the validation of simulation results is necessary to ensure the success of the simulation method.

6.6.2 Thermal Modelling of Silicon Crystallisation Techniques

The wafer material for crystalline silicon solar cells can be divided into those from ribbon and bulk crystals. For most of wafer production processes, numerical simulations are in use to describe the thermal conditions during the crystallisation. In the case of ribbon crystals, only the EFG [75, 76] and the STR process [77] have reached a market

production. The RGS process [78] is now in preparation for a commercial production. The Cz crystal-pulling technique is the standard process for microelectronic single-crystal wafers and covers an essential part of the PV market share [79, 80]. The TriSi crystal is a new variation of this process, especially for photovoltaic applications [81]. The characteristics of ingot crystallisation can be explained by the shape of their liquid–solid interface. Anyhow, today's ingot crystallisation goes more and more towards a mostly planar solidification. For the use of numerical simulations of the Cold Wall process, see [82, 83]; for the Heat Exchange Method (HEM), see [84] and for the Solidification by Planar Interface (SOPLIN) processes, see [85, 86].

To simulate the temperature history during crystallisation, various thermal effects must be taken into account. In Figure 6.28 the scheme of thermal conditions for the ribbon growth and ingot crystallisation is presented. The biggest difference between the two is the strong variation of the cooled surface to volume relation (SV) during crystal growth. This relationship can be used to qualify the cooling behaviour of the different crystals in an equivalent surrounding. For ribbon growth SV is given as 2/ribbon thickness and for ingots as 1/ingot height. The high number for ribbon growth (e.g. SV = 66/cm) means that the surface affects the crystallisation, while the low number for an ingot geometry (e.g. SV = 0.033/cm) shows that volume effects are more important for crystallisation. By this, the SV parameter characterises the requirements for the modelling of different crystallisation techniques. In the case of bulk crystallisation, the latent heat at the liquid–solid interface must be lead away by a heat sink at the bottom of the ingot. By this, the crystallisation is propagated by a conductive heat flow through the solid ingot volume and the temperature gradients inside the volume have to be simulated with high attention. In the case of ribbon growth, heat flow by convection and radiation at the silicon surface is the dominant heat-transport mechanism to lead away latent heat and propagate the solidification. Therefore, simulation results are very sensitive to heat-transition coefficients and the emission behaviour at the ribbon surface.

Furthermore, both techniques can be distinguished into quasi-steady state and moving boundary processes. Assuming a constant pulling speed, the ribbon growth is

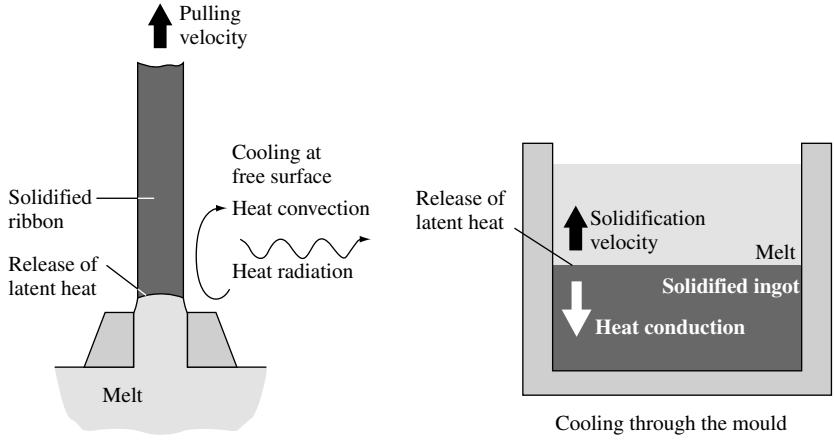


Figure 6.28 Scheme of thermal effects during ribbon growth and ingot crystallisation

characterised by a steady-state temperature field and the liquid–solid phase boundary can be modelled by a fixed-temperature boundary condition, as the silicon melting temperature of 1410°C. In the case of the ingot casting, the phase boundary moves through the crystal and the release of latent heat can be modelled by an enthalpy formulation. By this, the release of the latent heat of finite elements can be taken into account directly after their total solidification, or the fraction of latent heat must be considered for partly solidified elements [87, 88]. The importance of an accurate modelling of the release of latent heat may become more clear by estimating the crystallised volume rate in typical ingot processes to be around 9000 cm^3 per hour, which means a latent heat source of more than 8 kW at the location of the phase boundary. Pulling one 10-cm-wide ribbon, the crystallised volume rate is about 30 cm^3 per hour with a latent heat release of 0.03 kW.

The Czochralski and TriSi crystal-pulling techniques can be classified between ribbon and ingot crystallisation. The temperature profile can be assumed to be stationary and the SV parameter, given as 1/crystal diameter, lies, for example, in the range of 0.066/cm.

In general, the heat flow in silicon during crystallisation can be described by the heat-transport equation [89–91]:

$$\rho c_p \frac{\partial T}{\partial t} = \lambda \nabla^2 T + L \frac{\partial f_c}{\partial t}$$

with the silicon data:

density of solid silicon	$\rho_{(1410°C)}$	=	2.30 [g/cm^3]
density of liquid silicon	$\rho_{(1411°C)}$	=	2.53 [g/cm^3]
heat capacity	$c_{p(20°C)}$	=	0.83 [J/g K]
	$c_{p(1410°C)}$	=	1.03 [J/g K]
heat conductivity	$\lambda_{(20°C)}$	=	1.68 [W/cm K]
	$\lambda_{(1410°C)}$	=	0.31 [W/cm K]
latent heat of phase change	L	=	3300 [J/cm^3]

The time t and the temperature T are variable and result from the simulation. For the moving boundary case the solid fraction f_c becomes important. This parameter depends on the finite element temperature and varies between zero for a completely liquid finite element and one for a solid element.

Additionally to these material properties and the heat flow mechanisms in the silicon material, the description of the internal furnace construction must be taken into account to perform simulations of crystallisation facilities. This includes the geometrical description and material properties of the internal set-up as well as the radiative heat exchange with heaters and cooling facilities.

6.6.3 Simulation of Bulk Silicon Crystallisation

As an example of the temperature simulation of silicon ingot crystallisation, the SOPLIN casting technique is selected. To simulate this process, a finite element mesh of about 230 000 elements was built to describe the furnace geometry. This mesh includes the silicon ingot, the mould, all insulation materials and active heating and cooling facilities,

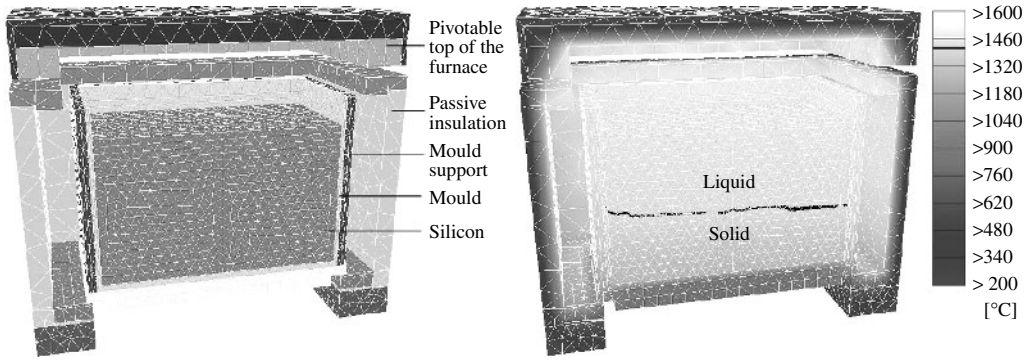


Figure 6.29 Finite element geometry of an ingot casting furnace and simulated temperature distribution during a reference process. The liquid–solid interface is marked by the black line

as shown in Figure 6.29. Because of confidentiality agreements with the industry, the heating and cooling systems are not shown in detail in this figure. All heat conductance and capacity effects as well as the non-stationary release of latent heat are taken into account. All material contact regions between silicon, mould or insulation materials are modelled by heat flow–resistance parameters. To describe the heat flux by radiation inside the furnace, a view-factor model is included in the software. All material data are treated in their temperature dependency and all the internal control systems of the furnace are added to the simulation software.

To start one simulation run, only the cooling water temperature and the time-dependent process control information are necessary as input data, as they are entered in the crystallisation furnace. Output from one calculation is the three-dimensional temperature history in the furnace, beginning after pouring the melt and ending with a homogeneous temperature of about 300°C inside the ingot. This calculation needs less than 6 h on a common one-processor workstation.

In Figure 6.29, an example of the temperature distribution during a reference process is shown in the middle, cut through the furnace. The liquid–solid interface is marked by the melting temperature isotherm. The solidification front is mostly flat, and a slight non-symmetry is caused by the specific construction of the heating system. These simulation results are verified in an experimental crystallisation furnace with good agreement to the measurement in the ingot volume during crystallisation.

In general, the shape of the solidification front is controlled by the lateral heat flux, while the vertical heating and cooling conditions control the solidification velocity. To investigate these general reflections for the described furnace, variations of the process control were simulated. In Figure 6.30, two variations are presented. By a 30% raise of heating power at the side walls of the ingot, the shape of the solidification front becomes more convex. Otherwise, a reduction of heating power by about 20% turns the solidification front to a more concave shape. Additionally, to this more or less predictable effect, simulation results show an increase in the solidification time for the convex crystallisation of 44% and a 30% reduced processing time for the concave solidification. Both effects are due to the total varying power input in the furnace. These simulation results enable

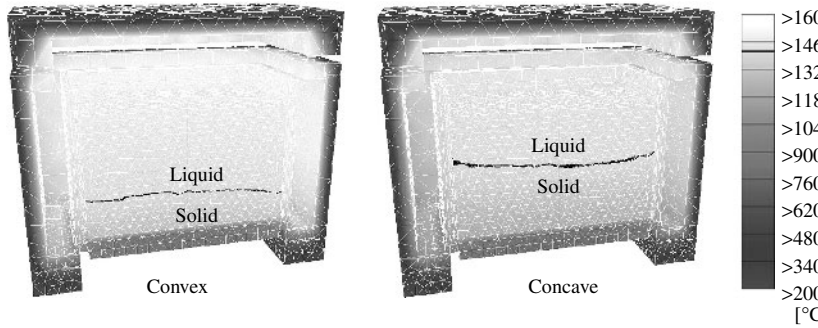


Figure 6.30 Examples of convex and concave liquid–solid interfaces due to the variation of side wall heating power. Both pictures are taken at the same process time

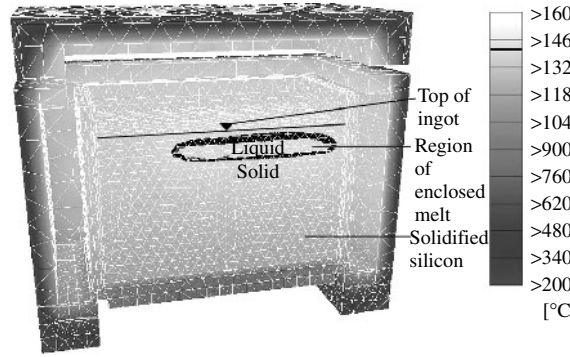


Figure 6.31 Simulation result representing a remarkable decrease of heating power at the top region of the ingot. By this, the solidification time is reduced to half, but solidification ends with an inclusion of silicon melt

the furnace operator to find the balance between material quality, which is known to be high in the case of planar solidification, and process economy.

In Figure 6.31, simulation results are shown, representing a noticeable reduction of heating power at the ingot top. By this, the solidification velocity can be speeded up and the time for solidification is reduced to half. However, in the simulated case study, the solidification ends with an encapsulation of the melt by solidified silicon. Because of the 10% higher density of liquid silicon with respect to the solid phase, this process scenario causes a burst out of melt from ingots volume. This can lead to a crack in the mould and to a damage of the furnace. These case-study simulations can find worst-case process conditions that must be avoided in production. For more simulation results of the SOPLIN process, see [92–94].

6.6.4 Simulation of Silicon Ribbon Growth

As a second example of silicon crystallisation processes, the RGS is taken. The basic idea of this process is the de-coupling of the pulling direction of substrates on which silicon

solidifies and the solidification direction of the silicon itself, as shown in Figure 6.32. By this, a very high production rate of one wafer per second is realisable. For this process numerical simulations were performed describing the crystallisation of the silicon ribbon in further detail. This simulation is realised by a phase-field approach [95]. In Figure 6.33 two nucleation states of the silicon on the substrate are compared by their temperature field in two-dimensional simulations. In the first case a supercooled region in front of the tip of the growing crystal leads to a more dendritic growth mode of the crystal, because the liquid–solid interface is morphologically non-stable. In the second crystallisation mode,

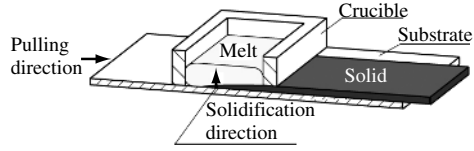


Figure 6.32 Scheme of the RGS process. The latent heat is removed through the substrate. By this, solidification is propagated vertical to the substrate and is de-coupled from substrates' pulling direction

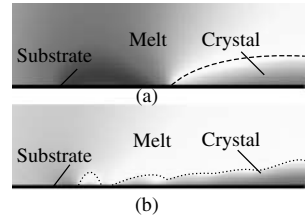


Figure 6.33 Simulated temperature profile on the RGS substrate. Light grey scales indicate high temperatures. The liquid–solid interface is marked with the dotted line. Unstable crystal growth into a supercooled melt at the tip of the ribbon. Nucleation of new grains limits the supercooling and leads to a stable columnar grain growth

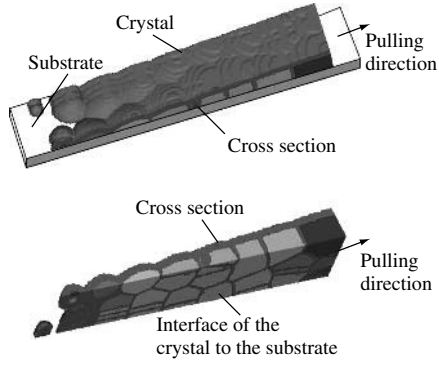


Figure 6.34 Simulation results of the growth of silicon grains on the RGS substrate during solidification. Different grains are marked by different grey scales. The liquid–solid interface is marked by a darker grey scale and envelops the grains. For a better visibility, the melt is not shown in this figure

the supercooling decreases owing to a nucleation of new grains on the substrate surface, which leads to a more columnar growth of the silicon sheet. Both crystallisation modes depend on the surface of the substrate and on the heating power controlled temperatures of the substrate and the melt. Numerical simulations allow investigating this crystal-growth tendency as well as the temperature field at the contact region of the ribbon on the substrate. In Figure 6.34 an example of the simulation of single silicon grain growth on the substrate is given [96]. In this way, numerical simulations can study the grain growth under various temperature conditions and grain-selection mechanisms of silicon crystals.

6.7 CONCLUSIONS

At the present time, the PV industry relies on solar cells made on crystalline silicon wafers, which provide around 90% of the total PV power installed. It is expected that monocrystalline and multicrystalline solar cells will continue dominating the industry for the next 10 years.

With rejects from the microelectronic industry as feedstock, the PV industry grows monocrystalline ingots by the Czochralski technique. Owing to more relaxed specifications than in microelectronics, the throughput of PV Cz pullers can be increased and still produce high-quality silicon, allowing the achievement of 15 to 17% efficient solar cells.

Tri-crystalline silicon (tri-Si) can be grown in standard production Cz growers using a quasi-continuous pulling with multiple recharging with high productivity and feedstock usage. Tri-Si allows slicing of ultra-thin wafers with higher mechanical yield than monocrystalline Si and obtaining solar cells of similar performance.

Multicrystalline Si can be manufactured at a lower cost than monocrystalline Si, but produces less efficient cells, mainly owing to the presence of dislocations and other crystal defects. With the introduction of new technologies, the gap between multicrystalline and monocrystalline solar cells is reducing.

Si ingots are sliced into thin wafers with multi-wire saws, with throughputs of about 500 to 700 wafers per day and per machine. Sawing is responsible for high material losses, and amounts to a substantial part of the wafer production cost. Understanding the microscopic processes of wire sawing allows optimising the technique and improving the sawing performance.

Silicon ribbon wafer/foil technologies have matured in the past decade to where they are serious contenders for competing on a scale equal to that of conventional silicon wafers. Several ribbon technologies have already demonstrated robust and reproducible processes, which have been scaled up to megawatt levels. The next round of expansion will probably reach the 50 to 100 MW factory size for individual technologies within 5 years. Factories of this scale will require considerable development of automated equipment and infrastructure in addition to continuous improvement on the basic process control and material quality. EFG and SF ribbon technologies are most notably in a position today to manufacture wafers on this scale and lead the anticipated growth of the photovoltaic industry.

During the last decade, computer power has been increasing strongly and there is a high progress in the modelling of physical phenomena and in the development of

simulation tools. By this, computer simulations become a powerful tool in science and industrial applications. The simulation results of industrial crystallisation processes that are shown and the detailed study of the crystallisation mode by numerical simulations are some examples of the possibilities today. These numerical simulations offer a wide range of possibilities to increase the knowledge about the basic physics of crystallisation and technical processes. One insistent demand on computer simulations is to close the gap between science and engineering to get a closer picture of reality.

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