Reconfigurable Self-Timed Dataflow Accelerator

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Overview

Talk 12.2.2
Thursday 16:30
Room Konf. 6

- Presented in D.Sokolov et al: "Reconfigurable Asynchronous Pipelines: from Formal Models to Silicon", DATE'18.
- Pipelining is a widely used approach to the design of high-throughput computation systems.
- Dynamic reconfiguration of dataflow pipelines enables different handling of different data items.
- Asynchronous pipelines exhibit average case performance as opposed to worst case in synchronous pipelines.
- Reconfigurable asynchronous pipelines need a formal behavioural model and design automation support.
- We propose Dataflow Structures (DFS) for modelling asynchronous pipelines, present Workcraft design automation for DFS, and demonstrate the overall design methodology by implementing ASIC accelerator for Ordinal Pattern Encoding (OPE).

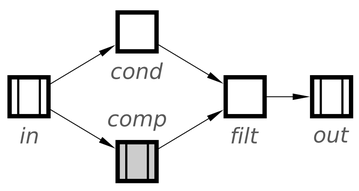
Dataflow Structures Model

DFS is a formal behavioural model for asynchronous pipelines with spread-token data propagation semantics. Graphically DFS is represented as a directed graph of the following nodes:

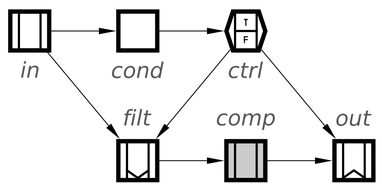
static nodes:
- logic — models evaluation combinational components
- register — models data latching in sequential components

dynamic extension:
- control — associates a data token with *True* or *False* value
- push — if controlled by *True* token → operates as a register, if controlled bu *False* token → consumes data token
- pop — if controlled by *True* token → operates as a register, if controlled bu *False* token → produces *fake* token

Example: conditional application of computationally expensive operation:

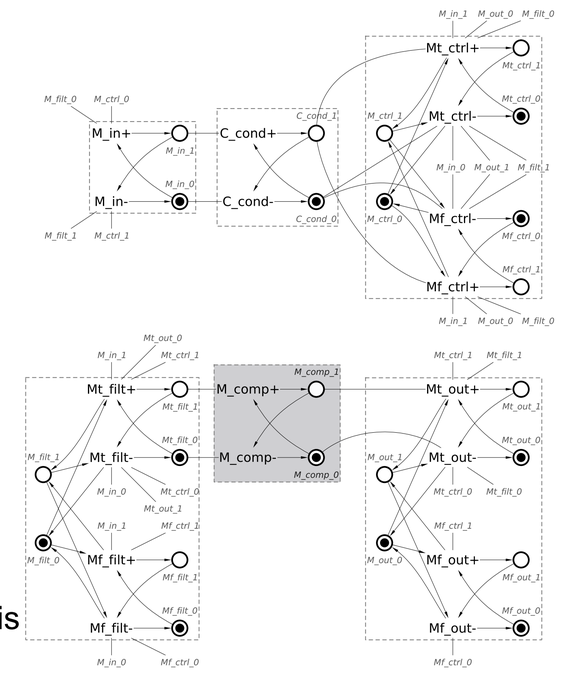


- DFS model with static nodes



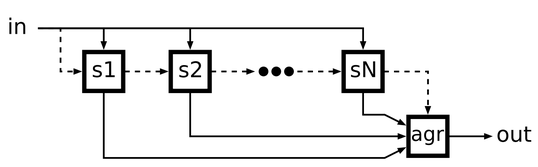
- DFS model with dynamic extension

Petri nets translation:
- simulation
- verification
- performance analysis



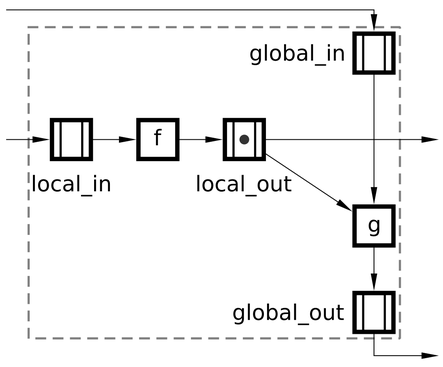
- Underlying Petri net semantics

Design of Static and Reconfigurable OPE Pipelines

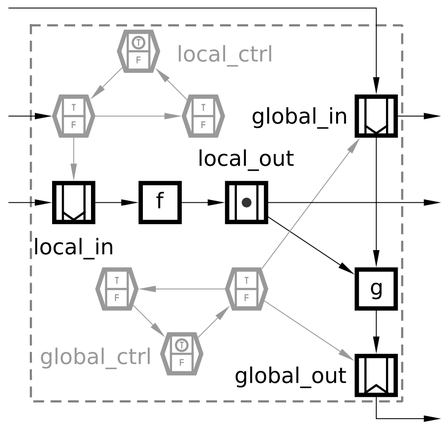


- N-stage OPE pipeline

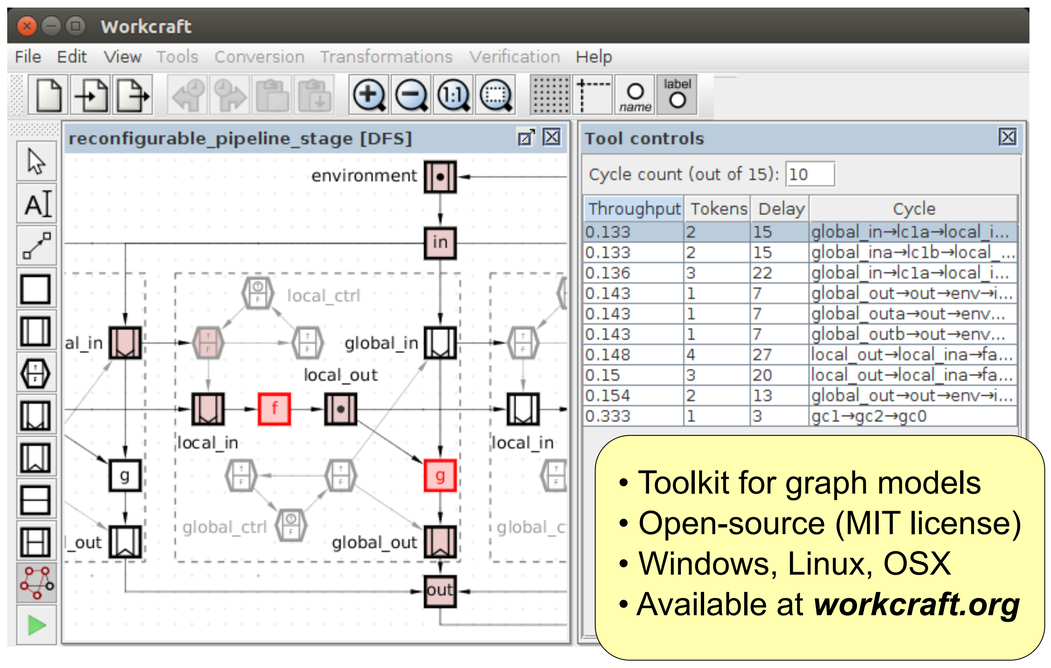
N-stage OPE pipeline ranks the last N items in an incoming data stream. Its stages can be implemented either in static or reconfigurable style.



- Static pipeline stage



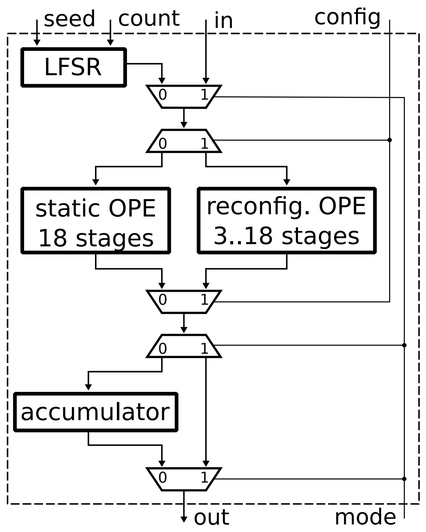
- Reconfigurable pipeline stage



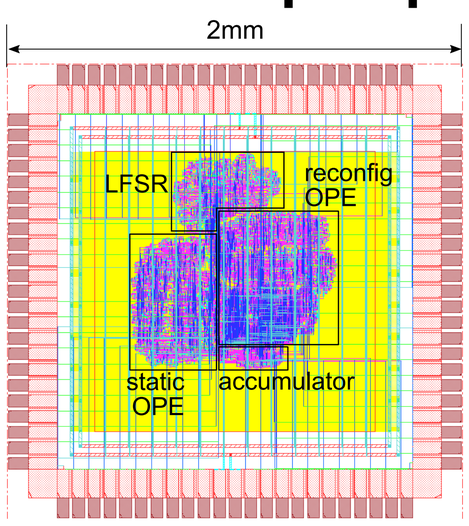
- Toolkit for graph models
- Open-source (MIT license)
- Windows, Linux, OSX
- Available at ***workcraft.org***

- Formal verification and performance analysis of DFS in Workcraft

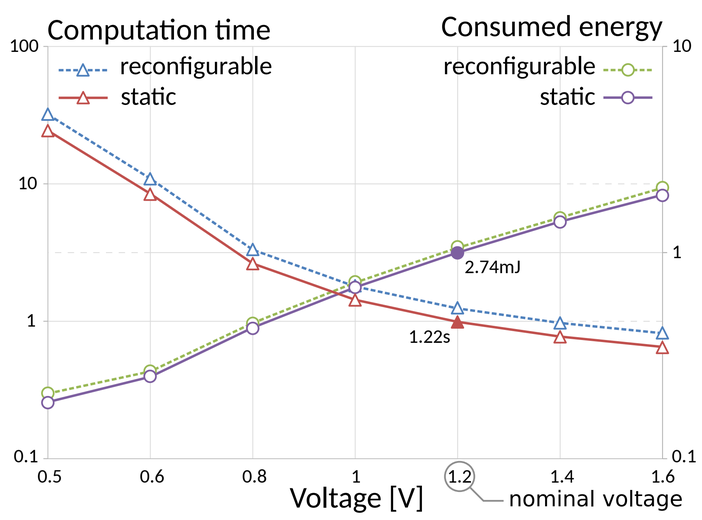
OPE Chip Implementation and Measurements



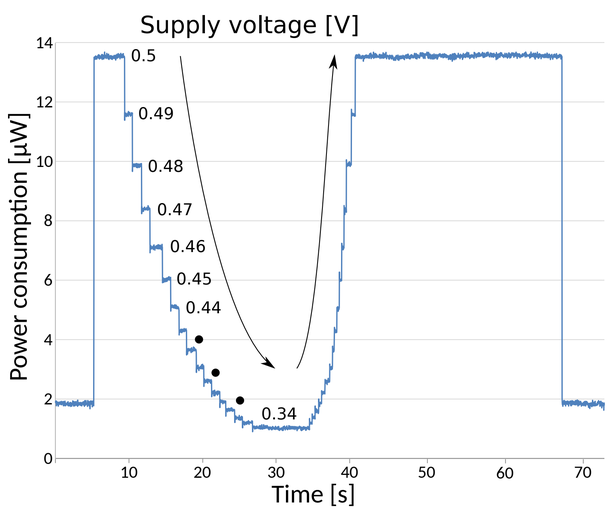
- High-level chip structure



- Floorplan (TSMC 90nm)



- Performance under different voltages



- Resilience to voltage variation

EPSRC Engineering and Physical Sciences Research Council

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SElf-timed DATapath synthEsis (SEDATE), Asynchronous design for Analogue electronics (A4A)

Newcastle University