

Formal Methods for Space Electronics

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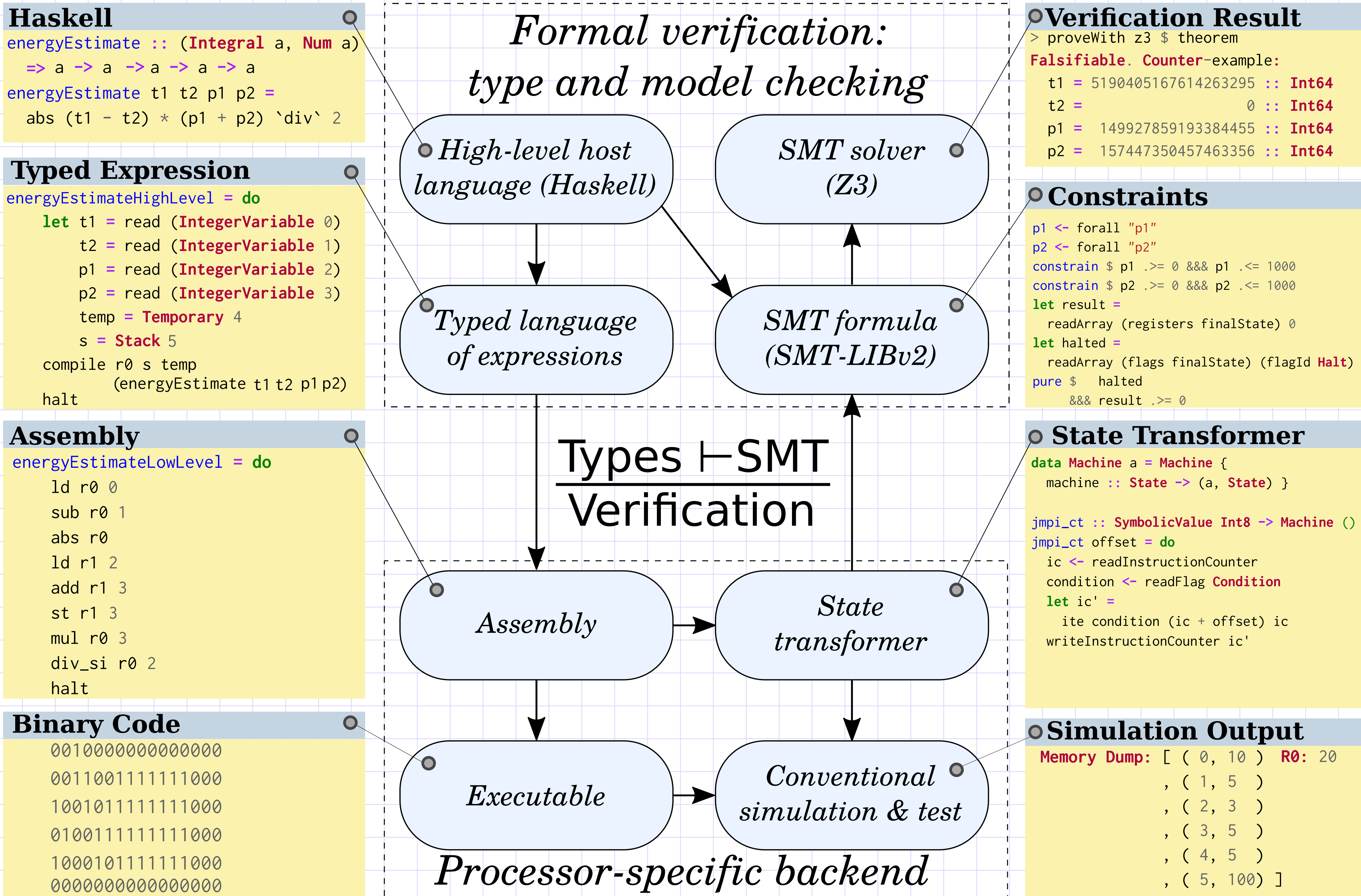
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Motivation

Verification of functional correctness of control programs is an essential task for the development of space electronics; it is difficult and time-consuming and typically outweighs design and programming tasks in terms of development hours. We present a verification approach designed to help engineers reduce the effort required for formal program verification.

The approach uses a **metalanguage** to describe the semantics of a program as a **state transformer**, which can be compiled to multiple targets for the purpose of verification and code generation.



Conclusion

The presented approach has been validated by developing a metalanguage for a processing core designed for space missions, defining a set of high-level programming constructs on top of the metalanguage, and implementing compilation pipelines for program execution, verification and code generation.

Future Work

- **Dependently-typed metalanguage and assembly** Both microarchitecture-level semantics and instruction set architecture level modelling language may benefit from more advanced type-driven verification via dependent types.
- **Hardware synthesis backend** To convey the model's verification power down to the bare metal, we may implement a verified translation from the state-transformer metalanguage to a hardware description language to petrify the semantics and turn it into silicon.

Related Work

- **SAIL** "Detailed Models of Instruction Set Architectures: From Pseudocode to Formal Semantics." Alasdair Armstrong et al., Automated Reasoning Workshop, 2018.