Design Rules Verification Report

Filename : C:\Users\Public\Documents\Altium\PCB_FINAL_SIM\Final_PayloadPCB.PcbD

<div align="right">

Warnings 0
Rule Violations 0

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Warnings

Total	0

Rule Violations

Clearance Constraint (Gap=0.254mm) (Disabled)(All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	0