QoS_DC

DC stage module to decode 4 new instructions in ISA:

1. ***en_parity_st***: Enable parity encoding
2. ***dis_parity_st***: Disable parity encoding
3. ***set_data***: Register protected data range and reference LUT
4. ***chk_ld***: Check the data using parity value

Gen_ parity

EX stage module, implement following operation:

1. ***parity*** in MEM stage is activated in case the stored data lies in the protected range

QoS_EX

EX stage module, implement following operation:

1. ***chk_ld_ex***: Activated by ***chk_ld***, verify parity bit of the incoming data. In case of missmatch, activate ***chk_ld_mem*** in MEM, otherwise activate ***chk_ld_wb_correct***

QoS_ MEM

MEM stage module, implement following operations:

1. ***parity***: Main parity encoding logic. Each 32 bits data generates 1 bit parity. Encode 32 words as 1 word parity, activate ***partiy_st*** logic in WB stage 32 bits parity are ready
2. ***chk_ld_mem***: When a parity missmatch is detected, get the address of corresponding LUT element and issue memory read. Activate ***chk_ld_wb_wrong*** in WB stage

QoS_WB

WB stage module, implement following operations:

1. ***parity_st***: Store 32 bits parity as one data word into data memory
2. ***Chk_ld_wb_wrong***: In case of parity missmatch, return the reference value from LUT
3. ***Chk_ld_wb_correct***: No parity missmatch, return the input value from instruction

QoS_ Registers

Special registers in RegisterFile,

1. set and re-set the processor state for load check.
2. Record the location for LUT and runtime offset to access the reference data.