Colorado State University

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Fort Collins, CO 80523

From: Matthew George, Lab 5 March 11, 2022, 11:00pm

Subject: Lab 5

To the Director of Research and Development,

The purpose of this research task was to create a 4-bit multiplier and combine it with our previous research and development project, the adder/subtractor, to make an Arithmetic Logic Unit (ALU).

The ALU was implemented by creating two separate logic symbols, the multiplier and the adder/subtractor, and then controlling output with two tri-state buffers. The schematic was then implemented and tested using the DEO board. **Figure 1** shows the complete Arithmetic Logic Unit. Note the addition/subtraction block and the multiplication block. These symbols were created using the schematics in **Figure 2** and **Figure 3**, respectively.

In figure 3, I have highlighted the longest path of signal propagation on the multiplier, where a signal will pass through 9 gates. Assuming that each gate takes 10ns, the worst-case estimate for multiplication time is 90ns.

The circuit was successfully implemented and tested using the DEO board.

Matthew George

Figure 1: Complete Arithmetic Logic Unit

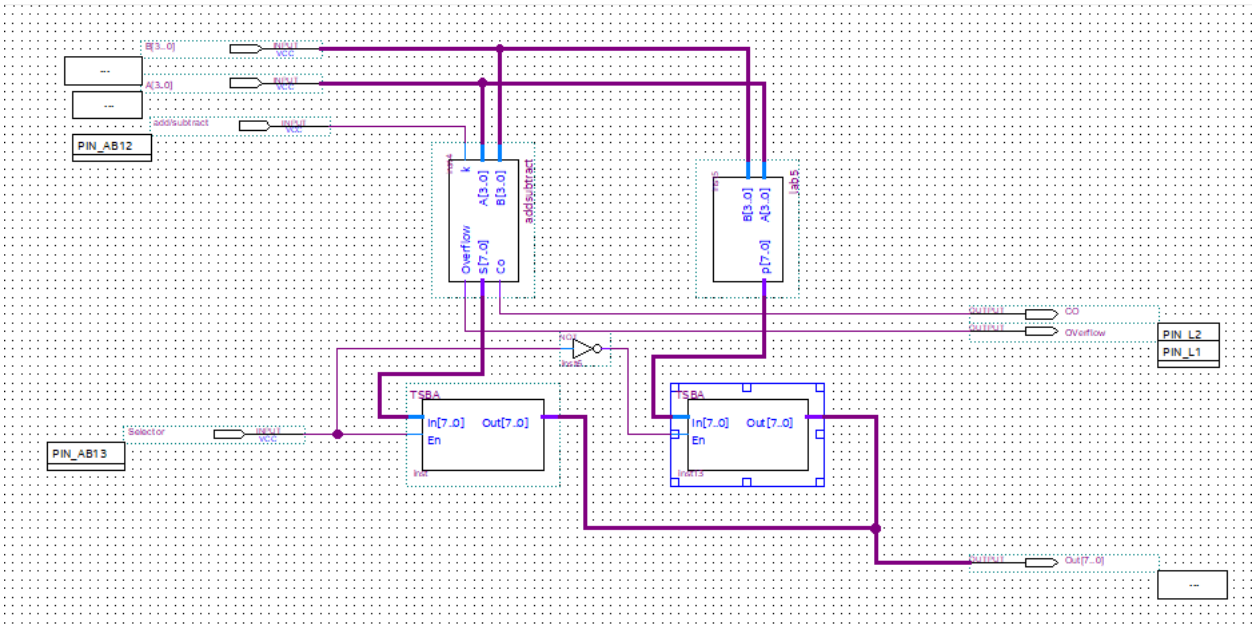

Figure 2: Adder/Subtractor

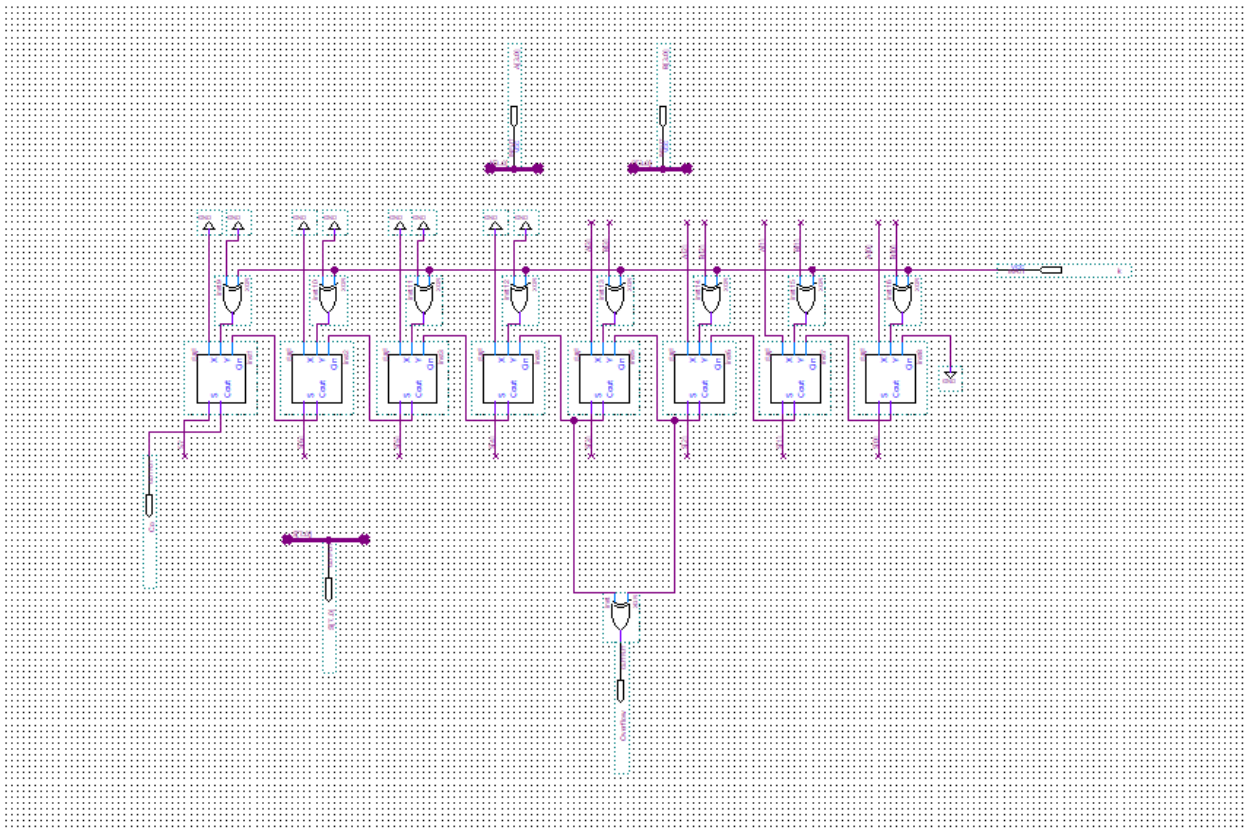

Figure 3: Multiplier With Longest Path of Signal Propagation