Colorado State University

Department of Electrical Engineering

Fort Collins, CO 80523

From: Matthew George, Lab 3 Feb 27, 11:00pm

Subject: Lab 4

To the Director of Research and Development,

The purpose of this research task was to complete the design and implementation of an 8-bit adder and subtractor using a string of full adders.

Using Quartus and limited to the use of AND, OR, XOR, and NOT gates, I designed a schematic and analyzed the implementation of the final product using a truth table and a functional simulation.

The first step was to build a logic component for the add and carry step, otherwise known as the full adder. The full adder sums a_n and b_n using an XOR gate. If both a_n and b_n are equal to one, then the XOR gate returns a zero and the c_{out} from that full adder is passed to the next full adder in the sequence. There are eight total full adder components strung together which means that the adder/subtractor is capable of returning sums of up to 8 bits in length. An addition/subtraction input pin switches the operation being performed on the binary numbers. If the subtraction pin is equal to one, then two's-complement addition is used to find the difference between the first number and the second number.

A schematic for the full adder can be found on the following page in **Figure 1. Figure 2** shows the completed schematic for the adder/subtractor with a string of eight full adders. **Table 1** is a truth table for the full adder component.

Implementation of this design was a success and a demonstration video is included displaying the results of the completed project.

Matthew George

Research and Development at Banana Electronics

Figure 1: Full adder schematic

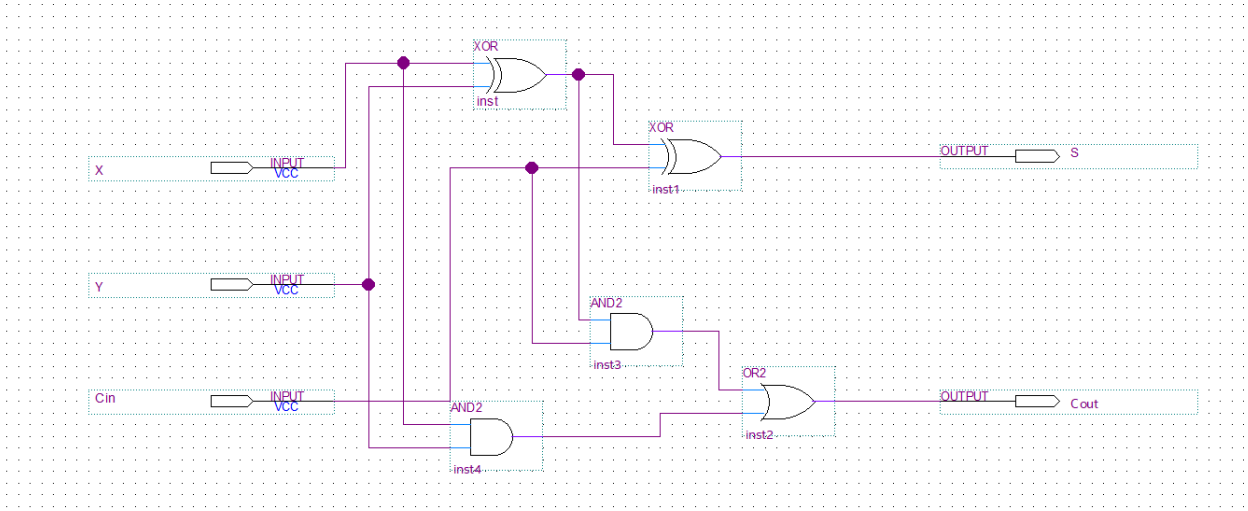

Figure 2: Binary adder/subtractor complete schematic

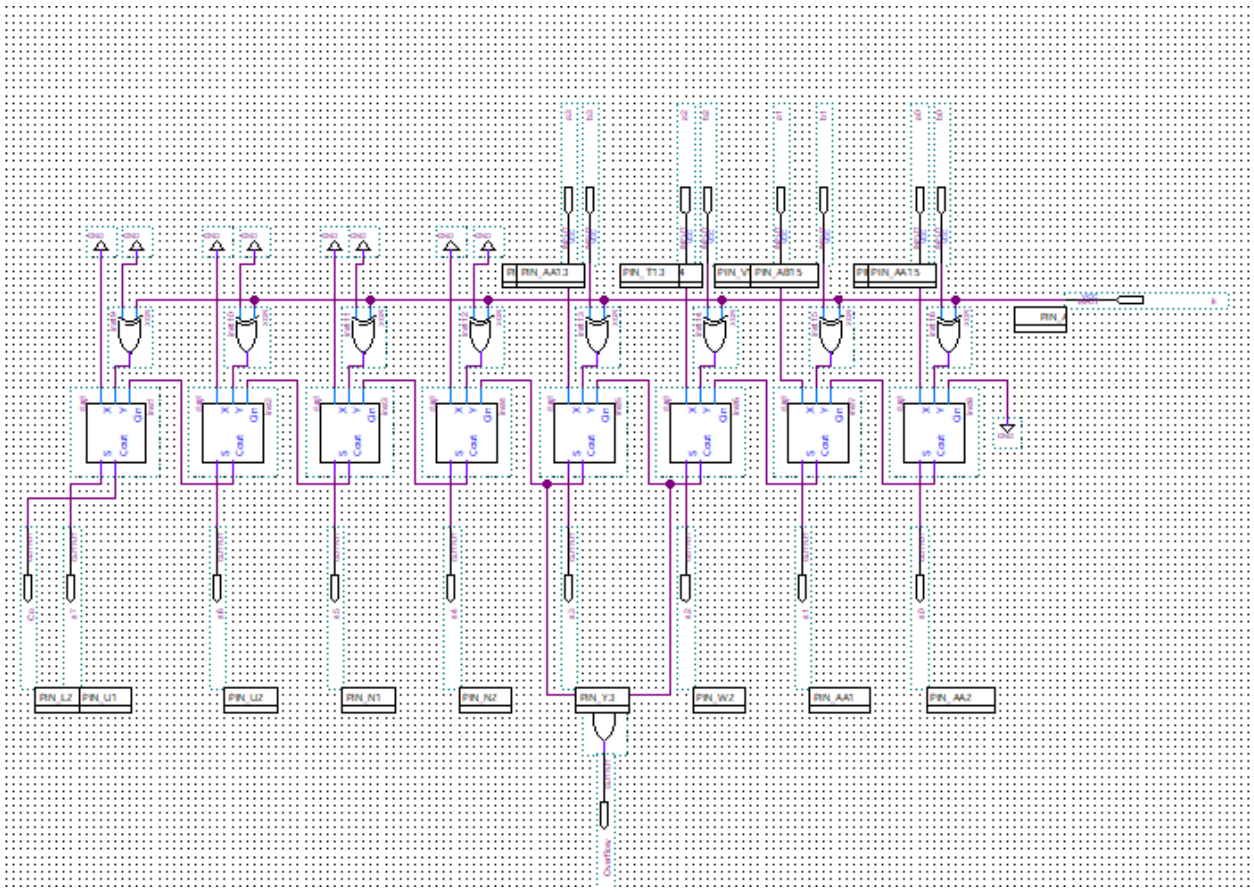

Figure 3: waveform output for adder/subtractor

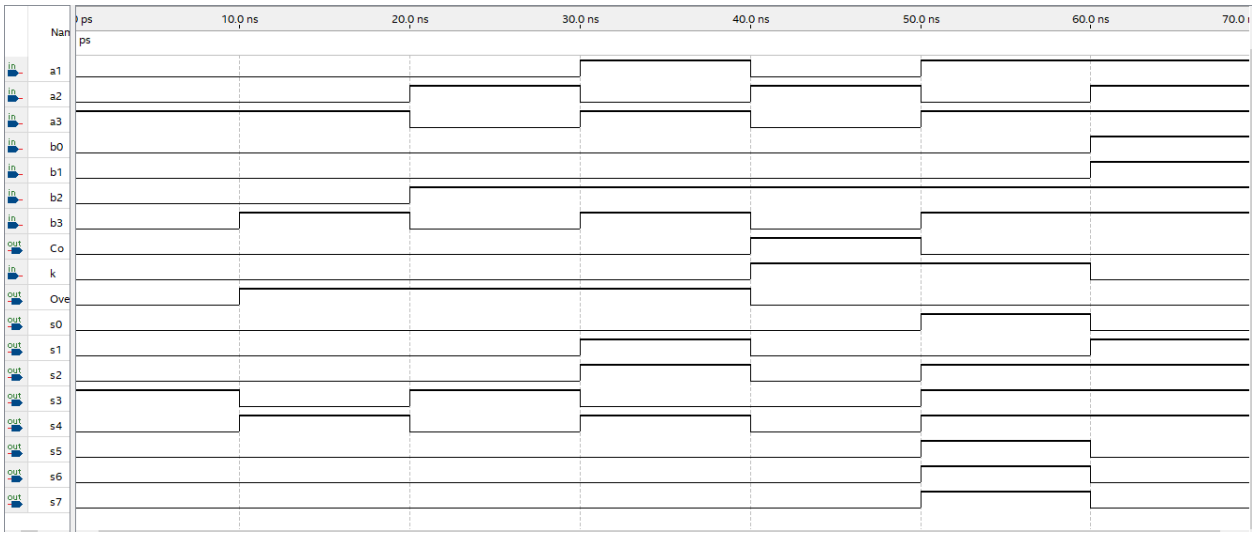

Table 1: truth table for full adder component

X	Y	Cin	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1