VHDL multiplex 8 para 1

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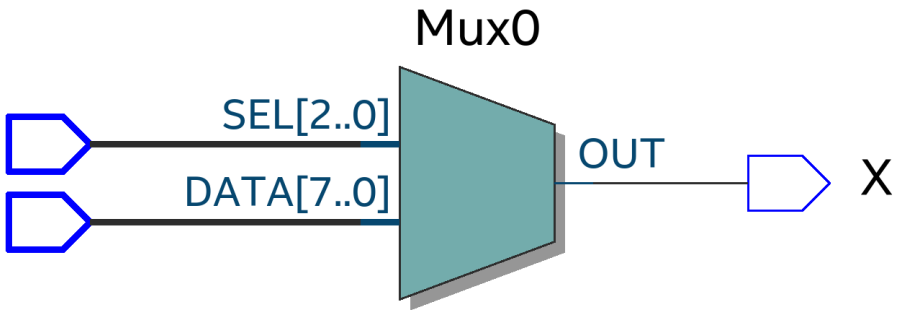
--
-- Autor: George Maximo, Data: 01/10/2019 | versao 1.0.0
--

	library IEEE;
	use IEEE.std_logic_1164.all;

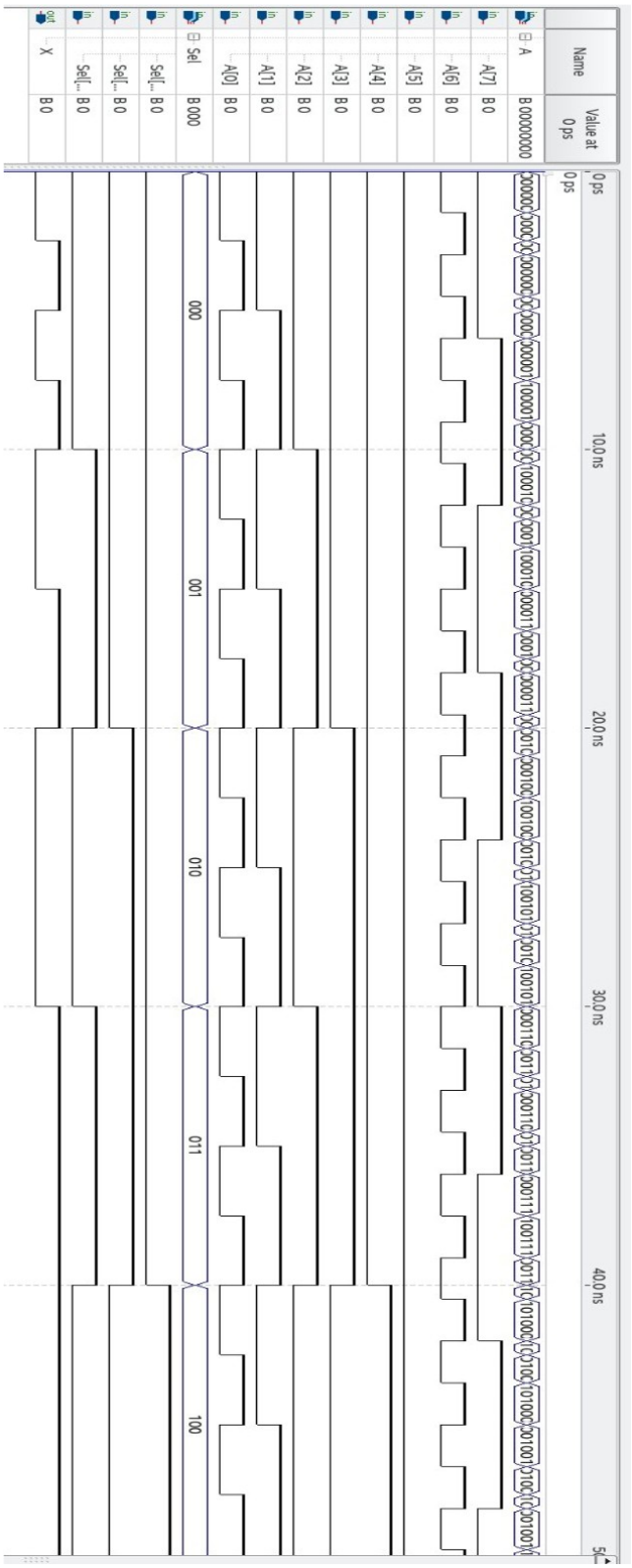
	entity multiplex8_to_1 is port
	(
		A	:	in std_logic_vector(7 downto 0);		--entradas
		Sel	:	in std_logic_vector(2 downto 0);		--selecao
		X		:	out std_logic
	);
	end multiplex8_to_1;

	architecture hardware of multiplex8_to_1 is
	begin
		with Sel select
			X <= A(0) when "000",
	   A(1) when "001",
	   A(2) when "010",
	   A(3) when "011",
	   A(4) when "100",
	   A(5) when "101",
	   A(6) when "110",
	   A(7) when "111";

	end hardware;
```



Saída waveforme mux 8 para 1:



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-- VHDL demux 1 para 8
-- George Maximo de Sousa

library IEEE;
use IEEE.std_logic_1164.all;


entity demux1_8 is port
(
	E		:	in std_logic;
	X		:	out std_logic_vector(7 downto 0);
	Sel	:	in std_logic_vector(2 downto 0)

);
end demux1_8;

architecture hardware of demux1_8 is
begin
process(Sel, E)
begin

	case Sel is
		when "000" => X(0) <= E;
		when "001" => X(1) <= E;
		when "010" => X(2) <= E;
		when "011" => X(3) <= E;
		when "100" => X(4) <= E;
		when "101" => X(5) <= E;
		when "110" => X(6) <= E;
		when "111" => X(7) <= E;
	end case;
end process;
end hardware;
```

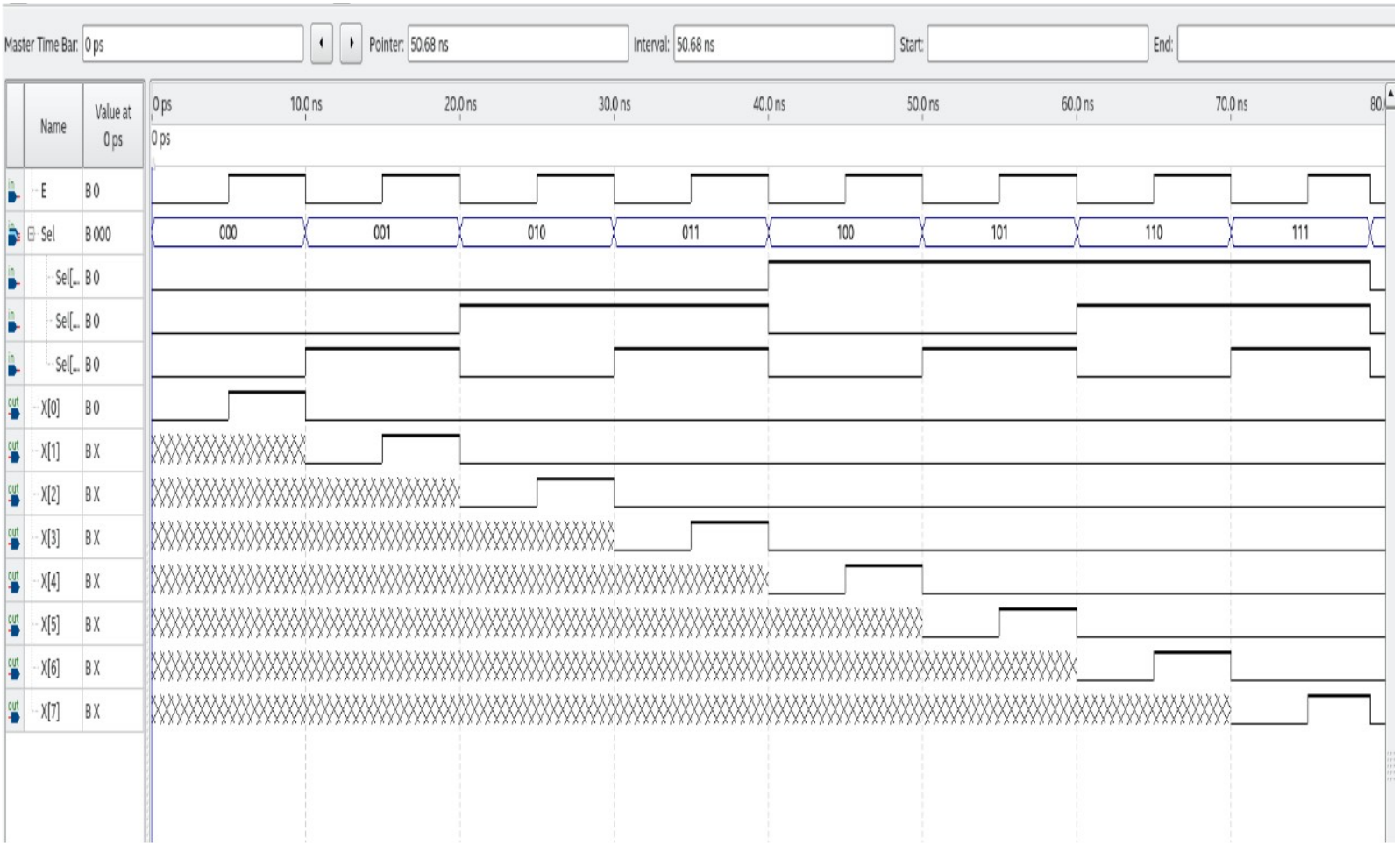
Master Time Bar: 0 ps
Pointer: 50.68 ns
Interval: 50.68 ns
Start:
End:
Name
Value at 0 ps
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
E
Sel
Sel[...
Sel[...
Sel[...
X[0]
X[1]
X[2]
X[3]
X[4]
X[5]
X[6]
X[7]
000
001
010
011
100
101
110
111