
Overview

Design Goal:

Create from scratch ¹ an 8-bit Turing complete computer.

Timeline:

May: Design decisions	Logic family Proof of concept logic gates What are the macro components I need?
June: Logisim macro components, Breadboard macro components	
July: Full Logisim computer, Breadboard macro components	
August: Complete design, Manufacturing	

Logic Families

	Pros	Cons
Resistor Transistor Logic (RTL)	Incredibly simple BJT transistors Inexpensive components Static electricity resistant	Power inefficient Lots of components needed Slow switching speed Susceptible to noise Bad fan out
Diode Transistor Logic (DTL)	BJT transistors Inexpensive components Static electricity resistant Handles noise well	Power inefficient More complicated than RTL Lots of components needed Slow switching speed
Transistor Transistor Logic (TTL)	Power efficient BJT transistors Inexpensive components Static electricity resistant	Ideally uses multiple emitter transistors More complicated than RTL Lots of components needed
Complementary Metal Oxide Semiconductor Logic (CMOS)	Incredibly power efficient Very fast switching speed	Static electricity susceptible Expensive components Complicated logic gates

¹ I will not be manufacturing resistors and transistors.

There are of course more logic families, these are simply the most common and have differences that will be relevant to the project. Due to the low clock speed of the final computer, I don't have to worry too much about transistor saturation².

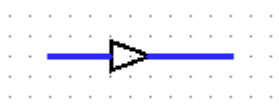
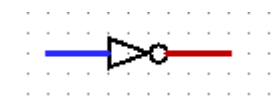
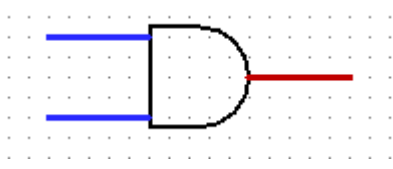
After screening³ I cut DTL for the more complicated gate design and CMOS for the price and complexity again. Comparing TTL and RTL, RTL's simplicity won out for me. I do not have access to an oscilloscope currently and I want to minimize the amount of high-speed troubleshooting I need to do.

Digital Logic

Logic Gates

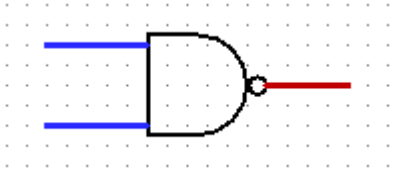
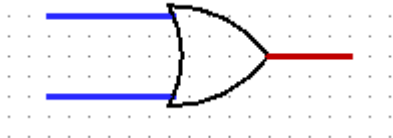
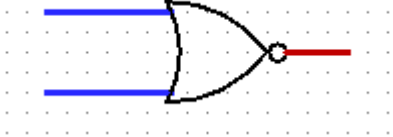


The fundamental building blocks of digital logic, these simply take in one or more input and give back one output.

Logic gates are commonly shown as block diagrams, which are summarized below:

	Block Diagram	Truth Table															
BUFFER		<table><tr><th>IN</th><th>OUT</th></tr><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr></table>	IN	OUT	0	0	1	1									
IN	OUT																
0	0																
1	1																
NOT		<table><tr><th>IN</th><th>OUT</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table>	IN	OUT	0	1	1	0									
IN	OUT																
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1	0																
AND		<table><tr><th>A</th><th>B</th><th>OUT</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	A	B	OUT	0	0	0	1	0	0	0	1	0	1	1	1
A	B	OUT															
0	0	0															
1	0	0															
0	1	0															
1	1	1															

² If your project is going to run at a very high clock speed, or you care about transistor saturation you should look at Schottky TTL.

³ Yes, we're using APSC 100-101 terminology.

NAND		<table> <tr><th>A</th><th>B</th><th>OUT</th></tr> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </table>	A	B	OUT	0	0	1	1	0	1	0	1	1	1	1	0
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OR		<table> <tr><th>A</th><th>B</th><th>OUT</th></tr> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </table>	A	B	OUT	0	0	0	1	0	1	0	1	1	1	1	1
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NOR		<table> <tr><th>A</th><th>B</th><th>OUT</th></tr> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </table>	A	B	OUT	0	0	1	1	0	0	0	1	0	1	1	0
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XNOR		<table> <tr><th>A</th><th>B</th><th>OUT</th></tr> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </table>	A	B	OUT	0	0	1	1	0	0	0	1	0	1	1	1
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0	1	0															
1	1	1															

Boolean Algebra

Boolean algebra allows us to compute what will happen in a more complex circuit. All of the logic gates above can be represented through 4 mathematical operations:

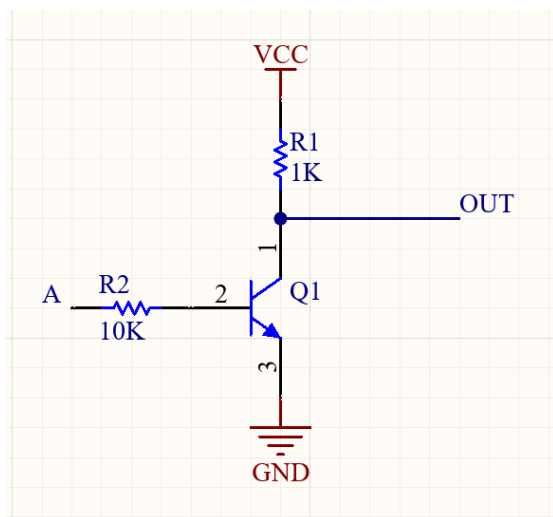
NOT	\bar{A}	Inverts the value of A	IN	OUT
			0	1
			1	0

OR	$A + B$	Returns 1 if either A or B is 1	A	B	OUT
			0	0	0
			1	0	1
			0	1	1
			1	1	1
AND	AB	Returns 1 if both A and B are 1	A	B	OUT
			0	0	0
			1	0	0
			0	1	0
			1	1	1
XOR	$A \oplus B$	Returns 1 if only A or B is 1	A	B	OUT
			0	0	0
			1	0	1
			0	1	1
			1	1	0

We can combine these operations to get any of the logic gates above.

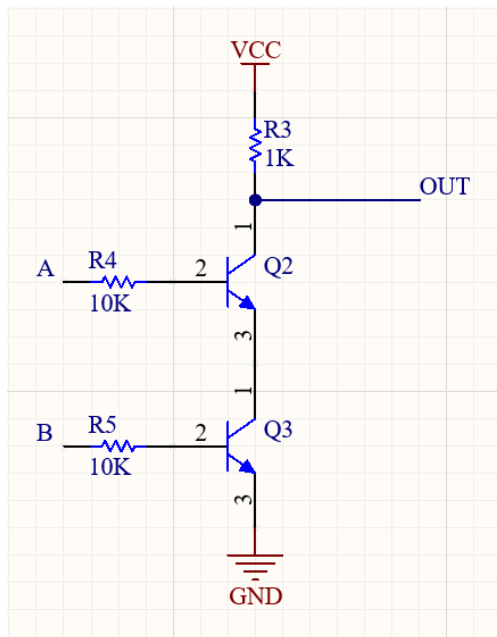
RTL Logic Gates

NOT



- 1 NPN Transistor
- 1 10K Resistor
- 1 1K Resistor

NAND

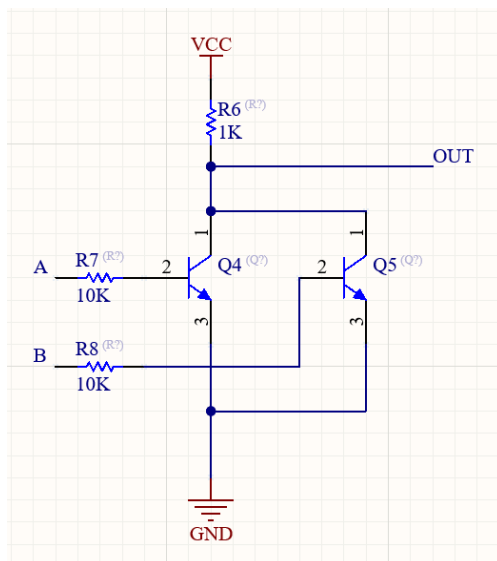


2 NPN Transistors

2 10K Resistors

1 1K Resistor

NOR

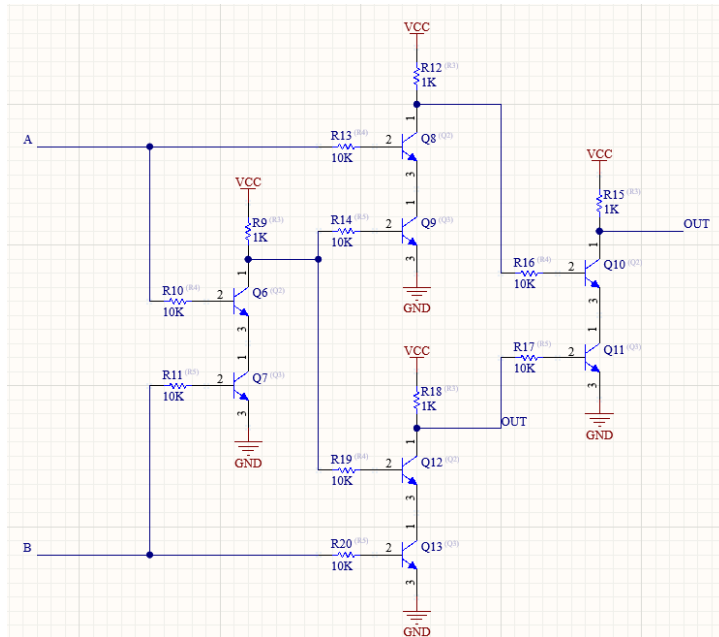


2 NPN Transistors

2 10K Resistors

1 1K Resistor

XOR (Find a more efficient circuit)



8 NPN Transistors

8 10K Resistors

4 1K Resistors

<https://www.youtube.com/watch?v=nB6724G3b3E>