Processor Simulator

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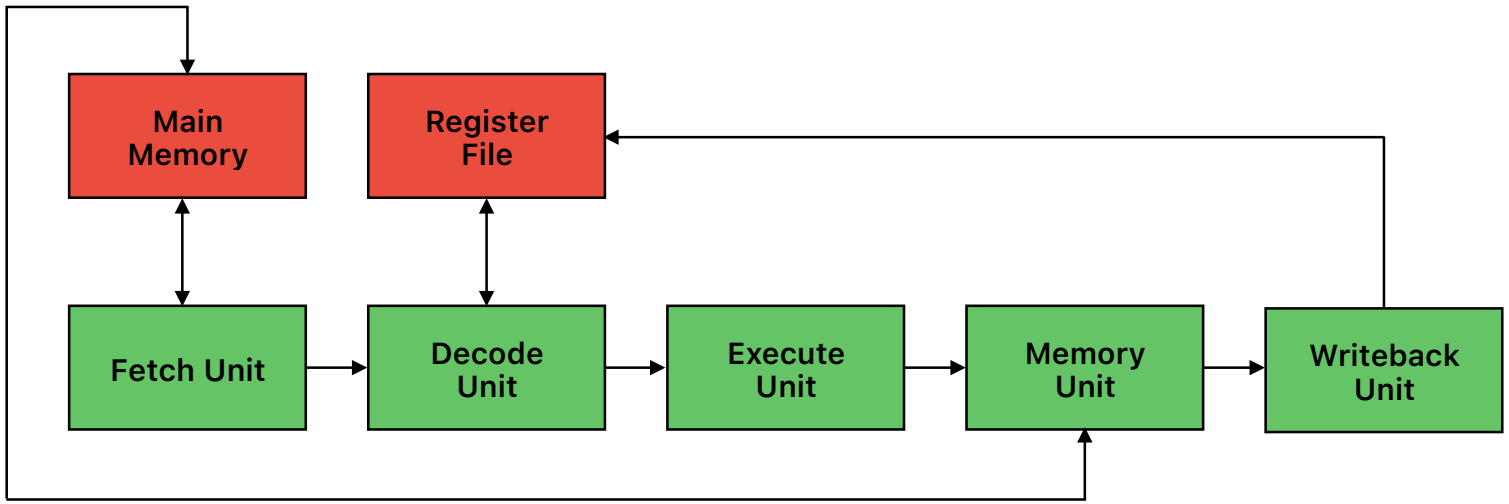
23rd February 2023

High-Level Architecture Diagram



Features

- Non-pipelined and scalar
- Five-stage cycle: fetch, decode, execute, memory, writeback
- Implements the RV32I base integer instruction set, except for the FENCE, ECALL, and EBREAK instructions
- Operation of each unit is dictated by control signals produced by the decode unit

Euclidean