Processor Simulator

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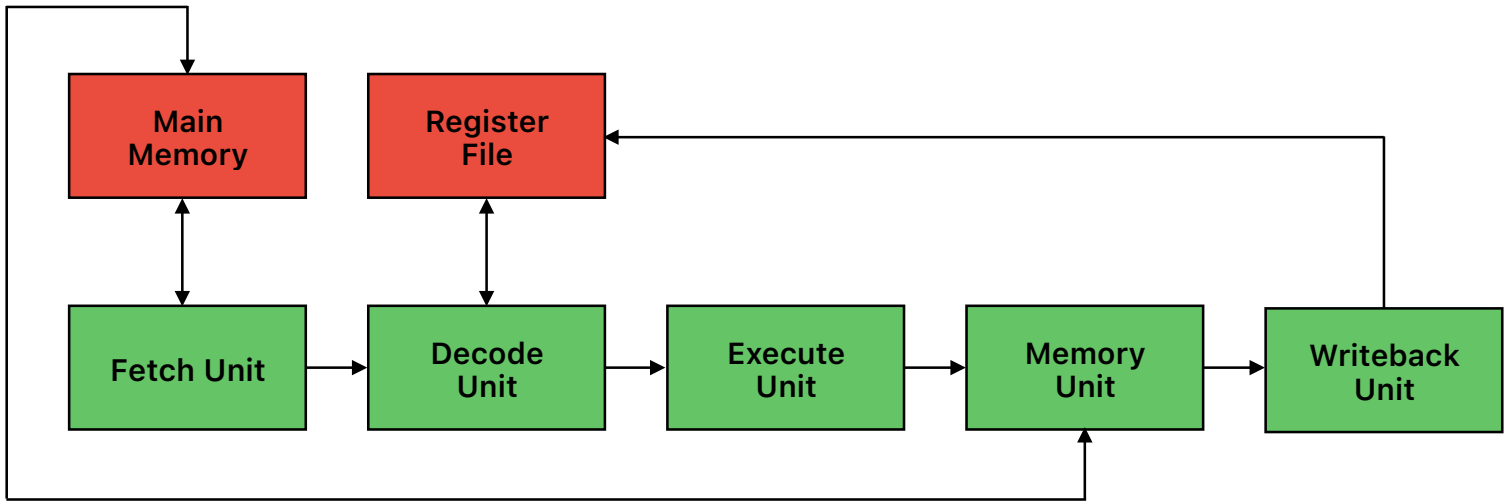
High-Level Architecture Diagram



Features

- Non-pipelined and scalar
- Five-stages: fetch, decode, execute, memory, writeback
- Implements the RV32I base integer instruction set, except for the FENCE, ECALL, and EBREAK instructions
- Operation of each unit is dictated by control signals produced by the decode unit

Benchmark Kernels Overview

- **Factorial**: Computes 12! with multiplication implemented via repeated addition.
- **Bubble Sort**: Sorts a descending list of 1000 integers into ascending order using the bubble sort algorithm.
- **Euclidean**: Computes the greatest common divisor of $7^3 \cdot 17^5$ and $7^3 \cdot 2$ using Euclid's original subtraction-based algorithm.
- **Matrix Multiply**: Multiplies a 10×50 matrix by a 50×10 matrix, with multiplication again implemented via repeated addition.

Benchmark Results

Kernel	Instructions	Cycles	IPC
Factorial	439,547,610	2,197,738,050	0.2
Bubble Sort	22,508,527	112,542,635	0.2
Euclidean	7,809,251	39,046,255	0.2
Matrix Multiply	16,571,974	82,859,870	0.2

Plans for the Final Submission

The following is a list of features that I would ideally like to implement for the final submission:

- Pipelining
- Out-of-order execution via Tomasulo's algorithm
- Multiple execution units
- Branch prediction
- Speculative execution
- More benchmark kernels