CISC processors

* Complex Instru, Set computer
* When an MCU supports many addressing modes for ALU instructions & for memory accesses & data tran
- * for instructions, the MCU is said to be CISC architecture
* Large number of complex instruction
* Instructions are of variable no,, of bytes
* Instructions take varying amt,, of time for execution

Section D

IV Answer the following

(26) @ Explain the working of T & D flipflop

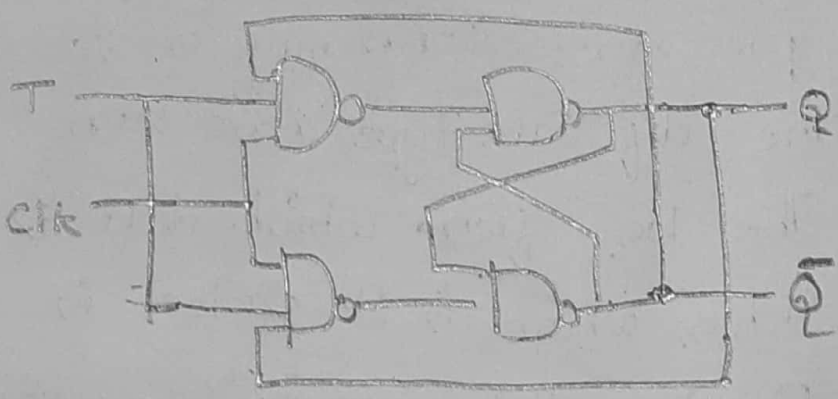
This is a much simpler version of J.K flipflop

Both e- J & K i/p are connected together & thus are also called a single Input J.K flipflop

When clock pluse is given to e- flipflop e- o/p begins to toggle

Truth table

Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0



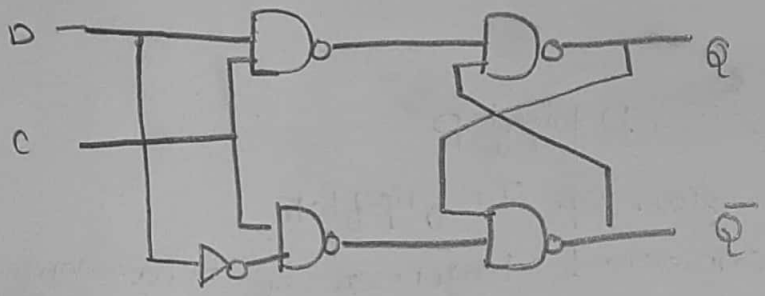
D flipflop

D flipflop is actually a slight modification of e⁻ above explained clk SR flipflop from e⁻ figure you can see that e⁻ D i/p is connected to S i/p & e⁻ complement of the D i/p is connected to e⁻ R i/p

When ci/p is 1 the latch o/p is placed in e⁻ setor reset state based on value of D

If D=1, the Q o/p goes to 1

If D=0, the Q o/p goes to 0.



function table

C	D	Next State of Q.
0	x	no change
1	0	Q=0 Reset
1	1	Q=1 Set

(b) Write a note on e⁻ d/f modes of data transfer.

There data has to be moved stored or send from or b/w the processor, external mry or I/O devices

The d/f data type have seen

The loc// from which data is copied is called source & loc// where is it pasted is called destination

During this operation e⁻ contents of source are not altered

The Data during this operation e⁻ contents of source are not altered

An inst$_{n}$ is a command to comp to perform a given operation on specified data

Opcode & operand

Opcode → Specifies what operation to be performed

Operand → data to be operated

Based on Source & destination loc$_{n}$, data transfer operation is classified.

* Data transfer from 1 register to other
* Data transfer b/w mry loc$_{n}$ & register
* Load direct data to acc$_{n}$ or register or mry loc$_{n}$
* Data transfer b/w i/o devices & accumulator

Comonly used data transfer operation

- MOV DST, SRC
- MVI DST, Direct data
- PUSH
- POP

Q7 (a) Explain interrupt cycle with a neat diagram.

Interrupt cycle

The interrupt cycle is a hardware implementation of a branch & save return address operation

An interrupt cycle flipflop R is included in e comp$_{n}$

When R = 0, the comp$_{n}$ goes through an instruction cycle

During e^{-} execute phase of e^{-} inst$_{n}$ cycle IEN is checked by e^{-} control.

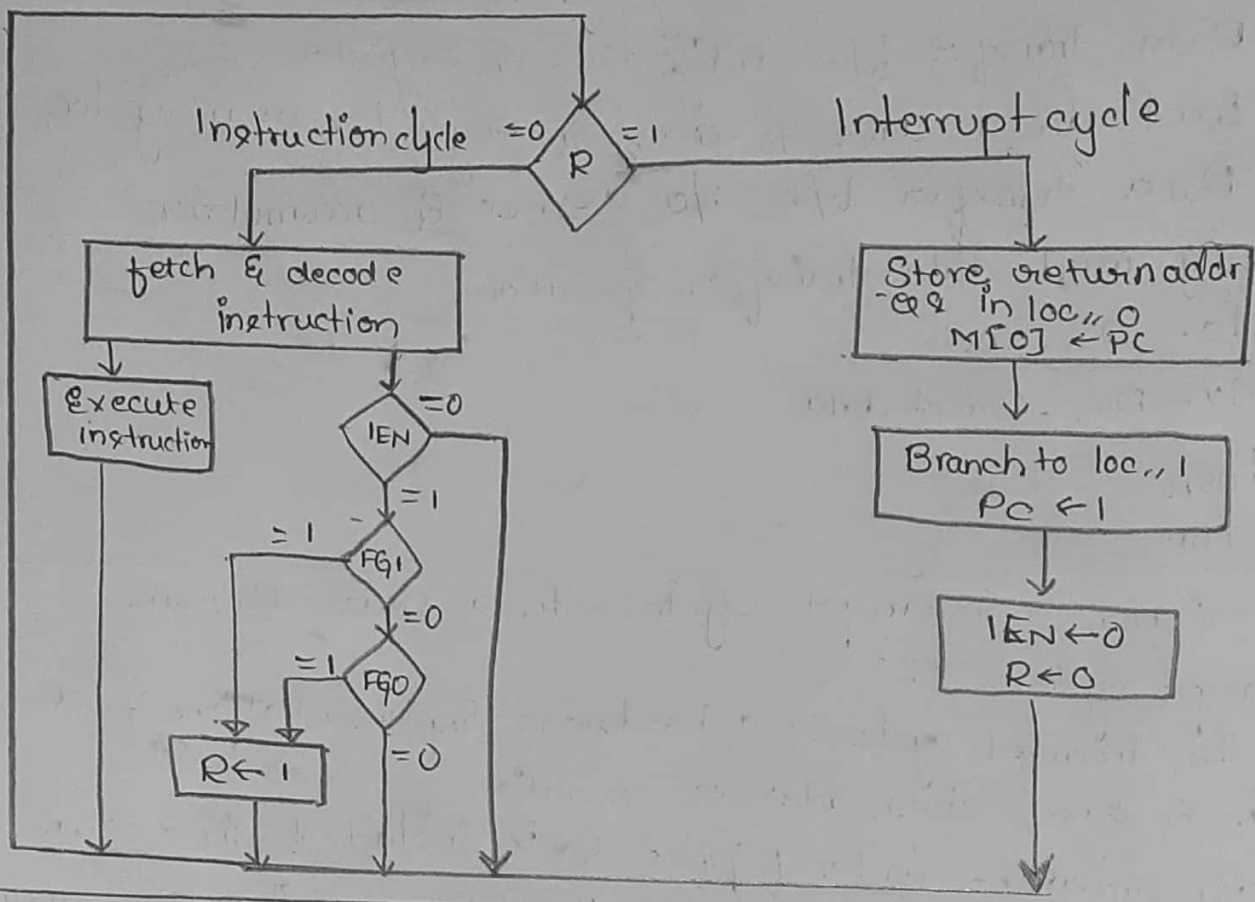
If it is 0, it indicates that e^{-} programmer does not want to use any interrupt, So control continues with e^{-} next inst$_{n}$ cycle.

If IEN is 1, control checks e^{-} flag bits

If both flags are 0, it indicates that neither e^{-} nor e^{-} o/p registers are ready for transfer of info$_{n}$

In this case control continues with the next instruction cycle if either flag is set to 1 while IEN = 1 flipflop R is set to 1

At the end of the execute phase, control checks the value of R, and if it is equal to 1, it goes to an interrupt instead of an instruction cycle



(07)

(b) Explain various i/p o/p instruction

I/p & o/p instru are needed for transferring info to & from AC, registers, for checking the flag bits & for controlling the interrupt facility

I/p & o/p instr have an operation code 1111 & are recognized by control when D7 = 1 & I = 1

The INP instr transfers the i/p info from INPR into 8 low order bits of AC & also clears the i/p flag to 0

The instru$_{n}$ that is skipped will normally be branch inst$_{n}$ to return & check e flag again

The branch inst$_{n}$ is not skipped if e flag = 0. If flag is 1 the branch inst$_{n}$ is skipped & i/p or o/p inst$_{n}$ is executed

The last 2 inst$_{n}$ set and clear an interrupt enable flip flop, IEN The purpose of IEN is explained in conjunction with e interrupt operation.

INP	AC(0-7) ← INPR, FGI ← 0	i/p char. to AC
OUT	OUTR ← AC(0-7), FGO ← 0	o/p char from AC
SKI	if(FGI = 1) then (PC ← PC+1)	Skip on i/p flag
SKO	if(FGO = 1) then (PC ← PC+1)	skip on o/p flag
ION	IEN ← 1	Interrupt enable on
IOF	IEN ← 0	Interrupt enable off