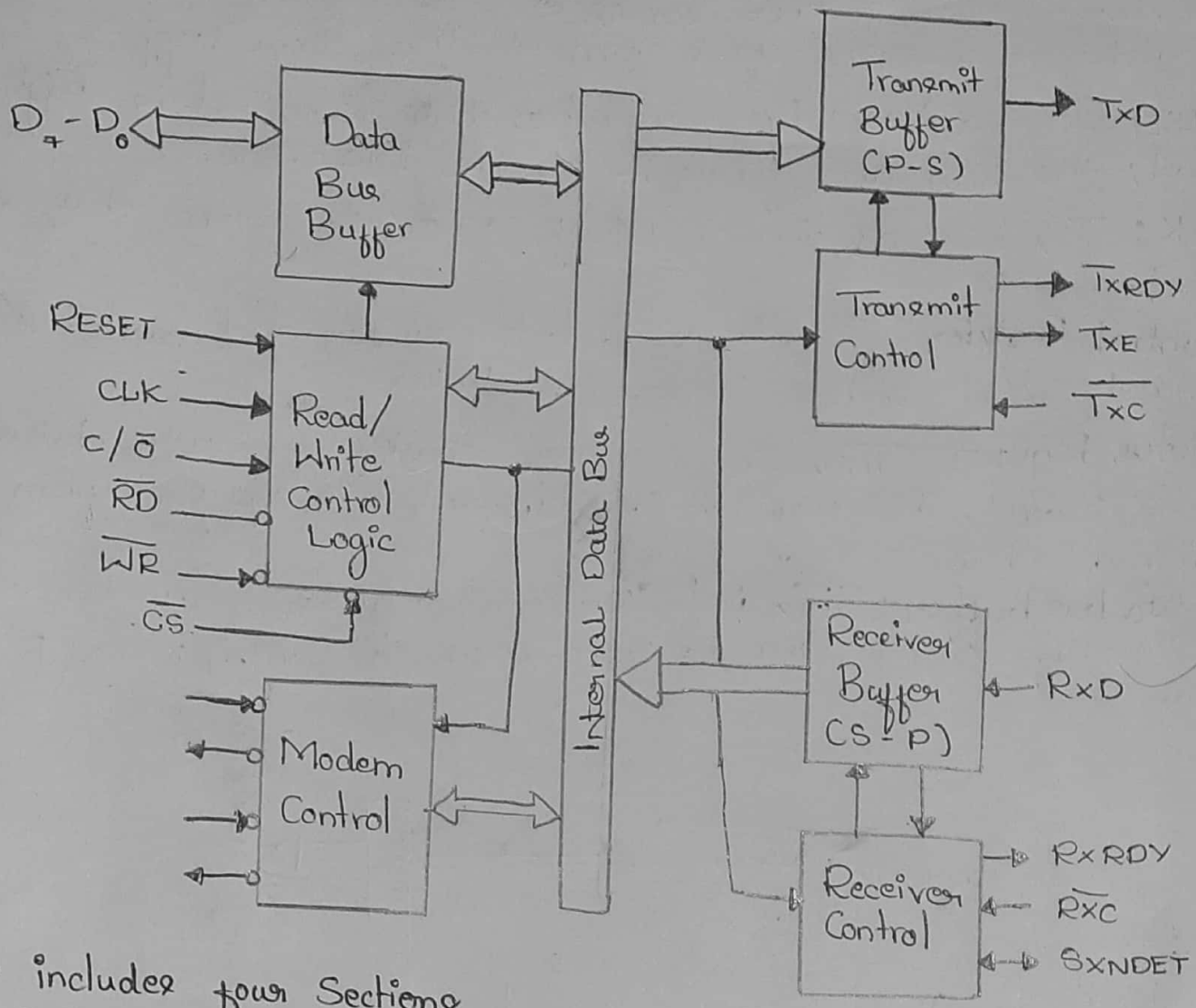
Assignment -01

① Draw block diagram of 8251A programmable communication Interface and Explain?



It includes four Sections

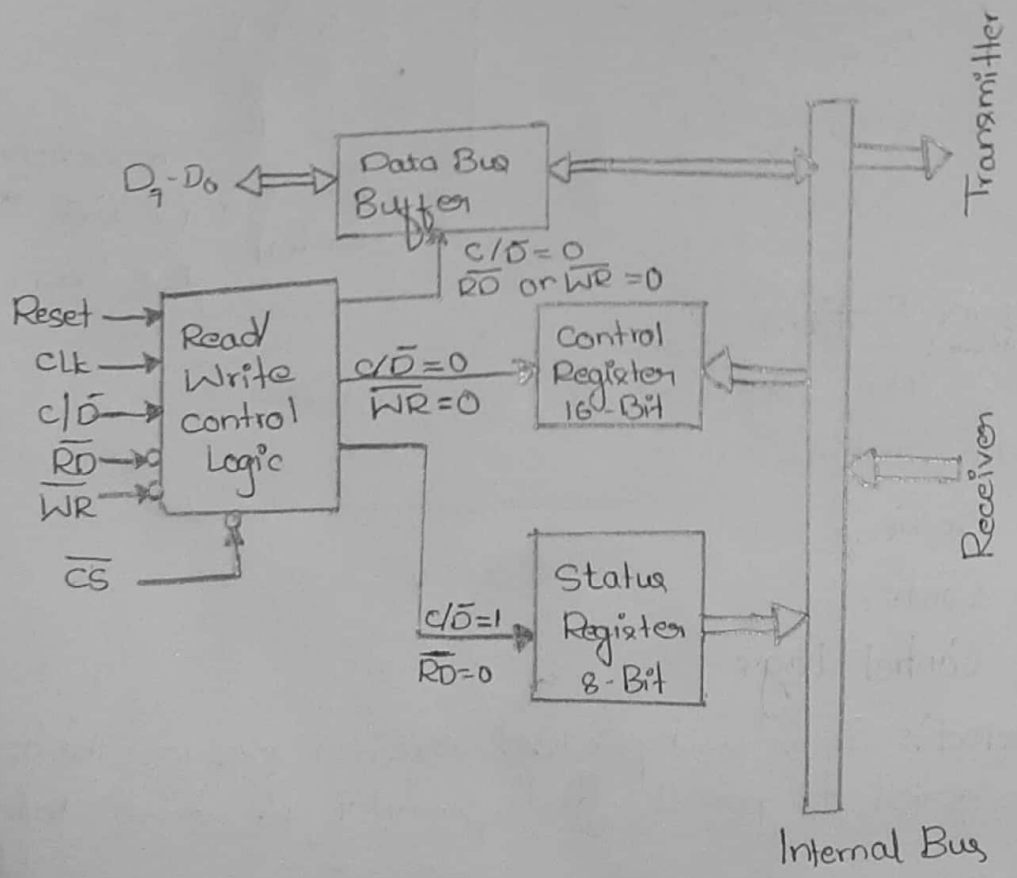
① Read/Write Control Logic
② Transmitter Sections
③ Receiver Sections
④ Modem Control

① Read/Write Control Logic

★ $\overline{CS}$ (Chip Select): It is a chip select terminal goes low the 8251A is selected for serial to parallel and parallel to serial data conversion.

★ C/$\overline{D}$ (Control/Data): A high on this terminal addresses the control register or status register for Read/Write operation. A low on this terminal addresses the data bus Buffer to Read Write the serial or parallel data.

* $\overline{WR}$ It is an active low write signal. When this terminal goes low, the MP either writes the control word register or sends o/p to the data buffer. This pin is connected to either low or $\overline{MEMW}$ signal
* $\overline{RD}$: It is an active low read signal. When this terminal goes low, the MP either reads a status from the status register or accepts data form the data buffer.
* RESET It is a Reset i/p pin. When this terminal is high, it resets the 8251 and forces it in the idle mode.
* CLK: This is a clk input, usually connected with the system clock.
* Control Register This is a 16-bit register and contains the control word with a independent byte
* Status Register This i/p register checks a Ready status of a peripheral. This register is addressed as an i/p port when c/$\overline{D}$ terminal is high.
* Data bus buffer: This is bidirectional register & can be addressed as an i/p port & and o/p port when c/$\overline{D}$ (control Data) pin is low.



② Transmitter Section

* The transmitter accepts parallel data from the MPU and converts them into serial data.
* It has 2 named as buffer register and output register.

* TXD (Transmit Data)

It is transmit data terminal. The serial bits are transmitted on this line.

* $\overline{Txc}$ (Transmitter Clock)

This pin is a Transmitter Clock. This signal controls e⁻ rate @ which bits are to be transimitted by the 8251A. The clk frequency can be 1, 16 or 64 times of e⁻ baud.

* Tx RDY (Transmitter Ready)

This is transmitter Ready pin. When it is high, it indicates that e⁻ buffer is empty and e⁻ 8251 is ready to accept a byte.

* TxE (Transmitter Empty)

It is used as o/p terminal. A high on this line indicates that e⁻ o/p register empty

③ Receiver Section

* The receiver section accepts serial data on e⁻ RxD line from a peripheral and converts them into parallel data.
* This section has two registers: the reciver i/p register & the buffer register.

* RXD (Read / Receive Data) It is receive data terminal. The serial bits are received on this line & converted to a parallel byte in e⁻ reciver i/p register

$\overline{Txc}$ (Receiver Clock): This pin is Receiver clk. This controls the rate @ which bits are received by e⁻ 8251A

* RxREADY (Receiver Ready)

This is Receiver Ready pin. When this o/p terminal is high, the 8251A has a character in e⁻ buffer register & is ready to transfer it to the MP.

Modem Control

The modem control section of e⁻ 8251A provides 2 i/p signals DSR (Data Set Ready), CTS (Clear to Send) and two o/p control signals DTR (Data Terminal Ready), RTS (Request to send) to handle DTE and DCE

$\overline{DCR}$ (Data Set Ready)

This is an active low i/p terminal used by e⁻ modem to indicate that it is ready for communication.

$\overline{CTB}$ (Clear to Send)

This active low i/p terminals is used by e⁻ modem to signal the DTE that e⁻ communication channel is clear & it can send out e⁻ serial data

DTR (Data Terminal Ready)

This o/p signal is used by e⁻ 8251 to signal e⁻ modem to indicate that e⁻ terminal is ready to communicate.

RTS (Request to Send)

This o/p signal is used by e⁻ 8251A to signal to modem that it has data to be transmitted.