Design and implementation of a multi-channel time division multiplexing anti-aliasing filter

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ABSTRACT

A multi-channel time division multiplexing anti-aliasing filter is designed for the aliasing of digital signals in a networked airborne acquisition system applied to flight tests, and adopts an anti-aliasing filter with variable sampling rate. In the digital signal processing process, due to the high sampling rate, digital signal aliasing may occur during integer multiple extraction, which solves the problem that digital signal aliasing may occur when performing integer multiple extraction in the digital signal processing process due to the high sampling rate. Digital filter is realized by FPGA, which realizes multi-channel time division multiplexing function and supports digital signal processing of 8 channels of synchronous sampling data. The filter characteristic test is performed on the system. For the original signal of 8 kHz, the cutoff frequency of the half-band filter is Fs/4, that is, 2 kHz, the signal frequency corresponding to -3 dB after the system is 2048 Hz. The amplitude-frequency characteristic curve of the system is consistent with the MATLAB simulation results.

CCS CONCEPTS

• **Computing methodologies** → Modeling and simulation; Model development and analysis; Modeling methodologies.

KEYWORDS

Time Division Multiplexing, Anti-aliasing, Digital Filter, FPGA, Compensation Filter, Butterworth

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1 INTRODUCTION

AD7606 is a commonly used analog/digital conversion acquisition chip that supports simultaneous sampling of 8 analog input signals. The chip itself has a second-order Butterworth anti-aliasing filter. The signal frequency corresponding to -3dB is 15 kHz When the input voltage range is ±5V, and, the signal frequency corresponding to -3dB is 23 kHz when the input voltage range is ±10V.

In a networked general airborne acquisition system for flight tests, AD7606 is used for the front-end analog-to-digital conversion of the analog signal acquisition module. The working mechanism of the analog signal acquisition module is as follows. AD7606 is synchronous sampling, the over-sampling rate is 200 kHz, and the read rate of A/D controlled by FPGA is 64 kHz. The sampling rate of each channel configured through the ground management software is exponentially multiplied by 2, like 16 Hz, 32 Hz...32 kHz. According to the configuration, each analog channel will extract the data, reduce the sampling rate, and finally pass the signal through a half-band digital filter, and then output the data [1-4].

In the process of signal acquisition and recovery of networked airborne acquisition equipment, when analog signal data is recovered by ground software and analyzed for amplitude-frequency characteristics, the following problems exist:

- The signal is aliased, and the data is distorted after recovery;
- The high frequency signal is sampled into the low frequency band.

2 ANALYSIS OF ALIASING DISTORTION

2.1 *Integer multiple decimation*

In this airborne acquisition system, the digital signal is sampled at 64 kHz and then Integer multiple decimation, which involves the problem of inverted signal decimation.

Extraction principle: Take out the data at equal intervals for the input signal and rearrange it once. After integer decimation of the signal, the amplitude-frequency characteristics of the signal will change. The amplitude and frequency of the digital signal is periodic, and the period is equal to the sampling rate. After Integer multiple decimation, the sampling rate is reduced, and the amplitude frequency period of the signal after decimation is reduced to the 1/D of original.

Assuming that in a certain system, the analog signal only has a signal in the frequency range of 0~2 (unit, the same below), and the A/D sampling is performed at a rate of 6, then the sampled signal has no amplitude-frequency aliasing, and the amplitude-frequency cycle is 6. The amplitude and frequency of the signal is shown in Figure 1(a).

If the signal with a sampling rate of 6 is decimated by 2 times, the signal amplitude frequency cycle is reduced to 3 after extraction. The amplitude frequency shape has not changed, but the period is

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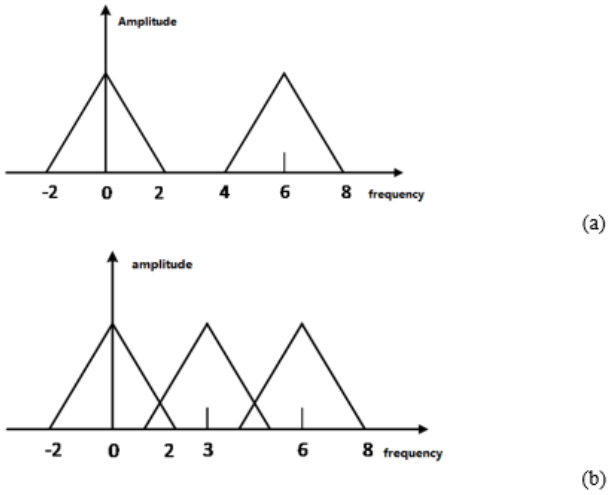

Figure 1: Signal amplitude and frequency diagram before and after signal extraction

shortened, which may cause the signal amplitude frequency aliasing problem, as shown in Figure 1 (b).

Therefore, in order to avoid the appearance of amplitude-frequency aliasing, the signal can be restored without distortion only when the sampling rate after extraction still meets the requirements of the sampling theorem, otherwise certain measures need to be taken [5].

2.2 *Analysis of Amplitude and Frequency Aliasing*

The digital signal sampling rate is initially 32 KHz, and its amplitude frequency is periodic 32 kHz. After D extract, the signal amplitude frequency cycle is reduced to 1/D of the original cycle. According to the amplitude-frequency characteristics of AD7606's own anti-aliasing filter, when the input voltage range is ±5V, the signal frequency corresponding to -3dB is 15 kHz, and when the input voltage range is ±10V, the signal frequency corresponding to -3dB is 23 kHz.

Decimating the data by integer (such as D=2), the frequency spectrum period reduces to 16 kHz. Since the signal frequency of the A/D analog anti-aliasing filter at -3dB is 15 kHz, and the signal spectrum period is 16kHz at this time, combined with the rule of integer decimation above, it is determined that there is a signal aliasing problem. Although there is a half-band filter Fc=Fs/4 for digital filtering after extraction, the high-frequency signal has already entered the low-frequency band and occurred aliasing during the extraction stage. At the same time, the transition band is wider, as shown in Figure 2

In view of the aliasing problem that occurs in the signal acquisition process, the usual measure is the anti-aliasing filter [6-8]. The anti-aliasing filter is to perform low-pass filtering on the signal before the signal is extracted, so that the frequency band of the signal is less than 1/2 of the frequency after sampling.

During the flight test, there is white noise distributed in the entire frequency band at the same time. For the digital signal processing

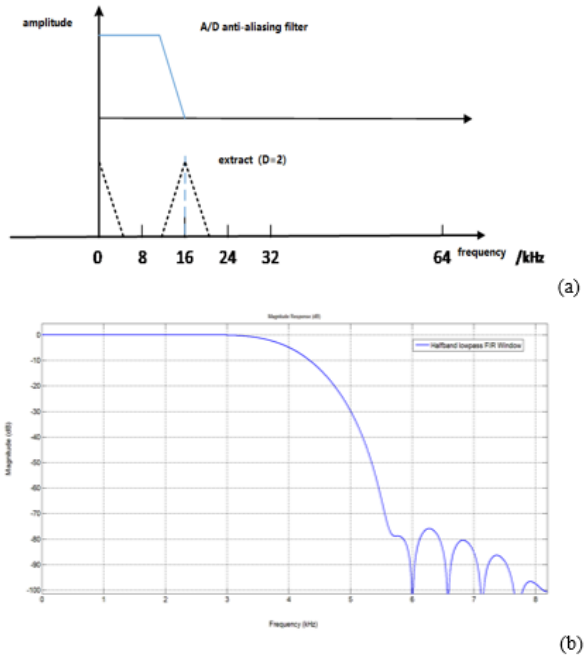

Figure 2: Extracting aliasing

of the airborne acquisition system, in order to suppress noise and avoid signal spectrum aliasing, it is very necessary to increase the anti-aliasing digital filter in the signal processing process.

3 INTRODUCTION TO ANTI-ALIASING FILTERS

Technical requirements for custom design of digital filters in FPGA:

1) The ripple coefficient in the frequency band of the useful signal meets the requirements;

2) After the multi-rate processing, the amplitude frequency aliasing problem will not occur;

3) The filter occupies less resources and the calculation speed is fast [9-10].

3.1 *Introduction to CIC filter*

In this airborne acquisition system, the digital signal is sampled at 64 kHz and then Integer multiple decimation, which involves the problem of inverted signal decimation.

CIC filters are often used in the communications industry, and are generally used in digital frequency conversion systems, such as digital down conversion (DDC) and digital up conversion (DUC). It is characterized by simple structure, no multiplier, only composed of adders, integrators and registers, suitable for multi-rate processing conditions, and is a zero-cancellation FIR filter [11].

The impulse response of a single-stage CIC filter is

$$h(n) = \begin{cases} 1, 0 \le n \le M-1 \\ 0, \text{Other} \end{cases} \quad (1)$$

In the formula, M is the length of the filter. CIC is essentially a special FIR filter with linear phase, and the system function is

$$H(z) = \sum_{n=0}^{M-1} Z^{-n} = (1 - Z^{-M})/(1 - Z^{-1}) \quad (2)$$

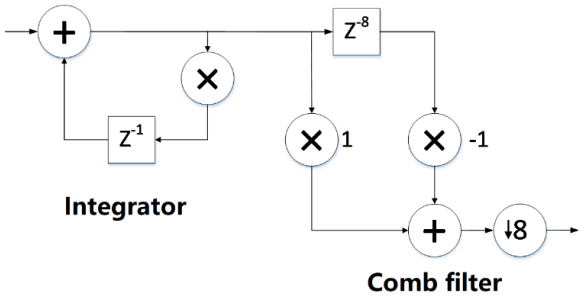

Figure 3: Primary CIC structure

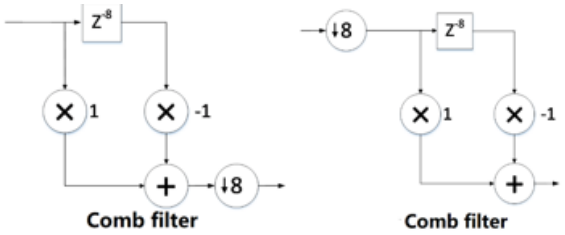

Figure 4: Comb filter equivalent structure

Carry out Fourier transform on formula (1) to get the CIC amplitude-frequency characteristic function.

3.2 *CIC filter structure*

The structure of a single-stage CIC is composed of an integrator and a comb filter, as shown in Figure 3

The comb filter undergoes equivalent transformation, and the structure is shown in Figure 4

3.3 *Matlab simulation of anti-aliasing filter*

By using MATLAB to simulate the amplitude-frequency characteristics of CIC [12], the appropriate number of cascade stages is obtained by comparison.

It can be seen from Figure 5 that under the one-stage CIC filter, although the length M of the filter is changed, the first sidelobe stopband attenuation remains basically unchanged.

If the five-level CIC is cascaded, the sidelobe attenuation of 60dB can be achieved, which basically meets the design requirements, but the negative impact is that the passband attenuation is significantly increased, as shown in Figure 6. The simulation of the CIC amplitude-frequency characteristics of five levels of different decimation coefficients shows that for the passband attenuation with a normalized passband frequency of 0.2, the more the number of levels, the greater the attenuation amplitude. For a given passband attenuation requirement, the passband range of the multi-stage CIC filter is lower than that of the first-stage filter, as shown in Figure 7

In view of the negative factors caused by the five-level CIC cascade, the general solution is to cascade a compensation FIR filter after the five-level CIC to compensate the passband attenuation and limit the transition band bandwidth at the same time [13-14]. The amplitude-frequency characteristic curve of the compensation FIR is shown in Figure 8

3.4 *Five-level CIC structure*

Combining the structure and equivalent transformation of the first-level CIC filter, the structure of the five-level CIC is shown in the figure, which is also the Homemaker structure diagram of the anti-aliasing filter verified by the simulation and finally realized by the logic in this paper, as shown in Figure 9

4 SIMULATION OF ANTI-ALIASING FILTER AND COMPENSATION FILTER

By the improved digital signal processing structure, combined with the characteristics of the AD7606's own anti-aliasing filter, when the input voltage range is ±5V, the signal frequency corresponding to -3dB is 15kHz, and when the input voltage range is ±10V, -3dB corresponds to The signal frequency is 23kHz. In order to solve the problem of a wider frequency spectrum when the input voltage is ±10V, the FPGA read speed is increased to 64 kHz, that is, the signal sampling rate is 64kHz.

The digital signal first enters the CIC digital filter for anti-aliasing and down-sampling processing, and then the output signal enters the compensation CFIR digital filter and HBFIR digital filter. The data stream processing process is shown in the following figure:

Simulating the above structure by MATLAB, the MATLAB simulation of "Five-level CIC-CFIR" is shown in the figure below. It can be seen that after 4 times of decimation, the sampling rate is changed from 64 kHz to 16kHz, and the frequency band has been attenuated around 8kHz. Without cascaded HBFIR, the first sidelobe attenuation is about -30dB, as shown in Figure 11

From the simulation of the amplitude-frequency characteristics of the three filters of CIC-CFIR-HBFIR after cascading, it can be found that the passband signal frequency has been further restricted to less than 4kHz, and the amplitude-frequency aliasing band has been avoided.

5 FPGA IMPLEMENTATION OF DIGITAL FILTER

5.1 *FPGA implementation of filter*

After the anti-aliasing filter is simulated in Matlab and the coefficients of the filter are obtained, the simulation model needs to be implemented in detail. Considering the limited logic resources of FPGA, in order to save resources and reduce power consumption to the greatest extent, a multi-channel signal time-division multiplexing anti-aliasing digital filter model is proposed.

The main functions of the filter module are as follows:

1) Currently supports eight channels of digital signal input, and the sampling rate of each channel can be set independently;

2) The module includes five-level CIC, compensation CFIR, HBFIR and IIR digital filters, and the signal output can choose FIR and IIR results (limited to space, only the anti-aliasing part is discussed);

3) After the filters are cascaded, the theoretical output accuracy is 0.01%.

The realization of the filter mainly relies on the integrator, differentiator, adder and on-chip memory, and at the same time effectively reduces the resource occupation through multiplexing [15-16]. The

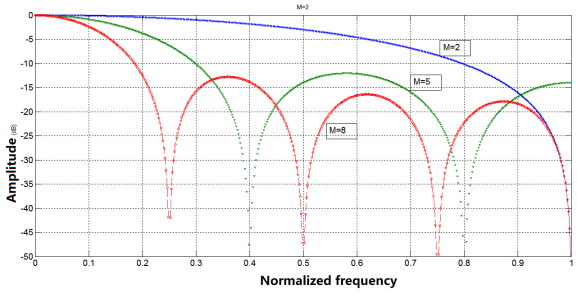

Figure 5: Amplitude-frequency characteristics of first-order CICs of different lengths

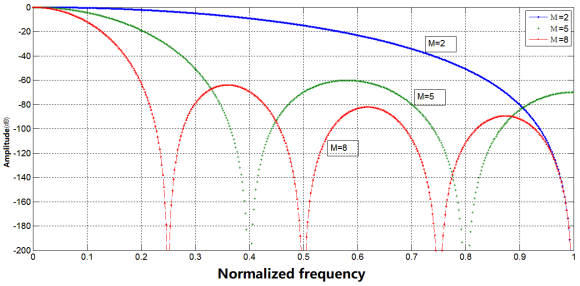

Figure 6: Amplitude-frequency characteristics of five-stage CICs of different lengths

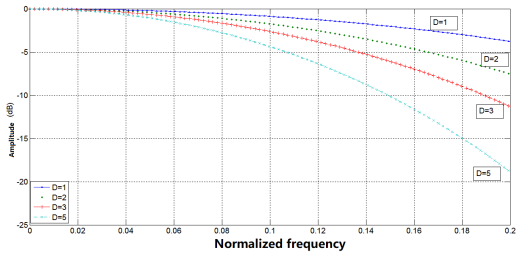

Figure 7: Amplitude-frequency characteristics of fifth-order CIC filters with different cascaded series

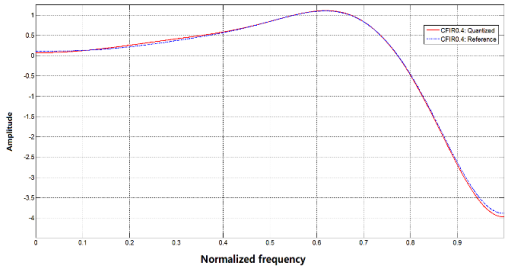

Figure 8: Compensation for the amplitude-frequency characteristic curve of FIR

FPGA structure of the filter module and the occupation of logic resources are shown in Figure 13

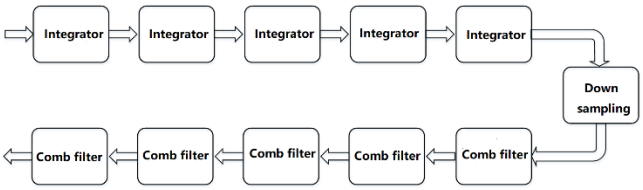

Figure 9: Five-stage CIC anti-aliasing filter

Figure 10: Digital filter cascade diagram such as anti-aliasing CIC

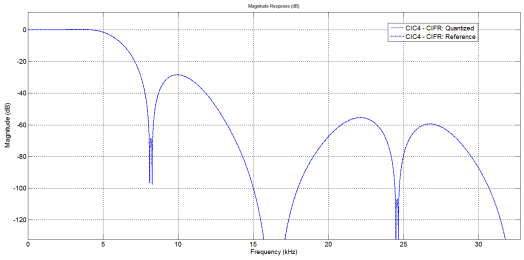

Figure 11: Five-stage CIC cascade CFIR amplitude-frequency characteristics

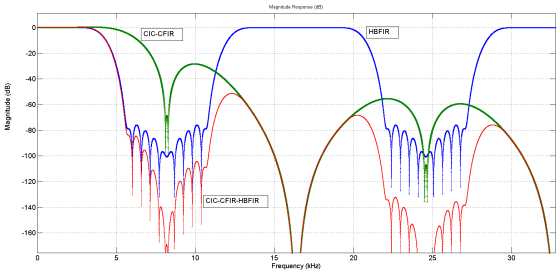

Figure 12: Comparison of amplitude-frequency characteristics of digital filters before and after improvement

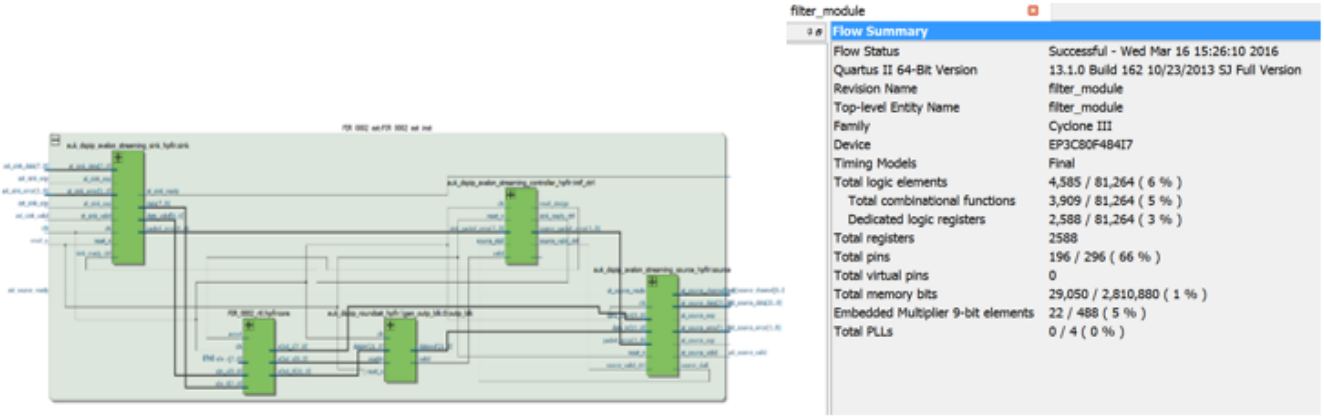

Figure 13: Filter FPGA implementation structure and resource occupation

5.2 *Filter actual filtering processing*

Solidify the program and test the filter characteristics. The sampling rate is 64 kHz, the decimation ratio is 8, and the frequency of the input signal is 100 Hz, 512 Hz, 1024 Hz, 1536 Hz, 1700 Hz, 1800 Hz, 1900 Hz, 2048 Hz, 2200 Hz, 2560 Hz, 3072 Hz, 4096 Hz, 5120 Hz, 6144 Hz, and 8000 Hz.

Calculate the amplitude attenuation corresponding to each frequency on the basis of 100Hz based on the collected data, and graph it. The analysis shows that after the 64kHz signal extracted by D=8, Fs becomes 8kHz, the cut-off frequency of the half-band filter is Fs/4, which is 2kHz, and the signal frequency corresponding to -3dB is 2048Hz, which achieves the expected effect.

At the same time, the amplitude-frequency characteristic curve is consistent with the MATLAB simulation result, achieving the original design purpose, as shown in Figure 14

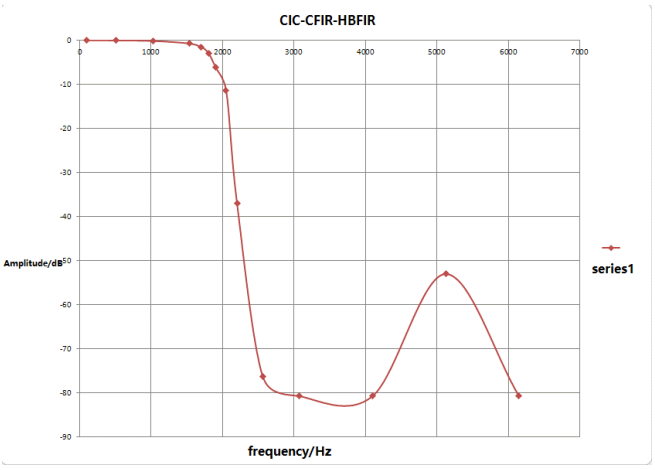

Figure 14: Amplitude-frequency characteristic curve of actual signal

6 CONCLUSION

In the field of aeronautical testing, in view of the signal aliasing caused by the signal acquisition mechanism of the networked general airborne test system used for flight test testing, a variable sampling rate anti-aliasing filter is proposed to solve this problem. This digital filter is realized by FPGA, and based on the consideration of saving resources, it uses multi-channel time division multiplexing technology to support digital signal processing of 8 channels of synchronously sampled data. It is verified by the filter characteristic test that the amplitude-frequency characteristic curve is consistent with the MATLAB simulation result, which realizes the original design purpose. n view of the popularization of high-speed acquisition in the field of flight test in the future, the application of CIC anti-aliasing filter in the field of aviation test will be broader.

REFERENCES

[1] Huang Huaqin, Liu Guiying, Zhou Luping. Design of SVG Data Synchronous Acquisition System Based on AD7606[J]. Journal of Electric Power, 2019, 34(02):144-149.

[2] Wang Donghua, Xu Zhiyong. Design of Multi-channel High Precision AD Sampling System Based on FPGA[J]. Digital technology and application, 2019,37(05):154-156.

[3] Yan Peiyu, Duan Ruibing, Liu Wenji. Design of High Precision Data Acquisition System for Welding Arc Signal Based on AD7606[J].Hot Working Technology, 2018, 47(17):176-179.

[4] Jiang Yanliang, Wang Zhenhua, Li Shasha. Design of an Intelligent Sensor Acquisition Unit Based on FPGA[J]. Electronic Design Engineering, 2018, 26(10): 155-159.

[5] Yang Fang, Fu Weiting, Qin Tiankai. Design of high frequency digital decimation filter[J]. Electronic technology application, 2017,43(12):25-28.

[6] Xie Haixia, Sun Zhixiong. An Improved CIC Decimation Filter Implementation Method [J]. Electronic Design Engineering, 2018, 26(14): 162-166.

[7] Wang Liqiang. Application of multi-rate signal processing technology in airborne universal collector[J]. Electronic Design Engineering, 2017, 25(08): 61-64.

[8] Dong Zhi, Ba Junhao, Huang Zhiping. Research on High Performance Wideband IF Signal Processing Method[J].Computer Measurement & Control, 2016, 24(12):172-176+179.

[9] Song Dingkun, Liu Guixiong, Tang Wenming. Implementation and Application of Dynamic FIR Digital Filter FPGA Based on CORDIC Algorithm[J]. China Measurement and Testing,2017,43(07):97-102.

[10] Lu Yongqin, Li Jianwen, Xu Wenwen. Design and Simulation of Digital Filter Based on FPGA[J]. Software Guide,2017,16(02):85-88.

[11] Xie Haixia, Sun Zhixiong. An improved CIC decimation filter implementation method [J]. Electronic Design Engineering, 2018, 26(14):162-166.

[12] Du Yongbian. Digital Filter MATLAB and FPGA Implementation (Altera/Verilog Edition) [M]. Beijing: Publishing House of Electronics Industry, 2015:1-42.

[13] Li Yilin, Xiao Shunwen, Yi Huan. Optimization Design of CIC Filter Based on FPGA[J].Journal of West China Normal University(Natural Science), 2017, 38(01):106-110.

[14] Liu Guowen, Zhu Weihua. Optimization Design of High Performance CIC Filter[J]. Computer Simulation,2016,33(02):234-238.

[15] Zhou Yunshui, Cai Xingpeng, Chen Tao. Tracking matched filter based on FPGA dynamic partial reconstruction[J]. Information Technology,2018(06):26-29.

[16] Wang Pu, Zhang Yuming, Tian Ye. Design and Implementation of Multi-level CIC Filter Based on FPGA[J]. Journal of Yunnan University (Natural Science Edition), 2018, 40(04):676-681.