

OLED DISPLAY MODULE

Application Notes

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| PRODUCT NUMBER | DD-25664YW-3A/4A with EVK board DD-25664BE-3A/4A with EVK board DD-25664WE-1A with EVK board DD-25664GE-1A with EVK board |
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REVISION RECORD

| Rev. | Date | Page | Chapt. | Comment | ECR no. |
|------|------------------------------|---------|--------|--|---------|
| A | 28 th May 2008 | | | First Issue | |
| B | 13 Nov 2009 | 4 14 | 1 6 | New EVK Schematic Recommended initial codes | |
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2 SYMBOL DEFINITION

D0-D7 □ These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. (Except for D2 pin in SPI mode)

E/RD# □ This pin is MCU interface input.

When interfacing to a 6800-series microprocessor, this pin will be used as the Enable

(E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.

When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to VSS.

W/R#: This pin is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.

When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin R/W (WR#) must be connected to VSS.

D/C#: This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the content at D[7:0] will be interpreted as data. When the pin is pulled LOW, the content at D[7:0] will be interpreted as command.

RES#: This pin is reset signal input.

When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.

CS#: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

BS0/BS1: These pins are MCU interface selection input. See the following table:

| BS[1:0] | Bus Interface Selection |
|---------|-------------------------|
| 00 | 4 line SPI |
| 01 | 3 line SPI |
| 10 | 8-bit 8080 parallel |
| 11 | 8-bit 6800 parallel |

VCC: This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC-DC voltage converter.

VDD: This is a voltage supply pin. It must be connected to external source.

VDDIO: Power supply for interface logic level. It should be matched with the MCU interface voltage level.

VCI: Low voltage power supply. VCI must always be equal to or higher than VDD and VDDIO.

VSS: This is a ground pin, it also as a reference for the logic pins and the OLED driving voltages. It must be connected to external ground.

NC: These pins should be left open individually.

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3 Timing characteristics

3.1 80 Series MPU parallel interface

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--------------------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 10 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 7 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| $t_{PWL R}$ | Read Low Time | 150 | - | - | ns |
| $t_{PWL W}$ | Write Low Time | 60 | - | - | ns |
| $t_{PWH R}$ | Read High Time | 60 | - | - | ns |
| $t_{PWH W}$ | Write High Time | 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |
| t_{CS} | Chip select setup time | 0 | - | - | ns |
| t_{CSH} | Chip select hold time to read signal | 0 | - | - | ns |
| t_{CSF} | Chip select hold time | 20 | - | - | ns |

Table 1: 80-Series MPU Parallel Interface Write Timing Characteristics

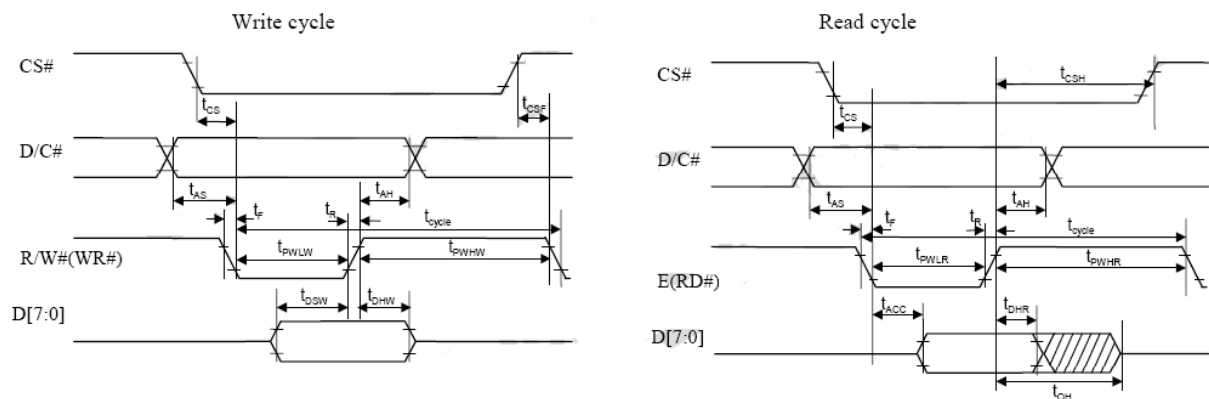


Figure 1: 80-series MPU parallel interface write timing diagram

3.2 68xx- Series MPU parallel interface

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO}=1.6V$, $V_{CI} = 3.3V$, $T_A = 25^{\circ}C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|-------------------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 10 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 7 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| PW_{CSL} | Chip Select Low Pulse Width (read) | 120 | - | - | ns |
| PW_{CSH} | Chip Select Low Pulse Width (write) | 60 | - | - | ns |
| t_r | Rise Time | - | - | 15 | ns |
| t_f | Fall Time | - | - | 15 | ns |

Table 2: 6800-Series MPU Parallel Interface Write Timing Characteristics

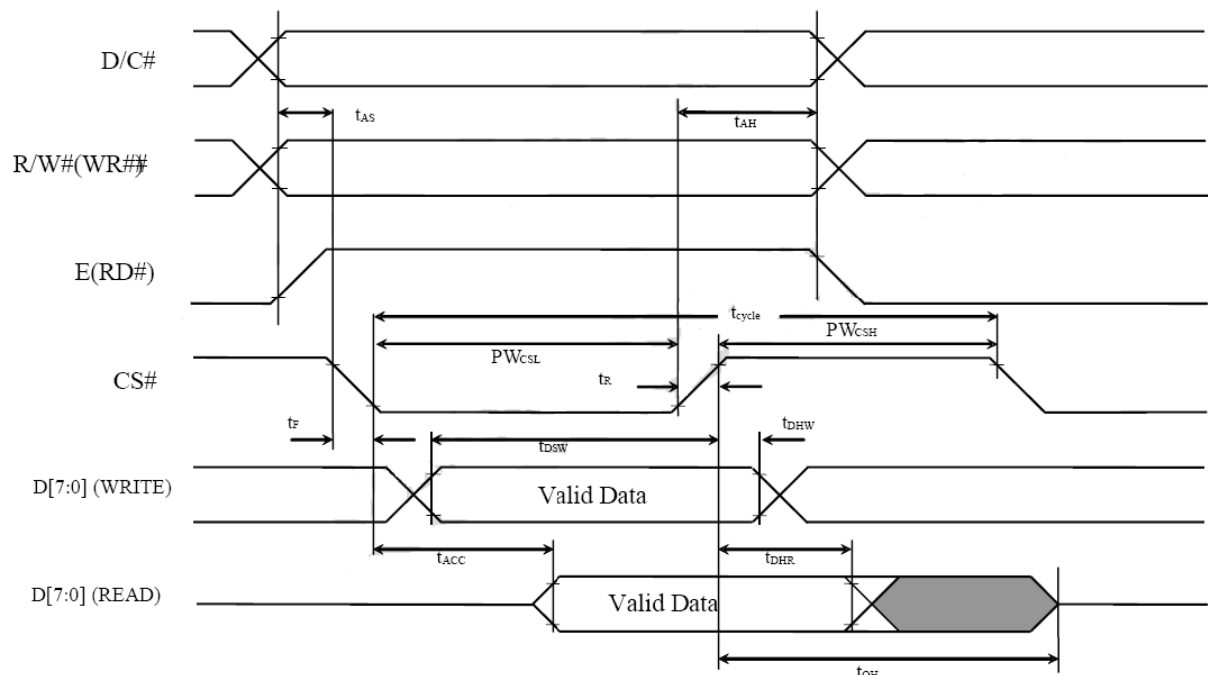


Figure 2: 6800-Series MPU Parallel Interface Write Timing diagram

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3.3 SPI(4 WIRE) INTERFACE

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO}=1.6V$, $V_{CI} = 3.3V$, $T_A = 25^{\circ}C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 100 | - | - | ns |
| t_{AS} | Address Setup Time | 15 | - | - | ns |
| t_{AH} | Address Hold Time | 15 | - | - | ns |
| t_{CSS} | Chip Select Setup Time | 20 | - | - | ns |
| t_{CSH} | Chip Select Hold Time | 10 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 15 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t_{CLKL} | Clock Low Time | 20 | - | - | ns |
| t_{CLKH} | Clock High Time | 20 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

Table 3: Serial Peripheral Interface(4-wire) Timing Characteristics

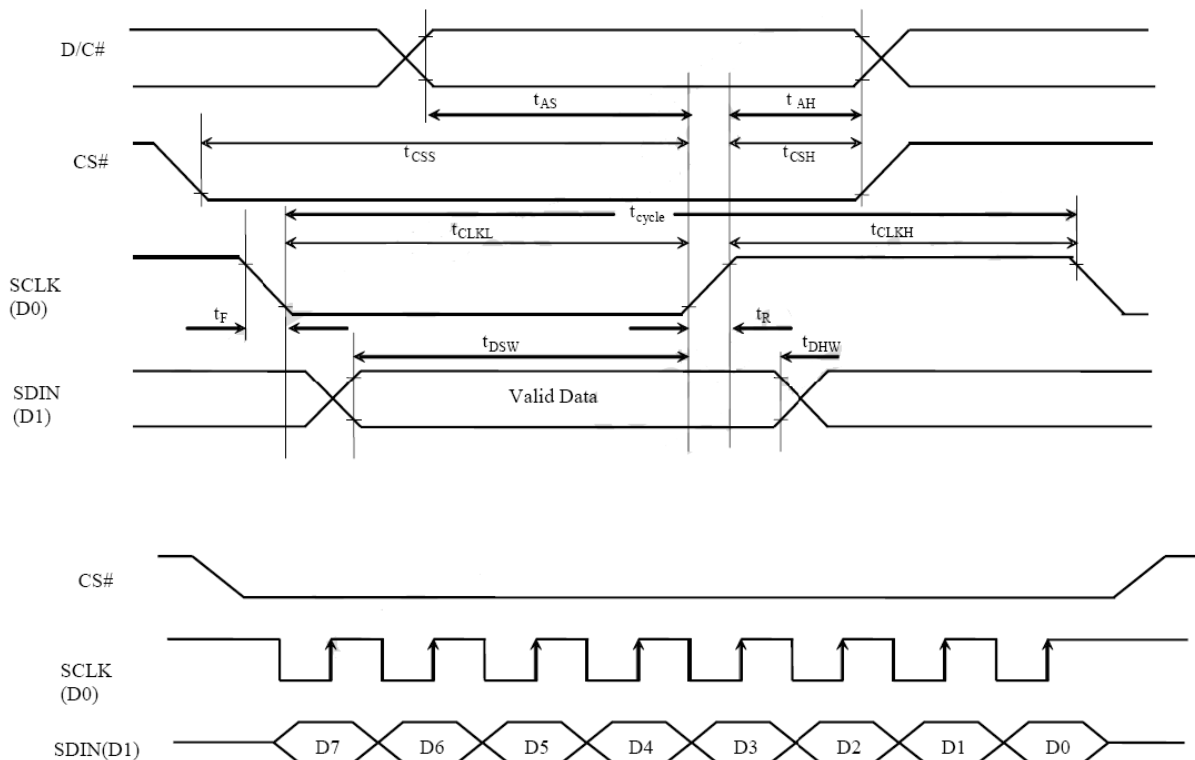


Figure 3: Serial Peripheral Interface(4 WIRE) Timing diagram

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3.4 SPI(3-WIRE) INTERFACE

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO}=1.6V$, $V_{CI} = 3.3V$, $T_A = 25^{\circ}C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 100 | - | - | ns |
| t_{AS} | Address Setup Time | 15 | - | - | ns |
| t_{AH} | Address Hold Time | 15 | - | - | ns |
| t_{CSS} | Chip Select Setup Time | 20 | - | - | ns |
| t_{CSH} | Chip Select Hold Time | 10 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 15 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t_{CLKL} | Clock Low Time | 20 | - | - | ns |
| t_{CLKH} | Clock High Time | 20 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

Table 4: Serial Peripheral Interface(3 wire) Timing Characteristics

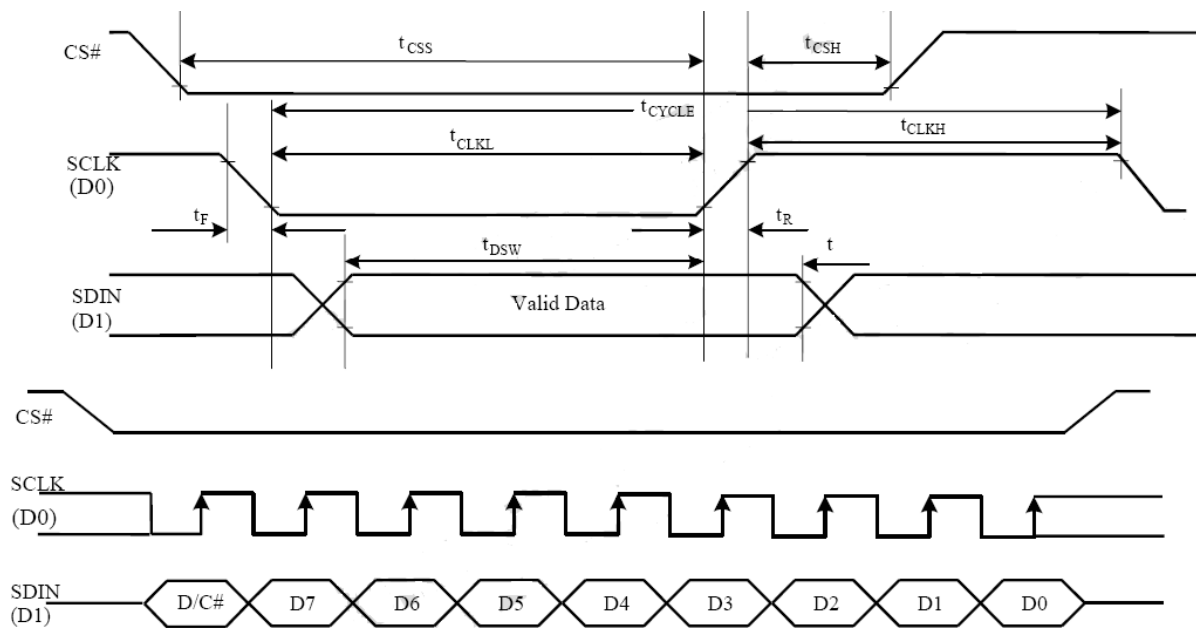


Figure 4: Serial Peripheral Interface(3-wire) Timing diagram

4 Connection Between OLED and EVK

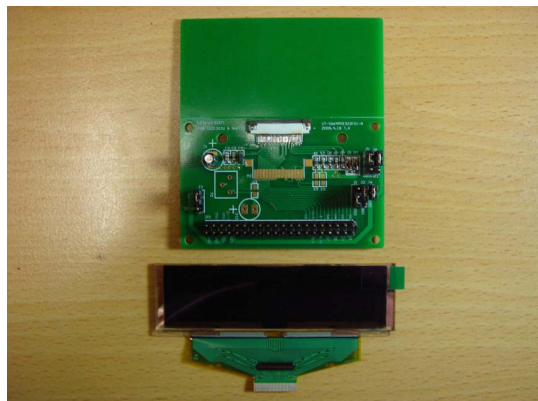


Figure 5 EVK PCB and DD-25664XX-3A-4A Module

The DD-25664XX-3A-4A are COF type module; please refer to figure 5 & 6. User can use leading wire to connect EVK with customers systems. The example shown in Fig 6.

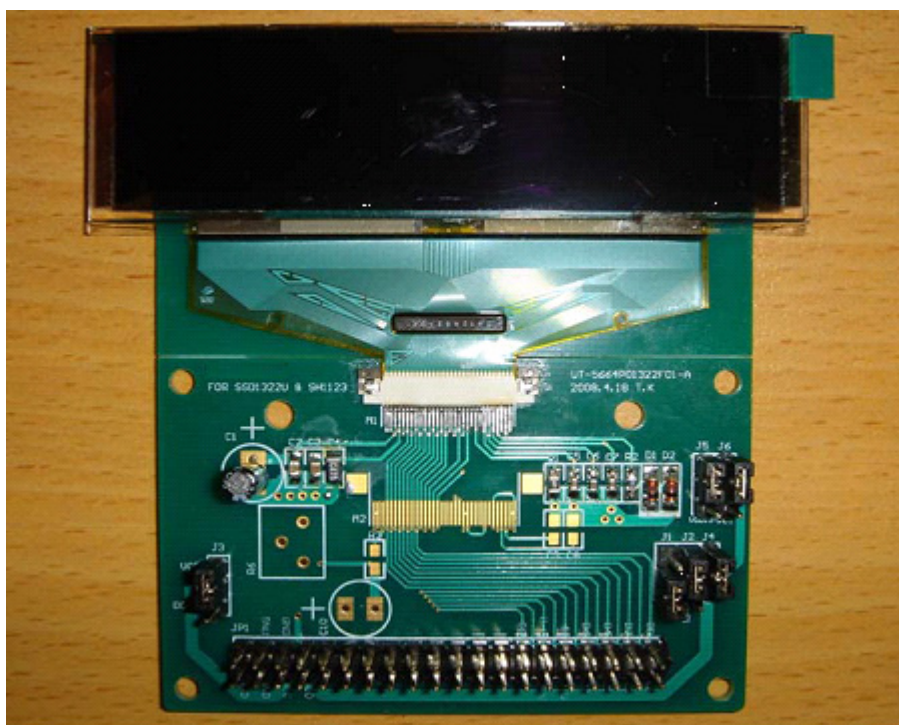


Figure 6 combination of the module and EVK

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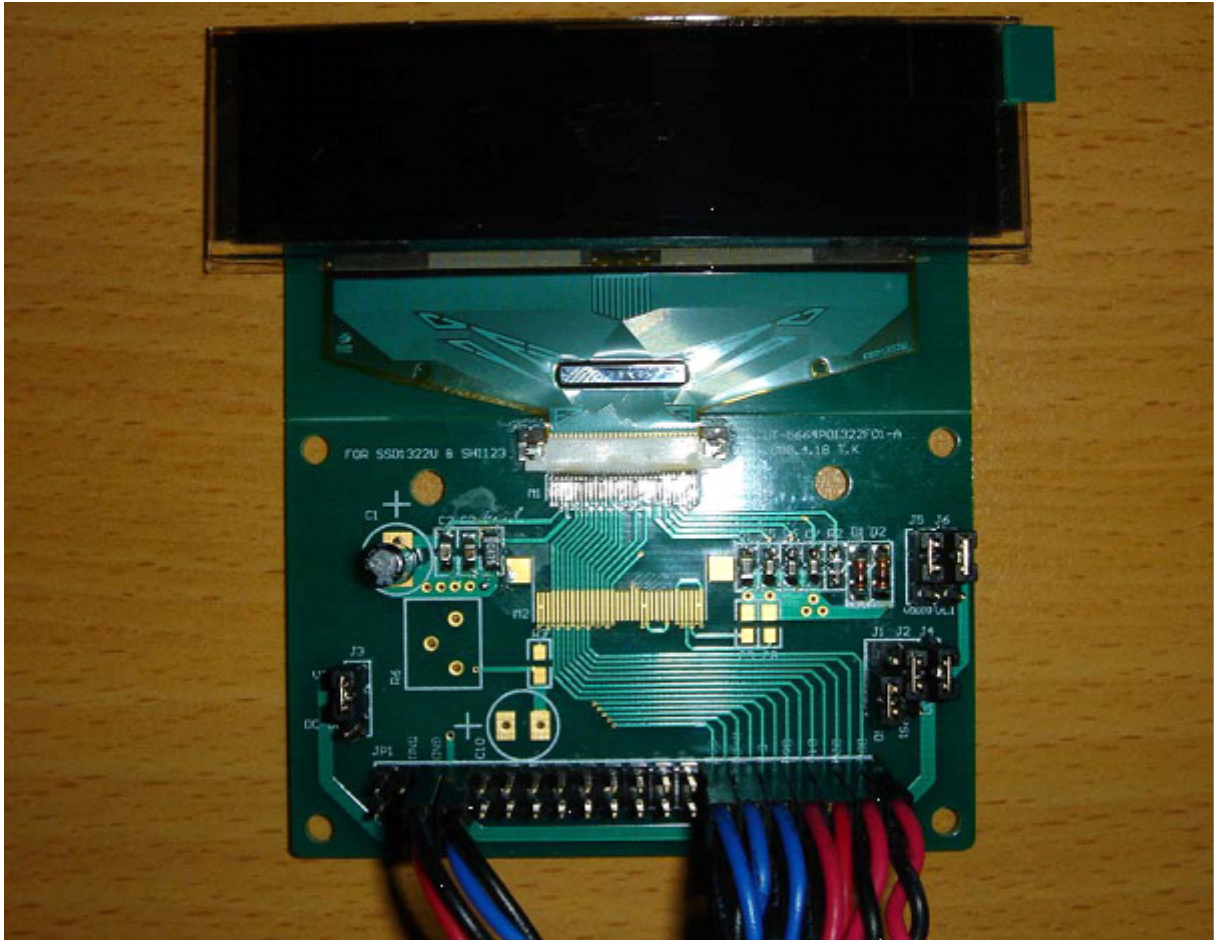


Figure 7 EVK with test platform

Note 1: It is OLED high voltage supply

Note 2: It is logic voltage supply

Note 3: Those are leading wire connect to control board. Those are data pin (D0~D7)

Note 4: Those are leading wire connect to control board. Those are control pin.
(E,R/W,D/C,RES,CS)

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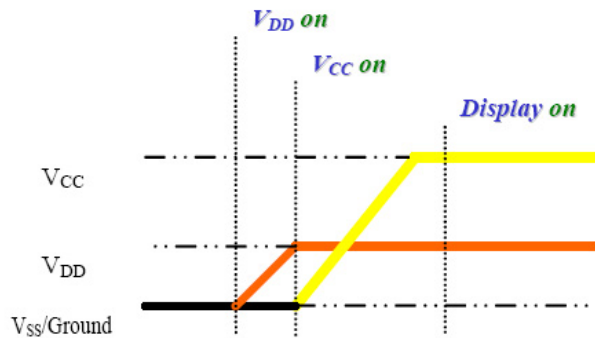
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5 Power down and Power Up sequence

To protect the OLED panel and extend the panel life time the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. So that the panel has enough time to charge up or discharge before/ after operation.

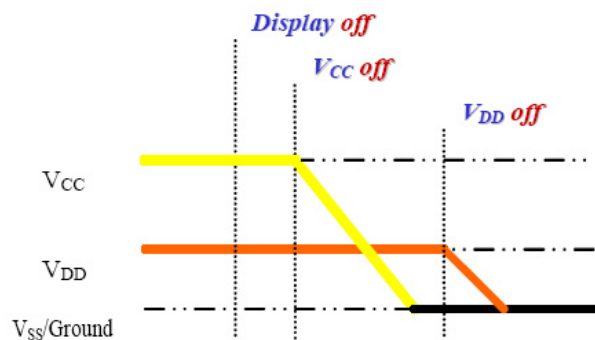
Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
(when V_{CC} is stable)
7. Send Display on command



Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
(when V_{CC} is reach 0 and
panel is completely
discharges)
4. Power down V_{DD}

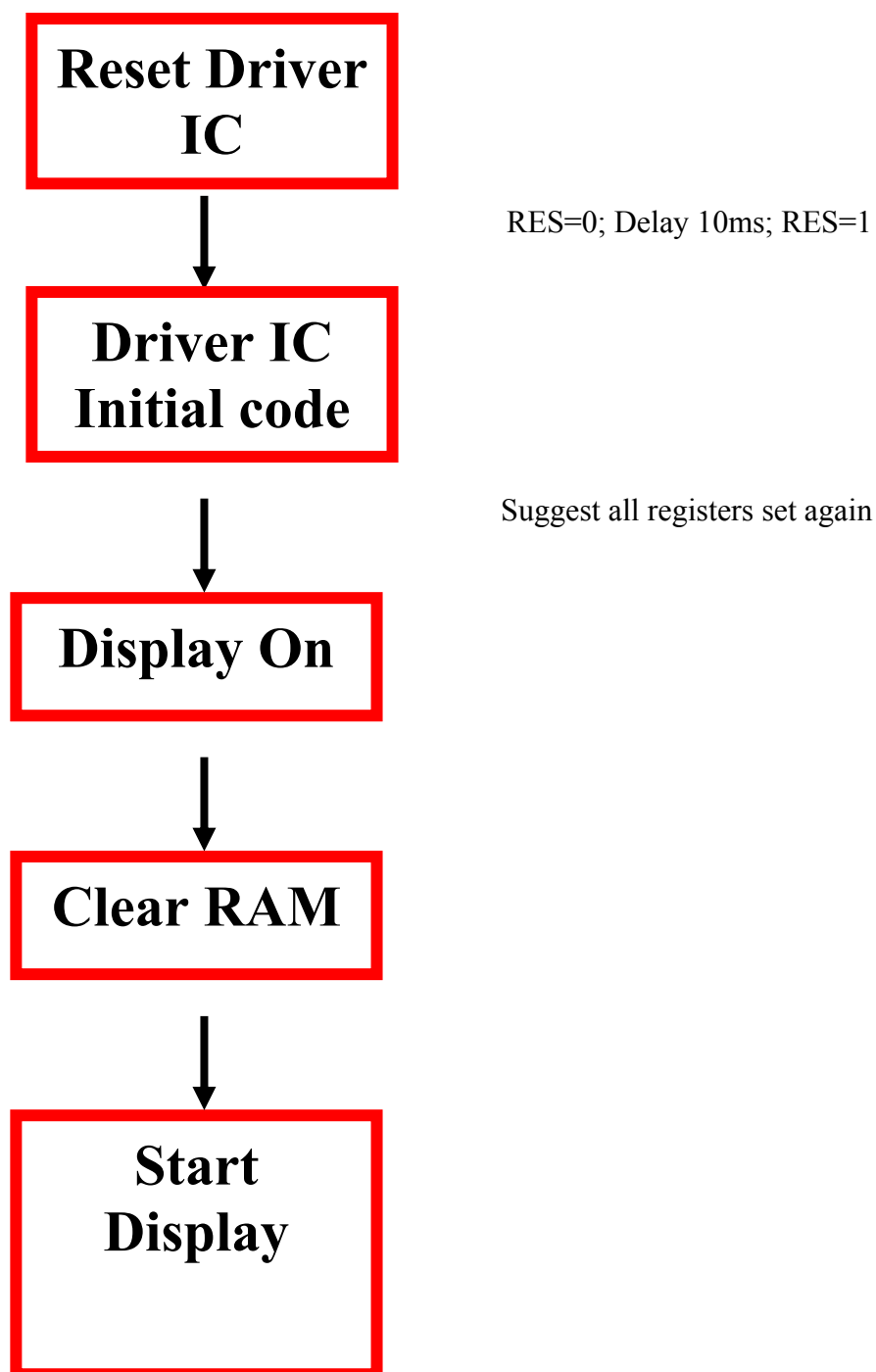


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6 How to use the DD-25664XX-3A-4A

Initial step flow



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6.1 Recommended Initial code

```

Set_Command_Lock(0x12);          // Unlock Basic Commands (0x12/0x16)
Set_Display_On_Off(0x00);        // Display Off (0x00/0x01)
Set_Display_Clock(0x91);         // Set Clock as 80 Frames/Sec
Set_Multiplex_Ratio(0x3F);       // 1/64 Duty (0x0F~0x3F)
Set_Display_Offset(0x00);        // Shift Mapping RAM Counter(0x00~0x3F)
Set_Start_Line(0x00);            // Set Mapping RAM Display Start Line
(0x00~0x7F)
Set_Remap_Format(0x14);          // Set Horizontal Address Increment
                                   // Column Address 0 Mapped to SEG0
                                   // Disable Nibble Remap
                                   // Scan from COM[N-1] to COM0
                                   // Disable COM Split Odd Even
                                   // Enable Dual COM Line Mode
Set_GPIO(0x00);                  // Disable GPIO Pins Input
Set_Function_Selection(0x01);    // Enable Internal VDD Regulator
Set_Display_Enhancement_A(0xA0,0xFD); // Enable External VSL
                                   // Set Low Gray Scale Enhancement
Set_Contrast_Current(0xDF);      // Set Segment Output Current
Set_Master_Current(Brightness);  // Set Scale Factor of Segment
Output Current Control
Set_Gray_Scale_Table();           // Set Pulse Width for Gray Scale Table
Set_Phase_Length(0xE8);          // Set Phase 1 as 17 Clocks & Phase 2
as 14 Clocks
Set_Display_Enhancement_B(0x20); // Enhance Driving Scheme Capability
(0x00/0x20)
Set_Precharge_Voltage(0x1F);     // Set Pre-Charge Voltage Level as
0.60*VCC
Set_Precharge_Period(0x08);      // Set Second Pre-Charge Period as 8
Clocks
Set_VCOMH(0x07);                 // Set Common Pins Deselect Voltage
Level as 0.86*VCC
Set_Display_Mode(0x02);           // Normal Display Mode
(0x00/0x01/0x02/0x03)
Set_Partial_Display(0x01,0x00,0x00); // Disable Partial Display

Fill_RAM(0x00);                   // Clear Screen

Set_Display_On_Off(0x01);         // Display On (0x00/0x01)

```

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