Supply Chain Explorer

By the Emerging Technology Observatory

This is an export from the ETO Supply Chain Explorer, available at: https://TBD.cset.tech You can see the web version of this content at https://TBD.cset.tech/?filter-choose=input-resource&input-resource=S3.

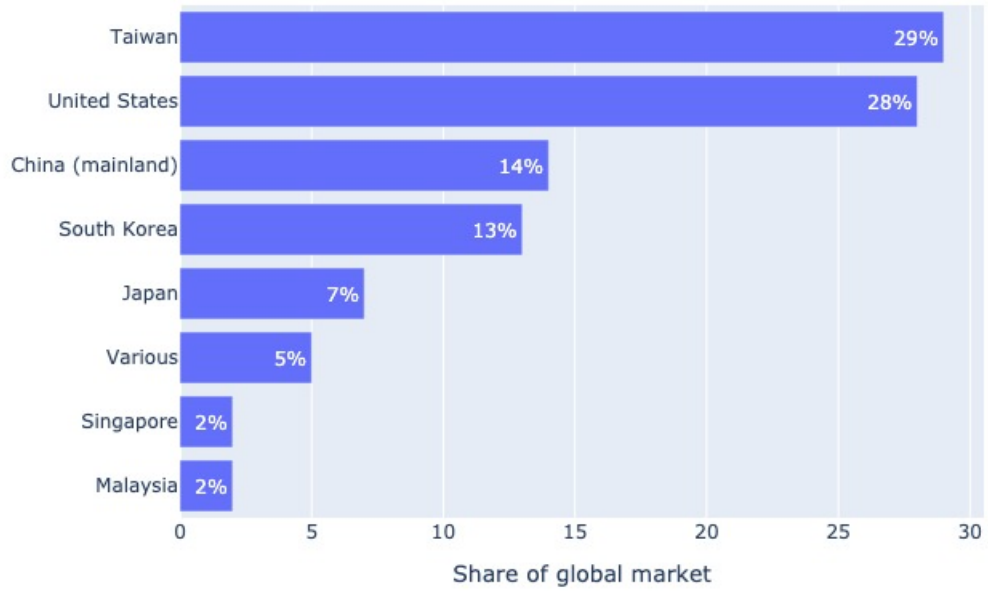
Assembly, testing, and packaging (ATP)

At the end of the fabrication process, the finished wafer contains dozens of chips in a grid pattern. During assembly, testing, and packaging, the wafer is separated into individual chips, or "dies." Each chip is mounted on a frame with wires that connect the chip to external devices, and enclosed in a protective casing. This produces the familiar look of a dark gray rectangle with metal pins at the edges. The chip is also tested to ensure it operates as intended.

Although ATP was historically low value, as transistor densities in logic chips have increased exponentially, packaging has increasingly become a bottleneck on chip performance.

ATP occurs under two business models: (1) as in-house ATP services performed by integrated device manufacturers (IDMs) and foundries after fabrication; and (2) by outsourced semiconductor assembly and test (OSAT) firms, which perform ATP for third-party customers. Firms headquartered in Taiwan, the United States, China, and South Korea are the main providers of ATP services.

Country provision



Notable supplier companies

- ASE - Taiwan
- Amkor - United States
- Intel - United States
- JCET - China (mainland)
- Micron - United States
- Powertech - Taiwan

- SK Hynix - South Korea
- Samsung - South Korea
- TSMC - Taiwan
- Tianshui Huatian Technology - China (mainland)
- TongFu - China (mainland)
- UTAC - Singapore