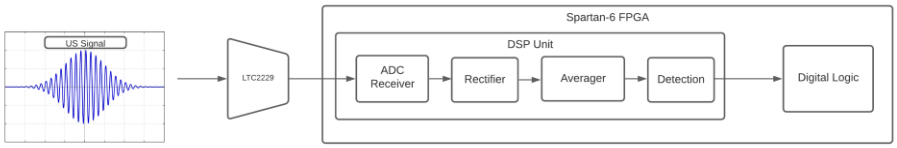
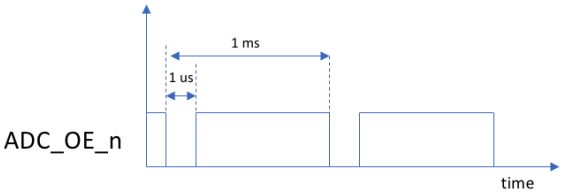
iota Biosciences Interview Question

System Overview:

You are tasked with developing the following DSP Unit as part of a system that detects foreign objects in the body. The system uses Xilinx's Spartan-6 FPGA to implement the DSP unit. The block diagram for the DSP unit is shown below.



The ultrasound signal is a 1.5 MHz differential signal sampled by the LTC2229 ADC at 32 Msps. The ADC is configured as a 2's complement output. The ADC is controlled by a module external to the FPGA that enables the ADC with the ADC_OE_n every 1 ms for a duration of 1 us and then disabled. Please see the timing diagram for the ADC_OE_n behavior below. The diagram is not to scale.



The DSP unit receives the data from the ADC, rectifies the signal, averages the rectified signal over the 1 us period that the ADC is enabled, and compares the average value to a variable threshold value. When the average output is equal to or greater than a variable, unsigned value, the DSP unit flags a signal declaring a foreign object has been detected. You are responsible for designing the DSP Unit using the Xilinx's Spartan-6 FPGA.

DSP Unit I/O Summary

Name	I/O	Description
CLK_100MHz	Input	100 MHz Clock Input
SRESET_n	Input	Active low synchronous reset
ADC_CLK	Input	32 MHz ADC Sample clock input generated off-chip
ADC_OE_n	Input	LTC2229 Enable bit
ADC_OF	Input	ADC Overflow Signal
ADC_DATA	Input	12-bit ADC Data Bus
DETECTION_THRESHOLD	Input	unsigned detection threshold input
DETECTED	Output	Object detected indicator

Sub-Module Summary:

- ADC Receiver: The ADC receiver handles the data coming in from the LTC2229 ADC by properly buffering the signals while the ADC is enabled as indicated by the input signal ADC_OE_n. The ADC signals (ADC_CLK, ADC_OE_n, ADC_OF, and ADC_DATA) are generated off-chip.
- Rectifier: The rectifier returns the absolute value of the incoming signal.
- Averager: The averager computes the average of the rectified signal for the duration of the ADC sample period of 1 us as indicated by the ADC_OE_n signal.
- Detection: The US Detection module outputs a logic high level if the average output is equal to or greater than a variable, unsigned value. If overflow was detected at any point during the valid signal period, the average value is invalid until the next ADC activation period.

Task:

Please design the RTL using verilog for the DSP unit described above for Xilinx's Spartan 6 FPGA. Design each submodule and connect the submodules in the top DSP Unit module.