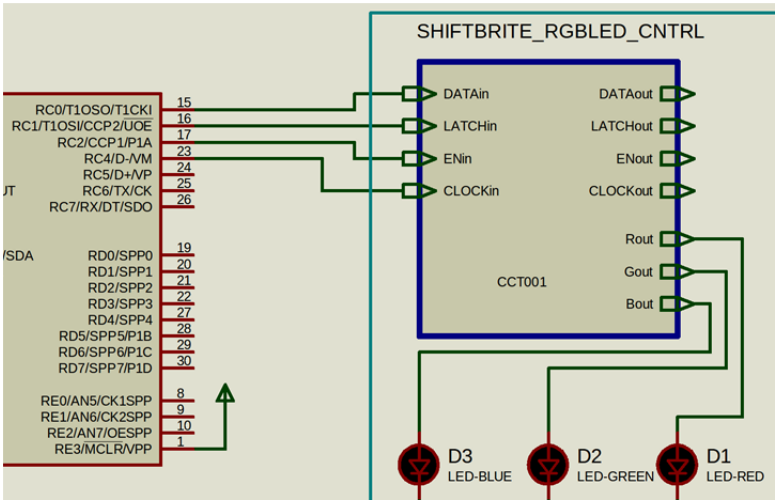
Computer Interfacing *Tercer Parcial*

9/1/2017 **Cognoms i Nom: _____ Doc. Identitat: _____**

Totes les respostes han d'estar degudament justificades. **Respostes sense un mínim text explicatiu no es tindran en consideració.**

1) En base a l'esquema de la figura, on es mostren les connexions realitzades entre el PIC18F i el controlador tipus SPI del LED RGB (A6281), contesteu els següents apartats: **(2 p.)**



a) Completeu les definicions següents:

```
#define DADES
#define CLOCK
#define LATCH
#define ENABLE
```

b) Completeu el codi adjunt per a que la subrutina Tx_Byte_SPI transmeti correctament un byte seguint el format de transmissió SPI.

```
void Tx_Byte_SPI (unsigned char b) {
  int j;
    for (j = 0; j < 8; j++) {
         DADES =  (b & 0x80) >>7;

         CLOCK = 0;
         __delay_ms(1);

                __delay_ms(1);
    }
}
```

c) Completeu el codi adjunt per a que la subrutina Activar_RGB_SPI activi el color passat per paràmetre.

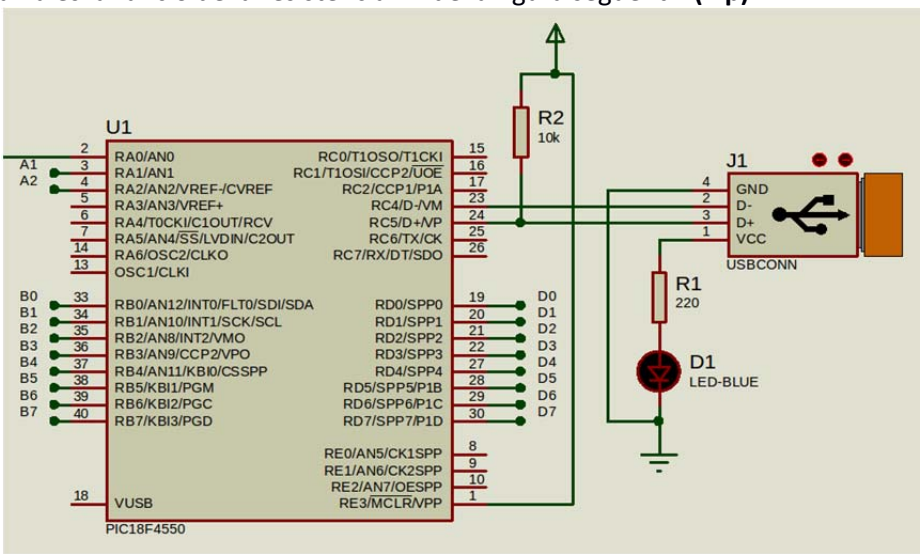
```
void  Activar_RGB_SPI (unsigned long color) {
    ENABLE = 0; // SLAVE SELECT
   Tx_byte_SPI  ( (BYTE)  (color>>16));

    Tx_byte_SPI  ( (BYTE)  (color>>8));

    Tx_byte_SPI  ( (BYTE)  (color>>0));

    __delay_ms(1);


    __delay_ms(1);
    ENABLE = 1;
}
```

d) En base al codi realitzat anteriorment i considerant que el temps d'execució del codi no és significatiu en front als retards (*delays*), quant de temps trigarà la subrutina en activar un color RGB?

e) En base al codi realitzat anteriorment, en quin ordre de significança es transmeten els bits en la subrutina Tx_byte_SPI(BYTE b)?

2) En un bus I2C, un Màster transmet un word (16 bits) de manera alternada a 3 esclaus a una velocitat d'100 kbps. Quina seria la velocitat de comunicació efectiva (en bps) entre el Màster i cadascun dels seus esclaus? **(1 p)**

3) En relació a les comunicacions USB, quina és la funció de la resistència R2 de la figura següent **(1 p)**



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4) En relació a les comunicacions USB en mode comunicacions Isòcrones FS (Full Speed), quina seria la mida d'un paquet de dades per a maximitzar la velocitat efectiva de comunicació, si el temps de frame (temps entre dos SOF) fos de 2 mseg? En respondre a la pregunta, no cal que la mida de les dades del paquet DATA0/1 sigui múltiple de 2.
Dades: Velocitat Full Speed= 12Mbps, Mida paquet IN/OUT= 35 bits, Mida paquet DATA0/1 = 34 bits + Dades,
Mida paquet ACK= 18 bits, Mida màxima de les dades d'un paquet DATA0/1= 1023 Bytes = 8184 bits. **(2 p)**

5) Configureu l'EUSART per a realitzar una comunicació asíncrona, a 57600 bauds, amb transmissió de 9 bits de dades. Indiqueu el valor dels bits dels registres TXSTA, RCSTA, BAUCON, SPBRGH i SPBRG. Fosc= 10 MHz (Inclogueu els càlculs necessaris, i justifiqueu la resposta). **(1,5 p)**

TABLE 20-1: BAUD RATE FORMULAS

Configuration Bits			BRG/EUSART Mode	Baud Rate Formula
SYNC	BRG16	BRGH		
0	0	0	8-bit/Asynchronous	Fosc/[64 (n + 1)]
0	0	1	8-bit/Asynchronous	Fosc/[16 (n + 1)]
0	1	0	16-bit/Asynchronous	
0	1	1	16-bit/Asynchronous	Fosc/[4 (n + 1)]
1	0	x	8-bit/Synchronous	
1	1	x	16-bit/Synchronous	

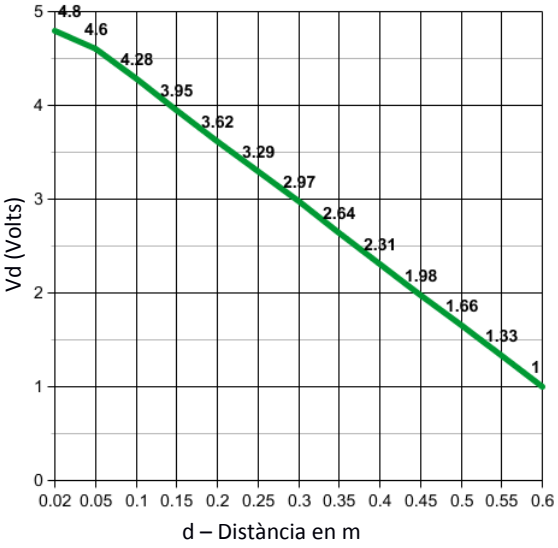
Legend: x = Don't care, n = value of SPBRGH:SPBRG register pair

6) Indiqueu damunt del següent cronograma d'una recepció d'un byte enviat per un dispositiu segons el protocol 1Wire, en quin moment el dispositiu Màster configura el seu pin 1Wire d'entrada o de sortida. **(1 p)**

7) Disposem d'un sensor que mesura la distància a un objecte, similar a l'utilitzat al laboratori. La relació tensió de sortida (**Vd**) en funció de la distància (**d**) es mostra a la figura adjunta.

Volem adquirir amb un PIC18F4550 (F_{OSC}= 1 MHz, V_{DD}=5V, V_{SS}=0V) la informació del sensor, que està connectat a l'entrada analògica 2, per a realitzar mesures en l'interval de 0,05 a 0,5 m, amb una resolució de 0,001 m., i 100 mostres/seg.

Indiqueu el nombre mínim de bits necessaris per l'ADC, i els valors dels registres ADCON0, ADCON1 i ADCON2 per a configurar el mòdul A/D amb un temps de conversió mínim. (Inclogueu els càlculs necessaris, i justifiqueu la resposta). **(1,5 p)**



ADCON0: A/D CONTROL REGISTER 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

0000 = Channel 0 (AN0); 0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2); 0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4); 0101 = Channel 5 (AN5)
0110 = Channel 6 (AN6); 0111 = Channel 7 (AN7)
1000 = Channel 8 (AN8); 1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10); 1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12); 1101 = Unimplemented
1110 = Unimplemented; 1111 = Unimplemented

bit 1 **GO/DONE:** A/D Conversion Status bit

When ADON = 1:
1 = A/D conversion in progress; 0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D converter module is enabled
0 = A/D converter module is disabled

ADCON1: A/D CONTROL REGISTER 1

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1**: Voltage reference Configutaion bit

1 = VREF- (AN2); 0 = Vss

bit 4 **VCFG0**: Voltage reference Configutaion bit

1 = VREF+ (AN2); 0 = V_{DD}

bit 3-0 **PCFG3:PCFG0:** A/D Port Configutaion Control bits

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7(2)	AN6(2)	AN5(2)	AN4	AN3	AN2	AN1	AN0
0000(1)	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111(1)	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

ADCON2: A/D CONTROL REGISTER 2

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified; 0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT2:ACQT0:** A/D Acquisition Time Select bits

111 = 20 TAD; 110 = 16 TAD
101 = 12 TAD; 100 = 8 TAD
011 = 6 TAD; 010 = 4 TAD
001 = 2 TAD; 000 = 0 TAD

bit 2-0 **ADCS2:ADCS0:** A/D Conversion Clock Select bits

111 = FRC (clock derived from A/D RC oscillator)
110 = FOSC/64; 101 = FOSC/16
100 = FOSC/4; 011 = FRC (clock derived from A/D RC oscillator)
010 = FOSC/32; 001 = FOSC/8
000 = FOSC/2

TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

bit 7 **CSRC**: Clock Source Select bit

Asynchronous mode: Don't care.
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9**: 9-Bit Transmit Enable bit

1 = Selects 9-bit transmission; 0 = Selects 8-bit transmission

bit 5 **TXEN**: Transmit Enable bit

1 = Transmit enabled; 0 = Transmit disabled

bit 4 **SYNC**: EUSART Mode Select bit

1 = Synchronous mode; 0 = Asynchronous mode

bit 3 **SENDB**: Send Break Character bit

Asynchronous mode:
1 = Send Sync Break on next transmission
0 = Sync Break transmission completed
Synchronous mode: Don't care.

bit 2 **BRGH**: High Baud Rate Select bit

Asynchronous mode:
1 = High speed; 0 = Low speed
Synchronous mode: Unused in this mode.

bit 1 **TRMT**: Transmit Shift Register Status bit

1 = TSR empty; 0 = TSR full

bit 0 **TX9D**: 9th bit of Transmit Data

Can be address/data bit or a parity bit.

RCSTA: RECEIVE STATUS AND CONTROL REGISTER

bit 7 **SPEN:** Serial Port Enable bit

1 = Serial port enabled
0 = Serial port disabled

bit 6 **RX9:** 9-Bit Receive Enable bit

1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5 **SREN:** Single Receive Enable bit

Asynchronous mode: Don't care.
Synchronous mode – Master:
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.
Synchronous mode – Slave: Don't care.

bit 4 **CREN:** Continuous Receive Enable bit

Asynchronous mode:
1 = Enables receiver
0 = Disables receiver
Synchronous mode:
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

bit 3 **ADDEN:** Address Detect Enable bit

Asynchronous mode 9-bit (RX9 = 1):
1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set
0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
Asynchronous mode 8-bit (RX9 = 0): Don't care.

bit 2 **FERR:** Framing Error bit

1 = Framing error (can be updated by reading RCREG register and receiving next valid byte)
0 = No framing error

bit 1 **OERR:** Overrun Error bit

1 = Overrun error (can be cleared by clearing bit CREN)
0 = No overrun error

bit 0 **RX9D:** 9th bit of Received Data

This can be address/data bit or a parity bit and must be calculated by user firmware.

BAUCON: BAUD RATE CONTROL REGISTER

bit 7 **ABDOVF**: Auto-Baud Acquisition Rollover Status bit

1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL**: Receive Operation Idle Status bit

1 = Receive operation is Idle
0 = Receive operation is active

bit 5 **RXDTP**: Received Data Polarity Select bit

Asynchronous mode:
1 = RX data is inverted
0 = RX data received is not inverted
Synchronous modes:
1 = Received Data (DT) is inverted. Idle state is a low level.
0 = No inversion of Data (DT). Idle state is a high level.

bit 4 **TXCKP**: Clock and Data Polarity Select bit

Asynchronous mode:
1 = TX data is inverted
0 = TX data is not inverted
Synchronous modes:
1 = Clock (CK) is inverted. Idle state is a high level.
0 = No inversion of Clock (CK). Idle state is a low level.

bit 3 **BRG16:** 16-Bit Baud Rate Register Enable bit

1 = 16-bit Baud Rate Generator – SPBRGH and SPBRG
0 = 8-bit Baud Rate Generator – SPBRG only (Compatible mode), SPBRGH value ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit

Asynchronous mode:
1 = EUSART will continue to sample the RX pin – interrupt generated on falling edge; bit cleared in hardware on following rising edge
0 = RX pin not monitored or rising edge detected
Synchronous mode: Unused in this mode.

bit 0 **ABDEN**: Auto-Baud Detect Enable bit

Asynchronous mode:
1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.
0 = Baud rate measurement disabled or completed
Synchronous mode: Unused in this mode.