CAMPUS VIRTUAL UPC / Les meves assignatures / 2021/22-01:FIB-270020-CUTotal / Unit 3.1: Introduction to parallel architectures I / Questions after video lesson 4 (parts 1 and 2) Començat el dimecres, 13 d'octubre 2021, 17:16 Estat Acabat Completat el dimecres, 13 d'octubre 2021, 17:16 Temps emprat 17 segons **Qualificació 2,00** sobre 2,00 (**100**%) Pregunta 1 Correcte Puntuació 1,00 sobre 1,00 Assume a system with two processors (cores) in a centralized memory system, each one with a private private cache (write-allocate and writeback policies) executing the following code sequences: CORE1 a = 1;while (a==1); a = 1;printf("Done 1!"); CORE2 a = 0;while (a==0); a = 0;printf("Done 2!"); In a non-coherent system, which one the following outputs would be possible (choose as many as possible): Trieu-ne una o més: Done1! Done2! Done2! Done1! Done1! Done2! When evaluating the condition in the while loop on a non-coherent system Nothing printed each core would retrieve the value that it has written in its own cache in the initial assignment. Therefore, both would get into an infinite loop. La teva resposta és correcta. Pregunta 2 Correcte Puntuació 1,00 sobre 1,00

However, if the system is coherent, which of the following outputs would be possible? (choose as many as possible)

Trieu-ne una o més:

■ Done1! Done2! ✓ Coherence will make changes visible to both cores. Therefore both

Done2! Done1!	~	Coherence will make changes visible to both cores. Therefore both cores will exit the loop at some point. The order cannot be determined though.
Done1!		
Done2!		
□ Nothing printed		
La teva resposta és correcta.		
→ Video lesson 4 (part 2): cache coherence problem		
Salta a		

Video lesson 4 (part 3): how to get coherence? ►

cores will exit the loop at some point. The order cannot be

determined though.