Començat el	dimecres, 24 de novembre 2021, 16:39
Estat	Acabat
Completat el	dimecres, 24 de novembre 2021, 16:47
Temps emprat	7 minuts 59 segons
Punts	3,00/10,00
Qualificació	**1,80** sobre 6,00 (**30**%)

Pregunta **1**

Incorrecte

Puntuació 0,00 sobre 1,00

In a NUMA (Non-Uniform Memory Access time) multiprocessor there are two or more identical (NUMA) nodes, each one with a processor and its complete memory hierarchy, including a portion of main memory. The overall memory of the system is physically distributed among all the nodes but logically shared by all of them (i.e., the processor in any node can access to its main memory and also to any memory location in any other node through the interconnection network).

Which of the following statements are true?

A given physical memory address can only be stored in the memory of a single node, although multiple copies of the line containing that address may be temporarily stored in the cache memories of other nodes.

Trieu-ne una:

- Vertader
- Fals ✖

In NUMA systems there is a unique address space shared by all the NUMA nodes; however, for multiprocessor scalability reasons the memory is physically distributed among the different NUMA nodes.

Pregunta **2**

Incorrecte

Puntuació 0,00 sobre 1,00

In a NUMA system, instructions different from the conventional load and store are required to access to variables stored in other nodes.

Trieu-ne una:

- Vertader ✖
- Fals

The only instructions that are used to perform memory accesses are load and store (i.e. PrRd and PrWr).

Pregunta **3**

Incorrecte

Puntuació 0,00 sobre 1,00

The way data is distributed among the different nodes of a NUMA multiprocessor system ...

Trieu-ne una:

Trieu-ne una:

- ... does not have any impact in the performance of the parallel application.
- ... is determined by the operating system based on a given data allocation policy (for example, first touch).
- ... dynamically changes with the objective of balancing the number of local accesses that are performed by the processors in the different NUMA nodes. ✖ In the architecture explained in class, once a given policy is applied (for example, first touch) the data allocation does not change during program execution.
- ... is statically determined by the compiler, based on the accesses that are performed by the tasks in the parallel program.

La teva resposta és incorrecta.

Pregunta **4**

Incorrecte

Puntuació 0,00 sobre 1,00

Assume that the coherence in a NUMA multiprocessor is based on a directory attached to the main memory in each node. The directory structure present in each node provides ...

Trieu-ne una:

- ... coherence information for the memory lines that are stored in the cache memory of the same node.
- ... information that allows a processor to find the data that is allocated in other nodes. ✖ The directory structure provides information to keep memory coherent (i.e. keep coherence among the multiple copies of each memory line). Finding where the data is allocated in the system is not the purpose of the directory.
- ... information to keep coherent all possible copies in cache of the lines stored in the memory of that node.
- ... information that allows a processor in that node to find the nearest node where to find a given memory address, in order to minimize the memory access time.

La teva resposta és incorrecta.

Pregunta **5**

Correcte

Puntuació 1,00 sobre 1,00

In a NUMA multiprocessor system, with directory-based coherence protocol, the number of bits in each entry of the directory depends on the number of nodes in the system, with one or several additional bits to keep the state of the associated line.

Trieu-ne una:

- Vertader ✔
- Fals

Well done! Remember that the protocol explained in class assumes three states (MSU, being U uncached), so 2 bits for the state; the protocol explained in a previous video lesson assumes a single D (dirty) bit to keep the state.

Pregunta **6**

Incorrecte

Puntuació 0,00 sobre 1,00

The number of entries in the directory of a NUMA node ...

Trieu-ne una:

- ... is the total number of cache lines in the overall NUMA system, helping to identify which caches have a copy of a memory line

... is the total number of cache lines in the overall NUMA system, helping to identify which caches have a copy of a memory line.

... is determined by the maximum number of copies that are allowed for each line in main memory.

... is the number of lines that are stored in the main memory associated to it.

... depends on the number of NUMA nodes in the system in order to implement the list of nodes with remote copies.

✖ The information required to implement the directory-based coherence protocol is centralised for each existing memory line and only allocated next to it. The number of entries in the directory is equal to the number of lines stored in its associated memory, one directory entry per memory line.

La teva resposta és incorrecta.

Pregunta **7**

Correcte

Puntuació 1,00 sobre 1,00

Assume a NUMA multiprocessor architecture with 1024 nodes, each node with a single processor and 24 GB of main memory, with directory-based MSU coherence protocol; memory lines are 128 bytes wide. In that system, which is the percentage of the whole main memory (**including both data and directory**) that is used by the directory to store all the information related to coherence?

Trieu-ne una:

With the information provided one can not compute the number. You should have provided the size of the cache memory in each node to be able to compute the requested percentage.

close to 200%

close to 50%

✔ Well done. For each line one needs 128 bytes (i.e. 1024 bits) for data and (1024+2) bits for the directory entry.

close to 100%

La teva resposta és correcta.

Pregunta **8**

Correcte

Puntuació 1,00 sobre 1,00

False sharing cannot occur across nodes in a NUMA multiprocessor architecture because the directory structure attached to main memory provides information about the location of each variable in the same line.

Trieu-ne una:

Vertader

Fals ✔

Well done! False sharing simply occurs by the fact of having multiple variables residing in the same line.

Pregunta **9**

Incorrecte

Puntuació 0,00 sobre 1,00

In a NUMA multiprocessor architecture, false sharing implies the simultaneous existence of at least two copies of the same cache line in M state in the associated directory entry.

Trieu-ne una:

Vertader ✖

Fals

There cannot co-exist in the system two copies of the same cache line in M state. The M state implies a single dirty copy of the line in the whole system.

Pregunta **10**

Incorrecte

Puntuació 0,00 sobre 1,00

Two different processors in a cache-coherent multiprocessor architecture (either UMA or NUMA) continuously executing a count++ instruction originate a false sharing situation.

Trieu-ne una:

Vertader ✖

Fals

Since the two processors are accessing the same variable to modify it, there is no false sharing; in fact this is a clear situation of true sharing.

◄ Notes for video lesson 5

Salta a...

NUMA coherence quizz (2) ►