CAMPUS VIRTUAL UPC / Les meves assignatures / 2021/22-01:FIB-270020-CUTotal / Unit 3.1: Introduction to parallel architectures I / Questions after video lesson 4 (part 4)

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Estat Acabat

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Temps emprat 3 minuts 5 segons

Qualificació 1,00 sobre 1,00 (100%)

Pregunta 1

Correcte

Puntuació 1,00 sobre 1,00

Assume a shared-memory multiprocessor system implementing a write-update coherence mechanism in which processors perform memory accesses in the following temporal order:

COREO reads variable A (gets a value of 6 from main memory)

CORE1 reads variable A

CORE2 writes 17 into variable A

CORE3 reads variable A

After that sequence, which of the following answers is true?:

Trieu-ne una:

- Only CORE2 and CORE3 have value 17 in their cache memories
- Only CORE2 has value 17 in cache memory, the other cores have value 6 in their cache memories
- All cores have value 17 in their respective cache memories

✓ Well done!

With a Write-update mechanism the processor that writes broadcasts the new value and forces all others to update their copies

All cores have the original value 6 in their respective caches

La teva resposta és correcta.

▼ Video lesson 4 (part 4): write-update snooping coherence

Salta a...

Video lesson 4 (part 5): write-invalidate snooping coherence ►