Començat el	dimecres, 13 d'octubre 2021, 17:38
Estat	Acabat
Completat el	dimecres, 13 d'octubre 2021, 17:41
Temps emprat	2 minuts 50 segons
Qualificació	**1,00** sobre 1,00 (**100**%)

Pregunta **1**

Correcte

Puntuació 1,00 sobre 1,00

Assume a shared-memory multiprocessor system implementing a write-invalidate coherence mechanism in which processors perform memory accesses in the following temporal order:

CORE0 reads variable A (gets a value of 6 from main memory)

CORE1 reads variable A

CORE2 writes 17 into variable A

CORE3 reads variable A

After that sequence, which of the following answers are true? (choose as many as you think are true):

Trieu-ne una o més:

- [x] Both CORE2 and CORE3 have value 17 in their respective cache memories
  - ✔ This one is correct since CORE3 reads the new value from the cache in CORE2, the only place where variable A is valid.
- [ ] CORE0 and CORE1 have value 6 in their respective caches as VALID
- [x] CORE0 and CORE1 have the entry for variable A marked as INVALID ✔
  - This one is correct since with write-invalidate the writing processor (CORE2) forces all others (CORE 0 and 1) to invalidate their copies, so a future access to the variable will result in a miss.
- [ ] Since the system is coherent, all cores have value 17 in their respective caches

La teva resposta és correcta.

◄ Video lesson 4 (part 5): write-invalidate snooping coherence

Salta a...

Additional material ►